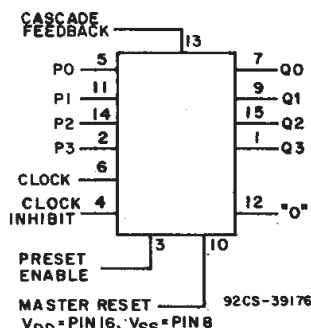


**NOT
RECOMMENDED FOR
NEW DESIGNS**

CD4522B Types

Advance Information/
Preliminary Data



FUNCTIONAL DIAGRAM

CMOS Programmable BCD Divide-by-"N" Counter

High-Voltage Types (20-Volt Rating)

Features:

- Internally synchronous for high internal and external speeds.
- Logic edge-clocked design — increments on positive Clock transition or on negative Clock Inhibit transition.
- 100% tested for quiescent current at 20-V.
- 5-V, 10-V, and 15-V parametric ratings.

- Standard symmetrical output characteristics.
- Maximum input current of 1 μ A at 18 V over full package-temperature range: 100 nA at 18 V and 25°C.
- Meets all requirements of JEDEC Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices."

■ CD4522B programmable BCD counter has a decoded "0" state output for divide-by-N applications. In single stage operation the "0" output is tied to the Preset Enable input. The Cascade Feedback allows multiple stage divide-by-N operation without the need for external gating. A HIGH on the Clock Inhibit disables the pulse-counting function. A HIGH on the Master Reset asynchronously resets the divide-by-N operation. The output is presented in BCD format.

Applications:

- Frequency synthesizers
- Phase-locked loops
- Programmable down counters
- Programmable frequency dividers

The CD4522B-series types are supplied in 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal) -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to $V_{DD} + 0.5V$

DC INPUT CURRENT, ANY ONE INPUT $\pm 10mA$

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -55^\circ C$ to $+100^\circ C$ 500mW

For $T_A = +100^\circ C$ to $+125^\circ C$ Derate Linearly at 12mW/ $^\circ C$ to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW

OPERATING-TEMPERATURE RANGE (T_A) $-55^\circ C$ to $+125^\circ C$

STORAGE TEMPERATURE RANGE (T_{stg}) $-65^\circ C$ to $+150^\circ C$

LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ inch ($1.59 \pm 0.79mm$) from case for 10s max $+265^\circ C$

3
COMMERCIAL CMOS
HIGH VOLTAGE ICs

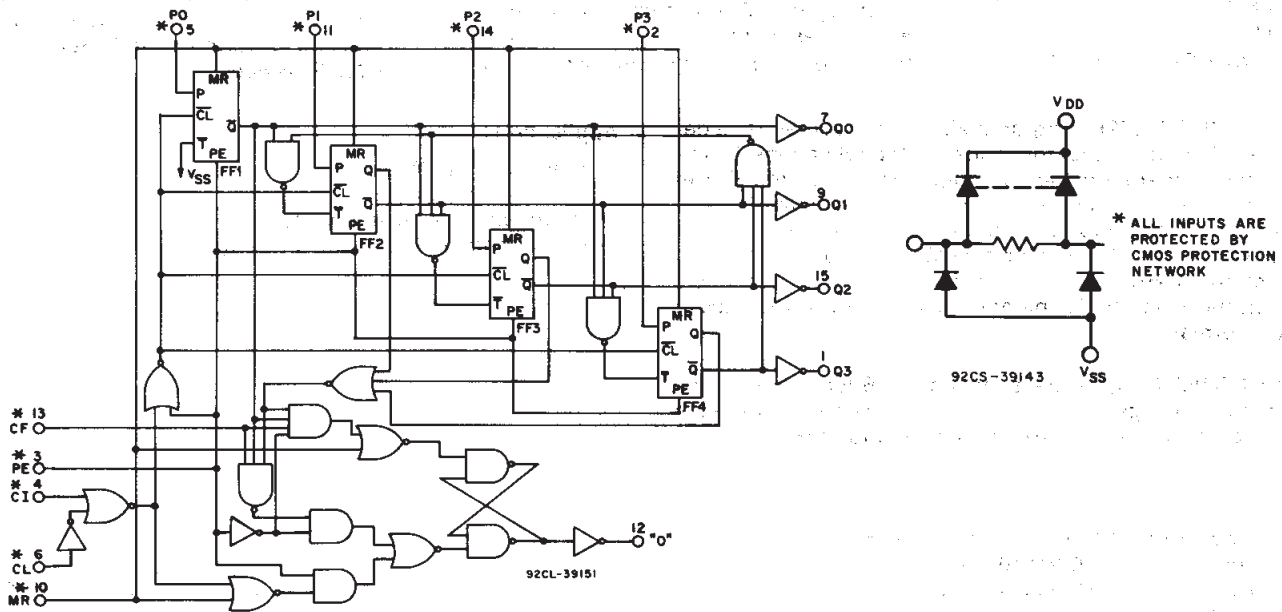
CD4522B Types

TRUTH TABLES

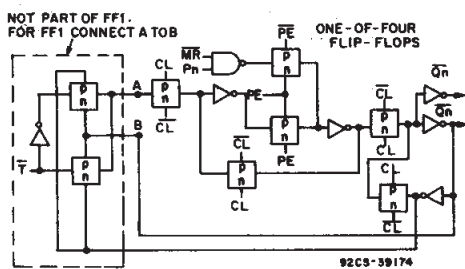
CLOCK	CLOCK INHIBIT	PRESET ENABLE	MASTER RESET	ACTION
0	0	0	0	No Count
1	0	0	0	Count Down
X	1	0	0	No Count
1	1	0	0	Count Down
X	X	1	0	Preset
X	X	X	1	Reset

X = Don't Care

Count	OUTPUTS			
	Q ₀	Q ₁	Q ₂	Q ₃
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1



a. Basic diagram.



b. Flip-flop detail.

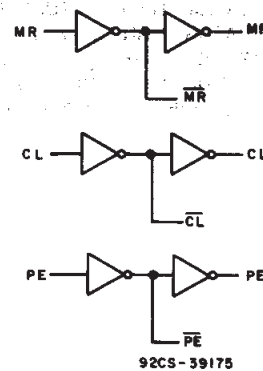


Fig. 1 - Logic diagram for the CD4522B.

CD4522B Types

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$, except as noted.

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	V_{DD} (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	18	V
Pulse Width:	5	250	—	ns
	10	100	—	
	15	80	—	
Clock, $t_{w(cc)}$	5	250	—	ns
	10	100	—	
	15	80	—	
Preset Enable, $t_{w(cc)}$	5	250	—	ns
	10	100	—	
	15	80	—	
Master Reset, $t_{w(MR)}$	5	350	—	ns
	10	250	—	
	15	200	—	
Clock Frequency, f_{CL}	5	—	1.5	MHz
	10	—	3.0	
	15	—	4.0	
Clock Rise and Fall Time t_{rCL} , t_{fCL}	5	—	15	μs
	10	—	15	
	15	—	15	
Preset Enable Set-up Time, t_{su}	5	0	—	ns
	10	0	—	
	15	0	—	
Preset Enable Hold Time, t_h	5	75	—	ns
	10	25	—	
	15	20	—	
Master Reset Removal Time, t_{rem}	5	130	—	ns
	10	50	—	
	15	30	—	

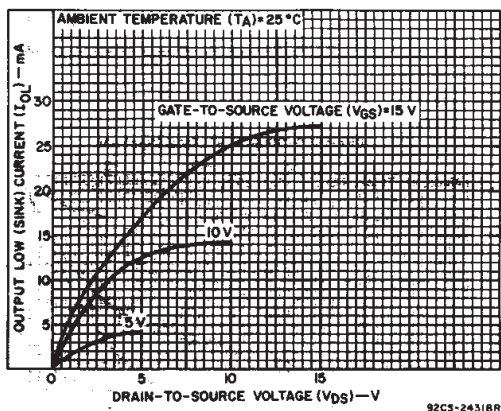


Fig. 2 — Typical output low (sink) current characteristics.

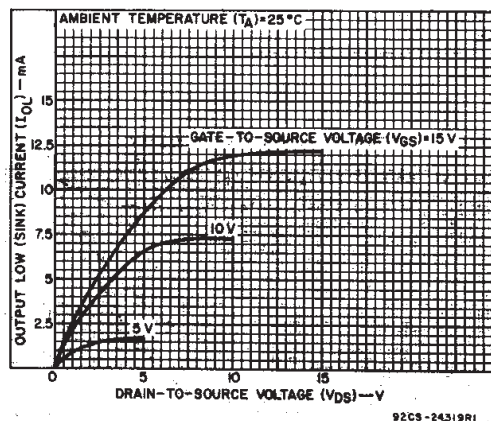


Fig. 3 — Minimum output low (sink) current characteristics.

CD4522B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTER- ISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)					+25			
				-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I _{DD} Max.	—	0, 5	5	5	5	150	150	—	0.04	5	μA
	—	0, 10	10	10	10	300	300	—	0.04	10	
	—	0, 15	15	20	20	600	600	—	0.04	20	
	—	0, 20	20	100	100	3000	3000	—	0.08	100	
Output Low (Sink) Current I _{OL} Min.	0.4	0, 5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0, 10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0, 15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I _{OH} Min.	4.6	0, 5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	
	2.5	0, 5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0, 10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
13.5	0, 15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—		
Output Voltage: Low-Level, V _{OL} Max.	—	0, 5	5	0.05				—	0	0.05	V
	—	0, 10	10	0.05				—	0	0.05	
	—	0, 15	15	0.05				—	0	0.05	
Output Voltage: High-Level V _{OH} Min.	—	0, 5	5	4.95				4.95	5	—	
	—	0, 10	10	9.95				9.95	10	—	
	—	0, 15	15	14.95				14.95	15	—	
Input low Voltage, V _{IL} Max.	0.5, 4.5	—	5	1.5				—	—	1.5	
	1, 9	—	10	3				—	—	3	
	1.5, 13.5	—	15	4				—	—	4	
Input High Voltage, V _{IH} Min.	0.5, 4.5	—	5	3.5				3.5	—	—	
	1, 9	—	10	7				7	—	—	
	1.5, 13.5	—	15	11				11	—	—	
Input Current, I _{IN} Max.	—	0, 18	18	±0.1	±0.1	±1	±1	—	±10 ⁻⁵	±0.1	μA

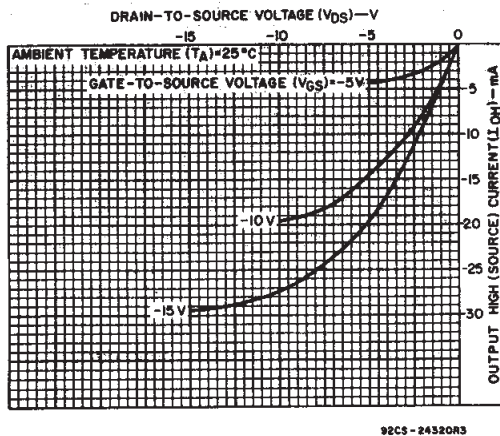


Fig. 4 — Typical output high (source) current characteristics.

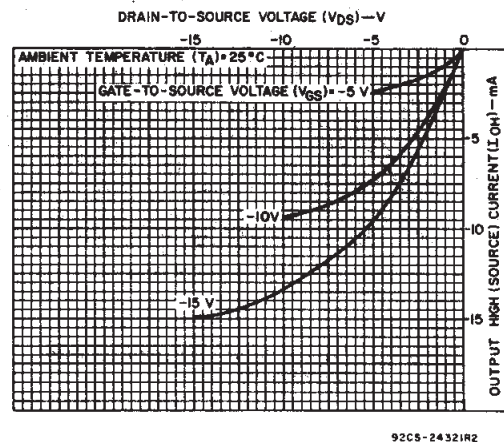


Fig. 5 — Minimum output high (source) current characteristics.

CD4522B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20\text{ ns}$, $C_i = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		V_{DD} (V)	Min.	Typ.	Max.
Propagation Delay Time; t_{PHL}, t_{PLH} : Clock to "Q" outputs		5	—	550	1100
		10	—	225	450
		15	—	160	320
Clock to "0" output		5	—	420	710
		10	—	160	270
		15	—	110	190
Clock inhibit to "Q" outputs		5	—	270	540
		10	—	100	200
		15	—	70	140
Master reset to "Q" outputs		5	—	270	540
		10	—	100	200
		15	—	70	140
Preset Enable Setup Time, t_{su}		5	—	0	0
		10	—	0	0
		15	—	0	0
Preset Enable Hold Time, t_h		5	—	75	150
		10	—	25	50
		15	—	20	40
Master Reset Removal Time, t_{rem}		5	—	130	260
		10	—	50	100
		15	—	30	60
Transition Time, t_{THL}, t_{TLH}		5	—	100	200
		10	—	50	100
		15	—	40	80
Minimum Pulse Width Clock, t_{WICL}		5	—	125	250
		10	—	50	100
		15	—	40	80
Preset Enable, t_{WPE}		5	—	125	250
		10	—	50	100
		15	—	40	80
Master Reset, t_{WMR}		5	—	175	350
		10	—	125	250
		15	—	100	200
Max Clock Freq, f_{CL}		5	—	3	1.5
		10	—	6	3.0
		15	—	8	4.0
Max Clock or Clock Inhibit Rise & Fall Time, t_{TLH}, t_{THL}		5	—	—	15
		10	—	—	15
		15	—	—	15
Input Capacitance, C_{IN}	Any Input		—	5	7.5
					pF

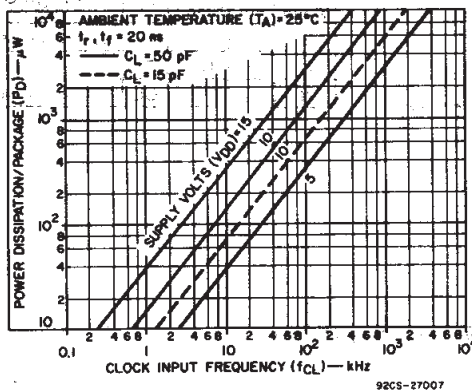
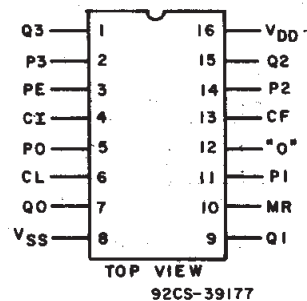


Fig. 6 — Typical dynamic power dissipation vs. frequency.



TERMINAL ASSIGNMENT

CD4522B Types

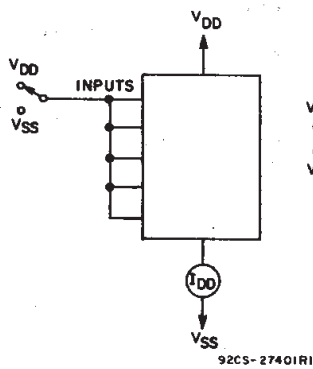


Fig. 7 — Quiescent device current test circuit.

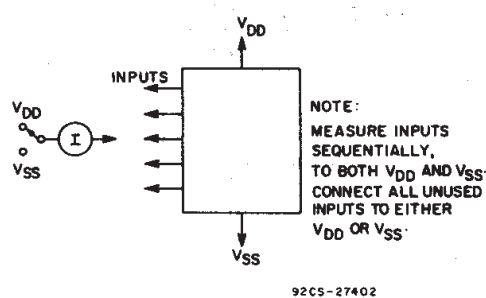


Fig. 8 — Input current test circuit.

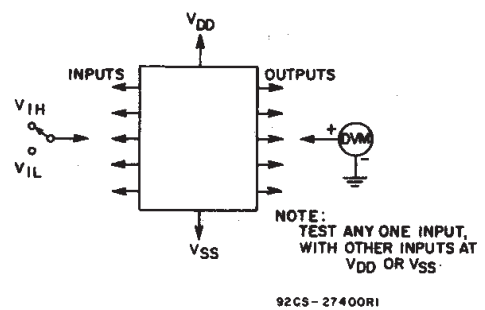


Fig. 9 — Input voltage test circuit.

APPLICATION CIRCUITS

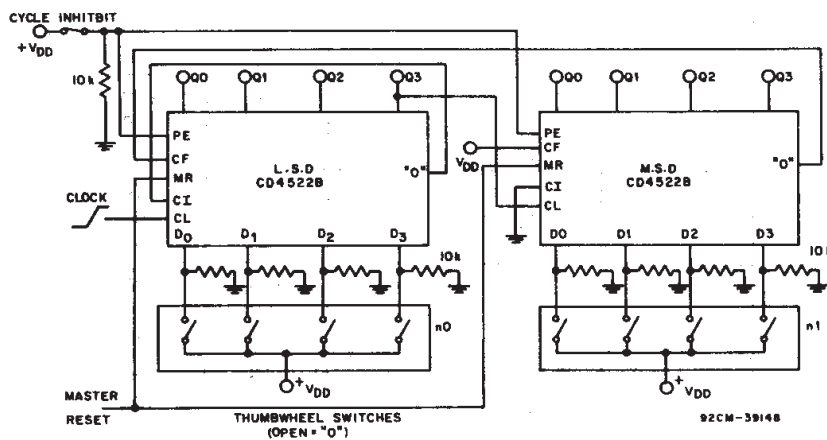


Fig. 10 — 2-Stage Programmable Down Counter (One Cycle)

From Stage	To Pin	From Stage	To Pin	Range of N
LSD	"0"	All	PE	$LSD < N < MSD$
N	"0"	N-1	CF	$LSD + 1 < N < MSD$
N	"0"	N+1	CL	$LSD < N < MSD-1$

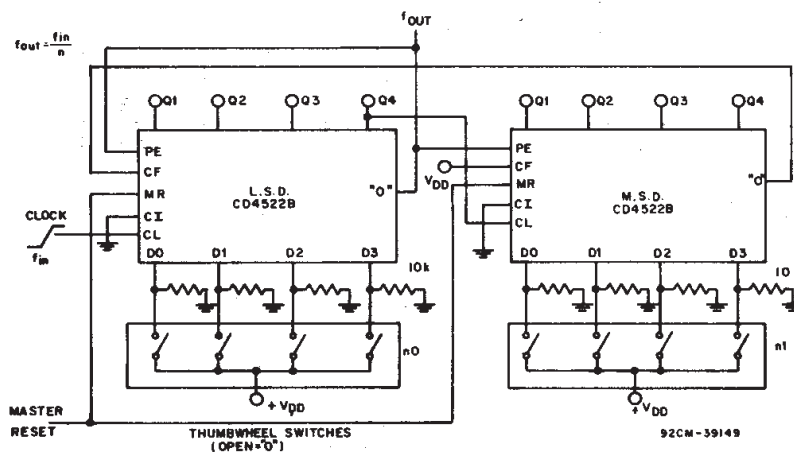
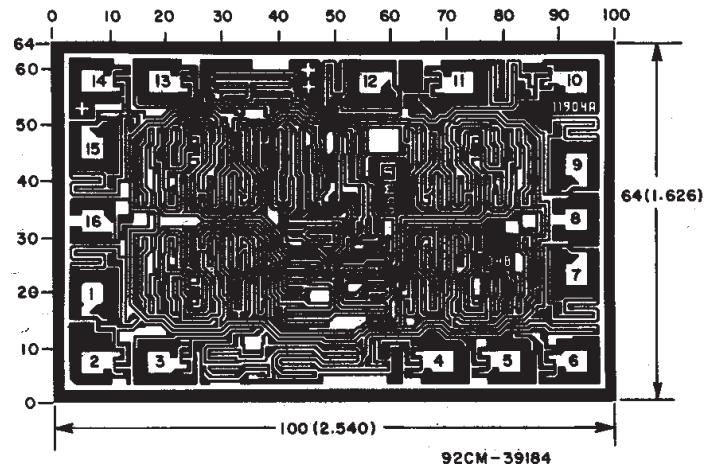


Fig. 11 — 2-Stage Programmable Frequency Divider

From Stage	To Pin	From Stage	To Pin	Range of N
LSD	"0"	All	PE	$LSD < N < MSD$
N	"0"	N-1	CF	$LSD + 1 < N < MSD$
N	"0"	N+1	CL	$LSD < N < MSD-1$

CD4522B Types



Dimensions and pad layout for CD4522BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD4522BE	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4522BE
CD4522BE.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4522BE
CD4522BM	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4522BM
CD4522BM.A	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4522BM
CD4522BMT	Active	Production	SOIC (D) 16	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4522BM
CD4522BMT.A	Active	Production	SOIC (D) 16	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4522BM
CD4522BPW	Active	Production	TSSOP (PW) 16	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM522B
CD4522BPW.A	Active	Production	TSSOP (PW) 16	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM522B

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD4522BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4522BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4522BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD4522BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD4522BM	D	SOIC	16	40	507	8	3940	4.32
CD4522BM.A	D	SOIC	16	40	507	8	3940	4.32
CD4522BPW	PW	TSSOP	16	90	530	10.2	3600	3.5
CD4522BPW.A	PW	TSSOP	16	90	530	10.2	3600	3.5

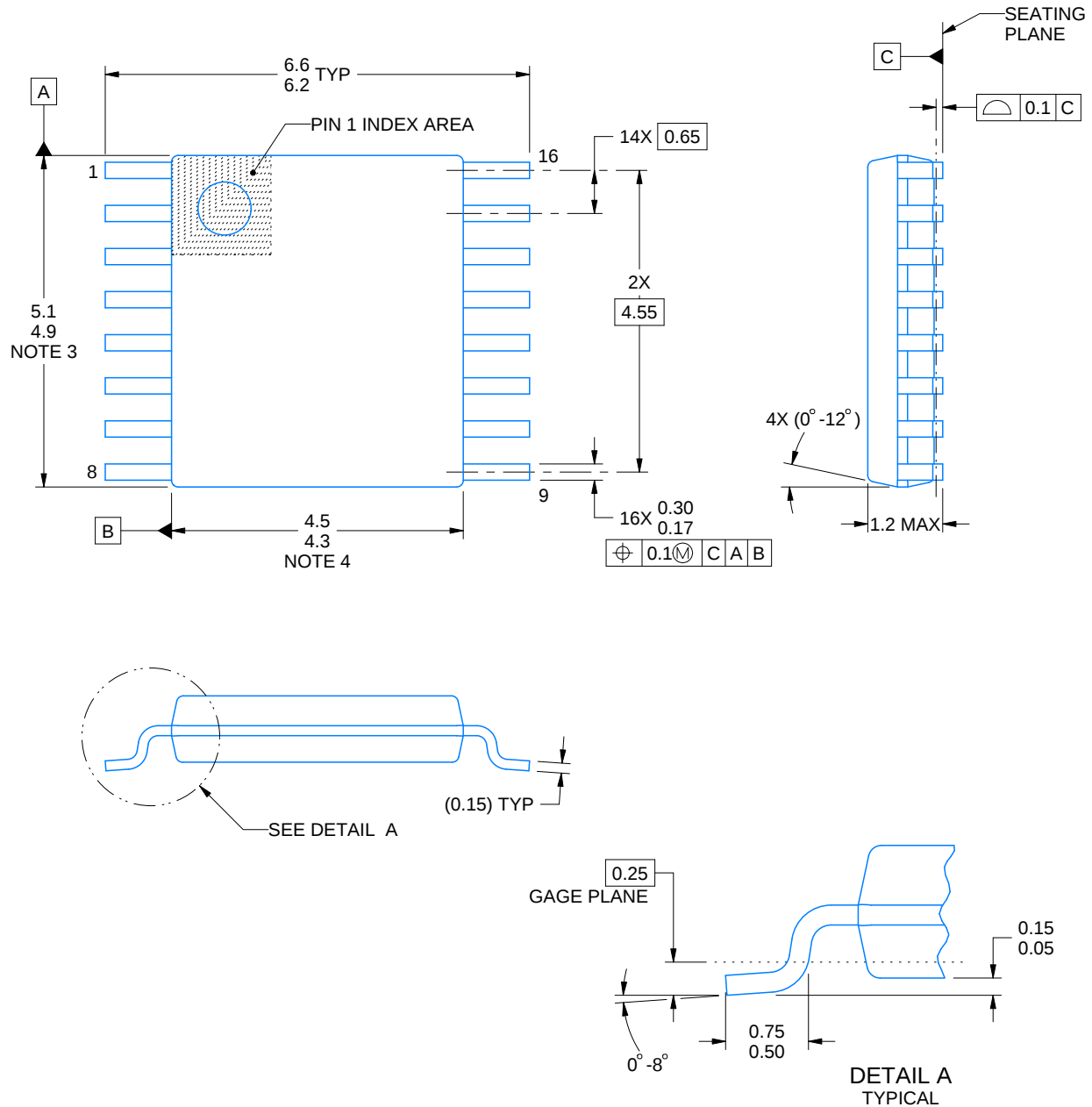
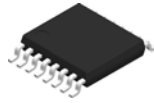
D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



4220204/B 12/2023

NOTES:

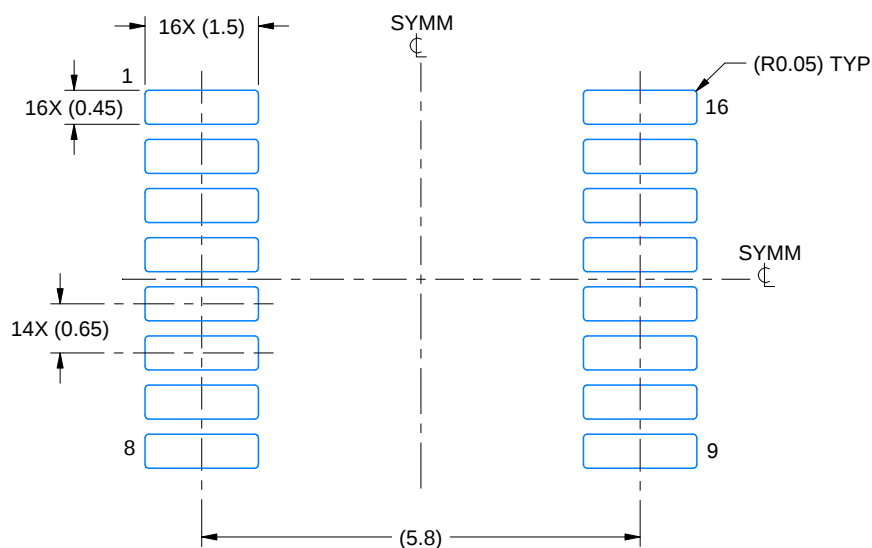
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

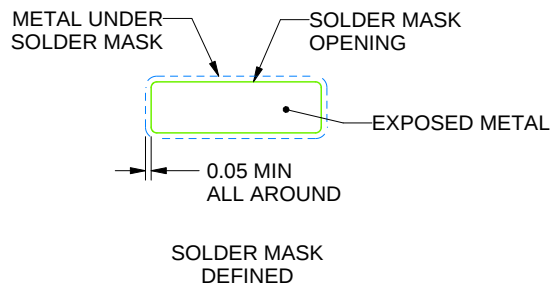
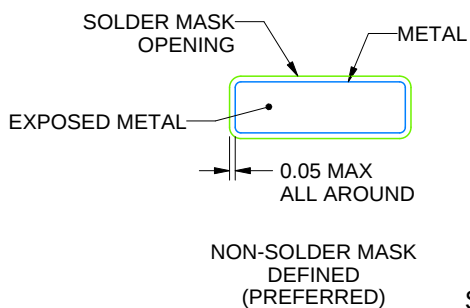
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

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