

CDx4ACT138 3-Line to 8-Line Decoders/Demultiplexers

1 Features

- Inputs are TTL-voltage compatible
- Speed of bipolar F, AS, and S, with significantly reduced power consumption
- Designed specifically for high-speed memory decoders and data-transmission systems
- Incorporate three enable inputs to simplify cascading and/or data reception
- Balanced propagation delays
- $\pm 24\text{mA}$ output drive current
 - Fanout to 15 F devices
- SCR-latchup-resistant CMOS process and circuit design
- Exceeds 2kV ESD protection per MIL-STD-883, method 3015

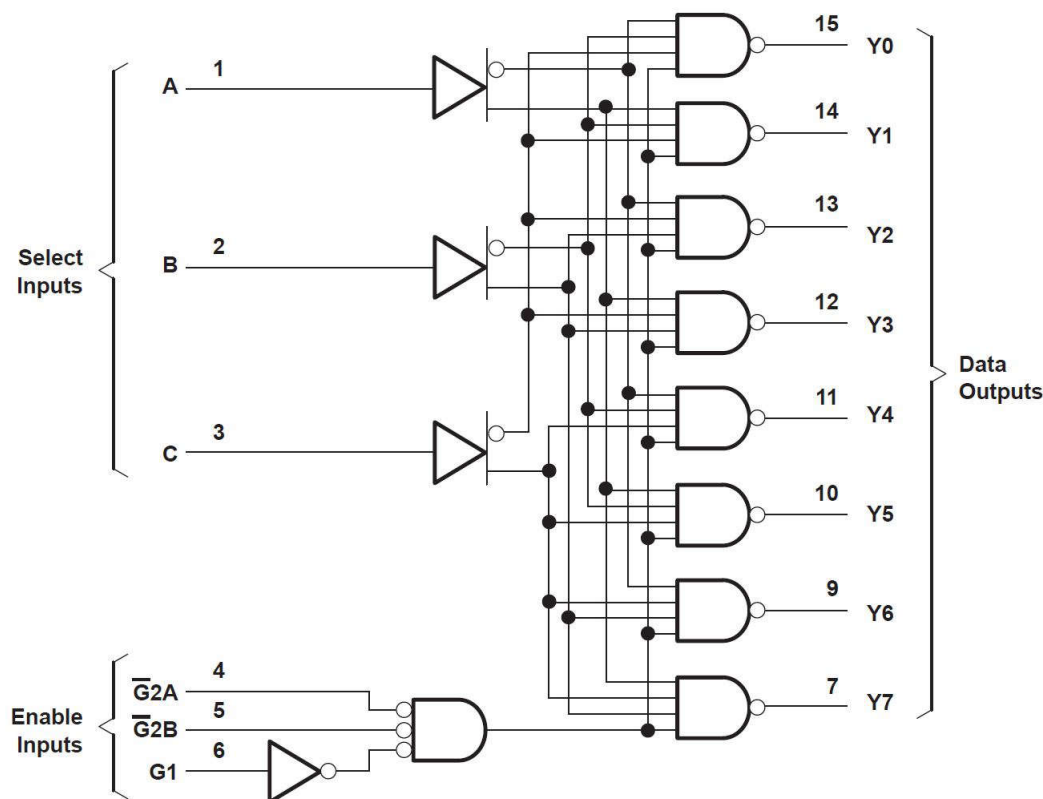
2 Description

The 'ACT138 decoders/demultiplexers are designed for high-performance memory-decoding and data-routing applications that require very short propagation-delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding.

Device Information

| PART NUMBER | PACKAGE ⁽¹⁾ | PACKAGE SIZE ⁽²⁾ | BODY SIZE ⁽³⁾ |
|-------------|------------------------|-----------------------------|--------------------------|
| CDx4ACT138 | BQB (WQFN, 16) | 3.5mm × 2.5mm | 3.5mm × 2.5mm |
| | D (SOIC, 16) | 9.9mm × 6mm | 9.9mm × 3.9mm |
| | N (PDIP, 16) | 19.3mm × 9.4mm | 19.3mm × 6.35mm |
| | PW (TSSOP, 16) | 5.00mm × 6.4mm | 5.00mm × 4.40mm |

- (1) For more information, see [Section 10](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram (Positive Logic)



Table of Contents

| | | | |
|--|---|--|----|
| 1 Features | 1 | 6.3 Device Functional Modes..... | 8 |
| 2 Description | 1 | 7 Application and Implementation | 10 |
| 3 Pin Configuration and Functions | 3 | 7.1 Application Information..... | 10 |
| 4 Specifications | 4 | 7.2 Power Supply Recommendations..... | 12 |
| 4.1 Absolute Maximum Ratings..... | 4 | 7.3 Layout..... | 12 |
| 4.2 ESD Ratings..... | 4 | 8 Device and Documentation Support | 13 |
| 4.3 Recommended Operating Conditions..... | 4 | 8.1 Documentation Support (Analog)..... | 13 |
| 4.4 Thermal Information..... | 4 | 8.2 Receiving Notification of Documentation Updates... 13 | |
| 4.5 Electrical Characteristics..... | 5 | 8.3 Support Resources..... | 13 |
| 4.6 Switching Characteristics..... | 5 | 8.4 Trademarks..... | 13 |
| 4.7 Operating Characteristics..... | 5 | 8.5 Electrostatic Discharge Caution..... | 13 |
| 5 Parameter Measurement Information | 6 | 8.6 Glossary..... | 13 |
| 6 Detailed Description | 8 | 9 Revision History | 13 |
| 6.1 Overview..... | 8 | 10 Mechanical, Packaging, and Orderable Information | 14 |
| 6.2 Functional Block Diagram..... | 8 | | |

3 Pin Configuration and Functions

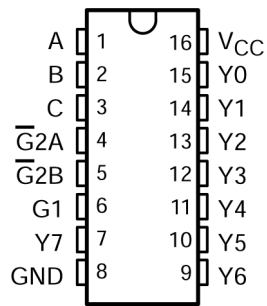


Figure 3-1. CD54ACT138 J Package; CD74ACT138 D, N, or PW Package; 16-Pin CDIP, SOIC, PDIP, or TSSOP (Top View)

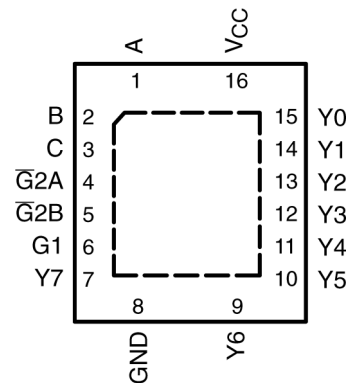


Figure 3-2. CD74ACT138 BQB Package, 16-Pin WQFN (Top View)

Table 3-1. Pin Functions

| PIN | | TYPE ⁽¹⁾ | DESCRIPTION |
|------------------|-----|---------------------|-----------------------------|
| NAME | NO. | | |
| A | 1 | I | Input A |
| B | 2 | I | Input B |
| C | 3 | I | Input C |
| $\overline{G2A}$ | 4 | I | Strobe Input 2A, active low |
| $\overline{G2B}$ | 5 | I | Strobe Input 2B, active low |
| G1 | 6 | I | Strobe Input |
| Y7 | 7 | O | Output 7 |
| GND | 8 | G | Ground |
| Y6 | 9 | O | Output 6 |
| Y5 | 10 | O | Output 5 |
| Y4 | 11 | O | Output 4 |
| Y3 | 12 | O | Output 3 |
| Y2 | 13 | O | Output 2 |
| Y1 | 14 | O | Output 1 |
| Y0 | 15 | O | Output 0 |
| V _{CC} | 16 | P | Positive Supply |

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|--------------------------------|---|---|-----|---------|
| V _{CC} | Supply voltage range | -0.5 | 6 | V |
| I _{IK} ⁽²⁾ | Input clamp current | (V _I < 0 V or V _I > V _{CC}) | | ±20 mA |
| I _{OK} ⁽²⁾ | Output clamp current | (V _O < 0 V or V _O > V _{CC}) | | ±50 mA |
| I _O | Continuous output current | (V _O > 0 V or V _O < V _{CC}) | | ±50 mA |
| | Continuous current through V _{CC} or GND | | | ±100 mA |
| T _{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

4.2 ESD Ratings

| | | | VALUE | UNIT |
|--------------------|-------------------------|---|-------|------|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | V |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | T _A = 25°C | | -55°C to 125°C | | -40°C to 85°C | | UNIT |
|-----------------|------------------------------------|-----------------------|-----------------|----------------|-----------------|---------------|-----------------|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| V _{CC} | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | 4.5 | 5.5 | V |
| V _{IH} | High-level input voltage | 2 | | 2 | | 2 | | V |
| V _{IL} | Low-level input voltage | | 0.8 | | 0.8 | | 0.8 | V |
| V _I | Input voltage | 0 | V _{CC} | 0 | V _{CC} | 0 | V _{CC} | V |
| V _O | Output voltage | 0 | V _{CC} | 0 | V _{CC} | 0 | V _{CC} | V |
| I _{OH} | High-level output current | | -24 | | -24 | | -24 | mA |
| I _{OL} | Low-level output current | | 24 | | 24 | | 24 | mA |
| Δt/Δv | Input transition rise or fall rate | | 10 | | 10 | | 10 | ns/V |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

4.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | CD74ACT138 | | | | UNIT |
|-------------------------------|--|------------|----------|----------|------------|------|
| | | BQB (WQFN) | D (SOIC) | N (PDIP) | PW (TSSOP) | |
| | | 16 PINS | 16 PINS | 16 PINS | 16 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 83.9 | 106.6 | 67 | 126.2 | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | V _{CC} | TA = 25 °C | | -55°C to 125°C | | -40°C to 85°C | | UNIT |
|---------------------------------|---|---|-----------------|------------|------|----------------|------|---------------|-----|------|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | V _I = V _{IH} or V _{IL} | I _{OH} = -50 μA | 4.5 V | 4.4 | | 4.4 | | 4.4 | V | |
| | | I _{OH} = -24 mA | 4.5 V | 3.94 | | 3.7 | | 3.8 | | |
| | | I _{OH} = -50 mA ⁽¹⁾ | 5.5 V | | | 3.85 | | | | |
| | | I _{OH} = -75 mA ⁽¹⁾ | 5.5 V | | | | | 3.85 | | |
| V _{OL} | V _I = V _{IH} or V _{IL} | I _{OL} = 50 μA | 4.5 V | | 0.1 | | 0.1 | 0.1 | V | |
| | | I _{OL} = 24 mA | 4.5 V | | 0.36 | | 0.5 | 0.44 | | |
| | | I _{OL} = 50 mA ⁽¹⁾ | 5.5 V | | | | 1.65 | | | |
| | | I _{OL} = 75 mA ⁽¹⁾ | 5.5 V | | | | | 1.65 | | |
| I _I | V _I = V _{CC} or GND | | 5.5 V | ±0.1 | | ±1 | | ±1 | μA | |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | | 5.5 V | 8 | | 160 | | 80 | μA | |
| ΔI _{CC} ⁽²⁾ | V _I = V _{CC} - 2.1 V | | 4.5 V to 5.5 V | 2.4 | | 3 | | 2.8 | mA | |
| C _i | | | | 10 | | 10 | | 10 | PF | |

- (1) Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.
- (2) Additional quiescent supply current per input pin, TTL inputs high, 1 unit load

Table 4-1. Act Input Load Table

| INPUT | UNIT LOAD |
|--------------------------------------|-----------|
| A, B, or C | 0.83 |
| $\overline{G}2A$ or $\overline{G}2B$ | 1 |
| G1 | 0.42 |

4.6 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5V ± 0.5V, C_L = 50pF (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

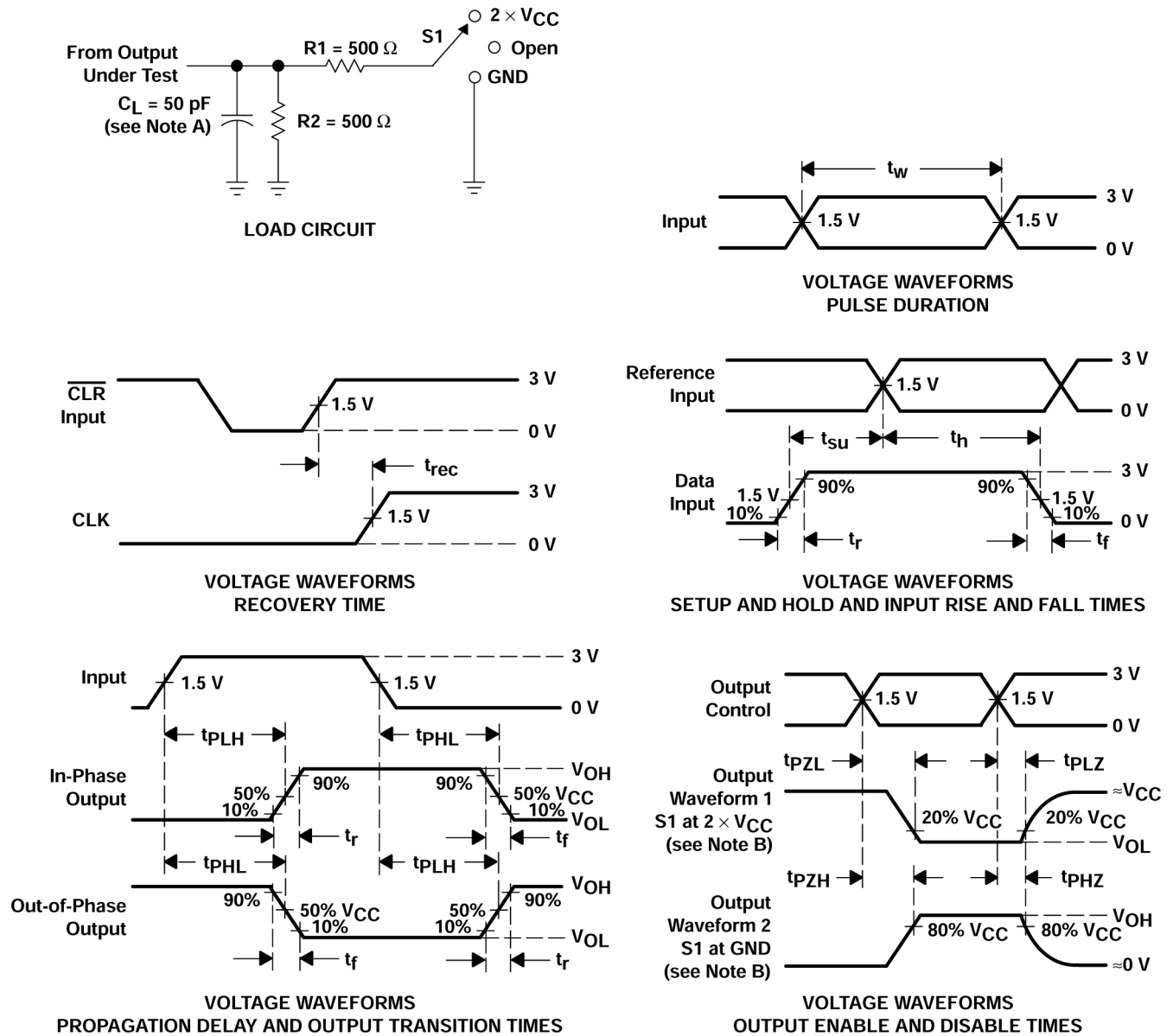
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | -55°C to 125°C | | -40°C to 85°C | | UNIT |
|------------------|----------------------------------|-------------|----------------|------|---------------|------|------|
| | | | MIN | MAX | MIN | MAX | |
| t _{PLH} | A, B, C | Any Y | 3 | 12 | 3.1 | 10.9 | ns |
| t _{PHL} | | | 3 | 12 | 3.1 | 10.9 | |
| t _{PLH} | G1 | Any Y | 2.8 | 11 | 2.8 | 10 | ns |
| t _{PHL} | | | 2.8 | 11 | 2.8 | 10 | |
| t _{PLH} | $\overline{G}2A, \overline{G}2B$ | Any Y | 2.6 | 10.5 | 2.7 | 9.5 | ns |
| t _{PHL} | | | 2.6 | 10.5 | 2.7 | 9.5 | |

4.7 Operating Characteristics

V_{CC} = 5V, T_A = 25°C

| PARAMETER | TYP | UNIT |
|-----------------|-----|------|
| C _{pd} | 110 | pF |

5 Parameter Measurement Information



- A. C_L includes probe and test-fixture capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 3$ ns, $t_f = 3$ ns. Phase relationships between waveforms are arbitrary.
- D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
- E. The outputs are measured one at a time with one input transition per measurement.
- F. t_{PLH} and t_{PHL} are the same as t_{pd} .
- G. t_{PZL} and t_{PZH} are the same as t_{en} .
- H. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- I. All parameters and waveforms are not applicable to all devices.

Figure 5-1. Load Circuit and Voltage Waveforms

| TEST | S1 |
|-------------------|-------------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | $2 \times V_{CC}$ |
| t_{PHZ}/t_{PZH} | GND |

6 Detailed Description

6.1 Overview

When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory usually are less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

The conditions at the binary-select inputs and the three enable inputs select one of eight output lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications (see Application Information).

6.2 Functional Block Diagram

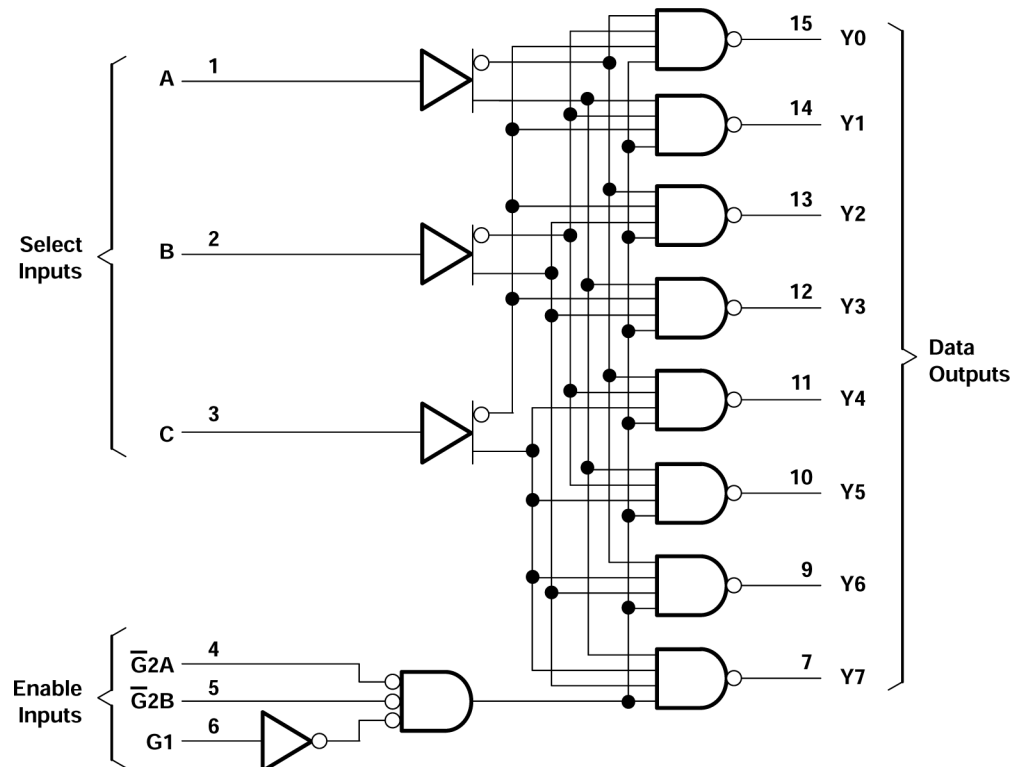


Figure 6-1. Logic Diagram (Positive Logic)

6.3 Device Functional Modes

Table 6-1. Function Table

| ENABLE INPUTS | | | SELECT INPUTS | | | OUTPUTS | | | | | | | |
|---------------|------------------|------------------|---------------|---|---|---------|----|----|----|----|----|----|----|
| G1 | $\overline{G2A}$ | $\overline{G2B}$ | C | B | A | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X | H | X | X | X | X | H | H | H | H | H | H | H | H |
| X | X | H | X | X | X | H | H | H | H | H | H | H | H |
| L | X | X | X | X | X | H | H | H | H | H | H | H | H |
| H | L | L | L | L | L | L | H | H | H | H | H | H | H |
| H | L | L | L | L | H | H | L | H | H | H | H | H | H |
| H | L | L | L | H | L | H | H | L | H | H | H | H | H |
| H | L | L | L | H | H | H | H | H | L | H | H | H | H |
| H | L | L | H | L | L | H | H | H | H | L | H | H | H |
| H | L | L | H | L | H | H | H | H | H | H | L | H | H |

Table 6-1. Function Table (continued)

| ENABLE INPUTS | | | SELECT INPUTS | | | OUTPUTS | | | | | | | |
|---------------|------------------|------------------|---------------|---|---|---------|----|----|----|----|----|----|----|
| G1 | $\overline{G2A}$ | $\overline{G2B}$ | C | B | A | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| H | L | L | H | H | L | H | H | H | H | H | H | L | H |
| H | L | L | H | H | H | H | H | H | H | H | H | H | L |

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

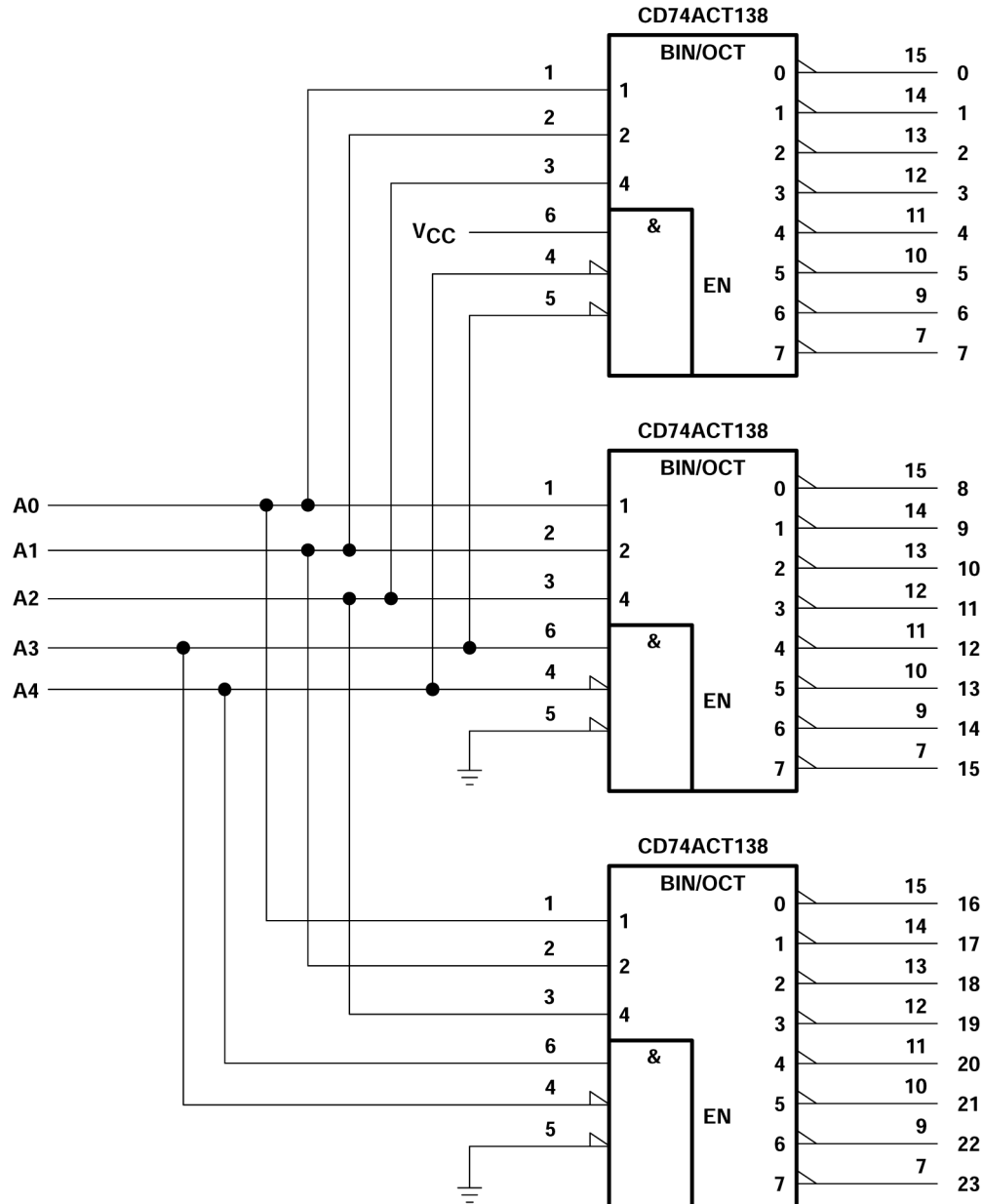


Figure 7-1. 24-Bit Decoding Scheme

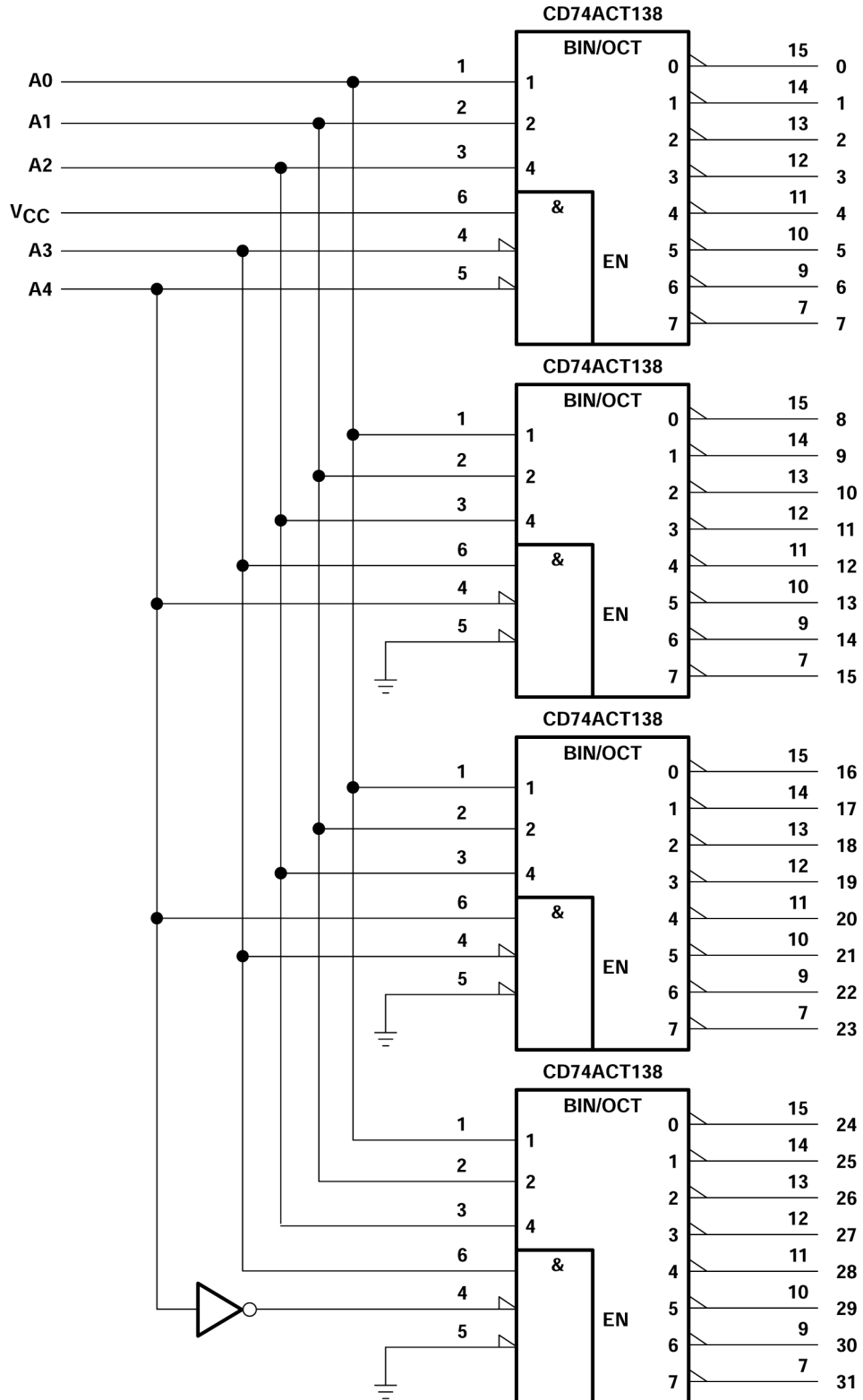


Figure 7-2. 32-Bit Decoding Scheme

7.2 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A $0.1\mu\text{F}$ capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The $0.1\mu\text{F}$ and $1\mu\text{F}$ capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

7.3 Layout

7.3.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

7.3.2 Layout Example

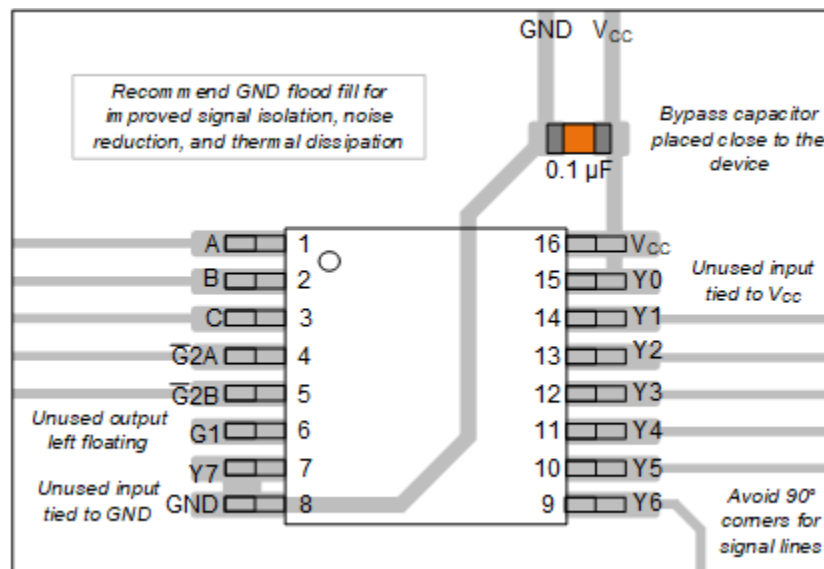


Figure 7-3. Example Layout for the CD74ACT138

8 Device and Documentation Support

8.1 Documentation Support (Analog)

8.1.1 Related Documentation

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| CD54ACT138 | Click here | Click here | Click here | Click here | Click here |
| CD74ACT138 | Click here | Click here | Click here | Click here | Click here |

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

| Changes from Revision B (April 2024) to Revision C (July 2024) | Page |
|---|------|
| • Added BQB and PW packages to <i>Device Information</i> table, <i>Pin Configuration and Functions</i> section, and <i>Thermal Information</i> table..... | 1 |
| • Changed E and M packages to N and D throughout data sheet..... | 1 |

| Changes from Revision A (February 2003) to Revision B (April 2024) | Page |
|---|------|
| • Added <i>Package Information</i> table, <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Device Functional Modes</i> , Application and Implementation section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section | 1 |
| • Updated RθJA values: M = 73 to 106.6, all values in °C/W | 4 |

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|--------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| CD54ACT138F3A | Active | Production | CDIP (J) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | CD54ACT138F3A |
| CD54ACT138F3A.A | Active | Production | CDIP (J) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | CD54ACT138F3A |
| CD74ACT138BQBR | Active | Production | WQFN (BQB) 16 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AD138 |
| CD74ACT138BQBR.A | Active | Production | WQFN (BQB) 16 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AD138 |
| CD74ACT138E | Active | Production | PDIP (N) 16 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74ACT138E |
| CD74ACT138E.A | Active | Production | PDIP (N) 16 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74ACT138E |
| CD74ACT138M | Obsolete | Production | SOIC (D) 16 | - | - | Call TI | Call TI | -55 to 125 | ACT138M |
| CD74ACT138M96 | Active | Production | SOIC (D) 16 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | ACT138M |
| CD74ACT138M96.A | Active | Production | SOIC (D) 16 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | ACT138M |
| CD74ACT138M96G4 | Active | Production | SOIC (D) 16 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | ACT138M |
| CD74ACT138PWR | Active | Production | TSSOP (PW) 16 | 3000 LARGE T&R | Yes | NIPDAU SN | Level-1-260C-UNLIM | -55 to 125 | AD138 |
| CD74ACT138PWR.A | Active | Production | TSSOP (PW) 16 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AD138 |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54ACT138, CD74ACT138 :

- Catalog : [CD74ACT138](#)
- Military : [CD54ACT138](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

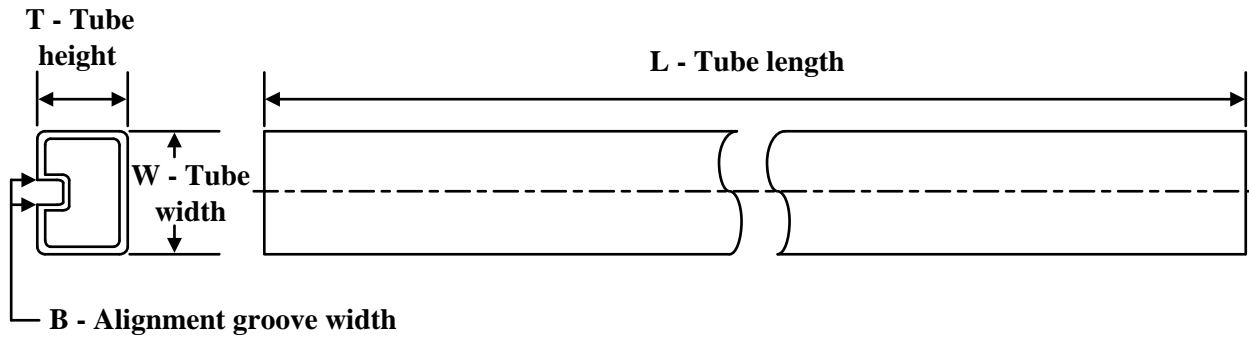

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74ACT138BQBR | WQFN | BQB | 16 | 3000 | 180.0 | 12.4 | 2.8 | 3.8 | 1.2 | 4.0 | 12.0 | Q1 |
| CD74ACT138M96 | SOIC | D | 16 | 2500 | 330.0 | 12.4 | 3.75 | 3.75 | 1.15 | 8.0 | 12.0 | Q1 |
| CD74ACT138M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74ACT138PWR | TSSOP | PW | 16 | 3000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74ACT138BQBR | WQFN | BQB | 16 | 3000 | 210.0 | 185.0 | 35.0 |
| CD74ACT138M96 | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |
| CD74ACT138M96 | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |
| CD74ACT138PWR | TSSOP | PW | 16 | 3000 | 353.0 | 353.0 | 32.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| CD74ACT138E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74ACT138E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74ACT138E.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74ACT138E.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

GENERIC PACKAGE VIEW

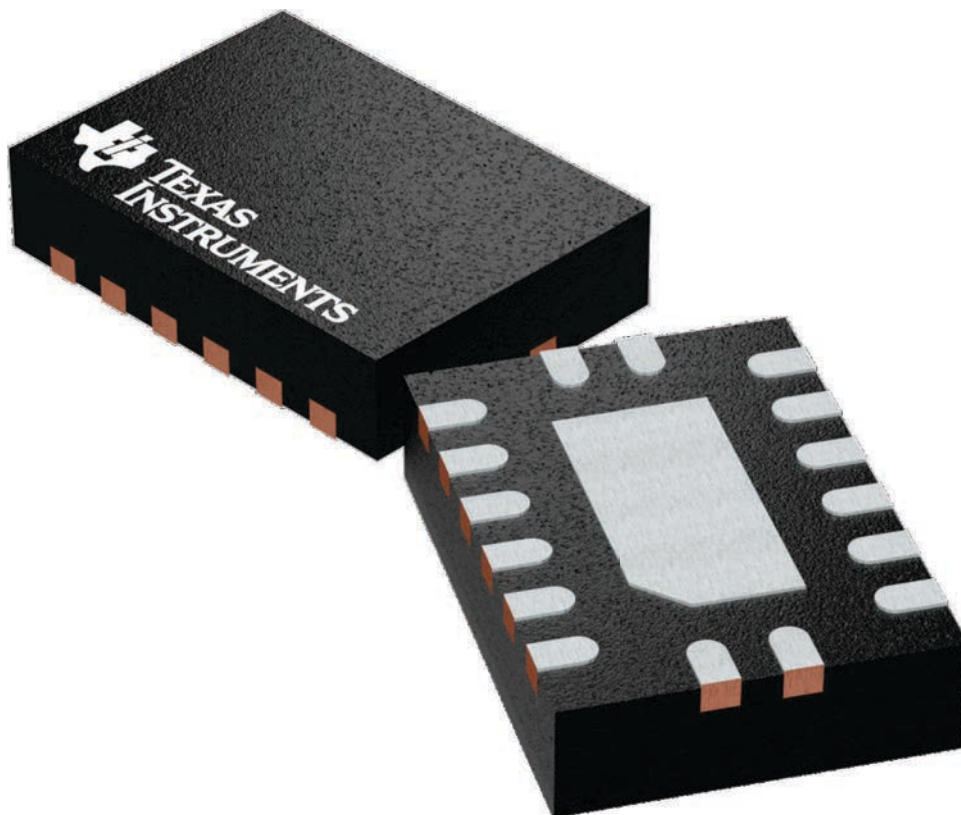
BQB 16

WQFN - 0.8 mm max height

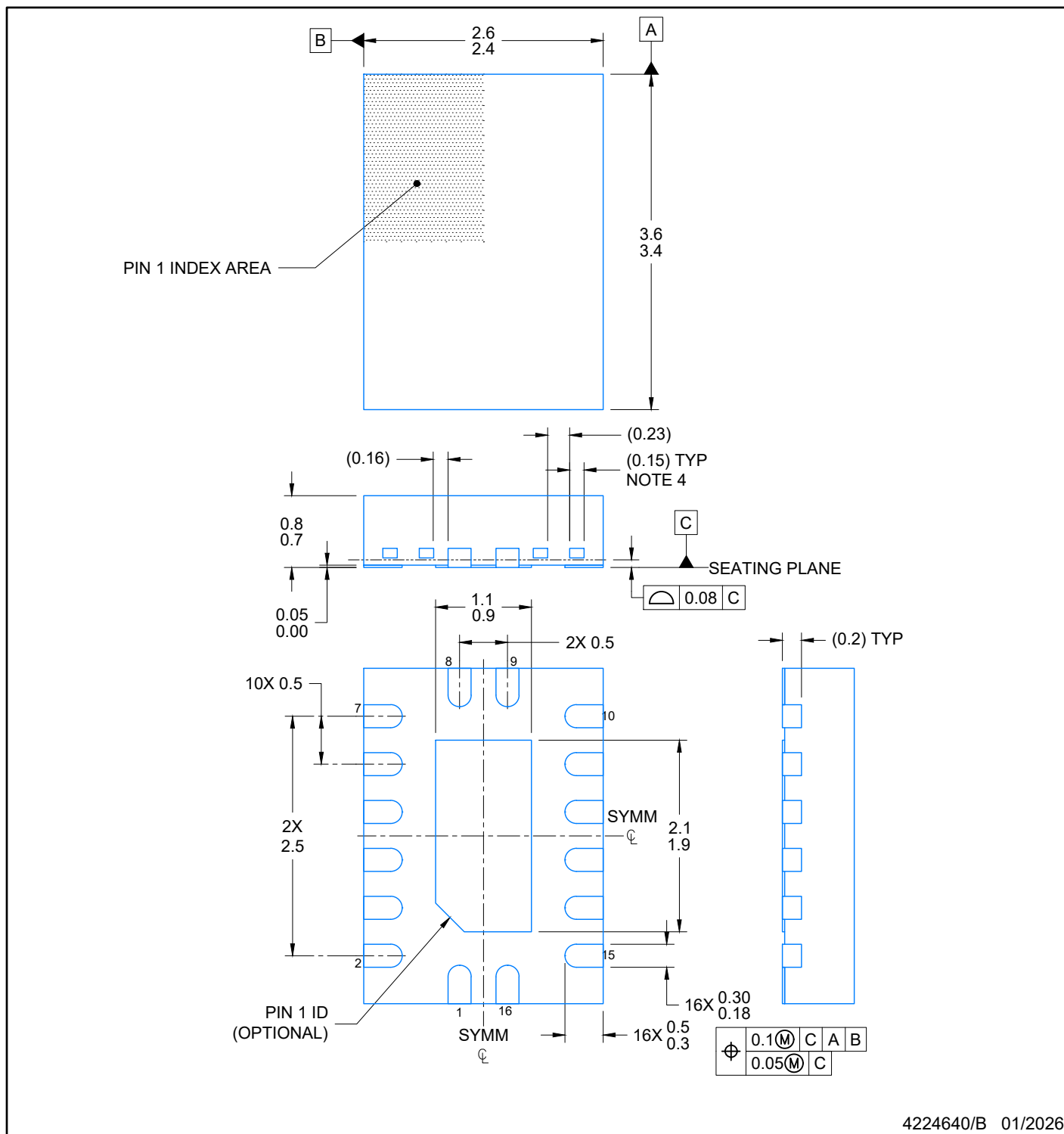
2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



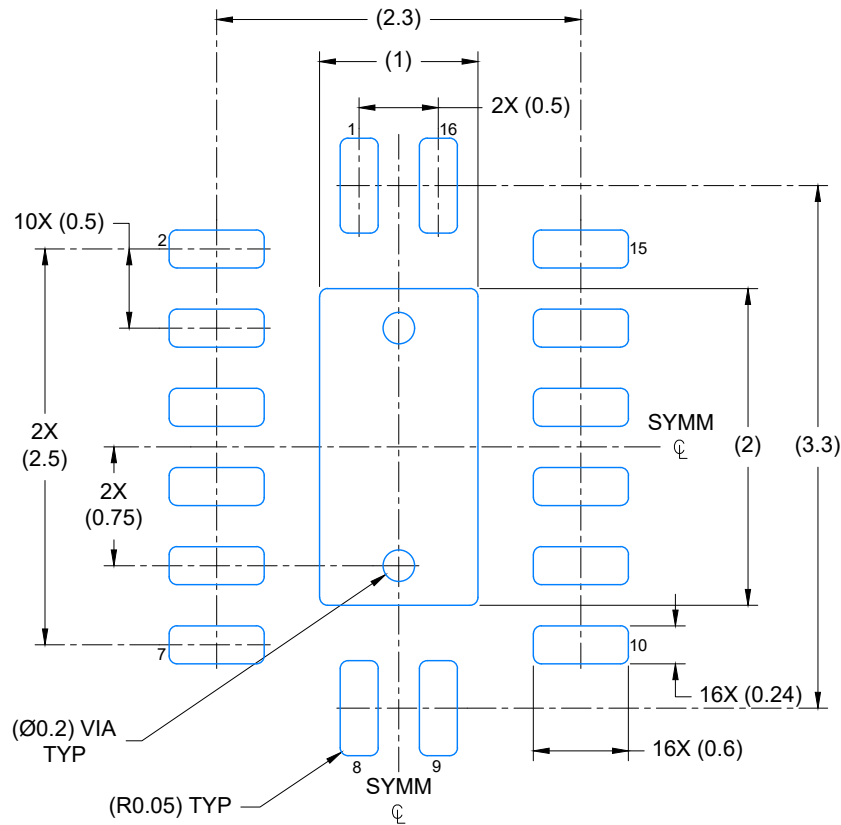
4226161/A



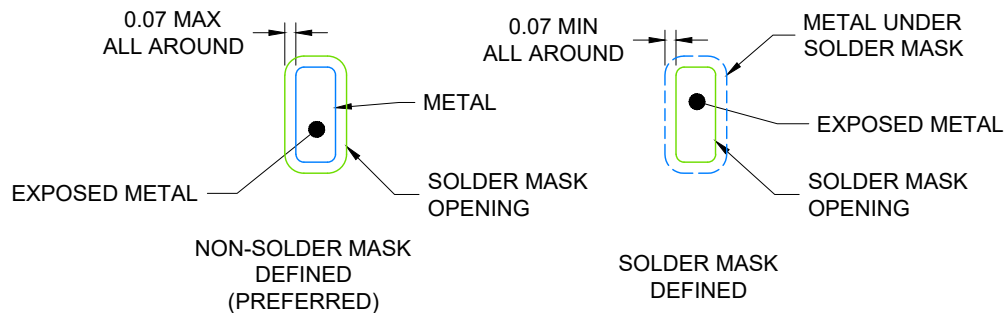
4224640/B 01/2026

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may differ or may not be present



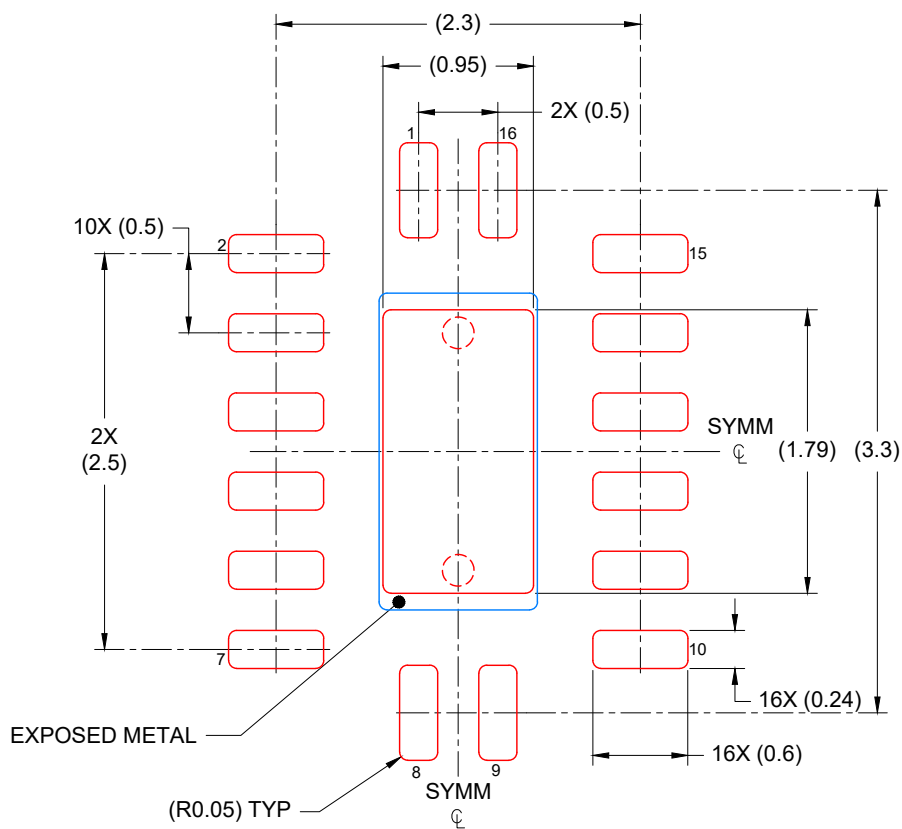
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224640/B 01/2026

1. NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
 85% PRINTED COVERAGE BY AREA
 SCALE: 20X

4224640/B 01/2026

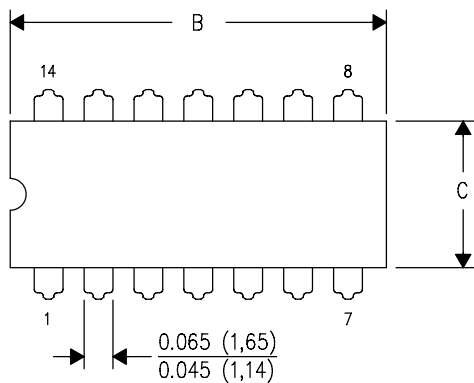
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE

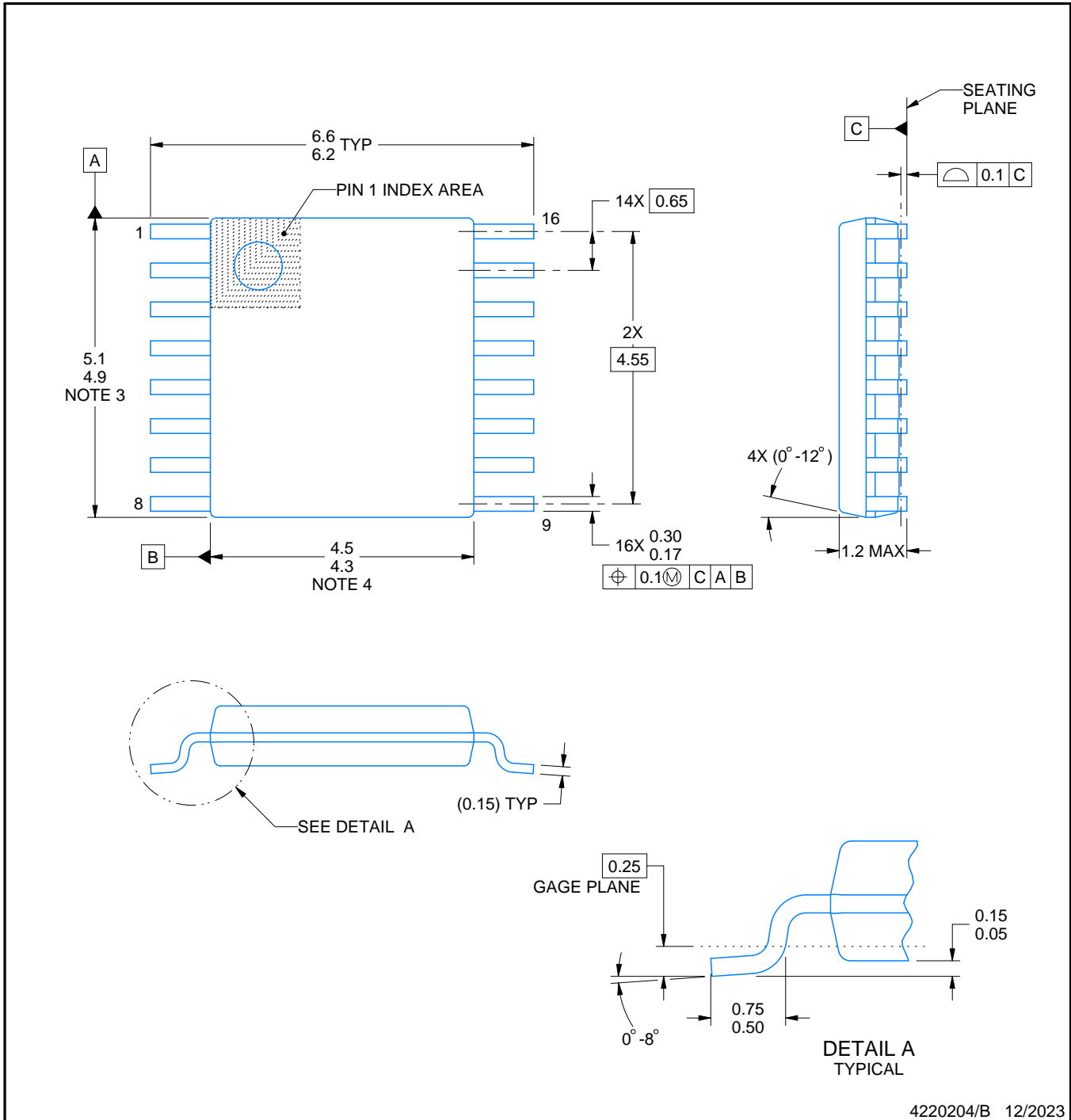


| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



4220204/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

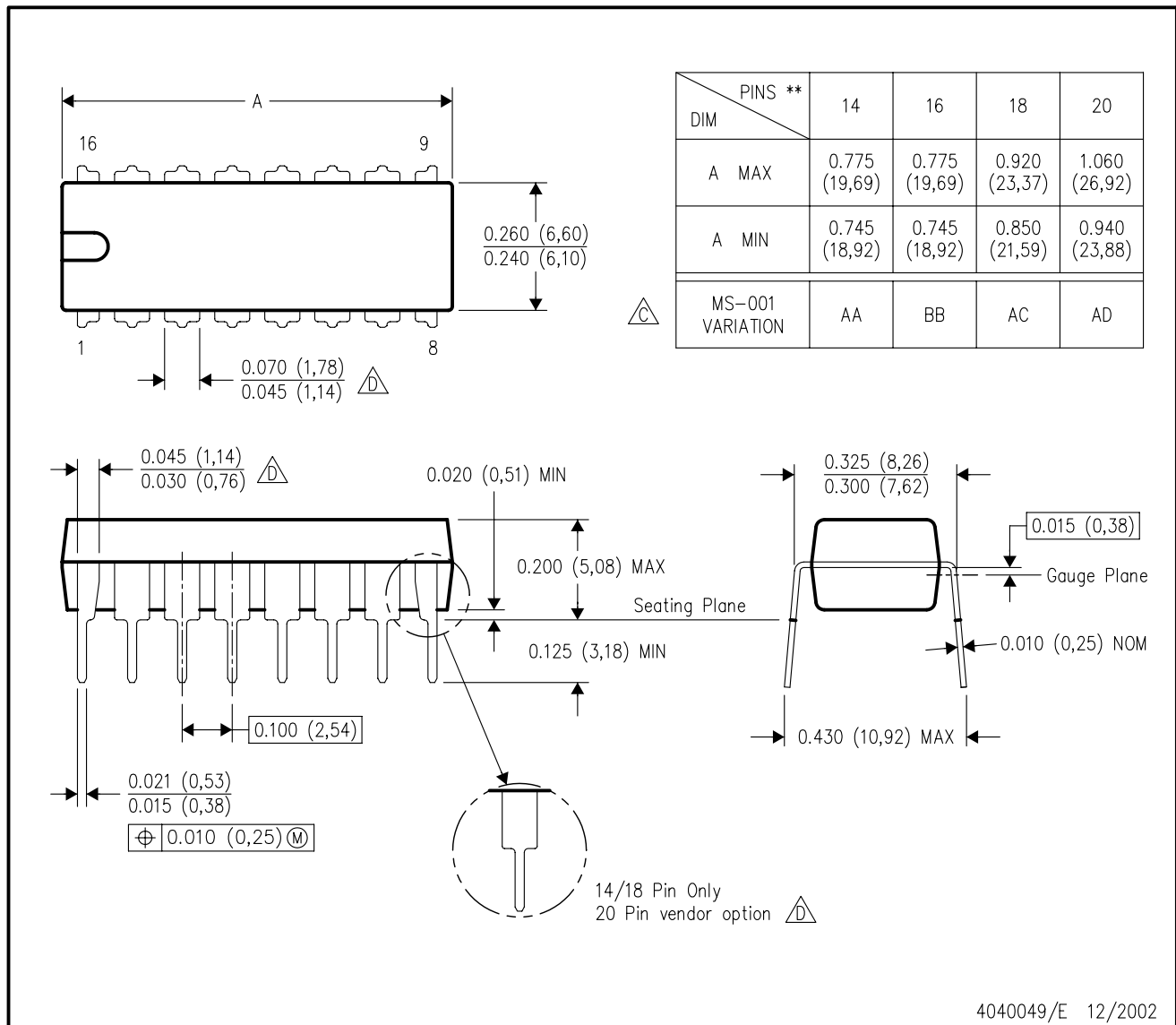
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

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