TEXAS INSTRUMENTS

CD54HC243, CD74HC243, CD54HCT243, CD74HCT243
SCHS168E – NOVEMBER 1998 – REVISED MARCH 2022

CDx4HC243, CDx4HCT243 High-Speed CMOS Logic Quad-Bus Transceiver with Three-State Outputs

1 Features

- Typical propagation delay (A to B, B to A) of 7ns at V_{CC} = 5 V, C_L = 15pF, T_A = 25ºC
- Three-state outputs
- Buffered inputs
- Fanout (over temperature range)
  - Standard outputs : 10 LSTTL loads
  - Bus driver outputs : 15 LSTTL loads
- Wide operating temperature range : -55ºC to 125ºC
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL logic ICs
- HC types
  - 2 V to 6 V Operation
  - High noise immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V
- HCT types
  - 4.5 V to 5.5 V operation
  - Direct LSTTL input logic compatibility, V_{IL} = 0.8 V (Max), V_{IH} = 2 V (Min)
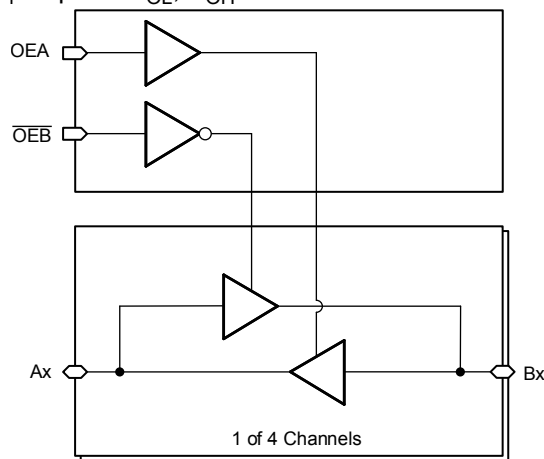 - CMOS input compatibility, I_I ≤ 1µA at V_{OL}, V_{OH}

2 Description

The CDx4HC243 and CDx4HCT243 are quad bus transceivers with 3-state outputs. The OEA and $\overline{OEB}$ inputs control both the high-impedance state as well as the direction of communication through the device.

Device Information

PART NUMBER	PACKAGE[1]	BODY SIZE (NOM)
CD54HC243F	CDIP (14)	19.55 mm × 6.71 mm
CD74HC243E	PDIP (14)	19.31 mm × 6.35 mm
CD74HC243M	SOIC (14)	8.65 mm × 3.90 mm
CD74HCT243E	PDIP (14)	19.31 mm × 6.35 mm
CD74HCT243M	SOIC (14)	8.65 mm × 3.90 mm

(1) For all packages see the orderable addendum at the end of the datasheet.
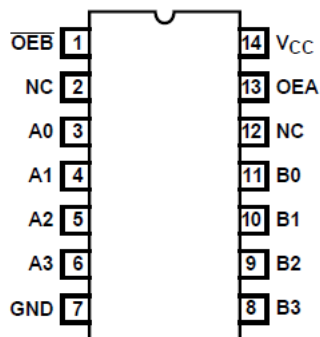

Functional Block Diagram

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3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (October 2003) to Revision E (March 2022)	Page
• Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards... 1	

4 Pin Configuration and Functions

```
        ┌───┬──╥──┬───┐
 OEB ──│ 1 │  ╙  │14 │── V_CC
 NC ───│ 2 │     │13 │── OEA
 A0 ───│ 3 │     │12 │── NC
 A1 ───│ 4 │     │11 │── B0
 A2 ───│ 5 │     │10 │── B1
 A3 ───│ 6 │     │ 9 │── B2
 GND ──│ 7 │     │ 8 │── B3
        └───┴─────┴───┘
```

J, N, or D Package
14-Pin CDIP, PDIP, or SOIC
Top View

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		-0.5	7	V
I_{IK}	Input diode current	For V_I < -0.5V or V_O > V_{CC} + 0.5V		±20	mA
I_{OK}	Output diode current	For V_C < -0.5V or V_O > V_{CC} + 0.5V		±20	mA
I_O	Drian Current, per output	For -0.5V < V_O < V_{CC} + 0.5V		±35	mA
I_O	Output source or sink current per output pin	For V_O > -0.5V or V_O < V_{CC} + 0.5V		±25	mA
	Continuous current through V_{CC} or GND			±70	mA
T_{stg}	Storage temperature range		-65	150	°C
T_J	Junction temperature			150	°C
	Lead temperature (Soldering 10s)(SOIC - Lead Tips Only)			300	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage range	HC Types	2	6	V
		HCT Types	4.5	5.5	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
t_t	Input rise and fall time	V_{CC} = 2V		1000	ns
		V_{CC} = 4.5V		500	
		V_{CC} = 6V		400	
T_A	Temperature Range		-55	125	°C

5.3 Thermal Information

THERMAL METRIC		N (PDIP)	D (SOIC)	UNIT
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	80	86	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS[1]	V$_{CC}$ (V)	25°C MIN	25°C TYP	25°C MAX	-40°C to 85°C MIN	-40°C to 85°C MAX	-55°C to 125°C MIN	-55°C to 125°C MAX	UNIT
HC TYPES											
V$_{IH}$	High-level input voltage		2	1.5			1.5		1.5		V
			4.5	3.15			3.15		3.15		
			6	4.2			4.2		4.2		
V$_{IL}$	Low-level input voltage		2			0.5		0.5		0.5	V
			4.5			1.35		1.35		1.35	
			6			1.8		1.8		1.8	
V$_{OH}$	High-level output voltage CMOS loads	I$_{OH}$ = −20µA	2	1.9			1.9		1.9		V
		I$_{OH}$ = −20µA	4.5	4.4			4.4		4.4		
		I$_{OH}$ = −20µA	6	5.9			5.9		5.9		
	High-level output voltage TTL loads	I$_{OH}$ = −6mA	4.5	3.98			3.84		3.7		
		I$_{OH}$ = −7.8mA	6	5.48			5.34		5.2		
V$_{OL}$	Low-level output voltage CMOS loads	I$_{OL}$ = 20µA	2			0.1		0.1		0.1	V
		I$_{OL}$ = 20µA	4.5			0.1		0.1		0.1	
		I$_{OL}$ = 20µA	6			0.1		0.1		0.1	
	Low-level output voltage TTL	I$_{OL}$ = 6mA	4.5			0.26		0.33		0.4	
		I$_{OL}$ = 7.8mA	6			0.26		0.33		0.4	
I$_I$	Input leakage current	V$_{CC}$ or GND	6			±0.1		±1		±1	µA
I$_{CC}$	Supply Current	V$_{CC}$ or GND	6			8		80		160	µA
I$_{OZ}$	Three-state leakage current	V$_{IL}$ or V$_{IH}$	6			±0.5		±0.5		±10	µA
HCT TYPES											
V$_{IH}$	High-level input voltage		4.5 to 5.5	2			2		2		V
V$_{IL}$	Low-level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V$_{OH}$	High-level output voltage CMOS loads	I$_{OH}$ = −20µA	4.5	4.4			4.4		4.4		V
	High-level output voltage TTL loads	I$_{OH}$ = −6mA	4.5	3.98			3.84		3.7		
V$_{OL}$	Low-level output voltage CMOS loads	I$_{OL}$ = 20µA	4.5			0.1		0.1		0.1	V
	Low-level output voltage TTL loads	I$_{OL}$ = 6mA	4.5			0.26		0.33		0.4	
I$_I$	Input leakage current	V$_{CC}$ to GND	5.5			±0.1		±1		±1	µA
I$_{CC}$	Supply current	V$_{CC}$ or GND	5.5			8		80		160	µA
ΔI$_{CC}$ [2][3]	Additional supply current per input pin	One of An or Bn	4.5 to 5.5		100	396		495		539	µA
		One of OEA or $\overline{OEB}$	4.5 to 5.5		100	216		270		294	
I$_{OZ}$	Three-state leakage current	V$_{IL}$ or V$_{IH}$	5.5			±0.5		±5		±10	µA

(1)   V$_I$ = V$_{IH}$ or V$_{IL}$, unless otherwise noted.
(2)   For dual-supply systems theoretical worst case (V$_I$ = 2.4 V, V$_{CC}$ = 5.5 V) specification is 1.8 mA.
(3)   Inputs held at V$_{CC}$ − 2.1.

5.5 Switching Characteristics

Input t_t = 6ns. Unless otherwise specified, C_L = 50pF

| PARAMETER		V_{CC} (V)	25°C		-40°C to 85°C	-55°C to 125°C	UNIT
			TYP	MAX	MAX	MAX	
HC TYPES							
t_{pd}	Propagation delay data to outputs	2		90	115	135	ns
		4.5	7[1]	18	23	27	
		6		15	20	23	
t_{PZL}, t_{PZH}	Output high-Z, to high level to low level	2		150	190	225	ns
		4.5	12[1]	30	38	45	
		6		26	33	38	
t_{PHZ}, t_{PLZ}	Output high level, output low level to high-Z	2		150	190	225	ns
		4.5	12[1]	30	38	45	
		6		26	33	38	
t_t	Output transition times	2		60	75	90	ns
		4.5		12	15	18	
		6		10	13	15	
C_i	Input capacitance			10	10	10	pF
C_O	Three-state output capacitance			20	20	20	pF
C_{pd} [2] [3]	Power dissipation capacitance	5	80				pF
HCT TYPES							
t_{pd}	Propagation delay data to outputs	4.5	9[1]	22	28	33	ns
t_{PZH}, t_{PLZ}	Output high-Z to high level to low level	4.5	14[1]	34	43	51	ns
t_{PHZ}, t_{PLZ}	Output high level, output low level to high-Z	4.5	14[1]	35	44	53	ns
t_t	Output transition times	4.5		12	15	18	ns
C_i	Input capacitance			10	10	10	pF
C_O	Three-state output capacitance			20	20	20	pF
C_{pd} [2] [3]	Power dissipation capacitance	5	91				pF

(1)   Typical value tested at 5V, C_L = 15pF.
(2) C_{PD} is used to determine the dynamic power consumption, per channel.
(3) $P_D = V_{CC}{}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, f_O = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

6   *Submit Document Feedback*

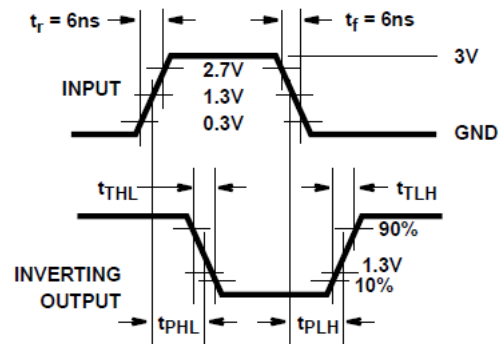Product Folder Links: *CD54HC243 CD74HC243 CD54HCT243 CD74HCT243*

6 Parameter Measurement Information

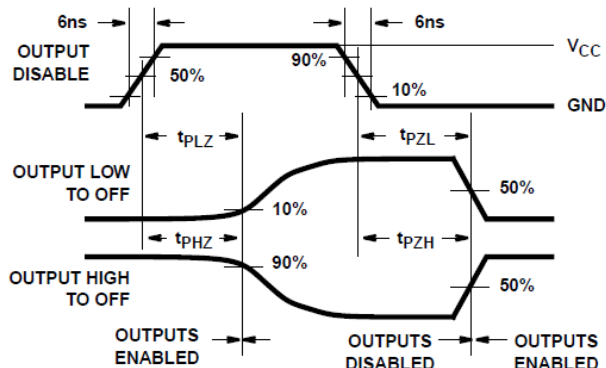t_{PD} is the maximum between t_{PLH} and t_{PHL}
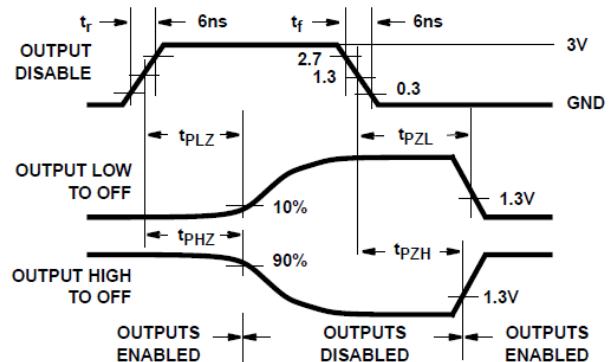
t_t is the maximum between t_{TLH} and t_{THL}
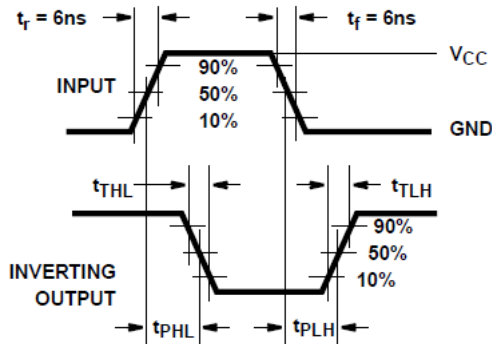
Figure 6-1. HC and HCT transition times and propagation delay times, combination logic
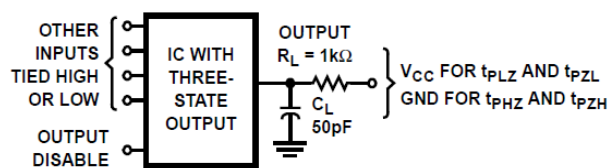
Figure 6-2. HCT transition times and tpopationg delay times, combination logic

Figure 6-3. HC three-state propagation delay waveform

Figure 6-4. HCT three-state propagation delay waveform

NOTE: Open drain waveforms t_{PLZ} and t_{PZL} are the same as those for three-state shown on the left. The test circuit is Output R_L = 1kΩ to V_{CC}, C_L = 50pF.

Figure 6-5. HC and HCT three-state propagation delay test circuit

7 Detailed Description

7.1 Overview

The CDx4HC243 and CDx4HCT243 silicon-gate CMOS three-state bidirectional noninverting buffers are intended for two-way asynchronous communication between data buses. They have high-drive-current outputs that enable high-speed operation when driving large bus capacitances. These circuits possess the low power dissipation of CMOS circuits and have speeds comparable to low-power Schottky TTL circuits. They can drive 15 LSTTL loads.

The states of the output-enable ($\overline{\text{OEB}}$, OEA) inputs determine both the direction of flow (A to B, B to A), and the three-state mode.
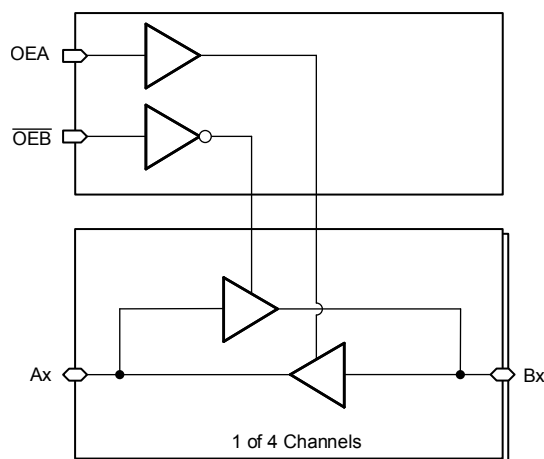
7.2 Functional Block Diagram

Figure 7-1. Functional Diagram

7.3 Device Functional Modes

Table 7-1. Truth Table[1][2]

| Control Inputs | | HC, HCT243 Series | |
| | | Data port status | |
$\overline{\text{OEB}}$	OEA	An	Bn
H	H	O	I
L	H	Z	Z
H	L	Z	Z
L	L	I	O

(1)   H = High voltage level. L = Low voltage level. I = Input. O = Output (Same level as input). Z = High Impedance

(2)   To prevent excess currents in the High Z modes all I/O terminals hsould be terminated with 10kΩ to 1MΩ resistors.

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
8409001CA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8409001CA CD54HC243F3A
CD54HC243F	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC243F
CD54HC243F.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC243F
CD54HC243F3A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8409001CA CD54HC243F3A
CD54HC243F3A.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8409001CA CD54HC243F3A
CD74HC243E	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC243E
CD74HC243E.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC243E
CD74HC243EE4	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC243E
CD74HC243M	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-55 to 125	HC243M
CD74HC243M96	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	HC243M
CD74HC243M96.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC243M
CD74HC243M96G4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC243M
CD74HC243M96G4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC243M
CD74HCT243E	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT243E
CD74HCT243E.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT243E
CD74HCT243M	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT243M
CD74HCT243M.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT243M

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54HC243, CD74HC243 :

• Catalog : CD74HC243

• Military : CD54HC243

NOTE: Qualified Version Definitions:

  • Catalog - TI's standard catalog product

  • Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

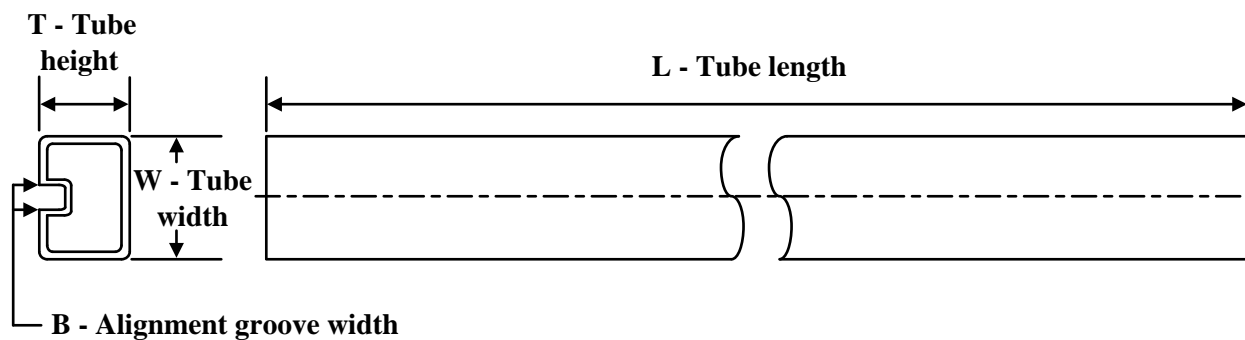| Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC243M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HC243M96	SOIC	D	14	2500	330.0	16.4	6.6	9.3	2.1	8.0	16.0	Q1
CD74HC243M96G4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC243M96	SOIC	D	14	2500	353.0	353.0	32.0
CD74HC243M96	SOIC	D	14	2500	366.0	364.0	50.0
CD74HC243M96G4	SOIC	D	14	2500	353.0	353.0	32.0

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC243E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC243E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC243E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC243E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC243EE4	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC243EE4	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT243E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT243E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT243E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT243E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT243M	D	SOIC	14	50	506.6	8	3940	4.32
CD74HCT243M.A	D	SOIC	14	50	506.6	8	3940	4.32
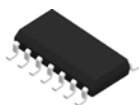
6.2
5.8 TYP

A

PIN 1 ID
AREA

1

14

12X 1.27

8.75
8.55
NOTE 3

2X
7.62

7

8

B

4.0
3.8
NOTE 4

14X 0.51
0.31

⊕ 0.25 Ⓜ C A B

C

SEATING PLANE

◯ 0.1 C

1.75 MAX

SEE DETAIL A

0.25
0.13 TYP

0.25
GAGE PLANE

0° - 8°

1.27
0.40

0.25
0.10

DETAIL A
TYPICAL
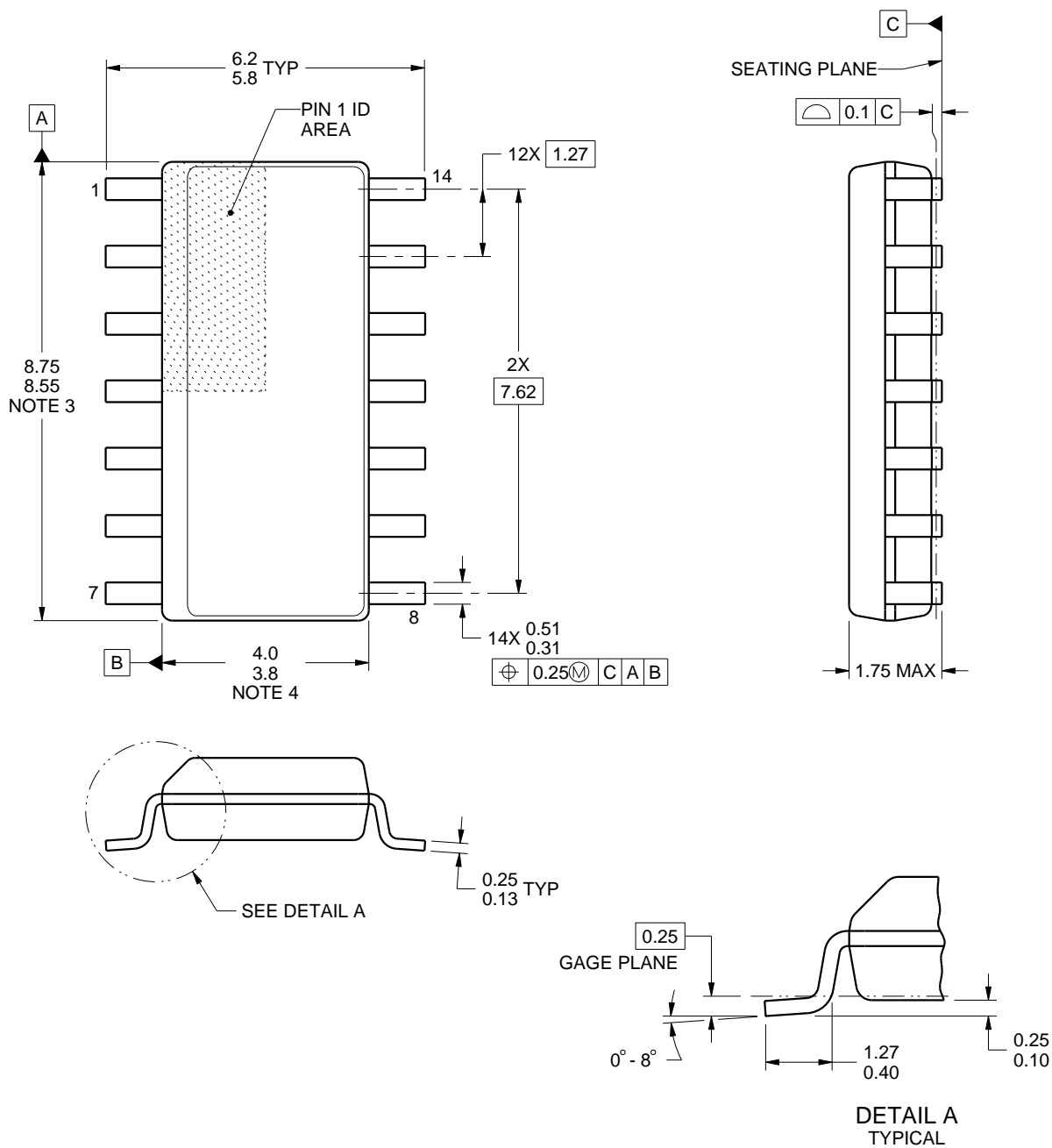
4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
   exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

14X (1.55)

1

14X (0.6)

12X (1.27)

SYMM

14

SYMM

7

8

(R0.05)
TYP

(5.4)
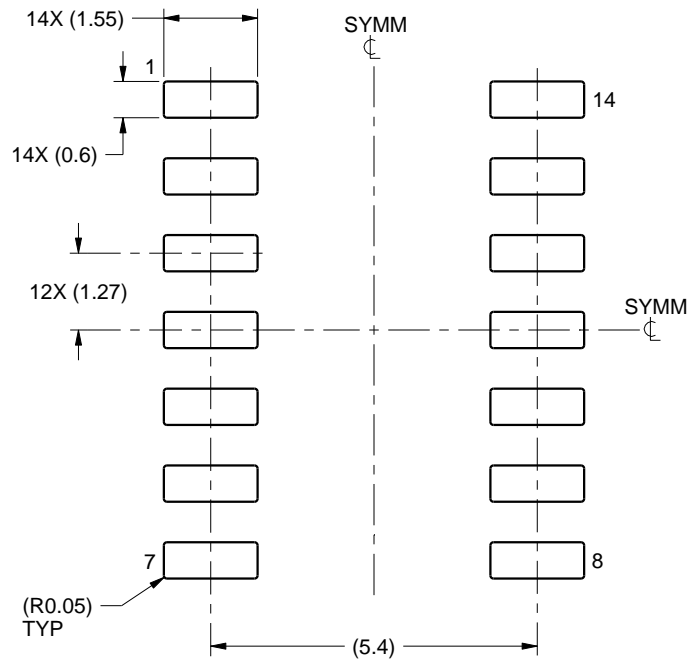
LAND PATTERN EXAMPLE
SCALE:8X

SOLDER MASK
OPENING

METAL

0.07 MAX
ALL AROUND

NON SOLDER MASK
DEFINED

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MIN
ALL AROUND
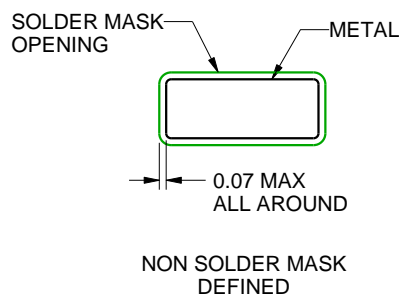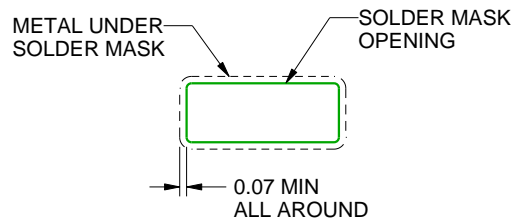
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220718/A   09/2016

NOTES: (continued)
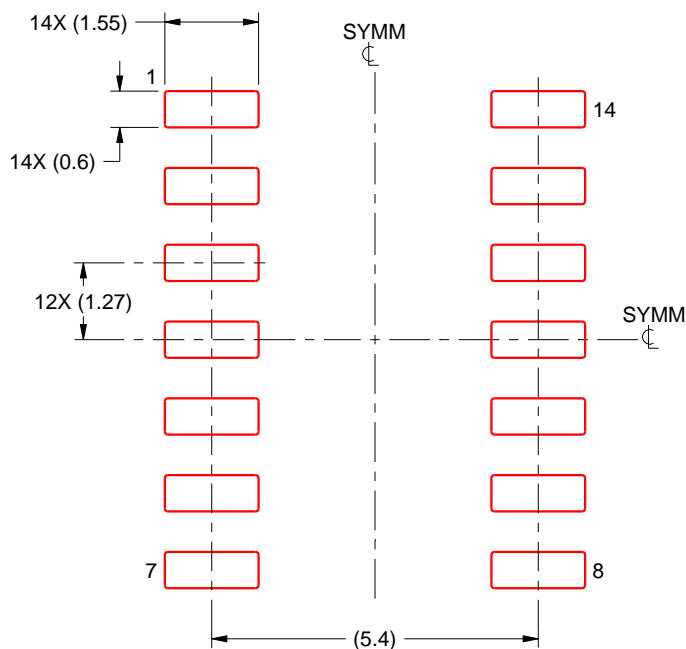
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

14X (1.55)

SYMM

1

14X (0.6)

12X (1.27)

SYMM

7

8

14

(5.4)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

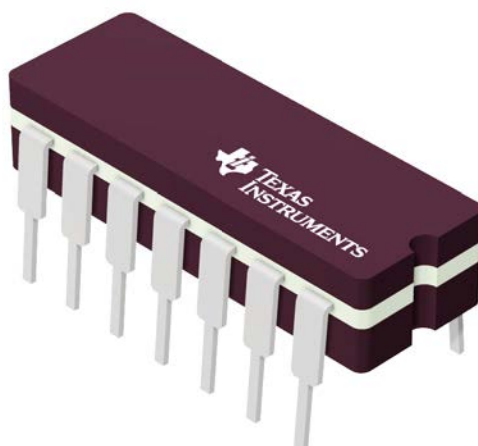4220718/A   09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
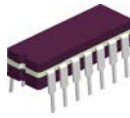9. Board assembly site may have different recommendations for stencil design.
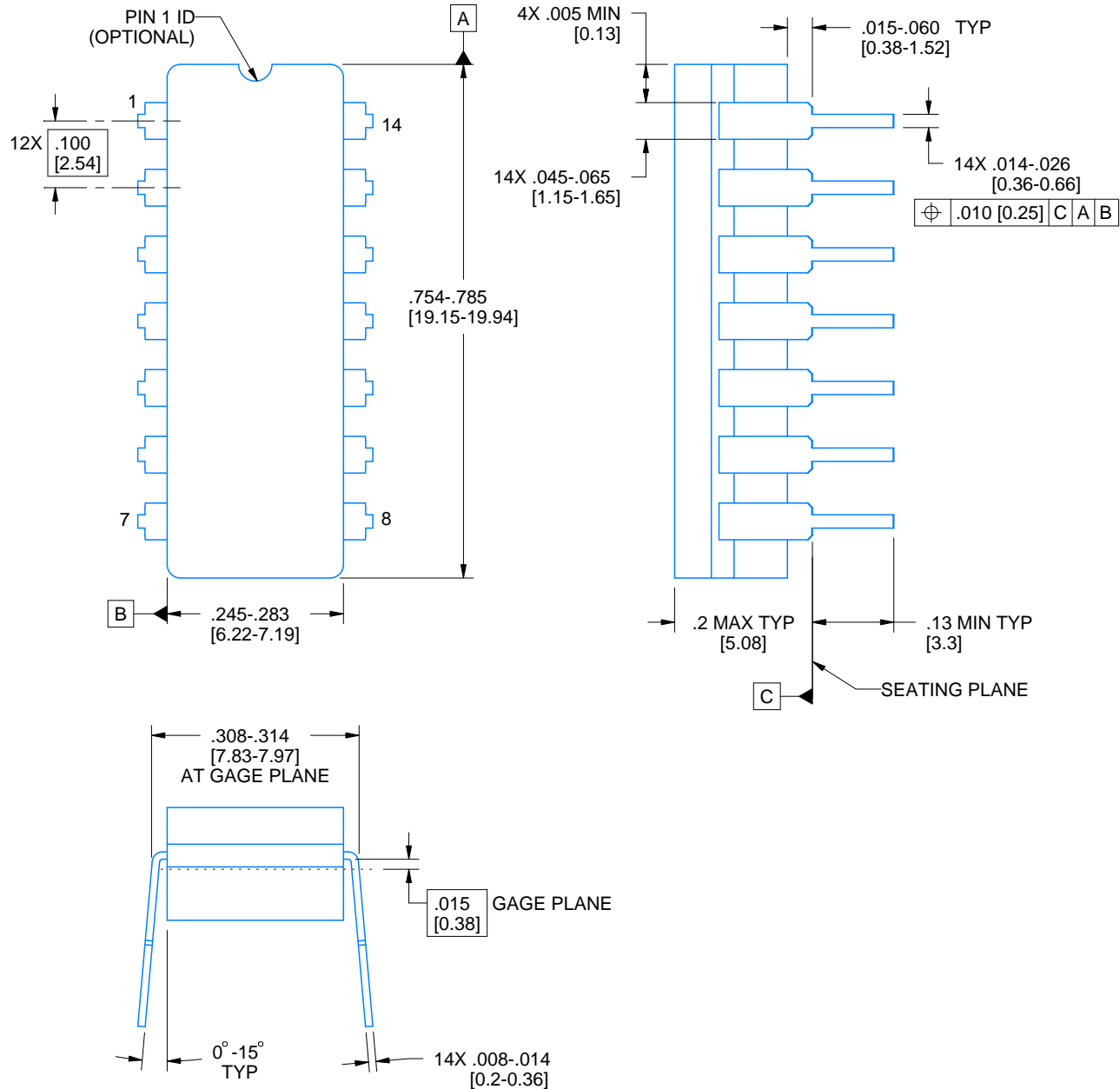
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

PIN 1 ID
(OPTIONAL)

A

4X .005 MIN
[0.13]

.015-.060 TYP
[0.38-1.52]

1

14

12X .100
[2.54]

14X .045-.065
[1.15-1.65]

14X .014-.026
[0.36-0.66]

⊕ .010 [0.25] C A B

.754-.785
[19.15-19.94]

7

8

B

.245-.283
[6.22-7.19]

.2 MAX TYP
[5.08]

.13 MIN TYP
[3.3]

C

SEATING PLANE

.308-.314
[7.83-7.97]
AT GAGE PLANE

.015   GAGE PLANE
[0.38]

0°-15°
TYP

14X .008-.014
[0.2-0.36]

4214771/A   05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
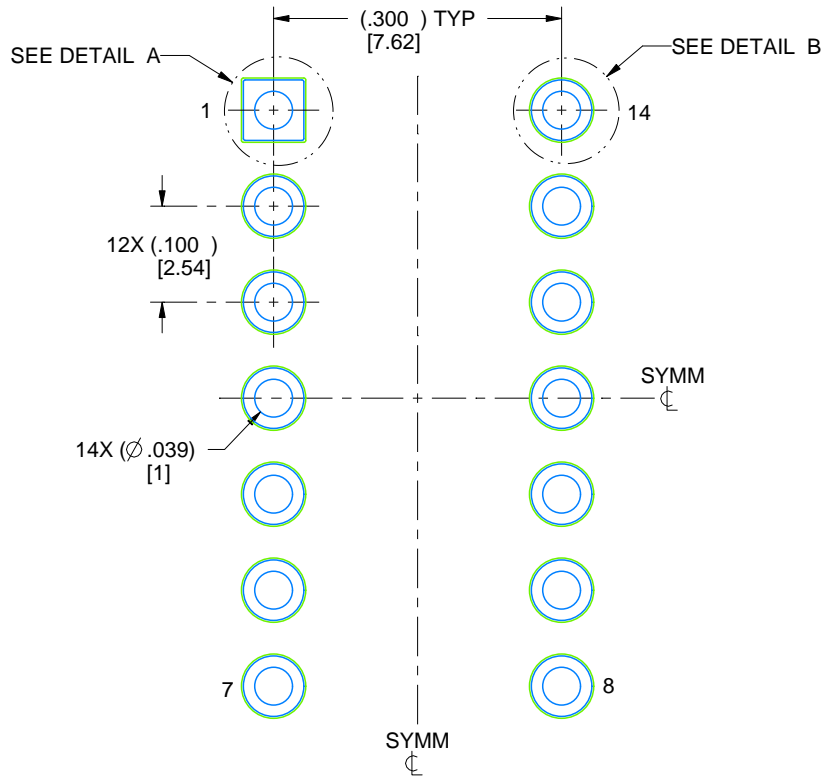5. Falls within MIL-STD-1835 and GDIP1-T14.

SEE DETAIL A

SEE DETAIL B

(.300) TYP
[7.62]

1

14

12X (.100)
[2.54]

SYMM
₵

14X (Ø .039)
[1]

7

8

SYMM
₵

LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

.002 MAX
[0.05]
ALL AROUND

(.063)
[1.6]

SOLDER MASK
OPENING

METAL

(R.002) TYP
[0.05]

DETAIL A
SCALE: 15X

METAL

(Ø .063)
[1.6]

SOLDER MASK
OPENING

.002 MAX
[0.05]
ALL AROUND

DETAIL B
13X, SCALE: 15X
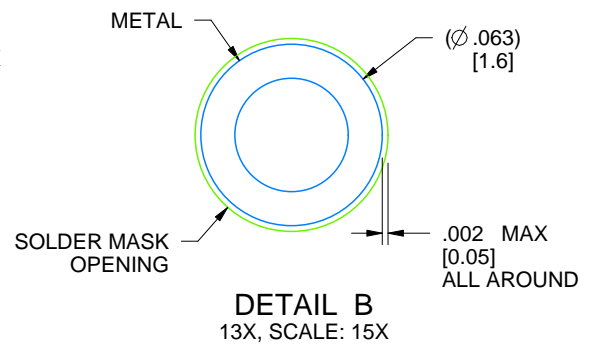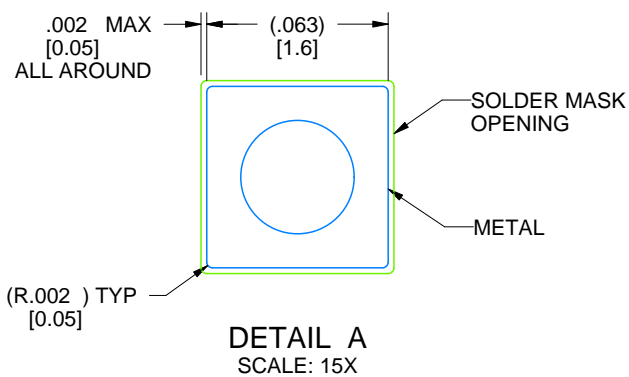
4214771/A   05/2017

N (R−PDIP−T**)
16 PINS SHOWN

PLASTIC DUAL−IN−LINE PACKAGE
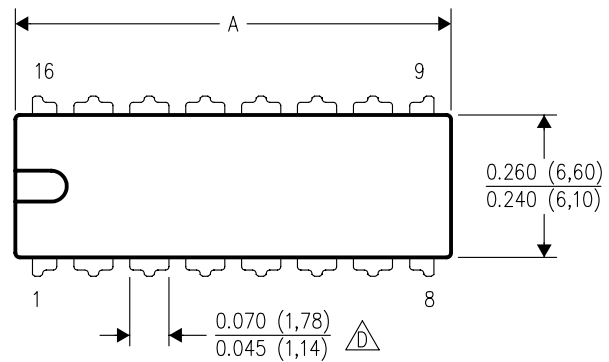
PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60)
0.240 (6,10)

0.070 (1,78)
0.045 (1,14)

0.045 (1,14)
0.030 (0,76)

0.020 (0,51) MIN

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.010 (0,25) NOM

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option
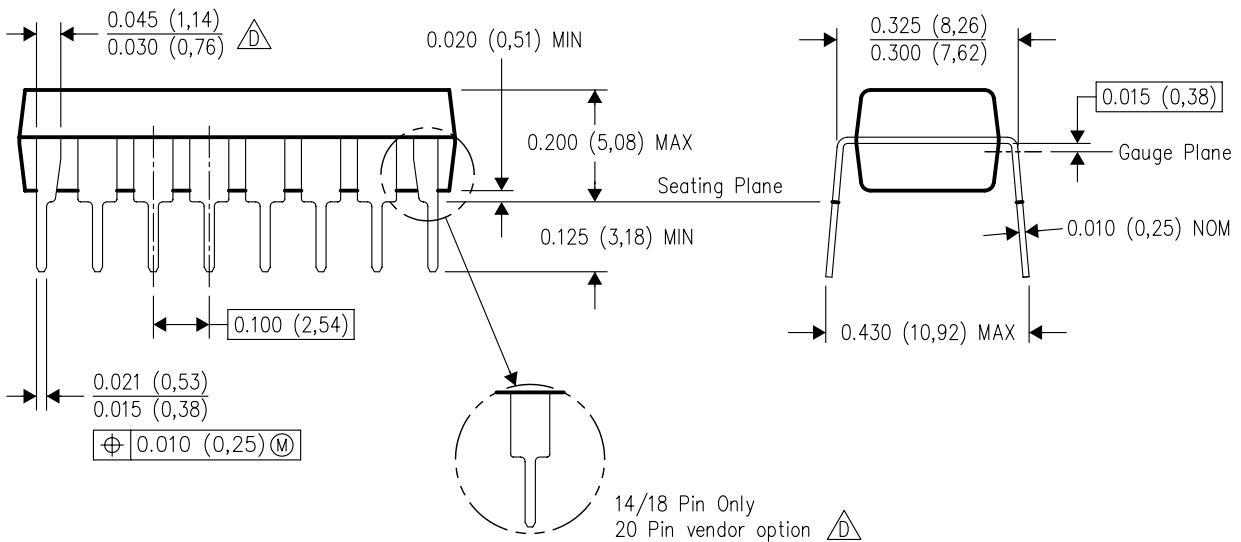
4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
         D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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