# CDx4AC157 Quadruple 2-Line to 1-Line Data Selectors/Multiplexers

## 1 Features

- AC types feature 1.5V to 5.5V operation and balanced noise immunity at 30% of the supply voltage
- Speed of bipolar F, AS, and S, with significantly reduced power consumption
- Balanced propagation delay
- ±24mA output drive current- fanout to 15F devices

## 2 Applications

- Data selection
- Multiplexing

## 3 Description

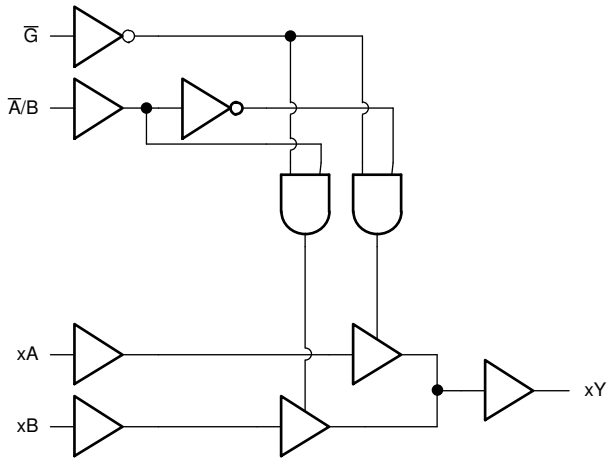
These quadruple 2-line to 1-line data selectors/multiplexers are designed for 1.5V to 5.5V $V_{CC}$ operation

The ’AC157 devices feature a common strobe (G) input. When the strobe is high, all outputs are low. When the strobe is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The devices provide true data.

**Device Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) | BODY SIZE(3) |
|---|---|---|---|
| CD54AC157 | J (CDIP, 16) | 21.34mm × 7.62mm | 21.34mm × 6.92mm |
| CD74AC157 | N (PDIP, 16) | 19.3mm × 9.4mm | 19.3mm × 6.35mm |
| | D (SOIC, 16) | 9.9mm × 6mm | 9.9mm × 3.91mm |
| | BQB (WQFN, 16) | 3.5mm × 2.5mm | 3.5mm × 2.5mm |

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.




**Logic Diagram**

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# 4 Pin Configuration and Functions

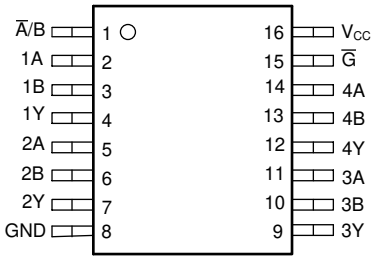



**Figure 4-1. CD54AC157 J Package (Top View)**

**Pin Functions**

| PIN | | | TYPE(1) | DESCRIPTION |
|---|---|---|---|---|
| NAME | PDIP NO. | LCCC NO. | | |
| $\overline{A}$/B | 1 | 2 | I | Address select |
| 1A | 2 | 3 | I | Channel 1, data input A |
| 1B | 3 | 4 | I | Channel 1, data input B |
| 1Y | 4 | 5 | I | Channel 1, data output |
| 2A | 5 | 7 | O | Channel 2, data input A |
| 2B | 6 | 8 | O | Channel 2, data input B |
| 2Y | 7 | 9 | I | Channel 2, data output |
| GND | 8 | 10 | G | Ground |
| 3Y | 9 | 12 | I | Channel 3, data output |
| 3B | 10 | 13 | I | Channel 3, data input B |
| 3A | 11 | 14 | I | Channel 3, data input A |
| 4Y | 12 | 15 | I | Channel 4, data output |
| 4B | 13 | 17 | I | Channel 4, data input B |
| 4A | 14 | 18 | I | Channel 4, data input A |
| $\overline{G}$ | 15 | 19 | I | Output strobe, active low |
| $V_{CC}$ | 16 | 20 | P | Positive supply |
| NC | | 1, 6, 11, 16 | — | Not internally connected |

(1) Signal Types: I = Input, O = Output, G = Ground, P = Power.

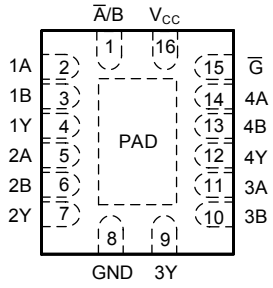



**Figure 4-2. CD74AC157 BQB Package (Top View)**

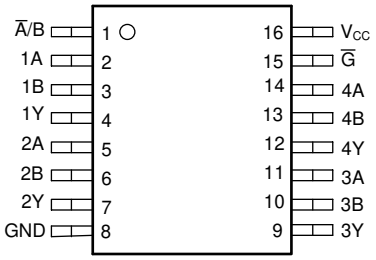



**Figure 4-3. CD74AC157 D , N Package (Top View)**

**Pin Functions**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| $\overline{A}$/B | 1 | I | Address select |
| 1A | 2 | I | Channel 1, data input A |
| 1B | 3 | I | Channel 1, data input B |
| 1Y | 4 | I | Channel 1, data output |
| 2A | 5 | O | Channel 2, data input A |
| 2B | 6 | O | Channel 2, data input B |
| 2Y | 7 | I | Channel 2, data output |
| GND | 8 | G | Ground |
| 3Y | 9 | I | Channel 3, data output |
| 3B | 10 | I | Channel 3, data input B |
| 3A | 11 | I | Channel 3, data input A |
| 4Y | 12 | I | Channel 4, data output |
| 4B | 13 | I | Channel 4, data input B |
| 4A | 14 | I | Channel 4, data input A |
| $\overline{G}$ | 15 | I | Output strobe, active low |
| $V_{CC}$ | 16 | P | Positive supply |
| Thermal Pad[2] | | — | The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply. |

(1) Signal Types: I = Input, O = Output, G = Ground, P = Power.
(2) BQB package only.

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range, $V_{CC}$ | | –0.5 | 6 | V |
| $I_{IK}$ | Input clamp current(2) | $V_I < 0$ or $V_I > V_{CC}$ | | ±20 | mA |
| $I_{OK}$ | Output clamp current(2) | $V_O < 0$ or $V_O >$ VCC | | ±50 | mA |
| $I_O$ | Continuous output current | $V_O = 0$ to $V_{CC}$ | | ±50 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±100 | mA |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | $T_A$ = 25°C | | -55°C to 125°C | | -40°C to 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 1.5 | 5.5 | 1.5 | 5.5 | 1.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.5V | 1.2 | | 1.2 | | 1.2 | | V |
| | | $V_{CC}$ = 3V | 2.1 | | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5V | 3.85 | | 3.85 | | 3.85 | | V |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 1.5V | | 0.3 | | 0.3 | | 0.3 | V |
| | | $V_{CC}$ = 3V | | 0.9 | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5V | | 1.65 | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 4.5V to 5.5V | | -24 | | -24 | | -24 | mA |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 4.5V to 5.5V | | 24 | | 24 | | 24 | mA |
| Δt/Δv | Input transition rise or fall rate | $V_{CC}$ = 1.5V to 3V | | 50 | | 50 | | 50 | ns/V |
| | | $V_{CC}$ = 3.6V to 5.5V | | 20 | | 20 | | 20 | |

## 5.4 Thermal Information

| PACKAGE | PINS | THERMAL METRIC(1) | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | $R_{\theta JA}$ | $R_{\theta JC(top)}$ | $R_{\theta JB}$ | $\Psi_{JT}$ | $\Psi_{JB}$ | $R_{\theta JC(bot)}$ | |
| E (PDIP) | 16 | 67 | - | - | - | - | - | °C/W |
| M (SOIC) | 16 | 73 | - | - | - | - | - | °C/W |
| BQB (WQFN) | 16 | 98.6 | 94.6 | 67.7 | 15.6 | 67.5 | 45.9 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

## 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $V_{CC}$ | $T_A$ = 25°C | | -55°C to 125°C | | -40°C to 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = -50µA | 1.5V | 1.4 | | 1.4 | | 1.4 | | V |
| | | | 3V | 2.9 | | 2.9 | | 2.9 | | |
| | | | 4.5V | 4.4 | | | | | | |
| | | $I_{OH}$ = -4mA | 3V | 2.58 | | | | | | |
| | | $I_{OH}$ = -24mA | 4.5V | 3.94 | | | | | | |
| | | $I_{OH}$ = -50mA(1) | 5.5V | | | | | | | |
| | | $I_{OH}$ = -75mA(1) | 5.5V | | | | | | | |
| $V_{OL}$ | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = 50µA | 1.5V | | 0.1 | | 0.1 | | 0.1 | V |
| | | | 3V | | 0.1 | | 0.1 | | 0.1 | |
| | | | 4.5V | | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 12mA | 3V | | 0.36 | | 0.5 | | 0.44 | |
| | | $I_{OL}$ = 24mA | 4.5V | | 0.36 | | 0.5 | | 0.44 | |
| | | $I_{OL}$ = 50mA(1) | 5.5V | | | | 1.65 | | | |
| | | $I_{OL}$ = 75mA(1) | 5.5V | | | | | | 1.65 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | | 5.5V | | ±0.1 | | ±1 | | ±1 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND | $I_O$= 0 | 5.5V | | 8 | | 160 | | 80 | µA |
| $C_i$ | | | | | 10 | | 10 | | 10 | pF |

(1) Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C

## 5.6 Switching Characteristics - $V_{CC}$ = 1.5V

over recommended operating free-air temperature range, $C_L$ = 50pF (unless otherwise noted). See *Parameter Measurement Information*

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | -55°C to 125°C | | -40°C to 85°C | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | Any Y | | 106 | | 97 | ns |
| $t_{PHL}$ | | | | 106 | | 97 | |
| $t_{PLH}$ | $\overline{A}$/B | Any Y | | 180 | | 164 | ns |
| $t_{PHL}$ | | | | 180 | | 164 | |
| $t_{PLH}$ | $\overline{G}$ | Any Y | | 169 | | 154 | ns |
| $t_{PHL}$ | | | | 169 | | 154 | |

## 5.7 Switching Characteristics: $V_{CC}$ = 3.3V ±0.3V

over recommended operating free-air temperature range, $C_L$ = 50pF (unless otherwise noted). See *Parameter Measurement Information*

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | -55°C TO 125°C | | -40°C TO 85°C | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A to B | Any Y | 3 | 11.9 | 3.2 | 10.8 | ns |
| $t_{PHL}$ | | | 3 | 11.9 | 3.2 | 10.8 | |
| $t_{PLH}$ | $\overline{A}$/B | Any Y | 5.1 | 20.3 | 5.4 | 18.5 | ns |
| $t_{PHL}$ | | | 5.1 | 20.3 | 5.4 | 18.5 | |
| $t_{PLH}$ | $\overline{G}$ | Any Y | 4.7 | 18.9 | 5.1 | 17.2 | ns |
| $t_{PHL}$ | | | 4.7 | 18.9 | 5.1 | 17.2 | |

## 5.8 Switching Characteristics: $V_{CC}$ = 5V ±0.5V

over recommended operating free-air temperature range, $C_L$ = 50pF (unless otherwise noted). See *Parameter Measurement Information*

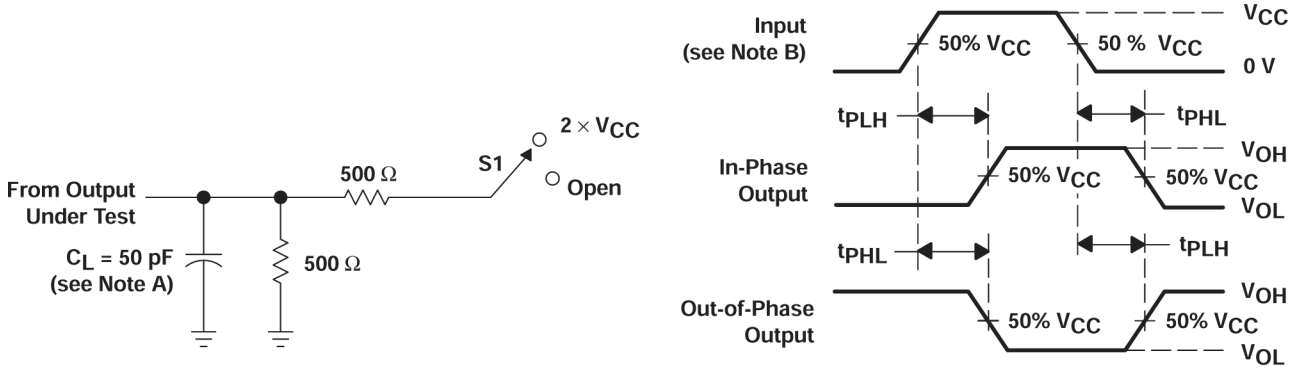
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | -55°C TO 125°C | | -40°C TO 85°C | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | Any Y | 2.1 | 8.5 | 2.2 | 7.7 | ns |
| $t_{PHL}$ | | | 2.1 | 8.5 | 2.2 | 7.7 | |
| $t_{PLH}$ | $\overline{A}$/B | Any Y | 3.6 | 14.5 | 3.8 | 13.2 | ns |
| $t_{PHL}$ | | | 3.6 | 14.5 | 3.8 | 13.2 | |
| $t_{PLH}$ | $\overline{G}$ | Any Y | 3.4 | 13.5 | 3.6 | 12.3 | ns |
| $t_{PHL}$ | | | 3.4 | 13.5 | 3.6 | 12.3 | |

## 5.9 Operating Characteristics

$V_{CC}$ = 5V, $T_A$ = 25°C

| PARAMETER | | TYP | UNIT |
|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | 156 | pF |

# 6 Parameter Measurement Information




A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
C. The outputs are measured one at a time with one input transition per measurement.

**Figure 6-1. Load Circuit and Voltage Waveforms**

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |

# 7 Detailed Description

## 7.1 Overview

The CDx4AC157 is a high speed silicon gate CMOS multiplexer an excellent choice for multiplexing and data routing applications. It contains four 2:1 multiplexers.

The CDx4AC157 operates asynchronously, with each Y output being equal to the input selected by the address input ($\overline{A}$/B). All four channels are controlled by the same address input.

The strobe ($\overline{G}$) input forces all Y outputs low, regardless of the state of other inputs.

## 7.2 Functional Block Diagram

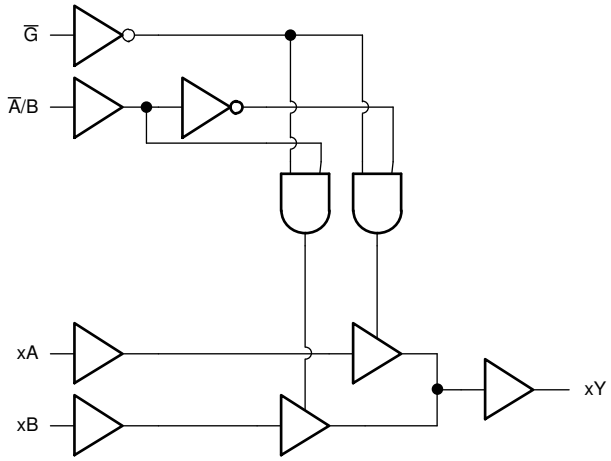



**Figure 7-1. Logic Diagram (Positive Logic) for CDx4AC157**

## 7.3 Feature Description

### *7.3.1 Balanced CMOS Push-Pull Outputs*

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important to limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs must be left disconnected.

### *7.3.2 Standard CMOS Inputs*

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at $V_{CC}$ or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; a 10kΩ resistor, however, is recommended and will typically meet all requirements.

### 7.3.3 Clamp Diode Structure

As shown in Figure 7-2, the inputs and outputs to this device have both positive and negative clamping diodes.

**CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

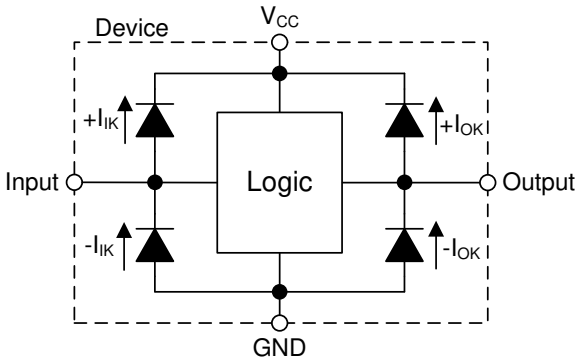



**Figure 7-2. Electrical Placement of Clamping Diodes for Each Input and Output**

## 7.4 Device Functional Modes

Function Table lists the functional modes of the CDx4AC157.

**Table 7-1. Function Table**

| INPUTS[1] | | | | OUTPUT |
|---|---|---|---|---|
| $\overline{G}$ | SELECT | DATA | | |
| | $\overline{A}$/B | A | B | Y |
| H | X | X | X | L |
| L | L | L | X | L |
| L | L | H | X | H |
| L | H | X | L | L |
| L | H | X | H | H |

(1) H = High Voltage Level, L = Low Voltage Level, X = Do not Care

# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

The CDx4AC157 is a quadruple 2-to-1 data selector/multiplexer. The following application shows an example of using the device with all required connections to switch a 4-bit data bus between two source devices.

## 8.2 Typical Application

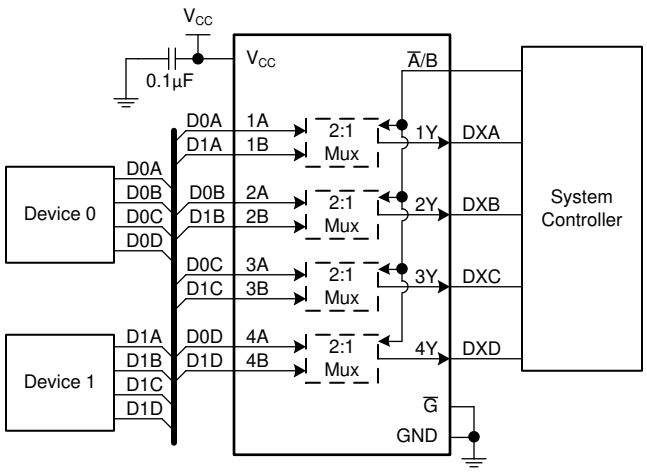



**Figure 8-1. Typical Application Block Diagram**

### *8.2.1 Design Requirements*

#### 8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the CDx4AC157 plus the maximum static supply current, $I_{CC}$, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through $V_{CC}$ listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the CDx4AC157 plus the maximum supply current, $I_{CC}$, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The CDx4AC157 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The CDx4AC157 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with $V_{OH}$ and $V_{OL}$. When outputting in the HIGH state, the

output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the $V_{CC}$ pin.

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and Cpd Calculation*.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*.

**CAUTION**

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

#### 8.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either $V_{CC}$ or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the CDx4AC157 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

The CDx4AC157 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

#### 8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the $V_{OH}$ specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the $V_{OL}$ specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to $V_{CC}$ or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

### *8.2.2 Detailed Design Procedure*

1. Add a decoupling capacitor from $V_{CC}$ to GND. The capacitor needs to be placed physically close to the device and electrically close to both the $V_{CC}$ and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the CDx4AC157 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than ($V_{CC}$ / $I_{O(max)}$)Ω. Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.

4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

### 8.2.3 Application Curve

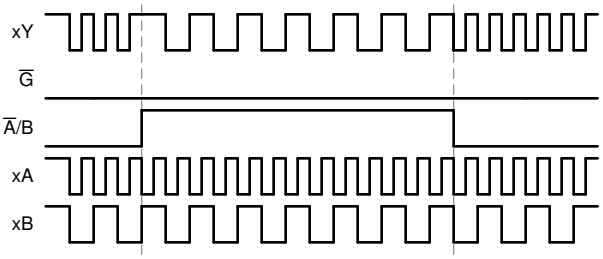



**Figure 8-2. Application Timing Diagram**

## 8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Recommended Operating Conditions*.

Each $V_{CC}$ terminal should have a good bypass capacitor to prevent power disturbance. For the CDx4AC157, a 0.1µF bypass capacitor is recommended. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1µF and 1µF are commonly used in parallel.

## 8.4 Layout

### 8.4.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - Parallel traces must be separated by at least 3x dielectric thickness
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer each signal that must branch separately

### 8.4.2 Layout Example

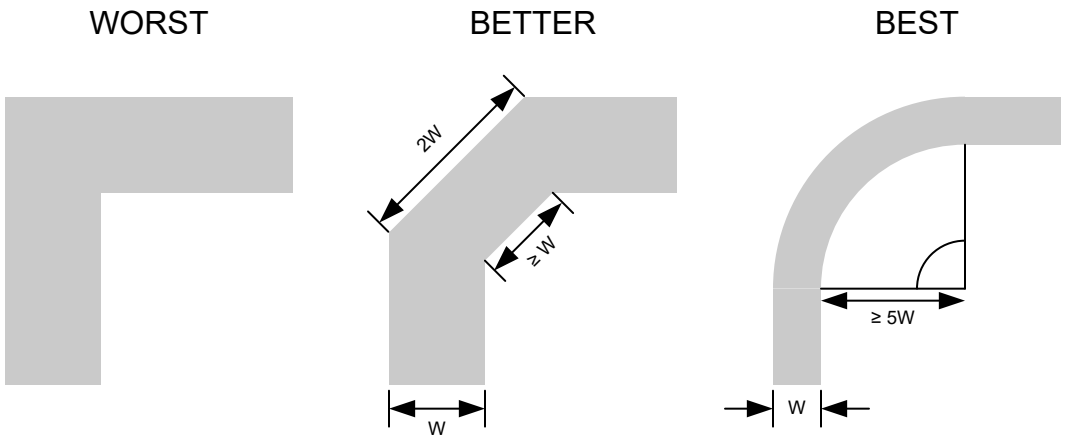



**Figure 8-3. Example Trace Corners for Improved Signal Integrity**

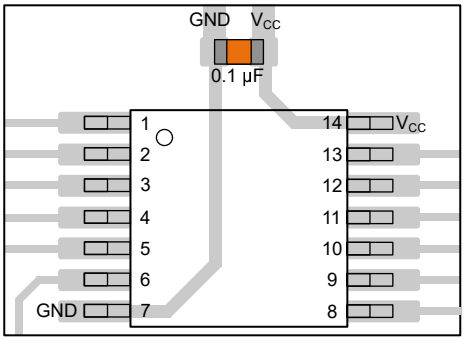



**Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages**

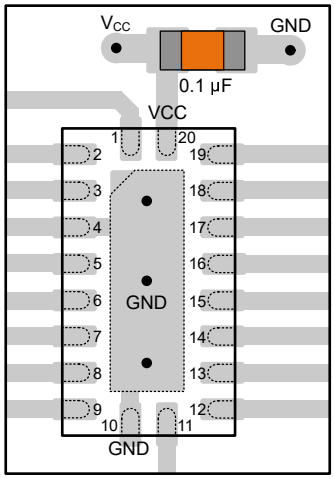



**Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages**

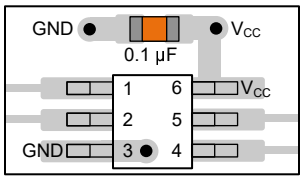



**Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages**

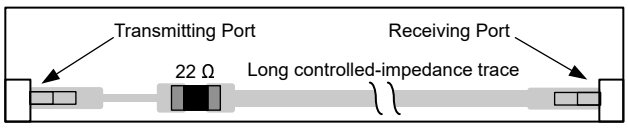



**Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity**

# 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 9.1 Documentation Support

### *9.1.1 Related Documentation*

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and $C_{pd}$ Calculation* application report
- Texas Instruments, *Designing With Logic* application report
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application report

## 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 9.4 Trademarks

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All trademarks are the property of their respective owners.

## 9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

## 10 Revision History

| Changes from Revision * (March 2003) to Revision A (June 2025) | Page |
|---|---|
| • Updated the numbering format for tables, figures, and cross-references throughout the document | 1 |
| • Added BQB package to the data sheet | 1 |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| CD54AC157F3A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | CD54AC157F3A |
| CD54AC157F3A.A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | CD54AC157F3A |
| CD74AC157BQBR | Active | Production | WQFN (BQB) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AC157 |
| CD74AC157E | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74AC157E |
| CD74AC157E.A | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74AC157E |
| CD74AC157M | Obsolete | Production | SOIC (D) \| 16 | - | - | Call TI | Call TI | -55 to 125 | AC157M |
| CD74AC157M96 | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AC157M |
| CD74AC157M96.A | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AC157M |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD54AC157, CD74AC157 :**

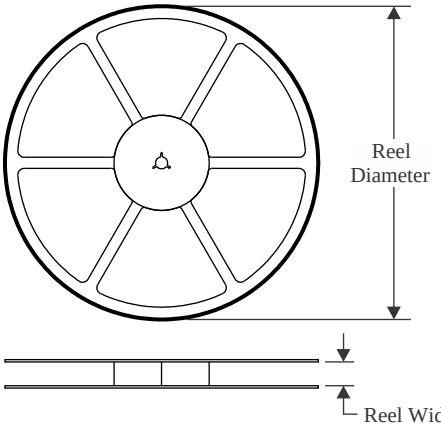
- Catalog : CD74AC157
- Military : CD54AC157

NOTE: Qualified Version Definitions:

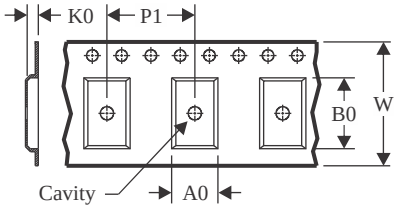
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

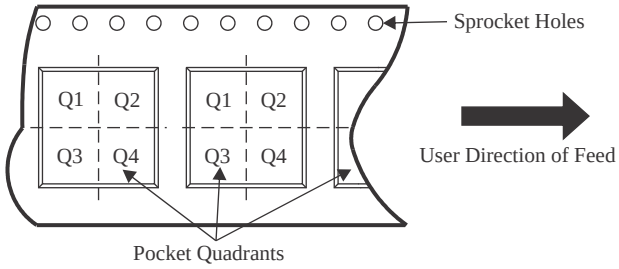



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

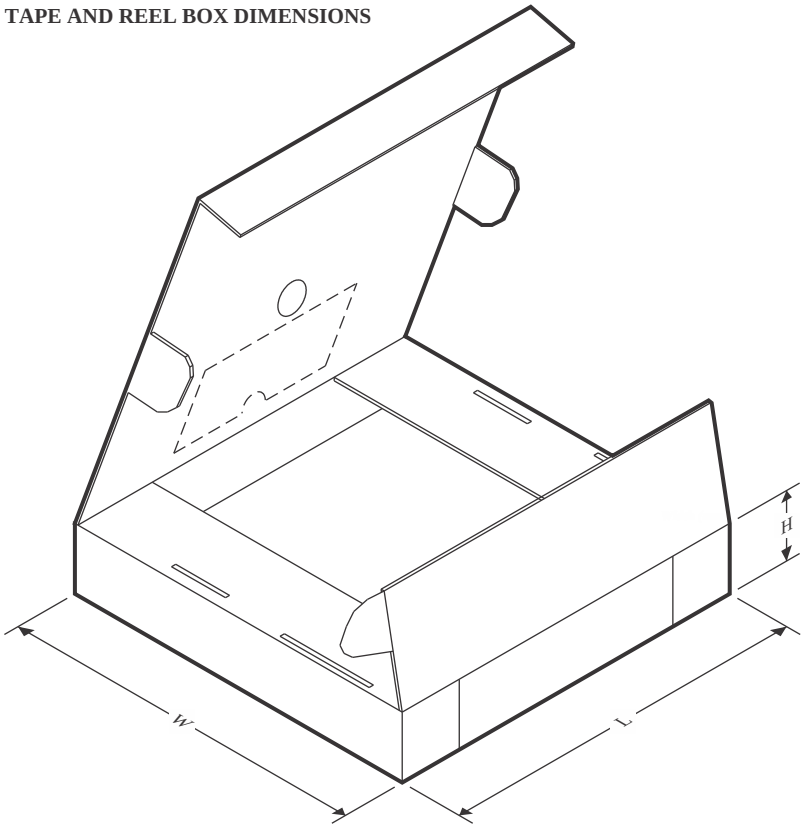
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CD74AC157BQBR | WQFN | BQB | 16 | 3000 | 180.0 | 12.4 | 2.8 | 3.8 | 1.2 | 4.0 | 12.0 | Q1 |
| CD74AC157M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

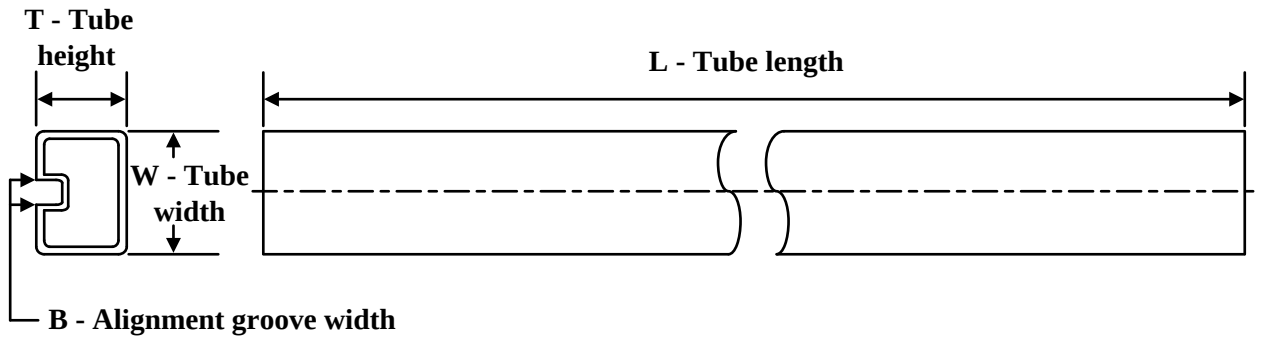
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CD74AC157BQBR | WQFN | BQB | 16 | 3000 | 210.0 | 185.0 | 35.0 |
| CD74AC157M96 | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| CD74AC157E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74AC157E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74AC157E.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74AC157E.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |

# GENERIC PACKAGE VIEW

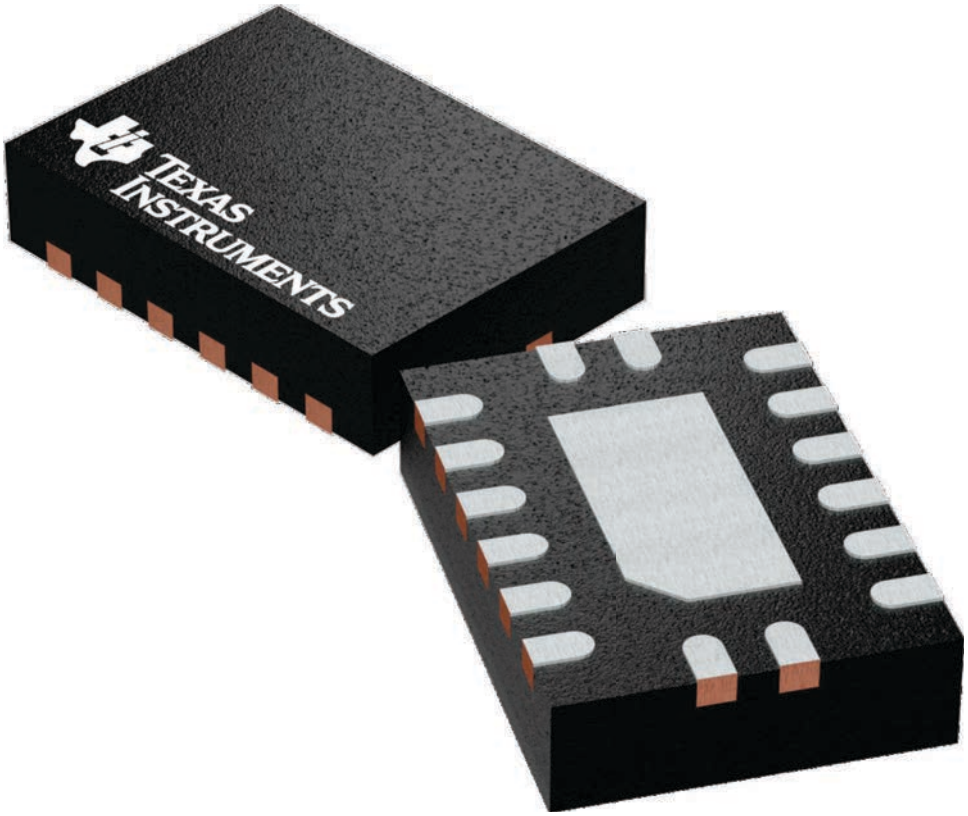
## BQB 16

## WQFN - 0.8 mm max height

**2.5 x 3.5, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



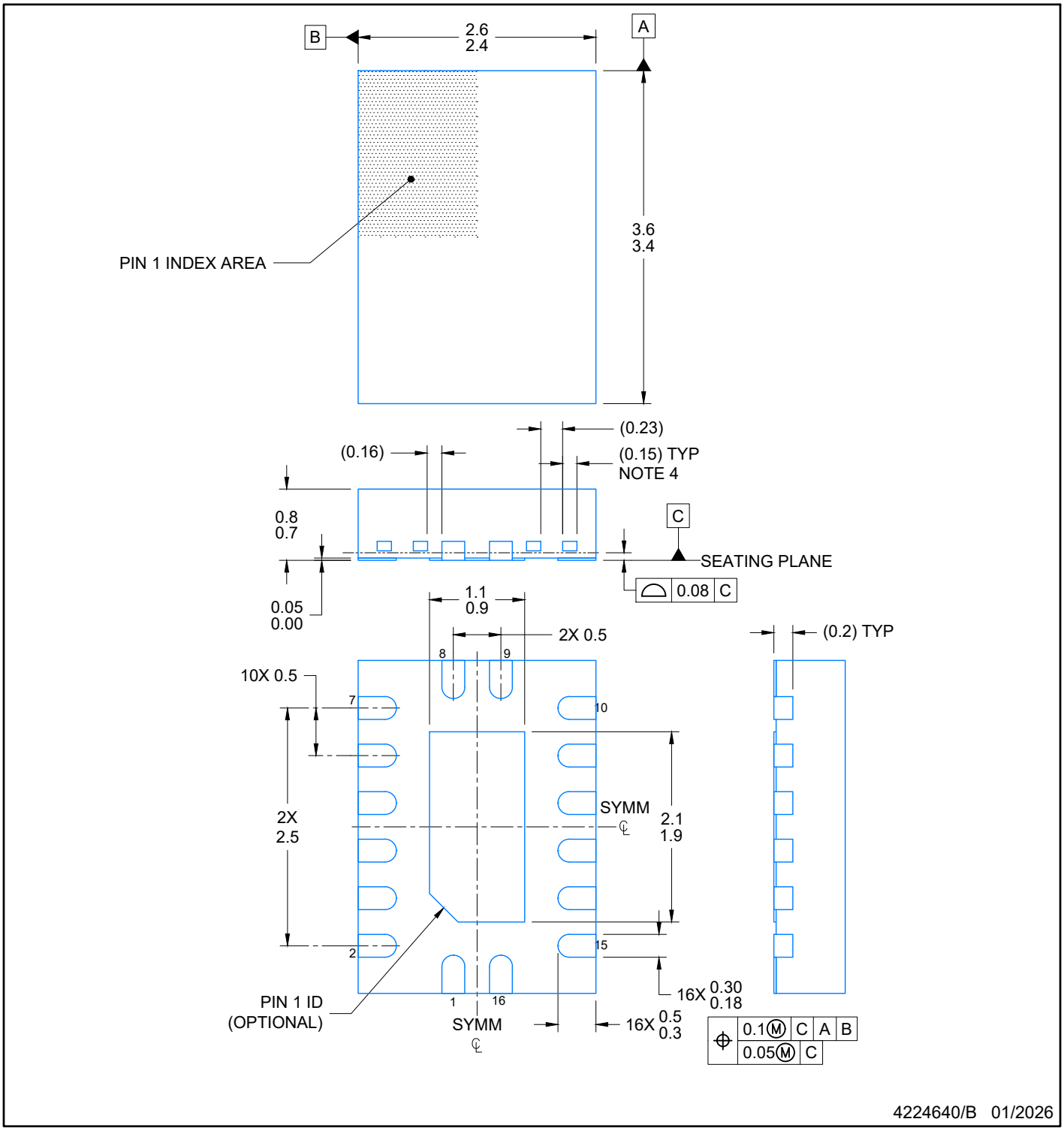

4226161/A

# PACKAGE OUTLINE

## BQB0016A

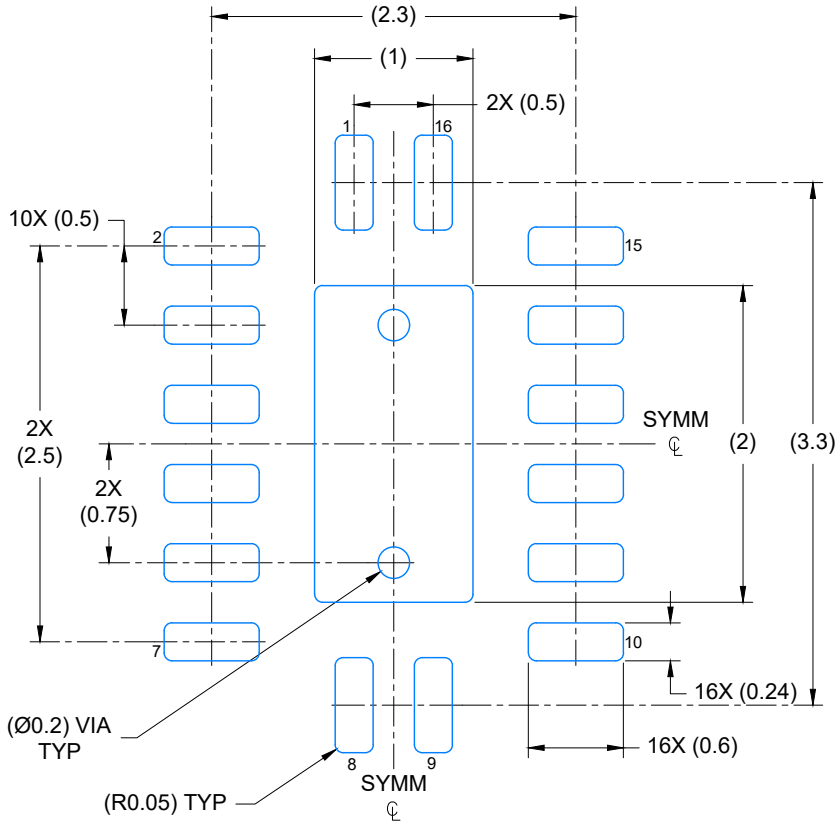
## WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

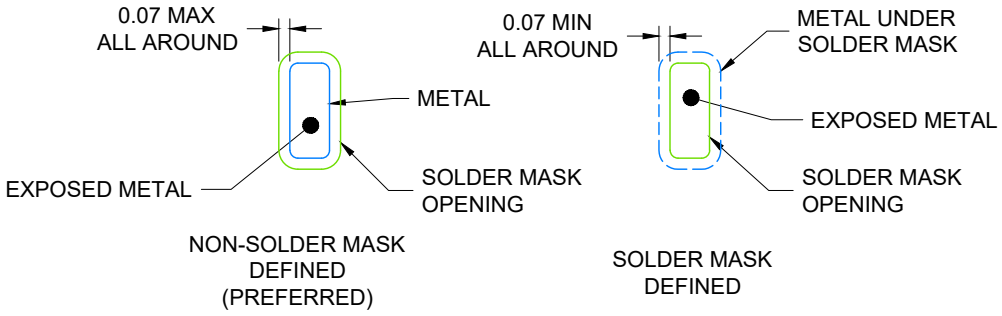



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may differ or may not be present




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

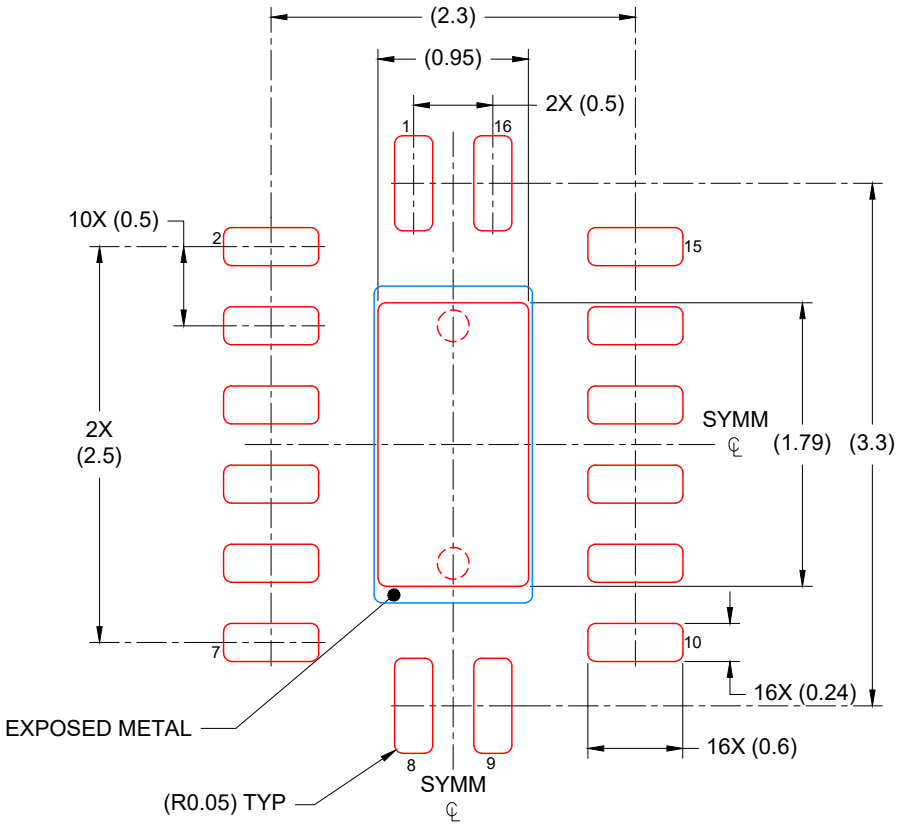



4224640/B 01/2026

1. NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

4224640/B 01/2026

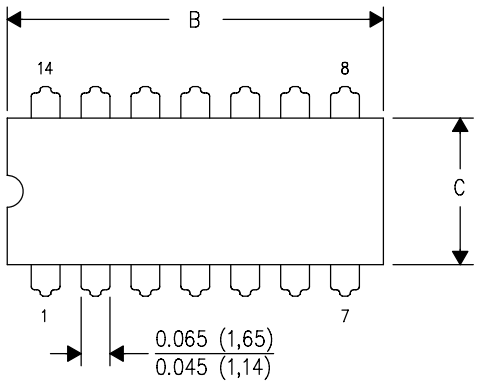
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

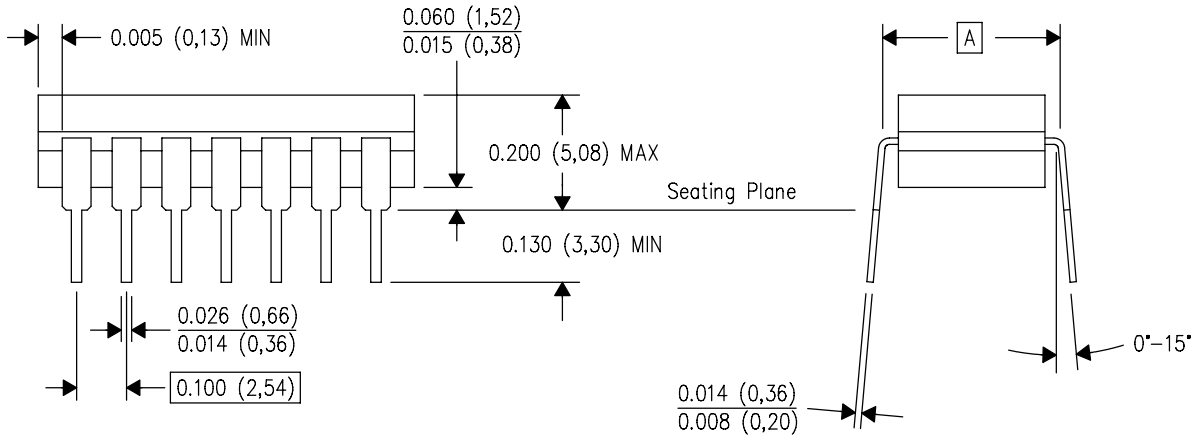
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



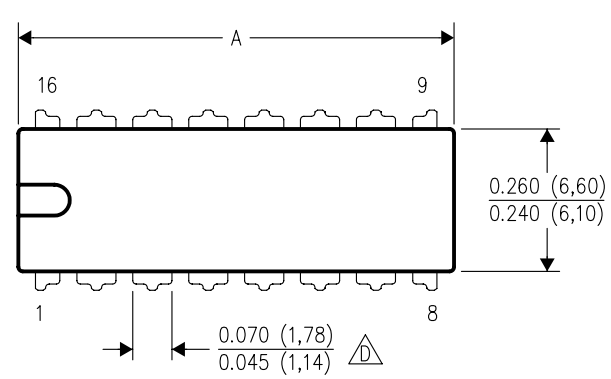

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

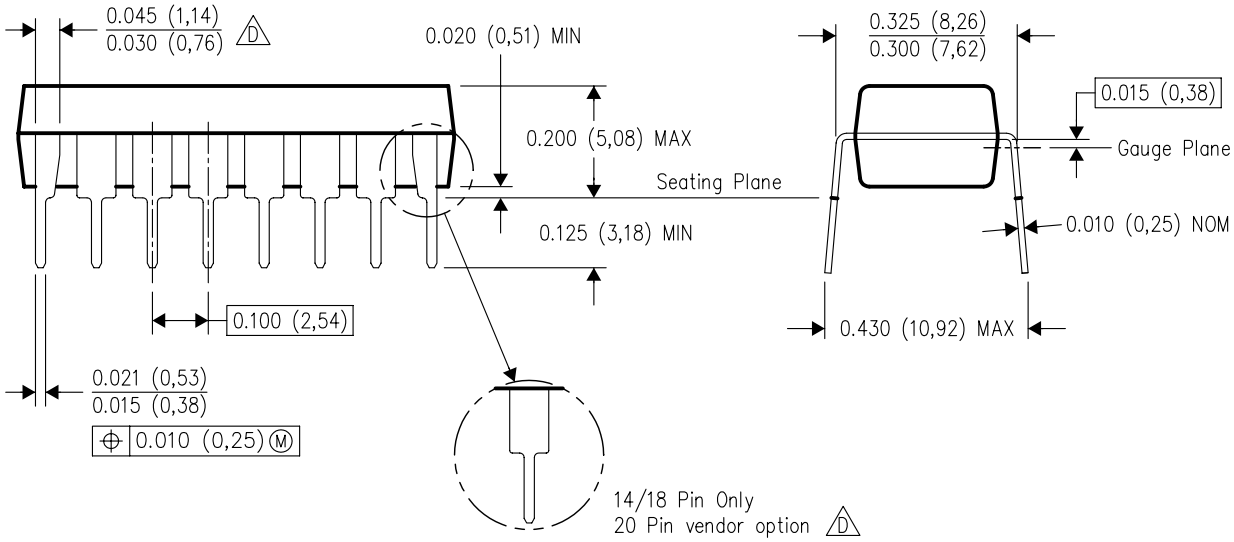
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



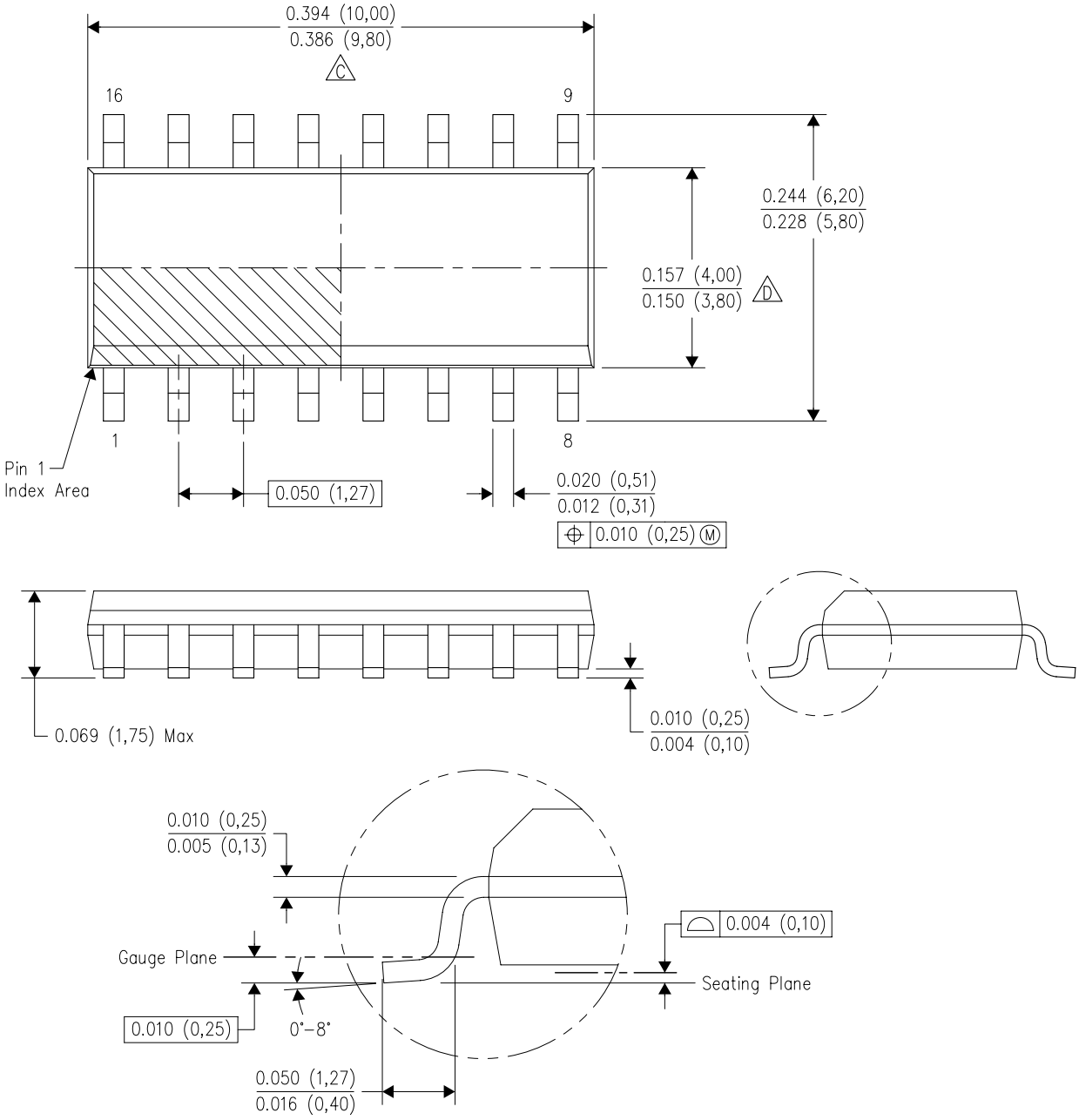

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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Last updated 10/2025