CD74AC238 3-Line to 8-Line Decoder/Demultiplexer

1 Features

- AC types feature 1.5V to 5.5V operation and balanced noise immunity at 30% of the supply voltage
- Speed of bipolar F, AS, and S, with significantly reduced power consumption
- Designed specifically for high-speed memory decoders and data-transmission systems
- Incorporates three enable inputs to simplify cascading and/or data reception
- Balanced propagation delays
- ±24mA output drive current
  - Fanout to 15 F devices
- SCR-latchup-resistant CMOS process and circuit design
- Exceeds 2kV ESD protection per MIL-STD-883, method 3015

2 Description

The CD74AC238 decoder/demultiplexer is designed for high-performance memory-decoding and data-routing applications that require very short propagation-delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding.

Package Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]	BODY SIZE[3]
CD74AC238	BQB (WQFN, 16)	3.5mm × 2.5mm	3.5mm × 2.5mm
	D (SOIC, 16)	9.9mm × 6mm	9.9mm × 3.9mm
	PW (TSSOP, 16)	5.00mm × 6.4mm	5.00mm × 4.40mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.
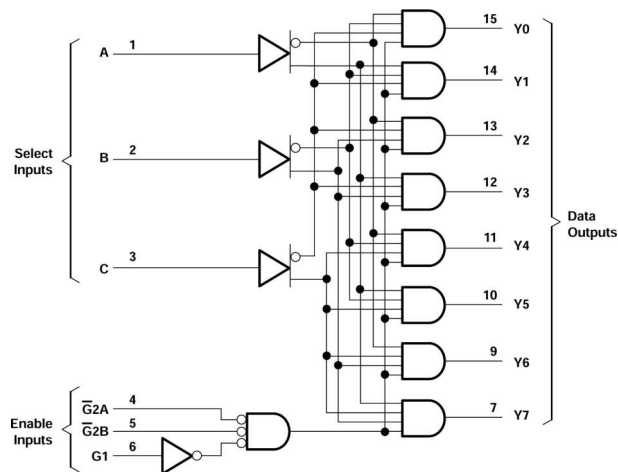
Table of Contents

3 Pin Configuration and Functions

Figure 3-1. CD74AC238 D or PW Package; 16-Pin SOIC or TSSOP (Top View)
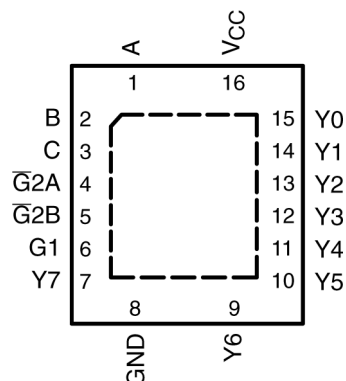
Figure 3-2. CD74AC238 BQB Package, 16-Pin WQFN (Top View)

Table 3-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
A	1	I	Input A
B	2	I	Input B
C	3	I	Input C
$\overline{G}$2A	4	I	Strobe Input 2A, active low
$\overline{G}$2B	5	I	Strobe Input 2B, active low
G1	6	I	Strobe Input
Y7	7	O	Output 7
GND	8	G	Ground
Y6	9	O	Output 6
Y5	10	O	Output 5
Y4	11	O	Output 4
Y3	12	O	Output 3
Y2	13	O	Output 2
Y1	14	O	Output 1
Y0	15	O	Output 0
V_{CC}	16	P	Positive Supply
Thermal Pad[2]		—	Thermal Pad

(1)   I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.
(2)   BQB package only

Product Folder Links: *CD74AC238*

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	6	V
I_{IK} [2]	Input clamp current	(V_I < 0 V or V_I > V_{CC})		±20	mA
I_{OK} [2]	Output clamp current	(V_O < 0 V or V_O > V_{CC})		±50	mA
I_O	Continuous output current	(V_O > 0 V or V_O < V_{CC})		±50	mA
	Continuous current through V_{CC} or GND			±200	mA
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

4.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)[1]

			T_A = 25°C		-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		1.5	5.5	1.5	5.5	1.5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 1.5 V	1.2		1.2		1.2		V
		V_{CC} = 3 V	2.1		2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 1.5 V		0.3		0.3		0.3	V
		V_{CC} = 3 V		0.9		0.9		0.9	
		V_{CC} = 5.5 v		1.65		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 4.5 V to 5.5 V		-24		-24		-24	mA
I_{OL}	Low-level output current	V_{CC} = 4.5 V to 5.5 V		24		24		24	mA
Δt/Δv	Input transition rise or fall rate	V_{CC} = 1.5 V to 3 V		50		50		50	ns/V
		V_{CC} = 3.6 V to 5.5 V		20		20		20	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

4.4 Thermal Information

THERMAL METRIC[1]	CD74AC238			UNIT
	BQB (WQFN)	D (SOIC)	PW (TSSOP)	
	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$ Junction-to-ambient thermal resistance	83.9	106.6	126.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25 °C		-55°C to 125°C		-40°C to 85°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = -50 µA	1.5 V	1.4		1.4		1.4		V
			3 V	2.9		2.9		2.9		
			4.5 V	4.4		4.4		4.4		
		I_{OH} = -4 mA	3 V	2.58		2.4		2.48		
		I_{OH} = -24 mA	4.5 V	3.94		3.7		3.8		
		I_{OH} = -50 mA[1]	5.5 V			3.85				
		I_{OH} = -75 mA[1]	5.5 V					3.85		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 50 µA	1.5 V		0.1		0.1		0.1	V
			3 V		0.1		0.1		0.1	
			4.5 V		0.1		0.1		0.1	
		I_{OL} = 12 mA	3 V		0.36		0.5		0.44	
		I_{OL} = 24 mA	4.5 V		0.36		0.5		0.44	
		I_{OL} = 50 mA[1]	5.5 V				1.65			
		I_{OL} = 75 mA[1]	5.5 V						1.65	
I_I	$V_I = V_{CC}$ or GND		5.5 V		±0.1		±1		±1	µA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	5.5 V		8		160		80	µA
C_i					10		10		10	pF

(1) Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.

4.6 Switching Characteristics, V_{CC} = 1.5 V

over recommended operating free-air temperature range, V_{CC} = 1.5 V, C_L = 50 pF (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	A, B, C	Any Y		187		170	ns
t_{PHL}				187		170	
t_{PLH}	G1	Any Y		208		189	ns
t_{PHL}				208		189	
t_{PLH}	G2A, G2B	Any Y		149		135	ns
t_{PHL}				149		135	

4.7 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V, C_L = 50 pF (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	A, B, C	Any Y	5.3	21	5.4	19.1	ns
t_{PHL}			5.3	21	5.4	19.1	
t_{PLH}	G1	Any Y	5.8	23.2	6	21.1	ns
t_{PHL}			5.8	23.2	6	21.1	
t_{PLH}	$\overline{G2A}$, $\overline{G2B}$	Any Y	4.2	16.7	4.3	15.2	ns
t_{PHL}			4.2	16.7	4.3	15.2	

4.8 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V, C_L = 50 pF (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

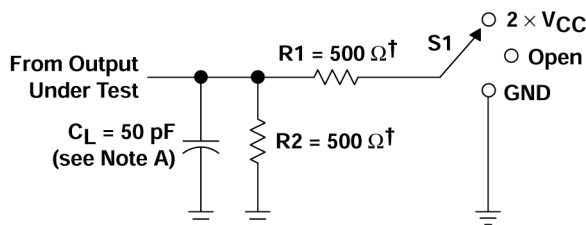| PARAMETER	FROM (INPUT)	TO (OUTPUT)	-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	A, B, C	Any Y	3.8	15	3.9	13.6	ns
t_{PHL}			3.8	15	3.9	13.6	
t_{PLH}	G1	Any Y	4.2	16.6	4.3	15.1	ns
t_{PHL}			4.2	16.6	4.3	15.1	
t_{PLH}	G2A, G2B	Any Y	3	11.9	3.1	10.7	ns
t_{PHL}			3	11.9	3.1	10.7	

4.9 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TYP	UNIT
C_{pd}	Power dissipation capacitance	110	pF

5 Parameter Measurement Information

LOAD CIRCUIT

From Output Under Test

R1 = 500 Ω† S1 2 × V_{CC} ○
○ Open
○ GND

C_L = 50 pF (see Note A)
R2 = 500 Ω†

† When V_{CC} = 1.5 V, R1 = R2 = 1 kΩ
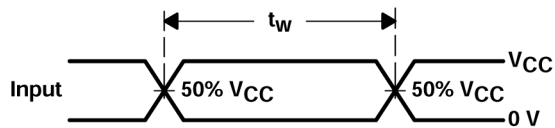
VOLTAGE WAVEFORMS PULSE DURATION

t_W

Input 50% V_{CC} 50% V_{CC} V_{CC} 0 V
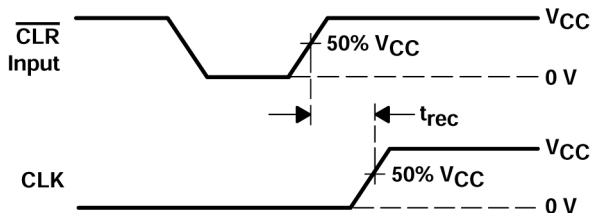
VOLTAGE WAVEFORMS RECOVERY TIME

$\overline{CLR}$ Input 50% V_{CC} V_{CC} 0 V

t_{rec}

CLK 50% V_{CC} V_{CC} 0 V
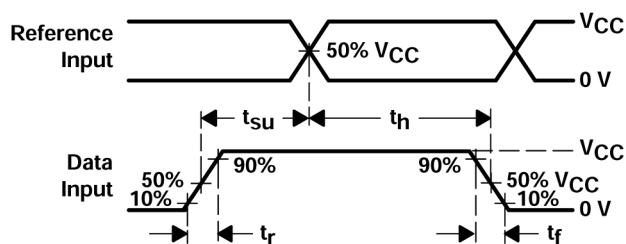
VOLTAGE WAVEFORMS SETUP AND HOLD AND INPUT RISE AND FALL TIMES

Reference Input 50% V_{CC} V_{CC} 0 V

t_{su} t_h

Data Input 50% 10% 90% 90% 50% V_{CC} 10% V_{CC} 0 V

t_r t_f
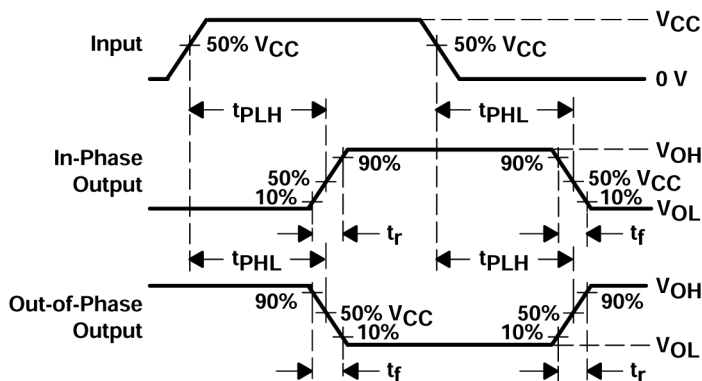
VOLTAGE WAVEFORMS PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

Input 50% V_{CC} 50% V_{CC} V_{CC} 0 V

t_{PLH} t_{PHL}

In-Phase Output 50% 10% 90% 90% 50% V_{CC} 10% V_{OH} V_{OL}

t_r t_f

t_{PHL} t_{PLH}

Out-of-Phase Output 90% 50% V_{CC} 10% 50% 10% 90% V_{OH} V_{OL}

t_f t_r
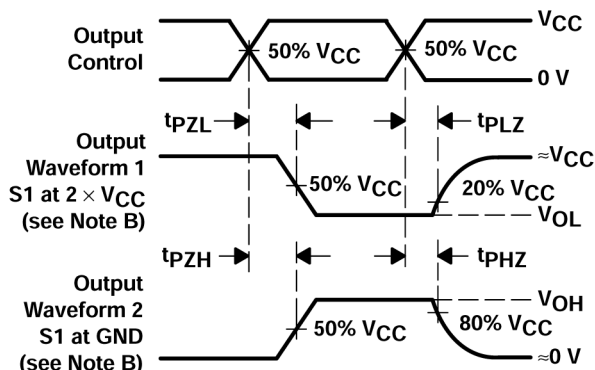
VOLTAGE WAVEFORMS OUTPUT ENABLE AND DISABLE TIMES

Output Control 50% V_{CC} 50% V_{CC} V_{CC} 0 V

t_{PZL} t_{PLZ}

Output Waveform 1 S1 at 2 × V_{CC} (see Note B) 50% V_{CC} 20% V_{CC} ≈V_{CC} V_{OL}

t_{PZH} t_{PHZ}

Output Waveform 2 S1 at GND (see Note B) 50% V_{CC} 80% V_{CC} V_{OH} ≈0 V

A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns. Phase relationships between waveforms are arbitrary.
D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. t_{PLH} and t_{PHL} are the same as t_{pd}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
I. All parameters and waveforms are not applicable to all devices.

Figure 5-1. Load Circuit and Voltage Waveforms

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

6 Detailed Description

6.1 Overview

When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory usually are less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

The conditions at the binary-select inputs and the three enable inputs select one of eight output lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications (see Application Information).

6.2 Functional Block Diagram
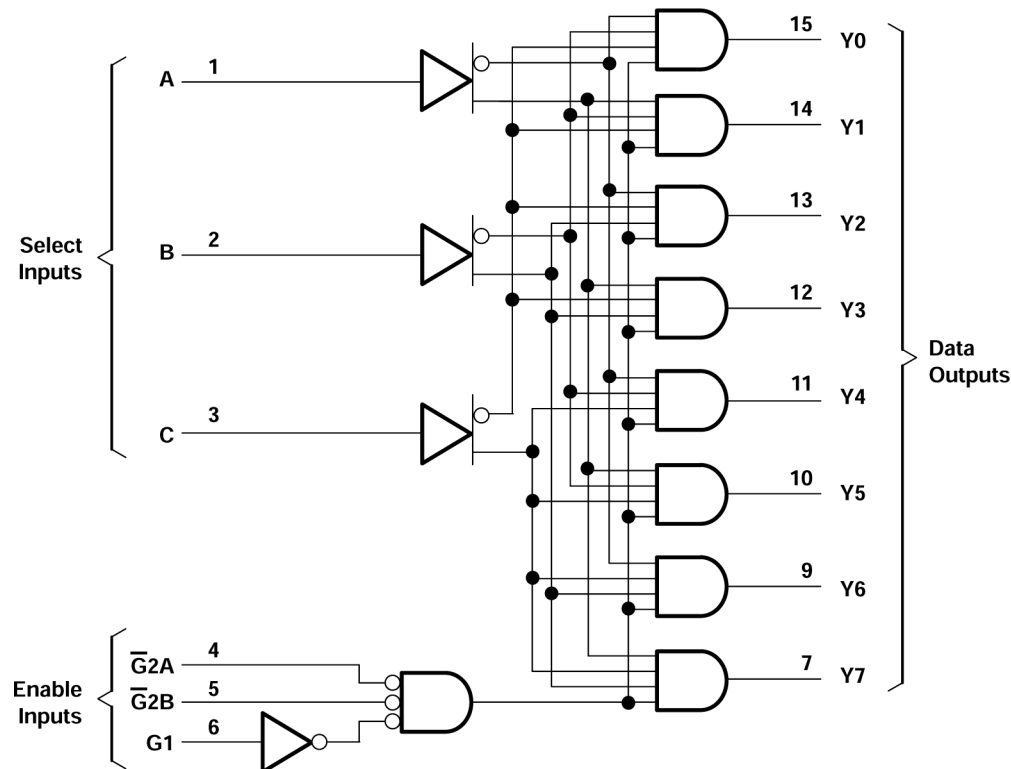
Figure 6-1. Logic Diagram (Positive Logic)

6.3 Device Functional Modes

Table 6-1. Function Table

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	L	L	L	L	L	L	L	L
X	X	H	X	X	X	L	L	L	L	L	L	L	L
L	X	X	X	X	X	L	L	L	L	L	L	L	L
H	L	L	L	L	L	H	L	L	L	L	L	L	L
H	L	L	L	L	H	L	H	L	L	L	L	L	L
H	L	L	L	H	L	L	L	H	L	L	L	L	L
H	L	L	L	H	H	L	L	L	H	L	L	L	L
H	L	L	H	L	L	L	L	L	L	H	L	L	L
H	L	L	H	L	H	L	L	L	L	L	H	L	L

Table 6-1. Function Table (continued)

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
H	L	L	H	H	L	L	L	L	L	L	L	H	L
H	L	L	H	H	H	L	L	L	L	L	L	L	H

Product Folder Links: *CD74AC238*

7 Application Information
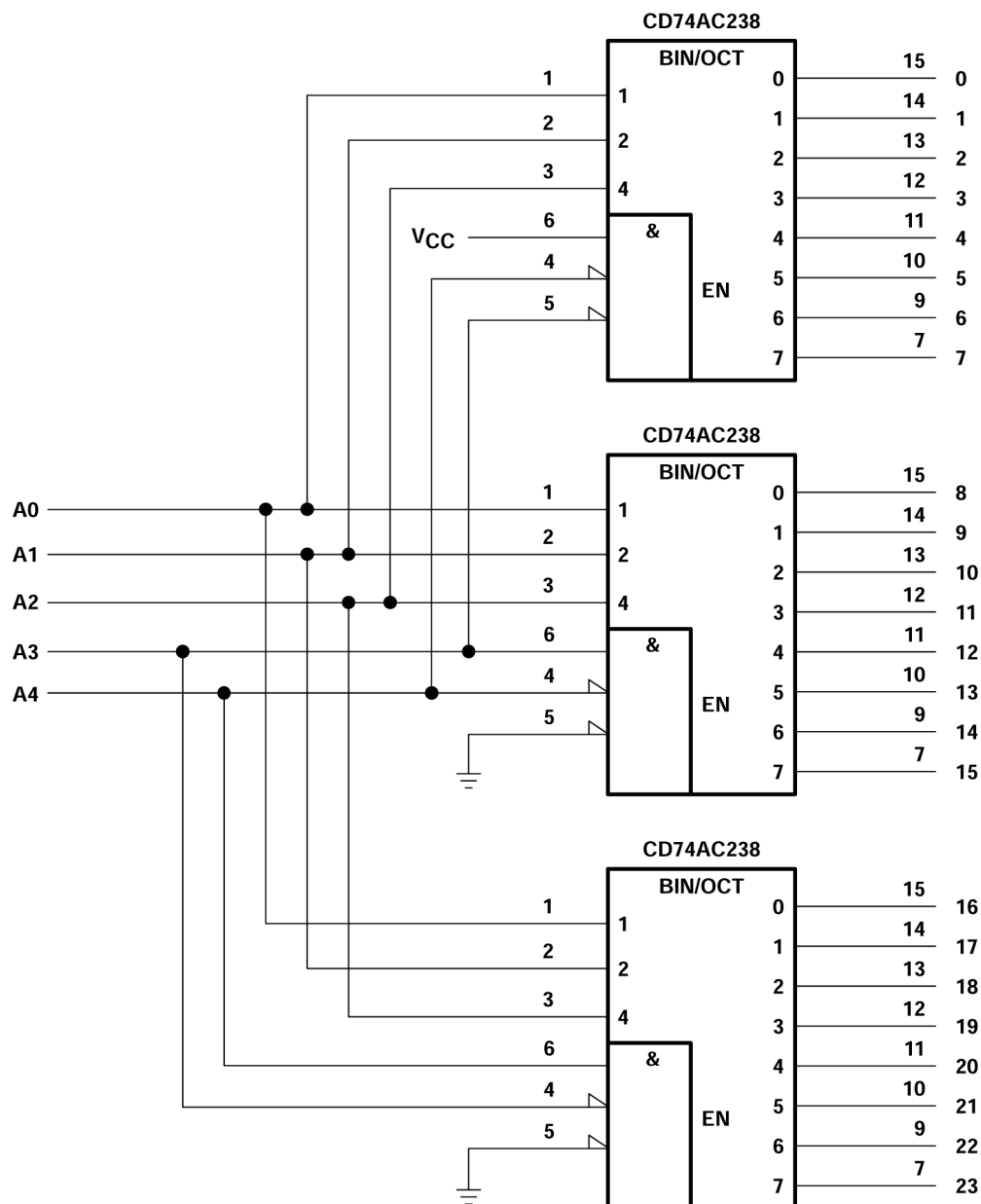
Figure 7-1. 24-Bit Decoding Scheme
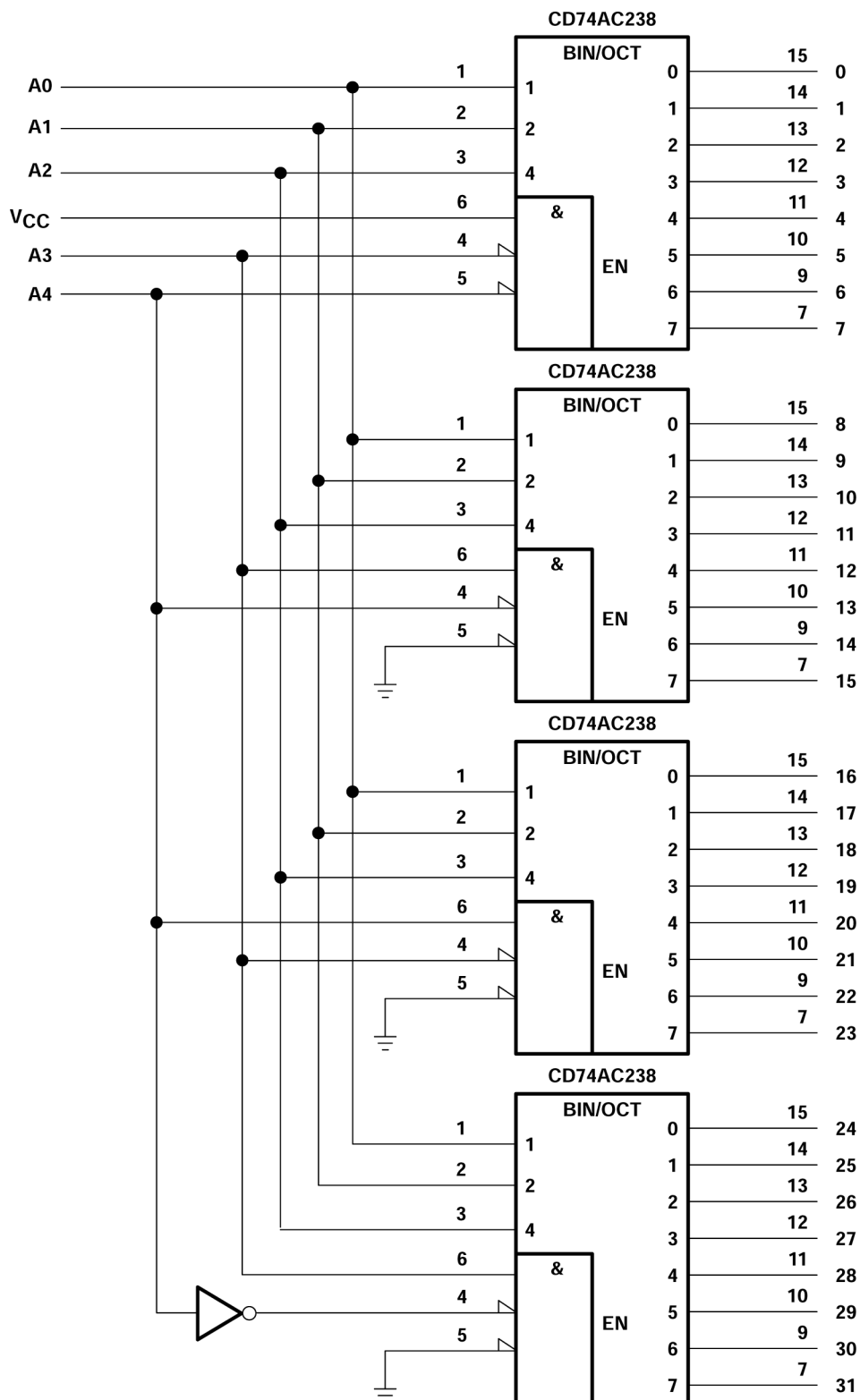
Figure 7-2. 32-Bit Decoding Scheme

7.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

7.2 Layout

7.2.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.
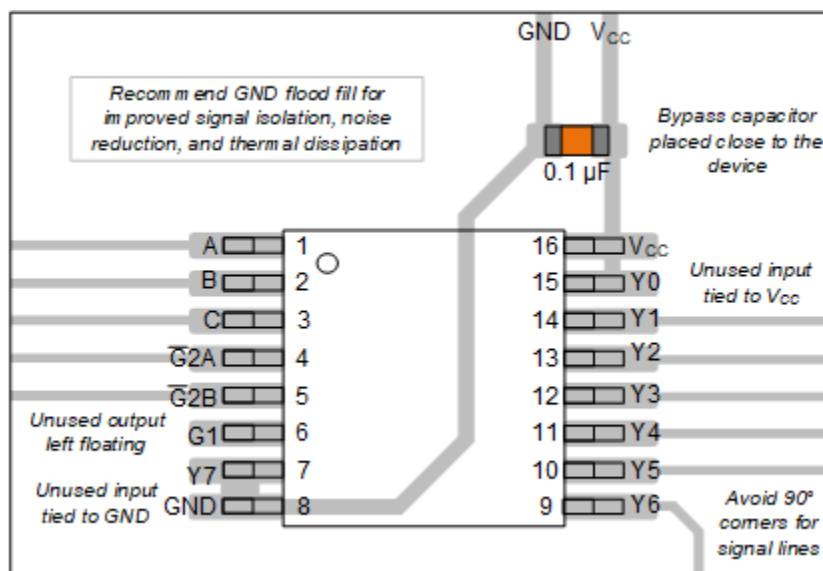
7.2.2 Layout Example

Figure 7-3. Example Layout for the CD74AC238

8 Device and Documentation Support

8.1 Documentation Support (Analog)

8.1.1 Related Documentation

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
CD74AC238	Click here	Click here	Click here	Click here	Click here

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD74AC238BQBR	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC238
CD74AC238BQBR.A	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC238
CD74AC238M96	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC238M
CD74AC238M96.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC238M
CD74AC238PWR	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	AC238
CD74AC238PWR.A	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC238

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
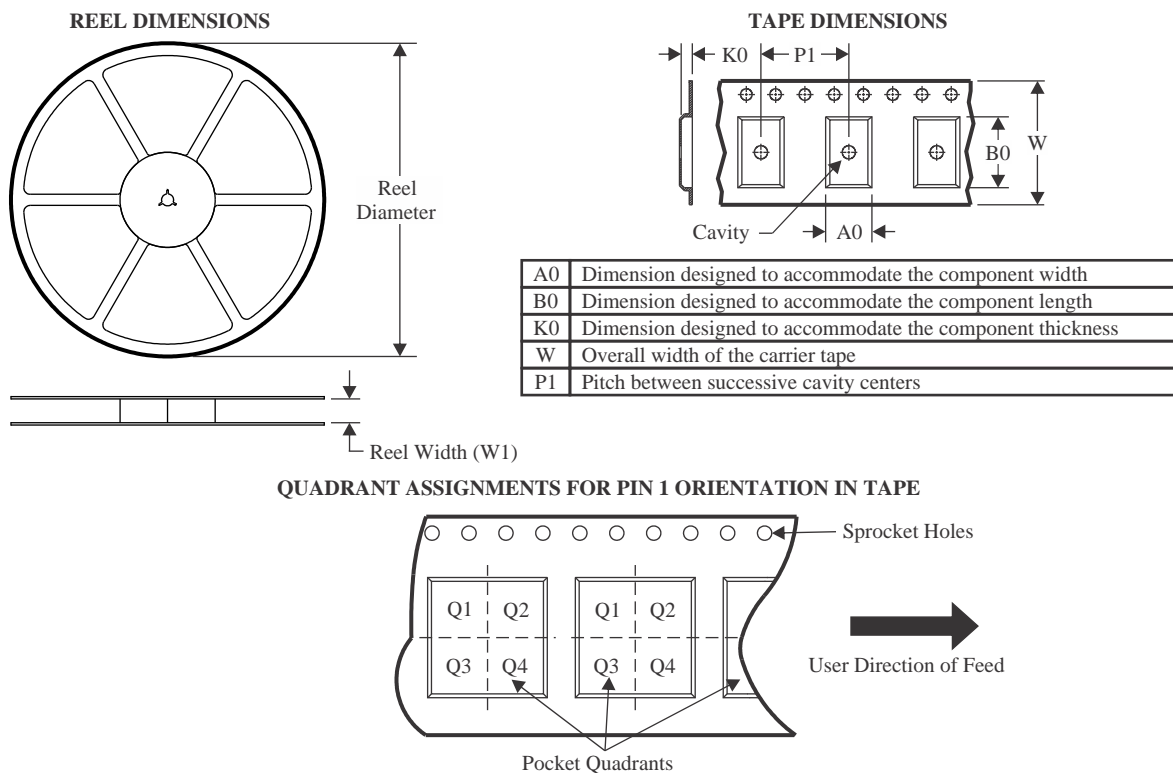
(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC238BQBR	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
CD74AC238M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74AC238M96	SOIC	D	16	2500	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
CD74AC238PWR	TSSOP	PW	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC238BQBR	WQFN	BQB	16	3000	210.0	185.0	35.0
CD74AC238M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74AC238M96	SOIC	D	16	2500	340.5	336.1	32.0
CD74AC238PWR	TSSOP	PW	16	3000	353.0	353.0	32.0

D (R−PDSO−G16) PLASTIC SMALL OUTLINE

0.394 (10,00)
0.386 (9,80)
⚠C

16 9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) ⚠D

1 8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25) 0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−6/M 06/11
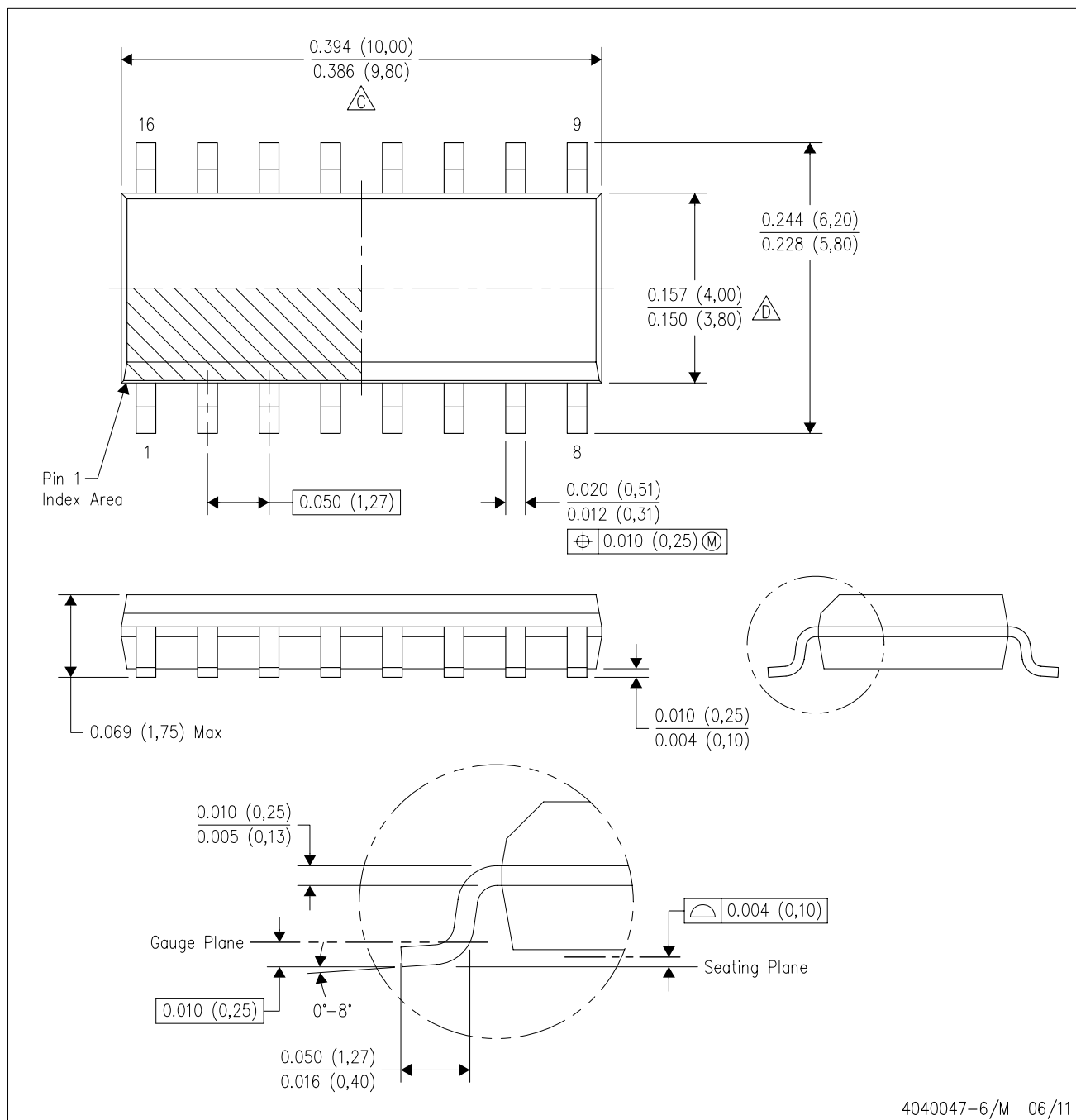
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
⚠C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
⚠D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS−012 variation AC.

BQB 16

2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4226161/A

B

2.6
2.4

A

PIN 1 INDEX AREA

3.6
3.4

(0.23)

(0.16)

(0.15) TYP
NOTE 4

0.8
0.7

C

SEATING PLANE

0.05
0.00

0.08 C

(0.2) TYP

1.1
0.9

2X 0.5

8   9

10X 0.5

7

10

2X
2.5

SYMM

2.1
1.9

2

15

PIN 1 ID
(OPTIONAL)

16X 0.30
0.18

1   16

SYMM

SYMM

16X 0.5
0.3

0.1 (M) C A B
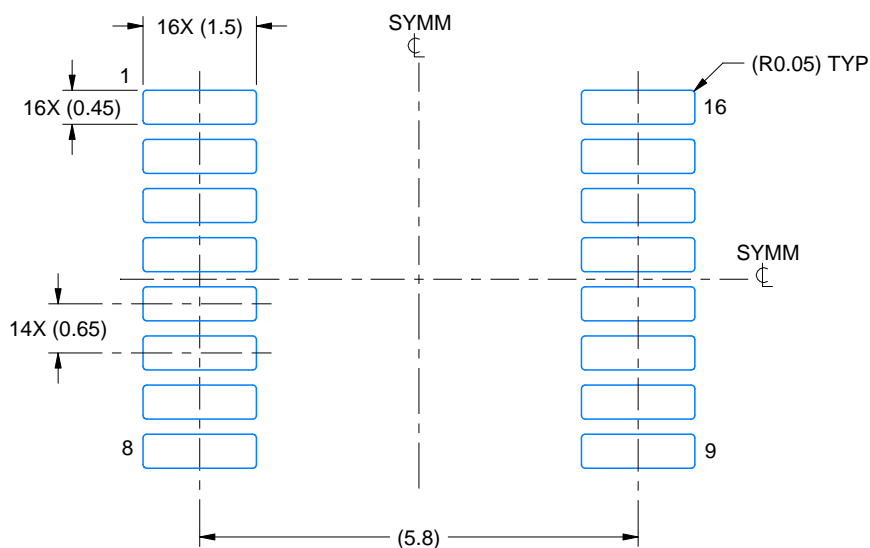0.05 (M) C
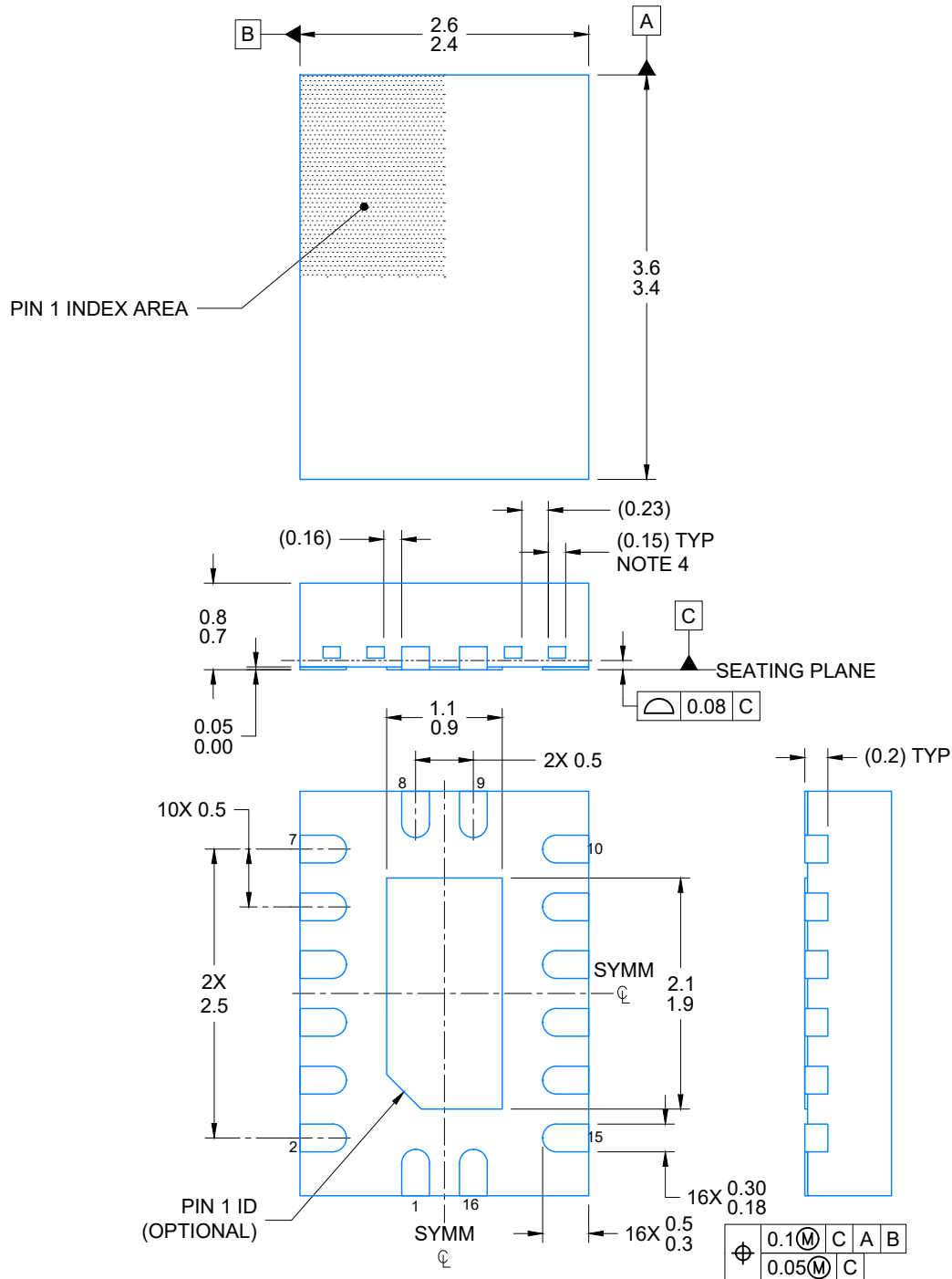
4224640/B   01/2026

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may differ or may not be present

(2.3)

(1)

2X (0.5)

1   16

10X (0.5)

2   15

2X
(2.5)

2X
(0.75)

SYMM
℄

(2)   (3.3)

7   10

(Ø0.2) VIA
TYP

16X (0.24)

16X (0.6)

(R0.05) TYP

8   9

SYMM
℄

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

METAL UNDER
SOLDER MASK

METAL

EXPOSED METAL

EXPOSED METAL

SOLDER MASK
OPENING

SOLDER MASK
OPENING

NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED
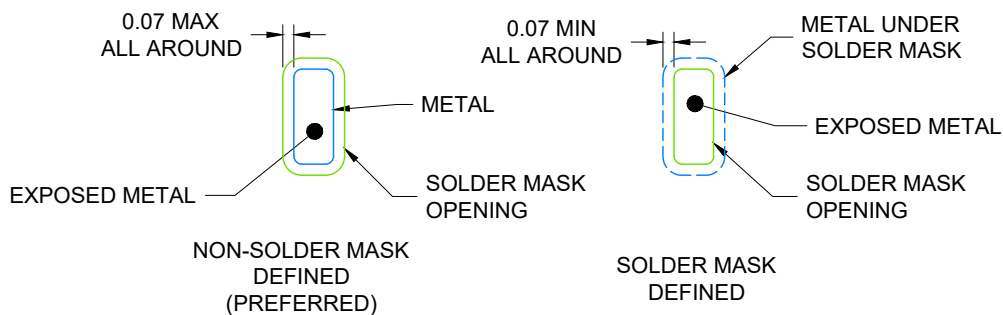
4224640/B   01/2026

1.   NOTES: (continued)

5.   This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

6.   Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

(2.3)

(0.95)

2X (0.5)

10X (0.5)

2X (2.5)

SYMM

(1.79) (3.3)

1

16

2

15

7

10

EXPOSED METAL

(R0.05) TYP

8

9

SYMM

16X (0.24)

16X (0.6)
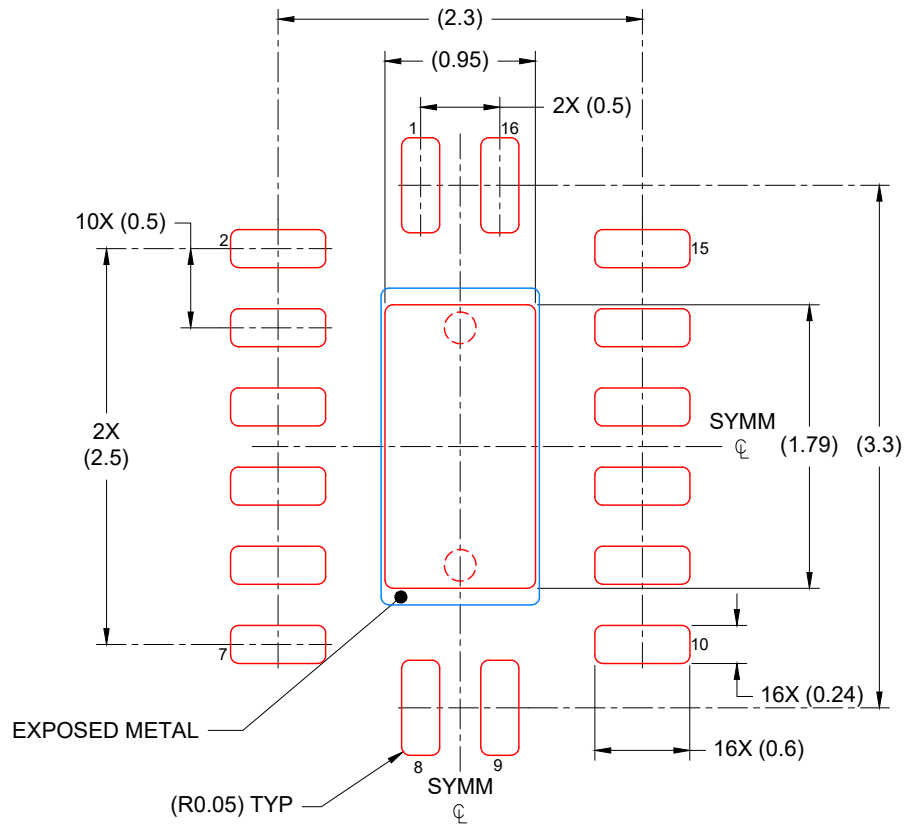
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

4224640/B   01/2026

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

SEATING PLANE

C

⌒ 0.1 C

6.6 / 6.2 TYP

A

PIN 1 INDEX AREA

14X 0.65

16

2X 4.55

5.1 / 4.9 NOTE 3

1

8

9

16X 0.30 / 0.17

⊕ 0.1 Ⓜ C A B

B

4.5 / 4.3 NOTE 4

4X (0°-12°)

1.2 MAX

SEE DETAIL A

(0.15) TYP

0.25 GAGE PLANE

0.15 / 0.05

0.75 / 0.50

0°-8°

DETAIL A
TYPICAL
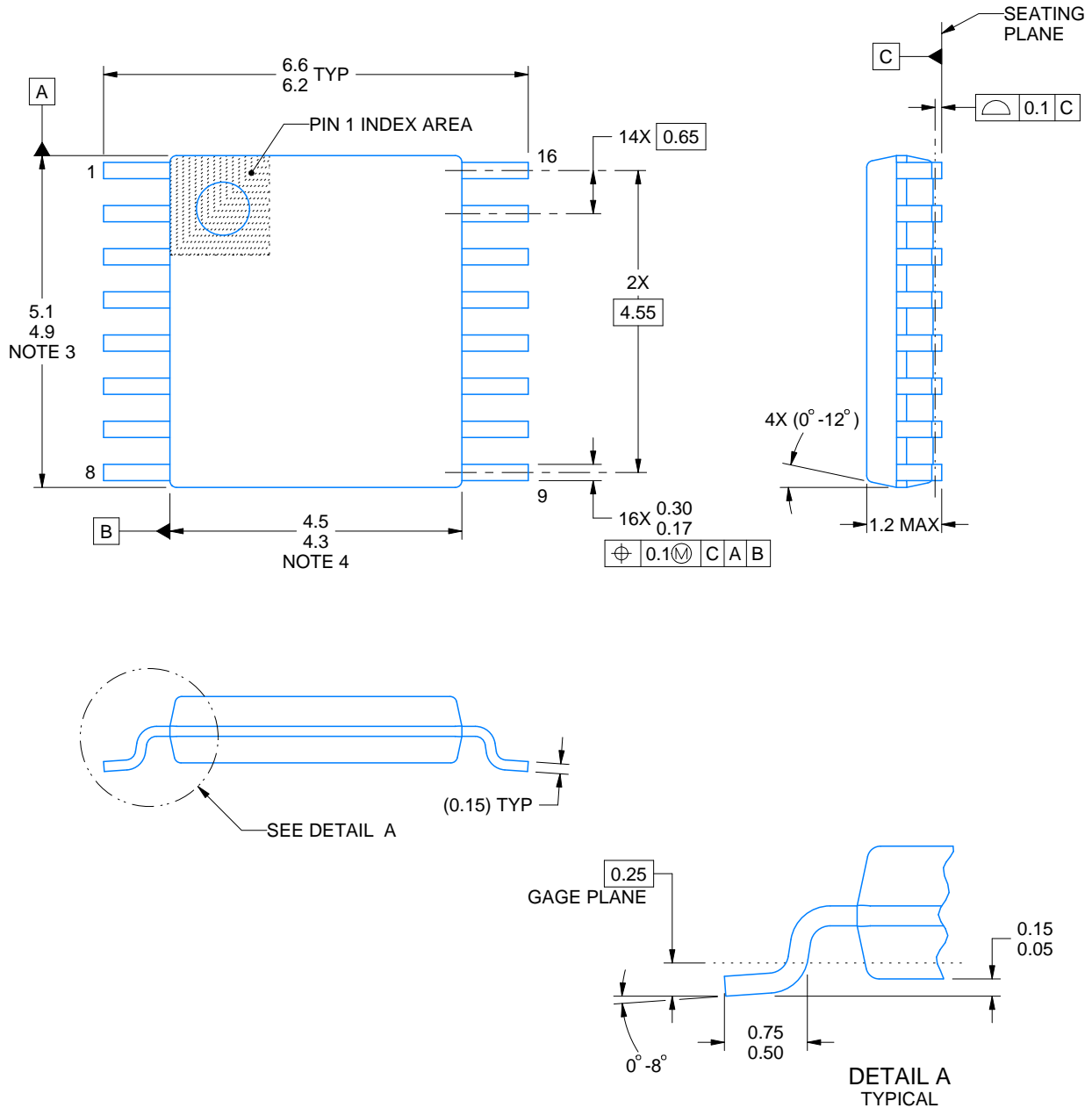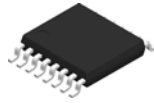
4220204/B   12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

16X (1.5)

SYMM

1

16X (0.45)

(R0.05) TYP

16

SYMM

14X (0.65)

8

9

(5.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED
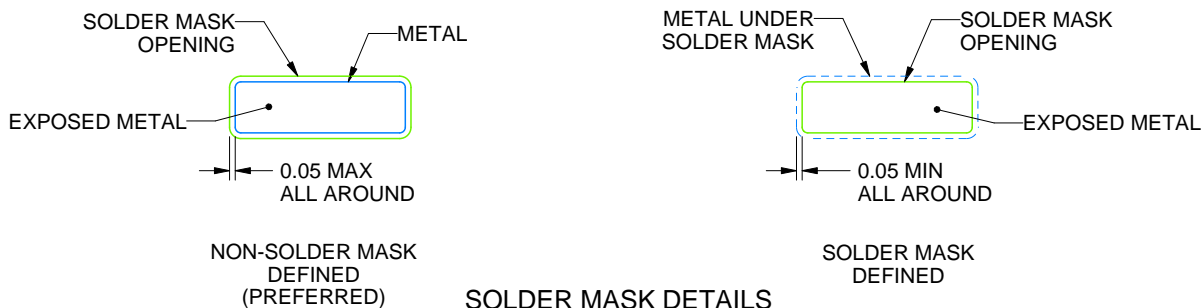
SOLDER MASK DETAILS

4220204/B   12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

16X (1.5)

SYMM

1

16X (0.45)

(R0.05) TYP

16

SYMM

14X (0.65)

8

9

(5.8)
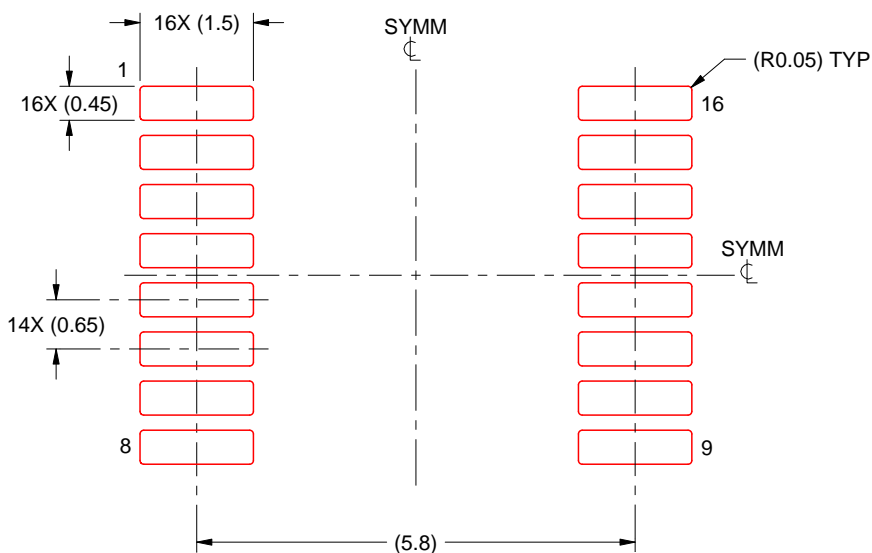
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B   12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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