CDx4AC574, CDx4ACT574 Octal D-Type Flip-Flop, 3-State Positive-Edge-Triggered

1 Features

- SCR-latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST*/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5V to 5.5V *operation and balanced noise immunity at 30% of the supply*
- ± 24mA output drive current
  - Fanout to 15 FAST* ICs
  - Drives 50ohm transmission lines

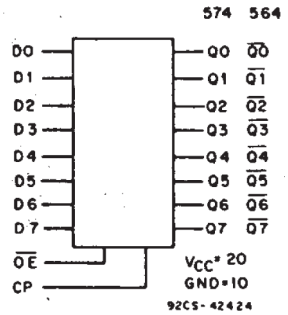
2 Description

The CDx4AC574 and the CDx4ACT574 octal D-type, 3-state, positive-edge-triggered flip-flops use the RCA ADVANCED CMOS technology.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
CDx4AC/ACT574	DW (SOIC, 20)	12.80mm × 10.3mm	12.80mm × 7.50mm
	N (PDIP, 20)	24.33mm × 9.4mm	24.33mm × 6.35mm

(1) For all available packages, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Functional Block Diagram

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

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3 Pin Configuration and Functions

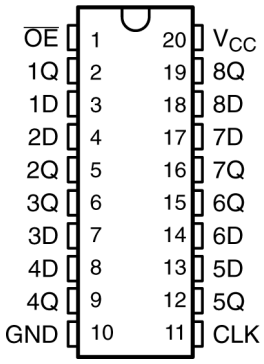

Figure 3-1. CDx4AC/ACT574 DW Package, 20-Pin SOIC; N Package, 20-Pin PDIP (Top View)

Table 3-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
$\overline{OE}$	1	I	Active low enable
1Q	2	O	Data output
1D	3	I	Data input
2D	4	I	Data input
2Q	5	O	Data output
3Q	6	O	Data output
3D	7	I	Data input
4D	8	I	Data input
4Q	9	O	Data output
GND	10	-	Ground pin
CLK	11	I	Clock pin
5Q	12	O	Data output
5D	13	I	Data input
6D	14	I	Data input
6Q	15	O	Data output
7Q	16	O	Data output
7D	17	I	Data input
8D	18	I	Data input
8Q	19	O	Data output
V_{CC}	20	-	Power pin

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4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply-voltage		-0.5	6	V
I_{IK}	Input diode current	(V_I < -0.5 V or V_I > V_{CC} + 0.5 V)		±20	mA
I_{Ok}	Output diode current	(V_o < -0.5 V or Vo > V_{CC} + 0.5 V)		±50	mA
I_O	Output source or sink current per output pin	(V_O > -0.5 V or V_O < V_{CC} ± 0.5 V)		±50	mA
	V_{CC} or ground current (I_{CC} or I_{GND})			±100	mA(2)
T_{stg}	Storage temperature		-65	+150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For up to 4 outputs per device; add ± 25 mA for each additional output.

4.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

	CHARACTERISTIC	MIN	MAX	UNIT
V_{CC} (2)	Supply-voltage range: (For T_A = full package-temperature range)			
	AC types	1.5	5.5	V
	ACT types	4.5	5.5	V
V_I, V_O	Input or output voltage	0	V_{CC}	V
T_A	Operating temperature	-55	+ 125	°C
dt/dv	Input rise and fall slew rate			
	at 1.5 V to 3 V (AC types)	0	50	ns/V
	at 3.6 V to 5.5 V (AC types)	0	20	ns/V
	at 4.5 V to 5.5 V (ACT types)	0	10	ns/V

(1) All unused inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report: Implications of Slow or FLoating CMOS Inputs.
(2) Unless otherwise specified, all voltages are referenced to ground.

4.4 Thermal Information

THERMAL METRIC(1)		CDx4AC/ACT574		UNIT
		DW (SOIC)	N (PDIP)	
		20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	101.2	50	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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4.5 Static Electrical Characteristics: AC Series

CHARACTERISTICS		TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNIT
					+25		-40 to +85		-55 to +125		
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
V_{IH}	High-Level Input Voltage			1.5	1.2	—	1.2	—	1.2		
				3	2.1	—	2.1	—	2.1	—	V
				5.5	3.85	—	3.85	—	3.85	—	
V_{IL}	Low-Level Input Voltage			1.5	—	0.3	—	0.3	—	0.3	
				3	—	0.9	—	0.9	—	0.9	V
				5.5	—	1.65	—	1.65	—	1.65	
V_{OH}	High-Level Output Voltage	V_{IH} or V_{IL} (1), (2)	-0.05	1.5	1.4	—	1.4	—	1.4		
			-0.05	3	2.9	—	2.9	—	2.9	—	
			-0.05	4.5	4.4	—	4.4	—	4.4	—	
			-4	3	2.58	—	2.48	—	2.4	—	V
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
V_{OL}	Low-Level Output Voltage	V_{IH} or V_{IL} (1), (2)	0.05	1.5	—	0.1	—	0.1	—	0.1	
			0.05	3	—	0.1	—	0.1	—	0.1	
			0.05	4.5	—	0.1	—	0.1	—	0.1	
			12	3	—	0.36	—	0.44	—	0.5	V
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
I_I	Input Leakage Current	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
I_{OZ}	3-State Leakage Current	V_{IH} or V_{IL} V_O = V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
I_{CC}	Quiescent Supply Current, MSI	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

(1) Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
(2) Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C. 75 ohms at +125°C.

4.6 Static Electrical Characteristics: ACT Series

CHARACTERISTICS		TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNIT
					+25		-40 to +85		-55 to.+125		
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
V_{IH}	High-Level Input Voltage			4.5 to 5.5	2	—	2	—	2	—	V
V_{IL}	Low-Level Input Voltage			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
V_{OH}	High-Level Output Voltage	V_{IH} or V_{IL} (1), (2)	-0.05	4.5	4.4	—	4.4	—	4.4	—	
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	V
			-50	5.5	—	—	—	—	3.85	—	

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CHARACTERISTICS		TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNIT
					+25		-40 to +85		-55 to.+125		
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
V_{OL}	Low-Level Output Voltage	V_{IH} or V_{IL} (1). (2)	0.05	4.5	—	±0.1	—	±.1	—	±.1	V
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
I_I	Input Leakage Current	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
I_{OZ}	3-State Leakage Current	V_{IH} or V_{IL} V_O = V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
I_{CC}	Quiescent Supply Current, MSI	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
ΔI_{CC}	Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

(1) Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
(2) Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at + 125°C.

Table 4-1. Act Input Loading Table

INPUT	UNIT LOADS(1)
D, $\overline{OE}$	0-7
CP	1.17

(1) Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

4.7 Prerequisite for Switching: AC Series

SYMBOL	CHARACTERISTICS	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) -°C				UNIT
			-40 to +85		-55 to +125		
			MIN	MAX	MIN	MAX	
t_W	Clock Pulse Width	1.5	44	—	50	—	ns
		3.3(1)	4.9	—	5.6	—	
		5(2)	3.5	—	4	—	
t_{SU}	Setup Time Data to Clock	1.5	2	—	2	—	ns
		3.3	2	—	2	—	
		5	2	—	2	—	
t_H	Hold Time Data to Clock	1.5	2	—	2	—	ns
		3.3	2	—	2	—	
		5	2	—	2	—	
f_{MAX}	Maximum Clock Frequency	1.5	11	—	10	—	MHz
		3.3	101	—	89	—	
		5	143	—	125	—	

(1) 3.3 V; min. is @ 3 V
(2) 5 V: min. is @ 4.5 V

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4.8 Switching Characteristics: AC Series

$_r$ t_l = 3 ns, C_L = 50 pF

SYMBOL	CHARACTERISTICS	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) -°C				UNIT
			-40 to +85		-55 to +125		
			MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation Delays: Clock to Q AC574	1.5	—	123	—	135	ns
		3.3[1]	4	13.7	3.8	15.1	
		5[2]	2.9	9.8	2.7	10.8	
t_{PLH} t_{PHL}	Clock to $\overline{Q}$ AC564	1.5	—	128	—	141	ns
		3.3	4.1	14.4	4	15.8	
		5	2.9	10.3	2.8	11.3	
t_{PZL} t_{PZH}	Output Enable to Q, $\overline{O}$	1.5	—	165	—	181	ns
		3.3	5.6	19.2	5.5	21.8	
		5	3.7	13.2	3.6	14.5	
t_{PLZ} t_{PHZ}	Output Disable to Q, $\overline{Q}$	1.5	—	165	—	181	ns
		3.3	4.7	16.5	4.5	18.1	
		5	3.7	13.2	3.6	14.5	
C_{PD} [3]	Power Dissipation Capacitance	—		67 Typ.		67 Typ.	pF
V_{OHV}	Min. (Valley) V_{OH}		4 Typ. @25°C				V
	During Switching of Other Outputs (Output Under Test Not Switching)	5					
V_{OLP}	Max. (Peak) V_{OL}		1 Typ. @25°C				V
	During Switching of Other Outputs (Output Under Test Not Switching)	5					
C_I	Input Capacitance	—	—	10	—	10	pF
C_O	3-State Output Capacitance	—	—	15	—	15	pF

(1) 3.3 V: min. is @ 3.6 V
(2) 5 V: min. is @ 5.5 V
(3) C_{PD} is used to determine the dynamic power consumption, per flip flop.

4.9 Prerequisite for Switching: ACT Series

SYMBOL	CHARACTERISTICS	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) -°C				UNIT
			-40 to +85		-55 to+125		
			MIN	MAX	MIN	MAX	
t_W	Clock Pulse Width	5[1]	3.9	—	4.5	—	ns
t_{SU}	Setup Time Data to Clock	5	2	—	2	—	ns
t_H	Hold Time Data to Clock	5	2.6	—	3	—	ns
f_{MAX}	Maximum Clock Frequency	5	125	—	110	—	MHz

(1) 5 V: min. is @ 4.5 V

4.10 Switching Characteristics: ACT Series

t_r, t, = 3 ns, C_L - 50 pF

SYMBOL	CHARACTERISTICS	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) -°C				UNITS
			-40 to +85		-55 to	+125	
			MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation Delays: Clock to Q ACT574	5[1]	2.9	10.2	2.8	11.2	ns
t_{PLH} t_{PHL}	Clock to $\overline{Q}$ ACT564	5	3	10.6	2.9	11.7	ns

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t_r, t, = 3 ns, C_L - 50 pF

SYMBOL	CHARACTERISTICS	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) -°C				UNITS
			-40 to +85		-55 to	+125	
			MIN	MAX	MIN	MAX	
t_{PLZ} t_{PHZ} t_{PZL} t_{PZH}	Output Enable and Disable to Q ACT574	5	3.7	13.2	3.6	14.5	ns
t_{PLZ} t_{PHZ} t_{PZL} t_{PZH}	Output Enable and Disable to $\overline{Q}$ ACT564	5	3.7	13.2	3.6	14.5	ns
C_{PD} (2)	Power Dissipation Capacitance	—		67 Typ.		67 Typ.	pF
V_{OHV}	Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	5	4 Typ. @25°C				V
V_{OLP}	Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	5	1 Typ. @ 25°C				V
C_I	Input Capacitance	—	—	10	—	10	pF
C_O	3-State Output Capacitance	—	—	15	—	15	pF

(1) 5 V: min. is @ 5.5 V
(2) C_{PD} is used to determine the dynamic power consumption, per flip flop.

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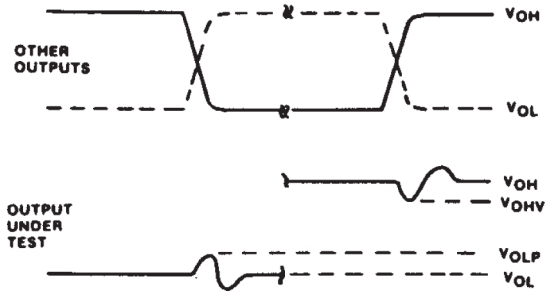
5 Parameter Measurement Information



A. V_{OHV} AND V_{OLP} are measured with respect to a ground REFERENCE NEAR THE OUTPUT UNDER TEST.
B. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS: PRR ≤ 1 MHz, t_r = 3 ns, t_f = 3 ns, SKEW 1 ns.
C. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED. IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1 *μF* CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.
D. 92CS-42406

Figure 5-1. Simultaneous Switching Transient Waveforms.

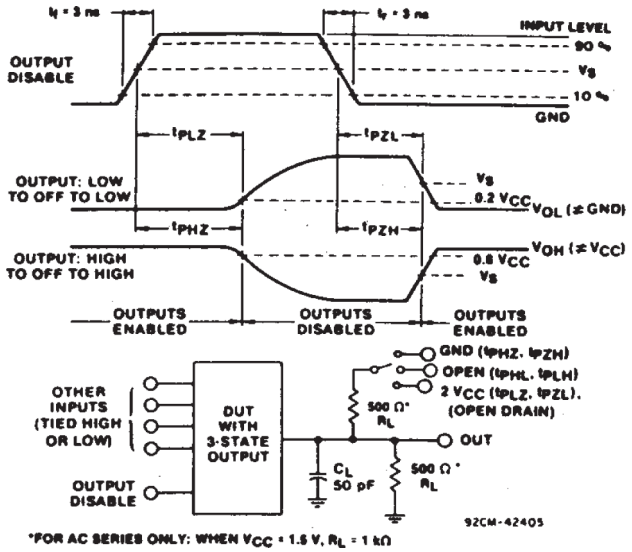


Figure 5-2. Three-state Propagation Delay Waveforms and Test Circuit.

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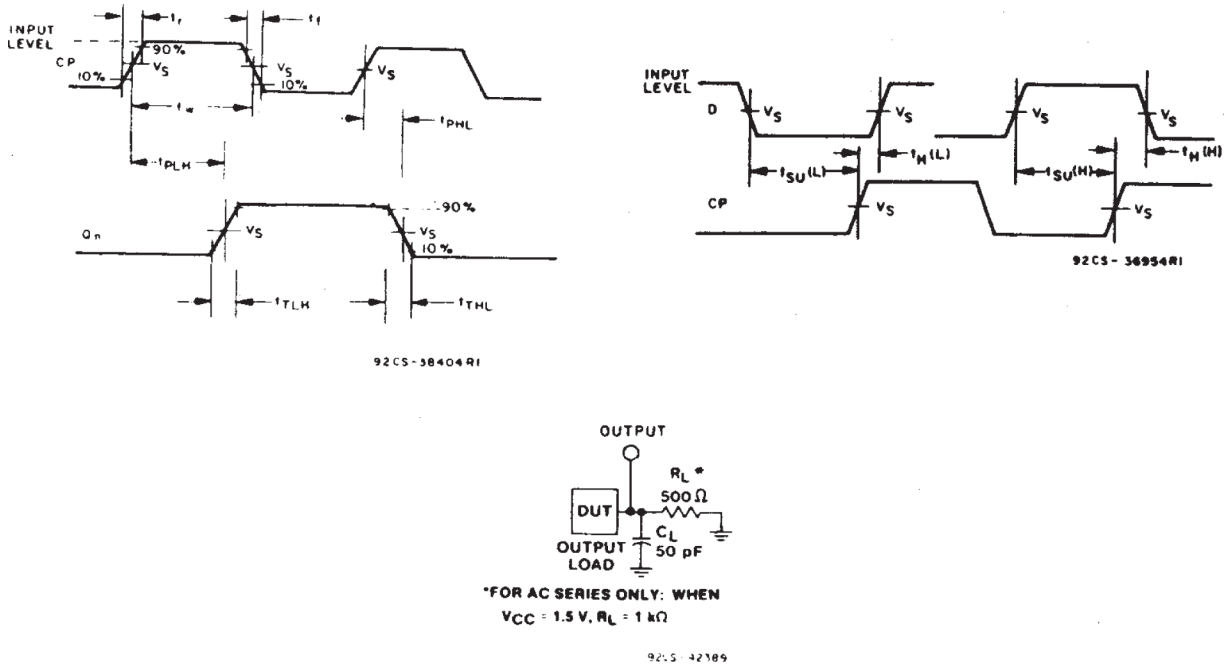

Figure 5-3. Propagation Delays Times and Test Circuit.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0 5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0 5 V_{CC}

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6 Detailed Description

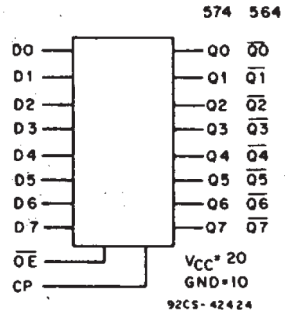
6.1 Overview

The CD54/74AC574 and the CD54/74ACT574 octal D-type, 3-state, positive-edge-triggered flip-flops use the RCA ADVANCED CMOS technology. The eight flip-flops enter data into their registers on the LOW-to-HIGH transition of the clock (CP). The Output Enable ($\overline{OE}$) controls the 3-state outputs and is independent of the register operation. When the Output Enable ($\overline{OE}$) is HIGH, the outputs are in the high-impedance state. The CD54/74AC/ACT574 share the same pin configurations, and the CD54/74AC/ACT574 has non-inverted outputs.

The CD74AC/ACT574 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC/ACT574, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

6.2 Functional Block Diagram



6.3 Device Functional Modes

Table 6-1. Truth Table

$\overline{\text{Output}}$ Enable	$\overline{\text{Latch}}$ Enable	Data	AC/ACT373 Output
L	H	H	H
L	H	L	L
L	L	l	L
L	L	h	H
H	X	X	Z

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in *Section 4.3*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends 0.1 µF and if there are multiple V_{CC} terminals, then TI recommends .01 µF or .022 µF for each power terminal. It is okay to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

7.2 Layout

7.2.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the I.O's so they also cannot float when disabled.

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8 Device and Documentation Support

8.1 Documentation Support (Analog)

8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
CD54AC574	Click here	Click here	Click here	Click here	Click here
CD74AC574	Click here	Click here	Click here	Click here	Click here
CD54ACT574	Click here	Click here	Click here	Click here	Click here
CD74ACT574	Click here	Click here	Click here	Click here	Click here

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 1998) to Revision A (May 2024)	Page
• Added *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Device Functional Modes, Application and Implementation* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Updated RθJA values: DW = 40 to 101.2, all values in °C/W	4

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10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD54AC574F3A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54AC574F3A
CD54AC574F3A.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54AC574F3A
CD54ACT574F3A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54ACT574F3A
CD54ACT574F3A.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54ACT574F3A
CD74AC574E	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74AC574E
CD74AC574E.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74AC574E
CD74AC574M	Obsolete	Production	SOIC (DW) | 20	-	-	Call TI	Call TI	-55 to 125	AC574M
CD74AC574M96	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC574M
CD74AC574M96.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC574M
CD74AC574M96G4	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC574M
CD74ACT574E	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74ACT574E
CD74ACT574E.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74ACT574E
CD74ACT574M	Obsolete	Production	SOIC (DW) | 20	-	-	Call TI	Call TI	-55 to 125	ACT574M
CD74ACT574M96	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT574M
CD74ACT574M96.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT574M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54AC574, CD54ACT574, CD74AC574, CD74ACT574 :

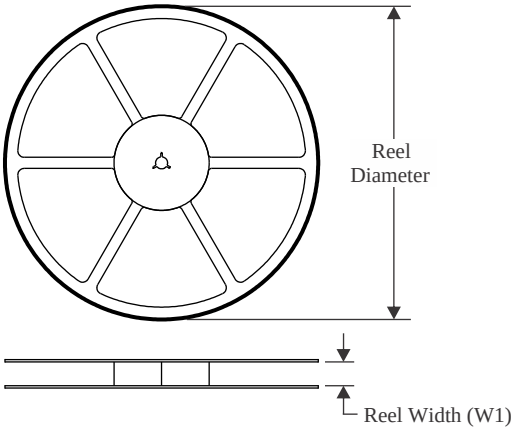
- Catalog : CD74AC574, CD74ACT574
- Military : CD54AC574, CD54ACT574

NOTE: Qualified Version Definitions:

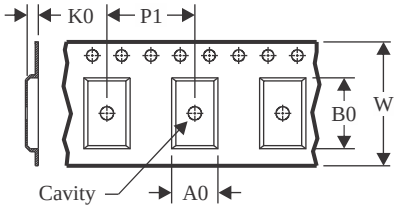
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

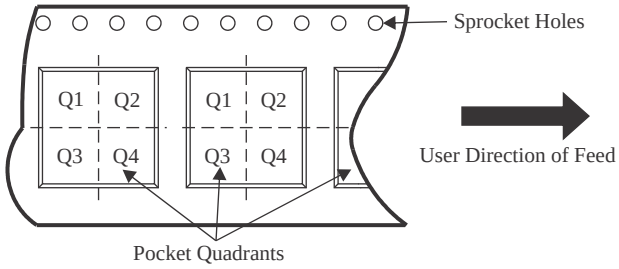


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

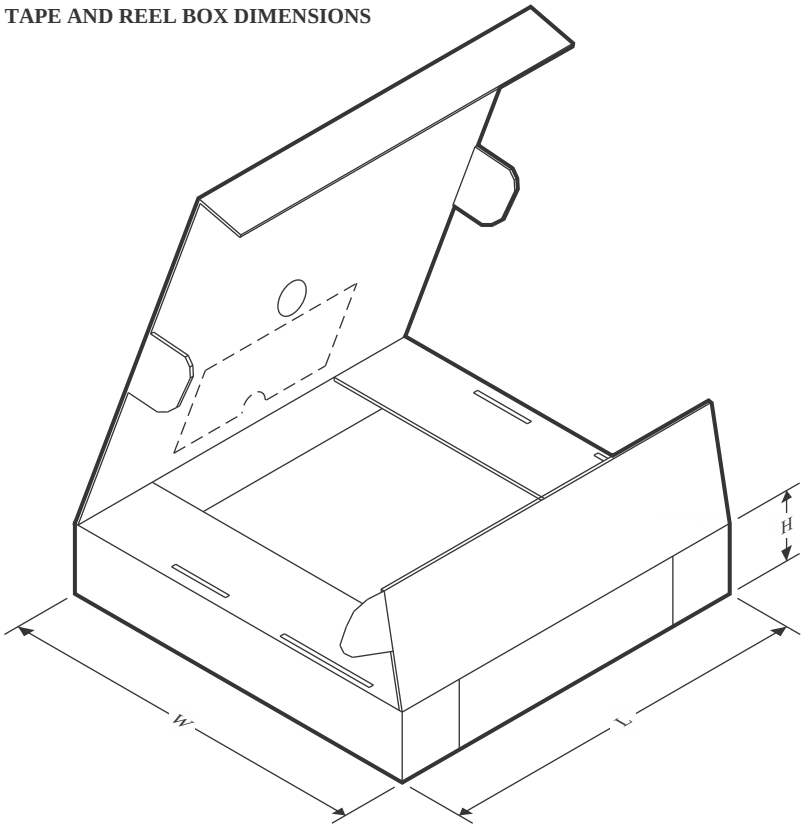
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC574M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74AC574M96	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
CD74ACT574M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

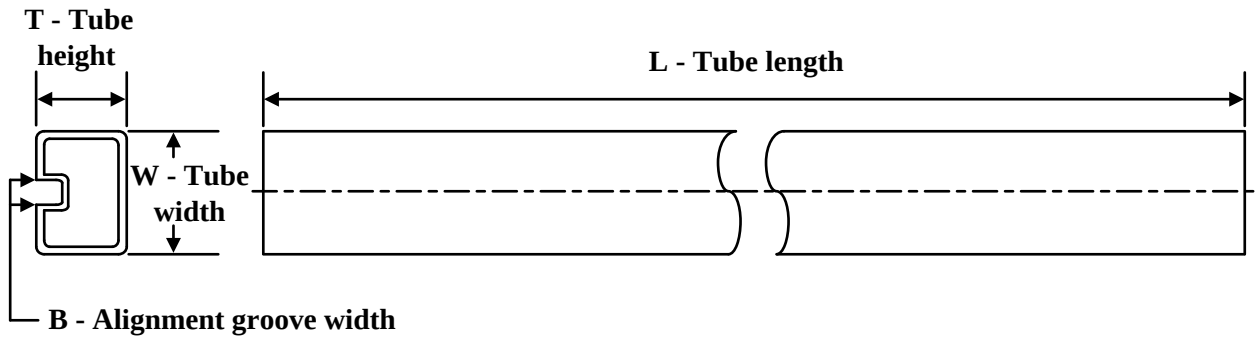
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC574M96	SOIC	DW	20	2000	356.0	356.0	45.0
CD74AC574M96	SOIC	DW	20	2000	356.0	356.0	45.0
CD74ACT574M96	SOIC	DW	20	2000	356.0	356.0	45.0

TUBE



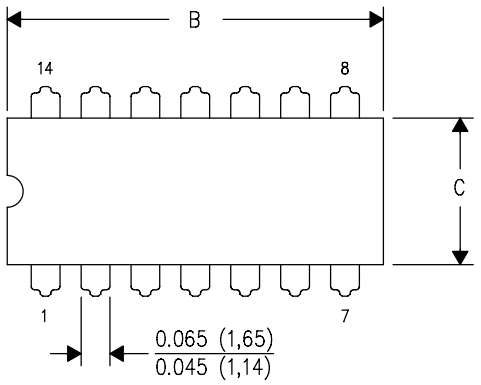
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74AC574E	N	PDIP	20	20	506	13.97	11230	4.32
CD74AC574E.A	N	PDIP	20	20	506	13.97	11230	4.32
CD74ACT574E	N	PDIP	20	20	506	13.97	11230	4.32
CD74ACT574E.A	N	PDIP	20	20	506	13.97	11230	4.32

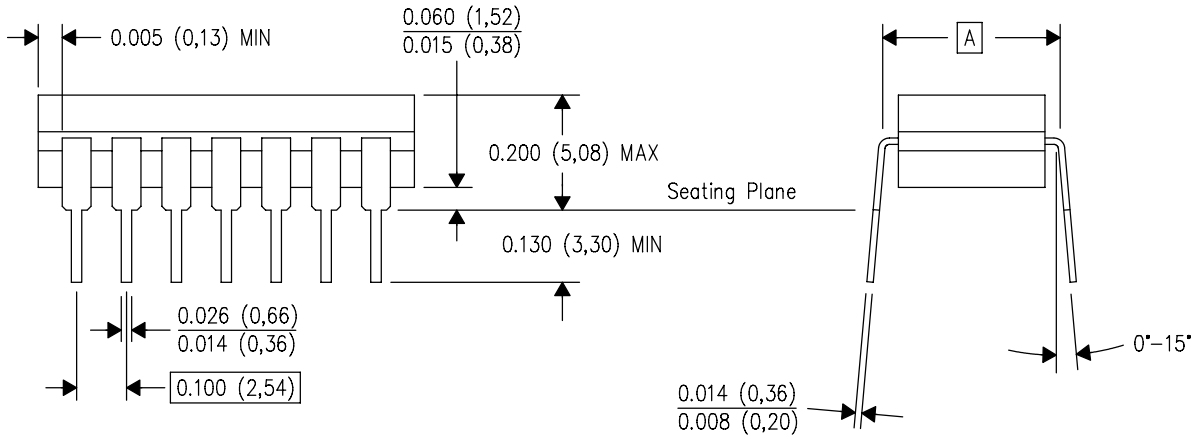
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



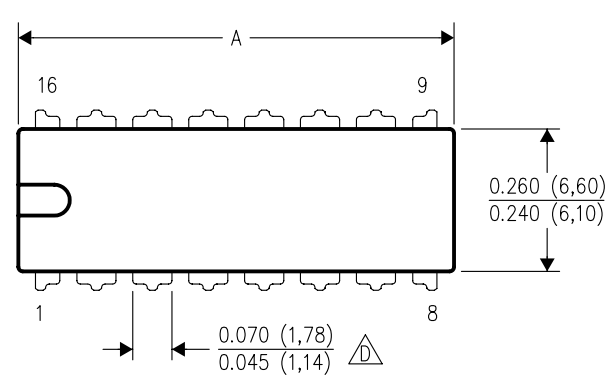
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

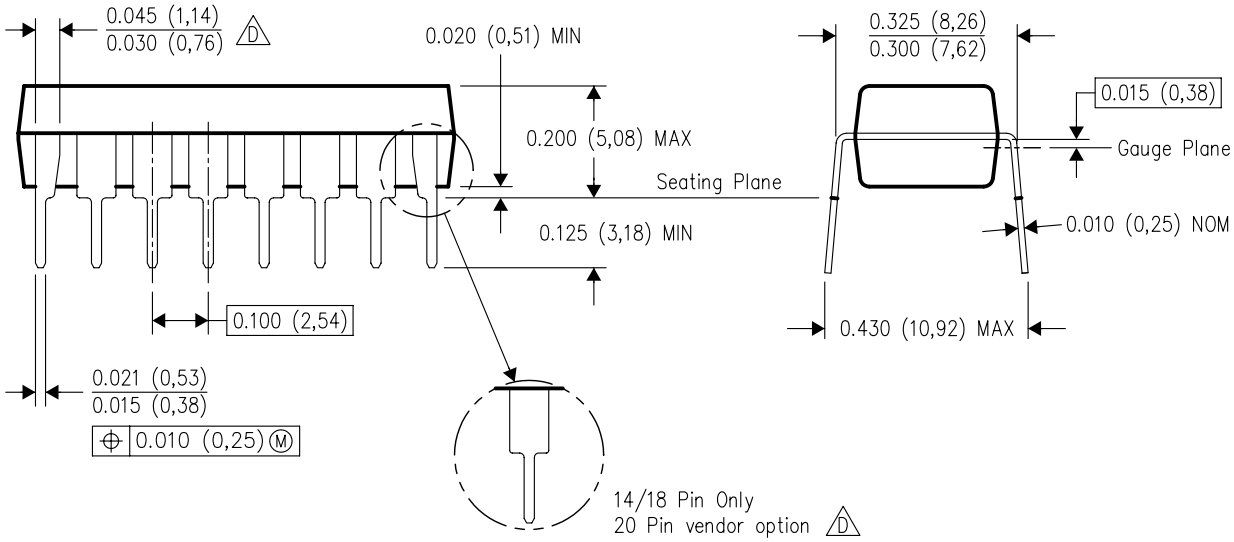
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

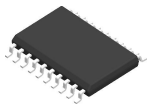


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

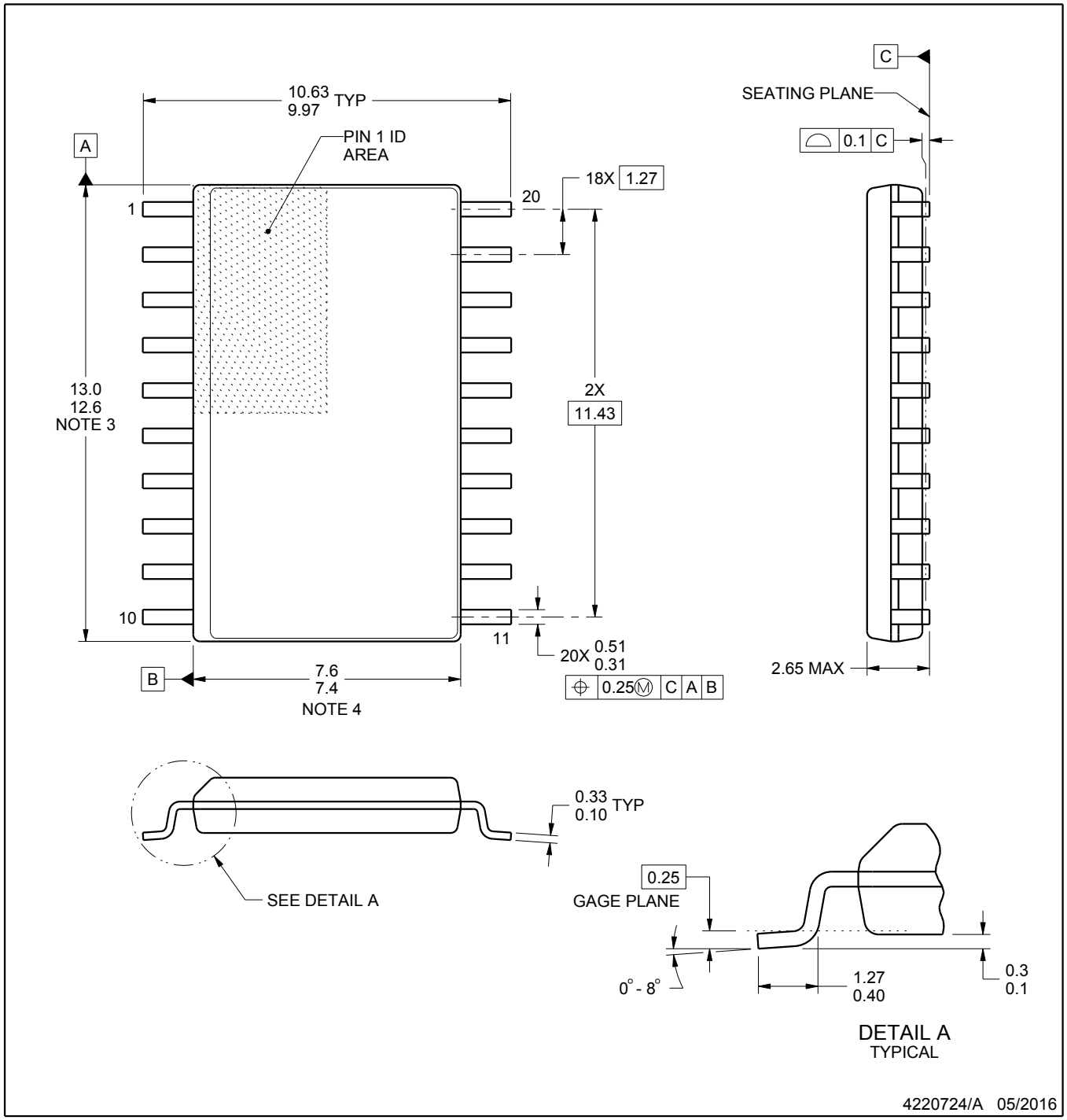


PACKAGE OUTLINE

DW0020A

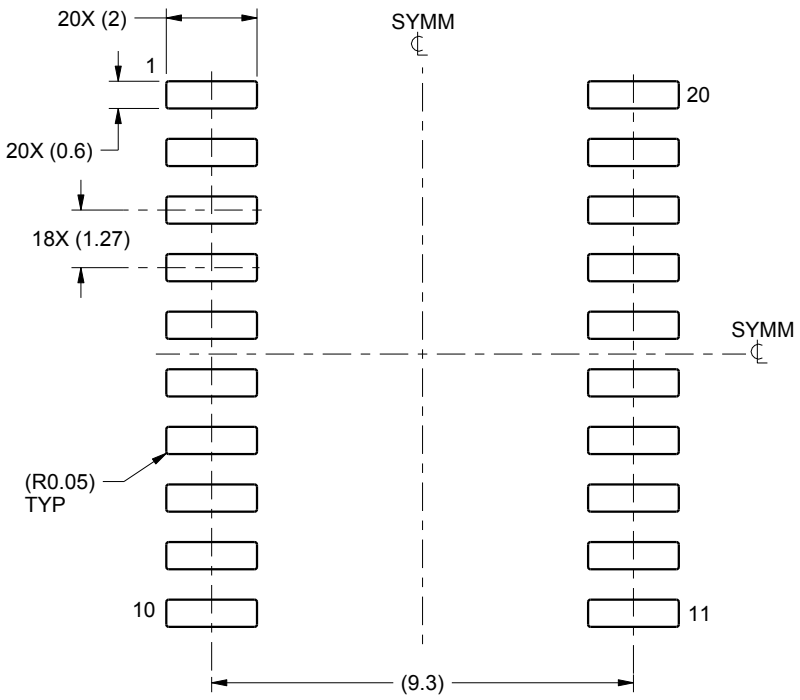
SOIC - 2.65 mm max height

SOIC

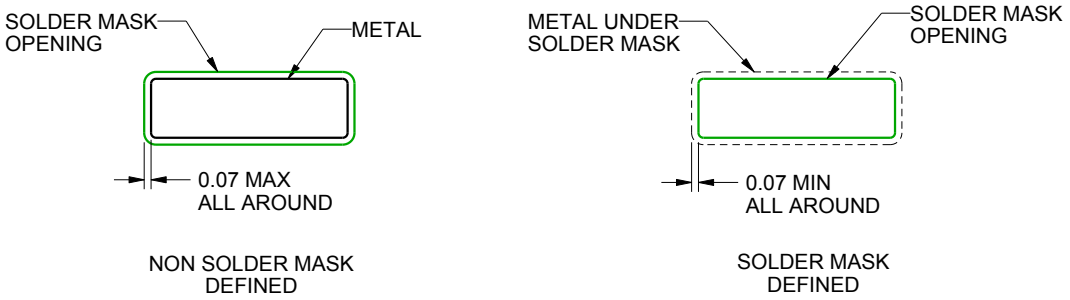


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

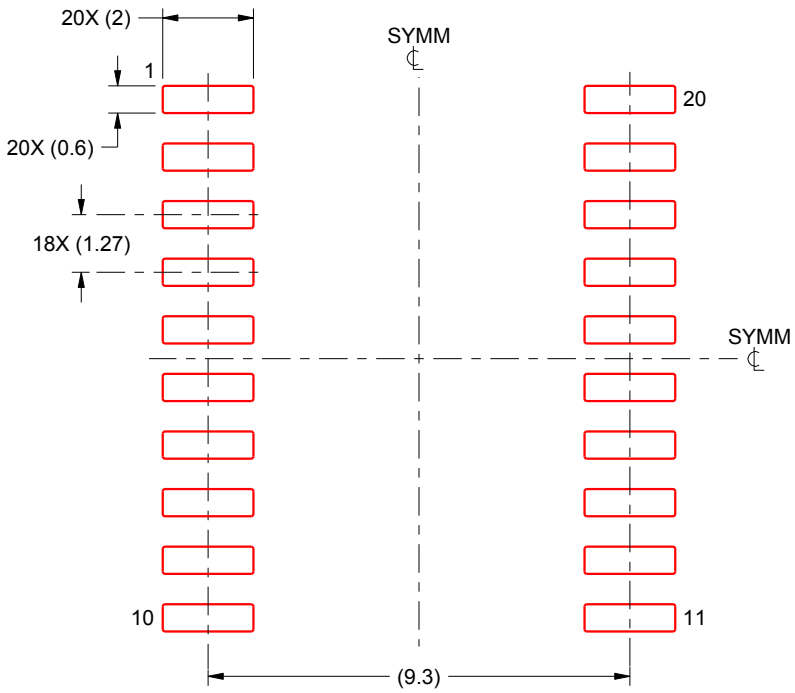


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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