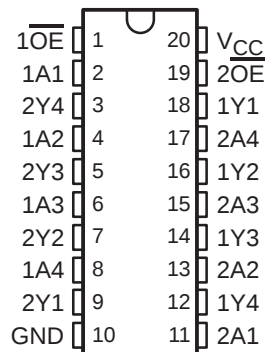


CD74FCT244, CD74FCT244AT BiCMOS OCTAL BUFFERS/LINE DRIVERS WITH 3-STATE OUTPUTS

SCBS722B – JULY 2000 – REVISED AUGUST 2003

- BiCMOS Technology With Low Quiescent Power
- Buffered Inputs
- Noninverted Outputs
- Input/Output Isolation From V_{CC}
- Controlled Output Edge Rates
- 64-mA Output Sink Current
- Output Voltage Swing Limited to 3.7 V
- SCR Latch-Up-Resistant BiCMOS Process and Circuit Design

CD74FCT244 . . . E, M, OR SM PACKAGE
CD74FCT244AT . . . E OR M PACKAGE
(TOP VIEW)



description/ordering information

The CD74FCT244 and CD74FCT244AT are octal buffer/line drivers with 3-state outputs using a small-geometry BiCMOS technology. The output stages are a combination of bipolar and CMOS transistors that limit the output high level to two diode drops below V_{CC} . This resultant lowering of output swing (0 V to 3.7 V) reduces the power-bus ringing [a source of electromagnetic interference (EMI)] and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 64 mA.

These devices are organized as two 4-bit buffers/line drivers with separate active-low output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – E	Tube	CD74FCT244E	CD74FCT244E
	SOIC – M	Tube	CD74FCT244M	74FCT244M
		Tape and reel	CD74FCT244M96	
	SSOP – SM	Tape and reel	CD74FCT244SM96	FCT244SM
	PDIP – E	Tube	CD74FCT244ATE	CD74FCT244ATE
	SOIC – M	Tube	CD74FCT244ATM	74FCT244ATM
		Tape and reel	CD74FCT244ATM96	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each buffer/driver)

INPUTS		OUTPUT Y
$\overline{OE}$	A	
L	H	H
L	L	L
H	X	Z



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

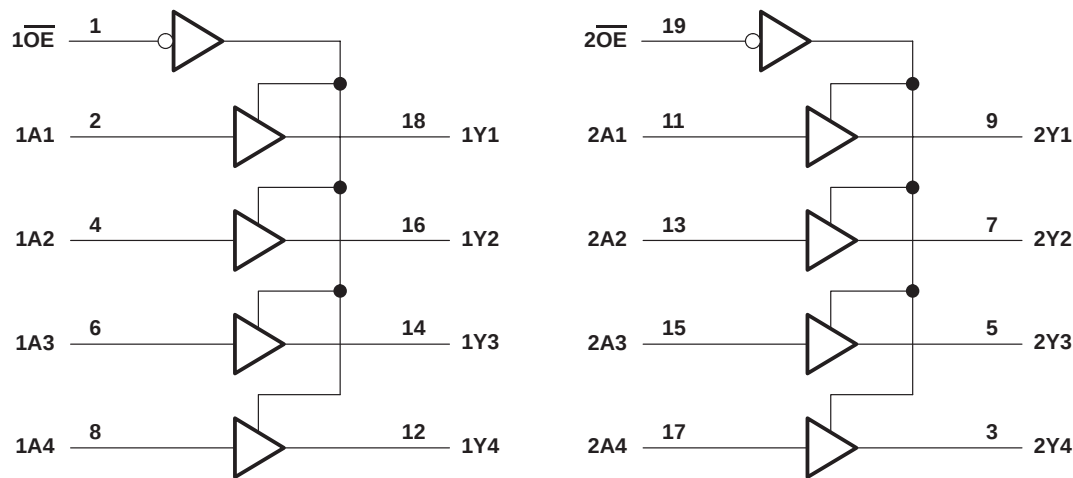
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CD74FCT244, CD74FCT244AT
BiCMOS OCTAL BUFFERS/LINE DRIVERS
WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

DC supply voltage range, V_{CC}	–0.5 V to 6 V
DC input clamp current, I_{IK} ($V_I < -0.5$ V)	–20 mA
DC output clamp current, I_{OK} ($V_O < -0.5$ V)	–50 mA
DC output sink current per output pin, I_{OL}	70 mA
DC output source current per output pin, I_{OH}	–30 mA
Continuous current through V_{CC} , I_{CC}	140 mA
Continuous current through GND	528 mA
Package thermal impedance, θ_{JA} (see Note 1): E package	69°C/W
M package	58°C/W
SM package	70°C/W

Storage temperature range, T_{stg}	–65°C to 150°C
--------------------------------------	----------------

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

	MIN	MAX	UNIT
V_{CC} Supply voltage	4.75	5.25	V
V_{IH} High-level input voltage	2		V
V_{IL} Low-level input voltage		0.8	V
V_I Input voltage	0	V_{CC}	V
V_O Output voltage	0	V_{CC}	V
I_{OH} High-level output current		–15	mA
I_{OL} Low-level output current		64	mA
$\Delta t/\Delta v$ Input transition rise or fall rate (slew rate)		10	ns/V
T_A Operating free-air temperature	0	70	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



CD74FCT244, CD74FCT244AT
BiCMOS OCTAL BUFFERS/LINE DRIVERS
WITH 3-STATE OUTPUTS

SCBS722B – JULY 2000 – REVISED AUGUST 2003

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
V _{IK}	I _I = –18 mA	4.75 V	–1.2		–1.2		V
V _{OH}	I _{OH} = –15 mA	4.75 V	2.4		2.4		V
V _{OL}	I _{OL} = 64 mA	4.75 V	0.55		0.55		V
I _I	V _I = V _{CC} or GND	5.25 V	±0.1		±1		μA
I _{OZ}	V _O = V _{CC} or GND	5.25 V	±0.5		±10		μA
I _{OS} [†]	V _I = V _{CC} or GND, V _O = 0	5.25 V	–60		–60		mA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.25 V	8		80		μA
ΔI _{CC} [‡]	One input at 3.4 V, Other inputs at V _{CC} or GND	5.25 V	1.6		1.6		mA
C _i	V _I = V _{CC} or GND		10		10		pF
C _o	V _O = V _{CC} or GND		15		15		pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 100 ms.

[‡] This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.25 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CD74FCT244			CD74FCT244AT			UNIT
			T _A = 25°C	MIN	MAX	T _A = 25°C	MIN	MAX	
			TYP			TYP			
t _{pd}	A	Y	4.5	1.5	6.5	3.8	1.5	5.3	ns
t _{en}	$\overline{\text{OE}}$	Y	6	1.5	8	4.8	1.5	6.5	ns
t _{dis}	$\overline{\text{OE}}$	Y	5	1.5	7	4.5	1.5	5.8	ns

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C

PARAMETER	MIN	TYP	MAX	UNIT
V _{OL(P)} Quiet output, maximum dynamic V _{OL}		1		V
V _{OH(V)} Quiet output, minimum dynamic V _{OH}		0.5		V
V _{IH(D)} High-level dynamic input voltage	2			V
V _{IL(D)} Low-level dynamic input voltage			0.8	V

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance	No load, f = 1 MHz	35	pF

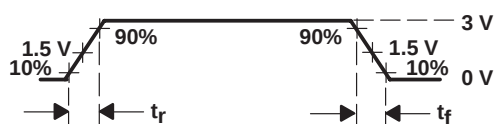
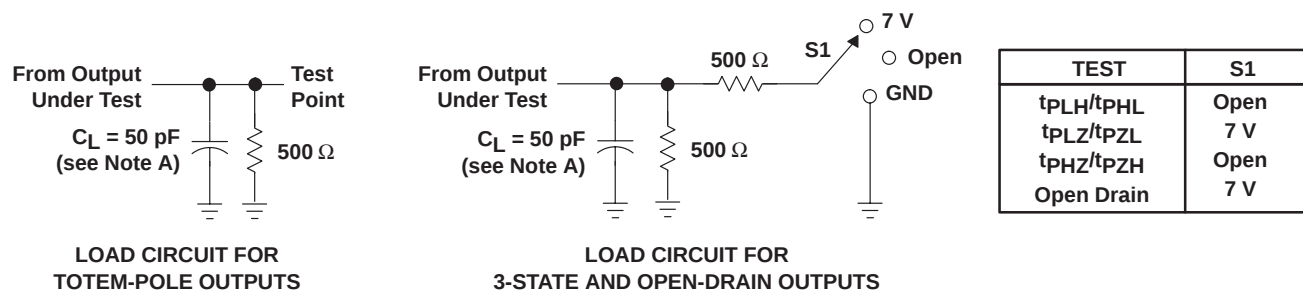
CD74FCT244, CD74FCT244AT

BiCMOS OCTAL BUFFERS/LINE DRIVERS

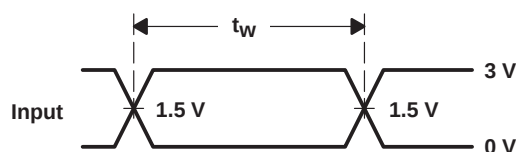
WITH 3-STATE OUTPUTS

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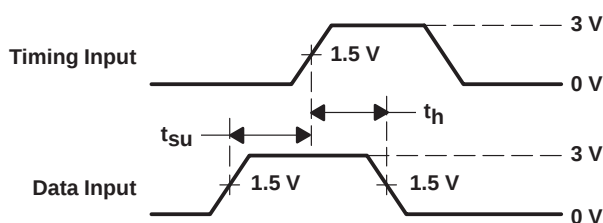
PARAMETER MEASUREMENT INFORMATION



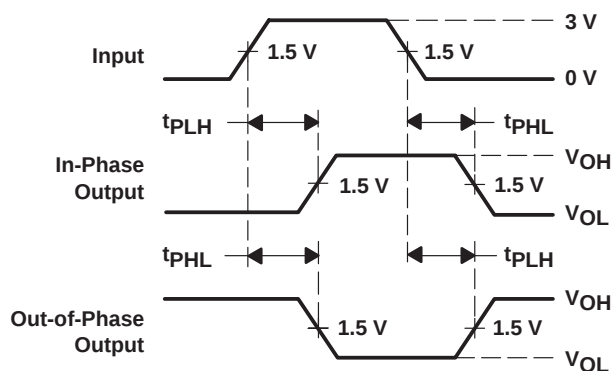
**VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES**



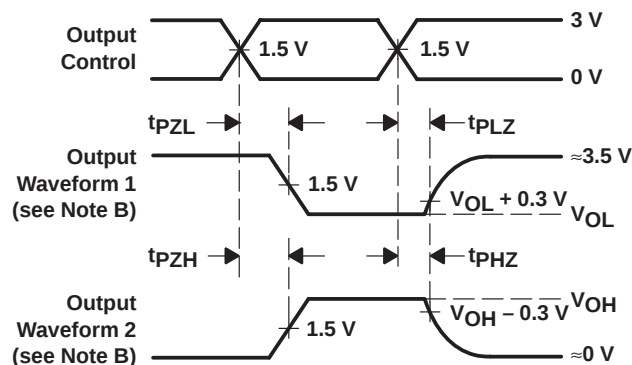
**VOLTAGE WAVEFORMS
PULSE DURATION**



**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, t_r and $t_f = 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{pZL} and t_{pZH} are the same as t_{en} .
- G. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD74FCT244ATE	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	CD74FCT244ATE
CD74FCT244ATE.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	CD74FCT244ATE
CD74FCT244ATM	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	0 to 70	74FCT244ATM
CD74FCT244ATM96	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74FCT244ATM
CD74FCT244ATM96.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74FCT244ATM
CD74FCT244E	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	CD74FCT244E
CD74FCT244E.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	CD74FCT244E
CD74FCT244M	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	0 to 70	74FCT244M
CD74FCT244M96	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74FCT244M
CD74FCT244M96.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74FCT244M

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

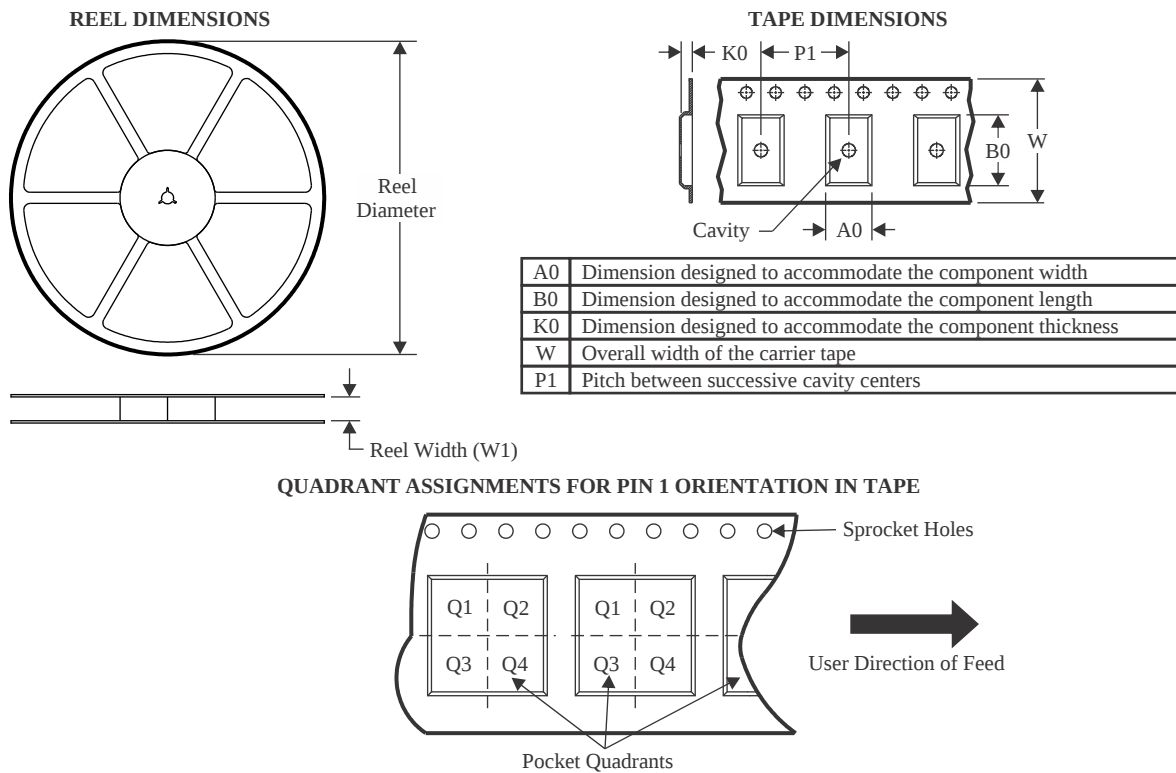
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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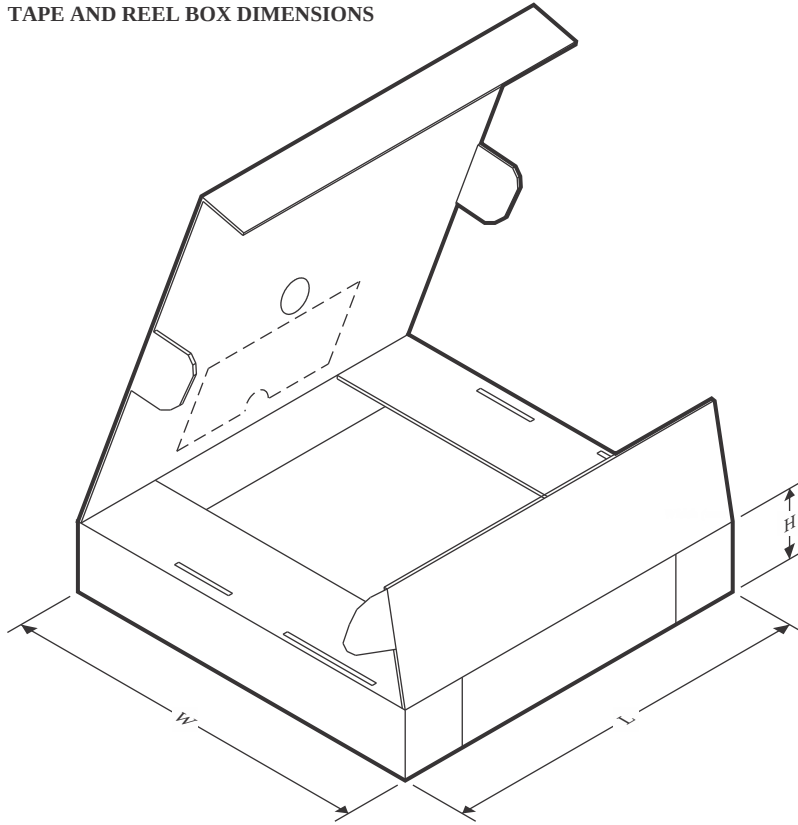
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74FCT244ATM96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74FCT244M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74FCT244ATM96	SOIC	DW	20	2000	356.0	356.0	45.0
CD74FCT244M96	SOIC	DW	20	2000	356.0	356.0	45.0

TUBE

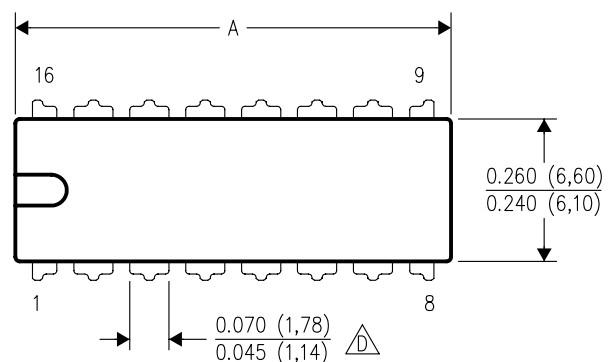

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74FCT244ATE	N	PDIP	20	20	506	13.97	11230	4.32
CD74FCT244ATE.A	N	PDIP	20	20	506	13.97	11230	4.32
CD74FCT244E	N	PDIP	20	20	506	13.97	11230	4.32
CD74FCT244E.A	N	PDIP	20	20	506	13.97	11230	4.32

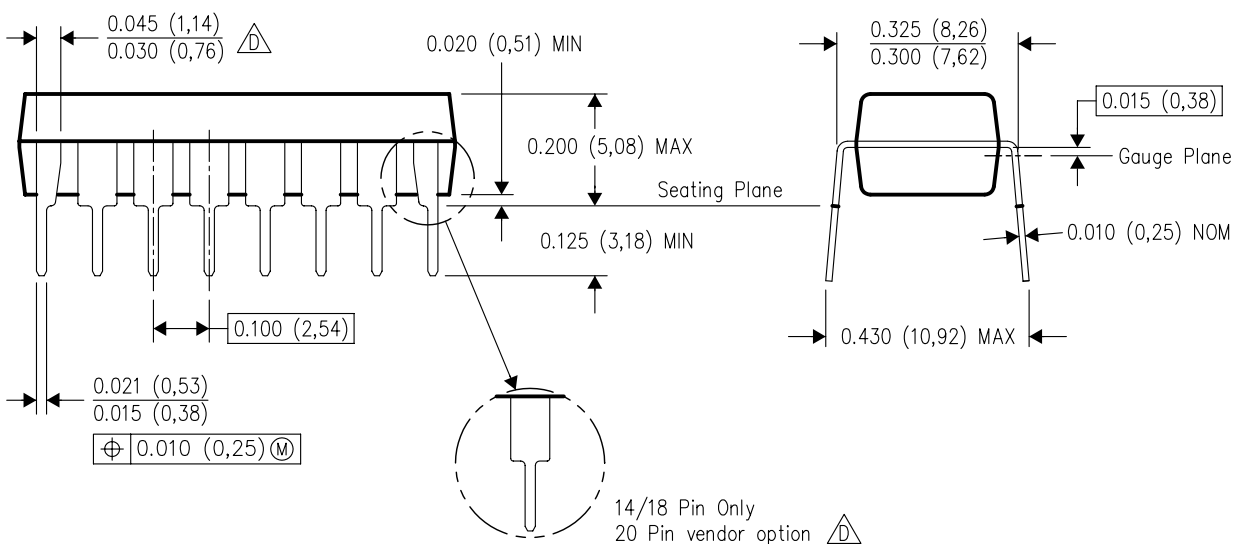
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



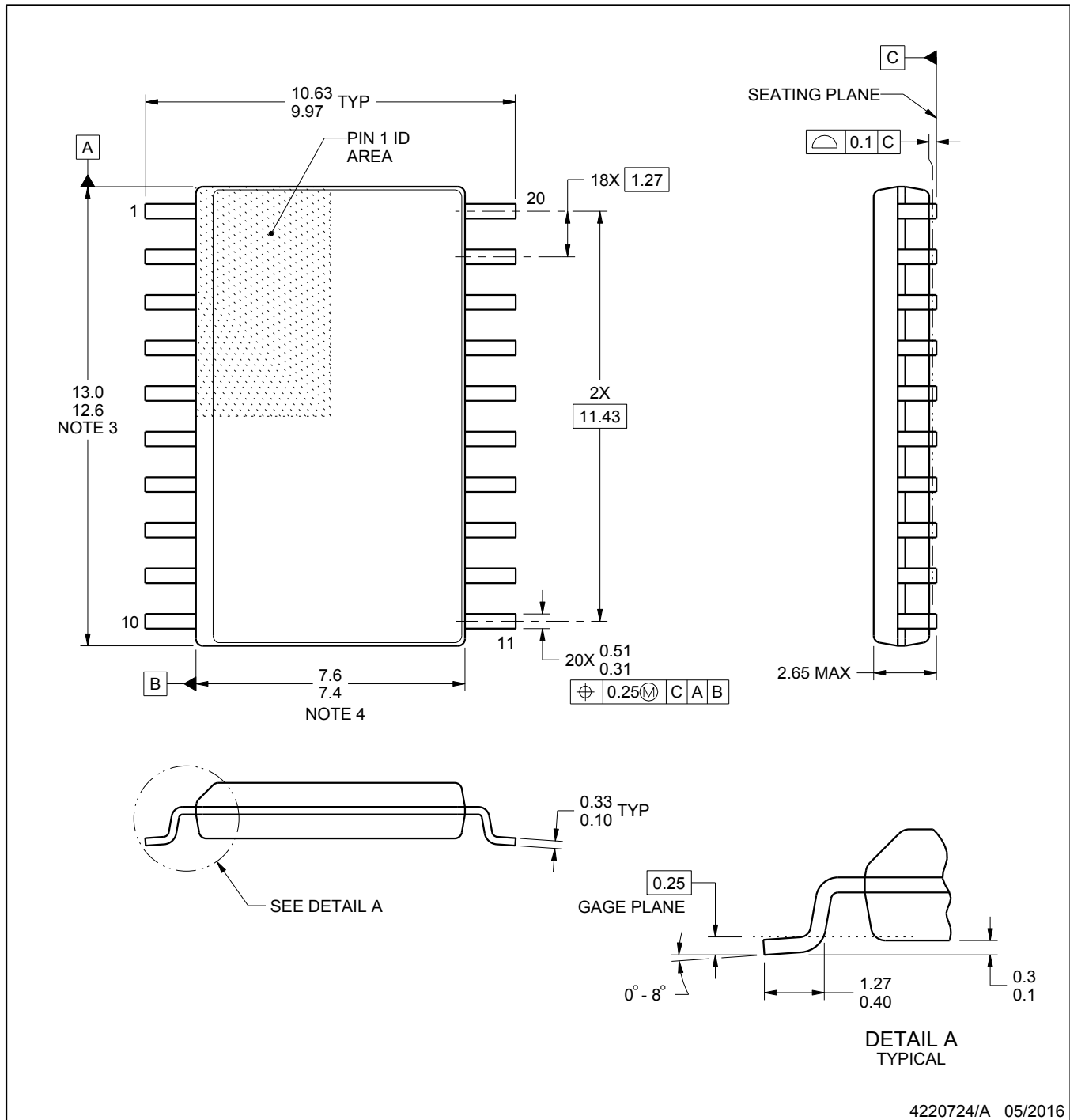
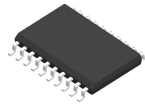
PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.



4220724/A 05/2016

NOTES:

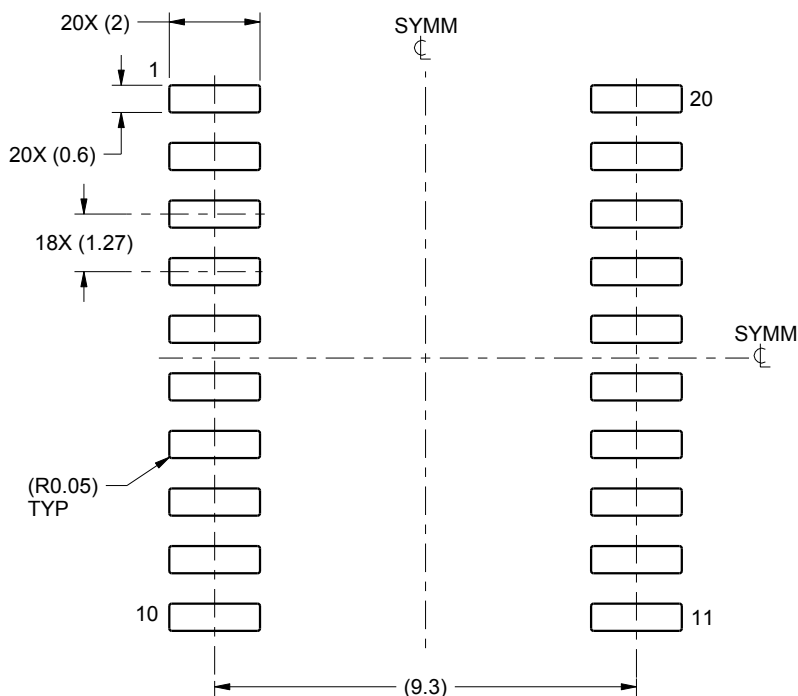
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

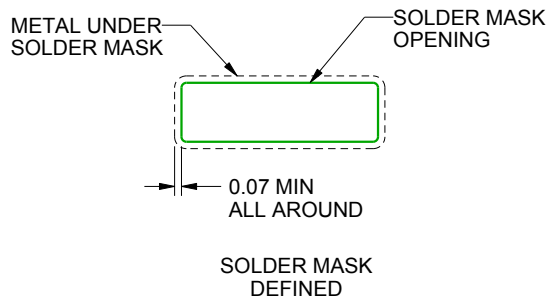
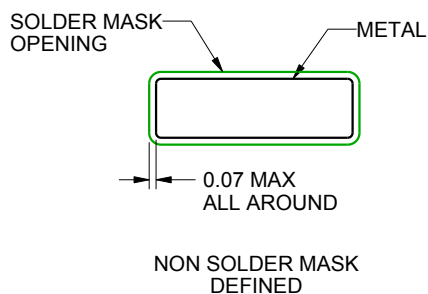
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

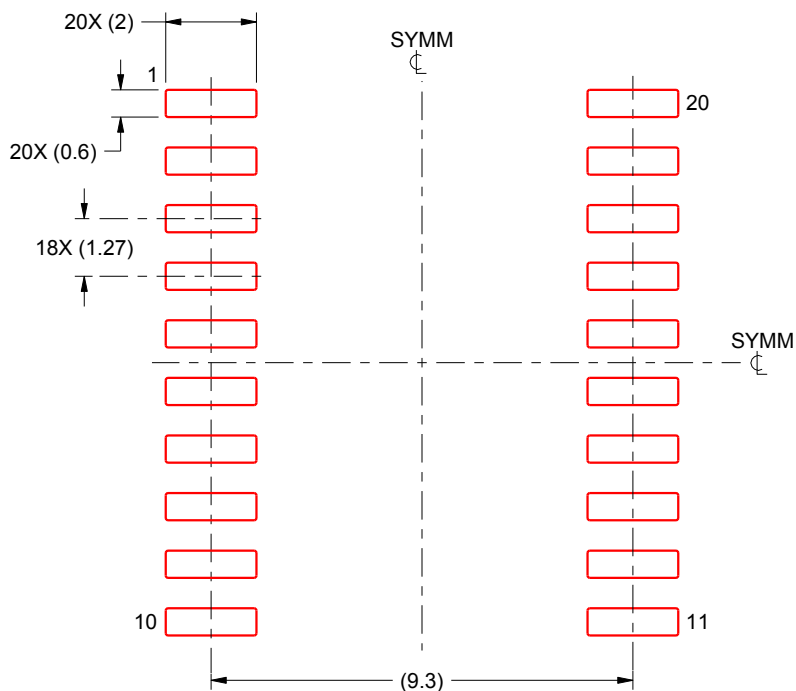
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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