

September 1997 - Revised October 2003

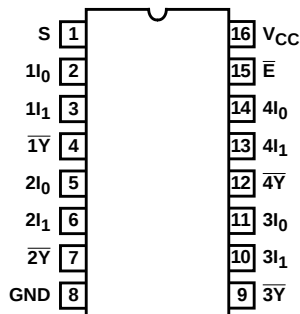
High-Speed CMOS Logic Quad 2-Input Multiplexers

Features

- Common Select Inputs
- Separate Enable Inputs
- Buffered inputs and Outputs
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)
 - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL} , V_{OH}

Pinout

CD54HC157, CD54HCT157, CD54HC158, CD54HCT158
(CERDIP)
CD74HC157, CD74HCT157, CD74HC158
(PDIP, SOIC)
CD74HCT158
(PDIP)
TOP VIEW



Description

The 'HC157, 'HCT157, 'HC158, and 'HCT158 are quad 2-input multiplexers which select four bits of data from two sources under the control of a common Select input (S). The Enable input ($\bar{E}$) is active Low. When ($\bar{E}$) is High, all of the outputs in the 158, the inverting type, ($1\bar{Y}$ - $4\bar{Y}$) are forced High and in the 157, the non-inverting type, all of the outputs ($1Y$ - $4Y$) are forced Low, regardless of all other input conditions.

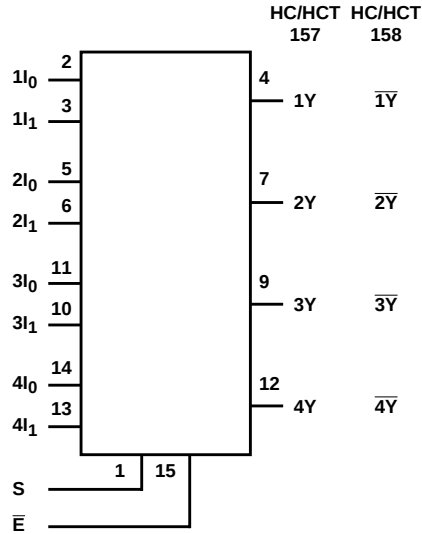
Moving data from two groups of registers to four common output buses is a common use of these devices. The state of the Select input determines the particular register from which the data comes. They can also be used as function generators.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC157F3A	-55 to 125	16 Ld CERDIP
CD54HCT157F3A	-55 to 125	16 Ld CERDIP
CD54HCT158F3A	-55 to 125	16 Ld CERDIP
CD74HC157E	-55 to 125	16 Ld PDIP
CD74HC157M	-55 to 125	16 Ld SOIC
CD74HC157MT	-55 to 125	16 Ld SOIC
CD74HC157M96	-55 to 125	16 Ld SOIC
CD74HCT157E	-55 to 125	16 Ld PDIP
CD74HCT157M	-55 to 125	16 Ld SOIC
CD74HCT157MT	-55 to 125	16 Ld SOIC
CD74HCT157M96	-55 to 125	16 Ld SOIC
CD74HCT158E	-55 to 125	16 Ld PDIP

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

Functional Diagram



TRUTH TABLE

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUT	
				157	158
$\overline{E}$	S	I0	I1	Y	$\overline{Y}$
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Voltage Level, L = Low Voltage Level, X = Don't Care

CD54/74HC157, CD54/74HCT157, CD54/74HC158, CD54/74HCT158

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} -0.5V to 7V
 DC Input Diode Current, I_{IK}
 For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ $\pm 20mA$
 DC Output Diode Current, I_{OK}
 For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ $\pm 20mA$
 DC Output Source or Sink Current per Output Pin, I_O
 For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ $\pm 25mA$
 DC V_{CC} or Ground Current, I_{CC} or I_{GND} $\pm 50mA$

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^{\circ}C/W$)
 E (PDIP) Package 67
 M (SOIC) Package 73
 Maximum Junction Temperature $150^{\circ}C$
 Maximum Storage Temperature Range $-65^{\circ}C$ to $150^{\circ}C$
 Maximum Lead Temperature (Soldering 10s) $300^{\circ}C$
 (SOIC - Lead Tips Only)

Operating Conditions

Temperature Range (T_A) $-55^{\circ}C$ to $125^{\circ}C$
 Supply Voltage Range, V_{CC}
 HC Types 2V to 6V
 HCT Types 4.5V to 5.5V
 DC Input or Output Voltage, V_I , V_O 0V to V_{CC}
 Input Rise and Fall Time
 2V 1000ns (Max)
 4.5V 500ns (Max)
 6V 400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V _{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V _{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I _I	V _{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I _{CC}	V _{CC} or GND	0	6	-	-	8	-	80	-	160	μA

CD54/74HC157, CD54/74HCT157, CD54/74HC158, CD54/74HCT158

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HCT TYPES												
High Level Input Voltage	V _{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I _I	V _{CC} and GND	0	5.5	-		±0.1	-	±1	-	±1	μA
Quiescent Device Current	I _{CC}	V _{CC} or GND	0	5.5	-	-	8	-	80	-	160	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI _{CC} (Note 2)	V _{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE:

2. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS	
	HCT157	HCT158
I (All)	0.95	0.4
$\bar{E}$	0.6	0.6
S	3	2.8

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g., 360μA max at 25°C.

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC/HCT157 TYPES											
Propagation Delay (Figure 1)	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	125	-	155	-	190	ns
Data to Output			4.5	-	-	25	-	31	-	38	ns
HC157		C _L =15pF	5	-	10	-	-	-	-	-	ns
HCT157				-	12	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	21	-	26	-	32	ns

CD54/74HC157, CD54/74HCT157, CD54/74HC158, CD54/74HCT158

Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Enable to Output	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	135	-	170	-	205	ns
			4.5	-	-	27	-	34	-	41	ns
C _L =15pF		5	-	11	-	-	-	-	-	ns	
			-	12	-	-	-	-	-	ns	
HC157		C _L = 50pF	6	-	-	23	-	29	-	35	ns
HCT157				-	-	23	-	29	-	35	ns
Select to Output	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	145	-	180	-	220	ns
4.5			-	-	29	-	36	-	44	ns	
HC157		C _L =15pF	5	-	12	-	-	-	-	-	ns
HCT157				-	15	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	25	-	31	-	38	ns
				-	-	25	-	31	-	38	ns
Power Dissipation Capacitance (Notes 3, 4)	C _{PD}	-	5								
HC157				-	62	-	-	-	-	-	pF
HCT157				-	70	-	-	-	-	-	pF
HC/HCT158 TYPES											
Data to Output	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	140	-	175	-	210	ns
			4.5	-	-	28	-	35	-	42	
HC158		C _L =15pF	5	-	11	-	-	-	-	-	ns
HCT 158				-	13	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	24	-	30	-	36	ns
Enable to Output	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	160	-	200	-	240	ns
			4.5	-	-	32	-	40	-	48	ns
HC158		C _L =15pF	5	-	13	-	-	-	-	-	ns
HCT 158				-	15	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	27	-	34	-	41	ns
Select to Output	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	150	-	190	-	225	ns
			4.5	-	-	30	-	38	-	45	ns
HC158		C _L =15pF	5	-	12	-	-	-	-	-	ns
HCT 158				-	14	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	26	-	33	-	38	ns
Output Transition Time	t _{TLH} , t _{THL}	C _L = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Power Dissipation Capacitance (Notes 3, 4)	C _{PD}	-	5								
HC158				-	35	-	-	-	-	-	pF
HCT 158				-	35	-	-	-	-	-	pF
Input Capacitance	C _{IN}	C _L = 50pF	-	-	-	10	-	10	-	10	pF

NOTES:

3. C_{PD} is used to determine the dynamic power consumption, per multiplexer.
4. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.

Test Circuits and Waveforms

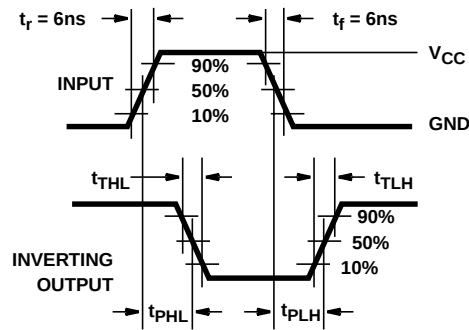


FIGURE 1. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

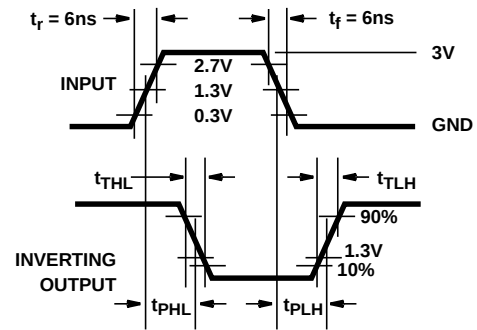


FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9070201MEA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9070201ME A CD54HCT157F3A
5962-9070301MEA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9070301ME A CD54HCT158F3A
CD54HC157F	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC157F
CD54HC157F.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC157F
CD54HC157F3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8606101EA CD54HC157F3A
CD54HC157F3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8606101EA CD54HC157F3A
CD54HCT157F3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9070201ME A CD54HCT157F3A
CD54HCT157F3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9070201ME A CD54HCT157F3A
CD54HCT158F3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9070301ME A CD54HCT158F3A
CD54HCT158F3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9070301ME A CD54HCT158F3A
CD74HC157E	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC157E
CD74HC157E.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC157E
CD74HC157M	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HC157M
CD74HC157M96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC157M
CD74HC157M96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC157M
CD74HC157MT	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HC157M
CD74HCT157E	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT157E
CD74HCT157E.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT157E
CD74HCT157M	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HCT157M

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD74HCT157M96	NRND	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT157M
CD74HCT157M96.A	NRND	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT157M
CD74HCT157MT	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HCT157M
CD74HCT158E	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT158E
CD74HCT158E.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT158E

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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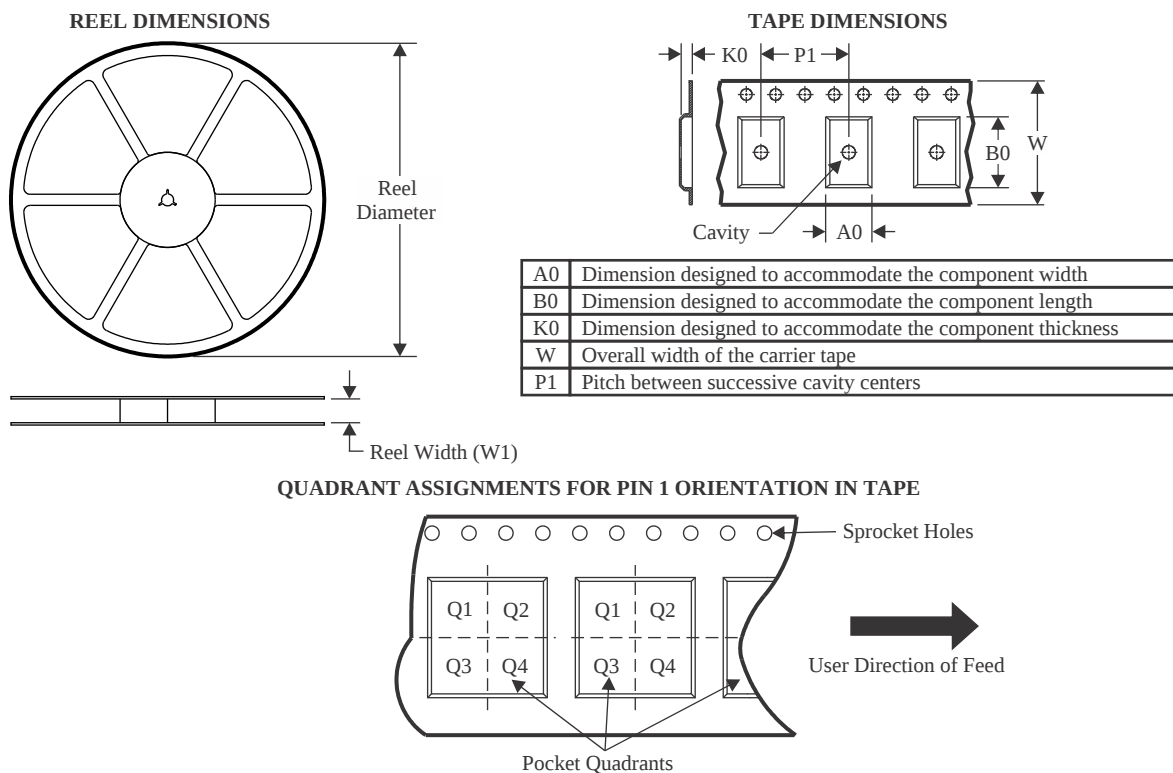
OTHER QUALIFIED VERSIONS OF CD54HC157, CD54HCT157, CD54HCT158, CD74HC157, CD74HCT157, CD74HCT158 :

- Catalog : [CD74HC157](#), [CD74HCT157](#), [CD74HCT158](#)
- Military : [CD54HC157](#), [CD54HCT157](#), [CD54HCT158](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

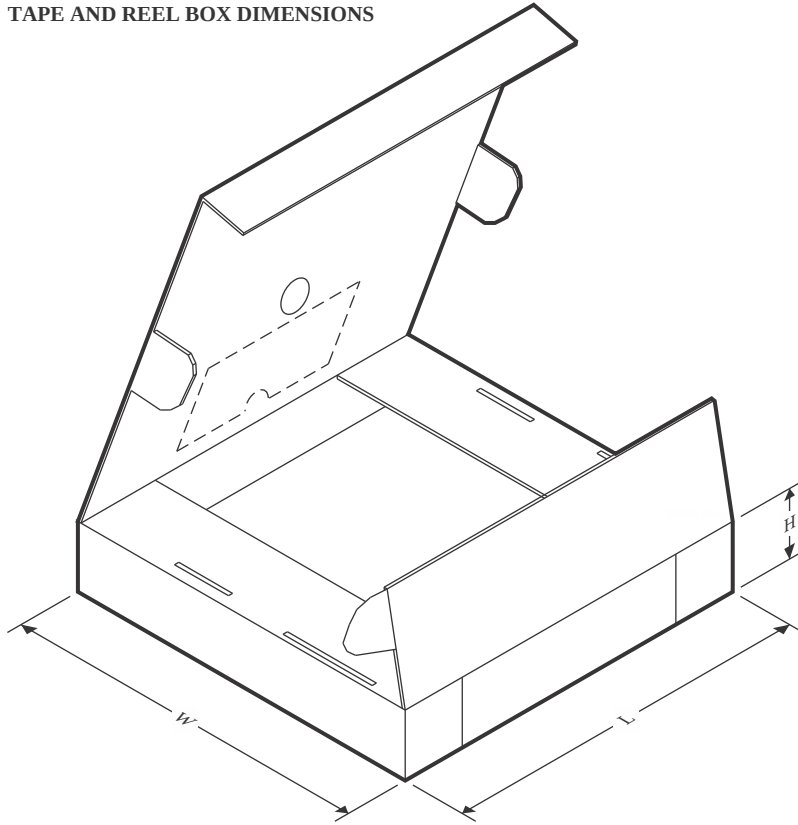
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC157M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT157M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC157M96	SOIC	D	16	2500	340.5	336.1	32.0
CD74HCT157M96	SOIC	D	16	2500	340.5	336.1	32.0

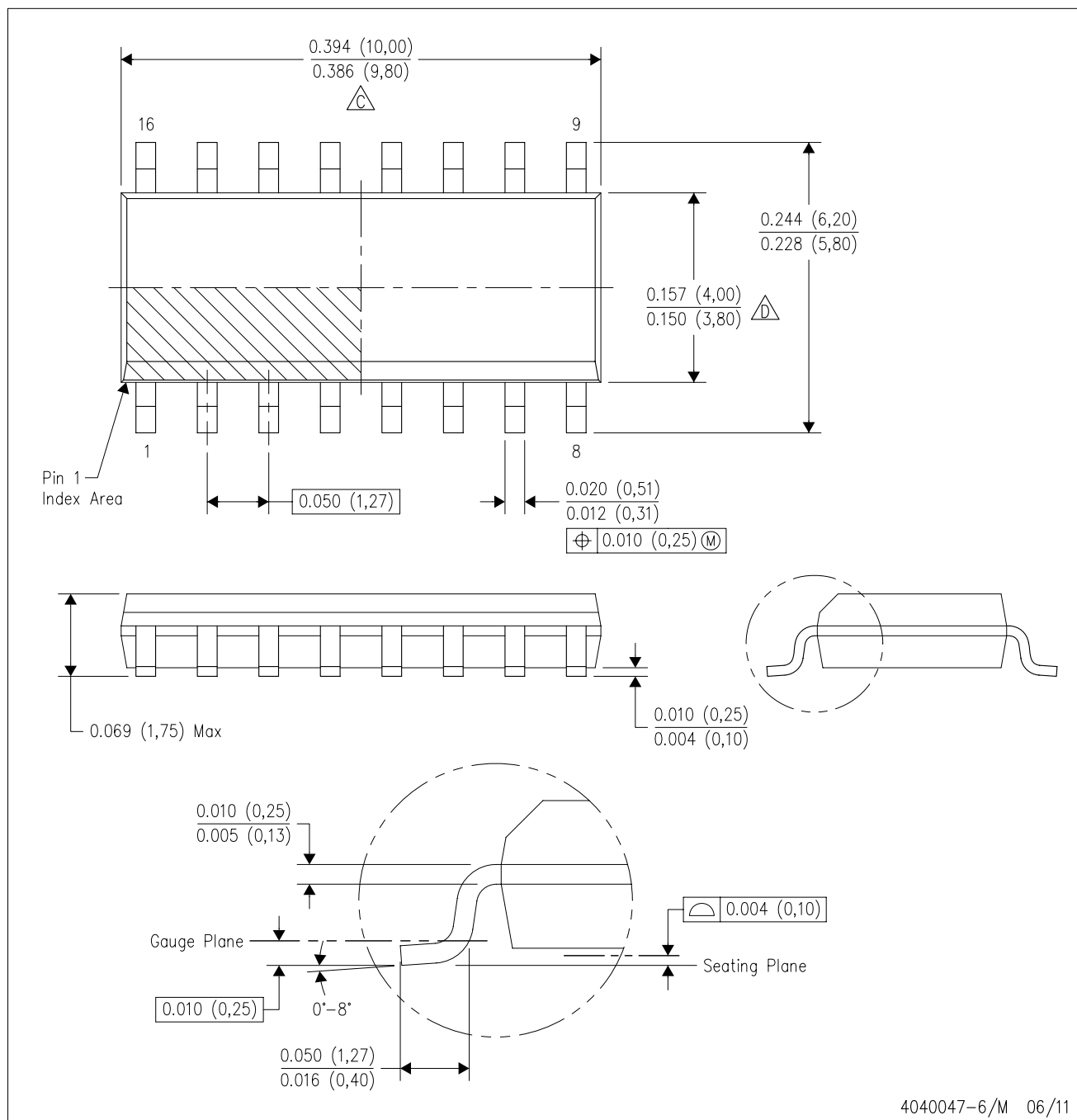
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HC157E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC157E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC157E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC157E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT157E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT157E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT157E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT157E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT158E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT158E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT158E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT158E.A	N	PDIP	16	25	506	13.97	11230	4.32

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



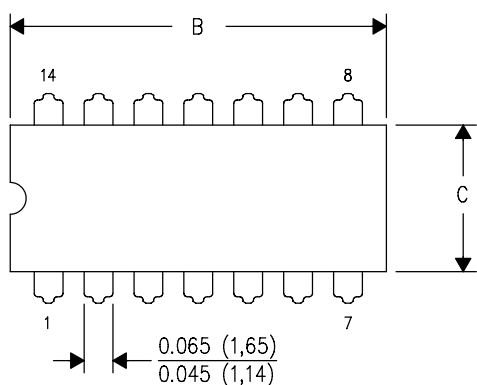
NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- Reference JEDEC MS-012 variation AC.

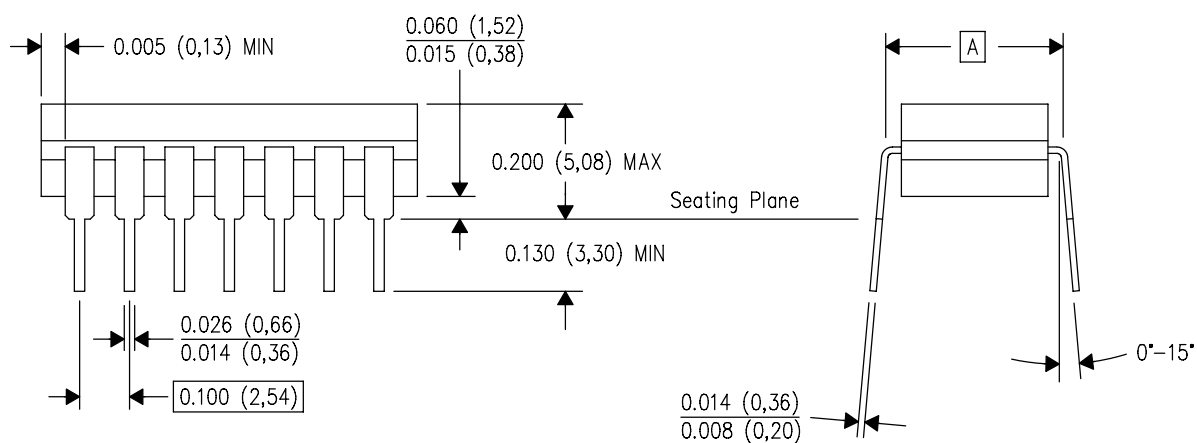
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



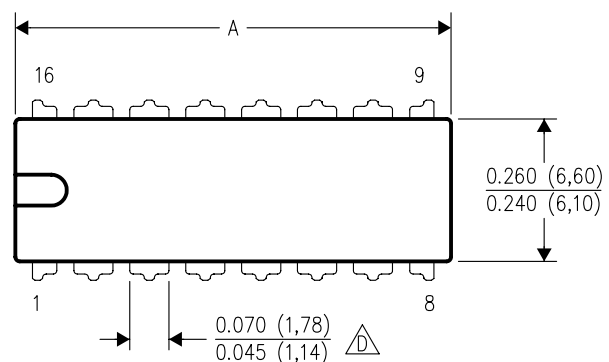
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

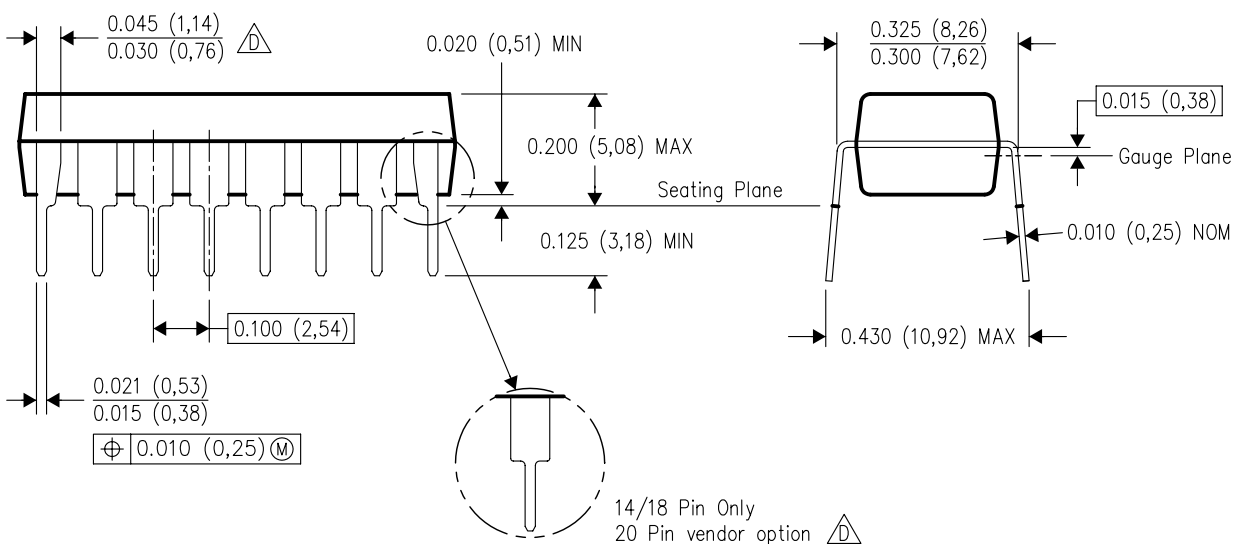
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

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