CDC318A
1-LINE TO 18-LINE CLOCK DRIVER WITH I²C CONTROL INTERFACE

SCAS614A − SEPTEMBER 1998 − REVISED JUNE 2002

- **High-Speed, Low-Skew 1-to-18 Clock Buffer for Synchronous DRAM (SDRAM) Clock Buffering Applications**
- **Output Skew, $t_{sk(o)}$, Less Than 250 ps**
- **Pulse Skew, $t_{sk(p)}$, Less Than 500 ps**
- **Supports up to Four Unbuffered SDRAM Dual Inline Memory Modules (DIMMs)**
- **I²C Serial Interface Provides Individual Enable Control for Each Output**
- **Operates at 3.3 V**
- **Distributed V_{CC} and Ground Pins Reduce Switching Noise**
- **100-MHz Operation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015**
- **Packaged in 48-Pin Shrink Small Outline (DL) Package**

DL PACKAGE
(TOP VIEW)

NC	1	48	NC
NC	2	47	NC
V_{CC}	3	46	V_{CC}
1Y0	4	45	4Y3
1Y1	5	44	4Y2
GND	6	43	GND
V_{CC}	7	42	V_{CC}
1Y2	8	41	4Y1
1Y3	9	40	4Y0
GND	10	39	GND
A	11	38	OE
V_{CC}	12	37	V_{CC}
2Y0	13	36	3Y3
2Y1	14	35	3Y2
GND	15	34	GND
V_{CC}	16	33	V_{CC}
2Y2	17	32	3Y1
2Y3	18	31	3Y0
GND	19	30	GND
V_{CC}	20	29	V_{CC}
5Y0	21	28	5Y1
GND	22	27	GND
V_{CC}	23	26	GND
SDATA	24	25	SCLOCK

NC − No internal connection

description

The CDC318A is a high-performance clock buffer designed to distribute high-speed clocks in PC applications. This device distributes one input (A) to 18 outputs (Y) with minimum skew for clock distribution. The CDC318A operates from a 3.3-V power supply. It is characterized for operation from 0°C to 70°C.

This device has been designed with consideration for optimized EMI performance. Depending on the application layout, damping resistors in series to the clock outputs (like proposed in the PC100 specification) may not be needed in most cases.

The device provides a standard mode (100K-bits/s) I²C serial interface for device control. The implementation is as a slave/receiver. The device address is specified in the I²C device address table. Both of the I²C inputs (SDATA and SCLOCK) are 5-V tolerant and provide integrated pullup resistors (typically 140 kΩ).

Three 8-bit I²C registers provide individual enable control for each of the outputs. All outputs default to enabled at powerup. Each output can be placed in a disabled mode with a low-level output when a low-level control bit is written to the control register. The registers are write only and must be accessed in sequential order (i.e., random access of the registers is not supported).

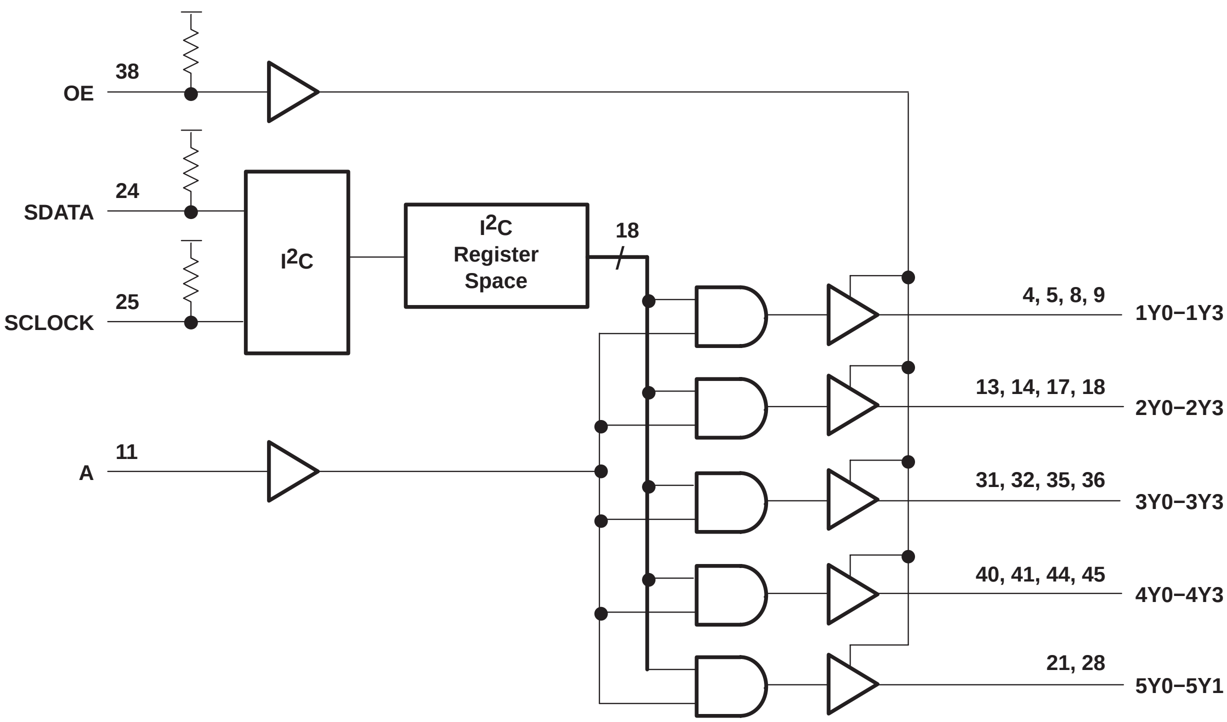
The CDC318A provides 3-state outputs for testing and debugging purposes. The outputs can be placed in a high-impedance state via the output-enable (OE) input. When OE is high, all outputs are in the operational state. When OE is low, the outputs are placed in a high-impedance state. OE provides an integrated pullup resistor.

FUNCTION TABLE

INPUTS		OUTPUTS				
OE	**A**	**1Y0−1Y3**	**2Y0−2Y3**	**3Y0−3Y3**	**4Y0−4Y3**	**5Y0−5Y1**
L	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
H	L	L	L	L	L	L
H	H	H†	H†	H†	H†	H†

† The function table assumes that all outputs are enabled via the appropriate I2C configuration register bit. If the output is disabled via the appropriate configuration bit, then the output is driven to a low state, regardless of the state of the A input.

logic diagram (positive logic)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
1Y0−1Y3	4, 5, 8, 9	O	3.3-V SDRAM byte 0 clock outputs
2Y0−2Y3	13, 14, 17, 18	O	3.3-V SDRAM byte 1 clock outputs
3Y0−3Y3	31, 32, 35, 36	O	3.3-V SDRAM byte 2 clock outputs
4Y0−4Y3	40, 41, 44, 45	O	3.3-V SDRAM byte 3 clock outputs
5Y0−5Y1	21, 28	O	3.3-V clock outputs provided for feedback control of external phase-locked loops (PLLs)
A	11	I	Clock input
OE	38	I	Output enable. When asserted, OE puts all outputs in a high-impedance state. A nominal 140-kΩ pullup resistor is internally integrated.
SCLOCK	25	I	I2C serial clock input. A nominal 140-kΩ pullup resistor is internally integrated.
SDATA	24	I/O	Bidirectional I2C serial data input/output. A nominal 140-kΩ pullup resistor is internally integrated.
GND	6, 10, 15, 19, 22, 26, 27, 30, 34, 39, 43		Ground
NC	1, 2, 47, 48		No internal connection. Reserved for future use.
V_{CC}	3, 7, 12, 16, 20, 23, 29, 33, 37, 42, 46		3.3-V power supply

I2C DEVICE ADDRESS

A7	A6	A5	A4	A3	A2	A1	A0 (R/W)
H	H	L	H	L	L	H	—

I2C BYTE 0-BIT DEFINITION†

BIT	DEFINITION	DEFAULT VALUE
7	2Y3 enable (pin 18)	H
6	2Y2 enable (pin 17)	H
5	2Y1 enable (pin 14)	H
4	2Y0 enable (pin 13)	H
3	1Y3 enable (pin 9)	H
2	1Y2 enable (pin 8)	H
1	1Y1 enable (pin 5)	H
0	1Y0 enable (pin 4)	H

† When the value of the bit is high, the output is enabled. When the value of the bit is low, the output is forced to a low state. The default value of all bits is high.

I2C BYTE 1-BIT DEFINITION†

BIT	DEFINITION	DEFAULT VALUE
7	4Y3 enable (pin 45)	H
6	4Y2 enable (pin 44)	H
5	4Y1 enable (pin 41)	H
4	4Y0 enable (pin 40)	H
3	3Y3 enable (pin 36)	H
2	3Y2 enable (pin 35)	H
1	3Y1 enable (pin 32)	H
0	3Y0 enable (pin 31)	H

† When the value of the bit is high, the output is enabled. When the value of the bit is low, the output is forced to a low state. The default value of all bits is high.

I2C BYTE 2-BIT DEFINITION†

BIT	DEFINITION	DEFAULT VALUE
7	5Y1 enable (pin 28)	H
6	5Y0 enable (pin 21)	H
5	Reserved	H
4	Reserved	H
3	Reserved	H
2	Reserved	H
1	Reserved	H
0	Reserved	H

† When the value of the bit is high, the output is enabled. When the value of the bit is low, the output is forced to a low state. The default value of all bits is high.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . −0.5 V to 4.6 V
Input voltage range, V_I (SCLOCK, SDATA) (see Note 1) . . . −0.5 V to 6.5 V
Output voltage range, V_O (SDATA) (see Note 1) . . . −0.5 V to 6.5 V
Voltage range applied to any output in the high or power-off state, V_O . . . −0.5 V to V_{CC} +0.5 V
Current into any output in the low state (except SDATA), I_O . . . 48 mA
Current into SDATA in the low state, I_O . . . 12 mA
Input clamp current, I_{IK} (V_I < 0) (SCLOCK) . . . −50 mA
Output clamp current, I_{OK} (V_O < 0) (SDATA) . . . −50 mA
Package thermal impedance, θ_{JA} (see Notes 2 and 3) . . . 84°C/W
Storage temperature range, T_{stg} . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero. The absolute maximum power dissipation allowed at T_A = 55°C (in still air) is 1.2 W.
3. Thermal impedance (Θ_{JA}) can be considerably lower if the device is soldered on the PCB board with a copper layer underneath the package. A simulation on a PCB board (3 in. × 3 in.) with two internal copper planes (1 oz. cu, 0.036 mm thick) and 0.071 mm cu (202) in area underneath the package, resulted in Θ_{JA} = 60°C/W. This would allow 1.2 W total power dissipation at TA = 70°C.

recommended operating conditions (see Note 4)

			MIN	TYP	MAX	UNIT
V_{CC}	3.3-V core supply voltage		3.135		3.465	V
V_{IH}	High-level input voltage	A, OE	2		V_{CC}+0.3	V
		SDATA, SCLOCK (see Note 3)	2.2		5.5	V
V_{IL}	Low-level input voltage	A, OE	−0.3		0.8	V
		SDATA, SCLOCK (see Note 3)	0		1.04	V
I_{OH}	High-level output current	Y outputs			−36	mA
I_{OL}	Low-level output current	Y outputs			24	mA
r_i	Input resistance to V_{CC}	SDATA, SCLOCK (see Note 3)		140		kΩ
$f_{(SCL)}$	SCLOCK frequency				100	kHz
$t_{(BUS)}$	Bus free time		4.7			µs
$t_{su(START)}$	START setup time		4.7			µs
$t_{h(START)}$	START hold time		4			µs
$t_{w(SCLL)}$	SCLOCK low pulse duration		4.7			µs
$t_{w(SCLH)}$	SCLOCK high pulse duration		4			µs
$t_{r(SDATA)}$	SDATA input rise time				1000	ns
$t_{f(SDATA)}$	SDATA input fall time				300	ns
$t_{su(SDATA)}$	SDATA setup time		250			ns
$t_{h(SDATA)}$	SDATA hold time		20			ns
$t_{su(STOP)}$	STOP setup time		4			µs
T_A	Operating free-air temperature		0		70	°C

NOTE 4: The CMOS-level inputs fall within these limits: V_{IH} min = 0.7 × V_{CC} and V_{IL} max = 0.3 × V_{CC}.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IK}	Input clamp voltage		V_{CC} = 3.135 V,	I_I = −18 mA			−1.2	V
V_{OH}	High-level output voltage	Y outputs	V_{CC} = Min to Max,	I_{OH} = −1 mA	V_{CC} − 0.1 V			V
			V_{CC} = 3.135 V,	I_{OH} = −36 mA	2.4			
V_{OL}	Low-level output voltage	Y outputs	V_{CC} = Min to Max,	I_{OL} = 1 mA			0.1	V
			V_{CC} = 3.135 V,	I_{OL} = 24 mA			0.4	
		SDATA	V_{CC} = 3.135 V	I_{OL} = 3 mA			0.4	
				I_{OL} = 6 mA			0.6	
I_{OH}	High-level output current	SDATA	V_{CC} = 3.135 V,	V_O = V_{CC} MAX			20	µA
		Y outputs	V_{CC} = 3.135 V,	V_O = 2 V	−54		−126	mA
			V_{CC} = 3.3 V,	V_O = 1.65 V		−92		
			V_{CC} = 3.465 V,	V_O = 3.135 V	−21		−46	
I_{OL}	Low-level output current	Y outputs	V_{CC} = 3.135 V,	V_O = 1 V	49		118	mA
			V_{CC} = 3.3 V,	V_O = 1.65 V		93		
			V_{CC} = 3.465 V,	V_O = 0.4 V	24		53	
I_{IH}	High-level input current	A	V_{CC} = 3.465 V,	V_I = V_{CC}			5	µA
		OE					20	
		SCLOCK, SDATA					20	
I_{IL}	Low-level input current	A	V_{CC} = 3.465 V,	V_I = GND			−5	µA
		OE			−10		−50	
		SCLOCK, SDATA			−10		−50	
I_{OZ}	High-impedance-state output current		V_{CC} = 3.465 V,	V_O = 3.465 V or 0			±10	µA
I_{off}	Off-state current	SCLOCK, SDATA	V_{CC} = 0,	V_I = 0 V to 5.5 V			50	µA
I_{CC}	Supply current		V_{CC} = 3.465 V,	I_O = 0		0.2	0.5	mA
ΔI_{CC}	Change in supply current		V_{CC} = 3.135 V to 3.465 V, One input at V_{CC} − 0.6 V, All other inputs at V_{CC} or GND				500	µA
	Dynamic I_{CC} at 100 MHz		V_{CC} = 3.465 V,	C_L = 20 pF,		230		mA
C_I	Input capacitance		V_I = V_{CC} or GND,	V_{CC} = 3.3 V		4		pF
C_O	Output capacitance		V_O = V_{CC} or GND,	V_{CC} = 3.3 V		6		pF
$C_{I/O}$	SDATA I/O capacitance		$V_{I/O}$ = V_{CC} or GND,	V_{CC} = 3.3 V		7		pF

switching characteristics over recommended operating conditions

PARAMETER			FROM	TO	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Low-to-high level propagation delay time		A	Y		1.2	4.5	ns
			SCLOCK↓	SDATA valid	V_{CC} = 3.3 V ±0.165 V, See Figure 3		2	µs
t_{PLH}	Low-to-high level propagation delay time		SDATA↑	Y	V_{CC} = 3.3 V ±0.165 V, See Figure 3		150	ns
t_{PHL}	High-to-low level propagation delay time		A	Y		1.2	4.5	ns
			SCLOCK↓	SDATA valid	V_{CC} = 3.3 V ±0.165 V, See Figure 3		2	µs
t_{PHL}	High-to-low level propagation delay time		SDATA↑	Y	V_{CC} = 3.3 V ±0.165 V, See Figure 3		150	ns
t_{PZH}	Enable time to the high level		OE	Y		1	7	ns
t_{PZL}	Enable time to the low level					1	7	
t_{PHZ}	Disable time from the high level		OE	Y		1	7	ns
t_{PLZ}	Disable time from the low level					1	7	
$t_{sk(o)}$	Skew time		A	Y			250	ps
$t_{sk(p)}$	Skew time		A	Y			500	ps
$t_{sk(pr)}$	Skew time		A	Y			1	ns
t_r	Rise time			Y		0.5	2.2	ns
t_r	Rise time (see Note 5 and Figure 3)	SDATA			C_L = 10 pF	6		ns
					C_L = 400 pF		950	
t_f	Fall time			Y		0.5	2.3	ns
t_f	Fall time (see Note 5 and Figure 3)	SDATA			C_L = 10 pF	20		ns
					C_L = 400 pF		250	

NOTE 5: This parameter has a lower limit than BUS specification. This allows use of series resistors for current spike protection.

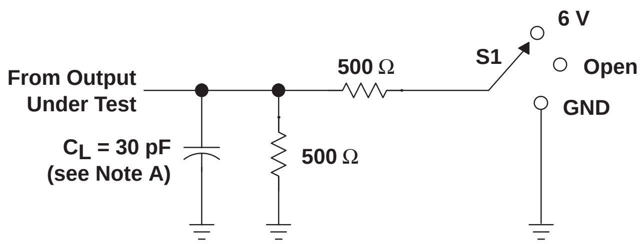
ESD information

ESD MODELS	LIMIT
Human Body Model (HBM)	2.0 kV
Machine Model (MM)	200 V
Charge Device Model (CDM)	2.0 kV

thermal information

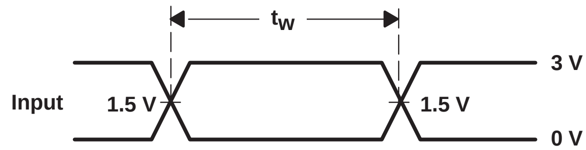
CDC318A 48-PIN SSOP			THERMAL AIR FLOW (CFM)				UNIT
			0	150	250	500	
$R_{\theta JA}$	High K		62	56	54	51	°C/W
$R_{\theta JA}$	Low K		95	71	65	58	°C/W
$R_{\theta JC}$	High K	36					°C/W
$R_{\theta JC}$	Low K	38					°C/W

PARAMETER MEASUREMENT INFORMATION

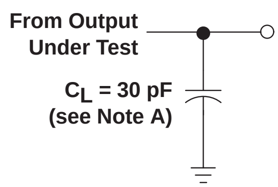


LOAD CIRCUIT FOR t_{pd} AND t_{sk}

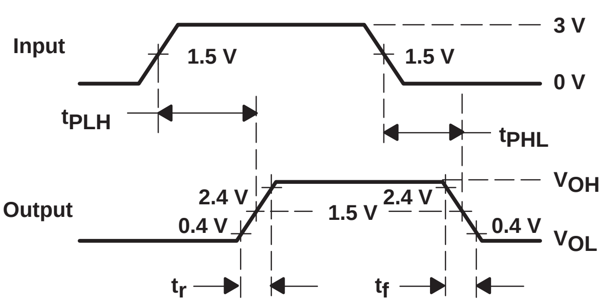
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



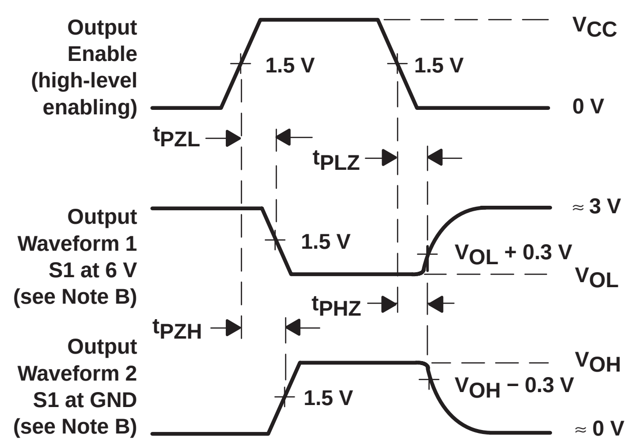
VOLTAGE WAVEFORMS



LOAD CIRCUIT FOR t_r AND t_f



VOLTAGE WAVEFORMS

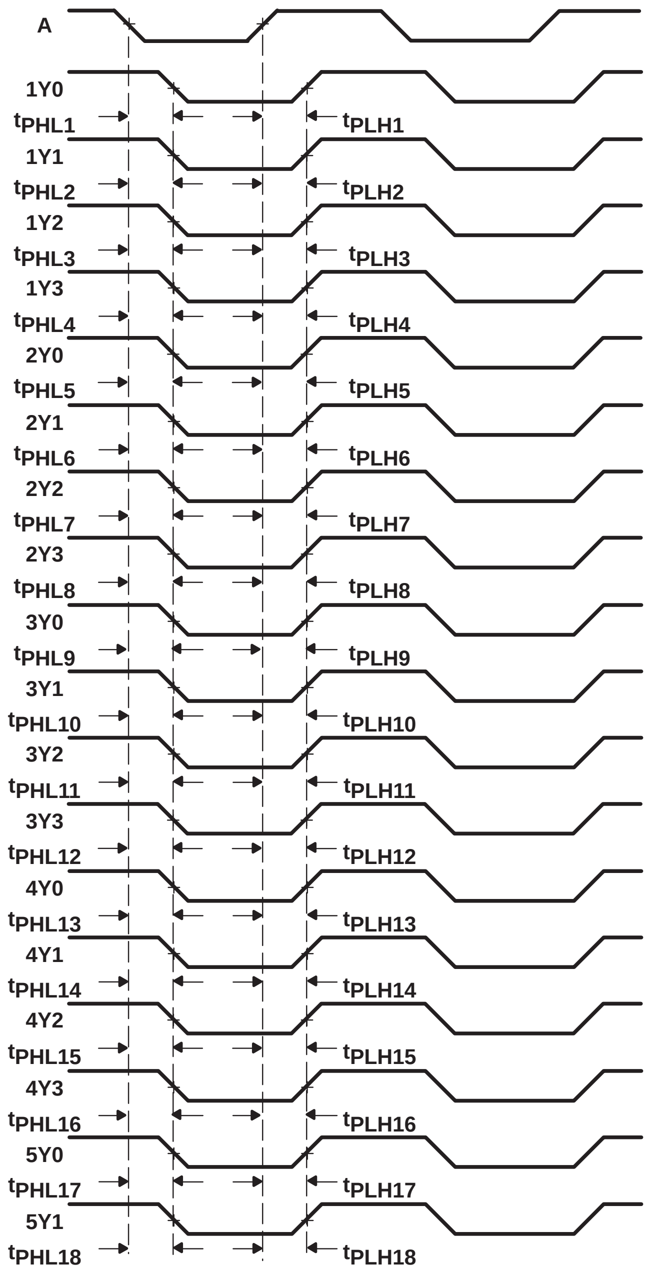


VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



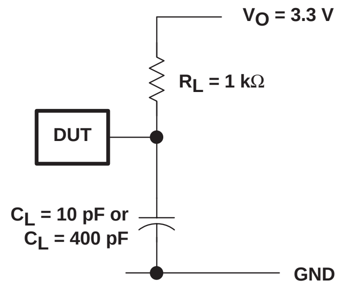
NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLHn} (n = 1:18)
- The difference between the fastest and slowest of t_{PHLn} (n = 1:18)

B. Pulse skew, $t_{sk(p)}$, is calculated as the greater of $|t_{PLHn} - t_{PHLn}|$ (n = 1:18)

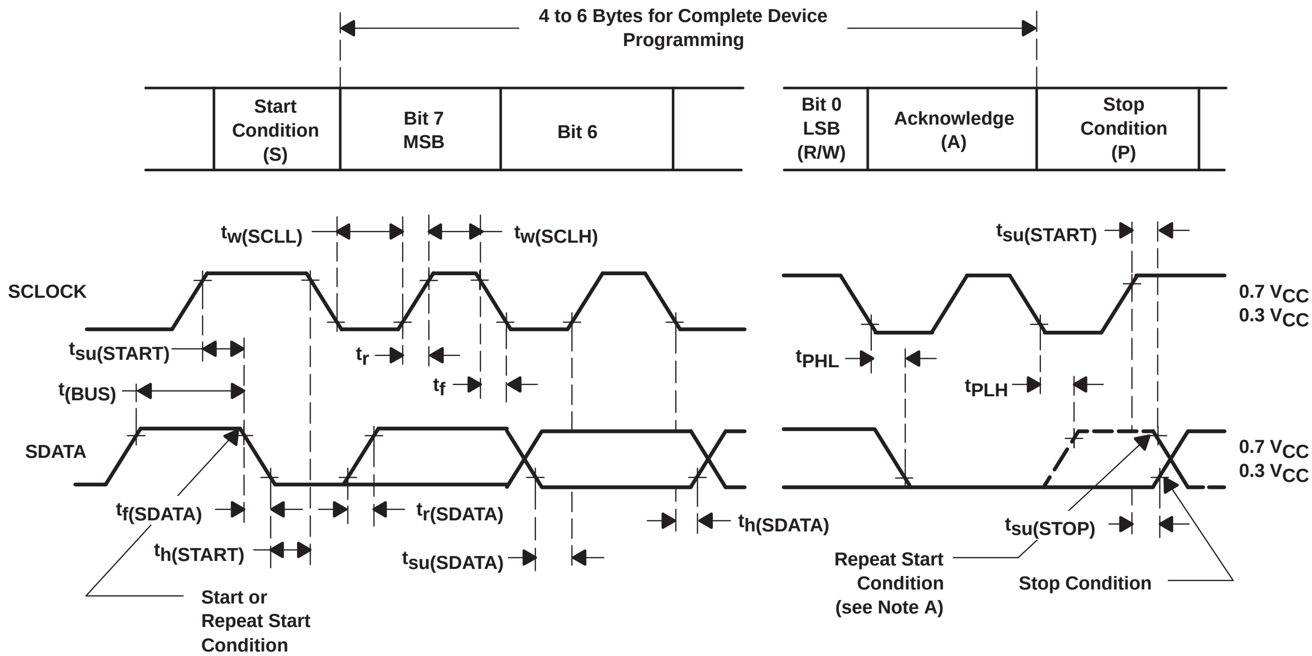
C. Process skew, $t_{sk(pr)}$, is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLHn} (n = 1:18) across multiple devices under identical operating conditions
- The difference between the fastest and slowest of t_{PHLn} (n = 1:18) across multiple devices under identical operating conditions

Figure 2. Waveforms for Calculation of $t_{sk(o)}$, $t_{sk(p)}$, $t_{sk(pr)}$

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I2C address
2	Command (dummy value, ignored)
3	Byte count (dummy value, ignored)
4	I2C data byte 0
5	I2C data byte 1
6	I2C data byte 2

NOTES: A. The repeat start condition is not supported.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 100 kHz, Z_O = 50 Ω, t_r ≥ 10 ns, t_f ≥ 10 ns.

Figure 3. Propagation Delay Times, t_r and t_f

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CDC318ADL	Active	Production	SSOP (DL) | 48	25 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	CDC318A
CDC318ADL.B	Active	Production	SSOP (DL) | 48	25 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	CDC318A
CDC318ADLG4	Active	Production	SSOP (DL) | 48	25 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	CDC318A
CDC318ADLR	Active	Production	SSOP (DL) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	CDC318A
CDC318ADLR.B	Active	Production	SSOP (DL) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	CDC318A
CDC318ADLRG4	Active	Production	SSOP (DL) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	CDC318A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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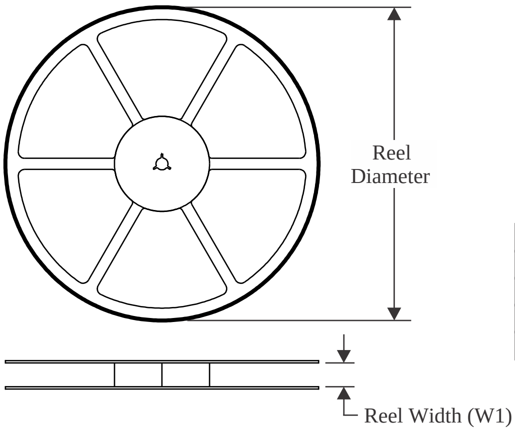
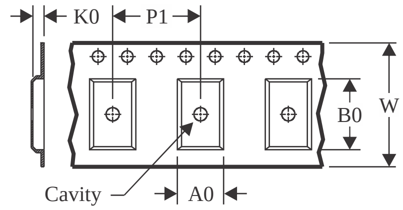
TAPE AND REEL INFORMATION

REEL DIMENSIONS

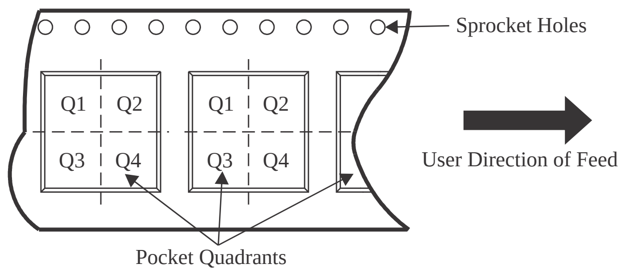


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

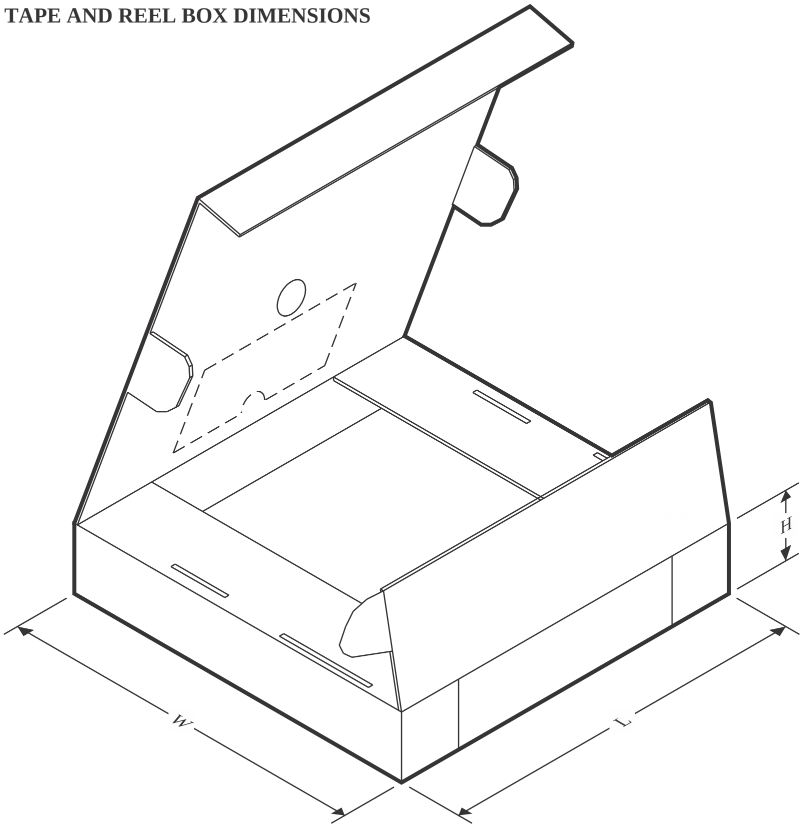
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDC318ADLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

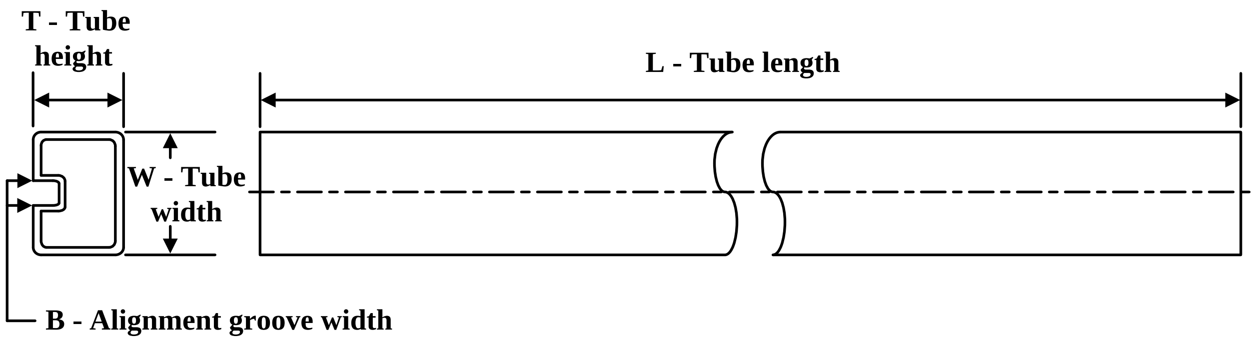
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDC318ADLR	SSOP	DL	48	1000	356.0	356.0	53.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CDC318ADL	DL	SSOP	48	25	473.7	14.24	5110	7.87
CDC318ADL.B	DL	SSOP	48	25	473.7	14.24	5110	7.87
CDC318ADLG4	DL	SSOP	48	25	473.7	14.24	5110	7.87