CDCE949-Q1: Programmable 4-PLL VCXO Clock Synthesizer With 1.8V, 2.5V, and 3.3V LVCMOS Outputs

1 Features

- Qualified for Automotive Applications
- Member of Programmable Clock Generator Family
  - CDCE913/CDCEL913: 1 PLLs, 3 Outputs
  - CDCE925/CDCEL925: 2 PLLs, 5 Outputs
  - CDCE937/CDCEL937: 3 PLLs, 7 Outputs
  - *CDCE949: 4 PLLs, 9 Outputs*
- In-System Programmability and EEPROM
  - Serial Programmable Volatile Register
  - Non-Volatile EEPROM to Store Customer Settings
- Highly Flexible Clock Driver
  - Three User-Definable Control Inputs [S0/S1/S2]; such as SSC-Selection, Frequency Switching, Output Enable or Power Down
  - Generates Highly-Accurate Clocks for Video, Audio, USB, IEEE1394, RFID, Generates Common Clock Frequencies Used with TI DaVinci™, OMAP™, DSPs
  - BlueTooth™, WLAN, Ethernet and GPS
  - Programmable SSC Modulation
  - Enables 0ppm Clock Generation
- Selectable Output Frequency up to 230MHz
- Flexible Input Clocking Concept
  - External Crystal: 8MHz to 32MHz
  - On-Chip VCXO: Pull-Range ±150ppm
  - Single-Ended LVCMOS up to 160MHz
- Low-Noise PLL Core
  - Integrated PLL Loop Filter Components
  - Very Low Period Jitter (typical 60ps)
- Separate Output Supply Pins
  - 3.3V and 2.5V
- 1.8V Device Power Supply
- Latch-Up Performance Meets 100mA Per JESD 78, Class I
- Wide Temperature Range –40°C to 125°C
- Packaged in TSSOP
- Development and Programming Kit for Ease PLL Design and Programming (TI ClockPro)

2 Applications

- Set-Top Boxes (STBs), High-Definition Televisions (HDTVs), Printers, DVD-Players, DVD-Recorders

3 Description

The CDCE949-Q1 is a modular PLL-based low-cost high-performance programmable clock synthesizer, multiplier, and divider. The device generates up to 9 output clocks from a single input frequency. Each output can be programmed in-system for any clock frequency up to 230MHz, using up to four independent configurable PLLs.

The CDCE949-Q1 has separate output supply pins, V_{DDOUT}, of 2.5V to 3.3V.

The input accepts an external crystal or LVCMOS clock signal. If an external crystal is used, an on-chip load capacitor is adequate for most applications. The value of the load capacitor is programmable from 0pF to 20pF. Additionally, an on-chip VCXO is selectable, allowing synchronization of the output frequency to an external control signal, that is, a PWM signal.

The deep M/N divider ratio allows the generation of zero-ppm audio/video, networking (WLAN, BlueTooth™, Ethernet, GPS) or Interface (USB, IEEE1394, Memory Stick) clocks from a reference input frequency, such as 27MHz.

All PLLs support SSC (Spread-Spectrum Clocking). SSC can be Center-Spread or Down-Spread clocking. This technique is common for reducing electro-magnetic interference (EMI).

Based on the PLL frequency and the divider settings, the internal loop-filter components are automatically adjusted to achieve high stability, and to optimize the jitter-transfer characteristics of each PLL.

The device supports non-volatile EEPROM programming for easy customization to the application. The CDCE949-Q1 is preset to a factory-default configuration (see the *Default Device Configuration* section). The device can be reprogrammed to a different application configuration before PCB assembly, or reprogrammed by in-system programming. All device settings are programmable through the SDA/SCL bus, a 2-wire serial interface.

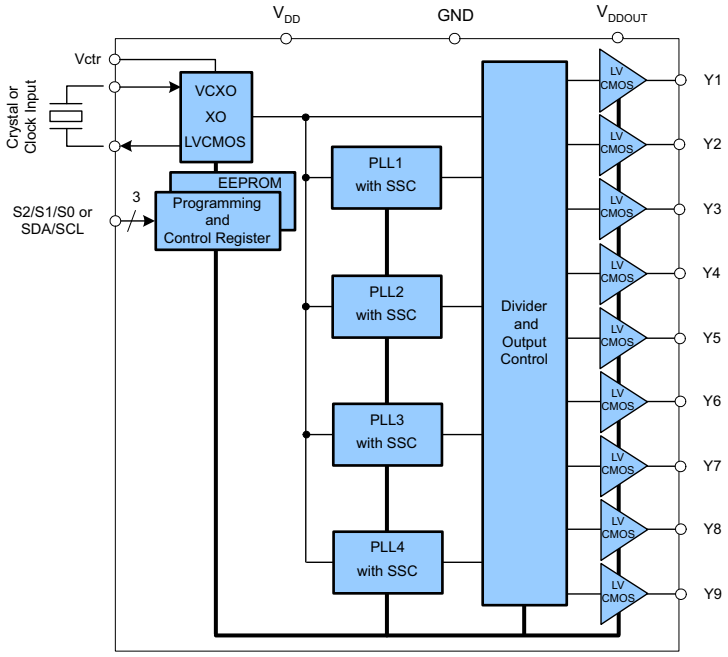
Three programmable control inputs, S0, S1 and S2, can be used to control various aspects of operation including frequency selection, changing the SSC parameters to lower EMI, PLL bypass, power down, and choosing between low level or 3-state for the output-disable function.

The CDCE949-Q1 operates in a 1.8V environment. The device operates within a temperature range of –40°C to 125°C.

Table 3-1. Package Information

DEVICE	PACKAGE(1)	PACKAGE SIZE(2)
CDCE949-Q1	PW (TSSOP, 24)	7.8mm × 6.4mm

(1) For more information, see Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



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4 Pin Functions

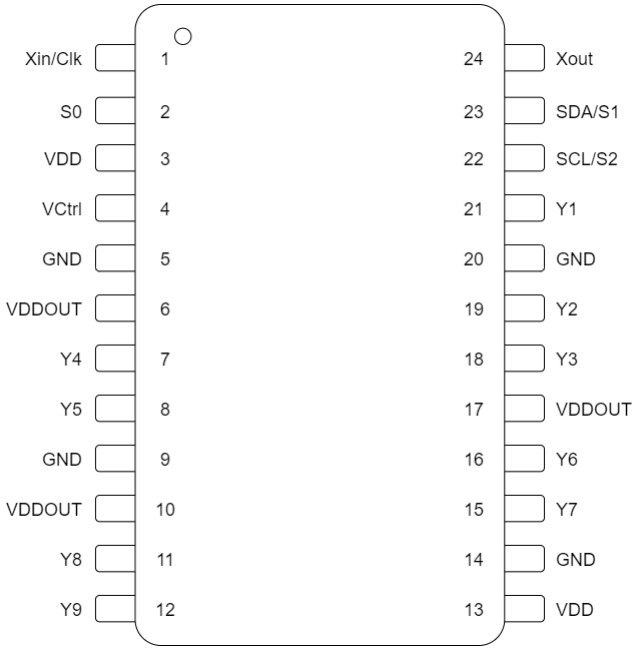


Figure 4-1. PW Package 24-Pin TSSOP Top View

Table 4-1. Pin Functions

TERMINAL		TYPE[1]	DESCRIPTION
NAME	NO.		
GND	5, 9, 14, 20	G	Ground
S0	2	I	User-programmable control input S0; LVCMOS inputs; internal pullup 500kΩ
SCL / S2	22	I	**SCL:** Serial clock input (default configuration), LVCMOS; internal pullup 500kΩ; or **S2:** User-programmable control input; LVCMOS inputs; internal pullup 500kΩ
SDA / S1	23	I/O, I	**SDA:** Bidirectional serial data input/output (default configuration), LVCMOS; internal pullup 500kΩ; or **S1:** User-programmable control input; LVCMOS inputs; internal pullup 500kΩ
V_{Ctrl}	4	I	VCXO control voltage (leave open or pull up when not used)
V_{DD}	3, 13	P	1.8V power supply for the device
V_{DDOUT}	6, 10, 17	P	3.3V or 2.5V supply for all outputs
Y1	21	O	LVCMOS outputs
Y2	19	O	
Y3	18	O	
Y4	7	O	
Y5	8	O	
Y6	16	O	
Y7	15	O	
Y8	11	O	
Y9	12	O	
Xin/CLK	1	I	Crystal oscillator input or LVCMOS clock input (selectable with SDA/SCL bus)
Xout	24	O	Crystal oscillator output (leave open or pullup when not used)

(1) I = Input, O = Output, P = Power, G = Ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE	UNIT
V_{DD}	Supply voltage range	–0.5 to 2.5	V
V_I	Input voltage range(2) (3)	–0.5 to V_{DD} + 0.5	V
V_O	Output voltage range(2)	–0.5 to V_{DDOUT} + 0.5	V
I_I	Input current (V_I < 0, V_I > V_{DD})	20	mA
I_O	Continuous output current	50	mA
T_{stg}	Storage temperature range	–65 to 150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output negative voltage ratings can be exceeded if the input and output clamp–current ratings are observed.
(3) SDA and SCL can go up to 3.6V as stated in the *Recommended Operating Conditions* table.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011(2)	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) Charged-device model ESD rating for corner pins is 750V.

5.3 Thermal Resistance Characteristics

PARAMETER(1)		AIRFLOW (lfm)	°C/W
θ_{JA}	Thermal resistance, junction to ambient	0	91
		150	75
		200	74
		250	73
		500	65
θ_{JC}	Thermal resistance, junction to case	—	27
θ_{JB}	Thermal resistance, junction to board	—	52
$R_{\theta JT}$	Thermal resistance, junction to top	—	0.5
$R_{\theta JB}$	Thermal resistance, junction to bottom	—	50

(1) The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).

5.4 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Device supply voltage		1.7	1.8	1.9	V
$V_{DD(OUT)}$	Output Yx supply voltage		2.3		3.6	V
V_{IL}	Low level input voltage LVCMOS				0.3 × V_{DD}	V
V_{IH}	High level input voltage LVCMOS		0.7 × V_{DD}			V
$V_{I(thresh)}$	Input voltage threshold LVCMOS			0.5 × V_{DD}		V
V_{IS}	Input voltage range S0		0		1.9	V
	Input voltage range S1, S2, SDA, SCL	$V_{Ithresh}$ = 0.5V_{DD}	0		3.6	
V_{ICLK}	Input voltage range CLK		0		1.9	V
I_{OH} /I_{OL}	Output current	V_{DDout} = 3.3V			±12	mA
		V_{DDout} = 2.5V			±10	mA
		V_{DDout} = 1.8V			±8	mA
C_L	Output load LVCMOS				10	pF
T_J	Operating junction temperature		–40		125	°C

5.5 Recommended Crystal/VCXO Specifications

		MIN	NOM	MAX	UNIT
f_{Xtal}	Crystal Input frequency range (fundamental mode) (1)	8	27	32	MHz
ESR	Effective series resistance			100	Ω
f_{PR}	Pulling range (0V ≤ V_{Ctrl} ≤ 1.8V)(2)	±120	±150		ppm
$V_{(Ctrl)}$	Frequency control voltage	0		V_{DD}	V
C_0/C_1	Pull-ability ratio			220	
C_L	On-chip load capacitance at Xin and Xout	0		20	pF

(1) For more information about VCXO configuration and crystal recommendation see *VCXO Application Guideline for CDCE(L)9xx Family* application note.
(2) Pulling range depends on crystal type, on-chip crystal load capacitance and PCB stray capacitance; pulling range of minimum ±120ppm applies for crystal listed in the *VCXO Application Guideline for CDCE(L)9xx Family* application note.

5.6 EEPROM Specification

		MIN	TYP	MAX	UNIT
EEcyc	EEcyc programming cycles of EEPROM	1000			cycles
EEret	EEret data retention	10			years

5.7 Electrical Characteristics

over recommended operating junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
OVERALL PARAMETER							
I_{DD}	Supply current (see Figure 5-2)	All outputs off, f_{CLK} = 27MHz, f_{VCO}= 135MHz	All PLLs on		38		mA
			Per PLL		9		
$I_{DD(OUT)}$	Supply current (see Figure 5-3)	No load, all outputs on, f_{out} = 27MHz, V_{DDOUT} = 3.3V			4		mA
$I_{DD(PD)}$	Power down current. Every circuit powered down except SDA/SCL.	f_{IN} = 0MHz, V_{DD} = 1.9V			50		µA
$V_{(PUC)}$	Supply voltage V_{DD} threshold for power up control circuit			0.85		1.45	V
f_{VCO}	VCO frequency range of PLL			80		230	MHz
f_{OUT}	LVCMOS output frequency			230			MHz
LVCMOS PARAMETER							
V_{IK}	LVCMOS input voltage	V_{DD} = 1.7V; I_I = –18mA				–1.2	V
I_I	LVCMOS input current	V_I = 0V or V_{DD}; V_{DD} = 1.9V				±5	µA
I_{IH}	LVCMOS input current for S0/S1/S2	V_I = V_{DD}; V_{DD} = 1.9V				5	µA
I_{IL}	LVCMOS input current for S0/S1/S2	V_I = 0V; V_{DD} = 1.9V				–4	µA
C_I	Input capacitance at Xin/Clk	V_{ICLK} = 0V or V_{DD}			6		pF
	Input capacitance at Xout	V_{IXout} = 0V or V_{DD}			2		
	Input capacitance at S0/S1/S2	V_{IS} = 0V or V_{DD}			3		
LVCMOS PARAMETER FOR V_{DDOUT} = 3.3V – MODE							
V_{OH}	LVCMOS high-level output voltage	V_{DDOUT} = 3V, I_{OH} = –0.1mA		2.9			V
		V_{DDOUT} = 3V, I_{OH} = –8mA		2.4			
		V_{DDOUT} = 3V, I_{OH} = –12mA		2.2			
V_{OL}	LVCMOS low-level output voltage	V_{DDOUT} = 3V, I_{OL} = 0.1mA				0.1	V
		V_{DDOUT} = 3V, I_{OL} = 8mA				0.5	
		V_{DDOUT} = 3V, I_{OL} = 12mA				0.8	
t_{PLH}, t_{PHL}	Propagation delay	PLL bypass			3.2		ns
t_r/t_f	Rise and fall time	V_{DDOUT} = 3.3V (20%–80%)			0.6		ns
$t_{jit(cc)}$	Cycle-to-cycle jitter(2) (3)	1 PLL switching, Y2-to-Y3			60	90	ps
		4 PLLs switching, Y2-to-Y9			120	170	
$t_{jit(per)}$	Peak-to-peak period jitter (2) (3)	1 PLL switching, Y2-to-Y3			70	100	ps
		4 PLLs switching, Y2-to-Y9			130	180	
$t_{sk(o)}$	Output skew(4)	f_{OUT} = 50MHz; Y1-to-Y3				60	ps
		f_{OUT} = 50MHz; Y2-to-Y5 or Y6-to-Y9				160	
odc	Output duty cycle(5)	f_{VCO} = 100MHz; Pdiv = 1		45		55	%

5.7 Electrical Characteristics (continued)

over recommended operating junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
LVCMOS PARAMETER FOR V_{DDOUT} = 2.5V – MODE						
V_{OH}	LVCMOS high-level output voltage	V_{DDOUT} = 2.3V, I_{OH} = –0.1mA	2.2			V
		V_{DDOUT} = 2.3V, I_{OH} = –6mA	1.7			
		V_{DDOUT} = 2.3V, I_{OH} = –10mA	1.6			
V_{OL}	LVCMOS low-level output voltage	V_{DDOUT} = 2.3V, I_{OL} = 0.1mA			0.1	V
		V_{DDOUT} = 2.3V, I_{OL} = 6mA			0.5	
		V_{DDOUT} = 2.3V, I_{OL} = 10mA			0.7	
t_{PLH}, t_{PHL}	Propagation delay	PLL bypass		3.4		ns
t_r/t_f	Rise and fall time	V_{DDOUT} = 2.5V (20%–80%)		0.8		ns
$t_{jit(cc)}$	Cycle-to-cycle jitter (2) (3)	1 PLL switching, Y2-to-Y3		60	90	ps
		4 PLLs switching, Y2-to-Y9		120	170	
$t_{jit(per)}$	Peak-to-peak period jitter (2) (3)	1 PLL switching, Y2-to-Y3		70	100	ps
		4 PLLs switching, Y2-to-Y9		130	180	
$t_{sk(o)}$	Output skew(4)	f_{OUT} = 50MHz; Y1-to-Y3			60	ps
		f_{OUT} = 50MHz; Y2-to-Y5 or Y6-to-Y9			160	
odc	Output duty cycle(5)	f_{VCO} = 100MHz; Pdiv = 1	45		55	%
SDA/SCL PARAMETER						
V_{IK}	SCL and SDA input clamp voltage	V_{DD} = 1.7V; I_I = –18mA			–1.2	V
I_{IH}	SCL and SDA input current	V_I = V_{DD}; V_{DD} = 1.9V			±10	µA
V_{IH}	SDA/SCL input high voltage(6)		0.7V_{DD}			V
V_{IL}	SDA/SCL input low voltage(6)				0.3V_{DD}	V
V_{OL}	SDA low-level output voltage	I_{OL} = 3mA, V_{DD} = 1.7V			0.2V_{DD}	V
C_I	SCL/SDA input capacitance	V_I = 0V or V_{DD}		3	10	pF

(1) All typical values are at respective nominal V_{DD}.
(2) 10000 cycles.
(3) Jitter depends on device configuration. Data is taken under the following conditions: 1-PLL: f_{IN} = 27MHz, Y2/3 = 27MHz, (measured at Y2), 4-PLL: f_{IN} = 27MHz, Y2/3 = 27MHz, (manured at Y2), Y4/5 = 16.384MHz, Y6/7 = 74.25MHz, Y8/9 = 48MHz.
(4) The $t_{sk(o)}$ specification is only valid for equal loading of each bank of outputs and outputs are generated from the same divider; data sampled on rising edge (t_r).
(5) odc depends on output rise- and fall-time (t_r/t_f).
(6) SDA and SCL pins are 3.3V tolerant.

5.8.1 CLK_IN Timing Requirements

over recommended ranges of supply voltage, load and operating free-air temperature

			MIN	NOM	MAX	UNIT
$f_{(CLK)}$	LVCMOS clock input frequency	PLL Bypass Mode	0		160	MHz
		PLL Mode	8		160	
t_r / t_f	Rise and fall time CLK signal (20% to 80%)				3	ns
$duty_{CLK}$	Duty cycle CLK at V_{DD} / 2		40%		60%	

5.8.2 SDA/SCL Timing Requirements

see Figure 5-1

		STANDARD MODE		FAST MODE		UNIT
		MIN	MAX	MIN	MAX	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{su(START)}$	START setup time (SCL high before SDA low)	4.7		0.6		µs

see Figure 5-1

		STANDARD MODE		FAST MODE		UNIT
		MIN	MAX	MIN	MAX	
$t_{h(START)}$	START hold time (SCL low after SDA low)	4		0.6		µs
$t_{w(SCLL)}$	SCL low-pulse duration	4.7		1.3		µs
$t_{w(SCLH)}$	SCL high-pulse duration	4		0.6		µs
$t_{h(SDA)}$	SDA hold time (SDA valid after SCL low)	0	3.45	0	0.9	µs
$t_{su(SDA)}$	SDA setup time	250		100		ns
t_r	SCL/SDA input rise time		1000		300	ns
t_f	SCL/SDA input fall time		300		300	ns
$t_{su(STOP)}$	STOP setup time	4.0		0.6		µs
t_{BUF}	Bus free time between a STOP and START condition	4.7		1.3		µs

5.9 Timing Diagrams

5.9.1 Timing Diagram for the SDA/SCL Serial Control Interface

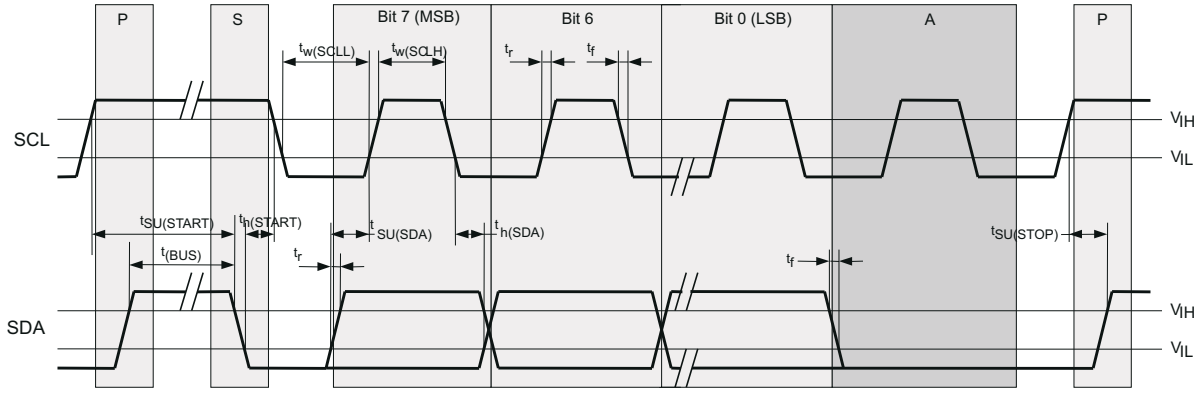


Figure 5-1. Timing Diagram for the SDA/SCL Serial Control Interface

5.10 Typical Characteristics

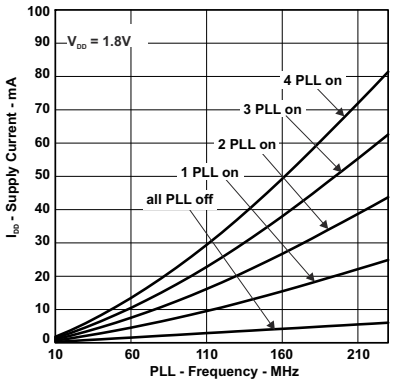


Figure 5-2. Supply Current vs PLL Frequency

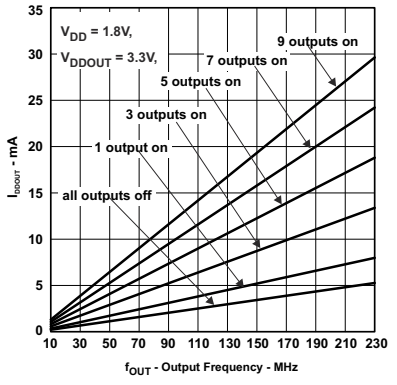


Figure 5-3. Output Current vs Output Frequency

6 Parameter Measurement Information

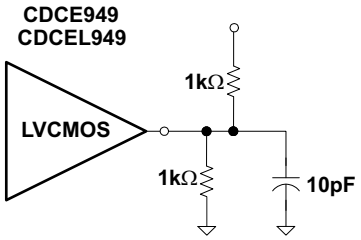


Figure 6-1. Test Load

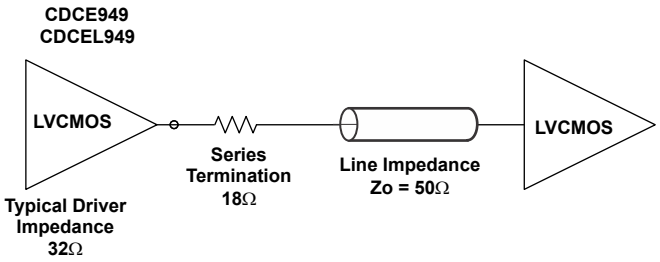


Figure 6-2. Test Load for 50Ω Board Environment

7 Detailed Description

7.1 Overview

The CDCE949-Q1 device is a modular PLL-based, low-cost, high-performance, programmable clock synthesizer, multiplier, and divider. The device generates up to nine output clocks from a single input frequency. Each output can be programmed in-system for any clock frequency up to 230MHz, using one of the four integrated configurable PLLs. The CDCE949-Q1 has output supply pins, VDDOUT, which can be 2.5V or 3.3V.

The input accepts an external crystal or LVCMOS clock signal. If an external crystal is used, an on-chip load capacitor is adequate for most applications. The value of the load capacitor is programmable from 0 to 20pF. Additionally, a selectable on-chip VCXO allows synchronization of the output frequency to an external control signal, that is, the PWM signal.

The deep M/N divider ratio allows the generation of 0ppm audio/video, networking (WLAN, BlueTooth, Ethernet, GPS) or Interface (USB, IEEE1394, Memory Stick) clocks from a reference input frequency such as 27MHz.

All PLLs supports SSC (Spread-Spectrum Clocking). SSC can be Center-Spread or Down-Spread clocking which is a common technique to reduce electro-magnetic interference (EMI).

Based on the PLL frequency and the divider settings, the internal loop filter components are automatically adjusted to achieve high stability and optimized jitter transfer characteristic of each PLL.

The device supports non-volatile EEPROM programming for ease-customized application. The device is preset to a factory default configuration (see Default Device Setting). The device can be reprogrammed to a different application configuration before PCB assembly, or reprogrammed by in-system programming. All device settings are programmable through SDA/SCL bus, a 2-wire serial interface

Three programmable control inputs, S0, S1 and S2, can be used to control various aspects of operation including frequency selection changing the SSC parameters to lower EMI, PLL bypass, power down, and choosing between low level or 3-state for output-disable function.

The CDCE949-Q1 operates in a 1.8V environment. The CDCE949-Q1 is characterized for operation from –40°C to 85°C.

7.2 Functional Block Diagram

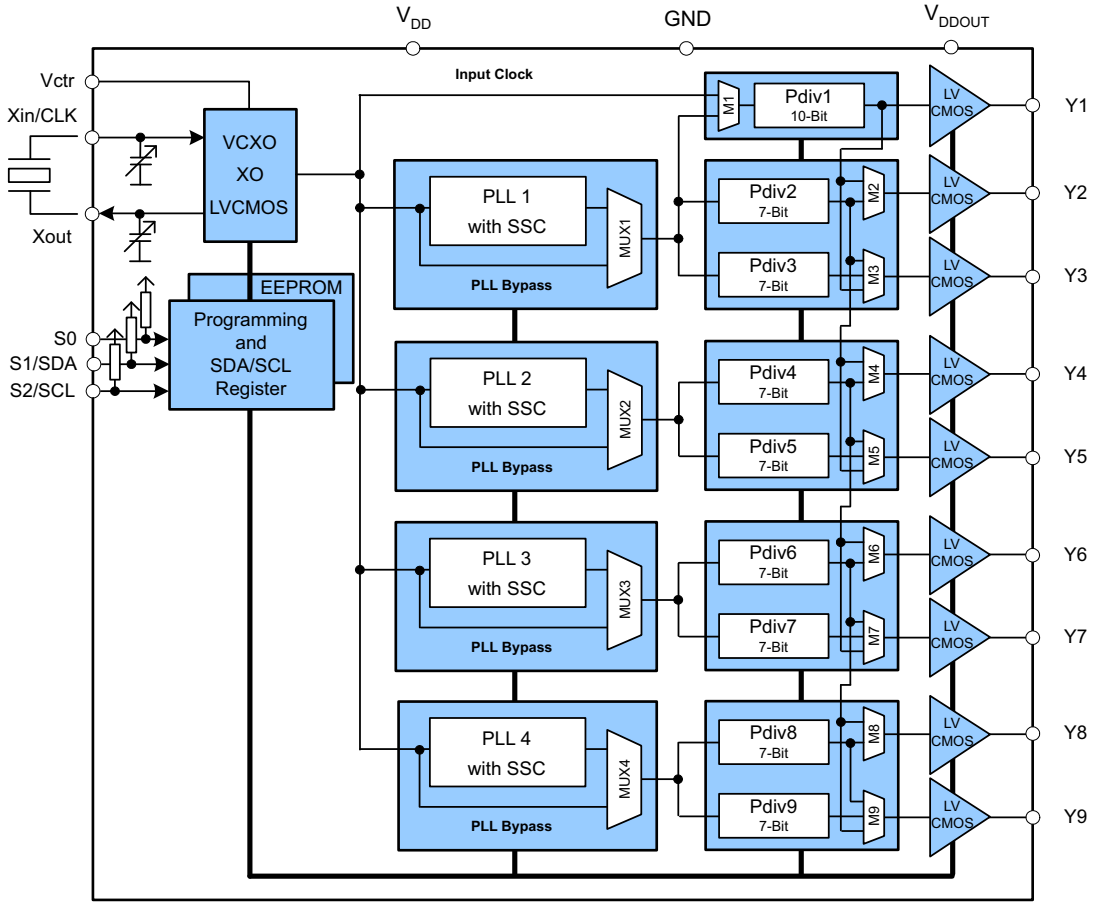


Figure 7-1. Functional Block Diagram

7.3 Feature Description

7.3.1 Control Terminal Configuration

The CDCE949 has three user-definable control terminals (S0, S1 and S2) which allow external control of device settings. The terminals can be programmed to perform any of the following functions:

- Spread-Spectrum Clocking selection: Spread-type and spread-amount selection
- Frequency selection: Switching between any of two user-defined frequencies
- Output-State selection: Output configuration and power-down control

The user can predefine up to eight different control settings. Table 7-1 and Table 7-2 explain these settings.

Table 7-1. Control Terminal Definition

External Control-Bits	PLL1 Setting			PLL2 Setting			PLL3 Setting			PLL4 Setting			Y1 Setting
Control Function	PLL Frequency Selection	SSC Selection	Output Y2/Y3 Selection	PLL Frequency Selection	SSC Selection	Output Y4/Y5 Selection	PLL Frequency Selection	SSC Selection	Output Y6/Y7 Selection	PLL Frequency Selection	SSC Selection	Output Y8/Y9 Selection	Output Y1 and Power Down Selection

Table 7-2. PLLx Setting (Can be Selected for Each PLL Individual) (1)

SSC Selection (Center/Down)				
SSCx [3-bits]			Center	Down
0	0	0	0% (off)	0% (off)
0	0	1	±0.25%	–0.25%

Table 7-2. PLLx Setting (Can be Selected for Each PLL Individual) (1) (continued)

SSC Selection (Center/Down)				
SSCx [3-bits]			Center	Down
0	1	0	±0.5%	–0.5%
0	1	1	±0.75%	–0.75%
1	0	0	±1.0%	–1.0%
1	0	1	±1.25%	–1.25%
1	1	0	±1.5%	–1.5%
1	1	1	±2.0%	–2.0%
FREQUENCY SELECTION(2)				
FSx			FUNCTION	
0			Frequency0	
1			Frequency1	
OUTPUT SELECTION(3) (Y2 ... Y9)				
YxYx			FUNCTION	
0			State0	
1			State1	

(1) Center/Down-Spread, Frequency0/1 and State0/1 are user-definable in PLLx Configuration Register;
(2) Frequency0 and Frequency1 can be any frequency within the specified f_{VCO} range.
(3) State0/1 selection is valid for both outputs of the corresponding PLL module and can be power down, 3-state, low or active

Table 7-3. Y1 Setting (1)

Y1 SELECTION	
Y1	FUNCTION
0	State 0
1	State 1

(1) State0 and State1 are user-definable in Generic Configuration Register and can be power down, 3-state, low or active.

The S1/SDA and S2/SCL pins of the CDCE949 are dual-function pins. In the default configuration the pins are defined as SDA/SCL for the serial interface. The pins can be programmed as control pins (S1/S2) by setting the appropriate bits in the EEPROM. Note that changes to the Control register (Bit [6] of Byte 02) have no effect until the changes are written into the EEPROM.

Once the pins are set as control pins, the serial programming interface is no longer available. However, if V_{DDOUT} is forced to GND, the two control-pins, S1 and S2, temporarily act as serial programming pins (SDA/SCL).

S0 is **not** a multi-use pin, this pin is a control pin only.

7.3.2 Default Device Setting

The internal EEPROM of CDCE949-Q1 is preconfigured as shown in Figure 7-2. The input frequency is passed through to the output as a default. The default setting appears after power is supplied or after a power-down/up sequence until the EEPROM of the device is reprogrammed by the user to a different application configuration. A new register setting is programmed using the serial SDA/SCL Interface.

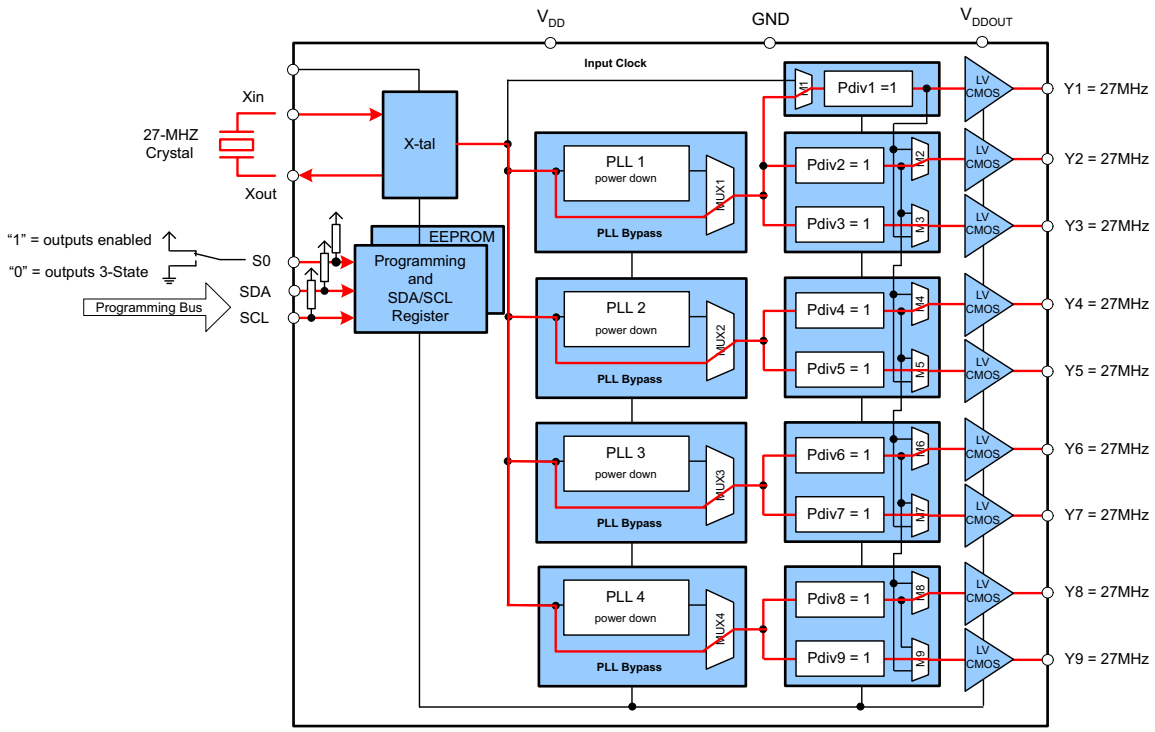


Figure 7-2. Default Configuration

Table 7-4 shows the default setting for the Control Terminal Register (external control pins). In normal operation, all 8 register settings are available, but in the default configuration only the first two settings (0 and 1) can be selected with S0, as S1 and S2 are configured as programming pins in default mode.

Table 7-4. Factory Default Setting for Control Terminal Register

EXTERNAL CONTROL-PINS(1)			Y1	PLL1 SETTING			PLL2 SETTING			PLL3 SETTING			PLL4 SETTING		
			Output Select	Freq. Select	SSC Sel.	Output Select	Freq. Select	SSC Sel.	Output Select	Freq. Select	SSC Sel.	Output Select	Freq. Select	SSC Sel.	Output Select
S2	S1	S0	Y1	FS1	SSC1	Y2Y3	FS2	SSC2	Y4Y5	FS3	SSC3	Y6Y7	FS4	SSC4	Y8Y9
SCL (I^2C)	SDA (I^2C)	0	3-State	f_{VCO1_0}	off	3-State	f_{VCO2_0}	off	3-State	f_{VCO3_0}	off	3-State	f_{VCO4_0}	off	3-State
SCL (I^2C)	SDA (I^2C)	1	enabled	f_{VCO1_0}	off	enabled	f_{VCO2_0}	off	enabled	f_{VCO3_0}	off	enabled	f_{VCO4_0}	off	enabled

(1) In default mode or when programmed respectively, S1 and S2 act as a serial programming interface, SDA/SCL. In this mode, the pins have no control-pin function, but are internally interpreted as if S1=0 and S2=0. S0, however, is a control-pin which in the default mode switches all outputs ON or OFF (as pre-defined above).

7.3.3 SDA/SCL Serial Interface

The CDCE949 operates as a target device on the 2-wire serial SDA/SCL bus, compatible with the popular SMBus or I2C™ specification. The device operates in the standard-mode transfer (up to 100kbps) and fast-mode transfer (up to 400kbps) and supports 7-bit addressing.

The S1/SDA and S2/SCL pins of the CDC9xx are dual-function pins. In the default configuration the pins are used as SDA/SCL serial programming interface. The pins can be reprogrammed as general purpose control pins, S1 and S2, by changing the corresponding EEPROM setting, Byte 02, Bit [6].

7.3.4 Data Protocol

The device supports *Byte Write and Byte Read* and *Block Write and Block Read* operations.

For *Byte Write/Read* operations, the system controller can individually access addressed bytes.

For *Block Write/Read* operations, the bytes are accessed in sequential order from lowest to highest byte (with most significant bit first) with the ability to stop after any complete byte has been transferred. The number of

bytes read out is defined by the Byte Count field in the Generic Configuration Register. During a Block Read instruction, the entire number of bytes defined in Byte Count must be read out to correctly finish the read cycle.

When a byte is sent to the device, the byte is written into the internal register and immediately takes effect. This applies to each transferred byte, whether in a *Byte Write* or a *Block Write* sequence.

If the EEPROM write cycle is initiated, the internal registers are written into the EEPROM. Data can be read out during the programming sequence (Byte Read or Block Read). The programming status can be monitored by EEPIP, Byte 01–Bit [6]. Before beginning EEPROM programming, pull CLKIN LOW. CLKIN must be held LOW for the duration of EEPROM programming. After initiating EEPROM programming with EEWRITE, Byte 06–Bit [0], do not write to the device registers until EEPIP is read back as a 0.

The offset of the indexed byte is encoded in the command code, as described in Table 7-6.

Table 7-5. Target Receiver Address (7 bits)

Device	A6	A5	A4	A3	A2	A1(1)	A0(1)	R/ $\overline{W}$
CDCE913/CDCEL913	1	1	0	0	1	0	1	1/0
CDCE925/CDCEL925	1	1	0	0	1	0	0	1/0
CDCE937/CDCEL937	1	1	0	1	1	0	1	1/0
CDCE949	**1**	**1**	**0**	**1**	**1**	**0**	**0**	**1/0**

(1) Address bits A0 and A1 are programmable via the SDA/SCL bus (Byte 01, Bit [1:0]). This allows addressing up to 4 devices connected to the same SDA/SCL bus. The least significant bit of the address byte designates a write or read operation.

Table 7-6. Command Code Definition

BIT	DESCRIPTION
7	0 = *Block Read* or *Block Write* operation 1 = *Byte Read* or *Byte Write* operation
(6:0)	Byte Offset for *Byte Read*, *Block Read*, *Byte Write* and *Block Write* operation.

7.3.5 PLL Multiplier/Divider Definition

At a given input frequency (f_{IN}), the output frequency (f_{OUT}) of the CDCE949 can be calculated by:

$$f_{OUT} = \frac{f_{IN}}{Pdiv} \times \frac{N}{M}$$

where

M (1 to 511) and N (1 to 4095) are the multiplier/divider values of the PLL;
Pdiv (1 to 127) is the output divider.

The target VCO frequency (f_{VCO}) of each PLL can be calculated:

$$f_{VCO} = f_{IN} \times \frac{N}{M}$$

The PLL operates as fractional divider and needs following multiplier/divider settings

N

$$P = 4 - \text{int}(\log_2 \frac{N}{M}) \text{ \{if P < 0 then P = 0\}}$$

$$Q = \text{int}(\frac{N'}{M})$$

$$R = N' - M \times Q$$

Where:

$N' = N \times 2^P$;

$N \geq M$;

$80MHz < f_{VCO} > 230MHz$.

Example 1: for f_{IN} = 27MHz; M = 1; N = 4; Pdiv = 2;
→ f_{OUT} = 54MHz;
→ f_{VCO} = 108MHz;
→ P = 4 – int($\log_2$4) = 4 –2 = 2;
→ N' = 4 × 2^2 = 16;
→ Q = int(16) = 16;
→ R = 16 – 16 = 0;

Example 2: for f_{IN} = 27MHz; M = 2; N = 11; Pdiv = 2;
→ f_{OUT} = 75.25MHz;
→ f_{VCO} = 148.50MHz;
→ P = 4 – int($\log_2$5.5) = 4 – 2 = 2;
→ N' = 11 × 2^2 = 44;
→ Q = int(22) = 22;
→ R = 44 – 44 = 0;

The values for P, Q, R and N' are automatically calculated when using TI ClockPro™ Software.

7.4 Device Functional Modes

7.4.1 SDA/SCL Hardware Interface

Figure 7-3 shows how the CDCE949-Q1 clock synthesizer is connected to the SDA/SCL serial interface bus. Multiple devices can be connected to the bus but the speed can be reduced (400kHz is the maximum) if many devices are connected.

Note that the pullup resistor value (R_P) depends on the supply voltage, bus capacitance, and number of connected devices. The recommended pullup value is 4.7kΩ. The pullup value must meet the minimum sink current of 3mA at V_{OLmax} = 0.4V for the output stages (for more details see the SMBus or I^2C Bus specification).

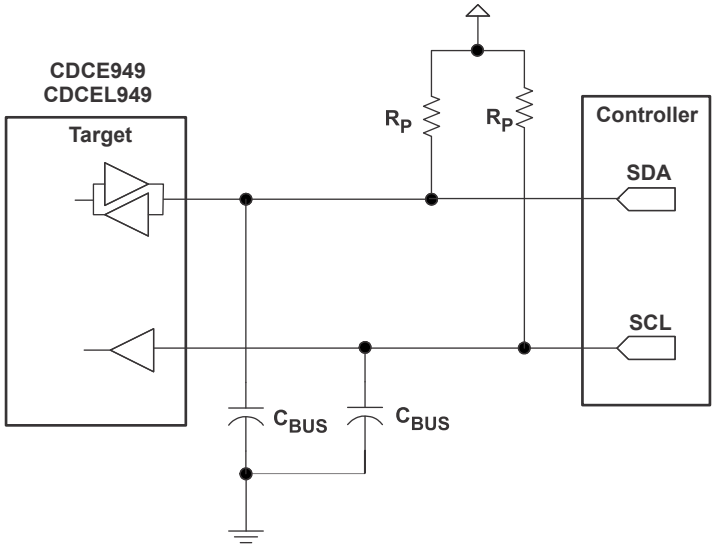


Figure 7-3. SDA/SCL Hardware Interface

7.5 Programming

7.5.1 Generic Programming Sequence

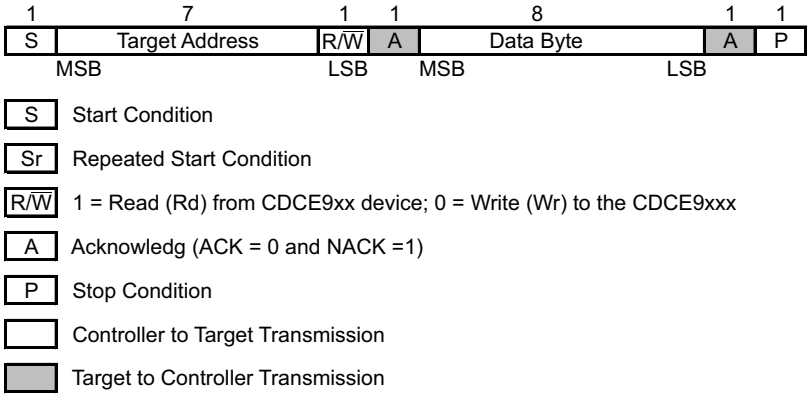


Figure 7-4. Generic Programming Sequence

7.5.2 Byte Write Programming Sequence

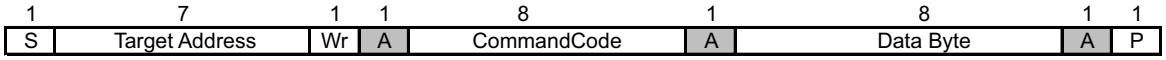


Figure 7-5. Byte Write Protocol

7.5.3 Byte Read Programming Sequence

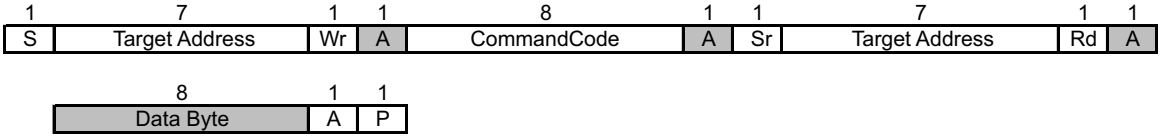
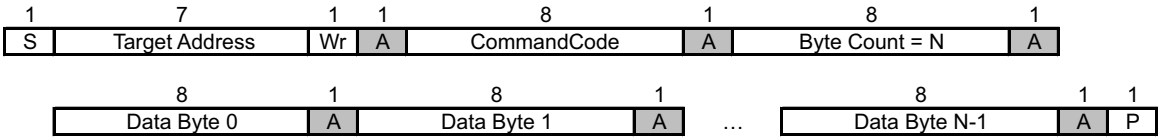


Figure 7-6. Byte Read Protocol

7.5.4 Block Write Programming Sequence



Data Byte 0 Bits [7:0] is reserved for Revision Code and Vendor Identification. The bits are used for internal test purpose and must not be overwritten.

Figure 7-7. Block Write Programming

7.5.5 Block Read Programming Sequence

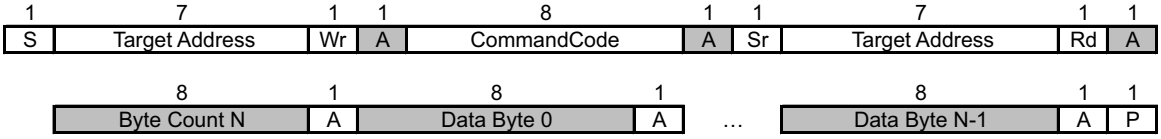


Figure 7-8. Block Read Protocol

8 Register Maps

8.1 SDA and SCL Registers

The clock input, control pins, PLLs and output stages are user configurable. The following tables and explanations describe the programmable functions of the CDCE949-Q1. All settings can be manually written to the device using the SDA/SCL bus, or are easily programmable by using the TI ClockPro software. TI ClockPro software allows the user to quickly make all settings and automatically calculates the values for optimized performance at lowest jitter.

Table 8-1. SDA/SCL Registers

ADDRESS OFFSET	REGISTER DESCRIPTION	TABLE
00h	Generic Configuration Register	Table 8-3
10h	PLL1 Configuration Register	Table 8-4
20h	PLL2 Configuration Register	Table 8-5
30h	PLL3 Configuration Register	Table 8-6
40h	PLL4 Configuration Register	Table 8-7

8.2 Configuration Registers

The gray-highlighted Bits described in the Configuration Registers tables on the following pages, belong to the Control Terminal Register. The user can predefine up to eight different control settings. These settings can then be selected by the external control pins, S0, S1, and S2 (See the *Control Terminal Configuration* section).

Table 8-2. Configuration Register, External Control Terminals

EXTERNAL CONTROL PINS			Y1	PLL1 SETTING			PLL2 SETTING			PLL3 SETTING			PLL4 SETTING		
			Output Select	Freq. Select	SSC Select	Output Select	Freq. Select	SSC Select	Output Select	Freq. Select	SSC Select	Output Select	Freq. Select	SSC Select	Output Select
S2	S1	S0	Y1	FS1	SSC1	Y2Y3	FS2	SSC2	Y4Y5	FS3	SSC3	Y6Y7	FS4	SSC4	Y8Y9
0	0	0	Y1_0	FS1_0	SSC1_0	Y2Y3_0	FS2_0	SSC2_0	Y4Y5_0	FS3_0	SSC3_0	Y6Y7_0	FS4_0	SSC4_0	Y8Y9_0
0	0	1	Y1_1	FS1_1	SSC1_1	Y2Y3_1	FS2_1	SSC2_1	Y4Y5_1	FS3_1	SSC3_1	Y6Y7_1	FS4_1	SSC4_1	Y8Y9_1
0	1	0	Y1_2	FS1_2	SSC1_2	Y2Y3_2	FS2_2	SSC2_2	Y4Y5_2	FS3_2	SSC3_2	Y6Y7_2	FS4_2	SSC4_2	Y8Y9_2
0	1	1	Y1_3	FS1_3	SSC1_3	Y2Y3_3	FS2_3	SSC2_3	Y4Y5_3	FS3_3	SSC3_3	Y6Y7_3	FS4_3	SSC4_3	Y8Y9_3
1	0	0	Y1_4	FS1_4	SSC1_4	Y2Y3_4	FS2_4	SSC2_4	Y4Y5_4	FS3_4	SSC3_4	Y6Y7_4	FS4_4	SSC4_4	Y8Y9_4
1	0	1	Y1_5	FS1_5	SSC1_5	Y2Y3_5	FS2_5	SSC2_5	Y4Y5_5	FS3_5	SSC3_5	Y6Y7_5	FS4_5	SSC4_5	Y8Y9_5
1	1	0	Y1_6	FS1_6	SSC1_6	Y2Y3_6	FS2_6	SSC2_6	Y4Y5_6	FS3_6	SSC3_6	Y6Y7_6	FS4_6	SSC4_6	Y8Y9_6
1	1	1	Y1_7	FS1_7	SSC1_7	Y2Y3_7	FS2_7	SSC2_7	Y4Y5_7	FS3_7	SSC3_7	Y6Y7_7	FS4_7	SSC4_7	Y8Y9_7
Addr. Offset(1)			04h	13h	10h-12h	15h	23h	20h-22h	25h	33h	30h-32h	35h	43h	40h-42h	45h

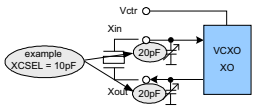
(1) Address Offset refers to the byte address in the Configuration Register on following pages.

8.2.1 Generic Configuration Register

Table 8-3. Generic Configuration Register

OFFSET(1)	Bit(2)	Acronym	Default(3)	DESCRIPTION
00h	7	E_EL	xb	Device Identification (read only): 1 is CDCE949 (3.3V), 0 is CDCEL949 (1.8V)
	6:4	RID	Xb	Revision Identification Number (read only)
	3:0	VID	1h	Vendor Identification Number (read only)

Table 8-3. Generic Configuration Register (continued)

OFFSET[1]	Bit[2]	Acronym	Default[3]	DESCRIPTION
01h	7	–	0b	Reserved - always write 0
	6	EEPIP	0b	EEPROM Programming Status[4]: (read only) 0 – EEPROM programming is completed 1 – EEPROM is in programming mode
	5	EELOCK	0b	Permanently Lock EEPROM Data[5]: 0 – EEPROM is not locked 1 – EEPROM is permanently locked
	4	PWDN	0b	Device power down (overwrites S0/S1/S2 setting; configuration register settings are unchanged) Note: PWDN cannot be set to 1 in the EEPROM. 0 – device active (all PLLs and all outputs are enabled) 1 – device power down (all PLLs in power down and all outputs in 3-State)
	3:2	INCLK	00b	Input clock selection: 00 – X-tal 01 – VCXO 10 – LVCMOS 11 – reserved
	1:0	I2C_ADR	00b	Programmable Address Bits A0 and A1 of the Target Receiver Address
02h	7	M1	1b	Clock source selection for output Y1: 0 – input clock 1 – PLL1 clock
	6	SPICON	0b	Operation mode selection for pin 22/23[6] 0 – serial programming interface SDA (pin 23) and SCL (pin 22) 1 – control pins S1 (pin 23) and S2 (pin 22)
	5:4	Y1_ST1	11b	Y1-State0/1 Definition (applies to Y1_ST1 and Y1_ST0) 00 – device power down (all PLLs in power down and all outputs in 3-state) 01 – Y1 disabled to 3-state 10 – Y1 disabled to low 11 – Y1 enabled (normal operation)
	3:2	Y1_ST0	01b	
	1:0	Pdiv1 [9:8]	001h	10-Bit Y1-Output-Divider Pdiv1: 0 – divider reset and stand-by 1-to-1023 – divider value
03h	7:0	Pdiv1 [7:0]		
04h	7	Y1_7	0b	Y1_x State Selection[7] 0 – State0 (predefined by Y1-State0 Definition [Y1_ST0]) 1 – State1 (predefined by Y1-State1 Definition [Y1_ST1])
	6	Y1_6	0b	
	5	Y1_5	0b	
	4	Y1_4	0b	
	3	Y1_3	0b	
	2	Y1_2	0b	
	1	Y1_1	1b	
	0	Y1_0	0b	
05h	7:3	XCSEL	0Ah	Crystal load capacitor selection[8]: 00h → 0pF 01h → 1pF 02h → 2pF 14h-to-1Fh → 20pF 
	2:0	—	0b	Reserved - do not write others than 0
06h	7:1	BCOUNT	50h	7-Bit Byte Count (Defines the number of Bytes which is sent from this device at the next Block Read transfer; all bytes must be read out to correctly finish the read cycle.)
	0	EEWRITE	0b	Initiate EEPROM Write Cycle[4] [9] 0 – no EEPROM write cycle 1 – start EEPROM write cycle (internal configuration register is saved to the EEPROM)
07h-0Fh	—	—	0h	Reserved – do not write others than 0

(1) Writing data beyond '50h' can adversely affect device function.
(2) All data is transferred MSB-first.
(3) Unless custom setting is used.
(4) During EEPROM programming, no data is allowed to be sent to the device using the SDA/SCL bus until the programming sequence is completed. Data, however, can be read during the programming sequence (Byte Read or Block Read).
(5) If this bit is set high in the EEPROM, the actual data in the EEPROM is permanently locked, and no further programming is possible. Data, however can still be written using SDA/SCL bus to the internal register to change device function on the fly. But new data can no longer be saved to the EEPROM. EELOCK is effective only if written into the EEPROM
(6) Selection of *control-pins* is effective only if written into the EEPROM. Once written into the EEPROM, the serial programming pins are no longer available. However, if V_{DDOUT} is forced to GND, the two control-pins, S1 and S2, temporarily act as serial programming pins (SDA/SCL), and the two target receiver address bits are reset to A0 = 0 and A1 = 0.
(7) These are the bits of the Control Terminal Register. The user can pre-define up to eight different control settings. These settings can then be selected by the external control pins, S0, S1, and S2.

(8) The internal load capacitor (C_1, C_2) must be used to achieve the best clock performance. External capacitors are used only to do a fine adjustment of C_L by few pF. The value of C_L can be programmed with a resolution of 1pF for a total crystal load range of 0pF to 20pF. For C_L > 20pF use additional external capacitors. Also, the device input capacitance must be considered; this adds 1.5pF (6pF//2pF) to the selected C_L. For more information about VCXO configuration and crystal recommendations, see application note SCAA085

(9) **NOTE: The EEPROM WRITE bit must be sent last.** This verifies that the content of all internal registers are written into the EEPROM. The EEWRITE cycle is initiated by the rising edge of the EEWRITE-Bit. A static level high does not trigger an EEPROM WRITE cycle. The EEWRITE-Bit must be reset low after the programming is completed. The programming status can be monitored by readout EEPIP. If EELOCK is set high, no EEPROM programming is possible.

8.2.2 PLL1 Configuration Register

Table 8-4. PLL1 Configuration Register

OFFSET(1)	Bit(2)	Acronym	Default(3)	DESCRIPTION
10h	7:5	SSC1_7 [2:0]	000b	SSC1: PLL1 SSC Selection (Modulation Amount)(4) **Down** / **Center** 000 (off) / 000 (off) 001 – 0.25% / 001 ± 0.25% 010 – 0.5% / 010 ± 0.5% 011 – 0.75% / 011 ± 0.75% 100 – 1.0% / 100 ± 1.0% 101 – 1.25% / 101 ± 1.25% 110 – 1.5% / 110 ± 1.5% 111 – 2.0% / 111 ± 2.0%
	4:2	SSC1_6 [2:0]	000b	
	1:0	SSC1_5 [2:1]	000b	
11h	7	SSC1_5 [0]		
	6:4	SSC1_4 [2:0]	000b	
	3:1	SSC1_3 [2:0]	000b	
	0	SSC1_2 [2]	000b	
12h	7:6	SSC1_2 [1:0]		
	5:3	SSC1_1 [2:0]	000b	
	2:0	SSC1_0 [2:0]	000b	
13h	7	FS1_7	0b	FS1_x: PLL1 Frequency Selection(4) 0 – f_{VCO1_0} (predefined by PLL1_0 – Multiplier/Divider value) 1 – f_{VCO1_1} (predefined by PLL1_1 – Multiplier/Divider value)
	6	FS1_6	0b	
	5	FS1_5	0b	
	4	FS1_4	0b	
	3	FS1_3	0b	
	2	FS1_2	0b	
	1	FS1_1	0b	
	0	FS1_0	0b	
14h	7	MUX1	1b	PLL1 Multiplexer: 0 – PLL1 1 – PLL1 Bypass (PLL1 is in power down)
	6	M2	1b	Output Y2 Multiplexer: 0 – Pdiv1 1 – Pdiv2
	5:4	M3	10b	Output Y3 Multiplexer: 00 – Pdiv1-Divider 01 – Pdiv2-Divider 10 – Pdiv3-Divider 11 – reserved
	3:2	Y2Y3_ST1	11b	Y2, Y3-State0/1definition: 00 – Y2/Y3 disabled to 3-State (PLL1 is in power down) 01 – Y2/Y3 disabled to 3-State (PLL1 on) 10–Y2/Y3 disabled to low (PLL1 on) 11 – Y2/Y3 enabled (normal operation, PLL1 on)
	1:0	Y2Y3_ST0	01b	
15h	7	Y2Y3_7	0b	Y2Y3_x Output State Selection(4) 0 – state0 (predefined by Y2Y3_ST0) 1 – state1 (predefined by Y2Y3_ST1)
	6	Y2Y3_6	0b	
	5	Y2Y3_5	0b	
	4	Y2Y3_4	0b	
	3	Y2Y3_3	0b	
	2	Y2Y3_2	0b	
	1	Y2Y3_1	1b	
	0	Y2Y3_0	0b	
16h	7	SSC1DC	0b	PLL1 SSC down/center selection: 0 – down 1 – center
	6:0	Pdiv2	01h	7-Bit Y2-Output-Divider Pdiv2: 0 – reset and stand-by 1-to-127 – divider value
17h	7	—	0b	Reserved – do not write others than 0
	6:0	Pdiv3	01h	7-Bit Y3-Output-Divider Pdiv3: 0 – reset and stand-by 1-to-127 – divider value

Table 8-4. PLL1 Configuration Register (continued)

OFFSET[1]	Bit[2]	Acronym	Default[3]	DESCRIPTION
18h	7:0	PLL1_0N [11:4	004h	PLL1_0: 30-Bit Multiplier/Divider value for frequency f_{VCO1_0} (for more information see *PLL Multiplier/Divider Definition*)
19h	7:4	PLL1_0N [3:0]		
	3:0	PLL1_0R [8:5]	000h	
1Ah	7:3	PLL1_0R[4:0]		
	2:0	PLL1_0Q [5:3]	10h	
1Bh	7:5	PLL1_0Q [2:0]		
	4:2	PLL1_0P [2:0]	010b	
	1:0	VCO1_0_RANGE	00b	f_{VCO1_0} range selection: 00 – f_{VCO1_0} < 125MHz; 01 – 125MHz ≤ f_{VCO1_0} < 150MHz; 10 – 150MHz ≤ f_{VCO1_0} < 175MHz; 11 – f_{VCO1_0} ≥ 175MHz
1Ch	7:0	PLL1_1N [11:4]	004h	PLL1_1: 30-Bit Multiplier/Divider value for frequency f_{VCO1_1} (for more information see paragraph *PLL Multiplier/Divider Definition*)
1Dh	7:4	PLL1_1N [3:0]		
	3:0	PLL1_1R [8:5]	000h	
1Eh	7:3	PLL1_1R[4:0]		
	2:0	PLL1_1Q [5:3]	10h	
1Fh	7:5	PLL1_1Q [2:0]		
	4:2	PLL1_1P [2:0]	010b	
	1:0	VCO1_1_RANGE	00b	f_{VCO1_1} range selection: 00 – f_{VCO1_1} < 125MHz; 01 – 125MHz ≤ f_{VCO1_1} < 150MHz; 10 – 150MHz ≤ f_{VCO1_1} < 175MHz; 11 – f_{VCO1_1} ≥ 175MHz

(1) Writing data beyond 50h can adversely affect device function.
(2) All data is transferred MSB-first.
(3) Unless a custom setting is used
(4) The user can pre-define up to eight different control settings. In normal device operation, these settings can be selected by the external control pins, S0, S1, and S2.

8.2.3 PLL2 Configuration Register

Table 8-5. PLL2 Configuration Register

OFFSET[1]	Bit[2]	Acronym	Default[3]	DESCRIPTION
20h	7:5	SSC2_7 [2:0]	000b	SSC2: PLL2 SSC Selection (Modulation Amount)[4] **Down** / **Center** 000 (off) / 000 (off) 001 – 0.25% / 001 ± 0.25% 010 – 0.5% / 010 ± 0.5% 011 – 0.75% / 011 ± 0.75% 100 – 1.0% / 100 ± 1.0% 101 – 1.25% / 101 ± 1.25% 110 – 1.5% / 110 ± 1.5% 111 – 2.0% / 111 ± 2.0%
	4:2	SSC2_6 [2:0]	000b	
	1:0	SSC2_5 [2:1]	000b	
21h	7	SSC2_5 [0]		
	6:4	SSC2_4 [2:0]	000b	
	3:1	SSC2_3 [2:0]	000b	
	0	SSC2_2 [2]	000b	
22h	7:6	SSC2_2 [1:0]		
	5:3	SSC2_1 [2:0]	000b	
	2:0	SSC2_0 [2:0]	000b	
23h	7	FS2_7	0b	FS2_x: PLL2 Frequency Selection[4] 0 – f_{VCO2_0} (predefined by PLL2_0 – Multiplier/Divider value) 1 – f_{VCO2_1} (predefined by PLL2_1 – Multiplier/Divider value)
	6	FS2_6	0b	
	5	FS2_5	0b	
	4	FS2_4	0b	
	3	FS2_3	0b	
	2	FS2_2	0b	
	1	FS2_1	0b	
	0	FS2_0	0b	

Table 8-5. PLL2 Configuration Register (continued)

OFFSET[1]	Bit[2]	Acronym	Default[3]	DESCRIPTION
24h	7	MUX2	1b	PLL2 Multiplexer: 0 – PLL2 1 – PLL2 Bypass (PLL2 is in power down)
	6	M4	1b	Output Y4 Multiplexer: 0 – Pdiv2 1 – Pdiv4
	5:4	M5	10b	Output Y5 Multiplexer: 00 – Pdiv2-Divider 01 – Pdiv4-Divider 10 – Pdiv5-Divider 11 – reserved
	3:2	Y4Y5_ST1	11b	Y4, Y5-State0/1definition: 00 – Y4/Y5 disabled to 3-State (PLL2 is in power down) 01 – Y4/Y5 disabled to 3-State (PLL2 on) 10–Y4/Y5 disabled to low (PLL2 on) 11 – Y4/Y5 enabled (normal operation, PLL2 on)
	1:0	Y4Y5_ST0	01b	
25h	7	Y4Y5_7	0b	Y4Y5_x Output State Selection[4] 0 – state0 (predefined by Y4Y5_ST0) 1 – state1 (predefined by Y4Y5_ST1)
	6	Y4Y5_6	0b	
	5	Y4Y5_5	0b	
	4	Y4Y5_4	0b	
	3	Y4Y5_3	0b	
	2	Y4Y5_2	0b	
	1	Y4Y5_1	1b	
	0	Y4Y5_0	0b	
26h	7	SSC2DC	0b	PLL2 SSC down/center selection: 0 – down 1 – center
	6:0	Pdiv4	01h	7-Bit Y4-Output-Divider Pdiv4: 0 – reset and stand-by 1-to-127 – divider value
27h	7	—	0b	Reserved – do not write others than 0
	6:0	Pdiv5	01h	7-Bit Y5-Output-Divider Pdiv5: 0 – reset and stand-by 1-to-127 – divider value
28h	7:0	PLL2_0N [11:4	004h	PLL2_0: 30-Bit Multiplier/Divider value for frequency f_{VCO2_0} (for more information see paragraph *PLL Multiplier/Divider Definition*)
29h	7:4	PLL2_0N [3:0]		
	3:0	PLL2_0R [8:5]	000h	
2Ah	7:3	PLL2_0R[4:0]		
	2:0	PLL2_0Q [5:3]	10h	
2Bh	7:5	PLL2_0Q [2:0]		
	4:2	PLL2_0P [2:0]	010b	
	1:0	VCO2_0_RANGE	00b	f_{VCO2_0} range selection: 00 – f_{VCO2_0} < 125MHz 01 – 125MHz ≤ f_{VCO2_0} < 150MHz 10 – 150MHz ≤ f_{VCO2_0} < 175MHz 11 – f_{VCO2_0} ≥ 175MHz
2Ch	7:0	PLL2_1N [11:4]	004h	PLL2_1: 30-Bit Multiplier/Divider value for frequency f_{VCO1_1} (for more information see paragraph *PLL Multiplier/Divider Definition*)
2Dh	7:4	PLL2_1N [3:0]		
	3:0	PLL2_1R [8:5]	000h	
2Eh	7:3	PLL2_1R[4:0]		
	2:0	PLL2_1Q [5:3]	10h	
2Fh	7:5	PLL2_1Q [2:0]		
	4:2	PLL2_1P [2:0]	010b	
	1:0	VCO2_1_RANGE	00b	f_{VCO2_1} range selection: 00 – f_{VCO2_1} < 125MHz 01 – 125MHz ≤ f_{VCO2_1} < 150MHz 10 – 150MHz ≤ f_{VCO2_1} < 175MHz 11 – f_{VCO2_1} ≥ 175MHz

(1) Writing data beyond 50h can adversely affect device function.
(2) All data is transferred MSB-first.
(3) Unless a custom setting is used
(4) The user can pre-define up to eight different control settings. In normal device operation, these settings can be selected by the external control pins, S0, S1, and S2.

8.2.4 PLL3 Configuration Register

Table 8-6. PLL3 Configuration Register

OFFSET[1]	Bit[2]	Acronym	Default[3]	DESCRIPTION
30h	7:5	SSC3_7 [2:0]	000b	SSC3: PLL3 SSC Selection (Modulation Amount)[4] **Down** / **Center** 000 (off) / 000 (off) 001 – 0.25% / 001 ± 0.25% 010 – 0.5% / 010 ± 0.5% 011 – 0.75% / 011 ± 0.75% 100 – 1.0% / 100 ± 1.0% 101 – 1.25% / 101 ± 1.25% 110 – 1.5% / 110 ± 1.5% 111 – 2.0% / 111 ± 2.0%
	4:2	SSC3_6 [2:0]	000b	
	1:0	SSC3_5 [2:1]	000b	
31h	7	SSC3_5 [0]		
	6:4	SSC3_4 [2:0]	000b	
	3:1	SSC3_3 [2:0]	000b	
	0	SSC3_2 [2]	000b	
32h	7:6	SSC3_2 [1:0]		
	5:3	SSC3_1 [2:0]	000b	
	2:0	SSC3_0 [2:0]	000b	
33h	7	FS3_7	0b	FS3_x: PLL3 Frequency Selection[4] 0 – f_{VCO3_0} (predefined by PLL3_0 – Multiplier/Divider value) 1 – f_{VCO3_1} (predefined by PLL3_1 – Multiplier/Divider value)
	6	FS3_6	0b	
	5	FS3_5	0b	
	4	FS3_4	0b	
	3	FS3_3	0b	
	2	FS3_2	0b	
	1	FS3_1	0b	
	0	FS3_0	0b	
34h	7	MUX3	1b	PLL3 Multiplexer: 0 – PLL3 1 – PLL3 Bypass (PLL3 is in power down)
	6	M6	1b	Output Y6 Multiplexer: 0 – Pdiv4 1 – Pdiv6
	5:4	M7	10b	Output Y7 Multiplexer: 00 – Pdiv4-Divider 01 – Pdiv6-Divider 10 – Pdiv7-Divider 11 – reserved
	3:2	Y6Y7_ST1	11b	Y6, Y7-State0/1definition: 00 – Y6/Y7 disabled to 3-State (PLL3 is in power down) 01 – Y6/Y7 disabled to 3-State (PLL3 on) 10 –Y6/Y7 disabled to low (PLL3 on) 11 – Y6/Y7 enabled (normal operation, PLL3 on)
	1:0	Y6Y7_ST0	01b	
35h	7	Y6Y7_7	0b	Y6Y7_x Output State Selection[4] 0 – state0 (predefined by Y6Y7_ST0) 1 – state1 (predefined by Y6Y7_ST1)
	6	Y6Y7_6	0b	
	5	Y6Y7_5	0b	
	4	Y6Y7_4	0b	
	3	Y6Y7_3	0b	
	2	Y6Y7_2	0b	
	1	Y6Y7_1	1b	
	0	Y6Y7_0	0b	
36h	7	SSC3DC	0b	PLL3 SSC down/center selection: 0 – down 1 – center
	6:0	Pdiv6	01h	7-Bit Y6-Output-Divider Pdiv6: 0 – reset and stand-by 1-to-127 – divider value
37h	7	—	0b	Reserved – do not write others than 0
	6:0	Pdiv7	01h	7-Bit Y7-Output-Divider Pdiv7: 0 – reset and stand-by 1-to-127 – divider value

Table 8-6. PLL3 Configuration Register (continued)

OFFSET[1]	Bit[2]	Acronym	Default[3]	DESCRIPTION
38h	7:0	PLL3_0N [11:4	004h	PLL3_0: 30-Bit Multiplier/Divider value for frequency f_{VCO3_0} (for more information see paragraph *PLL Multiplier/Divider Definition*)
39h	7:4	PLL3_0N [3:0]		
	3:0	PLL3_0R [8:5]	000h	
3Ah	7:3	PLL3_0R[4:0]		
	2:0	PLL3_0Q [5:3]	10h	
3Bh	7:5	PLL3_0Q [2:0]		
	4:2	PLL3_0P [2:0]	010b	
	1:0	VCO3_0_RANGE	00b	f_{VCO3_0} range selection: 00 – f_{VCO3_0} < 125MHz 01 – 125MHz ≤ f_{VCO3_0} < 150MHz 10 – 150MHz ≤ f_{VCO3_0} < 175MHz 11 – f_{VCO3_0} ≥ 175MHz
3Ch	7:0	PLL3_1N [11:4]	004h	PLL3_1: 30-Bit Multiplier/Divider value for frequency f_{VCO3_1} (for more information see paragraph *PLL Multiplier/Divider Definition*)
3Dh	7:4	PLL3_1N [3:0]		
	3:0	PLL3_1R [8:5]	000h	
3Eh	7:3	PLL3_1R[4:0]		
	2:0	PLL3_1Q [5:3]	10h	
3Fh	7:5	PLL3_1Q [2:0]		
	4:2	PLL3_1P [2:0]	010b	
	1:0	VCO3_1_RANGE	00b	f_{VCO3_1} range selection: 00 – f_{VCO3_1} < 125MHz 01 – 125MHz ≤ f_{VCO3_1} < 150MHz 10 – 150MHz ≤ f_{VCO3_1} < 175MHz 11 – f_{VCO3_1} ≥ 175MHz

(1) Writing data beyond 50h can adversely affect device function.
(2) All data is transferred MSB-first.
(3) Unless a custom setting is used
(4) The user can pre-define up to eight different control settings. In normal device operation, these settings can be selected by the external control pins, S0, S1, and S2.

8.2.5 PLL4 Configuration Register

Table 8-7. PLL4 Configuration Register

OFFSET[1]	Bit[2]	Acronym	Default[3]	DESCRIPTION
40h	7:5	SSC4_7 [2:0]	000b	SSC4: PLL4 SSC Selection (Modulation Amount)[4] **Down** / **Center** 000 (off) / 000 (off) 001 – 0.25% / 001 ± 0.25% 010 – 0.5% / 010 ± 0.5% 011 – 0.75% / 011 ± 0.75% 100 – 1.0% / 100 ± 1.0% 101 – 1.25% / 101 ± 1.25% 110 – 1.5% / 110 ± 1.5% 111 – 2.0% / 111 ± 2.0%
	4:2	SSC4_6 [2:0]	000b	
	1:0	SSC4_5 [2:1]	000b	
41h	7	SSC4_5 [0]		
	6:4	SSC4_4 [2:0]	000b	
	3:1	SSC4_3 [2:0]	000b	
	0	SSC4_2 [2]	000b	
42h	7:6	SSC4_2 [1:0]		
	5:3	SSC4_1 [2:0]	000b	
	2:0	SSC4_0 [2:0]	000b	
43h	7	FS4_7	0b	FS4_x: PLL4 Frequency Selection[4] 0 – f_{VCO4_0} (predefined by PLL4_0 – Multiplier/Divider value) 1 – f_{VCO4_1} (predefined by PLL4_1 – Multiplier/Divider value)
	6	FS4_6	0b	
	5	FS4_5	0b	
	4	FS4_4	0b	
	3	FS4_3	0b	
	2	FS4_2	0b	
	1	FS4_1	0b	
	0	FS4_0	0b	

Table 8-7. PLL4 Configuration Register (continued)

OFFSET[1]	Bit[2]	Acronym	Default[3]	DESCRIPTION
44h	7	MUX4	1b	PLL4 Multiplexer: 0 – PLL4 1 – PLL4 Bypass (PLL4 is in power down)
	6	M8	1b	Output Y8 Multiplexer: 0 – Pdiv6 1 – Pdiv8
	5:4	M9	10b	Output Y9 Multiplexer: 00 – Pdiv6-Divider 01 – Pdiv8-Divider 10 – Pdiv9-Divider 11 – reserved
	3:2	Y8Y9_ST1	11b	Y8, Y9-State0/1definition: 00 – Y8/Y9 disabled to 3-State (PLL4 is in power down) 01 – Y8/Y9 disabled to 3-State (PLL4 on) 10 –Y8/Y9 disabled to low (PLL4 on) 11 – Y8/Y9 enabled (normal operation, PLL4 on)
	1:0	Y8Y9_ST0	01b	
45h	7	Y8Y9_7	0b	Y8Y9_x Output State Selection[4] 0 – state0 (predefined by Y8Y9_ST0) 1 – state1 (predefined by Y8Y9_ST1)
	6	Y8Y9_6	0b	
	5	Y8Y9_5	0b	
	4	Y8Y9_4	0b	
	3	Y8Y9_3	0b	
	2	Y8Y9_2	0b	
	1	Y8Y9_1	1b	
	0	Y8Y9_0	0b	
46h	7	SSC4DC	0b	PLL4 SSC down/center selection: 0 – down 1 – center
	6:0	Pdiv8	01h	7-Bit Y8-Output-Divider Pdiv8: 0 – reset and stand-by 1-to-127 – divider value
47h	7	—	0b	Reserved – do not write others than 0
	6:0	Pdiv9	01h	7-Bit Y9-Output-Divider Pdiv9: 0 – reset and stand-by 1-to-127 – divider value
48h	7:0	PLL4_0N [11:4	004h	PLL4_0: 30-Bit Multiplier/Divider value for frequency f_{VCO4_0} (for more information see paragraph *PLL Multiplier/Divider Definition*)
49h	7:4	PLL4_0N [3:0]		
	3:0	PLL4_0R [8:5]	000h	
4Ah	7:3	PLL4_0R[4:0]		
	2:0	PLL4_0Q [5:3]	10h	
4Bh	7:5	PLL4_0Q [2:0]		
	4:2	PLL4_0P [2:0]	010b	
	1:0	VCO4_0_RANGE	00b	f_{VCO4_0} range selection: 00 – f_{VCO4_0} < 125MHz 01 – 125MHz ≤ f_{VCO4_0} < 150MHz 10 – 150MHz ≤ f_{VCO4_0} < 175MHz 11 – f_{VCO4_0} ≥ 175MHz
4Ch	7:0	PLL4_1N [11:4]	004h	PLL4_1: 30-Bit Multiplier/Divider value for frequency f_{VCO4_1} (for more information see paragraph *PLL Multiplier/Divider Definition*)
4Dh	7:4	PLL4_1N [3:0]		
	3:0	PLL4_1R [8:5]	000h	
4Eh	7:3	PLL4_1R[4:0]		
	2:0	PLL4_1Q [5:3]	10h	
4Fh	7:5	PLL4_1Q [2:0]		
	4:2	PLL4_1P [2:0]	010b	
	1:0	VCO4_1_RANGE	00b	f_{VCO4_1} range selection: 00 – f_{VCO4_1} < 125MHz 01 – 125MHz ≤ f_{VCO4_1} < 150MHz 10 – 150MHz ≤ f_{VCO4_1} < 175MHz 11 – f_{VCO4_1} ≥ 175MHz

(1) Writing data beyond 50h can adversely affect device function.
(2) All data is transferred MSB-first.
(3) Unless a custom setting is used
(4) The user can pre-define up to eight different control settings. In normal device operation, these settings can be selected by the external control pins, S0, S1, and S2.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The CDCE949-Q1 device is an easy-to-use, high-performance, programmable CMOS clock synthesizer which can be used as a crystal buffer or clock synthesizer with a separate output supply pin. The CDCE949-Q1 device features an on-chip loop filter and spread-spectrum modulation. Programming can be done through the I2C interface, or previously saved settings can be loaded from on-chip EEPROM. The pins S0, S1, and S2 can be programmed as control pins to select various output settings.

9.2 Typical Application

Figure 9-1 shows the use of the CDCE949-Q1 devices for replacement of crystals and crystal oscillators on a Gigabit Ethernet Switch application.

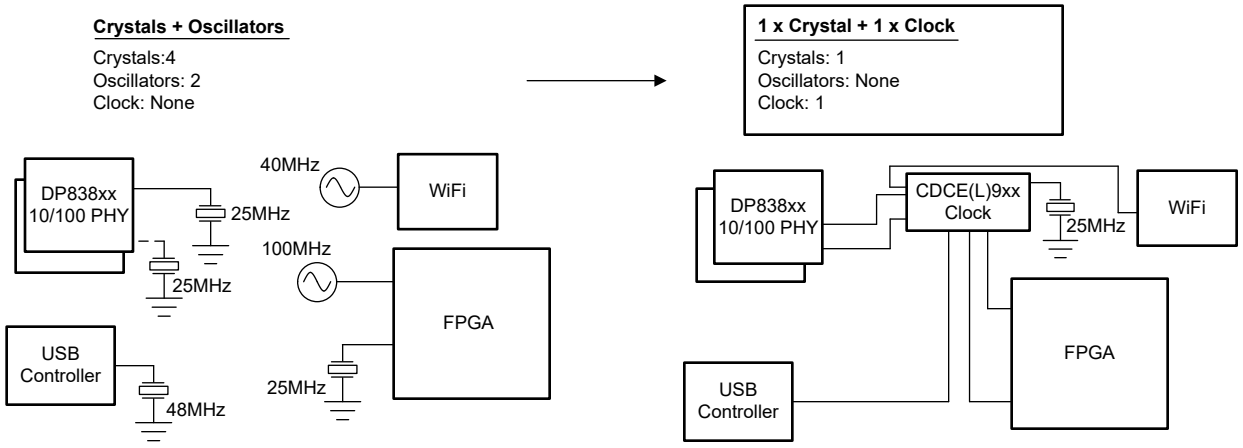


Figure 9-1. Crystal and Oscillator Replacement Example

9.2.1 Design Requirements

CDCE949-Q1 supports spread-spectrum clocking (SSC) with multiple control parameters:

- Modulation amount (%)
- Modulation frequency (>20kHz)
- Modulation shape (triangular)
- Center spread / down spread (± or -)

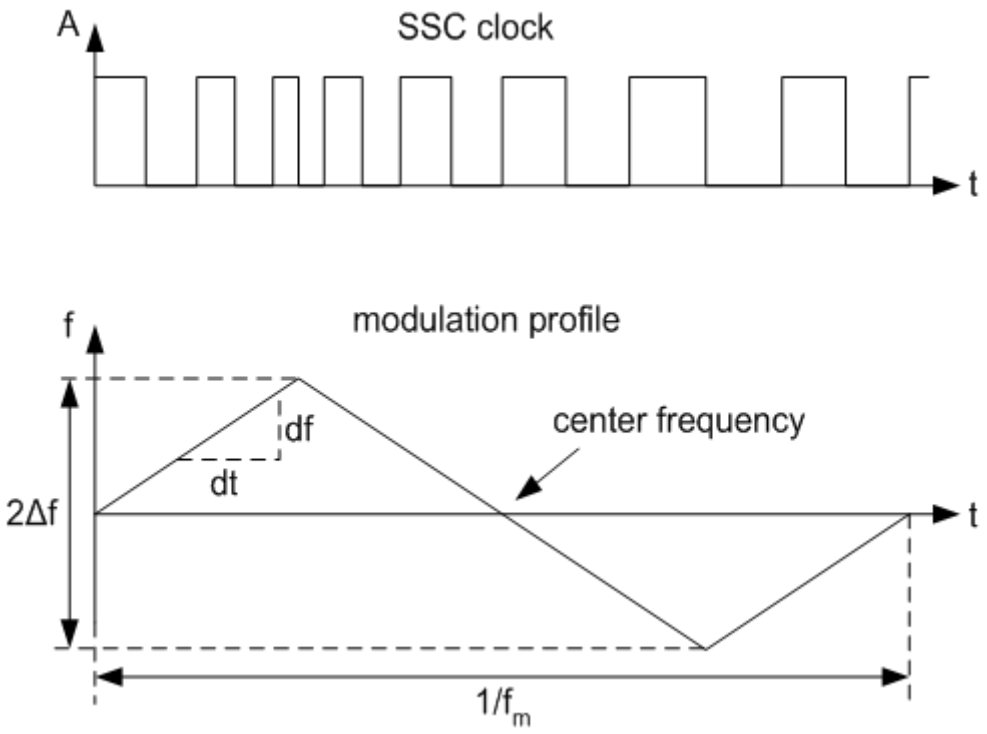


Figure 9-2. Modulation Frequency (fm) and Modulation Amount

9.2.2 Detailed Design Procedure

9.2.2.1 Spread Spectrum Clock (SSC)

Spread-spectrum modulation is a method to spread emitted energy over a larger bandwidth. In clocking, spread spectrum can reduce Electromagnetic Interference (EMI) by reducing the level of emission from clock distribution network.

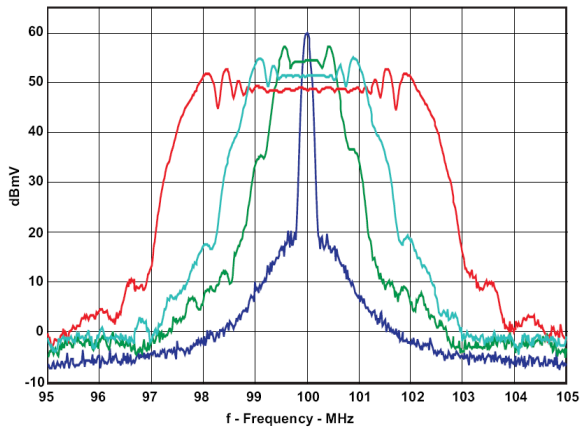


Figure 9-3. Comparison Between Typical Clock Power Spectrum and Spread-Spectrum Clock

9.2.2.2 PLL Frequency Planning

At a given input frequency (f_{IN}), the output frequency (f_{OUT}) of the CDCE949-Q1 are calculated with Equation 1.

$$f_{OUT} = \frac{f_{IN}}{Pdiv} \times \frac{N}{M} \quad (1)$$

where

- M (1 to 511) and N (1 to 4095) are the multiplier/divide values of the PLL
- Pdiv (1 to 127) is the output divider

The target VCO frequency (f_{VCO}) of each PLL is calculated with Equation 2.

$$f_{VCO} = f_{IN} \times \frac{N}{M} \quad (2)$$

The PLL internally operates as fractional divider and needs the following multiplier/divider settings:

- N
- P = 4 – int($\log_2 N/M$; if P < 0 then P = 0
- Q = int(N'/M)
- R = N′ – M × Q

where

$N' = N \times 2^P$

$N \geq M$;

$80MHz \leq f_{VCO} \leq 230MHz$

$16 \leq Q \leq 63$

$0 \leq P \leq 4$

$0 \leq R \leq 51$

Example:

for f_{IN} = 27MHz; M = 1; N = 4; Pdiv = 2

→ f_{OUT} = 54MHz

→ f_{VCO} = 108MHz

→ P = 4 – int($\log_2 4$) = 4 – 2 = 2

→ N' = 4 × 2^2 = 16

→ Q = int(16) = 16

→ R = 16 – 16 = 0

for f_{IN} = 27MHz; M = 2; N = 11; Pdiv = 2

→ f_{OUT} = 74.25MHz

→ f_{VCO} = 148.50MHz

→ P = 4 – int($\log_2 5.5$) = 4 – 2 = 2

→ N' = 11 × 2^2 = 44

→ Q = int(22) = 22

→ R = 44 – 44 = 0

The values for P, Q, R, and N' are automatically calculated when using TI ClockPro™ software.

9.2.2.3 Crystal Oscillator Start-Up

When the CDCE949-Q1 is used as a crystal buffer, crystal oscillator start-up dominates the start-up time compared to the internal PLL lock time. Figure 9-4 shows the oscillator start-up sequence for a 27MHz crystal input with an 8pF load. The start-up time for the crystal is in the order of approximately 250µs compared to approximately 10µs of lock time. In general, lock time is an order of magnitude less compared to the crystal start-up time.

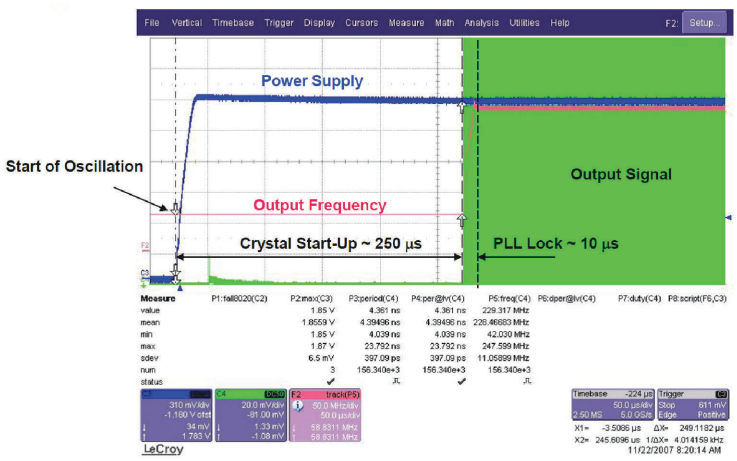


Figure 9-4. Crystal Oscillator Start-Up vs PLL Lock Time

9.2.2.4 Frequency Adjustment With Crystal Oscillator Pulling

The frequency for the CDCE949-Q1 is adjusted for media and other applications with the VCXO control input Vctrl. If a PWM modulated signal is used as a control signal for the VCXO, an external filter is needed.

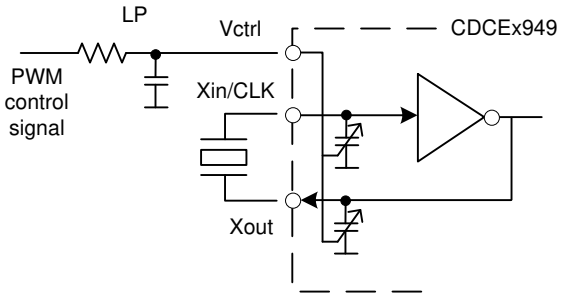


Figure 9-5. Frequency Adjustment Using PWM Input to the VCXO Control

9.2.2.5 Unused Inputs and Outputs

If VCXO pulling functionality is not required, Vctrl must be left floating. All other unused inputs must be set to GND. Unused outputs must be left floating. If one output block is not used, TI recommends disabling the output block. However, TI always recommends providing the supply for the second output block even if the output block is disabled.

9.2.2.6 Switching Between XO and VCXO Mode

When the CDCE949-Q1 is in crystal oscillator or in VCXO configuration, the internal capacitors require different internal capacitance. The following steps are recommended to switch to VCXO mode when the configuration for the on-chip capacitor is still set for XO mode. To center the output frequency to 0ppm:

1. While in XO mode, put Vctrl = Vdd / 2
2. Switch from XO mode to VCXO mode
3. Program the internal capacitors to obtain 0pmm at the output

9.2.3 Application Performance Plots

Figure 9-6, Figure 9-7, Figure 9-8, and Figure 9-9 show CDCE949-Q1 measurements with the SSC feature enabled. Device configuration: 27MHz input, 27MHz output.

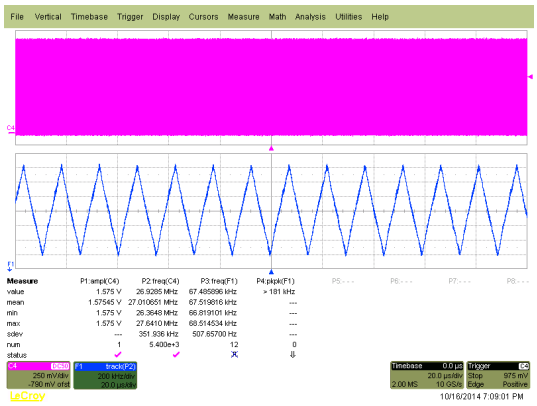


Figure 9-6. fout = 27MHz, VCO frequency < 125

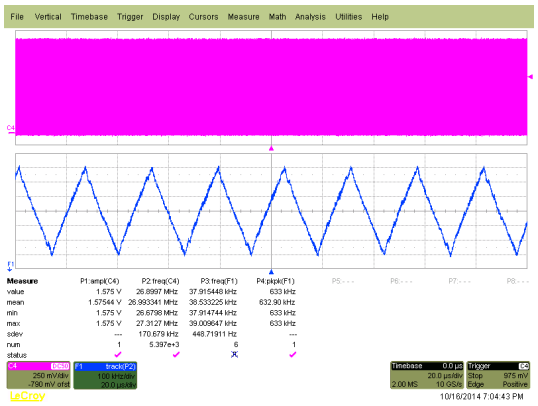


Figure 9-7. fout = 27MHz, VCO frequency > 175

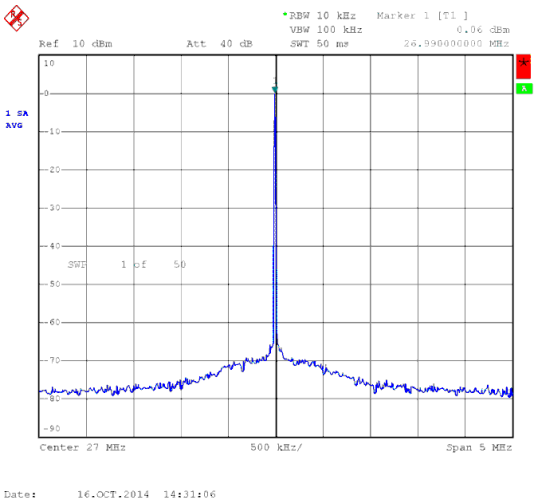


Figure 9-8. Output Spectrum With SSC Off

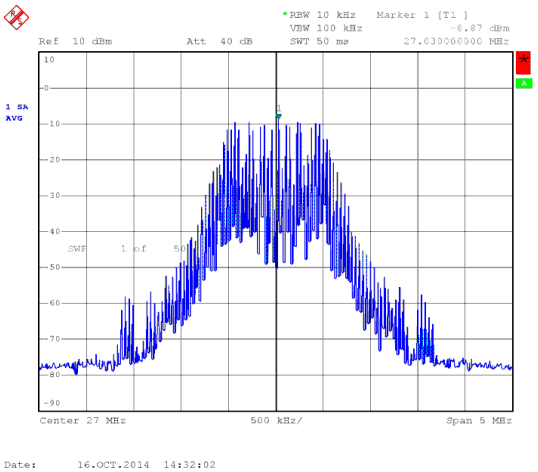


Figure 9-9. Output Spectrum With SSC On, 2%

9.3 Power Supply Recommendations

When using an external reference clock, Xin/CLK must be driven before V_{DD} ramps to avoid risk of unstable output. If V_{DDOUT} is applied before V_{DD}, TI recommends keeping V_{DD} pulled to GND until V_{DDOUT} is ramped. In case the V_{DDOUT} is powered while V_{DD} is floating, there is a risk of high current flowing on the V_{DDOUT}.

The device has a power-up control that is connected to the 1.8V supply. This keeps the whole device disabled until the 1.8V supply reaches a sufficient voltage level. Then, the device switches on all internal components, including the outputs. If a 3.3V V_{DDOUT} is available before the 1.8V, the outputs stay disabled until the 1.8V supply has reached a certain level.

9.4 Layout

9.4.1 Layout Guidelines

When the CDCE949-Q1 is used as a crystal buffer, any parasitics across the crystal affects the pulling range of the VCXO. Therefore, take care in placing the crystal units on the board. Crystals must be placed as close to the device as possible, verifying that the routing lines from the crystal terminals to XIN and XOUT have the same length.

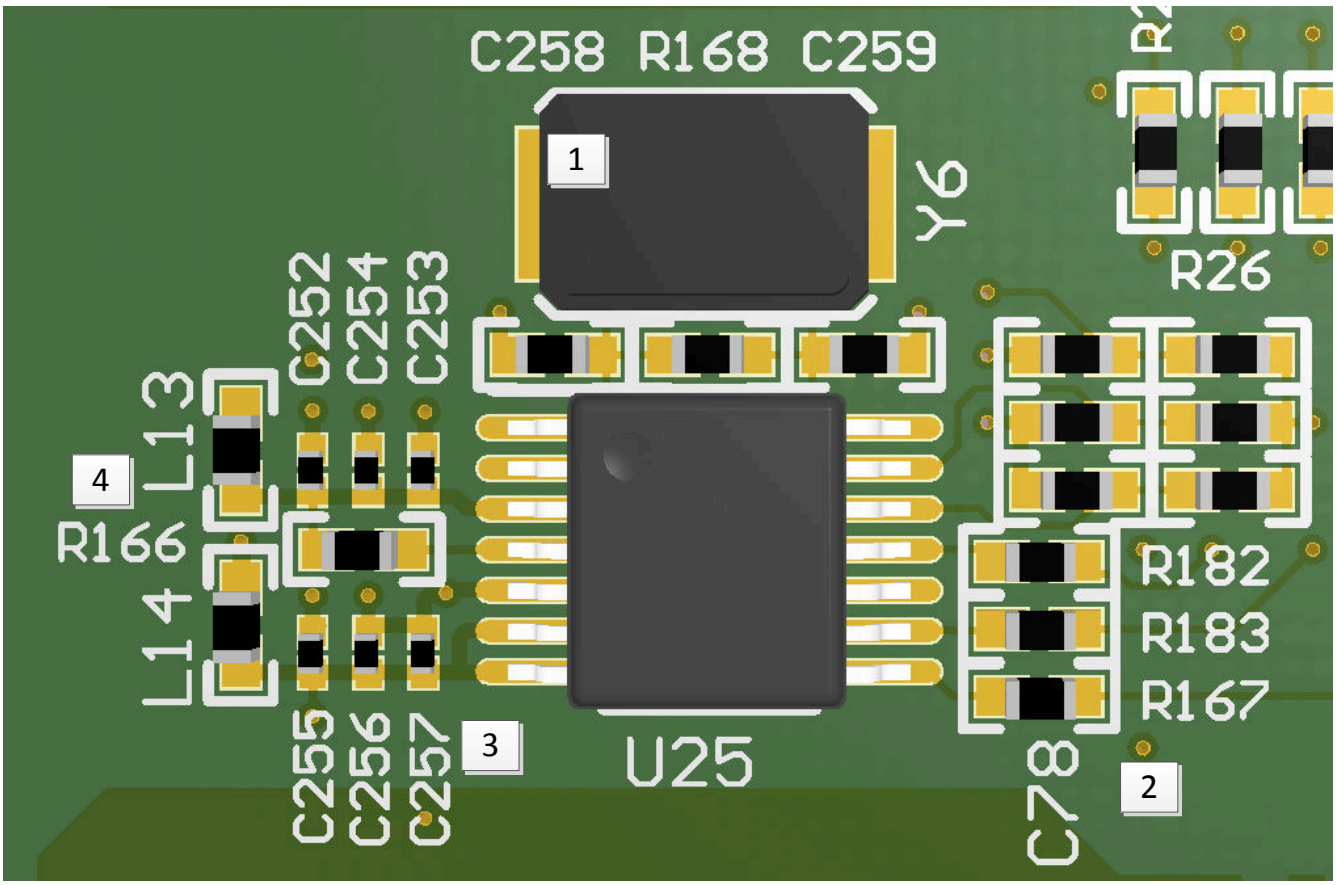
If possible, cut out both ground plane and power plane under the area where the crystal and the routing to the device are placed. In this area, always avoid routing any other signal line, to avoid creating a source of noise coupling.

Additional discrete capacitors can be required to meet the load capacitance specification of certain crystal. For example, a 10.7pF load capacitor is not fully programmable on the chip, because the internal capacitor can range from 0pF to 20pF with steps of 1pF. The 0.7pF capacitor therefore can be discretely added on top of an internal 10pF.

To minimize the inductive influence of the trace, TI recommends placing this small capacitor as close to the device as possible and symmetrically with respect to XIN and XOUT.

Figure 9-10 shows a conceptual layout detailing recommended placement of power supply bypass capacitors on the basis of CDCE949-Q1. For component side mounting, use 0402 body size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low-impedance connection to the ground plane.

9.4.2 Layout Example



1 Place crystal with associated load caps as close to the chip	2 Place series termination resistors at Clock outputs to improve signal integrity
3 Place bypass caps close to the device pins, ensure wide freq. range	4 Use ferrite beads to isolate the device supply pins from board noise sources

Figure 9-10. Annotated Layout

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

1. Texas Instruments, CDCE(L)9xx Performance Evaluation Module EVM User's Guide
2. Texas Instruments, VCXO Application Guideline for CDCE(L)9xx Family Application Report
3. Texas Instruments, General I2C/EEPROM Usage for the CDCE(L)9xx Family Application Report
4. Texas Instruments, Usage of I 2C™ for CDCE(L)949, CDCE(L)937, CDCE(L)925, CDCE(L)913 Application Report

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

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I2C™ is a trademark of Philips Electronics.
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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (February 2010) to Revision A (May 2025)	Page
• Replaced instances of "TI-Pro Clock" with "TI ClockPro"	1
• Added relevant end equipment links to Applications	1
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed the *Pin Functions* section to *Pin Configurations and Functions*	4
• Added pin out diagram	4
• Changed the *THERMAL RESISTANCE FOR TSSOP* table	5
• Updated the *THERMAL RESISTANCE FOR TSSOP* table to the *Thermal Resistance Characteristics* table	5
• Changed *Device Characteristics* to *Electrical Characteristics*	7
• Added the *Detailed Description*, *Overview*, *Feature Description*, and *Device Functional Modes* sections	11
• Added the *Overview* section	11
• Moved the functional Block Diagram to the *Functional Block Diagram* section	12
• Moved *SDA/SCL Serial Interface* to *Feature Description* section	14
• Added information on allowable data inputs during the EEPROM write cycle in Data Protocol	14
• Moved *SDA/SCL Hardware Interface* to *Feature Description* section	16
• Moved *Generic Programming Sequence* to *Programming* section	18
• Moved *Byte Write Programming Sequence* to *Programming* section	18
• Moved *Byte Read Programming Sequence* to *Programming* section	18
• Moved *Block Write Programming Sequence* to *Programming* section	18
• Moved *Block Read Programming Sequence* to *Programming* section	18
• Added *Register Maps* section	19
• Changed Table 8-3 RID From: 0h To: Xb	19
• Added note to the PWDN description, Table 8-3	19
• Added the *Typical Application*, *Design Requirements*, *Application Curves*, and *Detailed Design Procedure* sections	27
• Replaced instances of "master/slave" with "controller/target"	30
• Added the *Power Supply Recommendations* section	31
• Added the *Layout*, *Layout Guidelines*, and *Layout Example* sections	31
• Added the *Device and Documentation Support* section	33

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CDCE949QPWRQ1	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CDCE949Q
CDCE949QPWRQ1.B	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CDCE949Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF CDCE949-Q1 :

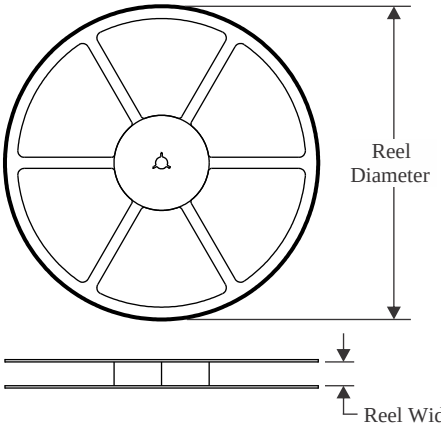
- Catalog : CDCE949

NOTE: Qualified Version Definitions:

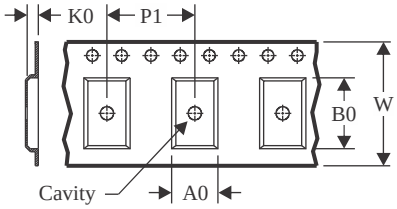
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

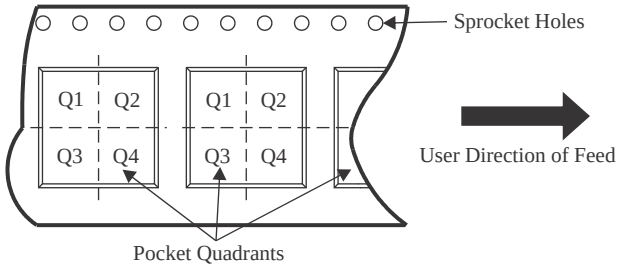


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

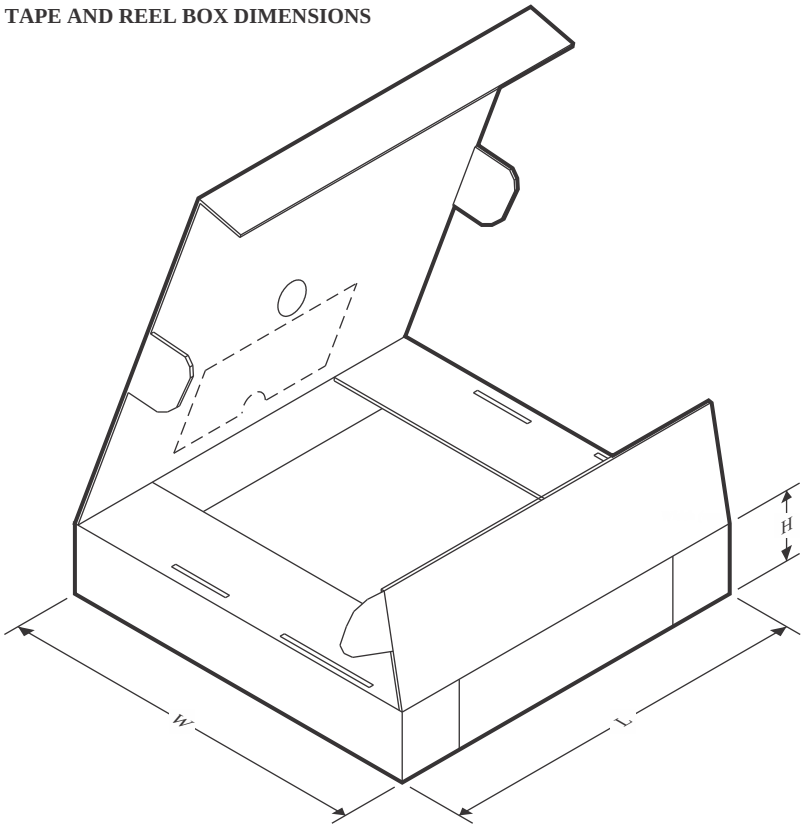
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCE949QPWRQ1	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

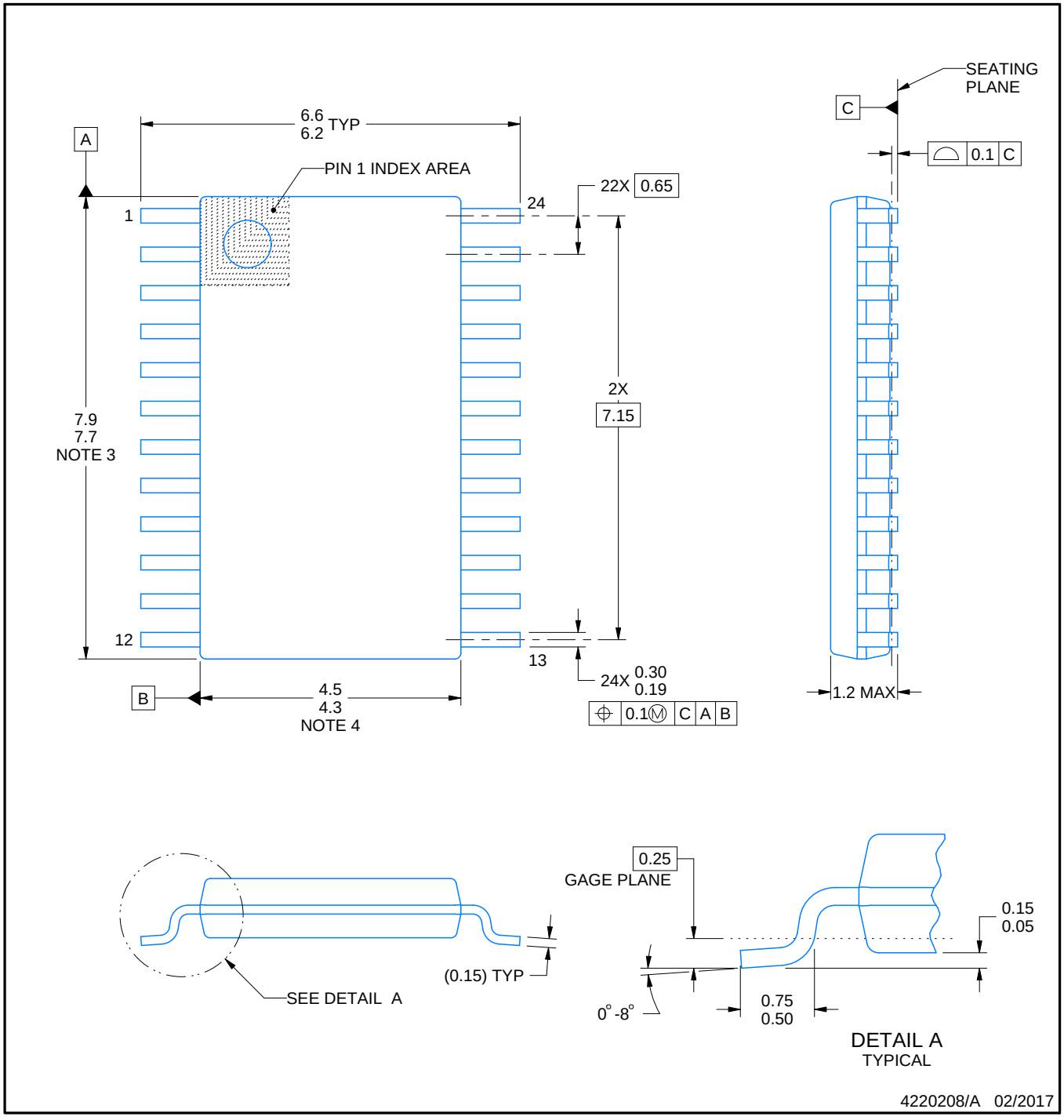
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCE949QPWRQ1	TSSOP	PW	24	2000	353.0	353.0	32.0

PACKAGE OUTLINE

PW0024A

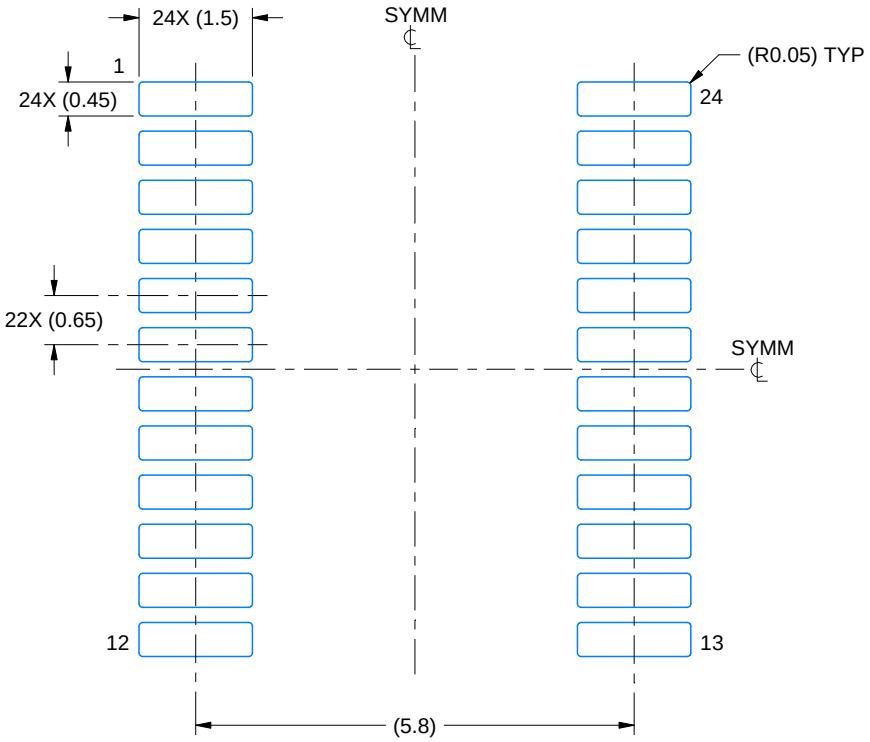
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

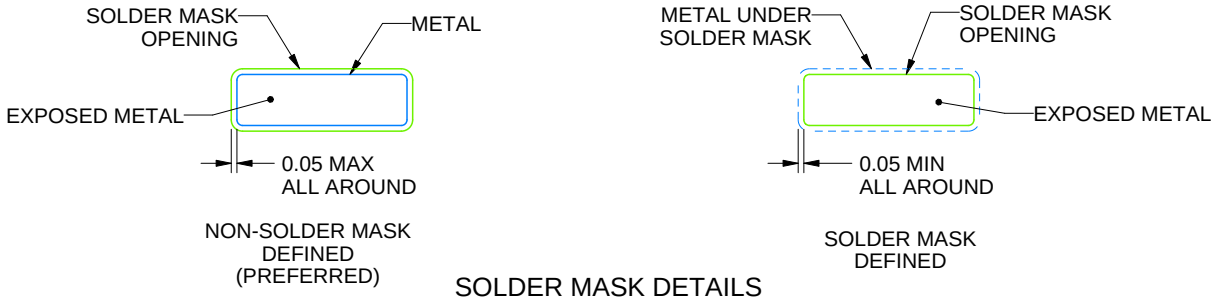


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

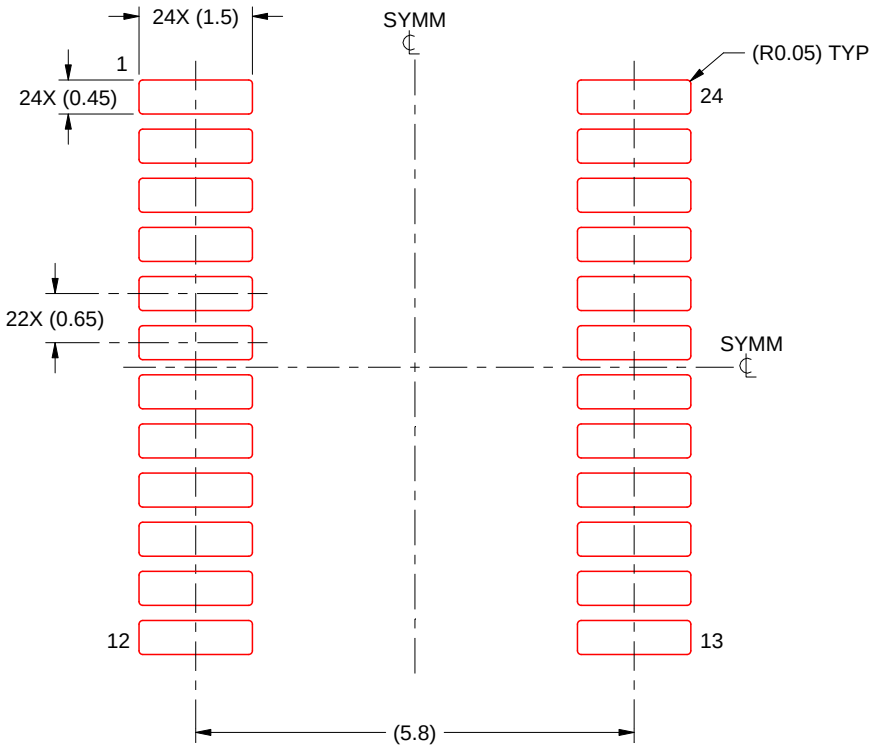


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025