

CSD17382F4 30-V N-Channel FemtoFET™ MOSFET

1 Features

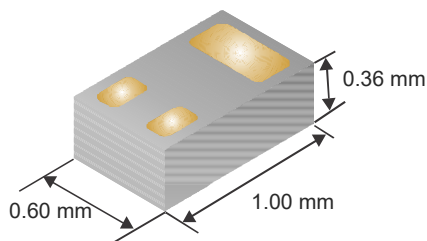
- Low on-resistance
- Low Q_g and Q_{gd}
- Low threshold voltage
- Ultra-small footprint (0402 case size)
 - 1.0 mm × 0.6 mm
- Ultra-low profile
 - 0.36-mm height
- Integrated ESD protection diode
 - Rated > 3-kV HBM
 - Rated > 2-kV CDM
- Lead and halogen free
- RoHS compliant

2 Applications

- Optimized for load switch applications
- Optimized for general purpose switching applications
- Single-cell battery applications
- Handheld and mobile applications

3 Description

This 30-V, 54-mΩ, N-Channel FemtoFET™ MOSFET technology is designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small signal MOSFETs while providing at least a 60% reduction in footprint size.



Typical Part Dimensions

Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	30	V
Q_g	Gate Charge Total (4.5 V)	2.1	nC
Q_{gd}	Gate Charge Gate-to-Drain	0.63	nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 1.8\text{ V}$	110 mΩ
		$V_{GS} = 2.5\text{ V}$	67 mΩ
		$V_{GS} = 4.5\text{ V}$	56 mΩ
		$V_{GS} = 8.0\text{ V}$	54 mΩ
$V_{GS(th)}$	Threshold Voltage	0.9	V

Device Information

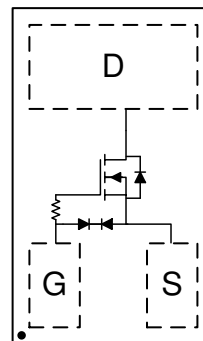
DEVICE ⁽¹⁾	QTY	MEDIA	PACKAGE	SHIP
CSD17382F4	3000	7-Inch Reel	Femto (0402) 1.0-mm × 0.6-mm SMD Lead Less	Tape and Reel
CSD17382F4T	250			

- (1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	10	V
I_D	Continuous Drain Current ⁽¹⁾	2.3	A
I_{DM}	Pulsed Drain Current ⁽²⁾	14.8	A
P_D	Power Dissipation ⁽¹⁾	500	mW
ESD Rating	Human Body Model (HBM)	3000	V
	Charged Device Model (CDM)	2000	V
T_J, T_{stg}	Operating Junction, Storage Temperature	–55 to 150	°C
E_{AS}	Avalanche Energy, Single Pulse $I_D = 6.5\text{ A}$, $L = 0.1\text{ mH}$, $R_G = 25\text{ }\Omega$	2.1	mJ

- (1) Typical $R_{\theta JA} = 245^\circ\text{C/W}$ on 1-in² (6.45-cm²), 2-oz. (0.071-mm) thick Cu pad on a 0.06-in (1.52-mm) thick FR4 PCB.
- (2) Pulse duration $\leq 100\text{ }\mu\text{s}$, duty cycle $\leq 1\%$.



Top View



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (October 2021) to Revision C (February 2022)	Page
• Changed ultra-low profile bullet from 0.35 mm to 0.36 mm in height.....	1
• Updated ultra-low profile image height from 0.35 mm to 0.36 mm.....	1
• Changed ultra-low profile image height from 0.35 mm to 0.36 mm.....	8
• Added FemtoFET Surface Mount Guide note.....	9

Changes from Revision A (December 2016) to Revision B (October 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1

Changes from Revision * (April 2016) to Revision A (December 2016)	Page
• Changed the TEST CONDITIONS for g_{fs} Transconductance From: $V_{DS} = 15\text{ V}$ To: $V_{DS} = 3\text{ V}$ in the Section 5.1 section.	3
• Added Section 6.2 in the Section 6 section.	7
• Updated all mechanical drawings.	8

5 Specifications

5.1 Electrical Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV _{DSS}	Drain-to-source voltage	V _{GS} = 0 V, I _{DS} = 250 μA	30			V
I _{DSS}	Drain-to-source leakage current	V _{GS} = 0 V, V _{DS} = 24 V			1	μA
I _{GSS}	Gate-to-source leakage current	V _{DS} = 0 V, V _{GS} = 10 V			5	μA
V _{GS(th)}	Gate-to-source threshold voltage	V _{DS} = V _{GS} , I _{DS} = 250 μA	0.7	0.9	1.2	V
R _{DS(on)}	Drain-to-source on-resistance	V _{GS} = 1.8 V, I _{DS} =0.5 A		110	180	mΩ
		V _{GS} = 2.5 V, I _{DS} =0.5 A		67	82	mΩ
		V _{GS} = 4.5 V, I _{DS} = 0.5 A		56	67	mΩ
		V _{GS} = 8.0 V, I _{DS} = 0.5 A		54	64	mΩ
g _{fs}	Transconductance	V _{DS} = 3 V, I _{DS} = 0.5 A		5.9		S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input capacitance	V _{GS} = 0 V, V _{DS} = 15 V, f = 1 MHz		267	347	pF
C _{oss}	Output capacitance			31.0	40.3	pF
C _{rss}	Reverse transfer capacitance			15.0	19.5	pF
R _G	Series gate resistance			220		Ω
Q _g	Gate charge total (4.5 V)	V _{DS} = 15 V, I _{DS} = 0.5 A		2.1	2.7	nC
Q _{gd}	Gate charge gate-to-drain			0.63		nC
Q _{gs}	Gate charge gate-to-source			0.41		nC
Q _{g(th)}	Gate charge at V _{th}			0.12		nC
Q _{oss}	Output charge	V _{DS} = 15 V, V _{GS} = 0 V		1.53		nC
t _{d(on)}	Turn on delay time	V _{DS} = 15 V, V _{GS} = 4.5 V, I _{DS} = 0.5 A, R _G = 0 Ω		59		ns
t _r	Rise time			111		ns
t _{d(off)}	Turn off delay time			279		ns
t _f	Fall time			270		ns
DIODE CHARACTERISTICS						
V _{SD}	Diode forward voltage	I _{SD} = 0.5 A, V _{GS} = 0 V		0.7	1.0	V

5.2 Thermal Information

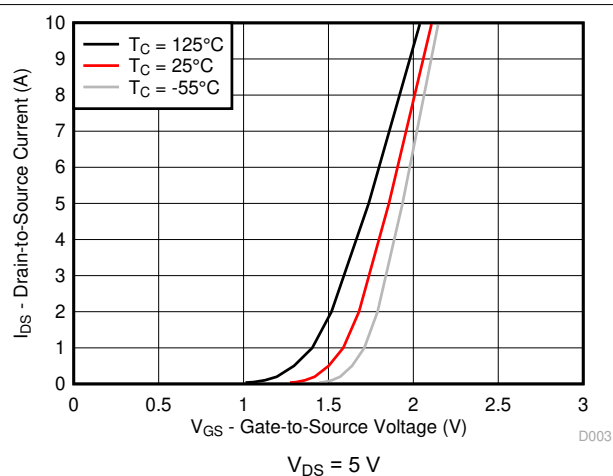
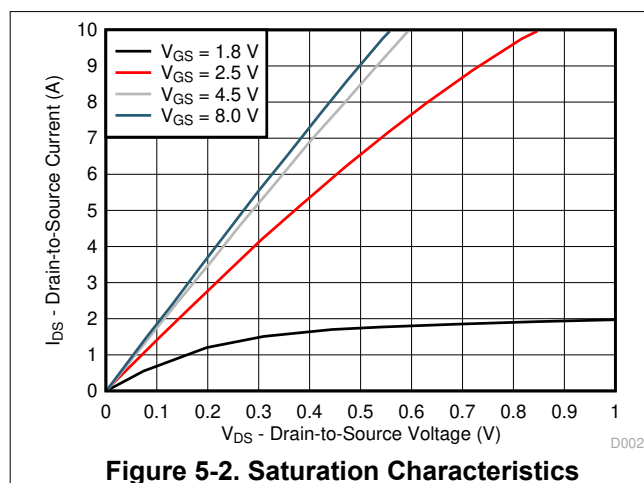
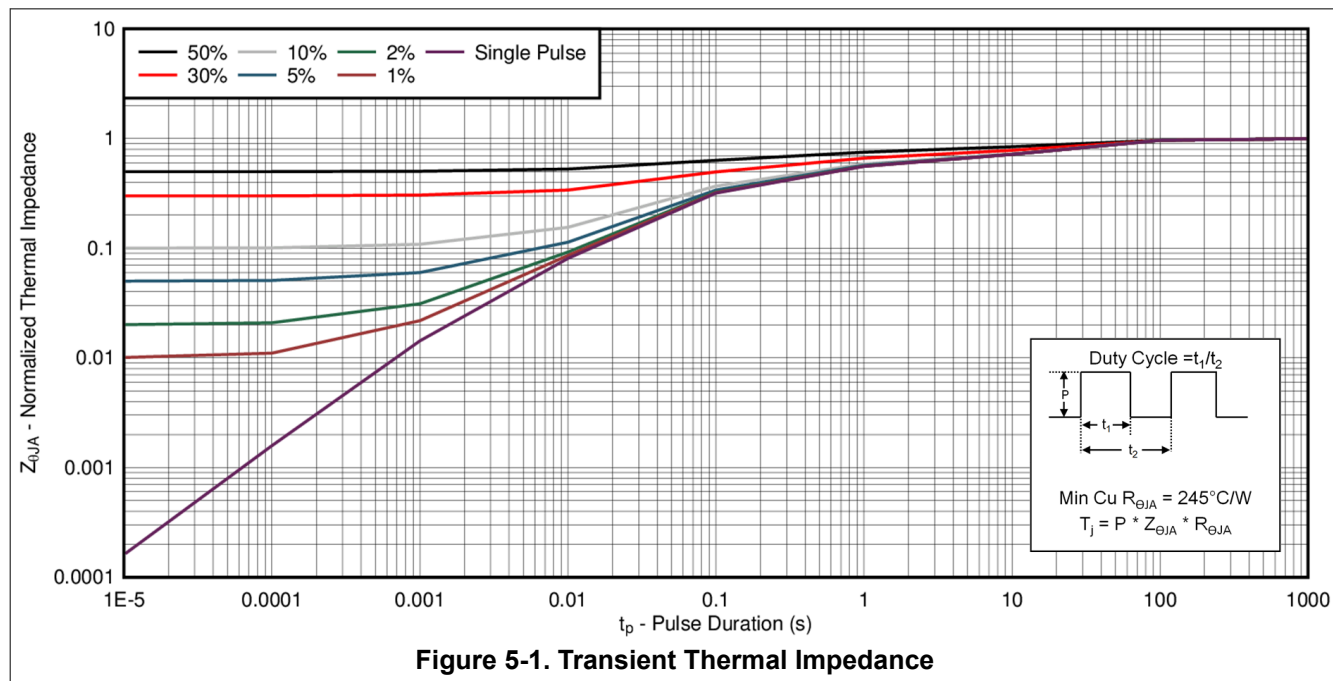
$T_A = 25^\circ\text{C}$ (unless otherwise stated)

THERMAL METRIC		TYPICAL VALUES	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽¹⁾	85	$^\circ\text{C/W}$
	Junction-to-ambient thermal resistance ⁽²⁾	245	$^\circ\text{C/W}$

- (1) Device mounted on FR4 material with 1-in² (6.45-cm²), 2-oz. (0.071-mm) thick Cu.
 (2) Device mounted on FR4 material with minimum Cu mounting area.

5.3 Typical MOSFET Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise stated)



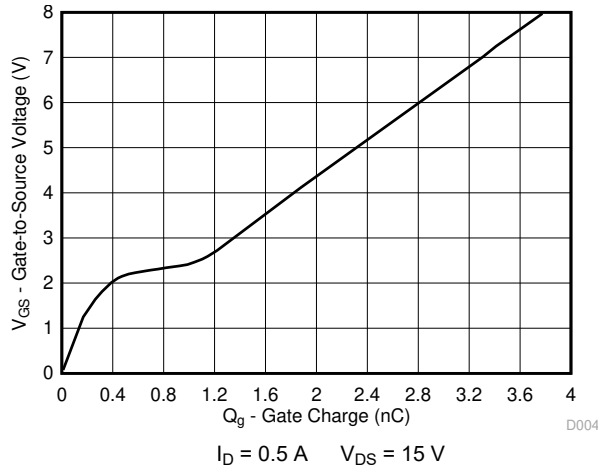


Figure 5-4. Gate Charge

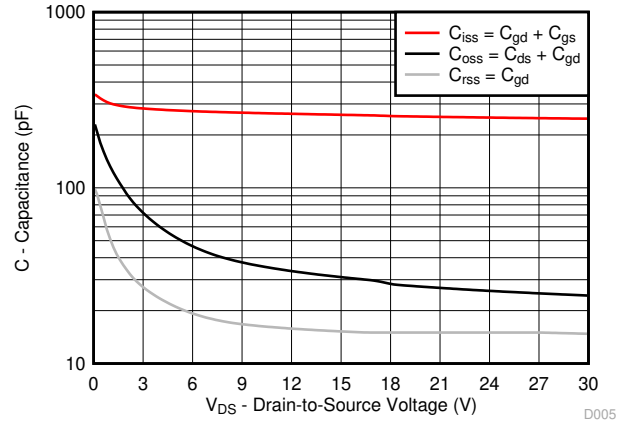


Figure 5-5. Capacitance

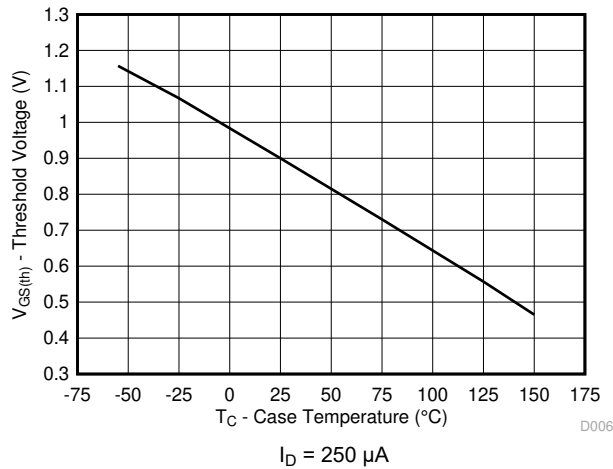


Figure 5-6. Threshold Voltage vs Temperature

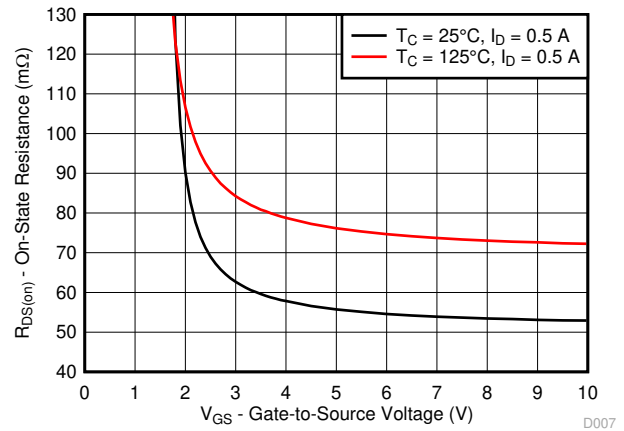


Figure 5-7. On-State Resistance vs Gate-to-Source Voltage

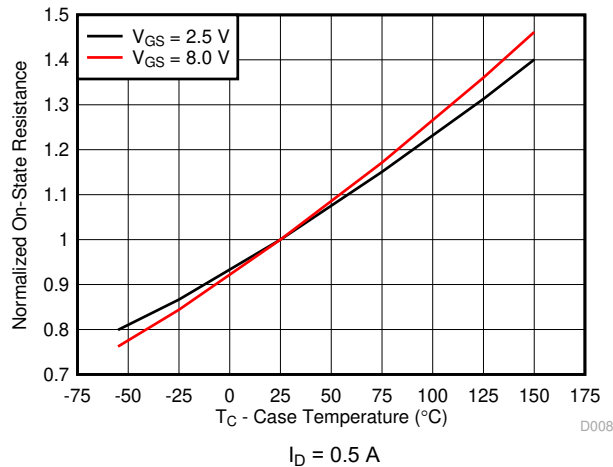


Figure 5-8. Normalized On-State Resistance vs Temperature

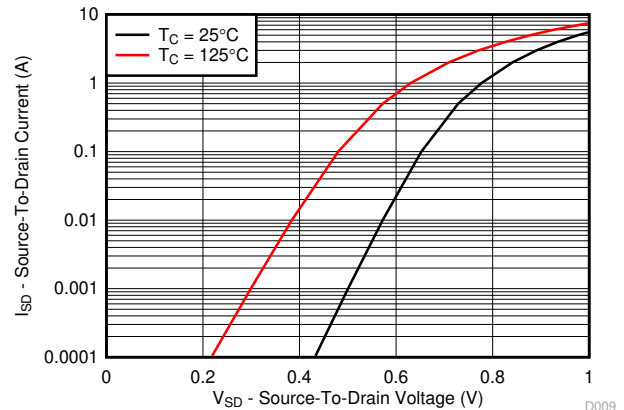


Figure 5-9. Typical Diode Forward Voltage

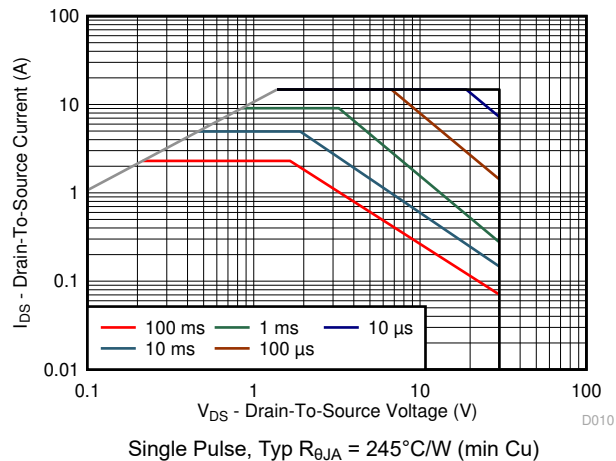


Figure 5-10. Maximum Safe Operating Area (SOA)

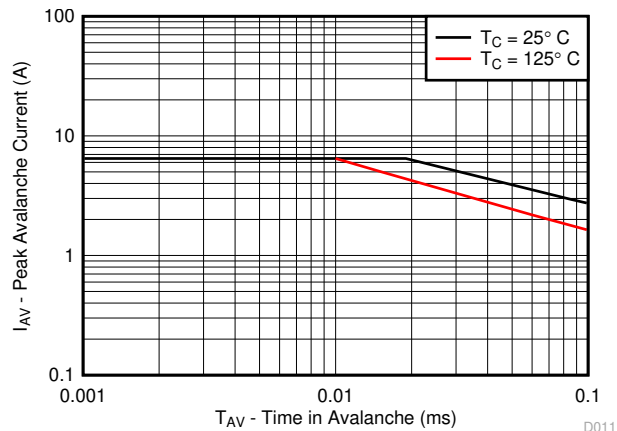


Figure 5-11. Single Pulse Unclamped Inductive Switching

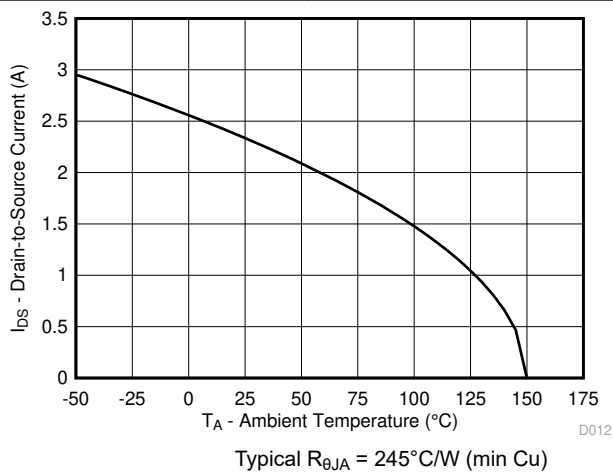


Figure 5-12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

6.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.3 Trademarks

FemtoFET™ is a trademark of Texas Instruments.

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

6.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.5 Glossary

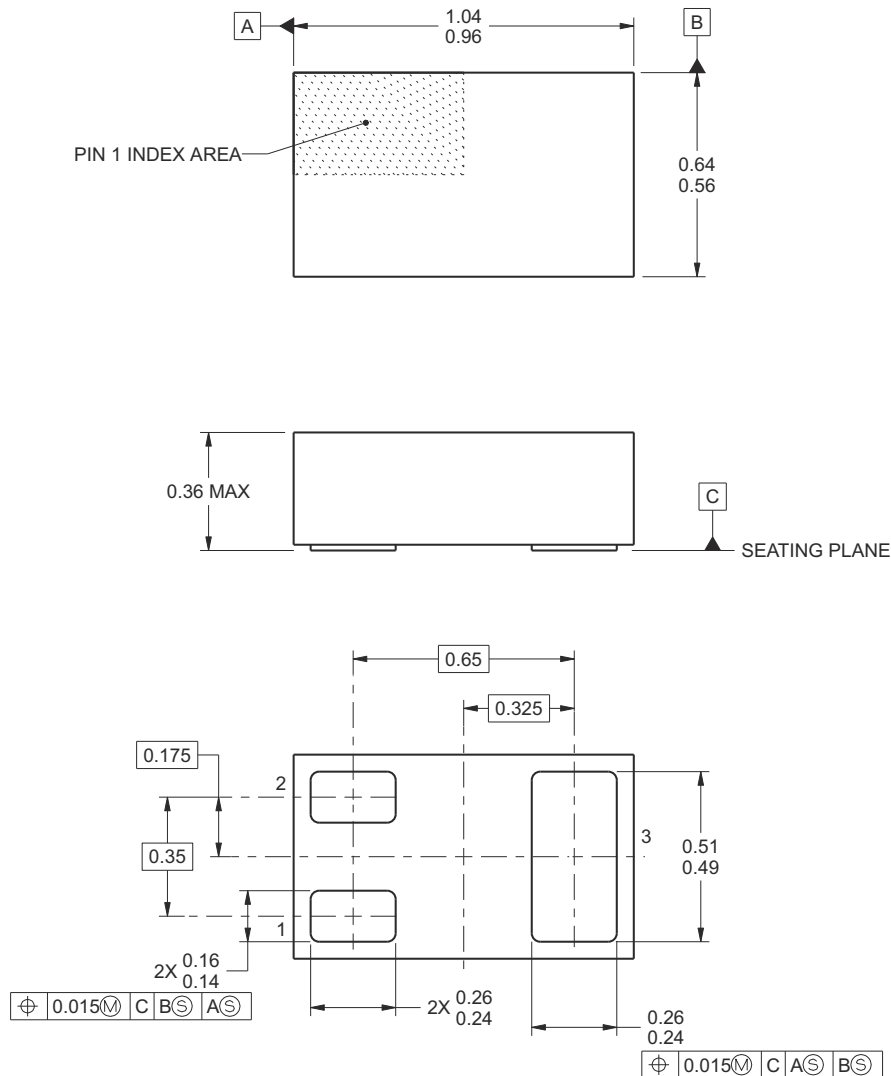
[TI Glossary](#)

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

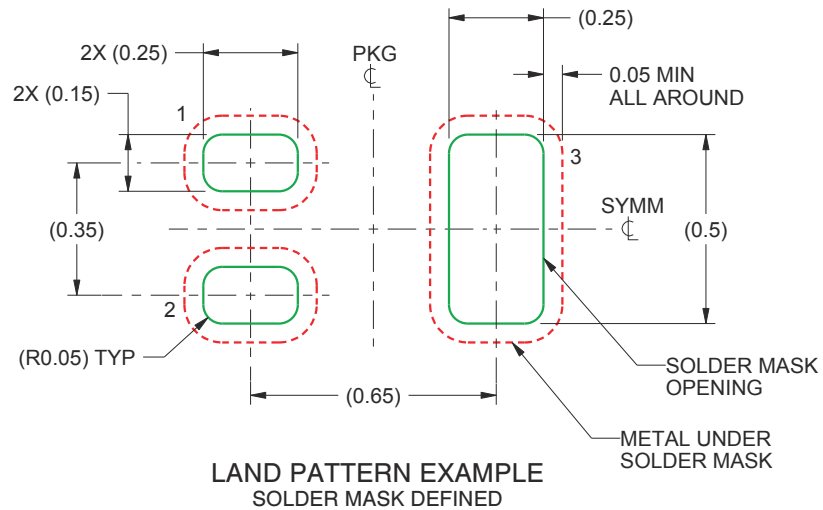
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Mechanical Dimensions



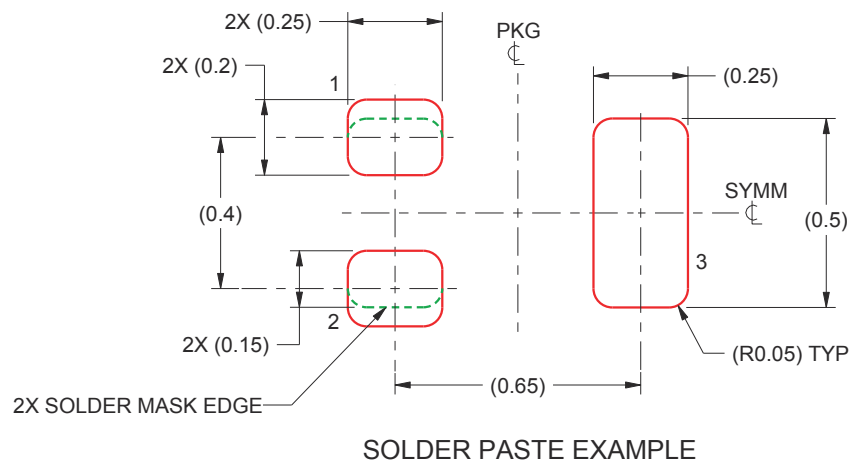
- A. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- B. This drawing is subject to change without notice.
- C. This package is a Pb-free bump design. Bump finish may vary. To determine the exact finish, refer to the device datasheet or contact a local TI representative.

7.2 Recommended Minimum PCB Layout



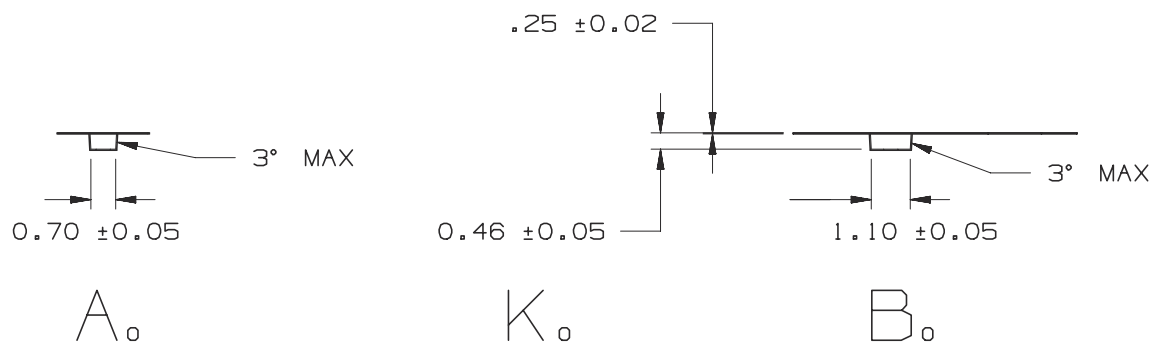
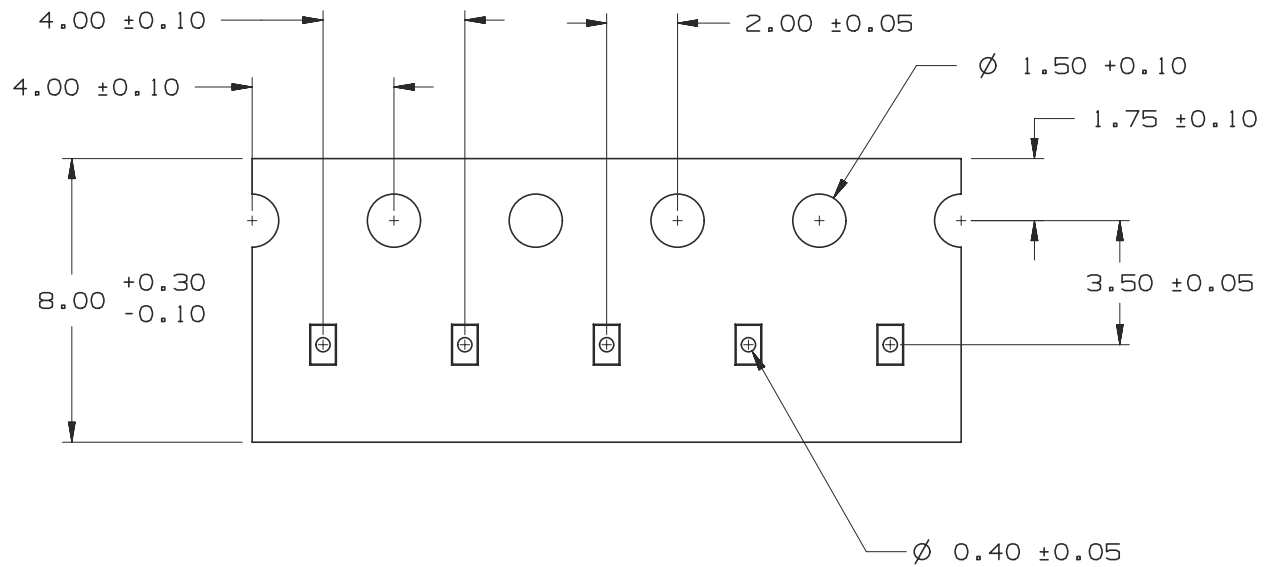
- A. All dimensions are in millimeters.
- B. For more information, see [FemtoFET Surface Mount Guide](#) (SLRA003D).

7.3 Recommended Stencil Pattern



- A. All dimensions are in millimeters.
- B. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

7.4 CSD17382F4 Embossed Carrier Tape Dimensions



- A. Pin 1 is oriented in the top-right quadrant of the tape enclosure (quadrant 2), closest to the carrier tape sprocket holes.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD17382F4	Active	Production	PICOSTAR (YJC) 3	3000 LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	HM
CSD17382F4.B	Active	Production	PICOSTAR (YJC) 3	3000 LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	HM
CSD17382F4T	Active	Production	PICOSTAR (YJC) 3	250 SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	HM
CSD17382F4T.B	Active	Production	PICOSTAR (YJC) 3	250 SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	HM

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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