

# CSD18514Q5A 40-V N-Channel NexFET™ Power MOSFET

## 1 Features

- Low  $R_{DS(on)}$
- Low-Thermal Resistance
- Avalanche Rated
- Logic Level
- Lead-Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm × 6-mm Plastic Package

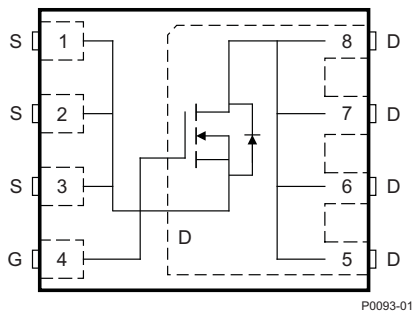
## 2 Applications

- DC-DC Conversion
- Secondary Side Synchronous Rectifier
- Battery Motor Control

## 3 Description

This 4.1-m $\Omega$ , SON 5-mm × 6-mm, 40-V NexFET™ power MOSFET is designed to minimize losses in power conversion applications.

Top View



## Product Summary

| $T_A = 25^\circ\text{C}$ |                               | TYPICAL VALUE           |     | UNIT       |
|--------------------------|-------------------------------|-------------------------|-----|------------|
| $V_{DS}$                 | Drain-to-Source Voltage       | 40                      |     | V          |
| $Q_g$                    | Gate Charge Total (10 V)      | 29                      |     | nC         |
| $Q_{gd}$                 | Gate Charge Gate-to-Drain     | 5.0                     |     | nC         |
| $R_{DS(on)}$             | Drain-to-Source On Resistance | $V_{GS} = 4.5\text{ V}$ | 6.0 | m $\Omega$ |
|                          |                               | $V_{GS} = 10\text{ V}$  | 4.1 |            |
| $V_{GS(th)}$             | Threshold Voltage             | 1.8                     |     | V          |

## Device Information<sup>(1)</sup>

| DEVICE       | MEDIA        | QTY  | PACKAGE                           | SHIP          |
|--------------|--------------|------|-----------------------------------|---------------|
| CSD18514Q5A  | 13-Inch Reel | 2500 | SON                               | Tape and Reel |
| CSD18514Q5AT | 7-Inch Reel  | 250  | 5.00-mm × 6.00-mm Plastic Package |               |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

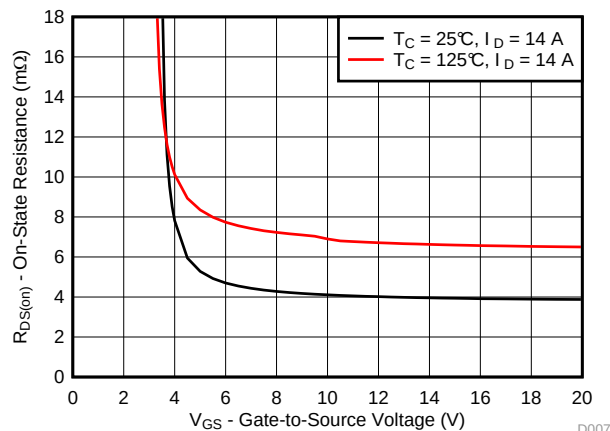
## Absolute Maximum Ratings

| $T_A = 25^\circ\text{C}$ |                                                                                                        | VALUE      | UNIT |
|--------------------------|--------------------------------------------------------------------------------------------------------|------------|------|
| $V_{DS}$                 | Drain-to-Source Voltage                                                                                | 40         | V    |
| $V_{GS}$                 | Gate-to-Source Voltage                                                                                 | ±20        | V    |
| $I_D$                    | Continuous Drain Current (Package Limited)                                                             | 50         | A    |
|                          | Continuous Drain Current (Silicon Limited), $T_C = 25^\circ\text{C}$                                   | 89         |      |
|                          | Continuous Drain Current <sup>(1)</sup>                                                                | 18         |      |
| $I_{DM}$                 | Pulsed Drain Current <sup>(2)</sup>                                                                    | 237        | A    |
| $P_D$                    | Power Dissipation <sup>(1)</sup>                                                                       | 3.1        | W    |
|                          | Power Dissipation, $T_C = 25^\circ\text{C}$                                                            | 74         |      |
| $T_J, T_{stg}$           | Operating Junction, Storage Temperature                                                                | –55 to 150 | °C   |
| $E_{AS}$                 | Avalanche Energy, Single Pulse<br>$I_D = 33\text{ A}$ , $L = 0.1\text{ mH}$ , $R_G = 25\text{ }\Omega$ | 55         | mJ   |

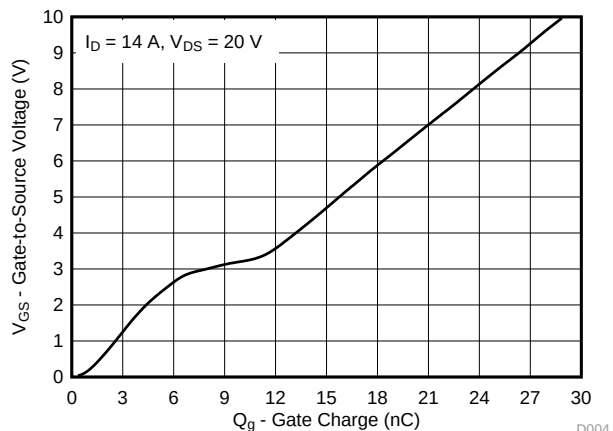
(1) Typical  $R_{\theta JA} = 40^\circ\text{C/W}$  on a 1-in<sup>2</sup>, 2-oz Cu pad on a 0.06-in thick FR4 PCB.

(2) Max  $R_{\theta JC} = 1.7^\circ\text{C/W}$ , pulse duration  $\leq 100\text{ }\mu\text{s}$ , duty cycle  $\leq 1\%$ .

$R_{DS(on)}$  vs  $V_{GS}$



Gate Charge



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## 4 Revision History

| Changes from Original (November 2016) to Revision A                                                                           | Page     |
|-------------------------------------------------------------------------------------------------------------------------------|----------|
| • Changed the charge values in the Dynamic Characteristics section of the <i>Electrical Characteristics</i> table.....        | <b>3</b> |
| • Changed <a href="#">Figure 4</a> in the <i>Typical MOSFET Characteristics</i> section to reflect updated gate charges ..... | <b>4</b> |

## 5 Specifications

### 5.1 Electrical Characteristics

 $T_A = 25^\circ\text{C}$  (unless otherwise stated)

| PARAMETER               |                                  | TEST CONDITIONS                                                                                 | MIN  | TYP | MAX  | UNIT |
|-------------------------|----------------------------------|-------------------------------------------------------------------------------------------------|------|-----|------|------|
| STATIC CHARACTERISTICS  |                                  |                                                                                                 |      |     |      |      |
| BV <sub>DSS</sub>       | Drain-to-source voltage          | V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA                                                  | 40   |     |      | V    |
| I <sub>DSS</sub>        | Drain-to-source leakage current  | V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 32 V                                                   |      |     | 1    | μA   |
| I <sub>GSS</sub>        | Gate-to-source leakage current   | V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 20 V                                                   |      |     | 100  | nA   |
| V <sub>GS(th)</sub>     | Gate-to-source threshold voltage | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA                                     | 1.5  | 1.8 | 2.4  | V    |
| R <sub>DS(on)</sub>     | Drain-to-source on resistance    | V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 14 A                                                  | 6.0  |     | 7.9  | mΩ   |
|                         |                                  | V <sub>GS</sub> = 10 V, I <sub>D</sub> = 14 A                                                   | 4.1  |     | 4.9  |      |
| g <sub>fs</sub>         | Transconductance                 | V <sub>DS</sub> = 4 V, I <sub>D</sub> = 14 A                                                    | 59   |     |      | S    |
| DYNAMIC CHARACTERISTICS |                                  |                                                                                                 |      |     |      |      |
| C <sub>iss</sub>        | Input capacitance                | V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 20 V, f = 1 MHz                                        | 2060 |     | 2680 | pF   |
| C <sub>oss</sub>        | Output capacitance               |                                                                                                 | 205  |     | 267  | pF   |
| C <sub>rss</sub>        | Reverse transfer capacitance     |                                                                                                 | 106  |     | 138  | pF   |
| R <sub>G</sub>          | Series gate resistance           |                                                                                                 | 1.3  | 2.6 |      | Ω    |
| Q <sub>g</sub>          | Gate charge total (4.5 V)        | V <sub>DS</sub> = 20 V, I <sub>D</sub> = 14 A                                                   | 14   |     | 18   | nC   |
| Q <sub>g</sub>          | Gate charge total (10 V)         |                                                                                                 | 29   |     | 38   | nC   |
| Q <sub>gd</sub>         | Gate charge gate-to-drain        |                                                                                                 | 5.0  |     |      | nC   |
| Q <sub>gs</sub>         | Gate charge gate-to-source       |                                                                                                 | 6.0  |     |      | nC   |
| Q <sub>g(th)</sub>      | Gate charge at V <sub>th</sub>   |                                                                                                 | 3.4  |     |      | nC   |
| Q <sub>oss</sub>        | Output charge                    | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V                                                   | 9.2  |     |      | nC   |
| t <sub>d(on)</sub>      | Turnon delay time                | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 10 V,<br>I <sub>DS</sub> = 14 A, R <sub>G</sub> = 0 Ω | 13   |     |      | ns   |
| t <sub>r</sub>          | Rise time                        |                                                                                                 | 22   |     |      | ns   |
| t <sub>d(off)</sub>     | Turnoff delay time               |                                                                                                 | 14   |     |      | ns   |
| t <sub>f</sub>          | Fall time                        |                                                                                                 | 6    |     |      | ns   |
| DIODE CHARACTERISTICS   |                                  |                                                                                                 |      |     |      |      |
| V <sub>SD</sub>         | Diode forward voltage            | I <sub>SD</sub> = 14 A, V <sub>GS</sub> = 0 V                                                   | 0.8  |     | 1.0  | V    |
| Q <sub>rr</sub>         | Reverse recovery charge          | V <sub>DS</sub> = 20 V, I <sub>F</sub> = 14 A,<br>di/dt = 300 A/μs                              | 8.5  |     |      | nC   |
| t <sub>rr</sub>         | Reverse recovery time            |                                                                                                 | 9    |     |      | ns   |

### 5.2 Thermal Information

 $T_A = 25^\circ\text{C}$  (unless otherwise stated)

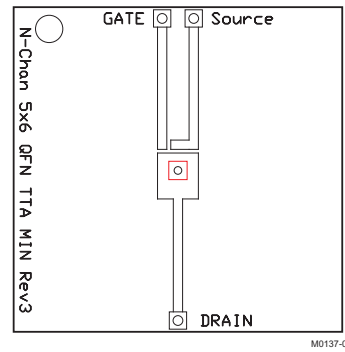
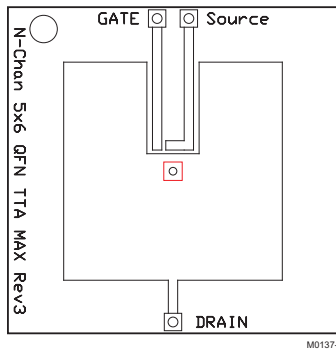
| THERMAL METRIC  |                                                          | MIN | TYP | MAX | UNIT                      |
|-----------------|----------------------------------------------------------|-----|-----|-----|---------------------------|
| $R_{\theta JC}$ | Junction-to-case thermal resistance <sup>(1)</sup>       |     |     | 1.7 | $^\circ\text{C}/\text{W}$ |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance <sup>(1)(2)</sup> |     |     | 50  |                           |

- $R_{\theta JC}$  is determined with the device mounted on a 1-in<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz (0.071-mm) thick Cu pad on a 1.5-in  $\times$  1.5-in (3.81-cm  $\times$  3.81-cm), 0.06-in (1.52-mm) thick FR4 PCB.  $R_{\theta JC}$  is specified by design, whereas  $R_{\theta JA}$  is determined by the user's board design.
- Device mounted on FR4 material with 1-in<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz (0.071-mm) thick Cu.

## CSD18514Q5A

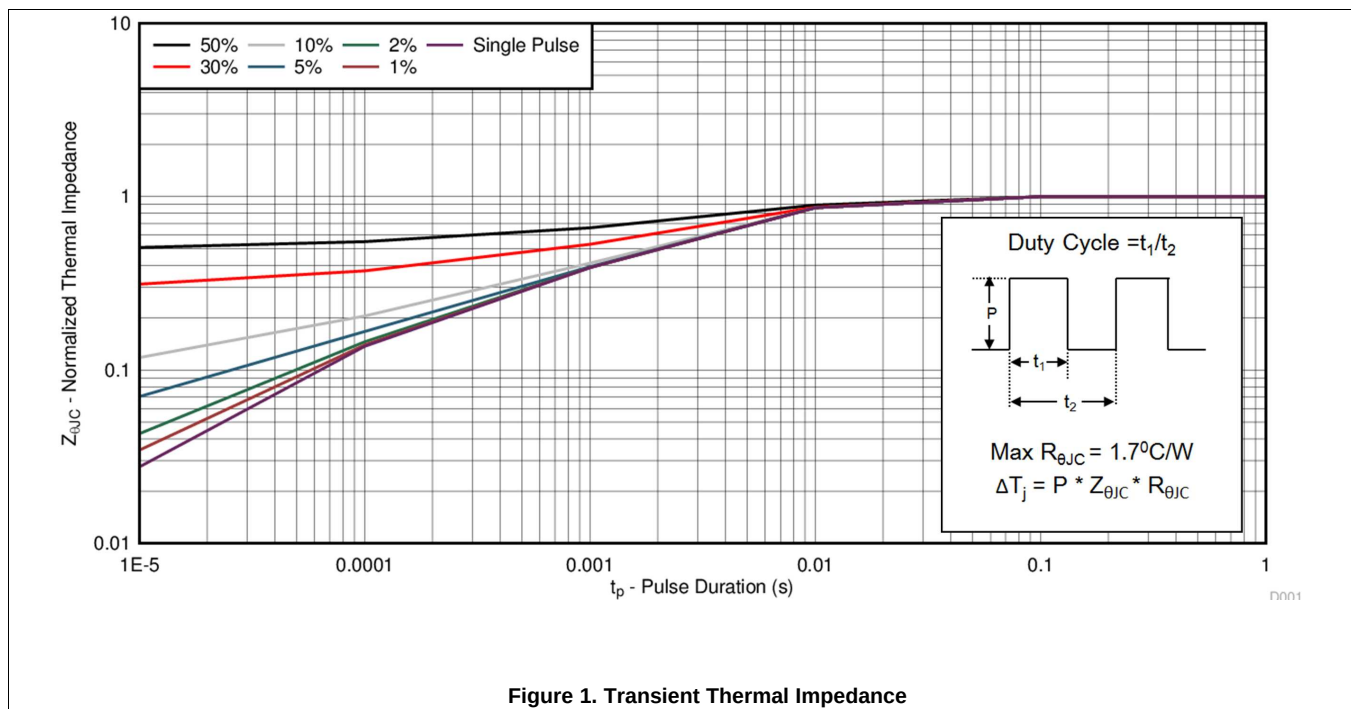
SLPS625A –NOVEMBER 2016–REVISED JANUARY 2017

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### 5.3 Typical MOSFET Characteristics

$T_A = 25^{\circ}\text{C}$  (unless otherwise stated)



## Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$  (unless otherwise stated)

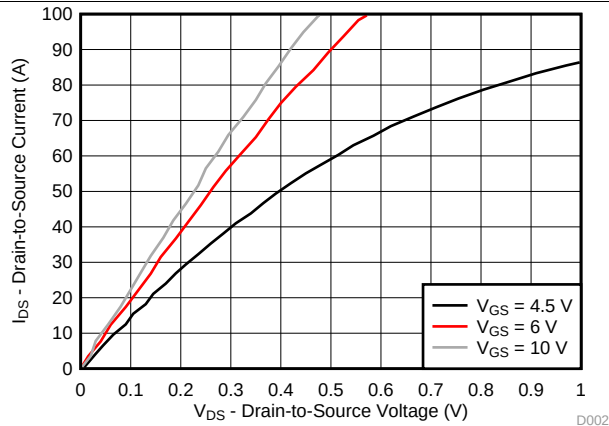


Figure 2. Saturation Characteristics

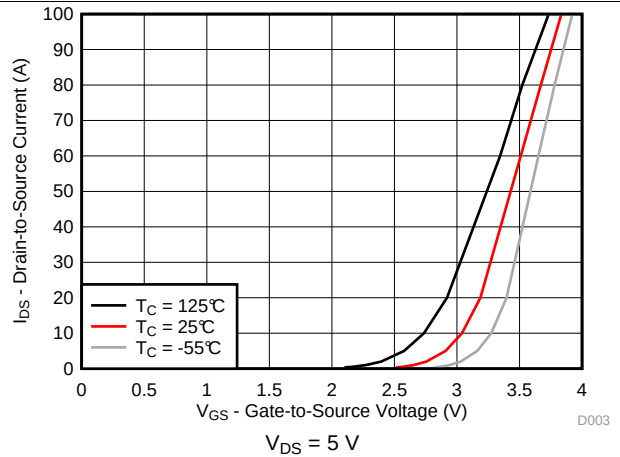


Figure 3. Transfer Characteristics

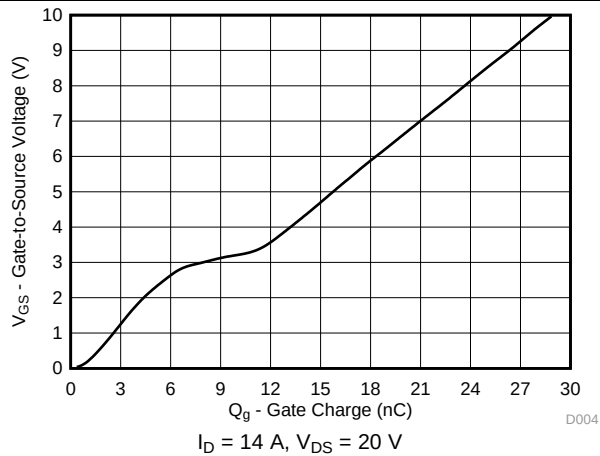


Figure 4. Gate Charge

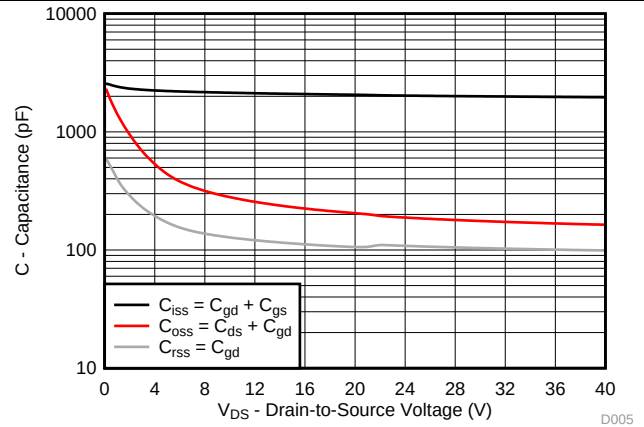


Figure 5. Capacitance

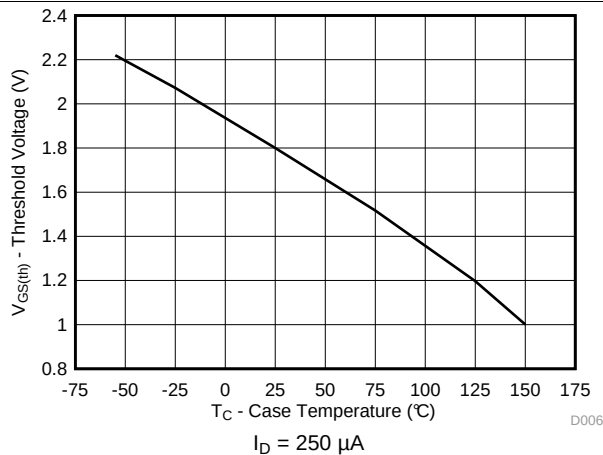


Figure 6. Threshold Voltage vs Temperature

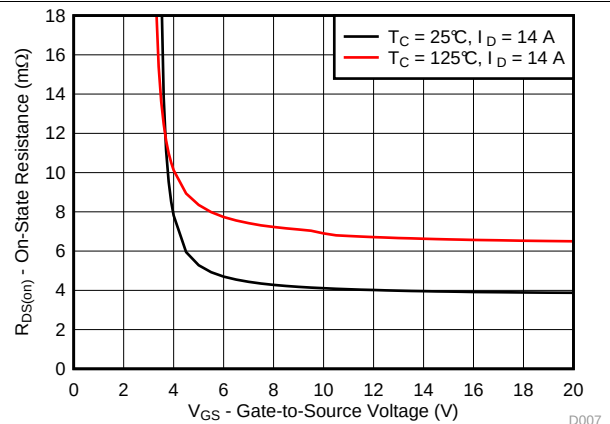


Figure 7. On-State Resistance vs Gate-to-Source Voltage

## Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$  (unless otherwise stated)

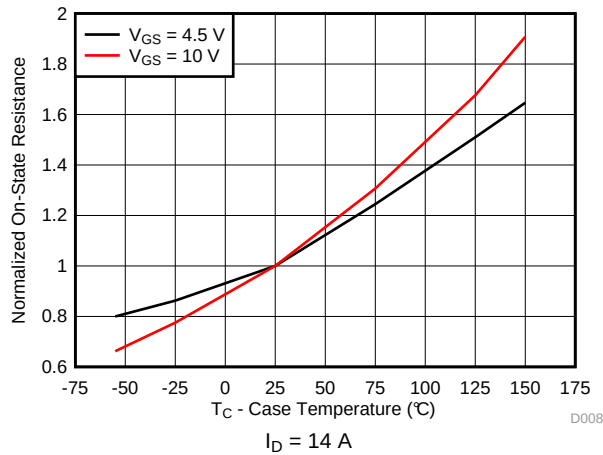


Figure 8. Normalized On-State Resistance vs Temperature

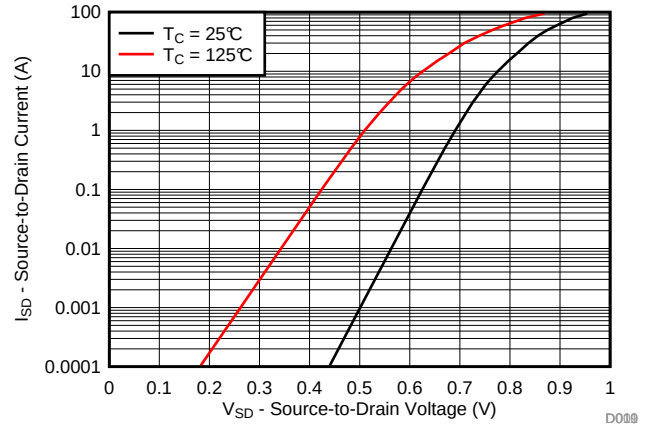


Figure 9. Typical Diode Forward Voltage

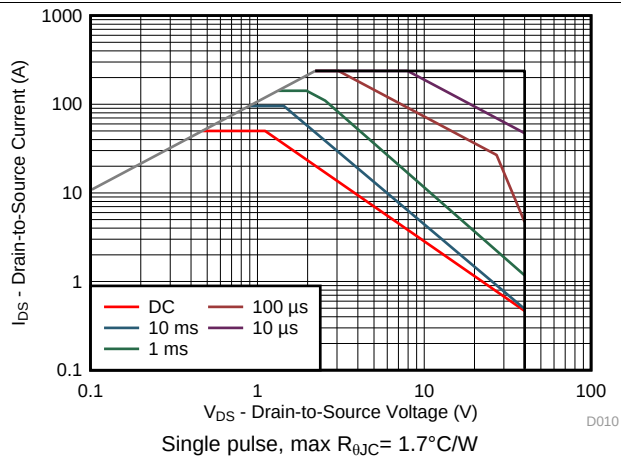


Figure 10. Maximum Safe Operating Area

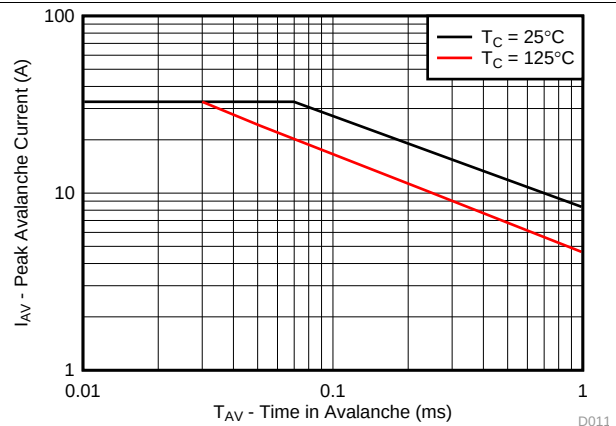


Figure 11. Single Pulse Unclamped Inductive Switching

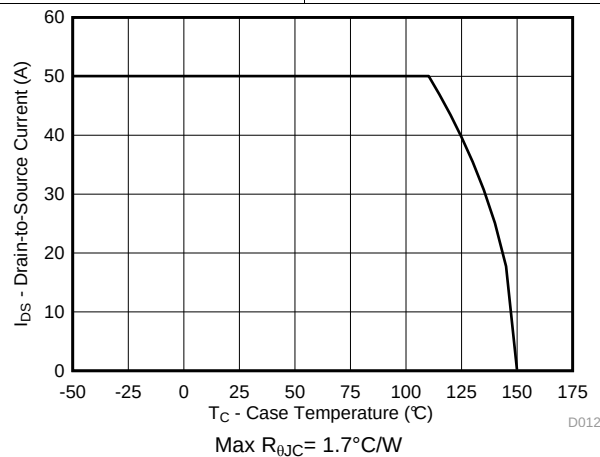


Figure 12. Maximum Drain Current vs Temperature

## 6 Device and Documentation Support

### 6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 6.3 Trademarks

NexFET, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 6.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 6.5 Glossary

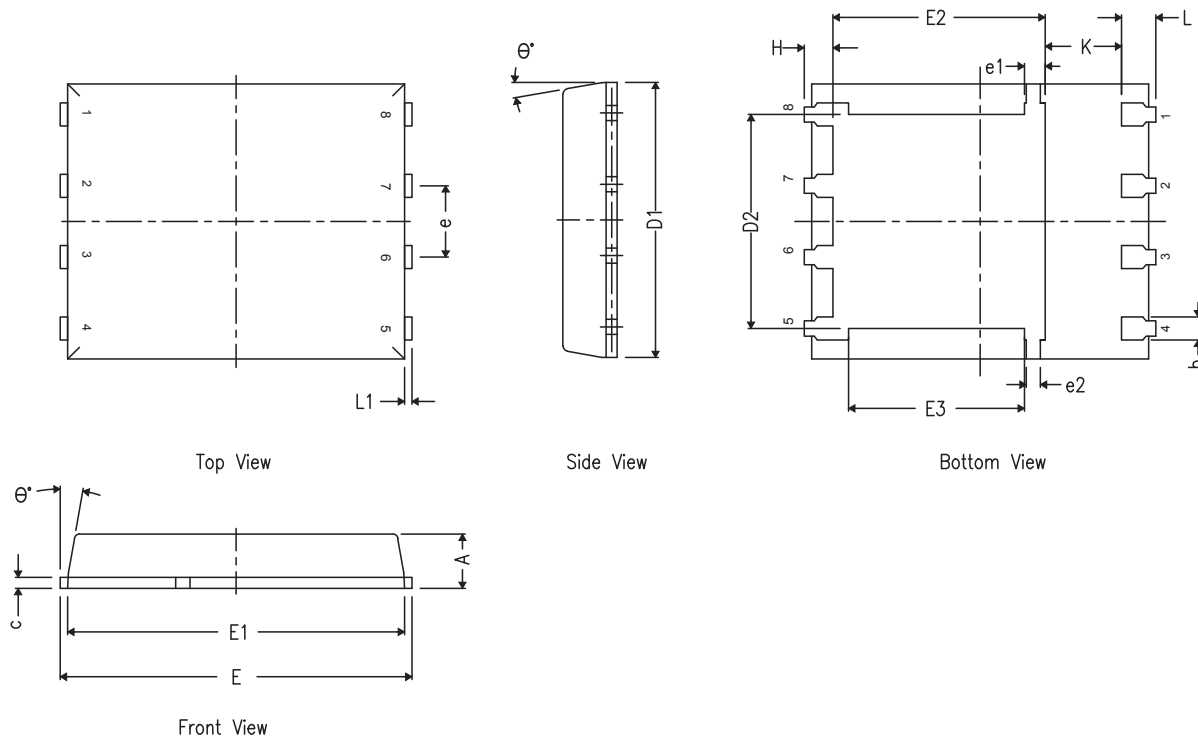
**SLYZ022** — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

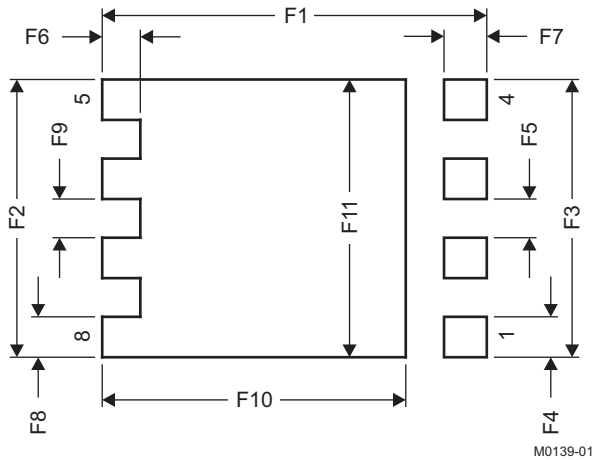
### 7.1 Q5A Package Dimensions



| DIM      | MILLIMETERS |      |      |
|----------|-------------|------|------|
|          | MIN         | NOM  | MAX  |
| A        | 0.90        | 1.00 | 1.10 |
| b        | 0.33        | 0.41 | 0.51 |
| c        | 0.20        | 0.25 | 0.34 |
| D1       | 4.80        | 4.90 | 5.00 |
| D2       | 3.61        | 3.81 | 4.02 |
| E        | 5.90        | 6.00 | 6.10 |
| E1       | 5.70        | 5.75 | 5.80 |
| E2       | 3.38        | 3.58 | 3.78 |
| E3       | 3.03        | 3.13 | 3.23 |
| e        | 1.17        | 1.27 | 1.37 |
| e1       | 0.27        | 0.37 | 0.47 |
| e2       | 0.15        | 0.25 | 0.35 |
| H        | 0.41        | 0.56 | 0.71 |
| K        | 1.10        | —    | —    |
| L        | 0.51        | 0.61 | 0.71 |
| L1       | 0.06        | 0.13 | 0.20 |
| $\theta$ | 0°          | —    | 12°  |



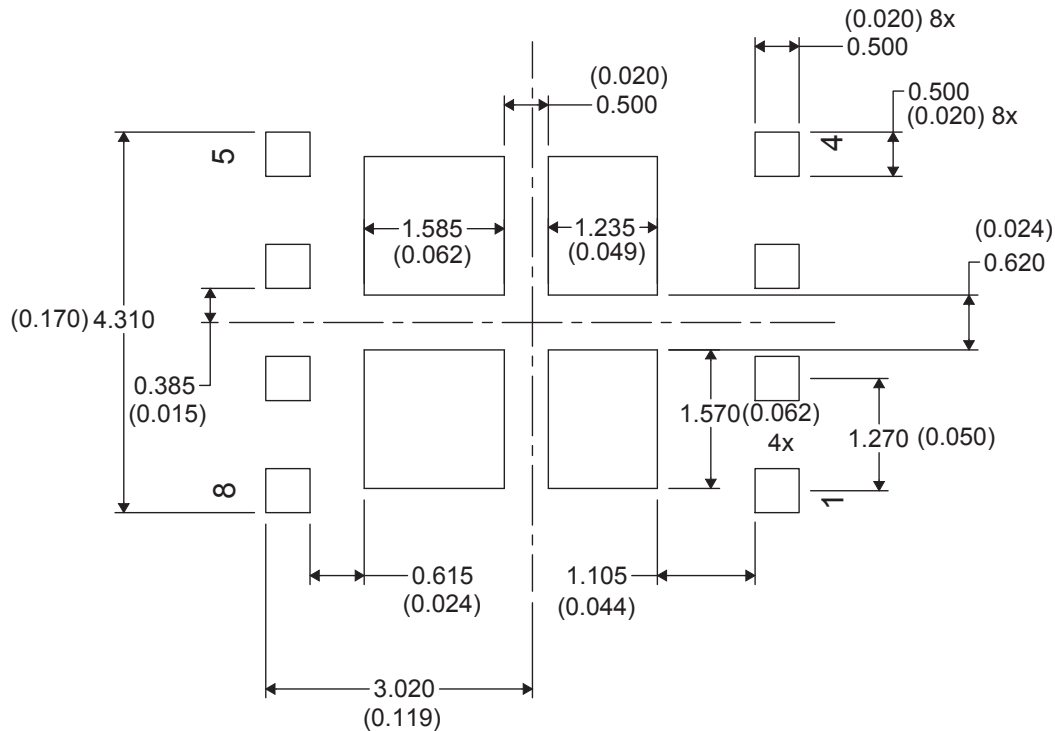
## 7.2 Recommended PCB Pattern



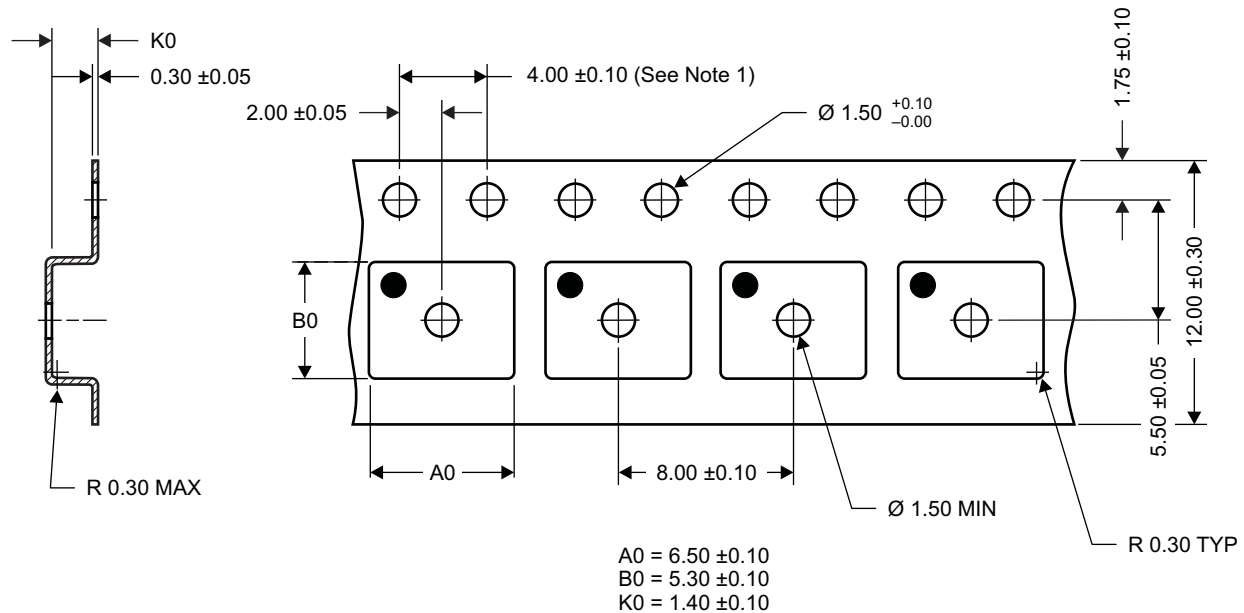
| DIM | MILLIMETERS |       | INCHES |       |
|-----|-------------|-------|--------|-------|
|     | MIN         | MAX   | MIN    | MAX   |
| F1  | 6.205       | 6.305 | 0.244  | 0.248 |
| F2  | 4.46        | 4.56  | 0.176  | 0.18  |
| F3  | 4.46        | 4.56  | 0.176  | 0.18  |
| F4  | 0.65        | 0.7   | 0.026  | 0.028 |
| F5  | 0.62        | 0.67  | 0.024  | 0.026 |
| F6  | 0.63        | 0.68  | 0.025  | 0.027 |
| F7  | 0.7         | 0.8   | 0.028  | 0.031 |
| F8  | 0.65        | 0.7   | 0.026  | 0.028 |
| F9  | 0.62        | 0.67  | 0.024  | 0.026 |
| F10 | 4.9         | 5     | 0.193  | 0.197 |
| F11 | 4.46        | 4.56  | 0.176  | 0.18  |

For recommended circuit layout for PCB designs, see [Reducing Ringing Through PCB Layout Techniques](#) (SLPA005).

### 7.3 Recommended Stencil Opening



### 7.4 Q5A Tape and Reel Information



M0138-01

#### Notes:

1. 10-sprocket hole-pitch cumulative tolerance  $\pm 0.2$ .
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm.
3. Material: black static-dissipative polystyrene.
4. All dimensions are in mm (unless otherwise specified).
5. A0 and B0 measured on a plane 0.3 mm above the bottom of the pocket.

## PACKAGING INFORMATION

| Orderable part number        | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">CSD18514Q5A</a>  | Active        | Production           | VSONP (DQJ)   8 | 2500   LARGE T&R      | ROHS Exempt | SN                                   | Level-1-260C-UNLIM                | -55 to 150   | CSD18514            |
| CSD18514Q5A.B                | Active        | Production           | VSONP (DQJ)   8 | 2500   LARGE T&R      | ROHS Exempt | SN                                   | Level-1-260C-UNLIM                | -55 to 150   | CSD18514            |
| <a href="#">CSD18514Q5AT</a> | Active        | Production           | VSONP (DQJ)   8 | 250   SMALL T&R       | ROHS Exempt | SN                                   | Level-1-260C-UNLIM                | -55 to 150   | CSD18514            |
| CSD18514Q5AT.B               | Active        | Production           | VSONP (DQJ)   8 | 250   SMALL T&R       | ROHS Exempt | SN                                   | Level-1-260C-UNLIM                | -55 to 150   | CSD18514            |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

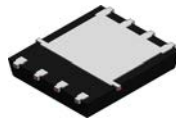
<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

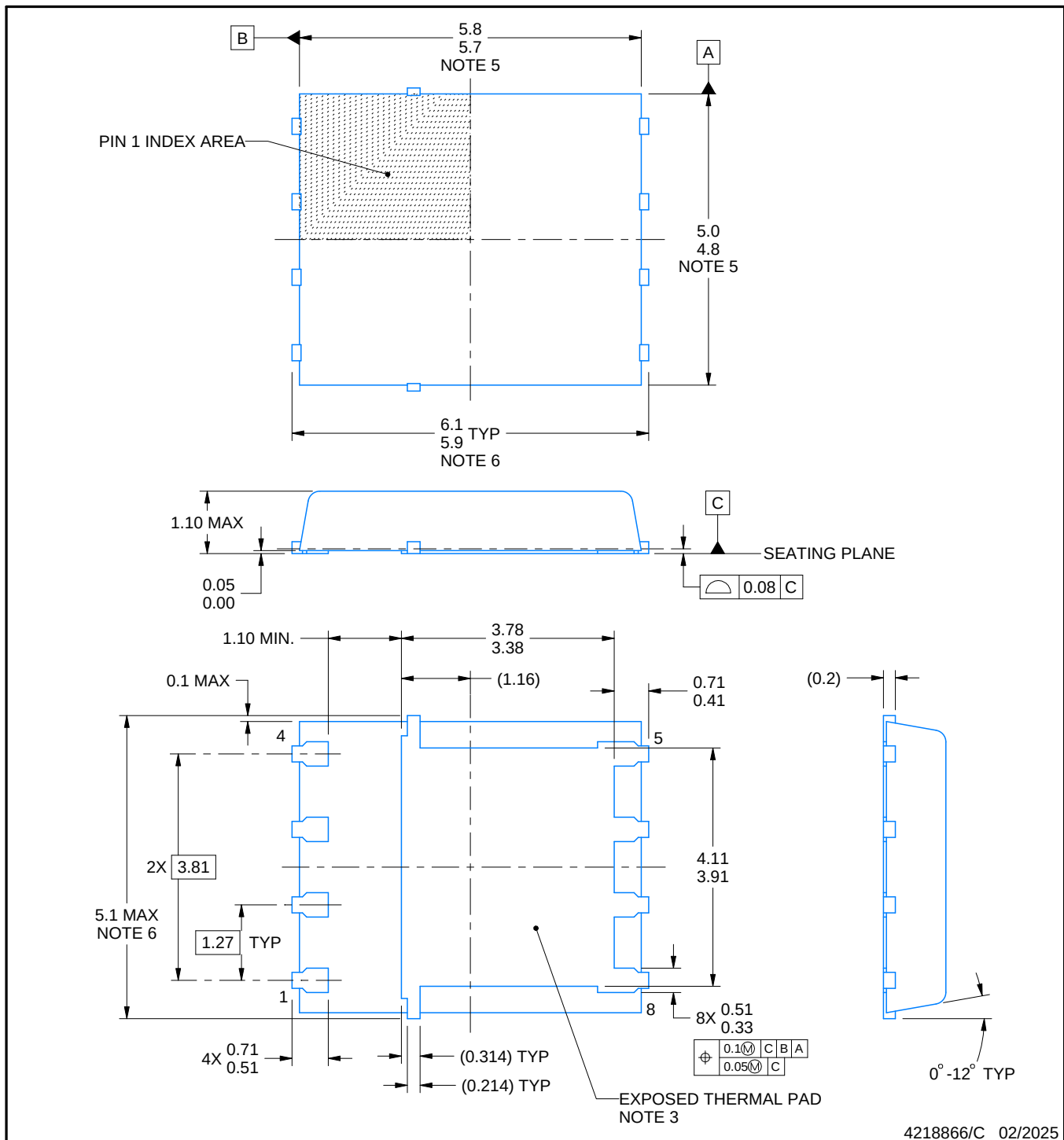
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**DQJ0008A****PACKAGE OUTLINE****VSONP - 1.1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD

**NOTES:**

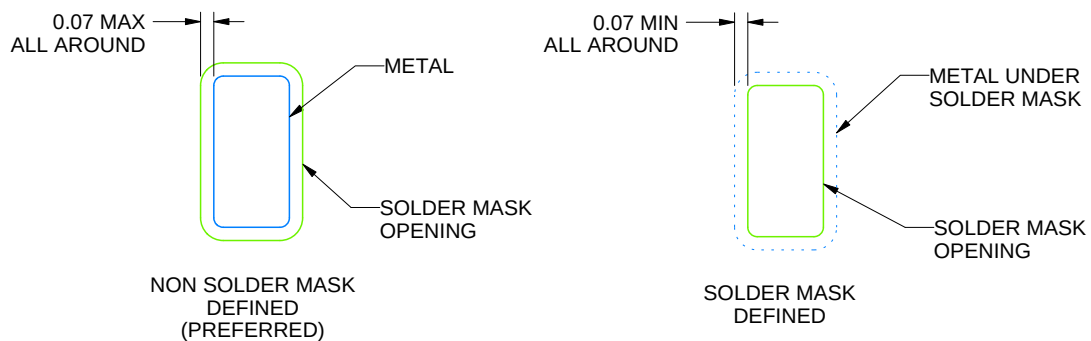
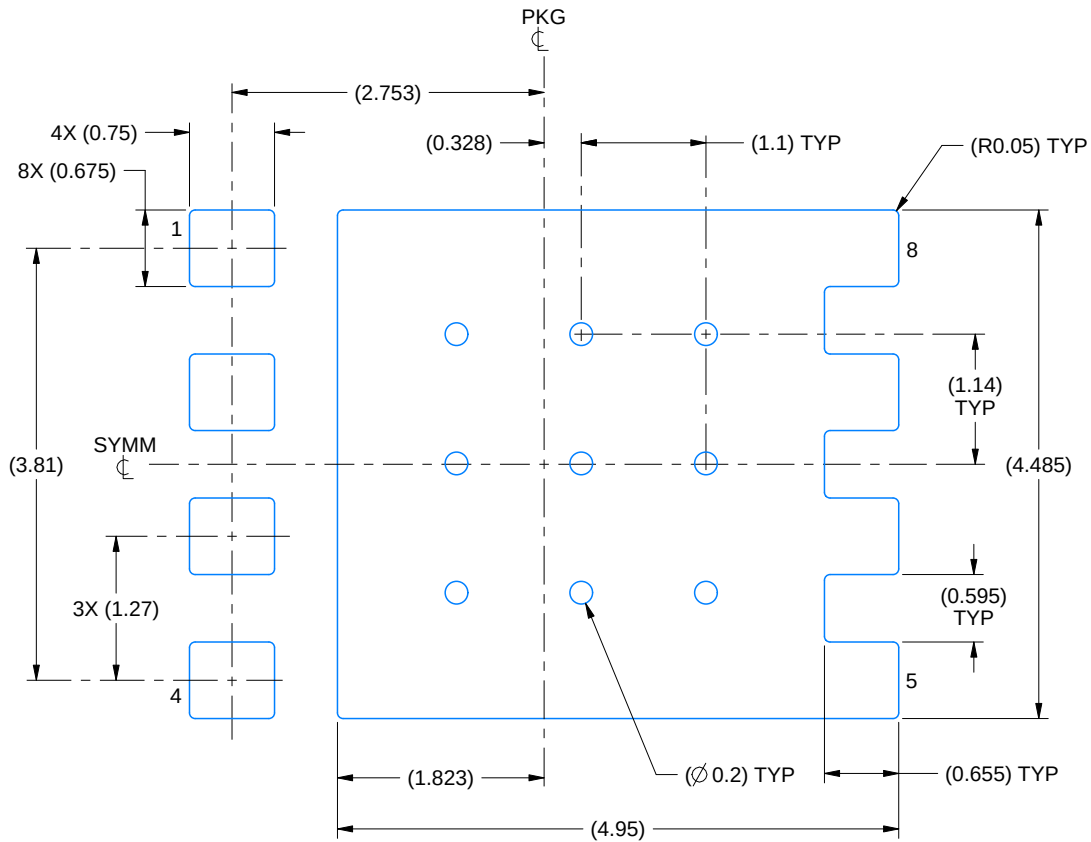
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Metalized features are supplier options and may not be on the package.
5. These dimensions do not include mold flash protrusions or gate burrs.
6. These dimensions include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25 mm per side.

# EXAMPLE BOARD LAYOUT

DQJ0008A

VSONP - 1.1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



## SOLDER MASK DETAILS

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NOTES: (continued)

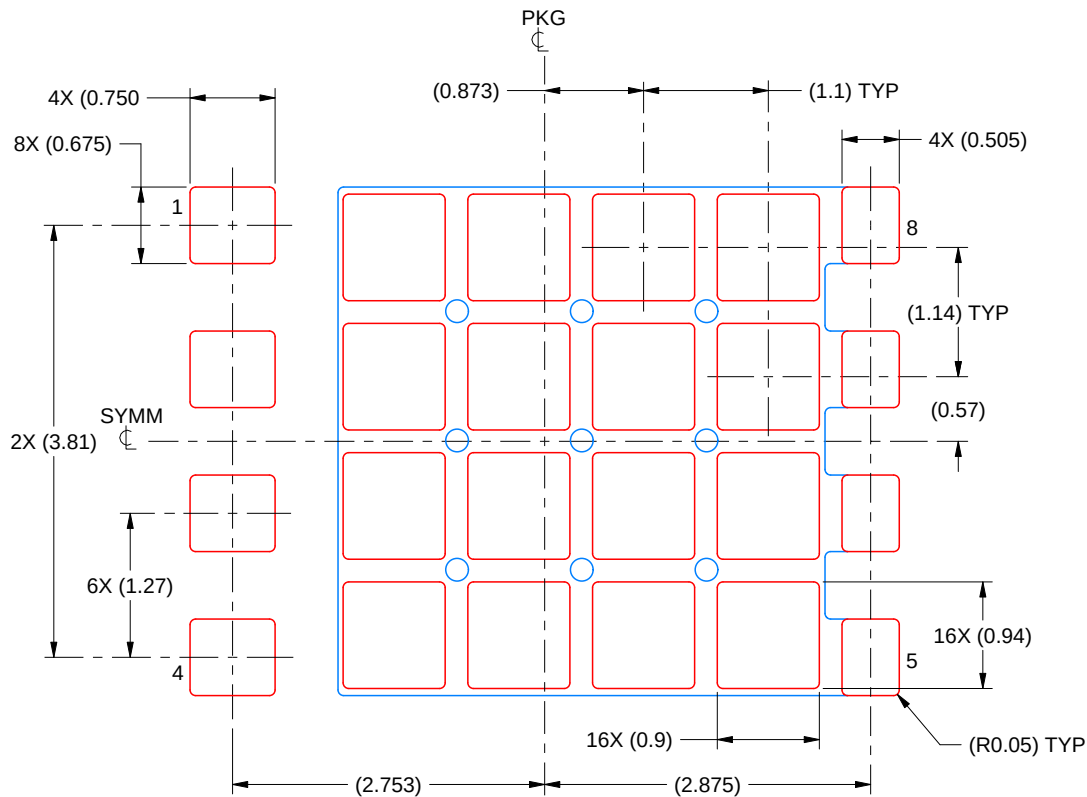
7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
8. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

# EXAMPLE STENCIL DESIGN

DQJ0008A

VSONP - 1.1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD:  
70% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE: 15X

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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