CSD18532Q5B 60V N-Channel NexFET™ Power MOSFETs

1 Features

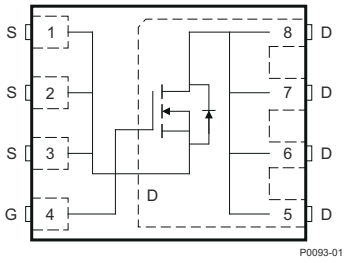
- Ultra-low Q_g and Q_{gd}
- Low thermal resistance
- Avalanche rated
- Logic level
- Lead-free terminal plating
- RoHS compliant
- Halogen free
- SON 5mm × 6mm plastic package

2 Applications

- DC-DC conversion
- Secondary side synchronous rectifier
- Isolated converter primary side switch
- Motor control

3 Description

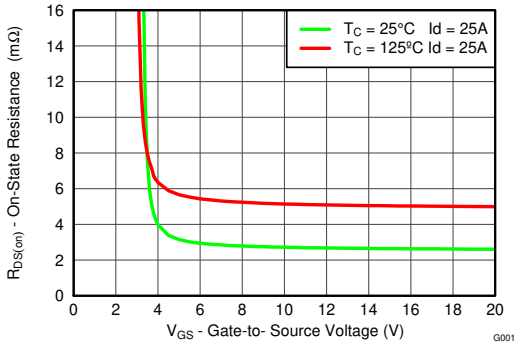
This 2.5mΩ, 60V SON 5mm × 6mm NexFET™ power MOSFET is designed to minimize losses in power conversion applications.



Top View

Product Summary

T_A = 25°C		TYPICAL VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	60	V
Q_g	Gate Charge Total (10V)	44	nC
Q_{gd}	Gate Charge Gate-to-Drain	6.9	nC



$R_{DS(on)}$ vs V_{GS}

Product Summary (continued)

T_A = 25°C		TYPICAL VALUE		UNIT
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 4.5V	3.3	mΩ
		V_{GS} = 10V	2.5	
$V_{GS(th)}$	Threshold Voltage	1.8		V

Package Information

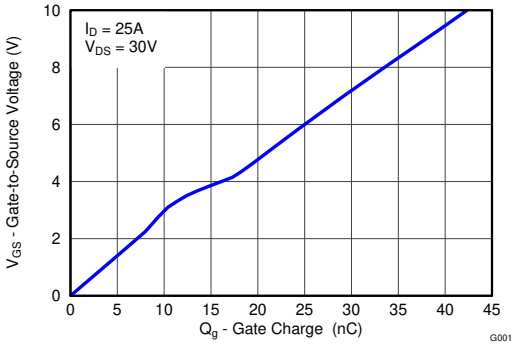
DEVICE	QTY	MEDIA	PACKAGE(1) (2)	SHIP
CSD18532Q5B	2500	13-Inch Reel	SON 5.00mm × 6.00mm Plastic Package	Tape and Reel
CSD18532Q5BT	250	13-Inch Reel		

(1) For all available packages, see the orderable addendum at the end of the datasheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	60	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current (Package Limited)	100	A
	Continuous Drain Current (Silicon Limited), T_C = 25°C	172	
	Continuous Drain Current(1)	23	
I_{DM}	Pulsed Drain Current(2)	400	A
P_D	Power Dissipation(1)	3.2	W
	Power Dissipation, T_C = 25°C	156	
T_J	Operating Junction Temperature	–55 to 150	°C
T_{stg}	Storage Temperature		
E_{AS}	Avalanche Energy, Single Pulse I_D = 80A, L = 0.1mH, R_G = 25Ω	320	mJ

(1) Typical $R_{\theta JA}$ = 40°C/W on a 1-in^2, 2oz Cu pad on a 0.06-in thick FR4 PCB.
(2) Maximum $R_{\theta JC}$ = 0.8°C/W, pulse duration ≤ 100 µs, duty cycle ≤ 1%.



Gate Charge

Table of Contents

4 Specifications

4.1 Electrical Characteristics

T_A = 25°C unless otherwise stated

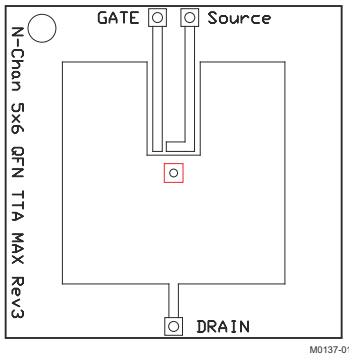
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0V, I_D = 250µA	60			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0V, V_{DS} = 48V			1	µA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0V, V_{GS} = 20V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	1.5	1.8	2.2	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 4.5V, I_D = 25A		3.3	4.3	mΩ
		V_{GS} = 10V, I_D = 25A		2.5	3.2	
g_{fs}	Transconductance	V_{DS} = 30V, I_D = 25A		143		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0V, V_{DS} = 30V, f = 1MHz		3900	5070	pF
C_{oss}	Output capacitance			470	611	pF
C_{rss}	Reverse transfer capacitance			13	17	pF
R_G	Series gate resistance			1.2	2.4	Ω
Q_g	Gate charge total (10V)	V_{DS} = 30V, I_D = 25A		44	58	nC
Q_{gd}	Gate charge gate-to-drain			6.9		nC
Q_{gs}	Gate charge gate-to-source			10		nC
$Q_{g(th)}$	Gate charge at V_{th}			6.3		nC
Q_{oss}	Output charge	V_{DS} = 30V, V_{GS} = 0V		52		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 30V, V_{GS} = 10V, I_{DS} = 25A, R_G = 0 Ω		5.8		ns
t_r	Rise time			7.2		ns
$t_{d(off)}$	Turnoff delay time			22		ns
t_f	Fall time			3.1		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 25A, V_{GS} = 0V		0.8	1	V
Q_{rr}	Reverse recovery charge	V_{DS} = 30V, I_F = 25A, di/dt = 300A/µs		111		nC
t_{rr}	Reverse recovery time			49		ns

4.2 Thermal Information

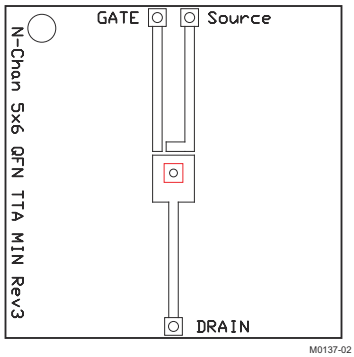
T_A = 25°C unless otherwise stated

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance(1)			0.8	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1) (2)			50	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1in^2 (6.45cm^2), 2oz. (0.071mm) thick Cu pad on a 1.5in × 1.5in (3.81cm × 3.81cm), 0.06in (1.52mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1in^2 (6.45cm^2), 2oz (0.071mm) thick Cu.



Maximum $R_{\theta JA}$ = 50°C/W when mounted on 1 in^2 (6.45cm^2) of 2oz (0.071mm) thick Cu.



Maximum $R_{\theta JA}$ = 125°C/W when mounted on a minimum pad area of 2oz (0.071mm) thick Cu.

4.3 Typical MOSFET Characteristics

T_A = 25°C unless otherwise stated

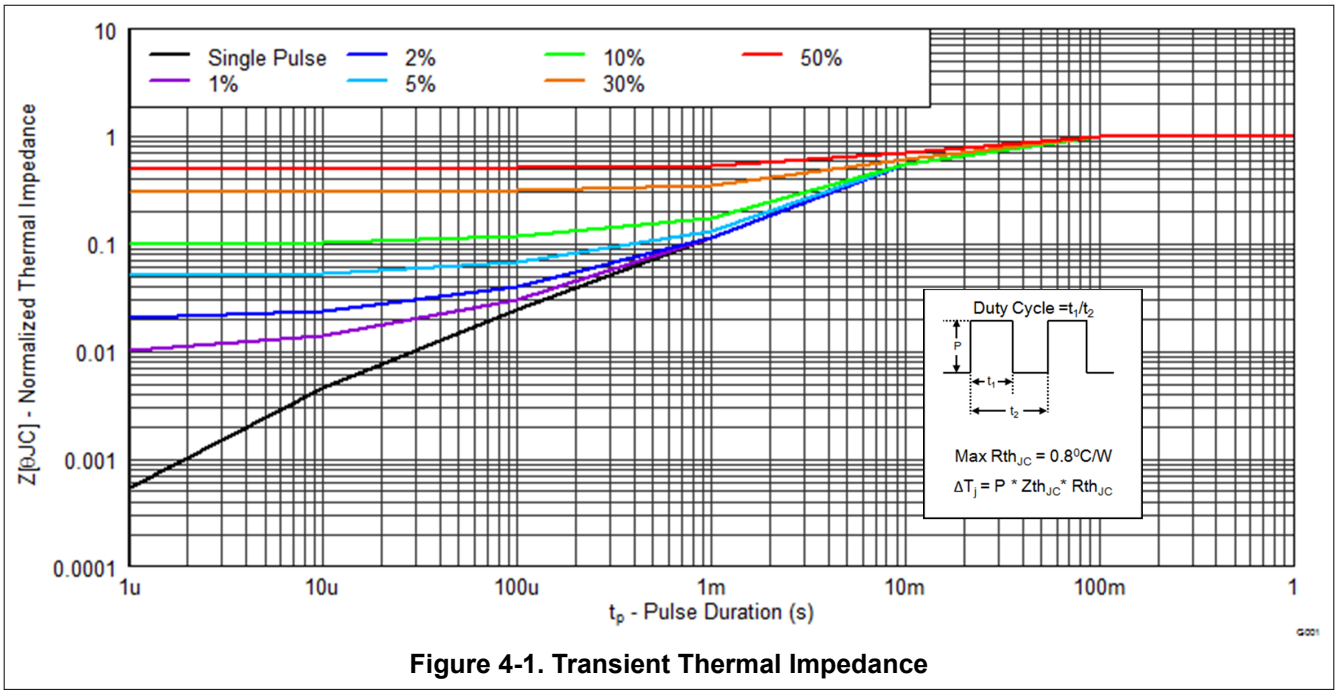


Figure 4-1. Transient Thermal Impedance

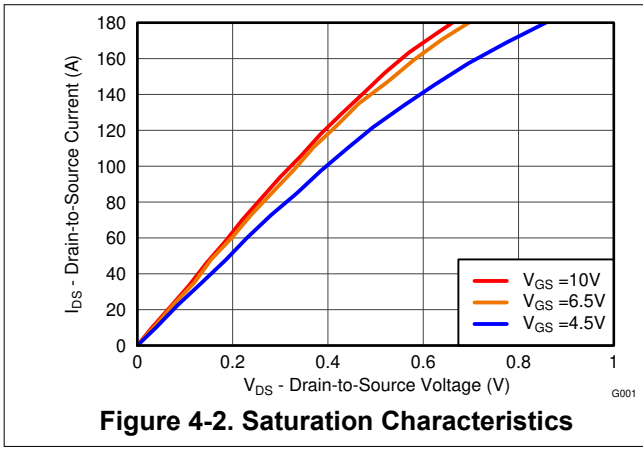


Figure 4-2. Saturation Characteristics

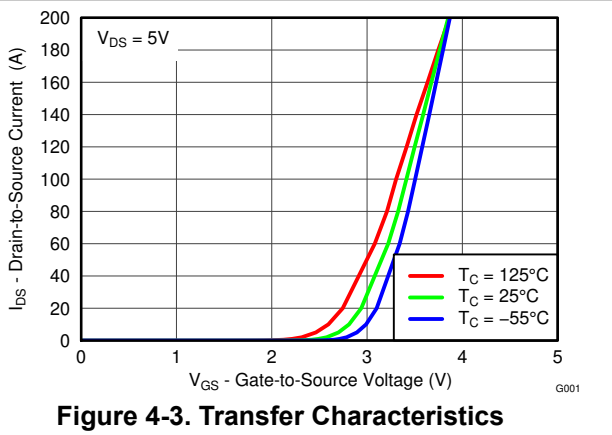


Figure 4-3. Transfer Characteristics

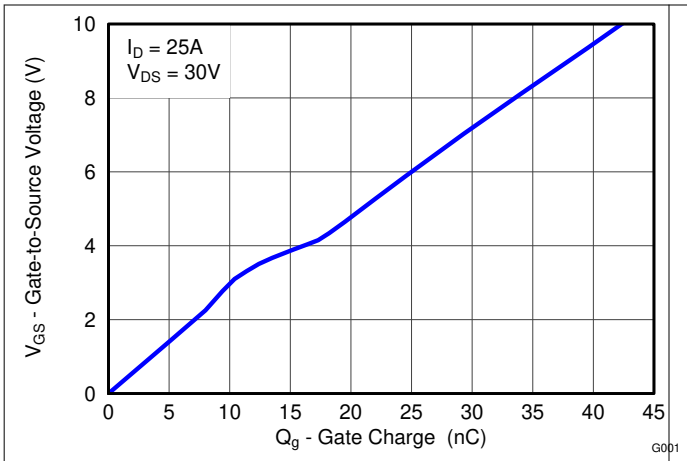


Figure 4-4. Gate Charge

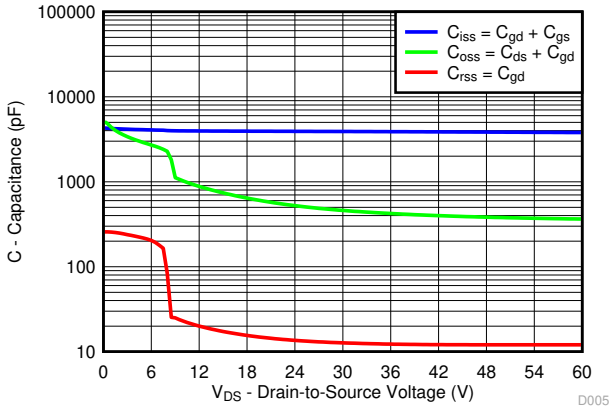


Figure 4-5. Capacitance

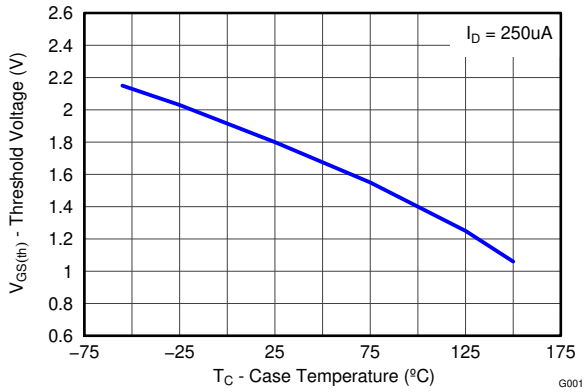


Figure 4-6. Threshold Voltage vs Temperature

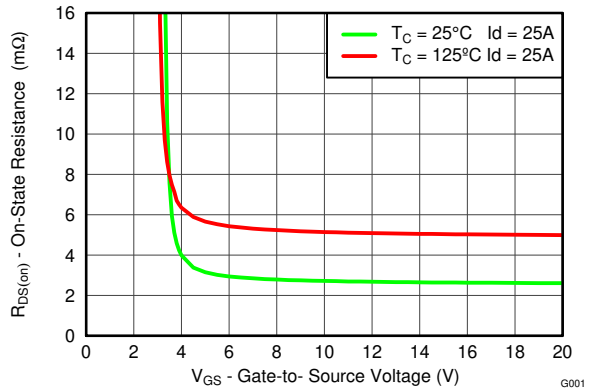


Figure 4-7. On-State Resistance vs Gate-to-Source Voltage

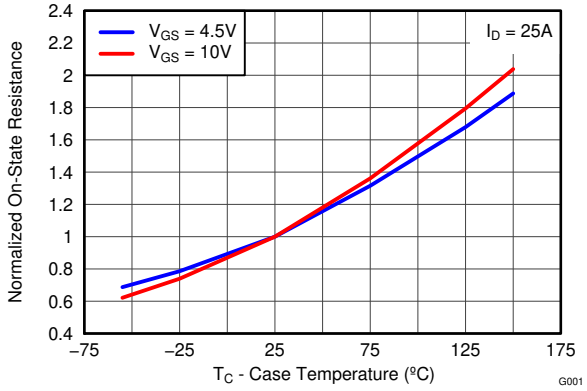


Figure 4-8. Normalized On-State Resistance vs Temperature

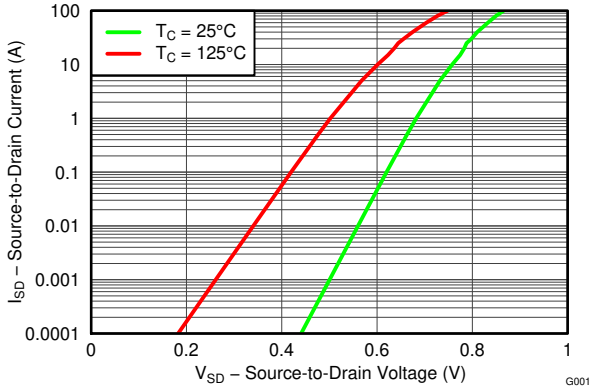


Figure 4-9. Typical Diode Forward Voltage

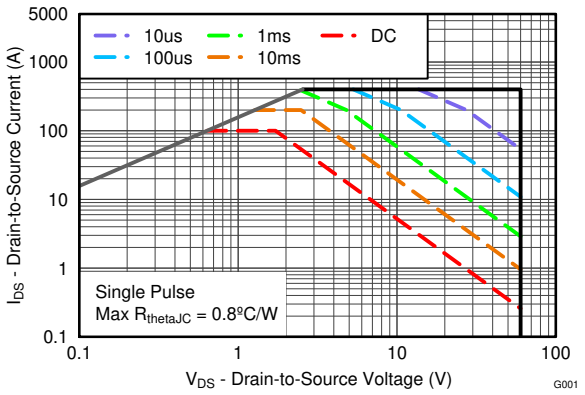


Figure 4-10. Maximum Safe Operating Area

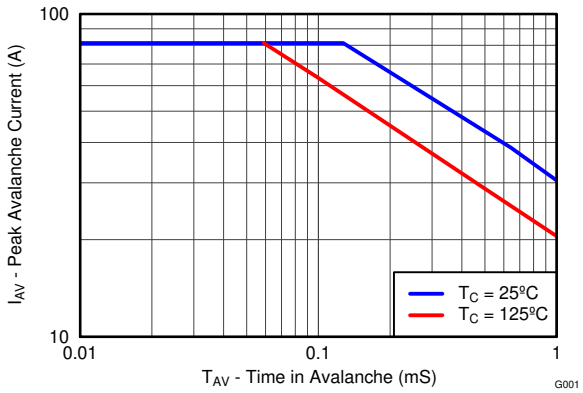


Figure 4-11. Single Pulse Unclamped Inductive Switching

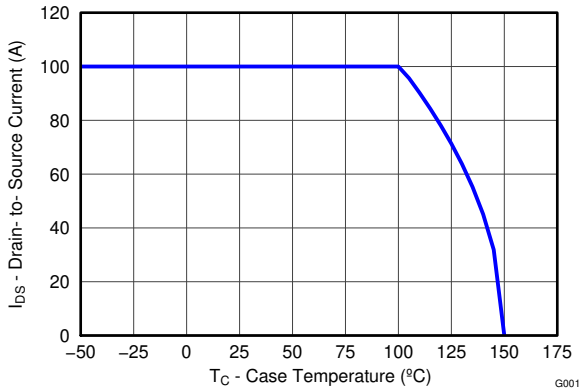


Figure 4-12. Maximum Drain Current vs Temperature

5 Device and Documentation Support

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5.2 Documentation Support

5.2.1 Related Documentation

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (February 2018) to Revision E (July 2026)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

Changes from Revision C (May 2017) to Revision D (February 2018)	Page
• Extended the V_{DS} on Figure 4-5 to 60V	4

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD18532Q5B	Active	Production	VSON-CLIP (DNK) | 8	2500 | LARGE T&R	ROHS Exempt	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 150	CSD18532
CSD18532Q5B.B	Active	Production	VSON-CLIP (DNK) | 8	2500 | LARGE T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	CSD18532
CSD18532Q5BG4	Active	Production	VSON-CLIP (DNK) | 8	2500 | LARGE T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	CSD18532
CSD18532Q5BG4.B	Active	Production	VSON-CLIP (DNK) | 8	2500 | LARGE T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	CSD18532
CSD18532Q5BT	Active	Production	VSON-CLIP (DNK) | 8	250 | SMALL T&R	ROHS Exempt	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 150	CSD18532
CSD18532Q5BT.B	Active	Production	VSON-CLIP (DNK) | 8	250 | SMALL T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	CSD18532

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

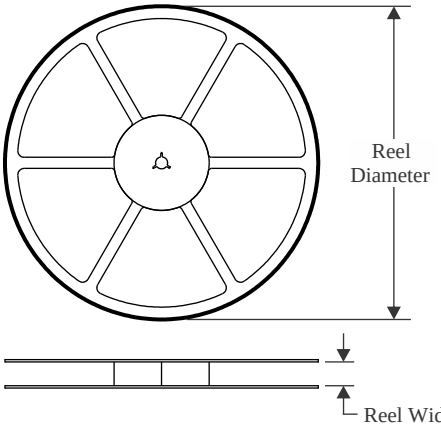
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

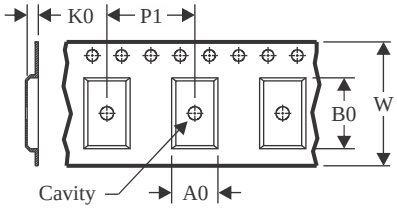
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

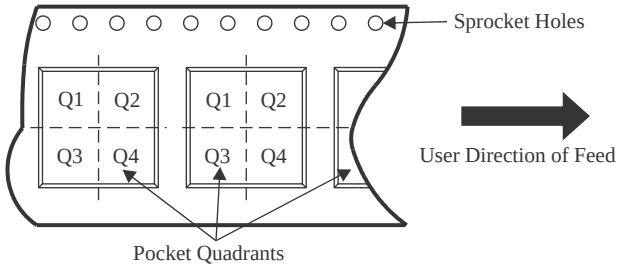


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

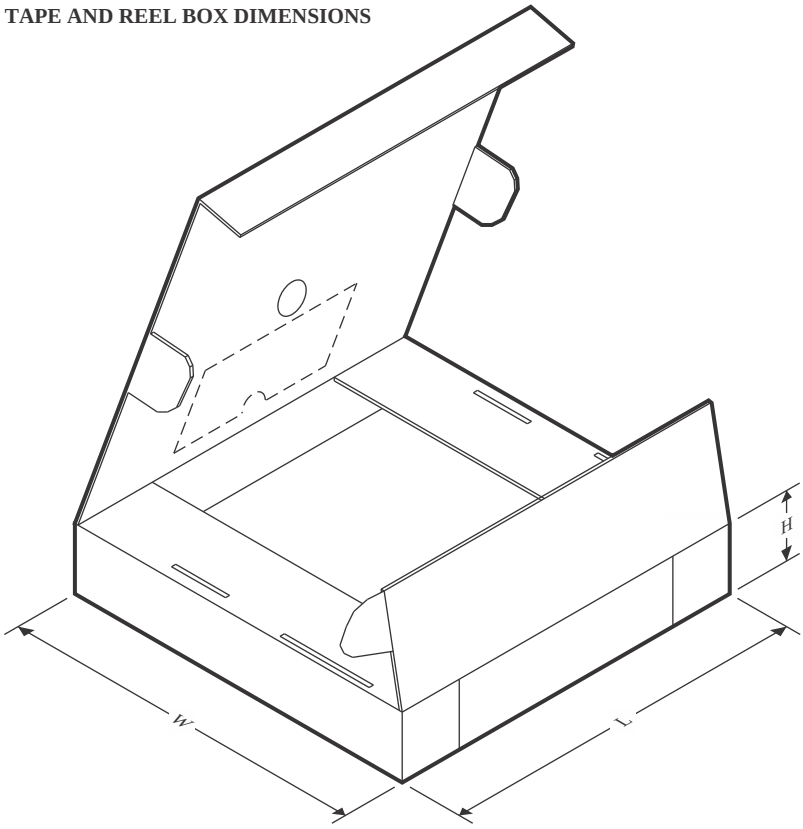
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD18532Q5B	VSON-CLIP	DNK	8	2500	330.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1
CSD18532Q5BG4	VSON-CLIP	DNK	8	2500	330.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1
CSD18532Q5BT	VSON-CLIP	DNK	8	250	180.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

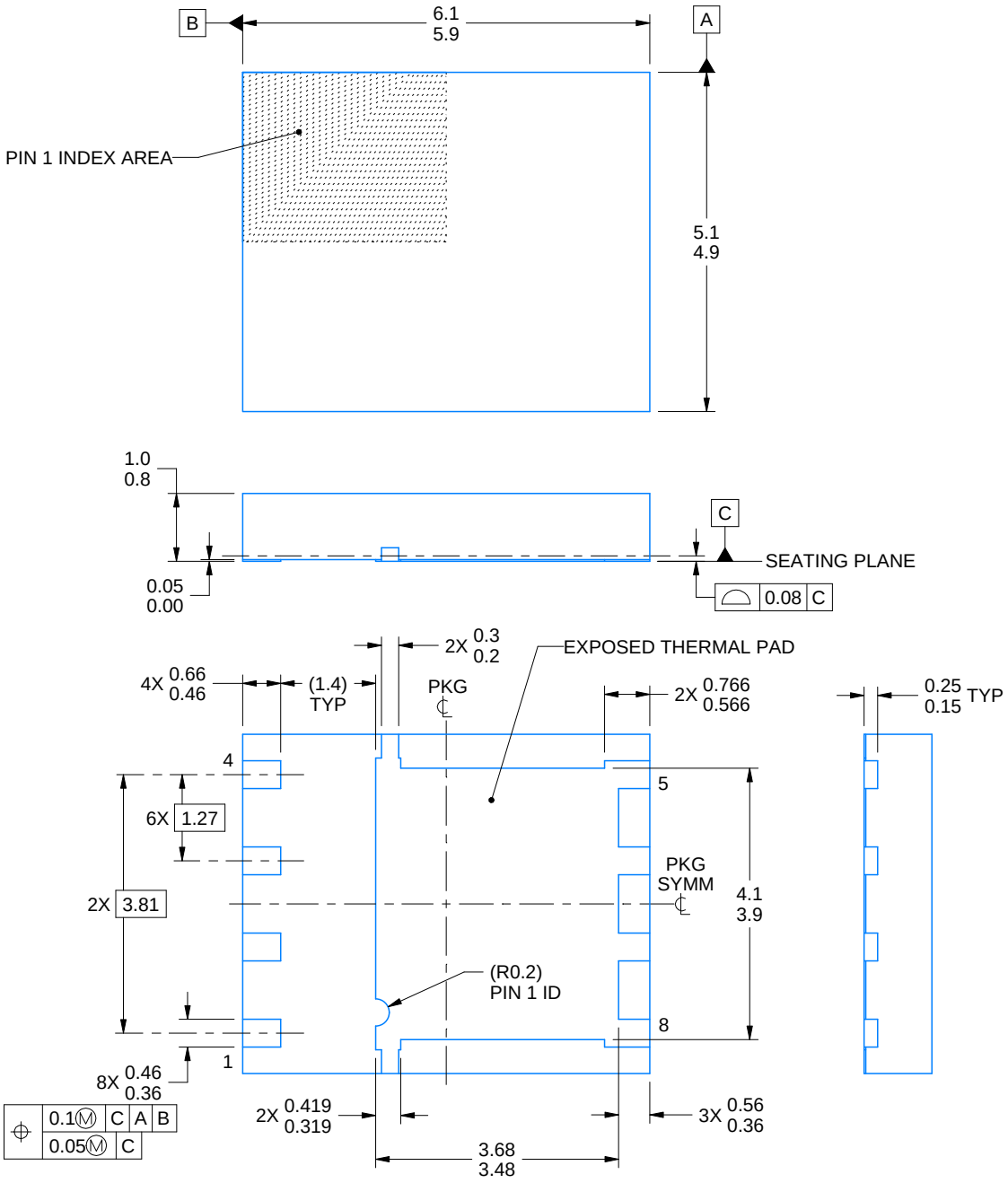
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD18532Q5B	VSON-CLIP	DNK	8	2500	346.0	346.0	33.0
CSD18532Q5BG4	VSON-CLIP	DNK	8	2500	346.0	346.0	33.0
CSD18532Q5BT	VSON-CLIP	DNK	8	250	182.0	182.0	20.0

PACKAGE OUTLINE

DNK0008A

VSON-CLIP - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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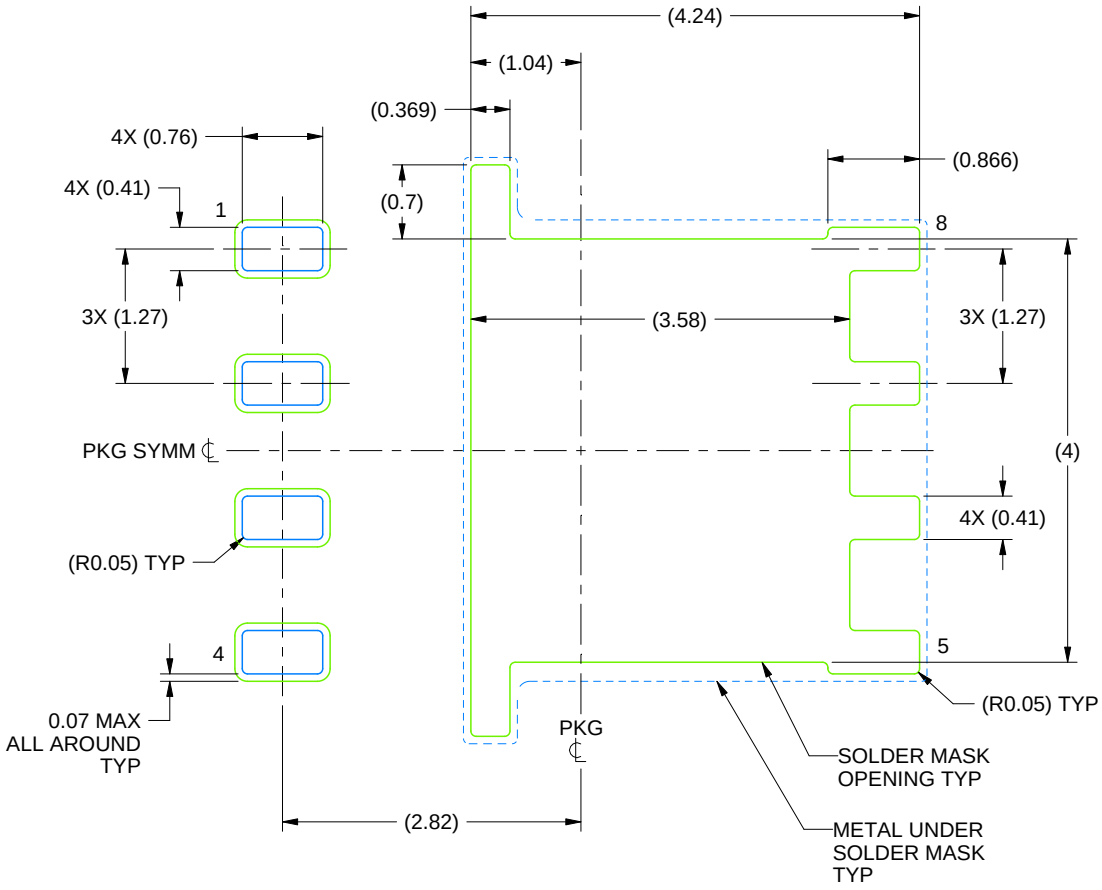
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE: 14X

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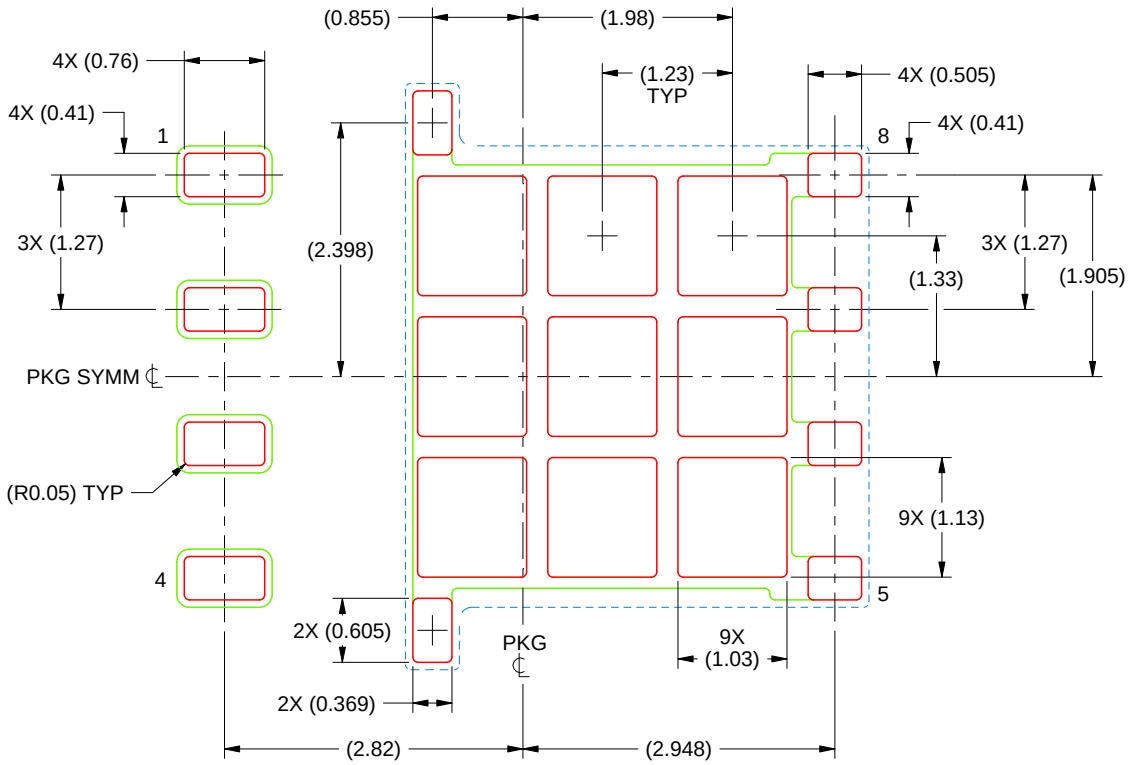
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 14X

74% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025