CSD25481F4 20 V P-Channel FemtoFET™ MOSFET

1 Features

- Ultra-low on resistance
- Ultra-low Q_g and Q_{gd}
- High operating drain current
- Ultra-small footprint (0402 Case Size)
  - 1 mm × 0.6 mm
- Ultra-low profile
  - 0.36 mm max height
- Integrated ESD protection diode
  - Rated >4 kV HBM
  - Rated >2 kV CDM
- Lead and halogen free
- RoHS compliant

2 Applications

- Optimized for load switch applications
- Optimized for general purpose switching applications
- Battery applications
- Handheld and mobile applications

3 Description

This 90-mΩ, 20-V P-Channel FemtoFET™ MOSFET is designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small signal MOSFETs while providing at least a 60% reduction in footprint size.

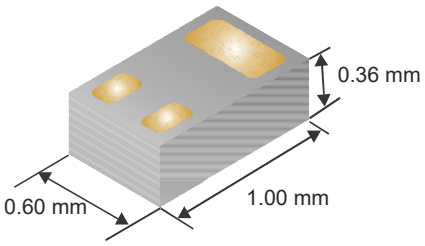


Figure 3-1. Typical Part Dimensions

Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	–20		V
Q_g	Gate Charge Total (–4.5 V)	913		pC
Q_{gd}	Gate Charge Gate-to-Drain	153		pC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = –1.8 V	395	mΩ
		V_{GS} = –2.5 V	145	mΩ
		V_{GS} = –4.5 V	90	mΩ
$V_{GS(th)}$	Threshold Voltage	–0.95		V

Ordering Information

Device(1)	Qty	Media	Package	Ship
CSD25481F4	3000	7-Inch Reel	Femto(0402) 1.0 mm × 0.6 mm Land Grid Array (LGA)	Tape and Reel
CSD25481F4T	250	7-Inch Reel		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

T_A = 25°C unless otherwise stated		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	–20	V
V_{GS}	Gate-to-Source Voltage	–12	V
I_D	Continuous Drain Current(1)	–2.5	A
I_{DM}	Pulsed Drain Current(2)	–13.1	A
I_G	Continuous Gate Clamp Current	–35	mA
	Pulsed Gate Clamp Current(2)	–350	
P_D	Power Dissipation(1)	500	mW
$V_{(ESD)}$	Human Body Model (HBM)	4	kV
	Charged Device Model (CDM)	2	kV
T_J, T_{stg}	Operating Junction and Storage Temperature Range	–55 to 150	°C

(1) Typical $R_{\theta JA}$ = 90°C/W on 1 inch^2 (6.45 cm^2), 2 oz. (0.071 mm thick) Cu pad on a 0.06 inch (1.52 mm) thick FR4 PCB.

(2) Pulse duration ≤ 100 µs, duty cycle ≤ 1%.

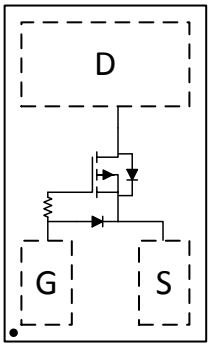


Figure 3-2. Top View

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Revision History....2
5 Specifications....3
5.1 Electrical Characteristics....3
5.2 Thermal Information....3
5.3 Typical MOSFET Characteristics....4
6 Device and Documentation Support....7
6.1 Support Resources....7
6.2 Trademarks....7
6.3 Electrostatic Discharge Caution....7
6.4 Glossary....7
7 Mechanical, Packaging, and Orderable Information....8
7.1 Mechanical Dimensions....8
7.2 Recommended Minimum PCB Layout....9
7.3 Recommended Stencil Pattern....9

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (December 2017) to Revision F (February 2022)	Page
• Changed ultra-low profile bullet from 0.35 mm to 0.36 mm in height	1
• Updated ultra-low profile image height from 0.35 mm to 0.36 mm	1
• Changed ultra-low profile image height from 0.35 mm to 0.36 mm	8
• Added FemtoFET Surface Mount Guide note	9

Changes from Revision D (October 2014) to Revision E (December 2017)	Page
• Changed the Pulsed Drain Current value From: –10 A To: –13.1 A in the *Absolute Maximum Ratings* table	1
• Changed Note 1 From: Typical $R_{\theta JA}$ = 85°C/W To: Typical $R_{\theta JA}$ = 90°C/W	1
• Changed Note 2 From: Pulse duration ≤ 300 µs, duty cycle ≤ 2% To: Pulse duration ≤ 100 µs, duty cycle ≤ 1%	1
• Changed the typical $R_{\theta JA}$ values in the *Thermal Information* table	3
• Updated Figure 5-1.	4
• Updated Figure 5-10 with newly measured data.	4
• Updated all mechanical drawings, increased the size of the pads in the *Section 7.3* section.	8

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_{DS} = –250 µA	–20			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = –16 V			–100	nA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = –12 V			–50	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = –250 µA	–0.7	–0.95	–1.2	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = –1.8 V, I_{DS} = –0.1 A		395	800	mΩ
		V_{GS} = –2.5 V, I_{DS} = –0.5 A		145	174	mΩ
		V_{GS} = –4.5 V, I_{DS} = –0.5 A		90	105	mΩ
		V_{GS} = –8 V, I_{DS} = –0.5 A		75	88	mΩ
g_{fs}	Transconductance	V_{DS} = –10 V, I_{DS} = –0.5 A		3.3		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = –10 V, f = 1 MHz		189		pF
C_{oss}	Output Capacitance			78		pF
C_{rss}	Reverse Transfer Capacitance			5.5		pF
R_G	Series Gate Resistance			20		Ω
Q_g	Gate Charge Total (4.5 V)	V_{DS} = –10 V, I_{DS} = –0.5 A		913		pC
Q_{gd}	Gate Charge Gate-to-Drain			153		pC
Q_{gs}	Gate Charge Gate-to-Source			240		pC
$Q_{g(th)}$	Gate Charge at V_{th}			116		pC
Q_{oss}	Output Charge	V_{DS} = –10 V, V_{GS} = 0 V		1030		pC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = –10 V, V_{GS} = –4.5 V, I_{DS} = –0.5 A,R_G = 2 Ω		4.1		ns
t_r	Rise Time			3.6		ns
$t_{d(off)}$	Turn Off Delay Time			16.9		ns
t_f	Fall Time			6.7		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_{SD} = –0.5 A, V_{GS} = 0 V		–0.75		V
Q_{rr}	Reverse Recovery Charge	V_{DS}= –10 V, I_F = –0.5 A, di/dt = 100 A/µs		1010		pC
t_{rr}	Reverse Recovery Time			7.5		ns

5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

THERMAL METRIC		TYPICAL VALUES	UNIT
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance(1)	90	°C/W
	Junction-to-Ambient Thermal Resistance(2)	250	

(1) Device mounted on FR4 material with 1 $inch^2$ (6.45 cm^2), 2 oz. (0.071 mm thick) Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

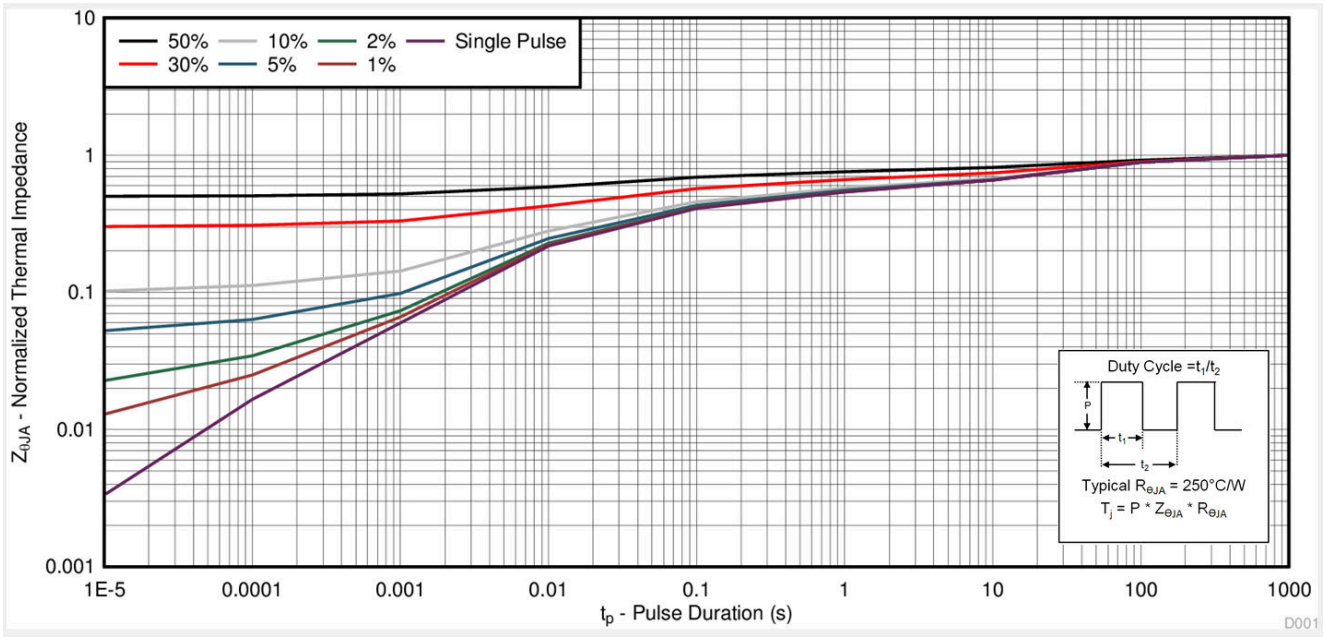


Figure 5-1. Transient Thermal Impedance

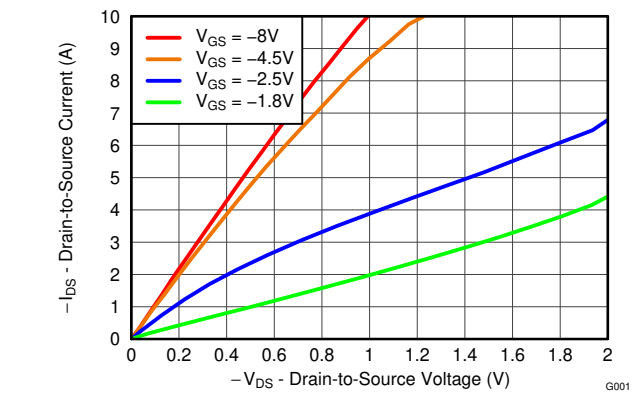


Figure 5-2. Saturation Characteristics

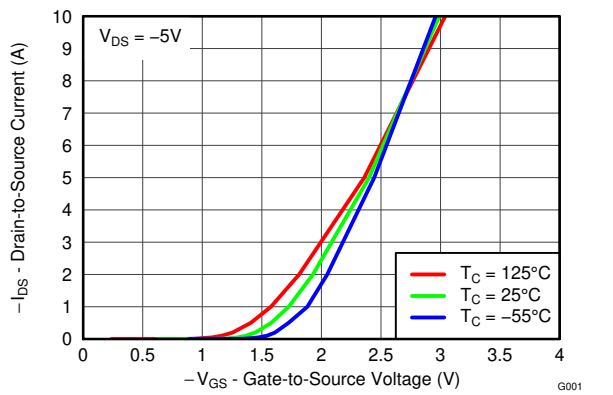


Figure 5-3. Transfer Characteristics

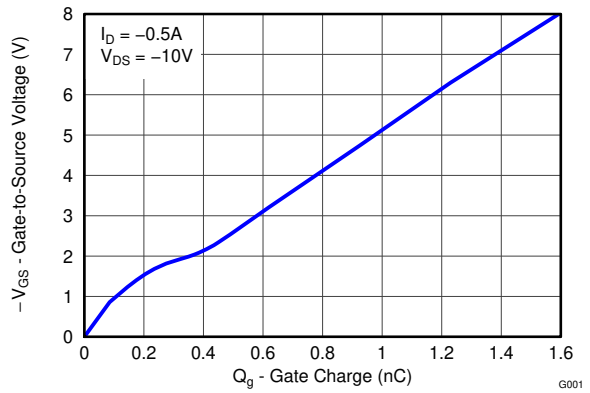


Figure 5-4. Gate Charge

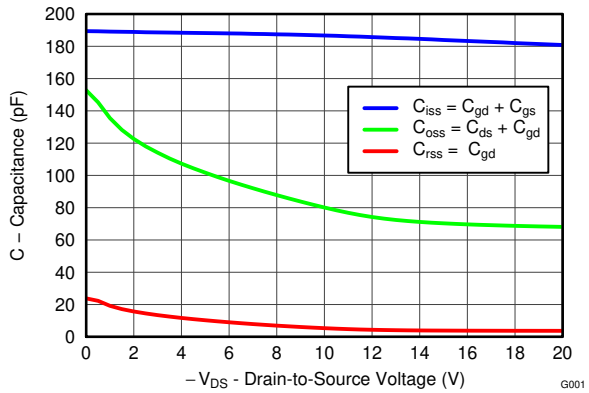


Figure 5-5. Capacitance

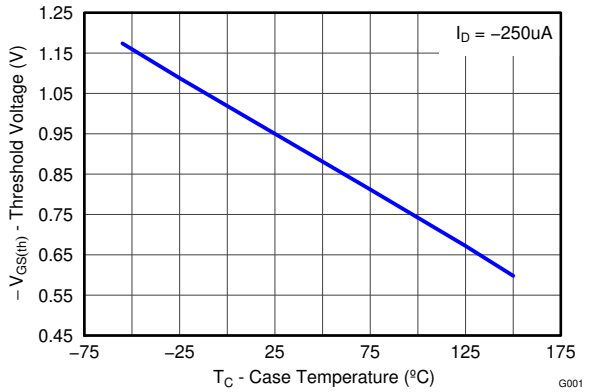


Figure 5-6. Threshold Voltage vs Temperature

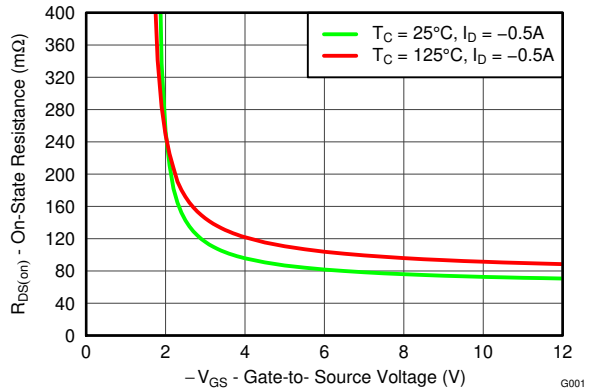


Figure 5-7. On-State Resistance vs Gate-to-Source Voltage

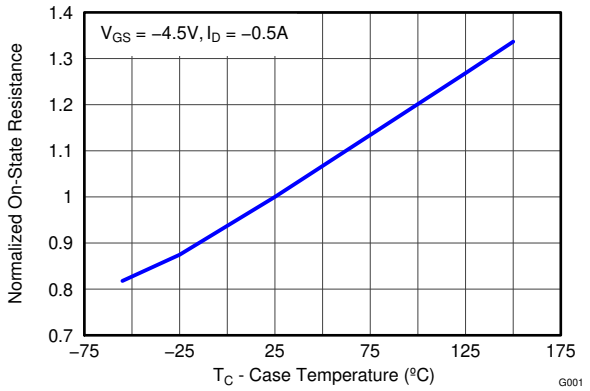


Figure 5-8. Normalized On-State Resistance vs Temperature

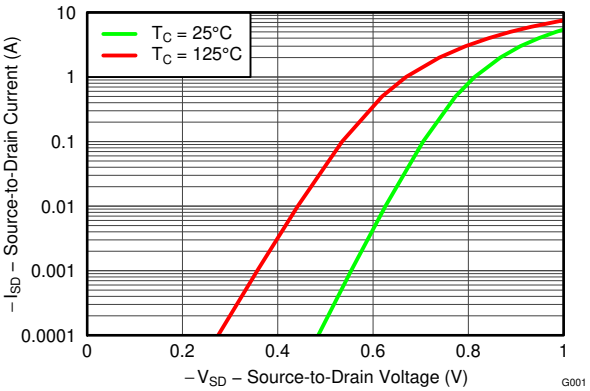
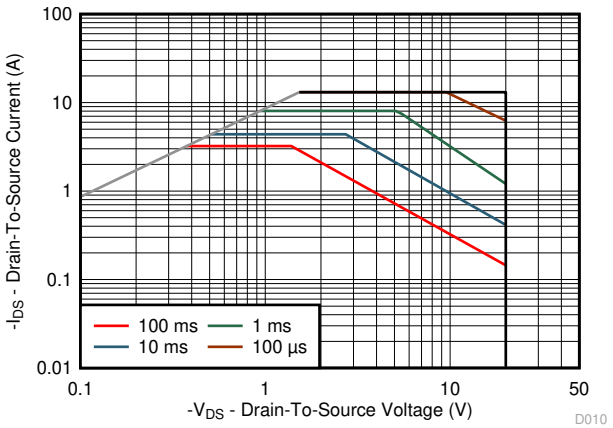
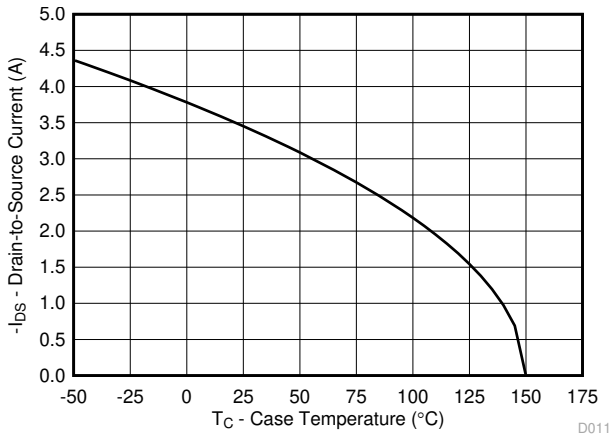


Figure 5-9. Typical Diode Forward Voltage



Single Pulse Typical $R_{\theta JA}$ =250°C/W (min Cu)

Figure 5-10. Maximum Safe Operating Area



Typical $R_{\theta JA}$ = 90°C/W (max Cu)

Figure 5-11. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

6.2 Trademarks

FemtoFET™ is a trademark of Texas Instruments.
TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

6.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

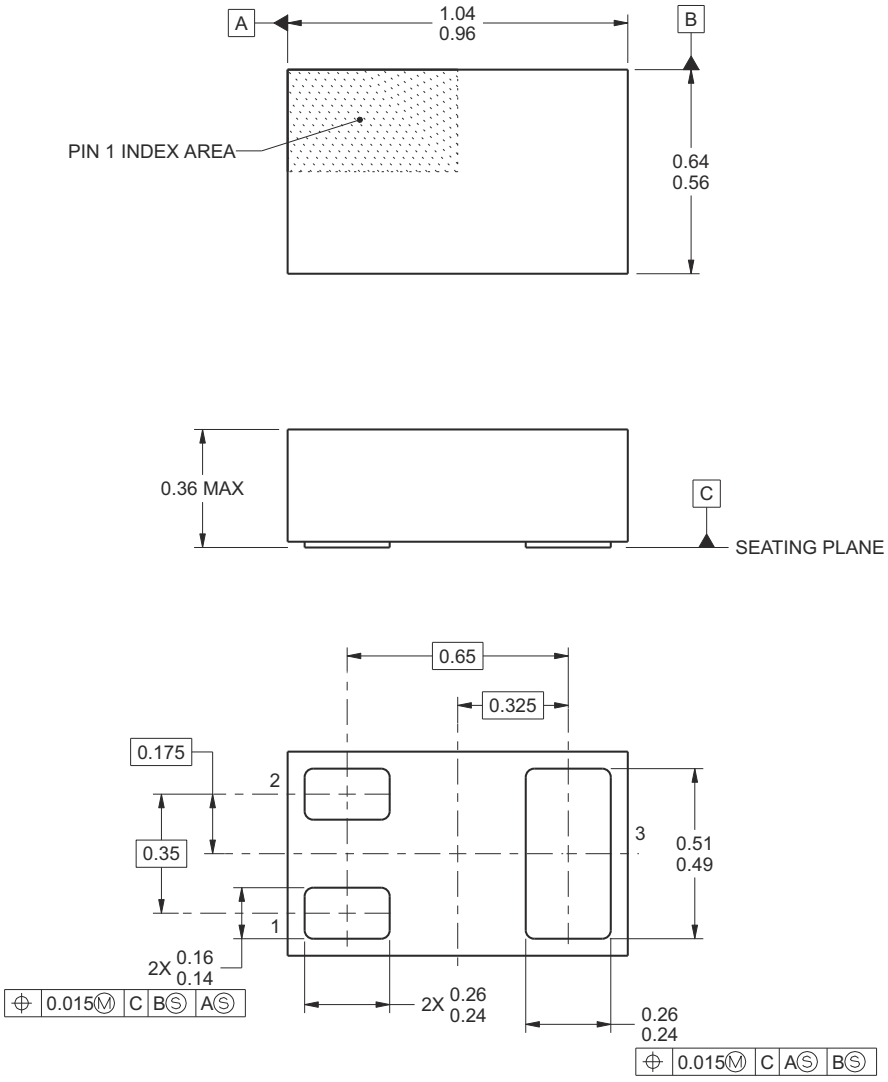
6.4 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Mechanical Dimensions



A. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

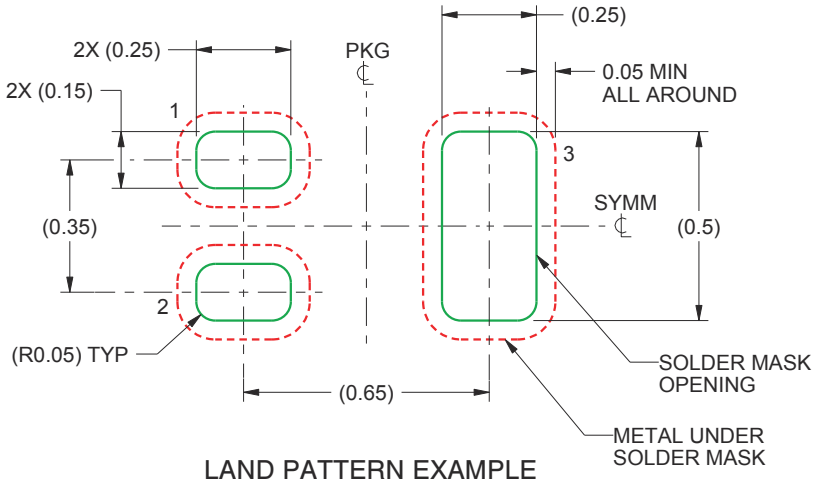
B. This drawing is subject to change without notice.

C. This package is a Pb-free bump design. Bump finish may vary. To determine the exact finish, refer to the device data sheet or contact a local TI representative.

Table 7-1. Pin Configuration

Position	Designation
Pin 1	Gate
Pin 2	Source
Pin 3	Drain

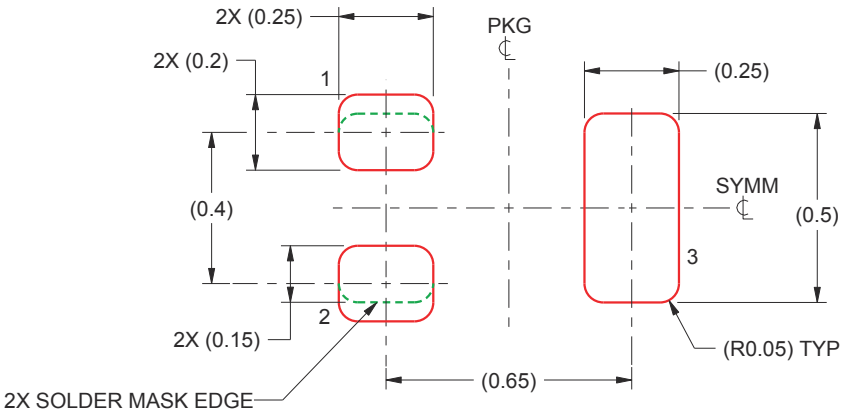
7.2 Recommended Minimum PCB Layout



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED

A. All dimensions are in millimeters.
B. For more information, see *FemtoFET Surface Mount Guide* (SLRA003D).

7.3 Recommended Stencil Pattern



SOLDER PASTE EXAMPLE

A. All dimensions are in millimeters.
B. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD25481F4	Active	Production	PICOSTAR (YJC) | 3	3000 | LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	CS
CSD25481F4.B	Active	Production	PICOSTAR (YJC) | 3	3000 | LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	CS
CSD25481F4T	Active	Production	PICOSTAR (YJC) | 3	250 | SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	CS
CSD25481F4T.B	Active	Production	PICOSTAR (YJC) | 3	250 | SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	CS

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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Last updated 10/2025