CSD25484F4 –20-V P-Channel FemtoFET™ MOSFET

1 Features

- Low on-resistance
- Ultra-low Q_g and Q_{gd}
- Low-threshold voltage
- Ultra-small footprint (0402 case size)
  - 1.0 mm × 0.6 mm
- Ultra-low profile
  - 0.2-mm height
- Integrated ESD protection diode
  - Rated > 4-kV HBM
  - Rated > 2-kV CDM
- Lead and halogen free
- RoHS compliant

2 Applications

- Optimized for load switch applications
- Optimized for general purpose switching applications
- Battery applications
- Handheld and mobile applications

3 Description

This 80-mΩ, –20-V, P-Channel FemtoFET™ MOSFET is designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small signal MOSFETs while providing at least a 60% reduction in footprint size.

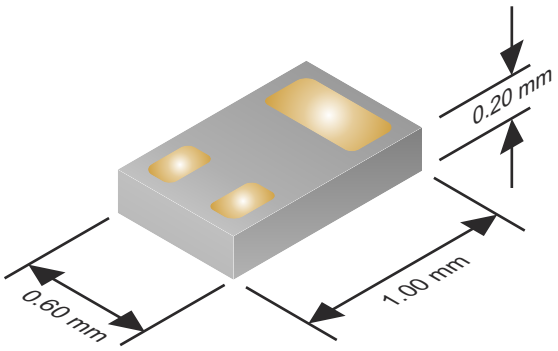

Figure 3-1. Typical Package Dimensions

Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-source voltage	–20		V
Q_g	Gate charge total (–4.5 V)	1090		pC
Q_{gd}	Gate charge gate-to-drain	150		pC
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = –1.8 V	405	mΩ
		V_{GS} = –2.5 V	150	
		V_{GS} = –4.5 V	93	
		V_{GS} = –8.0 V	80	
$V_{GS(th)}$	Threshold voltage	–0.95		V

Device Information

DEVICE	QTY	MEDIA	PACKAGE(1)	SHIP
CSD25484F4	3000	7-Inch Reel	Femto (0402) 1.00-mm × 0.60-mm Land Grid Array (LGA)	Tape and Reel
CSD25484F4T	250			

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-source voltage	–20	V
V_{GS}	Gate-to-source voltage	–12	V
I_D	Continuous drain current(1)	–2.5	A
I_{DM}	Pulsed drain current(1) (2)	–22	A
I_G	Continuous gate clamp current	–35	mA
	Pulsed gate clamp current(2)	–350	
P_D	Power dissipation(1)	500	mW
$V_{(ESD)}$	Human-body model (HBM)	4	kV
	Charged-device model (CDM)	2	
T_J, T_{stg}	Operating junction, storage temperature	–55 to 150	°C

(1) Typical $R_{\theta JA}$ = 85°C/W on 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu pad on a 0.06-in (1.52-mm) thick FR4 PCB.
(2) Pulse duration ≤ 100 µs, duty cycle ≤ 1%.

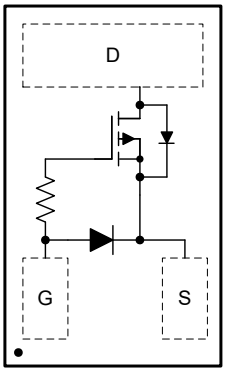

Figure 3-2. Top View

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4 Revision History

Changes from Revision A (August 2017) to Revision B (February 2022)	Page
• Added FemtoFET Surface Mount Guide note	9

Changes from Revision * (May 2015) to Revision A (August 2017)	Page
• Added the *Section 6.1* and the *Section 6*section	7
• Updated the *Section 7.2* and the *Section 7.3* sections	8

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_{DS} = –250 µA	–20			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = –16 V			–100	nA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = –12 V			–50	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = –250 µA	–0.7	–0.95	–1.2	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = –1.8 V, I_{DS} = –0.1 A		405	825	mΩ
		V_{GS} = –2.5 V, I_{DS} = –0.5 A		150	180	
		V_{GS} = –4.5 V, I_{DS} = –0.5 A		93	109	
		V_{GS} = –8 V, I_{DS} = –0.5 A		80	94	
g_{fs}	Transconductance	V_{DS} = –10 V, I_{DS} = –0.5 A		3.5		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = –10 V, f = 1 MHz		175	230	pF
C_{oss}	Output capacitance			78	102	pF
C_{rss}	Reverse transfer capacitance			5.5	7.2	pF
R_G	Series gate resistance			20		Ω
Q_g	Gate charge total (–4.5 V)	V_{DS} = –10 V, I_{DS} = –0.5 A		1090	1415	pC
Q_{gd}	Gate charge gate-to-drain			150		pC
Q_{gs}	Gate charge gate-to-source			350		pC
$Q_{g(th)}$	Gate charge at V_{th}			210		pC
Q_{oss}	Output charge	V_{DS} = –10 V, V_{GS} = 0 V		1290		pC
$t_{d(on)}$	Turnon delay time	V_{DS} = –10 V, V_{GS} = –4.5 V, I_{DS} = –0.5 A, R_G = 10 Ω		9.5		ns
t_r	Rise time			5		ns
$t_{d(off)}$	Turnoff delay time			18		ns
t_f	Fall Time			8.5		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = –0.5 A, V_{GS} = 0 V		–0.75		V
Q_{rr}	Reverse recovery charge	V_{DS}= –10 V, I_F = –0.5 A, di/dt = 100 A/µs		970		pC
t_{rr}	Reverse recovery time			7.5		ns

5.2 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		TYPICAL VALUES	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	85	°C/W
	Junction-to-ambient thermal resistance(2)	245	

(1) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

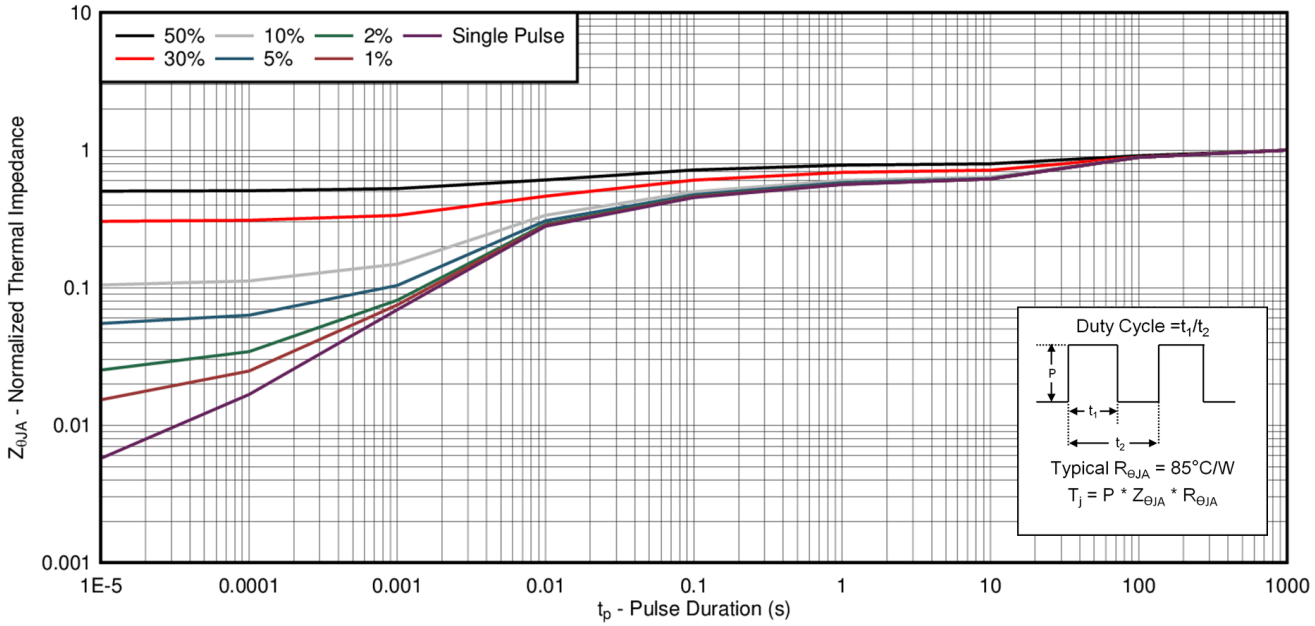


Figure 5-1. Transient Thermal Impedance

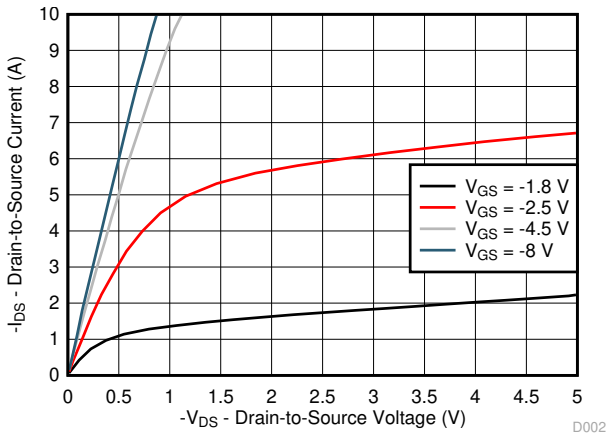
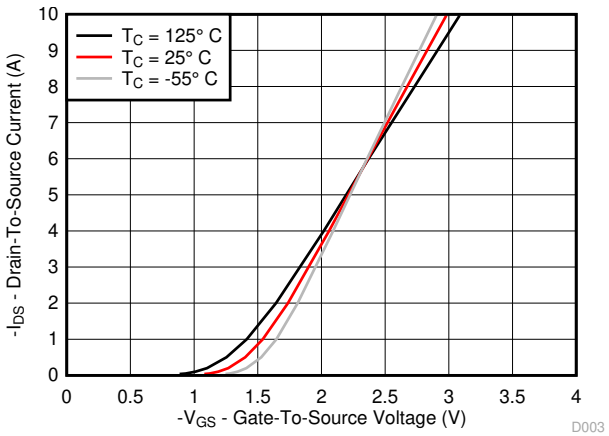
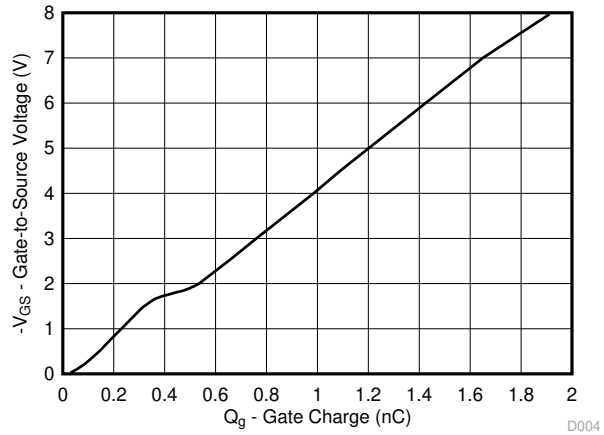


Figure 5-2. Saturation Characteristics



VDS = –5V

Figure 5-3. Transfer Characteristics



ID = –0.5 A VDS = –10 V

Figure 5-4. Gate Charge

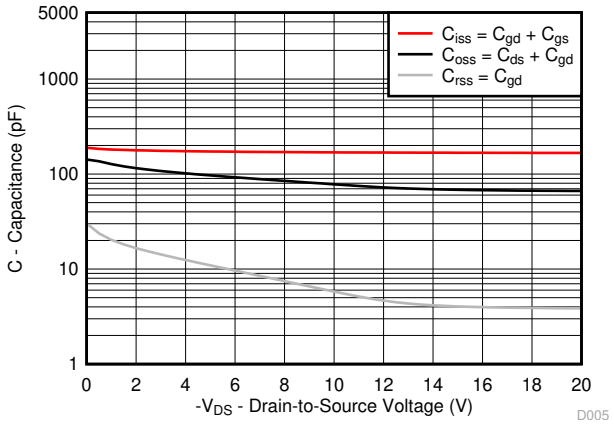
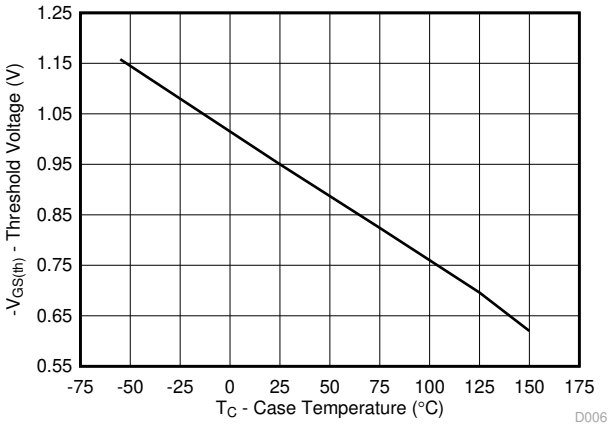


Figure 5-5. Capacitance



ID = –250 µA

Figure 5-6. Threshold Voltage vs Temperature

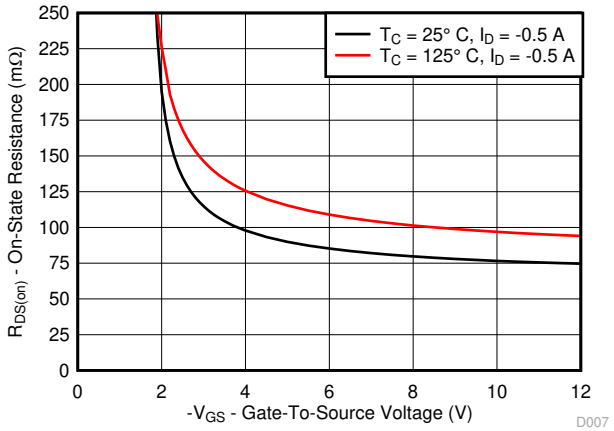
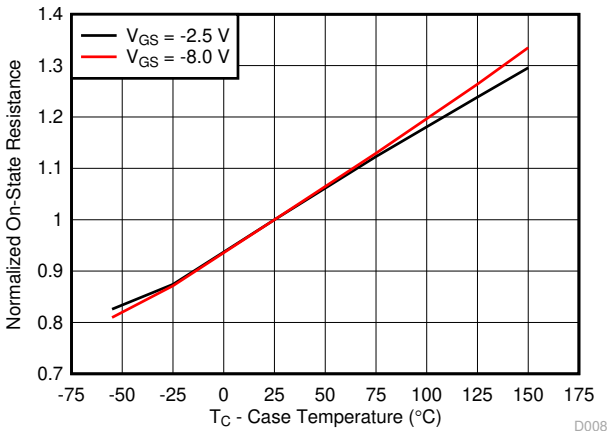


Figure 5-7. On-State Resistance vs Gate-to-Source Voltage



I_D = –0.5 A

Figure 5-8. Normalized On-State Resistance vs Temperature

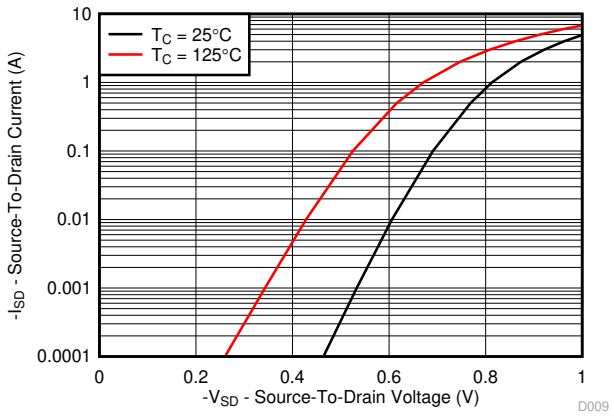
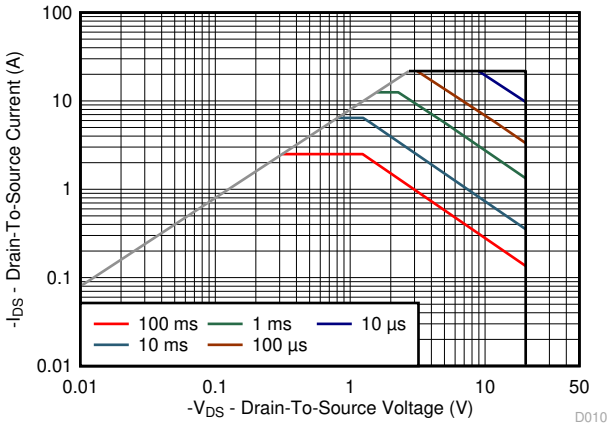


Figure 5-9. Typical Diode Forward Voltage



Single pulse, typical $R_{\theta JA}$ = 85°C/W

Figure 5-10. Maximum Safe Operating Area

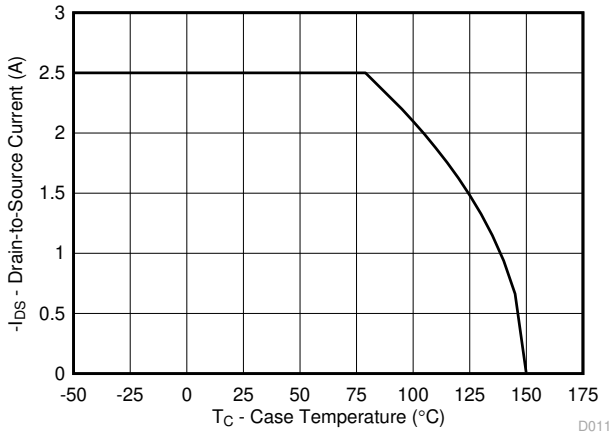


Figure 5-11. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

6.3 Trademarks

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TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

6.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

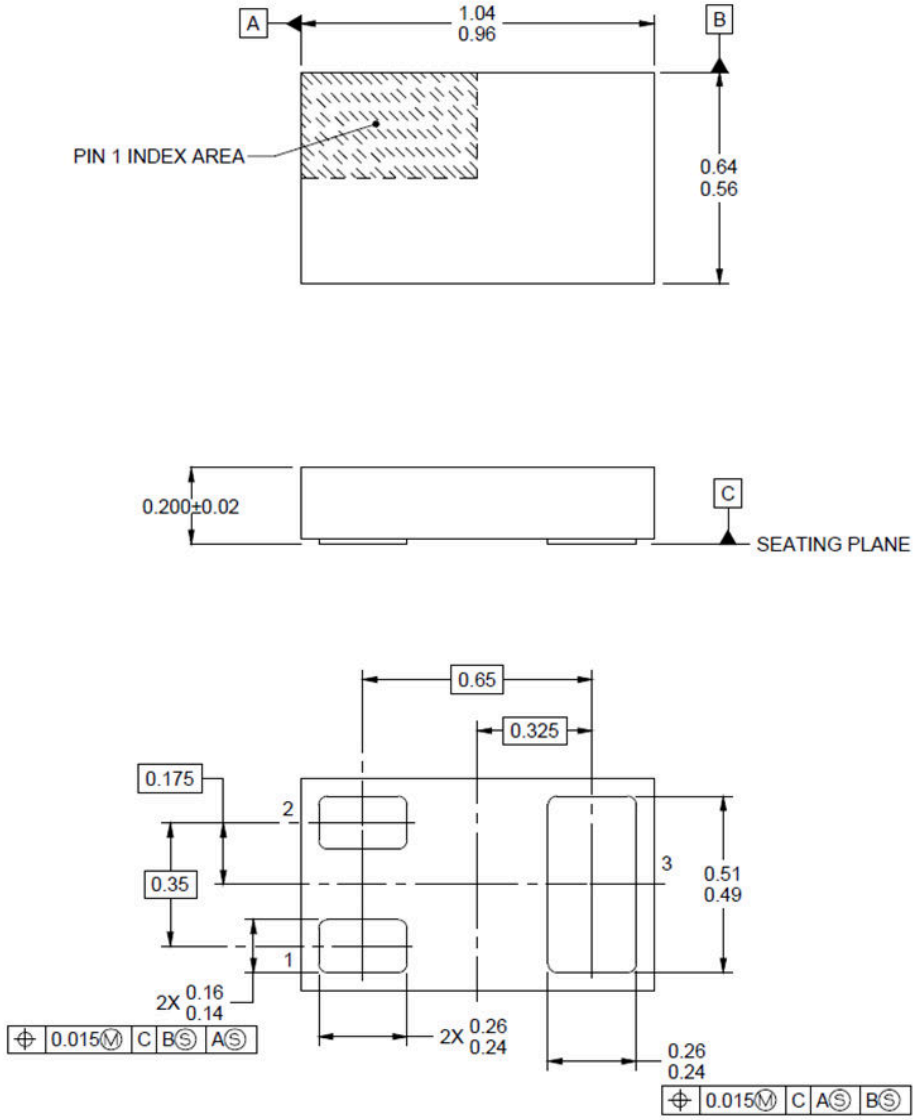
6.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Mechanical Dimensions

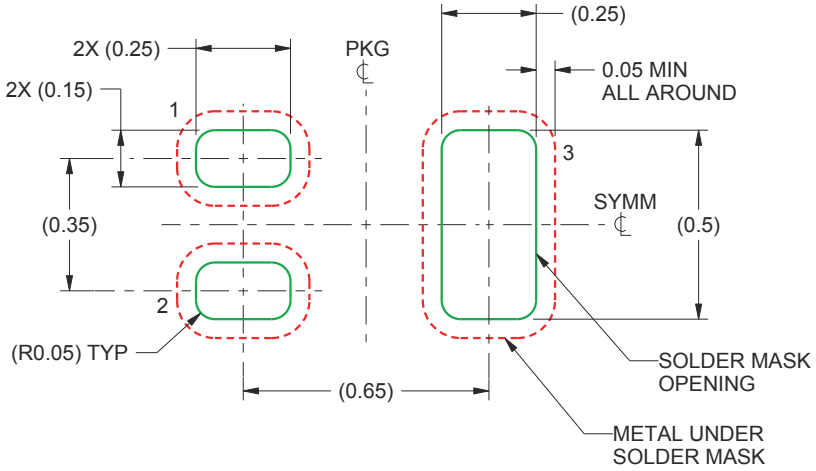


A. All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).
B. This drawing is subject to change without notice.
C. This package is a PB-free solder land design.

Table 7-1. Pin Configuration

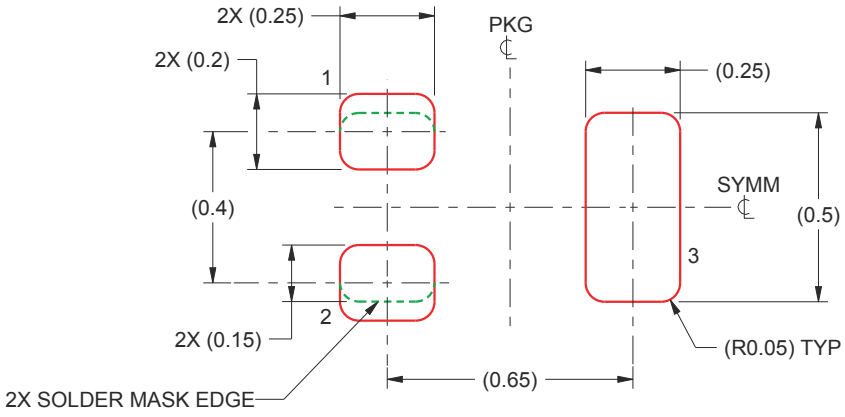
POSITION	DESIGNATION
Pin 1	Gate
Pin 2	Source
Pin 3	Drain

7.2 Recommended Minimum PCB Layout



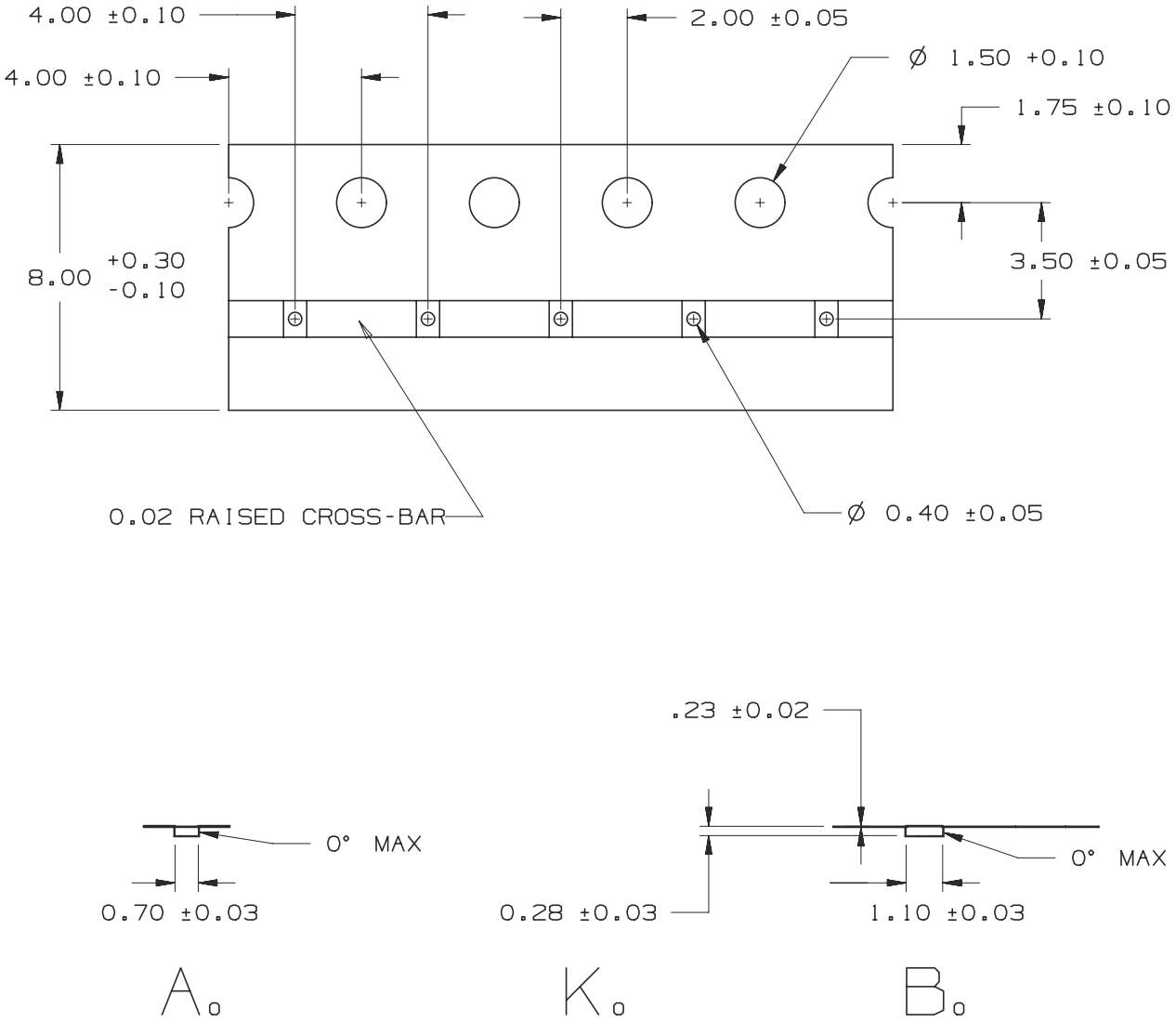
A. All dimensions are in millimeters.
B. For more information, see *FemtoFET Surface Mount Guide* (SLRA003D).

7.3 Recommended Stencil Pattern



A. All dimensions are in millimeters.

7.4 CSD68830F4 Embossed Carrier Tape Dimensions



A. Pin 1 is oriented in the top-right quadrant of the tape enclosure (quadrant 2), closest to the carrier tape sprocket holes.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD25484F4	Active	Production	PICOSTAR (YJJ) | 3	3000 | LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	G3
CSD25484F4.B	Active	Production	PICOSTAR (YJJ) | 3	3000 | LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	G3
CSD25484F4T	Active	Production	PICOSTAR (YJJ) | 3	250 | SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	G3
CSD25484F4T.B	Active	Production	PICOSTAR (YJJ) | 3	250 | SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	G3

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

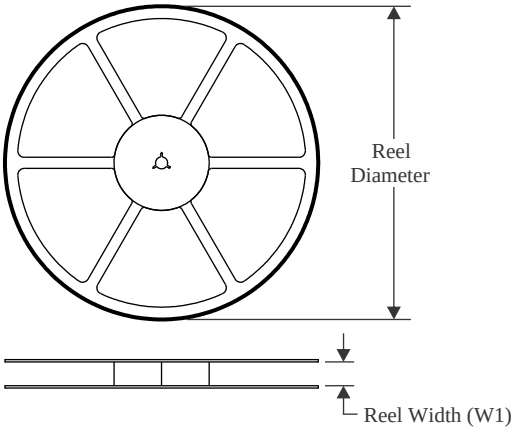
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

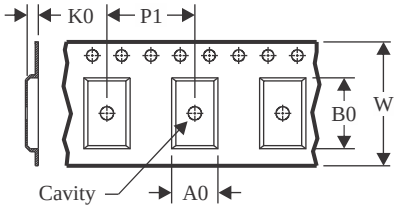
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

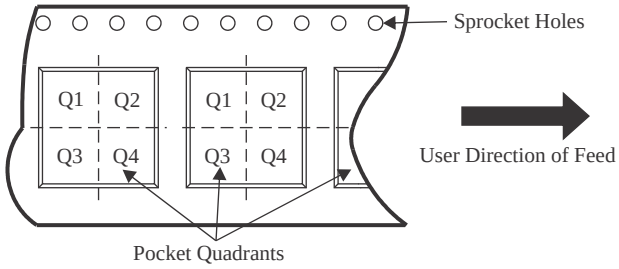


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

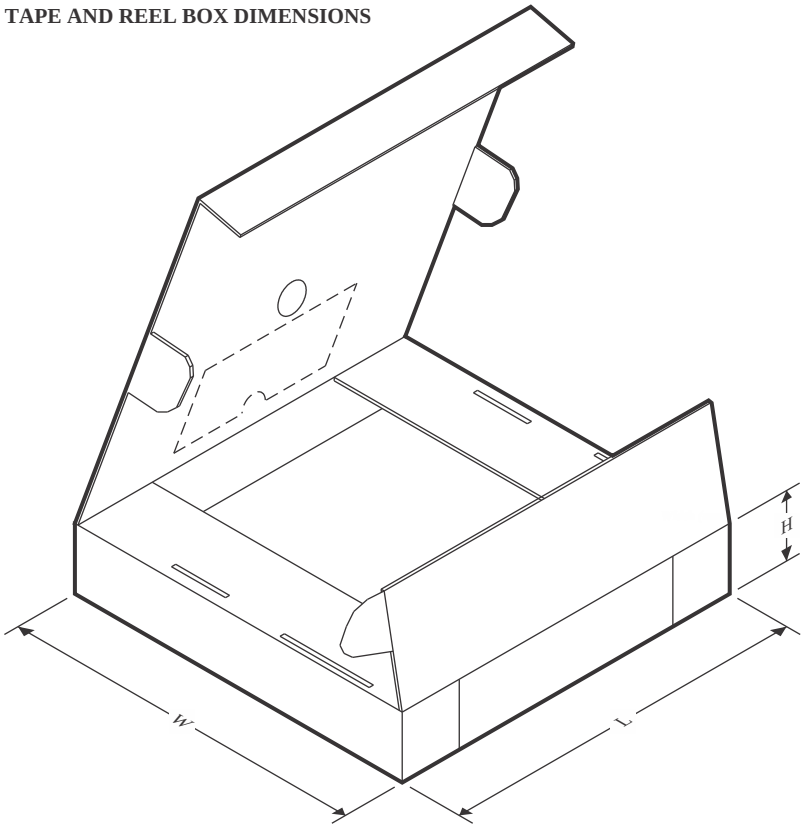
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD25484F4	PICOSTAR	YJJ	3	3000	180.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2
CSD25484F4T	PICOSTAR	YJJ	3	250	180.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

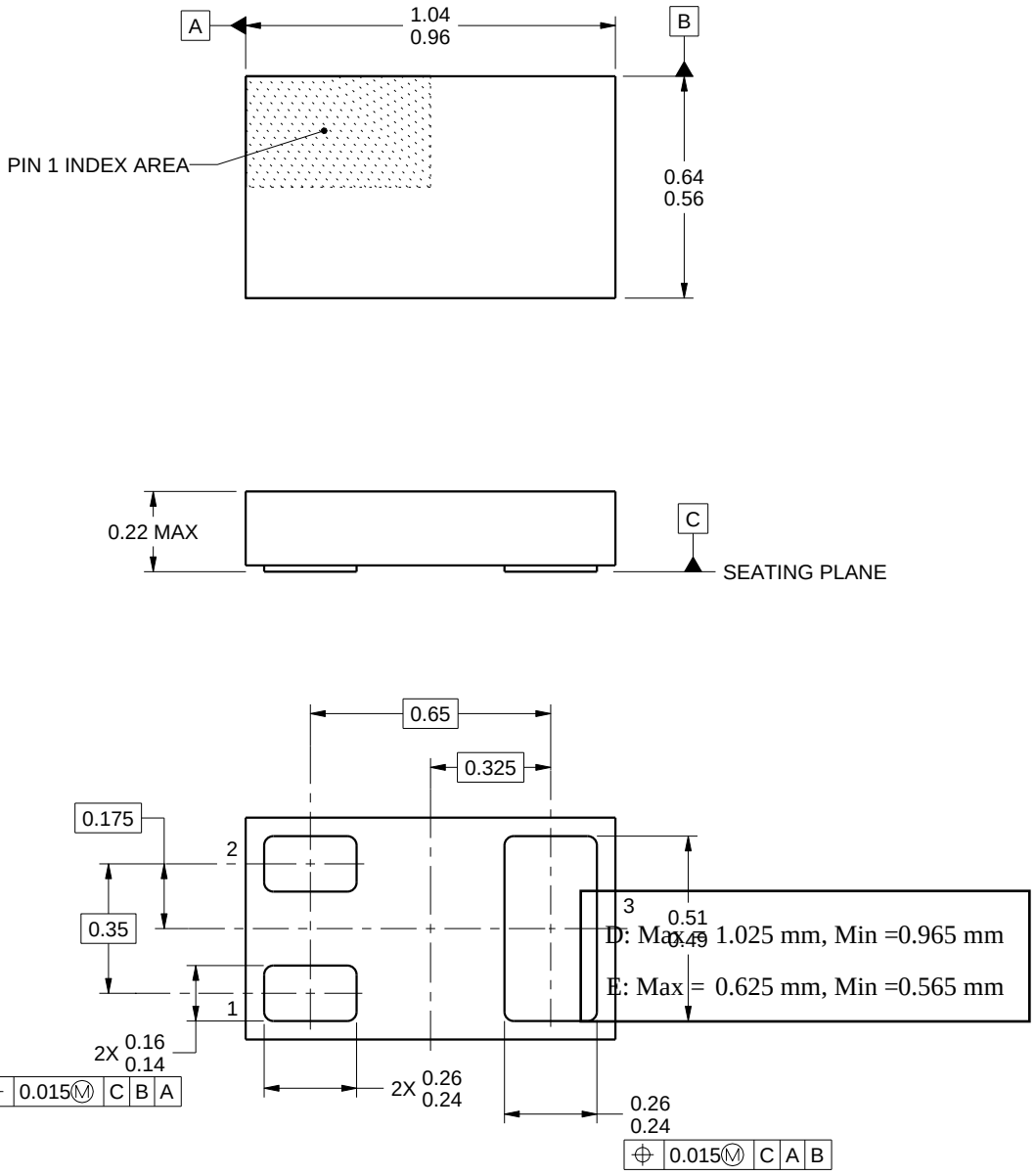
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD25484F4	PICOSTAR	YJJ	3	3000	182.0	182.0	20.0
CSD25484F4T	PICOSTAR	YJJ	3	250	182.0	182.0	20.0

PACKAGE OUTLINE

YJJ0003A

PicoStar™ - 0.22 mm max height

PicoStar™



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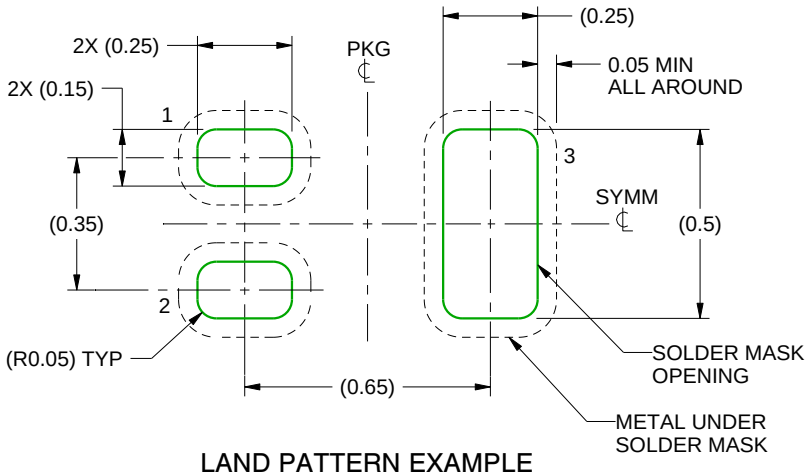
PicoStar is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.
3. This package is a Pb-free bump design. Bump finish may vary. To determine the exact finish, refer to the device datasheet or contact a local TI representative.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:50X

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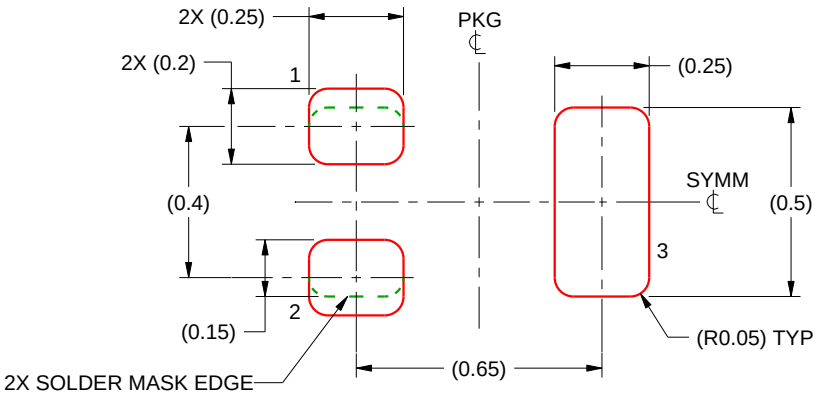
NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:50X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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