

CSD25501F3 –20V P-Channel FemtoFET™ MOSFET

1 Features

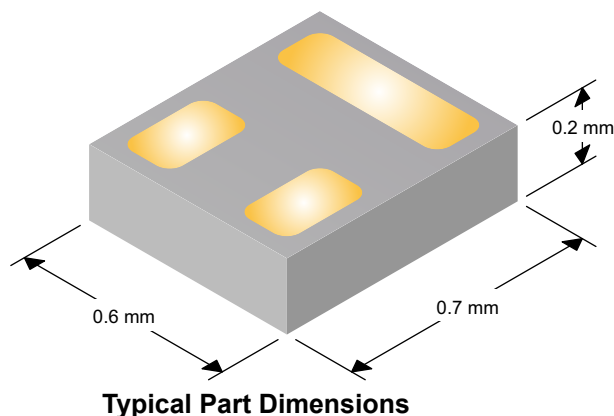
- Low on-resistance
- Ultra-low Q_g and Q_{gd}
- Ultra-small footprint
 - 0.7mm × 0.6mm
- Low profile
 - 0.22mm max height
- Integrated ESD protection diode
- Lead and halogen free
- RoHS compliant

2 Applications

- Optimized for load switch applications
- Battery applications
- Handheld and mobile applications

3 Description

This –20V, 64mΩ, P-Channel FemtoFET™ MOSFET is designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small signal MOSFETs while providing a substantial reduction in footprint size. The integrated 10kΩ clamp resistor (R_C) allows the gate voltage (V_{GS}) to be operated above the maximum internal gate oxide value of –6V, depending on duty cycle. The gate leakage (I_{GSS}) through the diode increases as V_{GS} is increased above –6V.



Product Summary

| $T_A = 25^\circ\text{C}$ | | TYPICAL VALUE | UNIT |
|--------------------------|-------------------------------|-------------------------|------|
| V_{DS} | Drain-to-Source Voltage | –20 | V |
| Q_g | Gate Charge Total (–4.5V) | 1.02 | nC |
| Q_{gd} | Gate Charge Gate-to-Drain | 0.09 | nC |
| $R_{DS(on)}$ | Drain-to-Source On-Resistance | $V_{GS} = -1.8\text{V}$ | 120 |
| | | $V_{GS} = -2.5\text{V}$ | 86 |
| | | $V_{GS} = -4.5\text{V}$ | 64 |
| $V_{GS(th)}$ | Threshold Voltage | –0.75 | V |

Device Information

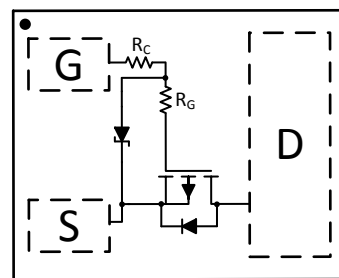
| DEVICE ⁽¹⁾ | QTY | MEDIA | PACKAGE | SHIP |
|-----------------------|------|-------------|---------------------------------------|---------------|
| CSD25501F3 | 3000 | 7 Inch Reel | Femto | Tape and Reel |
| CSD25501F3T | 250 | | 0.73mm × 0.64mm Land Grid Array (LGA) | |

- (1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

| $T_A = 25^\circ\text{C}$ (unless otherwise stated) | | VALUE | UNIT |
|--|---|------------|------------------|
| V_{DS} | Drain-to-Source Voltage | –20 | V |
| V_{GS} | Gate-to-Source Voltage | –20 | V |
| I_D | Continuous Drain Current ⁽¹⁾ | –3.6 | A |
| I_{DM} | Pulsed Drain Current ^{(1) (2)} | –13.6 | A |
| P_D | Power Dissipation ⁽¹⁾ | 500 | mW |
| $V_{(ESD)}$ | Human Body Model (HBM) | 4000 | V |
| | Charged Device Model (CDM) | 2000 | |
| T_J, T_{stg} | Operating Junction, Storage Temperature | –55 to 150 | $^\circ\text{C}$ |

- (1) Typical $R_{\theta JA} = 255^\circ\text{C/W}$ mounted on FR4 material with minimum Cu mounting area.
 (2) Pulse duration $\leq 100\mu\text{s}$, duty cycle $\leq 1\%$.



Top View



Table of Contents

| | | | |
|---|---|---|---|
| 1 Features | 1 | 5.1 Receiving Notification of Documentation Updates..... | 6 |
| 2 Applications | 1 | 5.2 Support Resources..... | 6 |
| 3 Description | 1 | 5.3 Trademarks..... | 6 |
| 4 Specifications | 3 | 5.4 Electrostatic Discharge Caution..... | 6 |
| 4.1 Electrical Characteristics..... | 3 | 5.5 Glossary..... | 6 |
| 4.2 Thermal Information..... | 3 | 6 Revision History | 6 |
| 4.3 Typical MOSFET Characteristics..... | 4 | 7 Mechanical, Packaging, and Orderable Information ... | 7 |
| 5 Device and Documentation Support | 6 | | |

4 Specifications

4.1 Electrical Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------------|----------------------------------|---|-------|--------|-------|------------|
| STATIC CHARACTERISTICS | | | | | | |
| BV_{DSS} | Drain-to-source voltage | $V_{GS} = 0\text{V}, I_{DS} = -250\mu\text{A}$ | -20 | | | V |
| I_{DSS} | Drain-to-source leakage current | $V_{GS} = 0\text{V}, V_{DS} = -16\text{V}$ | | | -50 | nA |
| I_{GSS} | Gate-to-source leakage current | $V_{DS} = 0\text{V}, V_{GS} = -6\text{V}$ | | | -50 | nA |
| | | $V_{DS} = 0\text{V}, V_{GS} = -16\text{V}$ | | | -1 | mA |
| $V_{GS(th)}$ | Gate-to-source threshold voltage | $V_{DS} = V_{GS}, I_{DS} = -250\mu\text{A}$ | -0.45 | -0.75 | -1.05 | V |
| $R_{DS(on)}$ | Drain-to-source on-resistance | $V_{GS} = -1.8\text{V}, I_{DS} = -0.1\text{A}$ | | 120 | 260 | m Ω |
| | | $V_{GS} = -2.5\text{V}, I_{DS} = -0.4\text{A}$ | | 86 | 125 | |
| | | $V_{GS} = -4.5\text{V}, I_{DS} = -0.4\text{A}$ | | 64 | 76 | |
| g_{fs} | Transconductance | $V_{DS} = -2\text{V}, I_{DS} = -0.4\text{A}$ | | 3.4 | | S |
| DYNAMIC CHARACTERISTICS | | | | | | |
| C_{iss} | Input capacitance | $V_{GS} = 0\text{V}, V_{DS} = -10\text{V}, f = 100\text{kHz}$ | | 295 | 385 | pF |
| C_{oss} | Output capacitance | | | 70 | 91 | pF |
| C_{riss} | Reverse transfer capacitance | | | 4.1 | 5.3 | pF |
| R_G | Series gate resistance | | | 33 | | Ω |
| R_C | Series clamp resistance | | | 10,000 | | Ω |
| Q_g | Gate charge total (-4.5 V) | $V_{DS} = -10\text{V}, I_{DS} = -0.4\text{A}$ | | 1.02 | 1.33 | nC |
| Q_{gd} | Gate charge gate-to-drain | | | 0.09 | | nC |
| Q_{gs} | Gate charge gate-to-source | | | 0.45 | | nC |
| $Q_{g(th)}$ | Gate charge at V_{th} | | | 0.36 | | nC |
| Q_{oss} | Output charge | $V_{DS} = -10\text{V}, V_{GS} = 0\text{V}$ | | 1.8 | | nC |
| $t_{d(on)}$ | Turnon delay time | $V_{DS} = -10\text{V}, V_{GS} = -4.5\text{V}, I_{DS} = -0.4\text{A}, R_G = 0\Omega$ | | 474 | | ns |
| t_r | Rise time | | | 428 | | ns |
| $t_{d(off)}$ | Turnoff delay time | | | 1154 | | ns |
| t_f | Fall time | | | 945 | | ns |
| DIODE CHARACTERISTICS | | | | | | |
| V_{SD} | Diode forward voltage | $I_{SD} = -0.4\text{A}, V_{GS} = 0\text{V}$ | -0.73 | -0.95 | | V |
| Q_{rr} | Reverse recovery charge | $V_{DS} = -10\text{V}, I_F = -0.4\text{A}, di/dt = 200\text{A}/\mu\text{s}$ | | 3.0 | | nC |
| t_{rr} | Reverse recovery time | | | 7.4 | | ns |

4.2 Thermal Information

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

| THERMAL METRIC | | TYPICAL VALUES | UNIT |
|-----------------|---|----------------|---------------------------|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance ⁽¹⁾ | 90 | $^\circ\text{C}/\text{W}$ |
| | Junction-to-ambient thermal resistance ⁽²⁾ | 255 | $^\circ\text{C}/\text{W}$ |

- (1) Device mounted on FR4 material with 1in^2 (6.45cm^2), 2oz (0.071mm) thick Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.

4.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

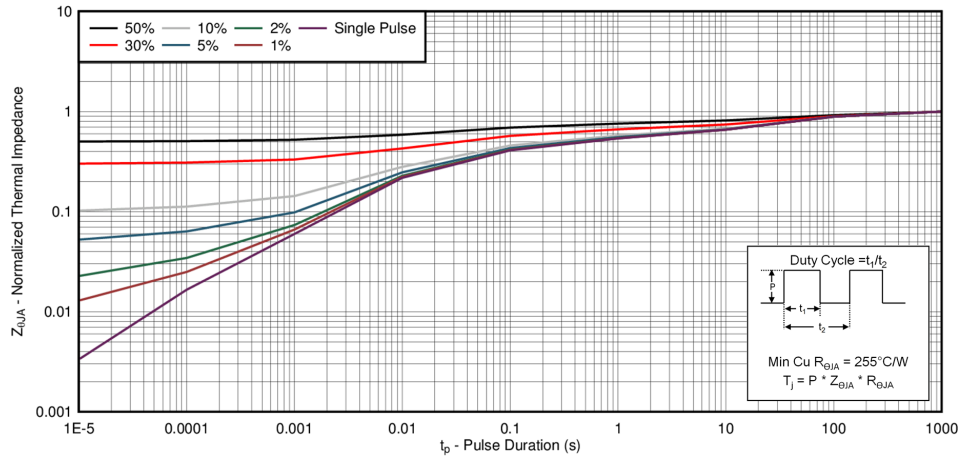


Figure 4-1. Transient Thermal Impedance

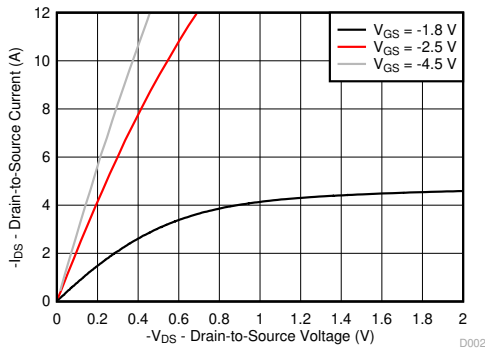


Figure 4-2. Saturation Characteristics

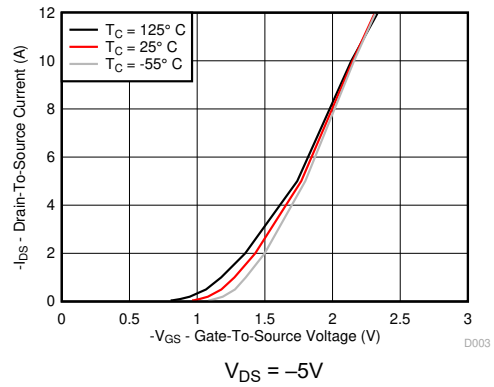


Figure 4-3. Transfer Characteristics

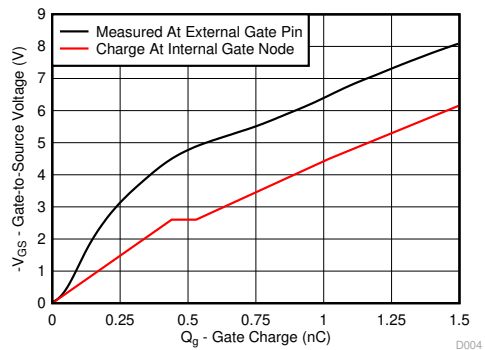


Figure 4-4. Gate Charge
I_D = -0.4A V_{DS} = -10V

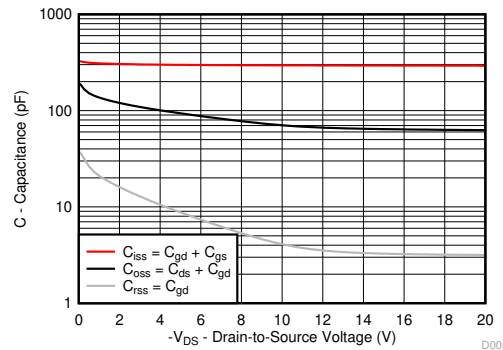


Figure 4-5. Capacitance

4.3 Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

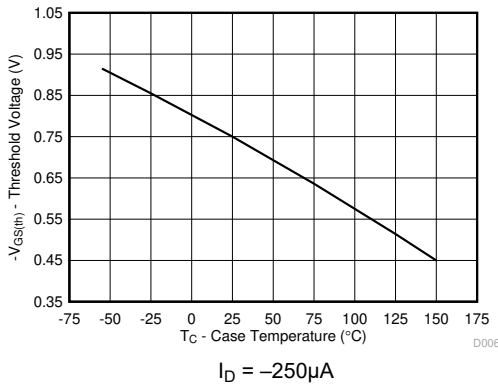


Figure 4-6. Threshold Voltage vs Temperature

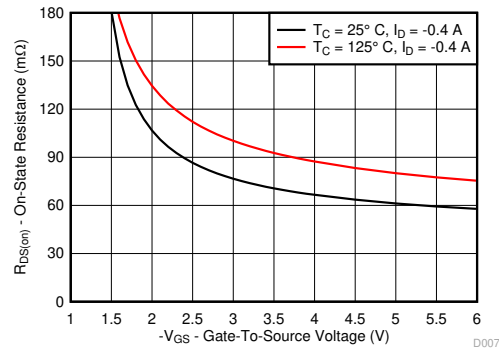


Figure 4-7. On-State Resistance vs Gate-to-Source Voltage

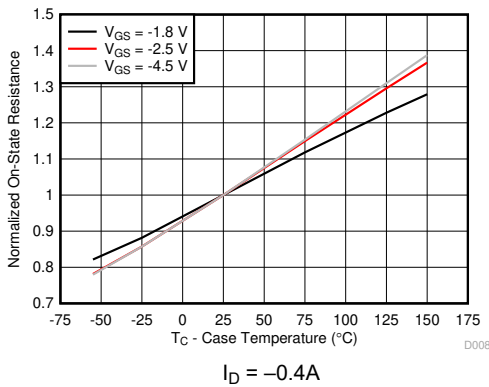


Figure 4-8. Normalized On-State Resistance vs Temperature

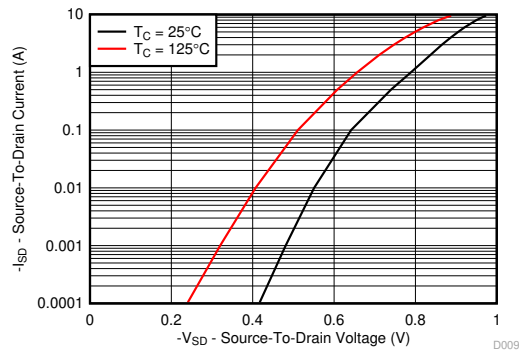


Figure 4-9. Typical Diode Forward Voltage

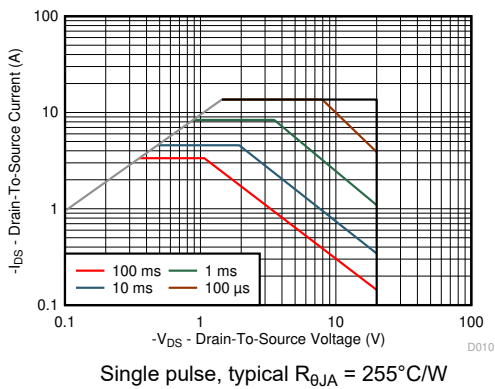


Figure 4-10. Maximum Safe Operating Area

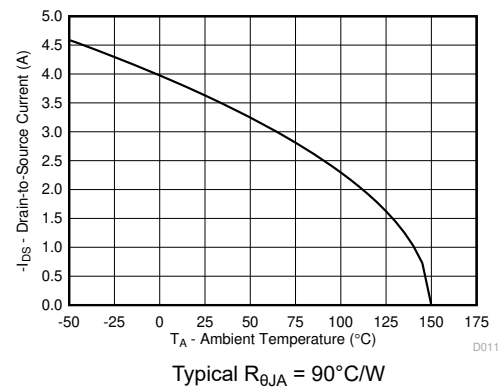


Figure 4-11. Maximum Drain Current vs Temperature

5 Device and Documentation Support

5.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

5.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5.3 Trademarks

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5.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision B (October 2021) to Revision C (June 2024) | Page |
|---|------|
| • Updated the numbering format for tables, figures, and cross-references throughout the document..... | 1 |

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Table 7-1. Pin Configuration

| POSITION | DESIGNATION |
|----------|-------------|
| Pin 1 | Gate |
| Pin 2 | Source |
| Pin 3 | Drain |

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------------|---------------|----------------------|--------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| CSD25501F3 | Active | Production | PICOSTAR (YJN) 3 | 3000 LARGE T&R | Yes | NIAU | Level-1-260C-UNLIM | -55 to 150 | V |
| CSD25501F3.B | Active | Production | PICOSTAR (YJN) 3 | 3000 LARGE T&R | Yes | NIAU | Level-1-260C-UNLIM | -55 to 150 | V |
| CSD25501F3T | Active | Production | PICOSTAR (YJN) 3 | 250 SMALL T&R | Yes | NIAU | Level-1-260C-UNLIM | -55 to 150 | V |
| CSD25501F3T.B | Active | Production | PICOSTAR (YJN) 3 | 250 SMALL T&R | Yes | NIAU | Level-1-260C-UNLIM | -55 to 150 | V |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

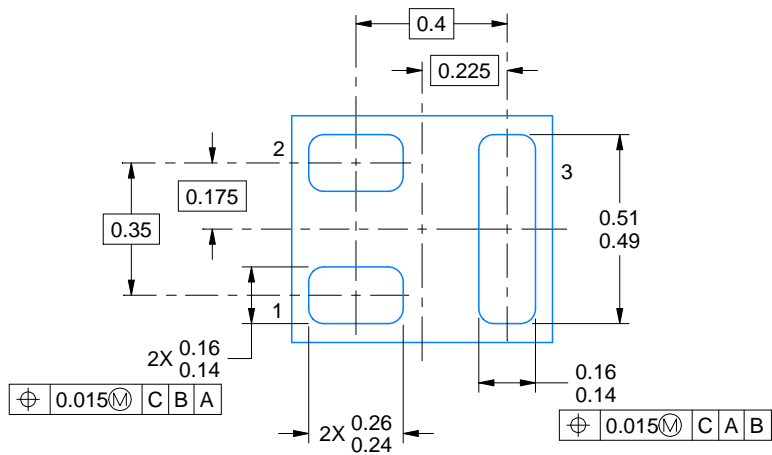
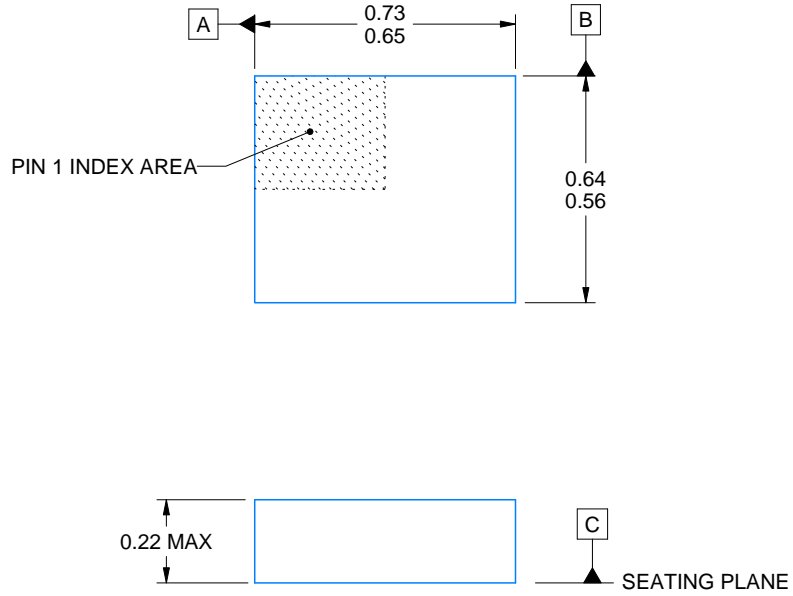
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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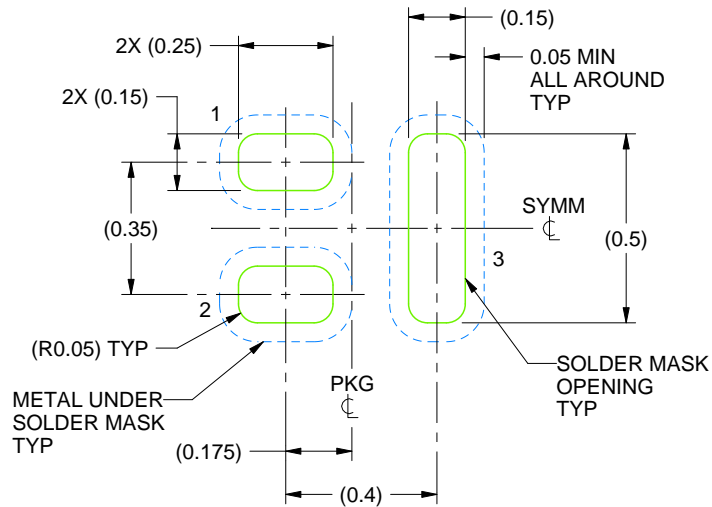


4223685/A 05/2017

NOTES:

PicoStar is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.
3. This package is a Pb-free bump design. Bump finish may vary. To determine the exact finish, refer to the device datasheet or contact a local TI representative.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:50X

4223685/A 05/2017

NOTES: (continued)

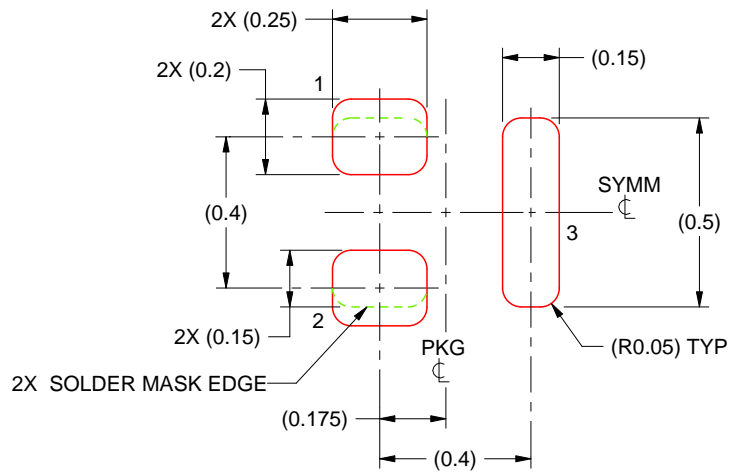
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

YJN0003A

PicoStar™ - 0.22 mm max height

PicoStar™



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:50X

4223685/A 05/2017

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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