CSD95485RWJ Synchronous Buck NexFET™ Smart Power Stage

1 Features

- 75-A continuous operating current capability
- Over 95% system efficiency at 30 A
- High-frequency operation (up to 1.25 MHz)
- Diode emulation function
- Temperature compensated bi-directional current sense
- Analog temperature output
- Fault monitoring
- 3.3-V and 5-V PWM signal compatible
- Tri-state PWM input
- Integrated bootstrap switch
- Optimized dead time for shoot-through protection
- High-density QFN 5-mm × 6-mm footprint
- Ultra-low-inductance package
- System optimized PCB footprint
- Thermally enhanced topside cooling
- RoHS compliant – lead-free terminal plating
- Halogen free

2 Applications

- Multiphase synchronous buck converters
  - High-frequency applications
  - High-current, low-duty cycle applications
- POL DC-DC converters
- Memory and graphic cards
- Desktop and server VR12.x / VR13.x V-core synchronous buck converters

3 Description

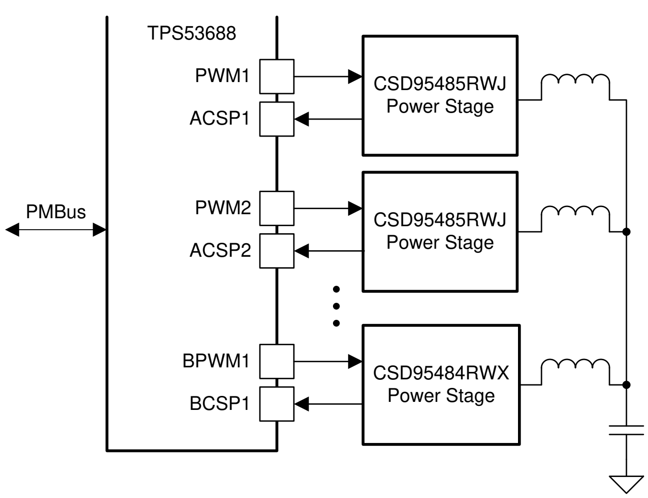
The CSD95485RWJ NexFET™ power stage is a highly optimized design for use in a high-power, high-density synchronous buck converter. This product integrates the driver IC and power MOSFETs to complete the power stage switching function. This combination produces high-current, high-efficiency, and high-speed switching capability in a small 5-mm × 6-mm outline package. It also integrates the accurate current sensing and temperature sensing functionality to simplify system design and improve accuracy. In addition, the PCB footprint has been optimized to help reduce design time and simplify the completion of the overall system design.

Device Information(1)

DEVICE	MEDIA	QTY	PACKAGE	SHIP
CSD95485RWJ	13-Inch Reel	2500	QFN 5.00-mm × 6.00-mm Package	Tape and Reel
CSD95485RWJT	7-Inch Reel	250		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Diagram



Typical Power Stage Efficiency and Power Loss

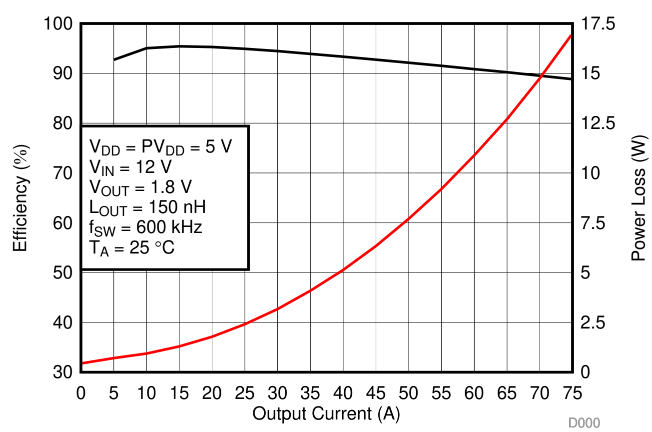


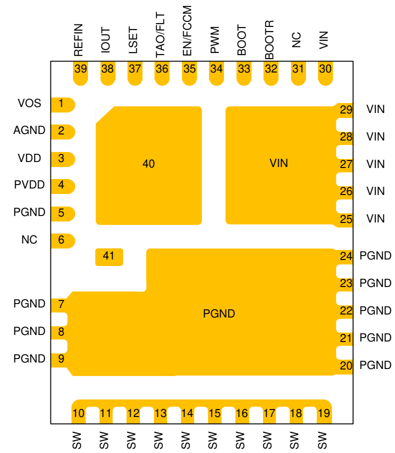
Table of Contents

4 Revision History

DATE	REVISION	NOTES
March 2020	*	Initial release.

5 Pin Configuration and Functions

RWJ Package
41-Pin QFN
Top View



Pin Functions

PIN		DESCRIPTION
NAME	NUMBER	
VOS	1	Output voltage sensing pin for the internal current sensing circuitry.
AGND	2	This pin is internally connected to PGND.
VDD	3	Supply voltage for internal circuitry. This pin should be bypassed directly to pin 2.
PVDD	4	Supply voltage for gate drivers. This pin should be bypassed to PGND.
PGND	5	Power ground.
NC	6	Not connected. This pin needs to be left floating in application.
PGND	7-9	Power ground.
VSW	10-19	Phase node connecting the HS MOSFET source and LS MOSFET drain – pin connection to the output inductor.
PGND	20-24	Power ground.
VIN	25-30	Input voltage pin. Connect input capacitors close to this pin.
NC	31	Not connected. This pin needs to be left floating in application.
BOOTR	32	Return path for HS gate driver. It is connected to VSW internally.
BOOT	33	Bootstrap capacitor connection. Connect a minimum 0.1-µF, 16-V, X5R ceramic capacitor from BOOT to BOOTR pins. The bootstrap capacitor provides the charge to turn on the control FET. The bootstrap diode is integrated.
PWM	34	Tri-state input from external controller. Logic low sets control FET gate low and sync FET gate high. Logic high sets control FET gate high and sync FET gate low. Both MOSFET gates are set low if PWM stays in Hi-Z for greater than the tri-state shutdown holdoff time (T_{3HT}).
EN/FCCM	35	This dual function pin either enables the diode emulation function or can be used as a simple enable for the device. When this pin is driven into the tri-state window and held there for more than the tri-state holdoff time, diode emulation mode is enabled for sync FET. When the pin is high, device operates in forced continuous conduction mode. When the pin is low, both FETs are held off. An internal resistor pulls this pin low if left floating.
TAO/FLT	36	Temperature amplifier output. Reports a voltage proportional to the IC temperature. An ORing diode is integrated in the IC. When used in a multi-phase application, a single wire can be used to connect the TAO pins of all the ICs. Only the highest temperature will be reported. TAO will be pulled up to 3.3 V if thermal shutdown LSOC or HSS detection circuit is tripped.
LSET	37	A resistor from this pin to PGND pin sets the inductor value for the internal current sensing circuitry.
IOUT	38	Output of current sensing amplifier. V(IOUT) – V(REFIN) is proportional to the phase current.
REFIN	39	External reference voltage input for current sensing amplifier.
PGND	40	Power ground.
NC	41	Not connected. This pin needs to be left floating in application.

6 Specifications

6.1 Absolute Maximum Ratings

T_A = 25°C (unless otherwise noted)(1)

			MIN	MAX	UNIT
	V_{IN} to P_{GND}		–0.3	20	V
	V_{IN} to V_{SW}		–0.3	20	V
	V_{IN} to V_{SW} (10 ns)	I_{LOAD} > 0 A(2)		23	V
	V_{SW} to P_{GND}		–0.3	20	V
	V_{SW} to P_{GND} (10 ns)	I_{LOAD} < 0 A(2)		23	V
	V_{SW} to P_{GND} (10 ns)		–7		V
	V_{DD} to P_{GND}		–0.3	7	V
	EN/FCCM, TAO/FLT, LSET to P_{GND}(3)		–0.3	V_{DD} + 0.3	V
	IOUT, VOS, PWM to P_{GND}		–0.3	7	V
	REFIN to P_{GND}		–0.3	3.6	V
	BOOT to P_{GND}		–0.3	30	V
	BOOT to BOOT_R(3)		–0.3	V_{DD} + 0.3	V
T_J	Operating junction temperature		–55	150	°C
T_{stg}	Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) I_{LOAD} is defined as the current flowing out of the VSW pins.
(3) Should not exceed 7 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM)	±2000	V
		Charged-device model (CDM)	±500	

6.3 Recommended Operating Conditions

T_A = 25°C (unless otherwise stated)

			MIN	MAX	UNIT
V_{DD}	Driver supply voltage		4.5	5.5	V
PV_{DD}	Gate drive voltage		4.5	5.5	V
V_{IN}	Input supply voltage(1)		4.5	16	V
V_{OUT}	Output voltage			5.5	V
	PWM to P_{GND}			V_{DD} + 0.3	V
I_{OUT}	Continuous output current	V_{IN} = 12 V, V_{DD} = 5 V, PV_{DD} = 5 V, V_{OUT} = 1.2 V, f_{SW} = 500 kHz(2)		75	A
I_{OUT-PK}	Peak output current(3)			105	A
f_{SW}	Switching frequency	C_{BST} = 0.1 µF (min), V_{OUT} = 2.5 V (max)		1250	kHz
	On-time duty cycle	f_{SW} = 1 MHz		85%	
	Minimum PWM on-time		20		ns
	Operating junction temperature		–40	125	°C

(1) Operating at high V_{IN} can create excessive AC voltage overshoots on the switch node (V_{SW}) during MOSFET switching transients. For reliable operation, the switch node (V_{SW}) to ground voltage must remain at or below the *Absolute Maximum Ratings*.
(2) Measurement made with six 10-µF (TDK C3216X7R1C106KT or equivalent) ceramic capacitors across V_{IN} to P_{GND} pins.
(3) System conditions as defined in Note 2. Peak output current is applied for t_p = 50 µs.

6.4 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
θ_{JC}	Thermal resistance, junction-to-case (top of package)		7.4		°C/W
θ_{JB}	Thermal resistance, junction-to-board[1]		2.2		°C/W
Ψ_{JT}	Junction-to-top characterization parameter		0.9		°C/W

(1) θ_{JB} is determined with the device mounted on a 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu pad on a 1.5-in × 1.5-in, 0.06-in (1.52-mm) thick FR4 board based on hottest board temperature within 1 mm of the package.

7 Application Schematic

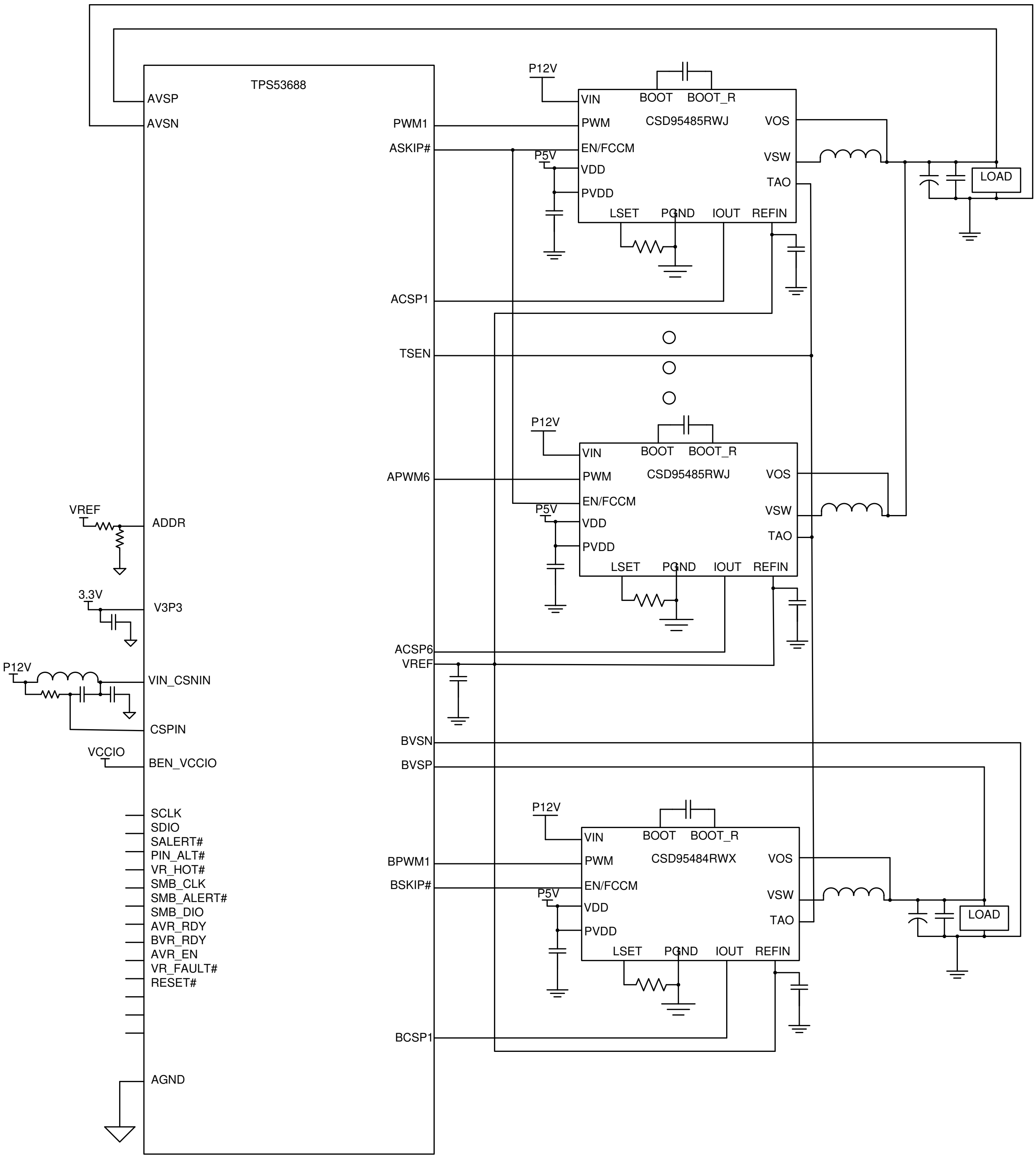


Figure 1. Application Schematic

Note: The schematic in Figure 1 is a conceptual drawing only. Actual designs may require additional components not shown.

8 Device and Documentation Support

8.1 Trademarks

NexFET is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

8.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

8.3 Glossary

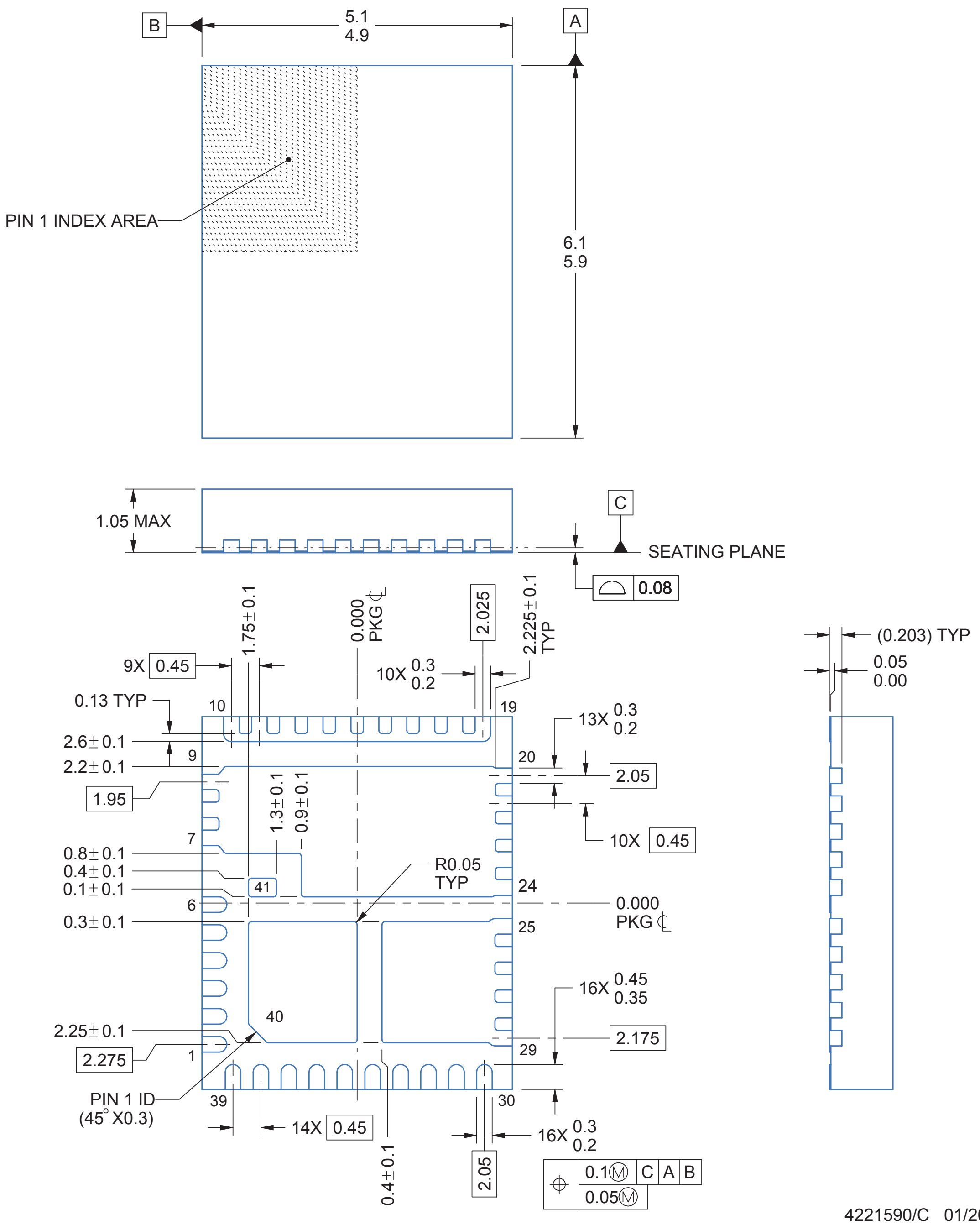
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

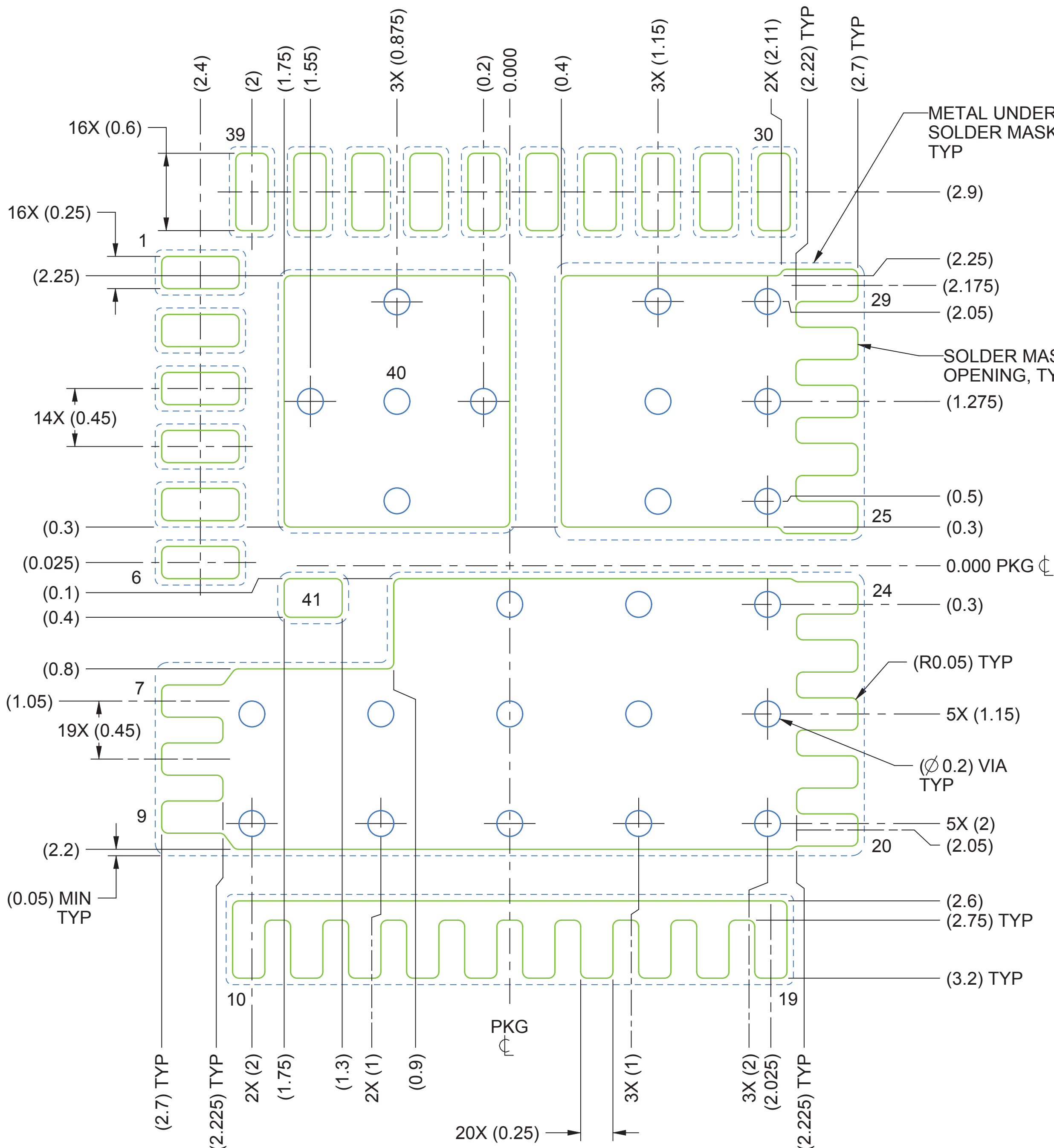
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

9.1 Mechanical Drawing



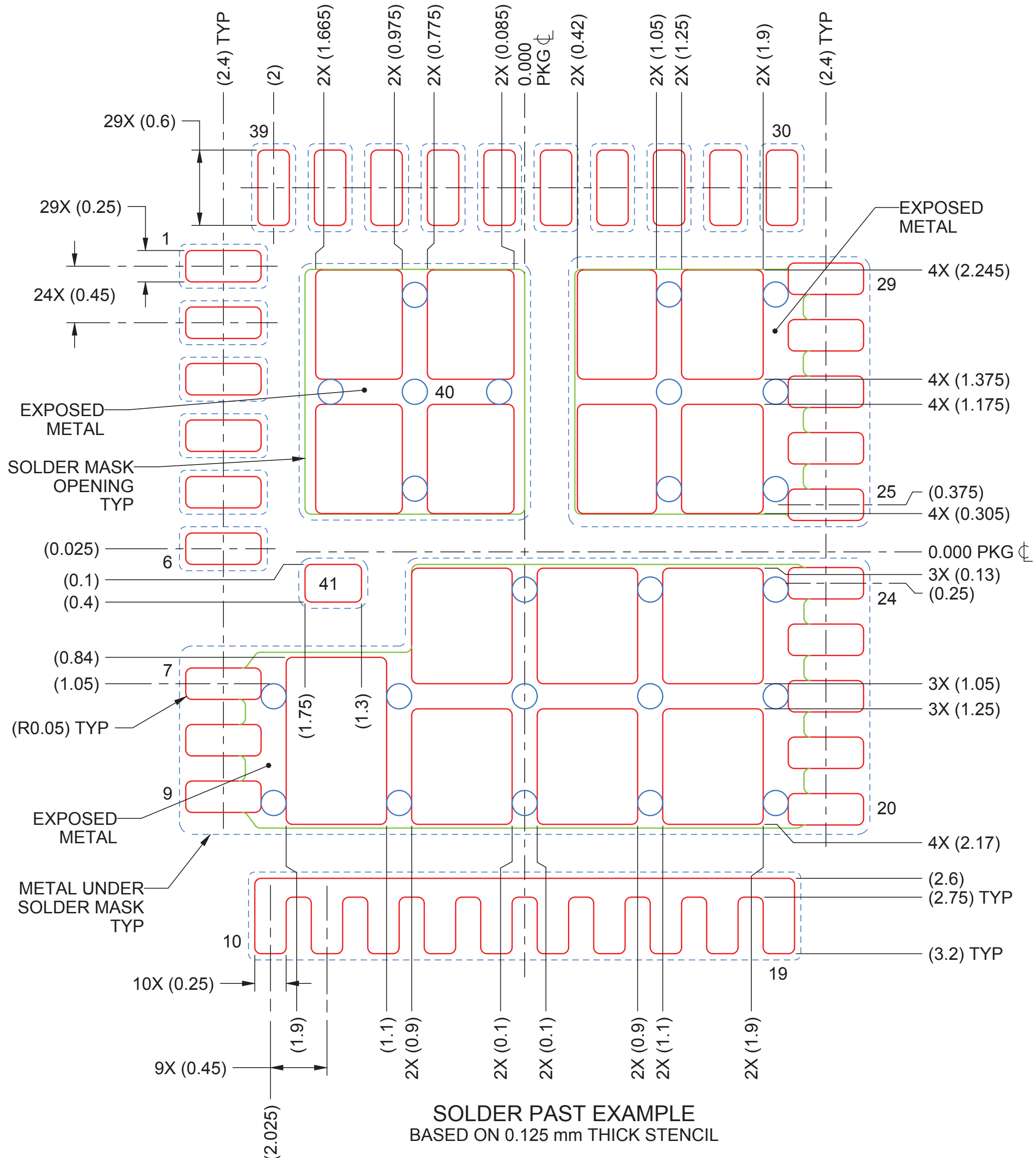
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.

9.2 Recommended PCB Land Pattern



1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is designed to be soldered to thermal pads on the board. For more information, see *QFN/SON PCB Attachment* (SLUA271).

9.3 Recommended Stencil Opening



SOLDER PAST EXAMPLE
BASED ON 0.125 mm THICK STENCIL

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD95485RWJ	NRND	Production	VQFN-CLIP (RWJ) | 41	2500 | LARGE T&R	ROHS Exempt	NIPDAU | SN	Level-2-260C-1 YEAR	-55 to 150	95485RWJ
CSD95485RWJ.B	NRND	Production	VQFN-CLIP (RWJ) | 41	2500 | LARGE T&R	-	Call TI	Call TI	-55 to 150	
CSD95485RWJT	NRND	Production	VQFN-CLIP (RWJ) | 41	250 | SMALL T&R	ROHS Exempt	NIPDAU | SN	Level-2-260C-1 YEAR	-55 to 150	95485RWJ
CSD95485RWJT.B	NRND	Production	VQFN-CLIP (RWJ) | 41	250 | SMALL T&R	-	Call TI	Call TI	-55 to 150	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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