

CSD95496QVM Synchronous Buck NexFET™ Smart Power Stage

1 Features

- 40-A Continuous Operating Current Capability
- Over 93% System Efficiency at 20 A
- High-Frequency Operation (up to 1.25 MHz)
- Diode Emulation Function
- Temperature Compensated Bi-Directional Current Sense
- Analog Temperature Output
- Fault Monitoring
- 3.3-V and 5-V PWM Signal Compatible
- Tri-State PWM Input
- Integrated Bootstrap Switch
- Optimized Dead Time for Shoot-Through Protection
- High-Density VSON 4-mm × 5-mm Footprint
- Ultra-Low-Inductance Package
- System Optimized PCB Footprint
- RoHS Compliant – Lead-Free Terminal Plating
- Halogen Free

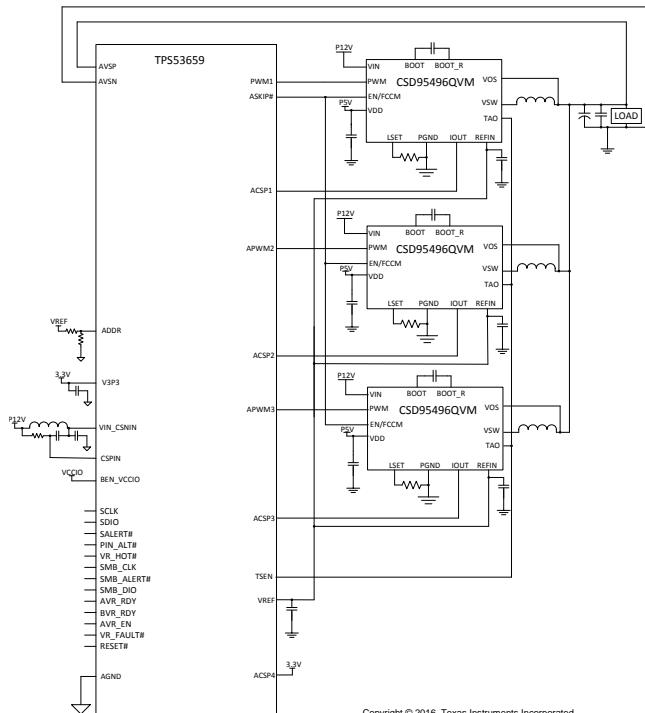
2 Applications

- Multiphase Synchronous Buck Converters
 - High-Frequency Applications
 - High-Current, Low-Duty Cycle Applications
- POL DC-DC Converters
- Memory and Graphic Cards
- Desktop and Server VR12.x / VR13.x VRM Synchronous Buck Converters

3 Description

The CSD95496QVM NexFET™ power stage is a highly optimized design for use in a high-power, high-density synchronous buck converter. This product integrates the driver IC and power MOSFETs to complete the power stage switching function. This combination produces high-current, high-efficiency, and high-speed switching capability in a small 4-mm × 5-mm outline package. It also integrates the accurate current sensing and temperature sensing functionality to simplify system design and improve accuracy. In addition, the PCB footprint has been optimized to help reduce design time and simplify the completion of the overall system design.

Application Diagram

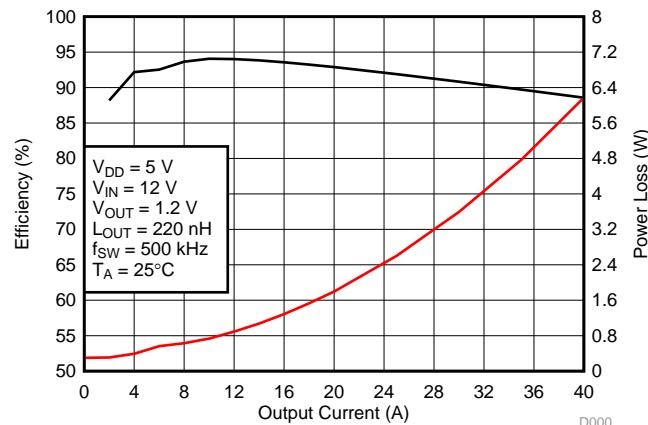


Device Information⁽¹⁾

DEVICE	MEDIA	QTY	PACKAGE	SHIP
CSD95496QVM	13-Inch Reel	2500	VSON 4.00-mm × 5.00-mm Package	Tape and Reel
CSD95496QVMT	7-Inch Reel	250		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Power Stage Efficiency and Power Loss



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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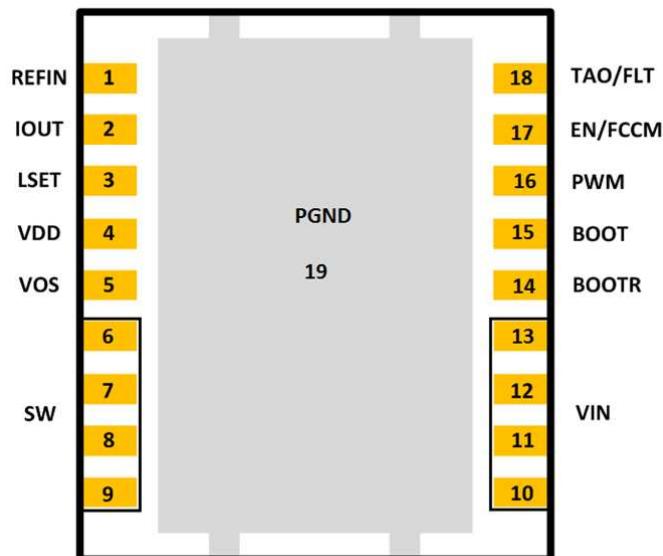
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4 Revision History

DATE	REVISION	NOTES
June 2017	*	Initial release.

5 Pin Configuration and Functions

Top View



Pin Functions

PIN		DESCRIPTION
NAME	NO.	
REFIN	1	External reference voltage input for current sensing amplifier.
IOUT	2	Output of current sensing amplifier. $V(IOUT) - V(REFIN)$ is proportional to the phase current.
LSET	3	A resistor from this pin to PGND pin sets the inductor value for the internal current sensing circuitry.
VDD	4	Supply voltage for gate drivers and internal circuitry.
VOS	5	Output voltage sensing pin for the internal current sensing circuitry.
SW	6-9	Phase node connecting the HS MOSFET Source and LS MOSFET drain – pin connection to the output inductor.
VIN	10-13	Input voltage pin. Connect input capacitors close to this pin.
BOOTR	14	Return path for HS gate driver. It is connected to VSW internally.
BOOT	15	Bootstrap capacitor connection. Connect a minimum 0.1- μ F, 16-V, X5R ceramic cap from BOOT to BOOTR pins. The bootstrap capacitor provides the charge to turn on the control FET. The bootstrap diode is integrated.
PWM	16	Tri-state input from external controller. Logic low sets control FET gate low and sync FET gate high. Logic high sets control FET gate high and sync FET gate low. Both MOSFET gates are set low if PWM stays in Hi-Z for greater than the tri-state shutdown holdoff time (t_{3HT}).
EN/FCCM	17	This dual function pin either enables the diode emulation function or can be used as a simple enable for the device. When this pin is driven into the tri-state window and held there for more than the tri-state holdoff time, Diode Emulation Mode is enabled for sync FET. When the pin is high, device operates in Forced Continuous Conduction Mode. When the pin is low, both FETs are held off. An internal resistor pulls this pin low if left floating.
TAO/FAULT	18	Temperature Amplifier Output. Reports a voltage proportional to the IC temperature. An ORing diode is integrated in the IC. When used in multiphase application, a single wire can be used to connect the TAO pins of all the ICs. Only the highest temperature will be reported. TAO will be pulled up to 3.3 V if thermal shutdown, LSOC, or HSS detection circuit is tripped.
PGND	19	Power ground.

6 Specifications

6.1 Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$ (unless otherwise stated)⁽¹⁾

		MIN	MAX	UNIT
V_{IN} to P_{GND}		-0.3	20	V
V_{IN} to V_{SW}		-0.3	20	V
V_{IN} to V_{SW} (10 ns)			23	V
V_{SW} to P_{GND}		-0.3	20	V
V_{SW} to P_{GND} (10 ns)		-7	23	V
V_{DD} to P_{GND}		-0.3	7	V
EN/FCCM, TAO/FLT, LSET to P_{GND} ⁽²⁾		-0.3	$V_{DD} + 0.3$	V
IOUT, VOS, PWM to P_{GND}		-0.3	7	V
REFIN		-0.3	3.6	V
BOOT to BOOTR ⁽²⁾		-0.3	$V_{DD} + 0.3$	V
BOOT to P_{GND}		-0.3	30	V
T_J	Operating junction temperature	-55	150	$^\circ\text{C}$
T_{stg}	Storage temperature	-55	150	$^\circ\text{C}$

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Should not exceed 7 V.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM)	± 2000
		Charged-device model (CDM)	

6.3 Recommended Operating Conditions

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

		MIN	MAX	UNIT
V_{DD}	Driver supply voltage	4.5	5.5	V
V_{IN}	Input supply voltage ⁽¹⁾	4.5	16	V
V_{OUT}	Output voltage		5.5	V
PWM	PWM to P_{GND}		V_{DD}	V
I_{OUT}	Continuous output current	$V_{IN} = 12\text{ V}$, $V_{DD} = 5\text{ V}$, $V_{OUT} = 1.2\text{ V}$, $f_{SW} = 500\text{ kHz}$ ⁽²⁾	40	A
$I_{OUT\text{-PK}}$	Peak output current ⁽³⁾		60	A
f_{SW}	Switching frequency	$C_{BST} = 0.1\text{ }\mu\text{F}$ (min), $V_{OUT} = 2.5\text{ V}$ (max)	1250	kHz
	On-time duty cycle	$f_{SW} = 1\text{ MHz}$	85%	
	Minimum PWM on-time		20	ns
	Operating junction temperature		-40	125
				$^\circ\text{C}$

(1) Operating at high V_{IN} can create excessive AC voltage overshoots on the switch node (V_{SW}) during MOSFET switching transients. For reliable operation, the switch node (V_{SW}) to ground voltage must remain at or below the *Absolute Maximum Ratings*.

(2) Measurement made with six 10- μF (TDK C3216X7R1C106KT or equivalent) ceramic capacitors across V_{IN} to P_{GND} pins.

(3) System conditions as defined in Note 2. Peak output current is applied for $t_p = 50\text{ }\mu\text{s}$.

7 Application Schematic

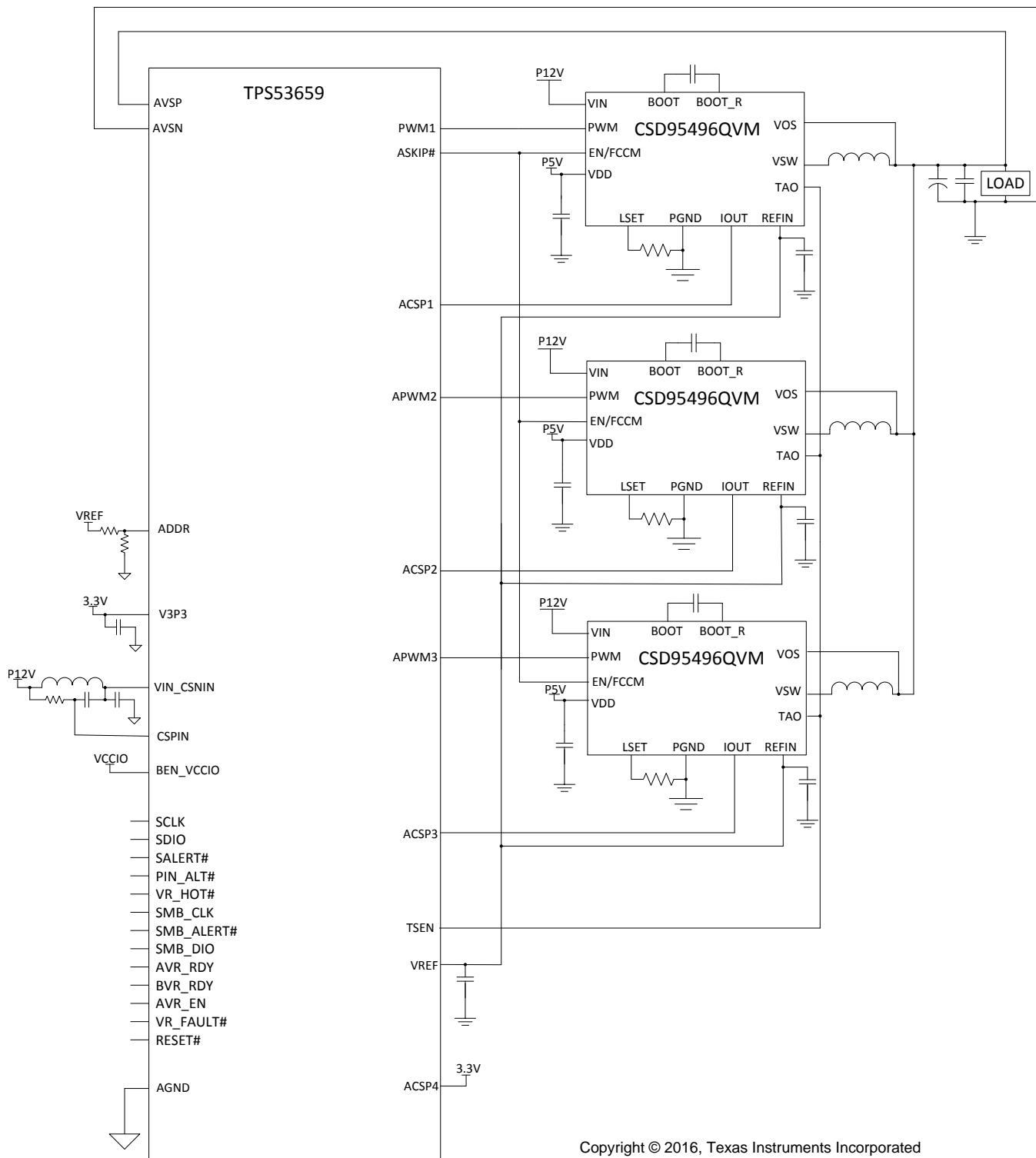


Figure 1. Application Schematic

Note: The schematic in [Figure 1](#) is a conceptual drawing only. Actual designs may require additional components not shown.

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

8.3 Trademarks

NexFET, E2E are trademarks of Texas Instruments.

All other trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

8.5 Glossary

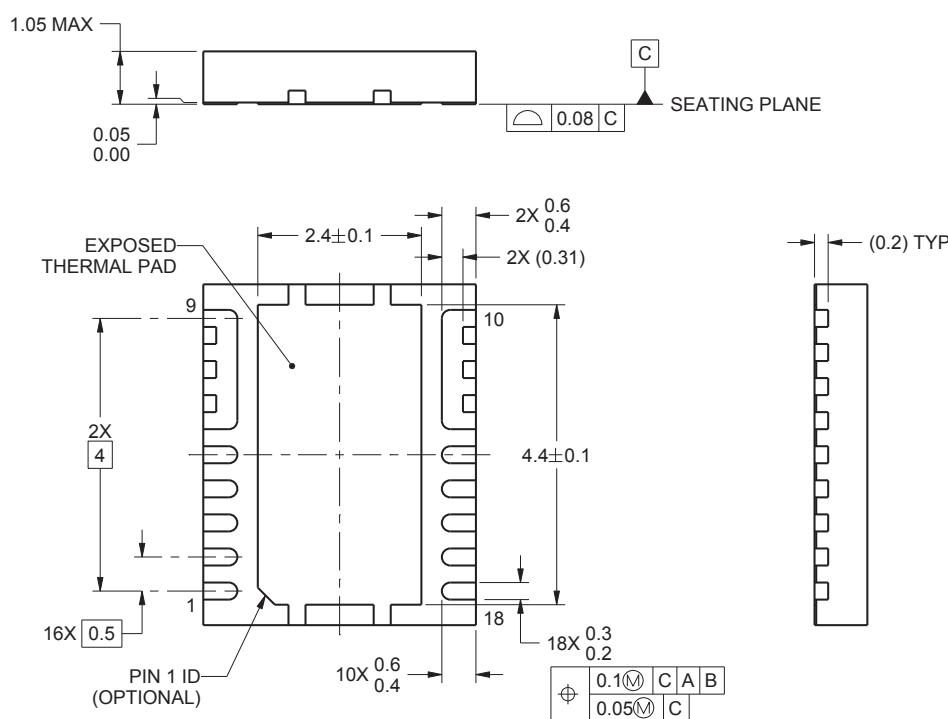
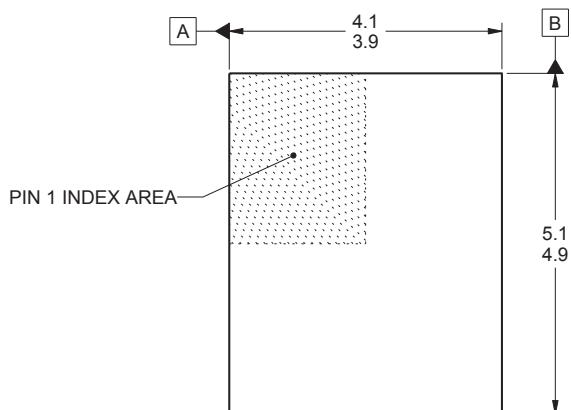
[SLYZ022 — TI Glossary](#).

This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

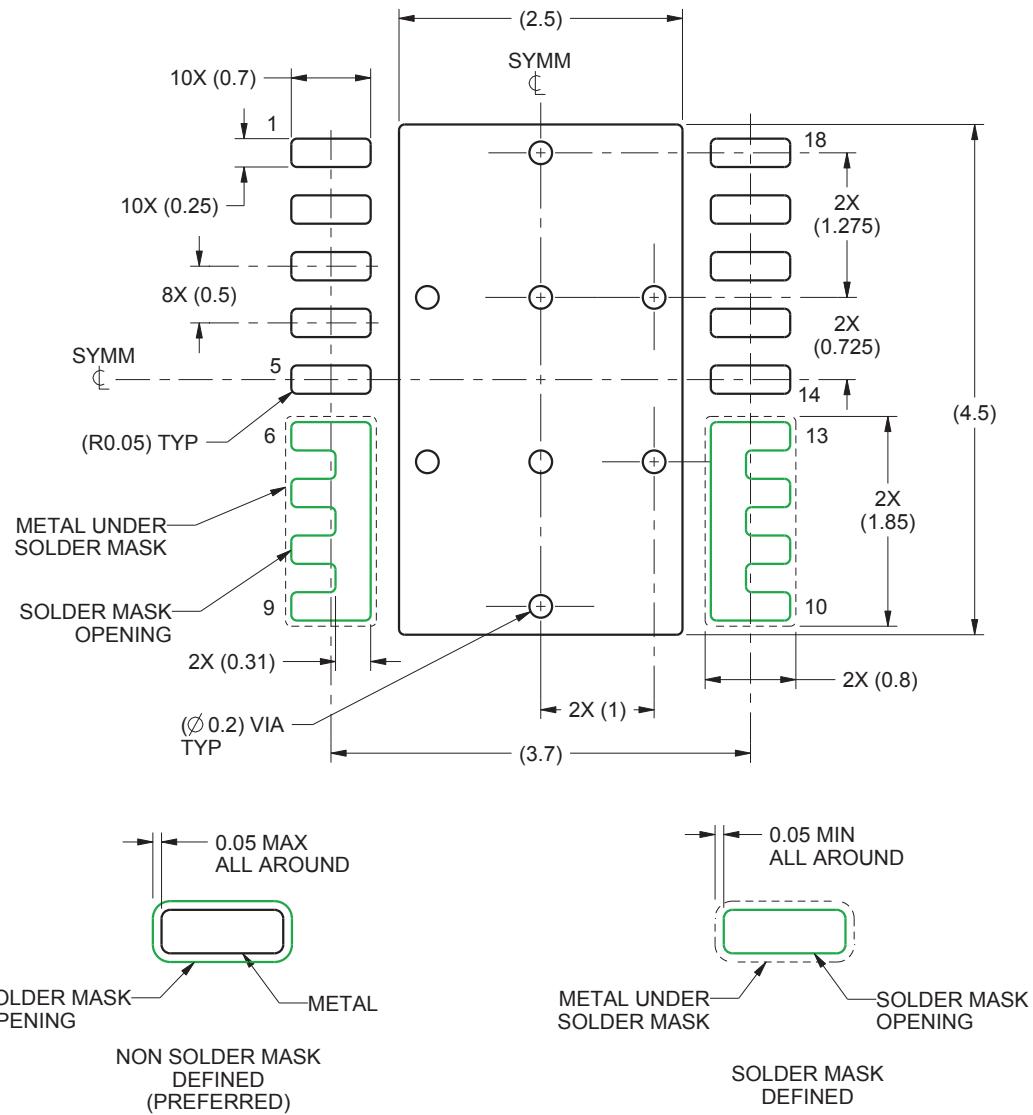
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

9.1 Mechanical Drawing



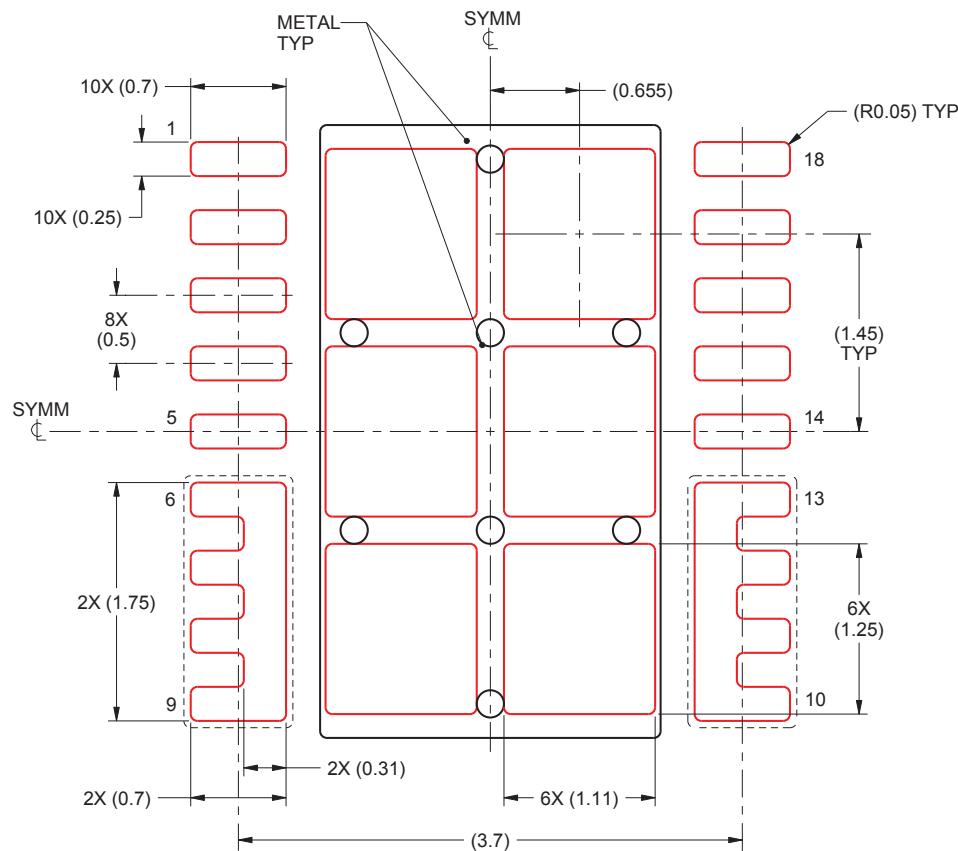
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

9.2 Recommended PCB Land Pattern



1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is designed to be soldered to a thermal pad on the board. For more information, see [QFN/SON PCB Attachment](#) (SLUA271).

9.3 Recommended Stencil Opening



1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD95496QVM	NRND	Production	VSON-CLIP (DMH) 18	2500 LARGE T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 150	95496QM
CSD95496QVMT	NRND	Production	VSON-CLIP (DMH) 18	250 SMALL T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 150	95496QM

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

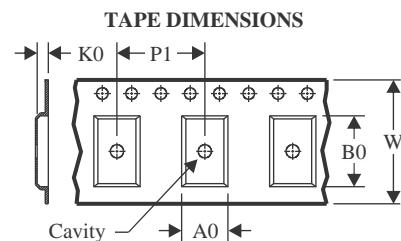
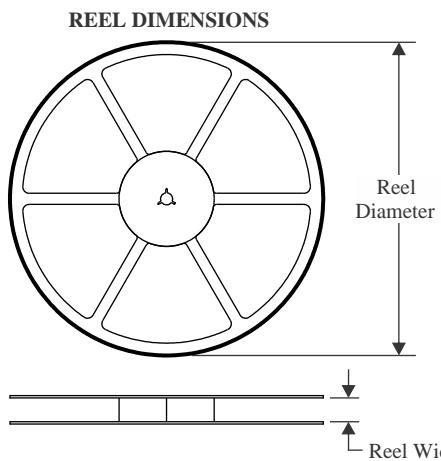
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

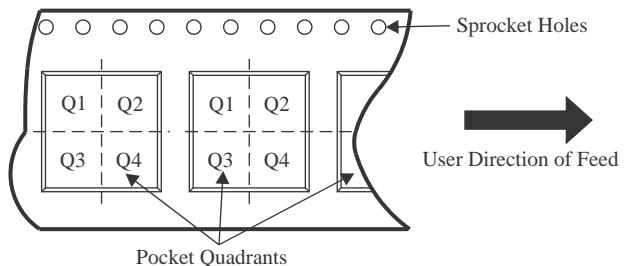
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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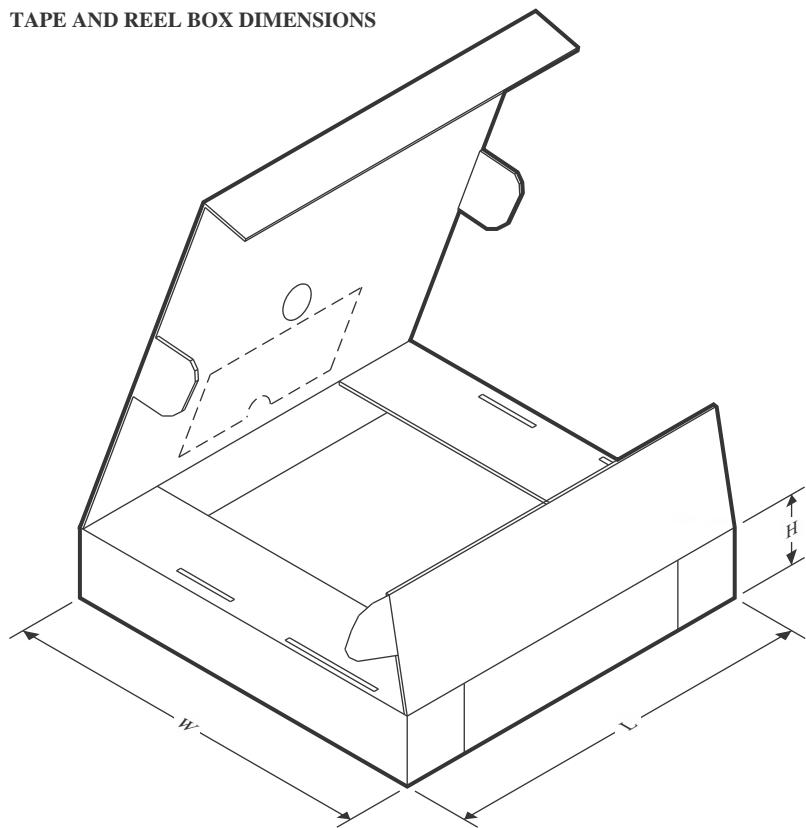
TAPE AND REEL INFORMATION


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD95496QVM	VSON-CLIP	DMH	18	2500	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
CSD95496QVMT	VSON-CLIP	DMH	18	250	180.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD95496QVM	VSON-CLIP	DMH	18	2500	367.0	367.0	38.0
CSD95496QVMT	VSON-CLIP	DMH	18	250	213.0	191.0	35.0

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Last updated 10/2025