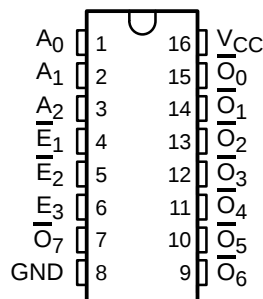
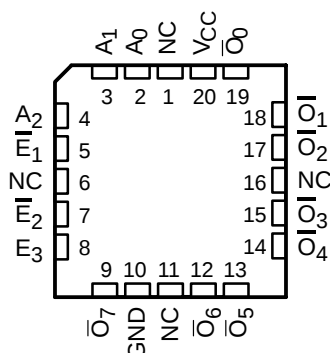


- Function, Pinout, and Drive Compatible With FCT and F Logic
- Reduced V_{OH} (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- I_{off} Supports Partial-Power-Down Mode Operation
- Matched Rise and Fall Times
- Fully Compatible With TTL Input and Output Logic Levels
- Dual 1-of-8 Decoder With Enables
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- CY54FCT138T
 - 32-mA Output Sink Current
 - 12-mA Output Source Current
- CY74FCT138T
 - 64-mA Output Sink Current
 - 32-mA Output Source Current

CY54FCT138T . . . D PACKAGE
CY74FCT138T . . . Q OR SO PACKAGE
(TOP VIEW)



CY54FCT138T . . . L PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'FCT138T devices are 1-of-8 decoders. These devices accept three binary weighted inputs (A_0 , A_1 , A_2) and, when enabled, provide eight mutually exclusive active-low outputs ($\overline{O}_0$ – $\overline{O}_7$). The 'FCT138T devices feature three enable inputs: two active low ($\overline{E}_1$, $\overline{E}_2$) and one active high (E_3).

All outputs are high unless $\overline{E}_1$ and $\overline{E}_2$ are low and E_3 is high. This multiple-enable function allows easy parallel expansion of the device to a 1-of-32 (five lines to 32 lines) decoder with just four 'FCT138T devices and one inverter.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

PIN DESCRIPTION

NAME	DESCRIPTION
A	Address inputs
$\overline{E}_1$, $\overline{E}_2$	Enable inputs (active low)
E_3	Enable input (active high)
$\overline{O}$	Outputs



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

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 On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

CY54FCT138T, CY74FCT138T 1-OF-8 DECODERS

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ORDERING INFORMATION

T _A	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QSOP – Q	Tape and reel	5	CY74FCT138CTQCT	FT138-3
	SOIC – SO	Tube	5	CY74FCT138CTSOC	FCT138C
		Tape and reel	5	CY74FCT138CTSOCT	
	QSOP – Q	Tape and reel	5.8	CY74FCT138ATQCT	FT138-1
	SOIC – SO	Tube	5.8	CY74FCT138ATSOC	FCT138A
		Tape and reel	5.8	CY74FCT138ATSOCT	
–55°C to 125°C	QSOP – Q	Tape and reel	9	CY74FCT138TQCT	FT138
	LCC – L	Tube	6	CY54FCT138CTLMB	
	LCC – L	Tube	12	CY54FCT138TLMB	
	CDIP – D	Tube	12	CY54FCT138TDMB	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E ₃	A ₀	A ₁	A ₂	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H	H
L	L	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = High logic level, L = Low logic level, X = Don't care



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The diagram illustrates a 3-to-8 decoder implemented using NAND gates. The inputs are A_0 , A_1 , and A_2 . The outputs are labeled $\overline{O}_0$ through $\overline{O}_7$. The circuit uses a combination of NAND gates and inverters to generate the eight output signals. The inputs A_0 , A_1 , and A_2 are connected to three NAND gates (labeled 1, 2, 3) to produce outputs $\overline{O}_0$ through $\overline{O}_7$. The diagram shows the internal wiring of the decoder, including the use of inverters and NAND gates to generate the eight output signals.

3

CY54FCT138T, CY74FCT138T 1-OF-8 DECODERS

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recommended operating conditions (see Note 2)

		CY54FCT138T			CY74FCT138T			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			–12			–32	mA
I_{OL}	Low-level output current			32			64	mA
T_A	Operating free-air temperature	–55		125	–40		85	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	CY54FCT138T			CY74FCT138T			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_{IN} = -18\text{ mA}$		–0.7	–1.2				V
	$V_{CC} = 4.75\text{ V}$, $I_{IN} = -18\text{ mA}$					–0.7	–1.2	
V_{OH}	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -12\text{ mA}$	2.4	3.3					V
	$V_{CC} = 4.75\text{ V}$, $I_{OH} = -32\text{ mA}$				2			
	$V_{CC} = 4.75\text{ V}$, $I_{OH} = -15\text{ mA}$				2.4	3.3		
V_{OL}	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 32\text{ mA}$	0.3	0.55					V
	$V_{CC} = 4.75\text{ V}$, $I_{OL} = 64\text{ mA}$				0.3	0.55		
V_{hys}	All inputs	0.2			0.2			V
I_I	$V_{CC} = 5.5\text{ V}$, $V_{IN} = V_{CC}$			5				μA
	$V_{CC} = 5.25\text{ V}$, $V_{IN} = V_{CC}$						5	
I_{IH}	$V_{CC} = 5.5\text{ V}$, $V_{IN} = 2.7\text{ V}$			± 1				μA
	$V_{CC} = 5.25\text{ V}$, $V_{IN} = 2.7\text{ V}$						± 1	
I_{IL}	$V_{CC} = 5.5\text{ V}$, $V_{IN} = 0.5\text{ V}$			± 1				μA
	$V_{CC} = 5.25\text{ V}$, $V_{IN} = 0.5\text{ V}$						± 1	
$I_{OS}^\ddagger$	$V_{CC} = 5.5\text{ V}$, $V_{OUT} = 0\text{ V}$	–60	–120	–225				mA
	$V_{CC} = 5.25\text{ V}$, $V_{OUT} = 0\text{ V}$				–60	–120	–225	
I_{off}	$V_{CC} = 0\text{ V}$, $V_{OUT} = 4.5\text{ V}$			± 1			± 1	μA
I_{CC}	$V_{CC} = 5.5\text{ V}$, $V_{IN} \leq 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$	0.1	0.2					mA
	$V_{CC} = 5.25\text{ V}$, $V_{IN} \leq 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$				0.1	0.2		
ΔI_{CC}	$V_{CC} = 5.5\text{ V}$, $V_{IN} = 3.4\text{ V}^\S$, $f_1 = 0$, Outputs open	0.5	2					mA
	$V_{CC} = 5.25\text{ V}$, $V_{IN} = 3.4\text{ V}^\S$, $f_1 = 0$, Outputs open				0.5	2		
$I_{CCD}^\P$	$V_{CC} = 5.5\text{ V}$, Outputs open, One bit switching at 50% duty cycle, $V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$	0.06	0.12					mA/ MHz
	$V_{CC} = 5.25\text{ V}$, Outputs open, One bit switching at 50% duty cycle, $V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$				0.06	0.12		

† Typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

§ Per TTL-driven input ($V_{IN} = 3.4\text{ V}$); all other inputs at V_{CC} or GND

¶ This parameter is derived for use in total power-supply calculations.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS			CY54FCT138T			CY74FCT138T			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I _C [#]	V _{CC} = 5.5 V, Outputs open, Switch $\overline{E}_1$, $\overline{E}_2$, or E ₃	One output switching at f ₁ = 10 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V	0.7	1.4				mA	
			V _{IN} = 3.4 V or GND	1	2.4					
	V _{CC} = 5.25 V, Outputs open, Switch $\overline{E}_1$, $\overline{E}_2$, or E ₃	One output switching at f ₁ = 10 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V			0.7	1.4			
			V _{IN} = 3.4 V or GND			1	2.4			
C _i				5	10	5	10		pF	
C _O				9	12	9	12		pF	

† Typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

$I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

Where:

I_C = Total supply current

I_{CC} = Power-supply current with CMOS input levels

ΔI_{CC} = Power-supply current for a TTL high input ($V_{IN} = 3.4 \text{ V}$)

D_H = Duty cycle for TTL inputs high

N_T = Number of TTL inputs at D_H

I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)

f_0 = Clock frequency for registered devices, otherwise zero

f_1 = Input signal frequency

N_1 = Number of inputs changing at f_1

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the I_{CC} formula.

switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY54FCT138T		CY54FCT138CT		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	A	$\bar{O}$	1.5	12	1.5	6	ns
t_{PHL}			1.5	12	1.5	6	
t_{PLH}	$\bar{E}_1$ or $\bar{E}_2$	$\bar{O}$	1.5	12.5	1.5	6.1	ns
t_{PHL}			1.5	12.5	1.5	6.1	
t_{PLH}	E_3	$\bar{O}$	1.5	12.5	1.5	6.1	ns
t_{PHL}			1.5	12.5	1.5	6.1	

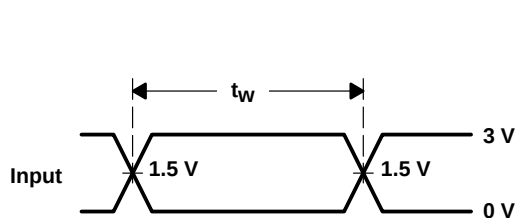
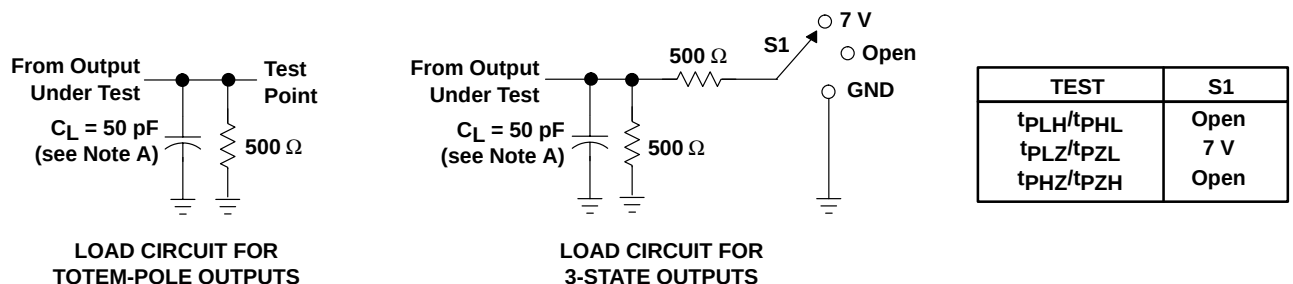
switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT138T		CY74FCT138AT		CY74FCT138CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	$\bar{O}$	1.5	9	1.5	5.8	1.5	5	ns
t_{PHL}			1.5	9	1.5	5.8	1.5	5	
t_{PLH}	$\bar{E}_1$ or $\bar{E}_2$	$\bar{O}$	1.5	9	1.5	5.9	1.5	5	ns
t_{PHL}			1.5	9	1.5	5.9	1.5	5	
t_{PLH}	E_3	$\bar{O}$	1.5	9	1.5	5.9	1.5	5	ns
t_{PHL}			1.5	9	1.5	5.9	1.5	5	

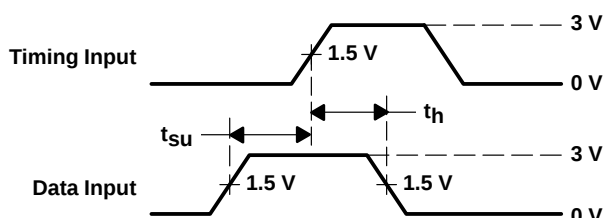
CY54FCT138T, CY74FCT138T 1-OF-8 DECODERS

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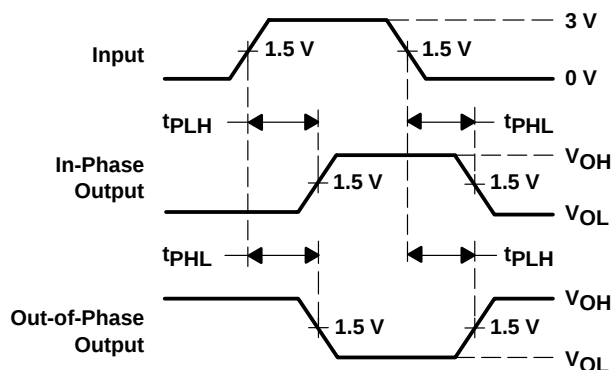
PARAMETER MEASUREMENT INFORMATION



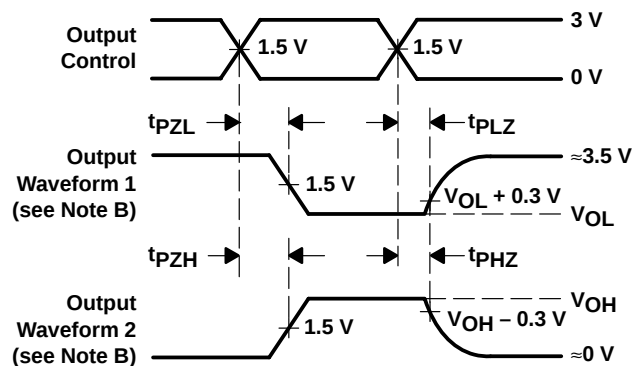
**VOLTAGE WAVEFORMS
PULSE DURATION**



**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9223302M2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9223302M2A CY54FCT 138TLMB
5962-9223302MEA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9223302ME A CY54FCT138TDMB
5962-9223306M2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9223306M2A CY54FCT 138CTLMB
5962-9223306MEA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9223306ME A
CY54FCT138CTLMB	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9223306M2A CY54FCT 138CTLMB
CY54FCT138TDMB	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9223302ME A CY54FCT138TDMB
CY54FCT138TLMB	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9223302M2A CY54FCT 138TLMB
CY74FCT138ATQCT	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FT138-1
CY74FCT138ATQCT.B	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FT138-1
CY74FCT138ATSOC	Active	Production	SOIC (DW) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT138A
CY74FCT138ATSOC.B	Active	Production	SOIC (DW) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT138A
CY74FCT138ATSOCG4	Active	Production	SOIC (DW) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT138A
CY74FCT138ATSOCT	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT138A
CY74FCT138ATSOCT.B	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT138A
CY74FCT138CTQCT	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FT138-3
CY74FCT138CTQCT.B	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FT138-3

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CY74FCT138CTSOC	Active	Production	SOIC (DW) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT138C
CY74FCT138CTSOC.B	Active	Production	SOIC (DW) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT138C
CY74FCT138TQCT	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FT138
CY74FCT138TQCT.B	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FT138

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT138ATQCT	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
CY74FCT138ATSOCT	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
CY74FCT138CTQCT	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
CY74FCT138TQCT	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT138ATQCT	SSOP	DBQ	16	2500	340.5	338.1	20.6
CY74FCT138ATSOCT	SOIC	DW	16	2000	350.0	350.0	43.0
CY74FCT138CTQCT	SSOP	DBQ	16	2500	340.5	338.1	20.6
CY74FCT138TQCT	SSOP	DBQ	16	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9223302M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9223306M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
CY54FCT138CTLMB	FK	LCCC	20	55	506.98	12.06	2030	NA
CY54FCT138TLMB	FK	LCCC	20	55	506.98	12.06	2030	NA
CY74FCT138ATSOC	DW	SOIC	16	40	506.98	12.7	4826	6.6
CY74FCT138ATSOC.B	DW	SOIC	16	40	506.98	12.7	4826	6.6
CY74FCT138ATSOCG4	DW	SOIC	16	40	506.98	12.7	4826	6.6
CY74FCT138CTSOC	DW	SOIC	16	40	506.98	12.7	4826	6.6
CY74FCT138CTSOC.B	DW	SOIC	16	40	506.98	12.7	4826	6.6

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