TEXAS INSTRUMENTS

CY74FCT16652T
CY74FCT162652T

SCCS061B - July 1994 - Revised September 2001

16-Bit Registered Transceivers

Features

- **I_{off} supports partial-power-down mode operation**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Typical output skew < 250 ps**
- **ESD > 2000V**
- **TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages**
- **Industrial temperature range of −40˚C to +85˚C**
- **V_{CC} = 5V ± 10%**

CY74FCT16652T Features:

- **64 mA sink current, 32 mA source current**
- **Typical V_{OLP} (ground bounce) <1.0V at V_{CC} = 5V, T_A = 25˚C**

CY74FCT162652T Features:

- **Balanced 24 mA output drivers**
- **Reduced system switching noise**
- **Typical V_{OLP} (ground bounce) <0.6V at V_{CC} = 5V, T_A= 25˚C**

Functional Description

These 16-bit, high-speed, low-power, registered transceivers that are organized as two independent 8-bit bus transceivers with three-state D-type registers and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal storage registers. OEAB and $\overline{OEBA}$ control pins are provided to control the transceiver functions. SAB and SBA control pins are provided to select either real-time or stored data transfer.

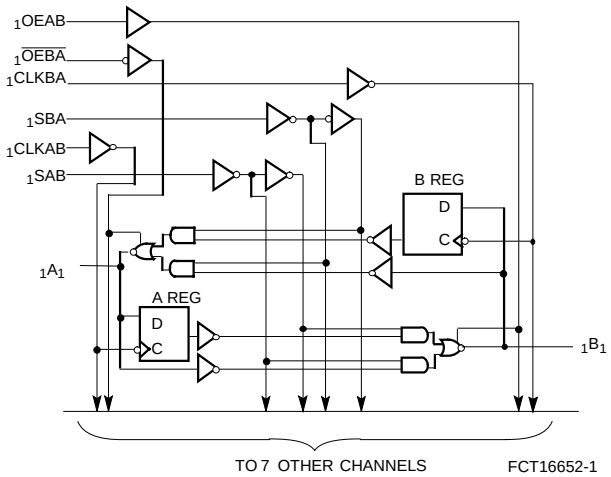
Data on the A or B data bus, or both, can be stored in the internal D flip-flops by LOW-to-HIGH transitions at the appropriate clock pins (CLKAB or CLKBA), regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{OEBA}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

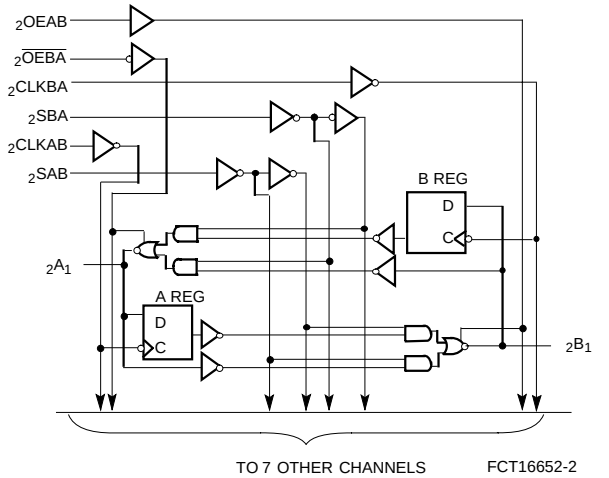
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The CY74FCT16652T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162652T has 24-mA balanced output drivers with current-limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162652T is ideal for driving transmission lines.

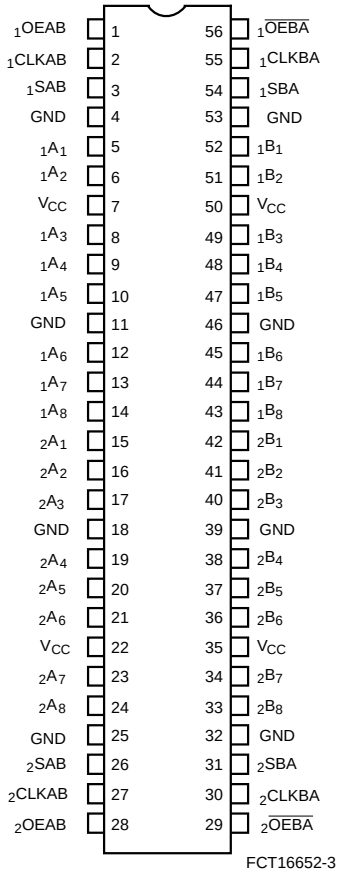
Logic Block Diagrams





Pin Configuration

SSOP/TSSOP
Top View



FCT16652-3

Pin Description

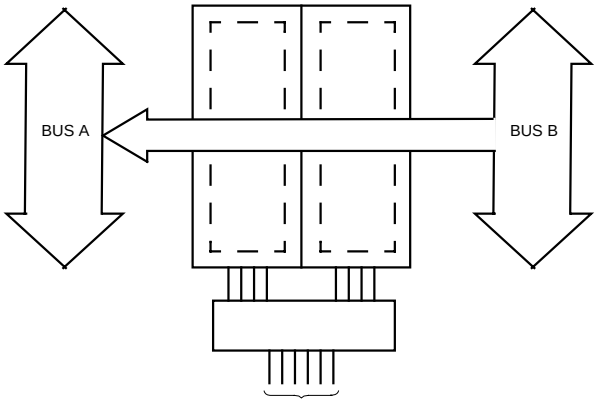
Name	Description
A	Data Register A Inputs Data Register B Outputs
B	Data Register B Inputs Data Register A Outputs
CLKAB, CLKBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
OEAB, $\overline{OEBA}$	Output Enable Inputs

Function Table[1]

Inputs						Data I/O[2]		Operation or Function
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA	A	B	
L L	H H	H or L ↓	H or L ↓	X X	X X	Input	Input	Isolation Store A and B Data
X H	H H	↓ ↓	H or L ↓	X X[3]	X X	Input Input	Unspecified[2] Output	Store A, Hold B Store A in Both Registers
L L	X L	H or L ↓	↓ ↓	X X	X X[3]	Unspecified[2]	Input Input	Hold A, Store B Store B in both Registers
L L	L L	X X	X H or L	X X	L H	Output	Input	Real Time B Data to A Bus Stored B Data to A Bus
H H	H H	X H or L	X X	L H	X X	Input	Output	Real Time A Data to B Bus Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

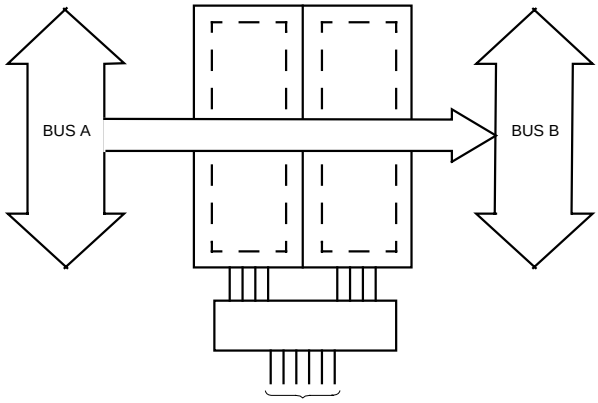
Notes:

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↓ =LOW-to-HIGH Transition
2. The data output functions may be enabled or disabled by various signals at the OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
3. Select control=L; clocks can occur simultaneously.
   Select control=H; clocks must be staggered to load both registers.



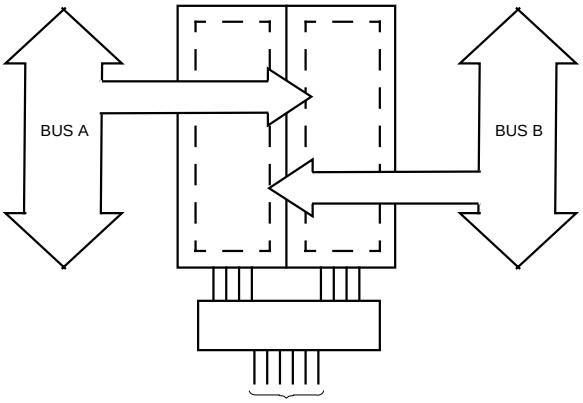
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

Real-Time Transfer
Bus B to Bus A



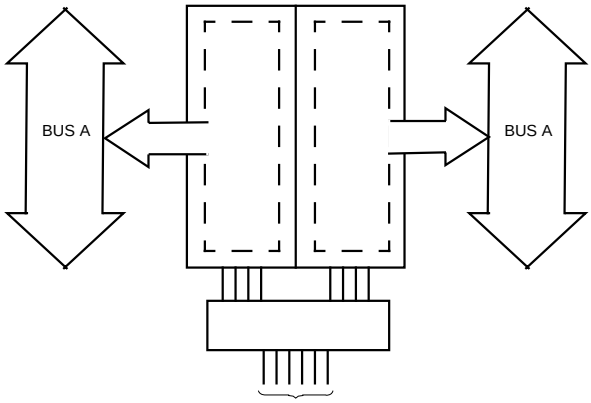
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	L	X	X	L	X

Real-Time Transfer
Bus A to Bus B



OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
X	H	⌐	X	X	X
L	X	X	⌐	X	X
L	H	⌐	⌐	X	X

Storage from
A and/or B



OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	L	H or L	H or L	H	H

Transfer Stored Data
to A and/or B

Maximum Ratings[4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....Com'l –55°C to +125°C

Ambient Temperature with
Power Applied .....Com'l –55°C to +125°C

DC Input Voltage .....–0.5V to +7.0V

DC Output Voltage .....–0.5V to +7.0V

DC Output Current
(Maximum Sink Current/Pin) .....–60 to +120 mA

Power Dissipation 1.0W

Static Discharge Voltage.....>2001V
(per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40°C to +85°C	5V ± 10%

Note:

4. Stresses greater than those listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions[5]	Min.	Typ.[6]	Max.	Unit
V_{IH}	Input HIGH Voltage	Logic HIGH Level	2.0			V
V_{IL}	Input LOW Voltage	Logic LOW Level			0.8	V
V_H	Input Hysteresis			100		mV
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=–18 mA		–0.7	–1.2	V
I_{IH}	Input HIGH Current	V_{CC}=Max., V_I=V_{CC}			±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_I=GND			±1	µA
I_{OZH}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=2.7V			±1	µA
I_{OZL}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=0.5V			±1	µA
I_{OS}	Short Circuit Current[8]	V_{CC}=Max., V_{OUT}=GND	–80	–140	–200	mA
I_O	Output Drive Current[8]	V_{CC}=Max., V_{OUT}=2.5V	–50		–180	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}≤4.5V[7]			±1	µA

Output Drive Characteristics for CY74FCT16652T

Parameter	Description	Test Conditions[5]	Min.	Typ.[6]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=–3 mA	2.5	3.5		V
		V_{CC}=Min., I_{OH}=–15 mA	2.4	3.5		
		V_{CC}=Min., I_{OH}=–32 mA	2.0	3.0		
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162652T

Parameter	Description	Test Conditions[5]	Min.	Typ.[6]	Max.	Unit
I_{ODL}	Output LOW Current[8]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	60	115	150	mA
I_{ODH}	Output HIGH Current[8]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=–24 mA	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=24 mA		0.3	0.55	V

Capacitance (T_A = +25˚C, f = 1.0 MHz)

Parameter	Description[10]	Test Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

Notes:

5. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
6. Typical values are at V_{CC}=5.0V, +25°C ambient.
7. Tested at T_A= +25°C.
8. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
9. Duration of the condition cannot exceed one second.
10. This parameter is measured at characterization but not tested.

Power Supply Characteristics

Param.	Description	Test Conditions[11]		Min.	Typ.[12]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max.	$V_{IN} \le 0.2V$ $V_{IN} \ge V_{CC}-0.2V$	—	5	500	μA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN}=3.4V[13]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[14]	V_{CC}=Max. Outputs Open OEAB=$\overline{OEAB}$=GND One Input Toggling 50% Duty Cycle	$V_{IN}=V_{CC}$ or V_{IN}=GND	—	75	120	μA/ MHz
I_C	Total Power Supply Current[15]	V_{CC}=Max. Outputs Open f_0=10 MHz (CLKBA) 50% Duty Cycle OEAB=$\overline{OEBA}$=GND One-Bit Toggling f_1=5 MHz 50% Duty Cycle	$V_{IN}=V_{CC}$ or V_{IN}=GND	—	0.8	1.7	mA
			V_{IN}=3.4V or V_{IN}=GND	—	1.3	3.2	mA
		V_{CC}=Max. Outputs Open f_0=10 MHz (CLKBA) 50% Duty Cycle OEAB=$\overline{OEBA}$=GND Sixteen Bits Toggling f_1=2.5 MHz 50% Duty Cycle	$V_{IN}=V_{CC}$ or V_{IN}=GND	—	3.8	6.5[16]	mA
			V_{IN}=3.4V or V_{IN}=GND	—	8.3	20.0[16]	mA

Notes:

11. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
12. Typical values are at V_{CC}=5.0V +25° ambient.
13. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
14. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
15. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
16. Values for these conditions are examples of the I_{CC} formula. These limits are specified but not tested.

Switching Characteristics Over the Operating Range[17]

Parameter	Description	CY74FCT16652AT CY74FCT162652AT		Unit	Fig. No.[18]
		Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	1.5	6.3	ns	1, 3
t_{PZH} t_{PHL}	Output Enable Time OEAB or $\overline{OEBA}$ to Bus	1.5	9.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time OEAB or $\overline{OEBA}$ to Bus	1.5	6.3	ns	1, 7, 8
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	1.5	6.3	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to Bus	1.5	7.7	ns	1, 5
t_{SU}	Set-Up time HIGH or LOW Bus to Clock	2.0	—	ns	4
t_H	Hold Time HIGH or LOW Bus to Clock	1.5	—	ns	4
t_W	Clock Pulse Width HIGH or LOW	5.0	—	ns	5
$t_{SK(O)}$	Output Skew[19]	—	0.5	ns	

Parameter	Description	CY74FCT16652CT CY74FCT162652CT		Unit	Fig. No.[18]
		Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	1.5	5.4	ns	1, 3
t_{PZH} t_{PHL}	Output Enable Time OEAB or $\overline{OEBA}$ to Bus	1.5	7.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time OEAB or $\overline{OEBA}$ to Bus	1.5	6.3	ns	1, 7, 8
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	1.5	5.7	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to Bus	1.5	6.2	ns	1, 5
t_{SU}	Set-Up Time HIGH or LOW Bus to Clock	2.0	—	ns	4
t_H	Hold Time HIGH or LOW Bus to Clock	1.5	—	ns	4
t_W	Clock Pulse Width HIGH or LOW	5.0	—	ns	5
$t_{SK(O)}$	Output Skew[19]	—	0.5	ns	

Notes:
17. Minimum limits are specified, but not tested, on propagation delays.
18. See “Parameter Measurement Information” in the General Information section.
19. Skew between any two outputs of the same package switching in the same direction. This parameter ensured by design.

Ordering Information CY74FCT16652

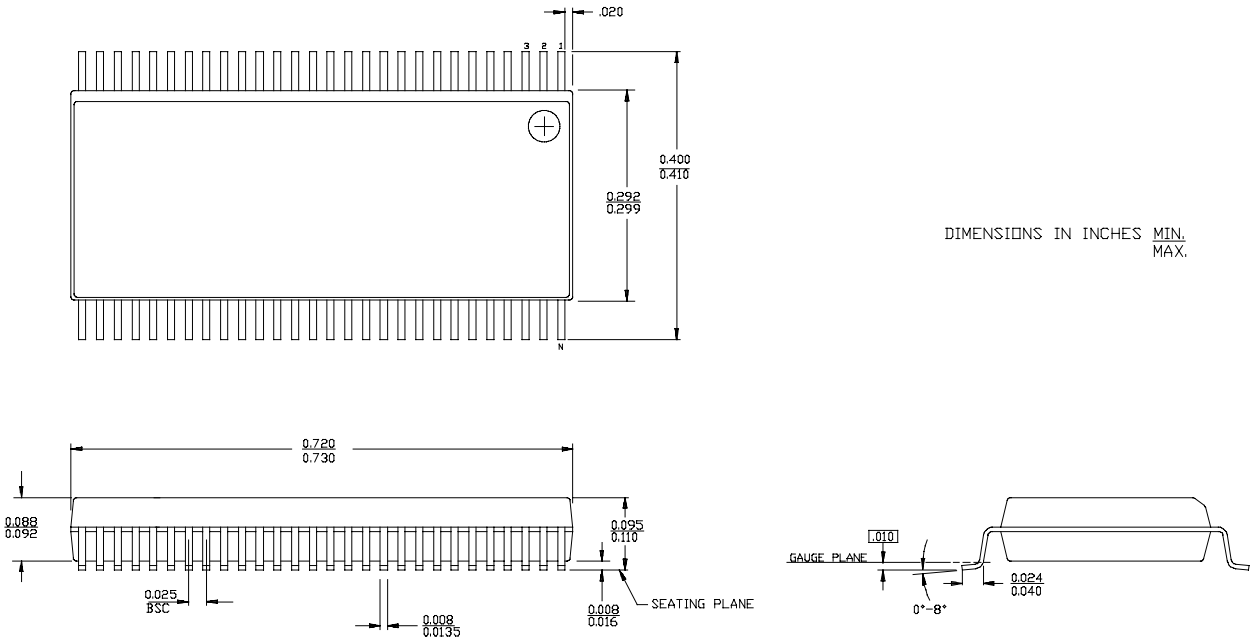
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.4	CY74FCT16652CTPVC/PVCT	O56	56-Lead (300-Mil) SSOP	Industrial
6.3	CY74FCT16652ATPVC/PVCT	O56	56-Lead (300-Mil) SSOP	Industrial

Ordering Information CY74FCT162652

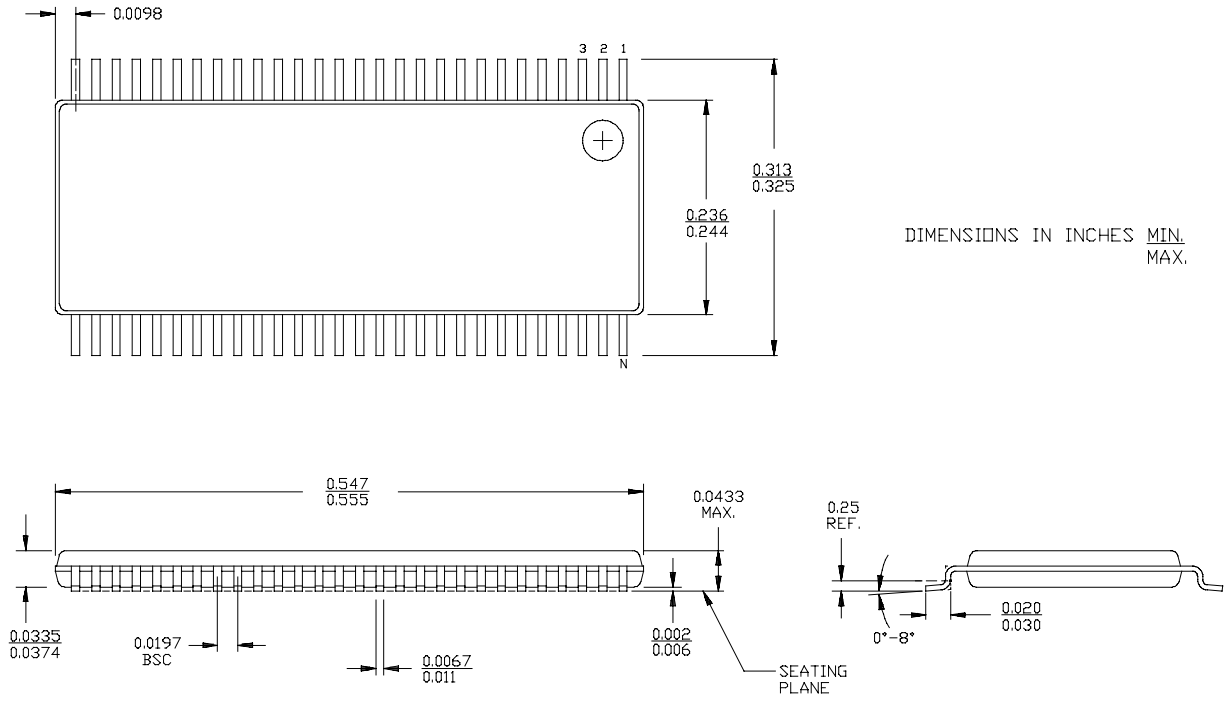
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.4	74FCT162652CTPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162652CTPVC	O56	56-Lead (300-Mil) SSOP	
	74FCT162652CTPVCT	O56	56-Lead (300-Mil) SSOP	
6.3	CY74FCT162652ATPVC	O56	56-Lead (300-Mil) SSOP	Industrial
	74FCT162652ATPVCT	O56	56-Lead (300-Mil) SSOP	

Package Diagrams

56-Lead Shrunk Small Outline Package O56



56-Lead Thin Shrunk Small Outline Package Z56



PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74FCT162652CTPACT	Obsolete	Production	TSSOP (DGG) | 56	-	-	Call TI	Call TI	-40 to 85	FCT162652C
CY74FCT16652ATPVCT	Obsolete	Production	SSOP (DL) | 56	-	-	Call TI	Call TI	-40 to 85	FCT16652A

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

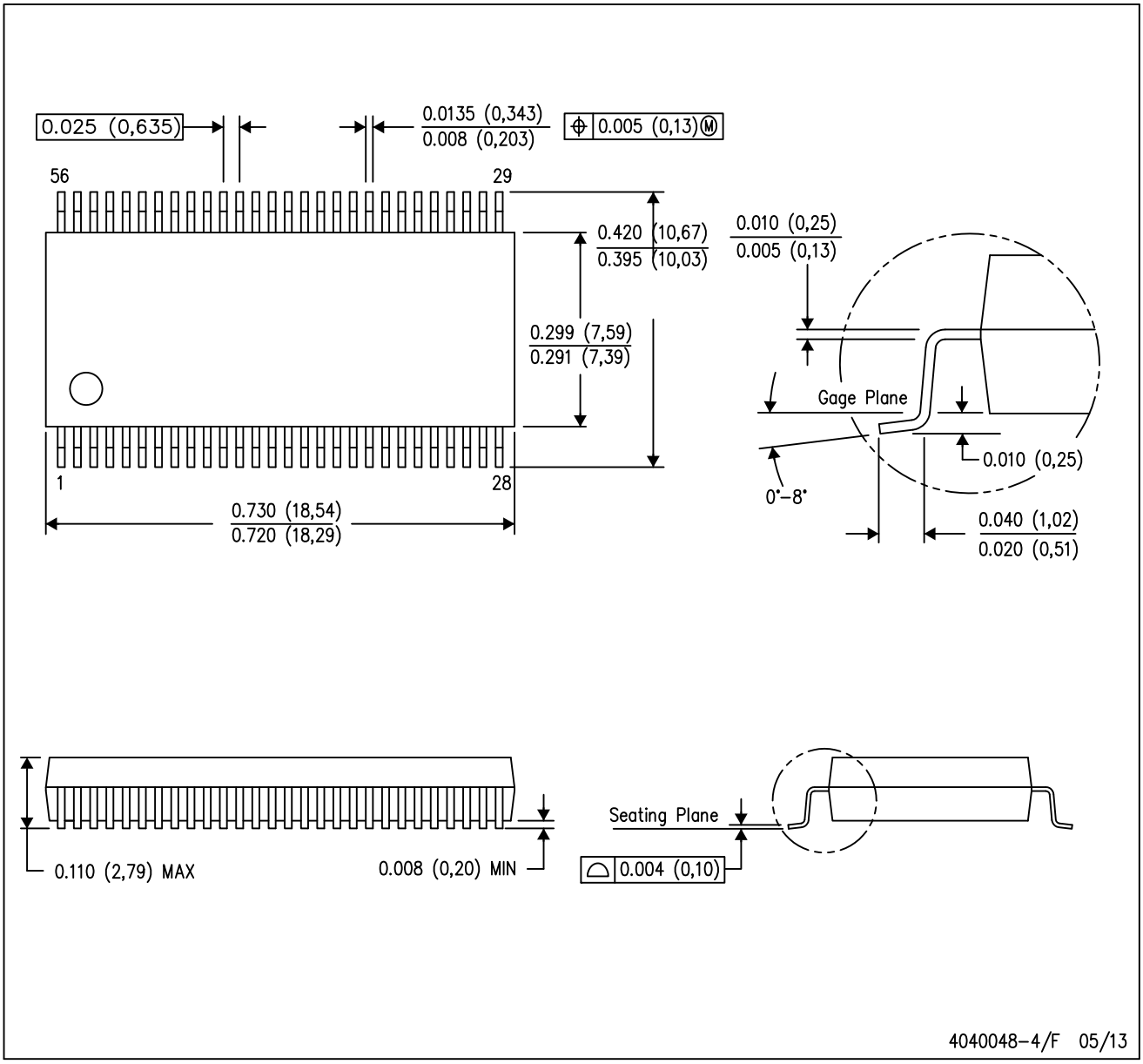
(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

DL (R–PDSO–G56) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

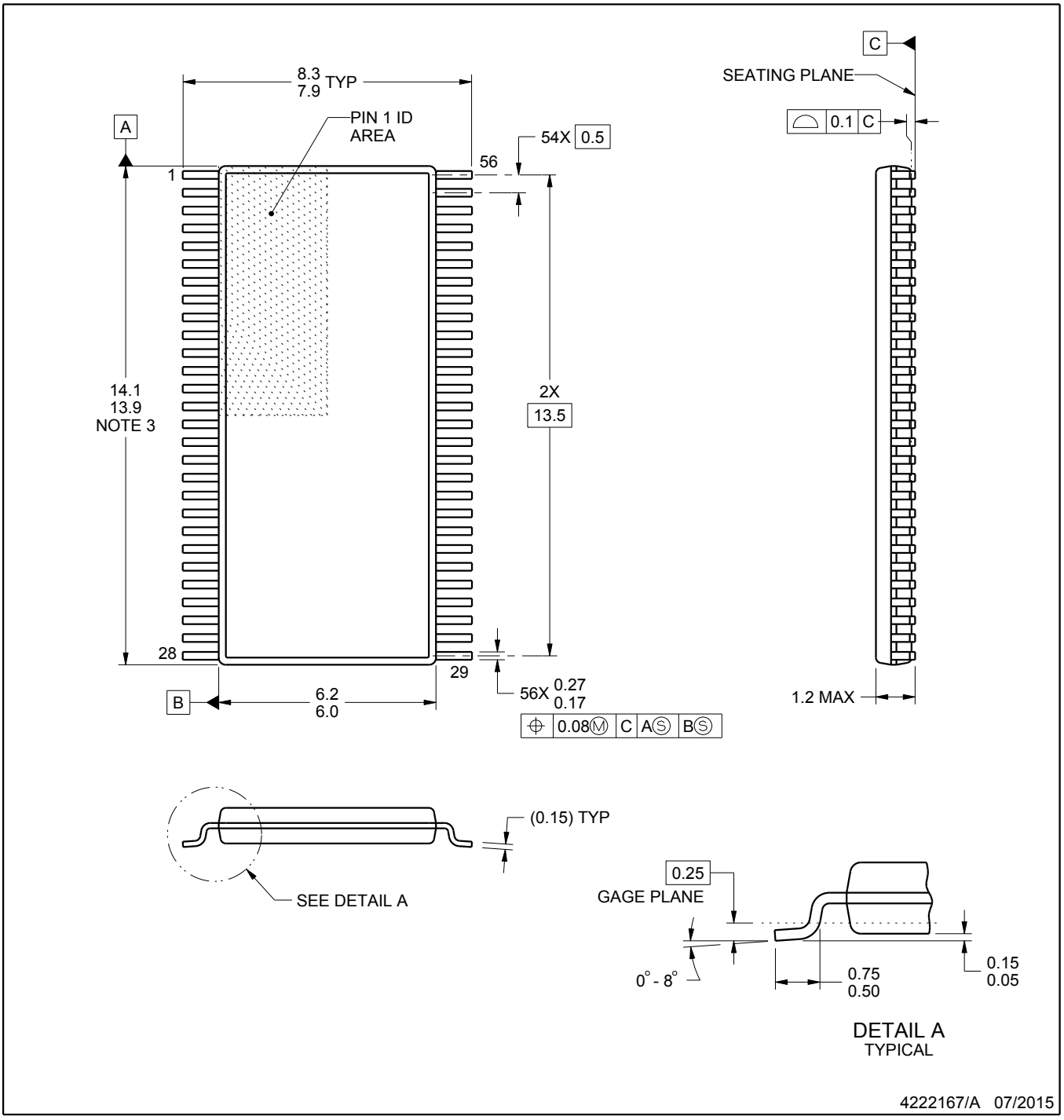
PowerPAD is a trademark of Texas Instruments.

PACKAGE OUTLINE

DGG0056A

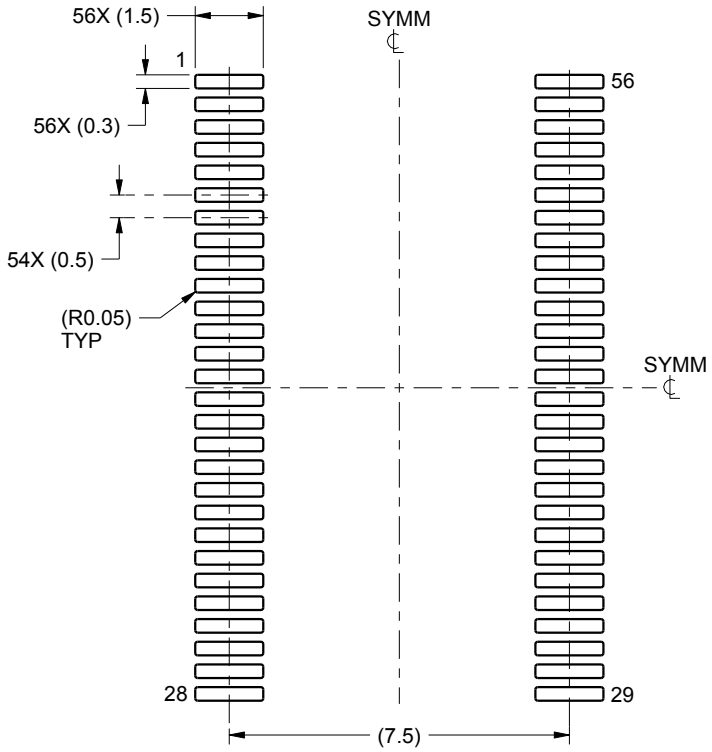
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

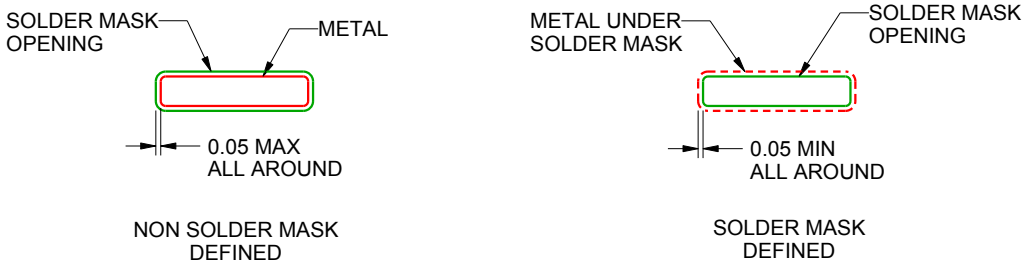


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

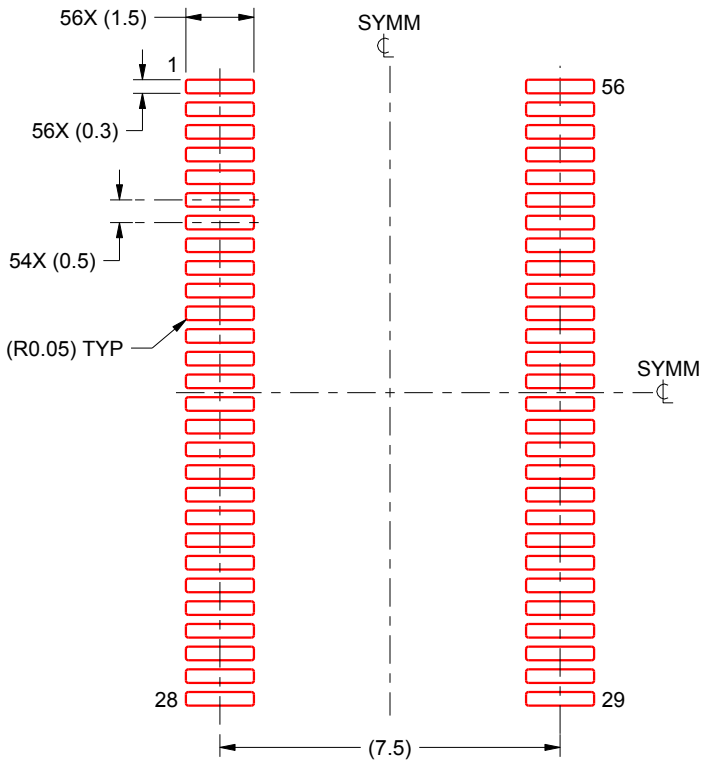


SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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