



SCCS064B - August 1994 - Revised September 2001

CY74FCT16827T CY74FCT162827T

20-Bit Buffers/Line Drivers

Features

- I_{off} Supports Partial-Power-Down Mode Operation
- Edge-rate control circuitry for significantly improved noise characteristics
- Typical output skew < 250 ps
- ESD > 2000V
- TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages
- Industrial temperature range of -40°C to $+85^{\circ}\text{C}$
- $V_{CC} = 5V \pm 10\%$

CY74FCT16827T Features:

- 64 mA sink current, 32 mA source current
- Typical V_{OLP} (ground bounce) < 1.0V at $V_{CC} = 5V$, $T_A = 25^{\circ}\text{C}$

CY74FCT162827T Features:

- Balanced 24 mA output drivers
- Reduced system switching noise
- Typical V_{OLP} (ground bounce) < 0.6V at $V_{CC} = 5V$, $T_A = 25^{\circ}\text{C}$

Functional Description

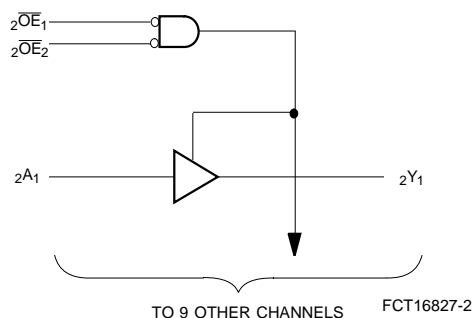
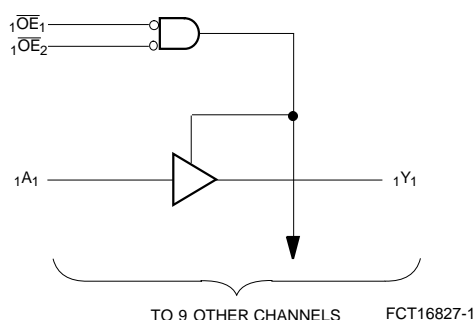
The CY74FCT16827T 20-bit buffer/line driver and the CY74FCT162827T 20-bit buffer/line driver provide high-performance bus interface buffering for wide data/address paths or buses carrying parity. These parts can be used as a single 20-bit buffer or two 10-bit buffers. Each 10-bit buffer has a pair of NANDed OE for increased flexibility.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The CY74FCT16827T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

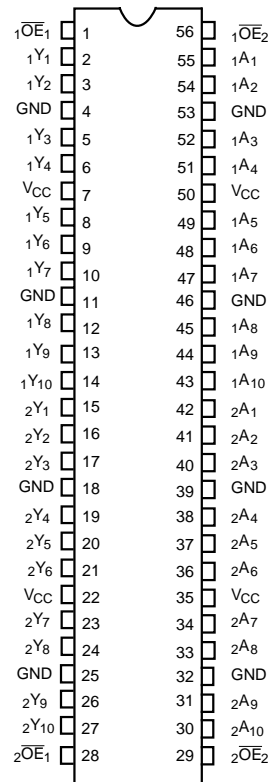
The CY74FCT162827T has 24-mA balanced output drivers with current-limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162827T is ideal for driving transmission lines.

Logic Block Diagrams



Pin Configuration

SSOP/TSSOP Top View



FCT16827-3

Pin Description

Name	Description
OE	Output Enable Inputs (Active LOW)
A	Data Inputs
Y	Three-State Outputs

Function Table^[1]

Inputs			Outputs
OE ₁	OE ₂	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

Maximum Ratings^[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature..... –55°C to +125°C

Ambient Temperature with
Power Applied..... –55°C to +125°C

DC Input Voltage–0.5V to +7.0V

DC Output Voltage–0.5V to +7.0V

DC Output Current
(Maximum Sink Current/Pin)–60 to +120 mA

Power Dissipation 1.0W

Static Discharge Voltage.....>2001V
(per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V _{CC}
Industrial	–40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. ^[4]	Max.	Unit
V _{IH}	Input HIGH Voltage		2.0			V
V _{IL}	Input LOW Voltage				0.8	V
V _H	Input Hysteresis ^[5]			100		mV
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =–18 mA		–0.7	–1.2	V
I _{IH}	Input HIGH Current	V _{CC} =Max., V _I =V _{CC}			±1	μA
I _{IL}	Input LOW Current	V _{CC} =Max., V _I =GND			±1	μA
I _{OZH}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =2.7V			±1	μA
I _{OZL}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =0.5V			±1	μA
I _{OS}	Short Circuit Current ^[6]	V _{CC} =Max., V _{OUT} =GND	–80	–140	–200	mA
I _O	Output Drive Current ^[6]	V _{CC} =Max., V _{OUT} =2.5V	–50		–180	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} ≤4.5V ^[7]			±1	μA

Output Drive Characteristics for CY74FCT16827T

Parameter	Description	Test Conditions	Min.	Typ. ^[4]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =–3 mA	2.5	3.5		V
		V _{CC} =Min., I _{OH} =–15 mA	2.4	3.5		
		V _{CC} =Min., I _{OH} =–32 mA	2.0	3.0		
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA		0.2	0.55	V

1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care. Z = HIGH Impedance.

2. Operation beyond the limits set forth may impair the useful life of the device. Unless noted, these limits are over the operating free-air temperature range.

3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

4. Typical values are at V_{CC}= 5.0V, T_A= +25°C ambient.

5. This parameter is specified but not tested.

6. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

7. Tested at +25°C.

Output Drive Characteristics for CY74FCT162827T

Parameter	Description	Test Conditions	Min.	Typ. ^[4]	Max.	Unit
I_{ODL}	Output LOW Current ^[6]	$V_{CC}=5V$, $V_{IN}=V_{IH}$ or V_{IL} , $V_{OUT}=1.5V$	60	115	150	mA
I_{ODH}	Output HIGH Current ^[6]	$V_{CC}=5V$, $V_{IN}=V_{IH}$ or V_{IL} , $V_{OUT}=1.5V$	-60	-115	-150	mA
V_{OH}	Output HIGH Voltage	$V_{CC}=\text{Min.}$, $I_{OH}=-24\text{ mA}$	2.4	3.3		V
V_{OL}	Output LOW Voltage	$V_{CC}=\text{Min.}$, $I_{OL}=24\text{ mA}$		0.3	0.55	V

Capacitance^[5] ($T_A = +25^\circ\text{C}$, $f = 1.0\text{ MHz}$)

Parameter	Description	Test Conditions	Typ. ^[4]	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	4.5	6.0	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	5.5	8.0	pF

Power Supply Characteristics

Parameter	Description	Test Conditions		Min.	Typ. ^[4]	Max.	Unit
I _{CC}	Quiescent Power Supply Current	V _{CC} =Max.	V _{IN} ≤0.2V, V _{IN} ≥V _{CC} −0.2V	—	5	500	μA
ΔI _{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V _{CC} =Max.	V _{IN} =3.4V ^[8]	—	0.5	1.5	mA
I _{CCD}	Dynamic Power Supply Current ^[9]	V _{CC} =Max., One Input Toggling, 50% Duty Cycle, Outputs Open, OE ₁ =OE ₂ =GND,	V _{IN} =V _{CC} or V _{IN} =GND	—	60	100	μA/MHz
I _C	Total Power Supply Current ^[10]	V _{CC} =Max., f ₁ =10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, OE ₁ =OE ₂ =GND	V _{IN} =V _{CC} or V _{IN} =GND	—	0.6	1.5	mA
			V _{IN} =3.4V or V _{IN} =GND	—	0.9	2.3	
		V _{CC} =Max., f ₁ =2.5 MHz, 50% Duty Cycle, Outputs Open, Twenty Bits Toggling, OE ₁ =OE ₂ =GND	V _{IN} =V _{CC} or V _{IN} =GND	—	3.0	5.5 ^[11]	
			V _{IN} =3.4V or V _{IN} =GND	—	8.0	20.5 ^[11]	

Notes:

8. Per TTL driven input ($V_{IN}=3.4V$); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
 I_{CC} = Quiescent Current with CMOS input levels
 ΔI_{CC} = Power Supply Current for a TTL HIGH input ($V_{IN}=3.4V$)
 D_H = Duty Cycle for TTL inputs HIGH
 N_T = Number of TTL inputs at D_H
 I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
 f_0 = Clock frequency for registered devices, otherwise zero
 f_1 = Input signal frequency
 N_1 = Number of inputs changing at f_1
 All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are specified but not tested.

Switching Characteristics Over the Operating Range^[12]

Parameter	Description	Condition ^[13]	CY74FCT16827AT CY74FCT162827AT		CY74FCT162827BT		Unit	Fig. No. ^[13]
			Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay A to Y	C _L =50 pF R _L =500Ω	1.5	8.0	1.5	5.0	ns	1, 3
		C _L =300 pF R _L =500Ω	1.5	15.0	1.5	13.0		
t _{PZH} t _{PZL}	Output Enable Time OE to Y	C _L =50 pF R _L =500Ω	1.5	12.0	1.5	8.0	ns	1, 7, 8
		C _L =300 pF R _L =500Ω	1.5	23.0	1.5	15.0		
t _{PHZ} t _{PLZ}	Output Disable Time OE to Y	C _L =5 pF R _L =500Ω	1.5	9.0	1.5	6.0	ns	1, 7, 8
		C _L =50 pF R _L =500Ω	1.5	10.0	1.5	7.0		
t _{SK(O)}	Output Skew ^[14]		—	0.5	—	0.5	ns	—

Parameter	Description	Condition ^[12]	CY74FCT16827CT CY74FCT162827CT		Unit	Fig. No. ^[13]
			Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay A to Y	C _L =50 pF R _L =500Ω	1.5	4.2	ns	1, 3
		C _L =300 pF R _L =500Ω	1.5	10.0		
t _{PZH} t _{PZL}	Output Enable Time OE to Y	C _L =50 pF R _L =500Ω	1.5	5.6	ns	1, 7, 8
		C _L =300 pF R _L =500Ω	1.5	14.0		
t _{PHZ} t _{PLZ}	Output Disable Time OE to Y	C _L =5 pF R _L =500Ω	1.5	5.7	ns	1, 7, 8
		C _L =50 pF R _L =500Ω	1.5	6.0		
t _{SK(O)}	Output Skew ^[14]		—	0.5	ns	—

Notes:

12. Minimum limits are specified but not tested on Propagation Delays.

13. See "Parameter Measurement Information" in the General Information section.

14. Skew between any two outputs of the same package switching in the same direction. This parameter is ensured by design.

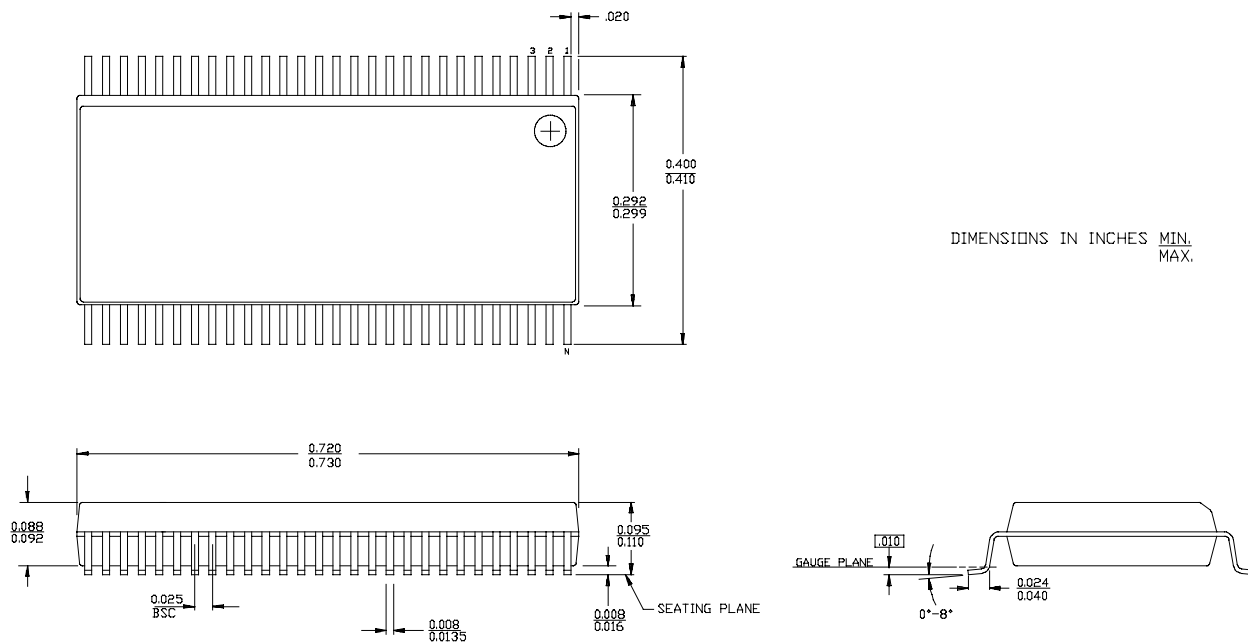
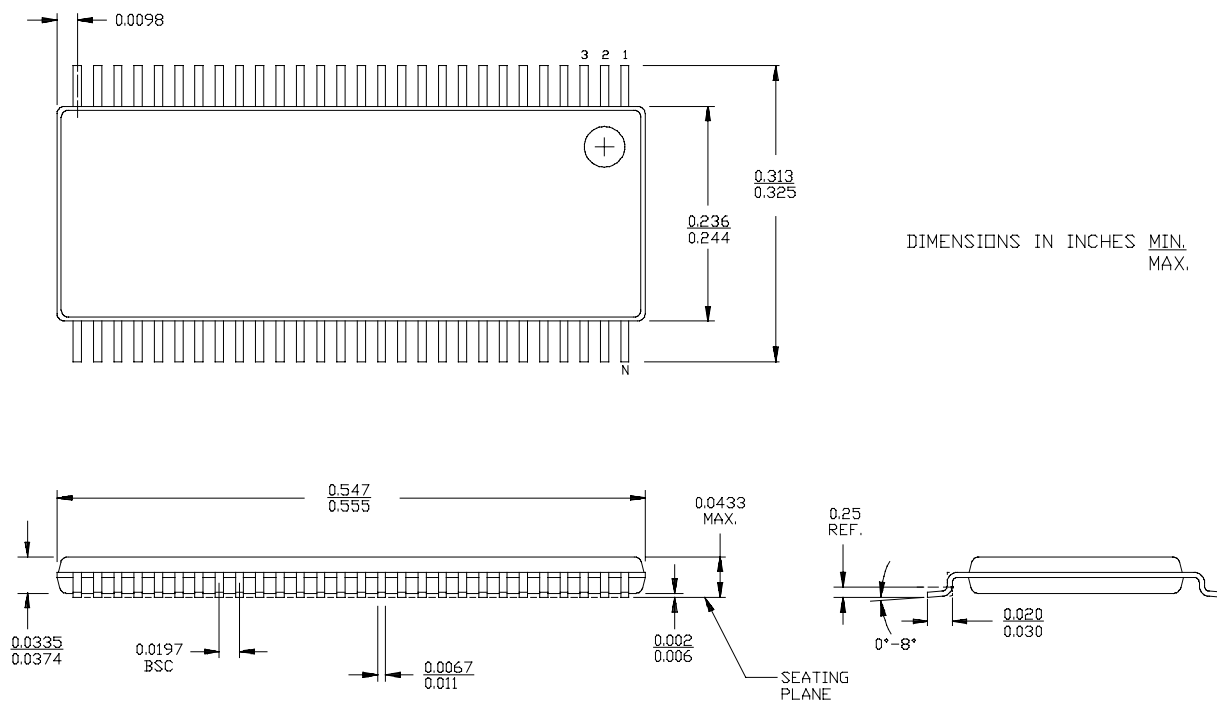
Ordering Information CY74FCT16827

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.2	CY74FCT16827CTPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT16827CTPVC/PVCT	O56	56-Lead (300-Mil) SSOP	
8.0	CY74FCT16827ATPVC/PVCT	Z56	56-Lead (240-Mil) SSOP	Industrial

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Ordering Information CY74FCT162827

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.2	74FCT162827CTPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162827CTPVC	Z56	56-Lead (240-Mil) SSOP	
	74FCT162827CTPVCT	Z56	56-Lead (240-Mil) SSOP	
5.0	CY74FCT162827BTPVC	O56	56-Lead (300-Mil) SSOP	Industrial
	74FCT162827BTPVCT	O56	56-Lead (300-Mil) SSOP	
8.0	CY74FCT162827ATPVC	O56	56-Lead (300-Mil) SSOP	Industrial
	74FCT162827ATPVCT	O56	56-Lead (300-Mil) SSOP	

Package Diagrams
56-Lead Shrunk Small Outline Package O56

56-Lead Thin Shrunk Small Outline Package Z56


PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74FCT162827ATPACT	Obsolete	Production	TSSOP (DGG) 56	-	-	Call TI	Call TI	-40 to 85	FCT162827A
CY74FCT16827ATPVC	Obsolete	Production	SSOP (DL) 56	-	-	Call TI	Call TI	-40 to 85	FCT16827A
CY74FCT16827CTPACT	Obsolete	Production	TSSOP (DGG) 56	-	-	Call TI	Call TI	-40 to 85	FCT16827C

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

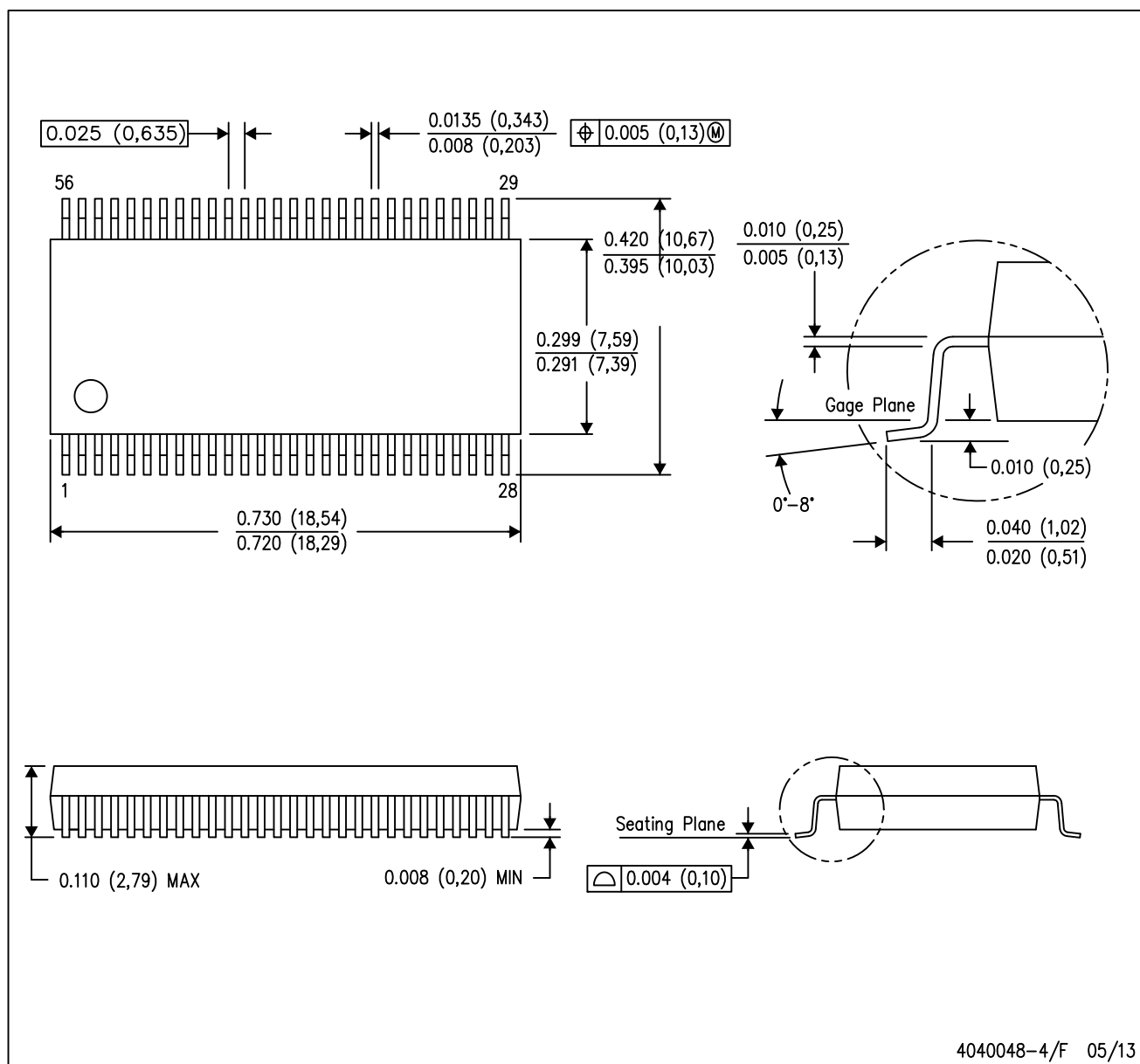
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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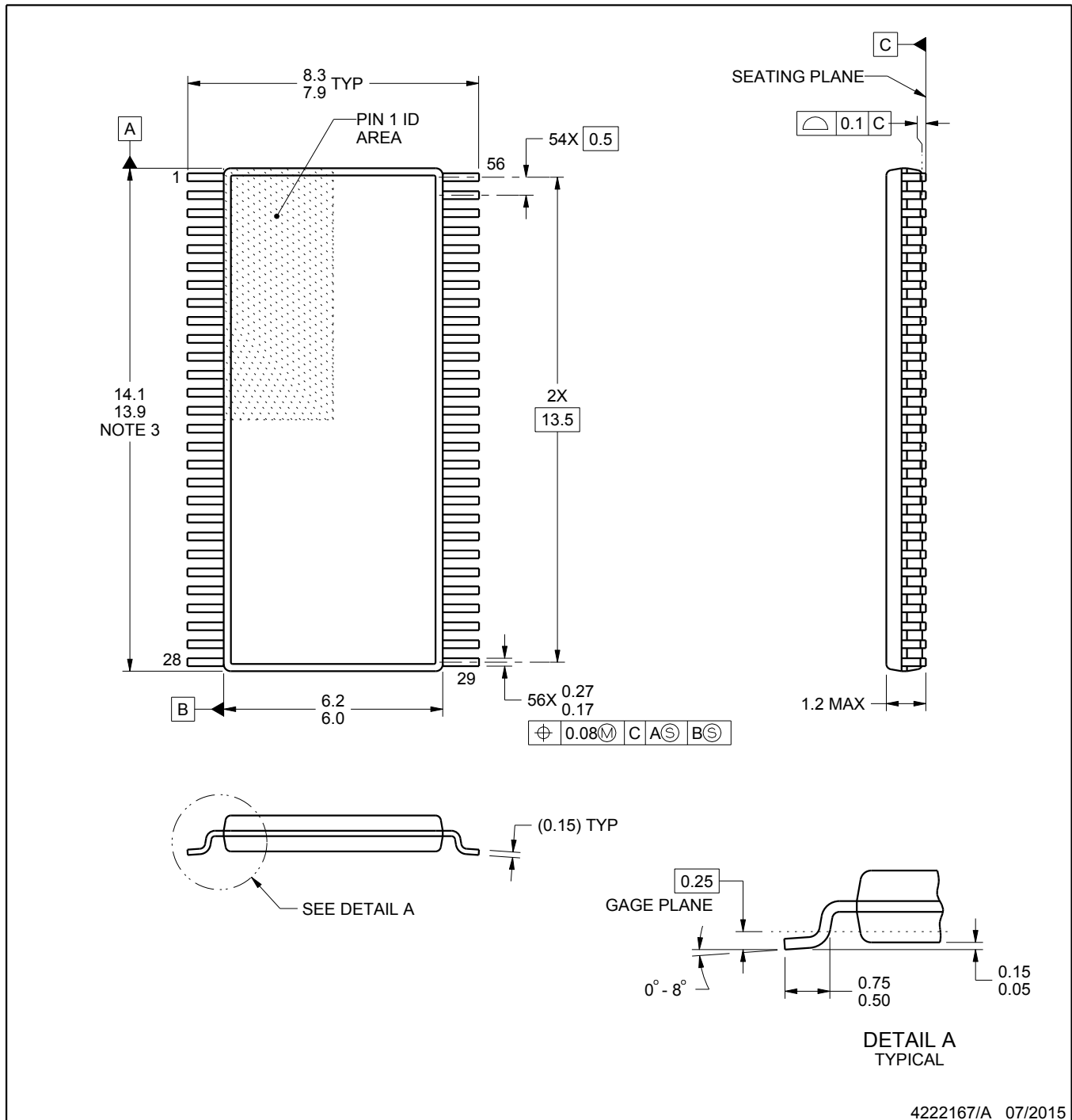
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DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MO-118



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NOTES:

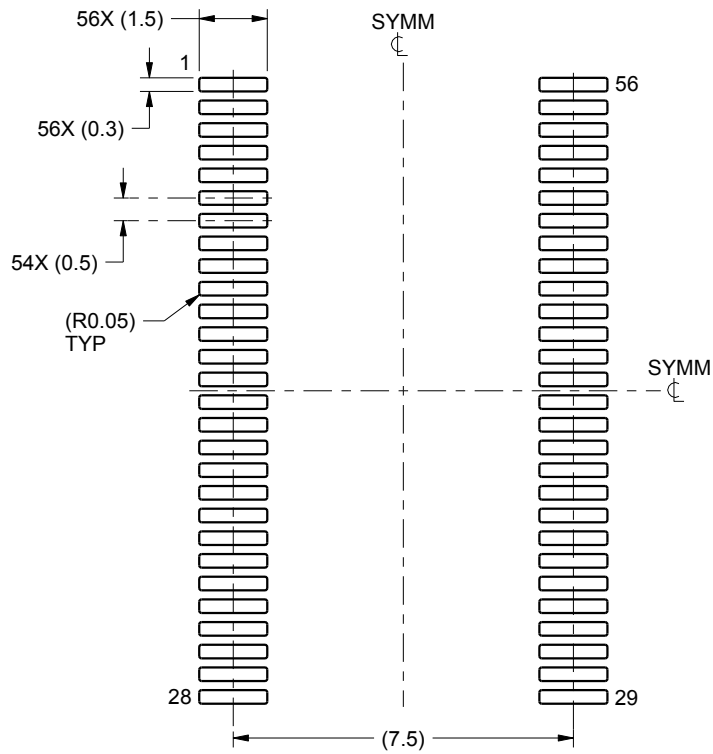
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

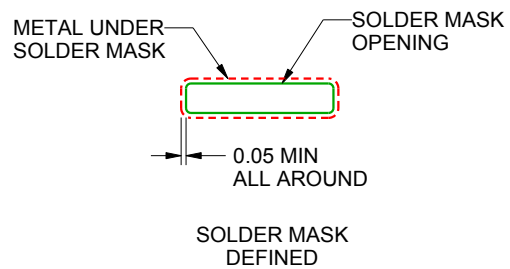
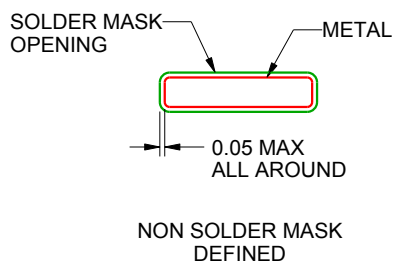
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

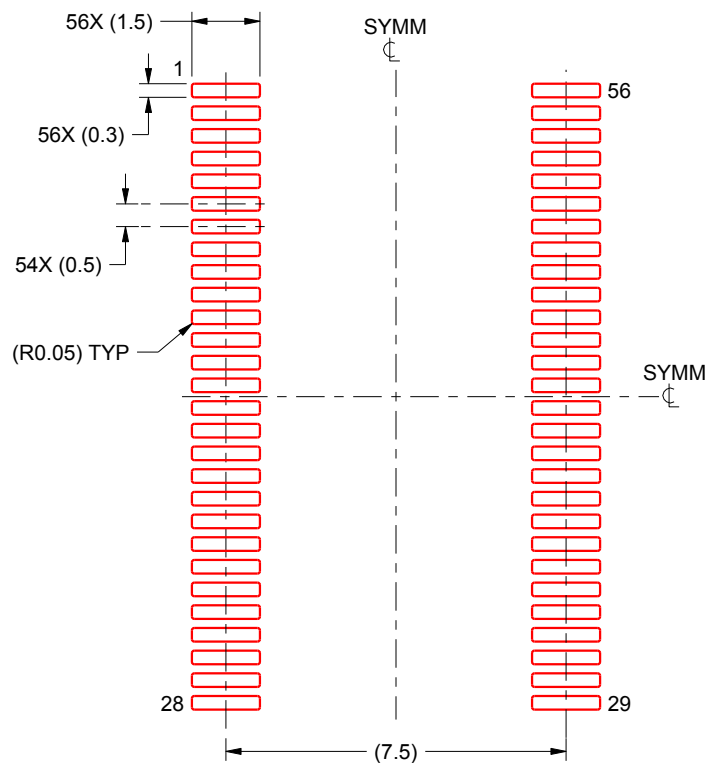
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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