# DUAL 12-BIT 200-MSPS DIGITAL-TO-ANALOG CONVERTER

## FEATURES

- **Controlled Baseline**
  - **One Assembly**
  - **One Test Site**
  - **One Fabrication Site**
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree** (1)
- **12-Bit Dual Transmit Digital-to-Analog Converter (DAC)**
- **200-MSPS Update Rate**
- **Single Supply: 3 V to 3.6 V**
- **High Spurious-Free Dynamic Range (SFDR): 85 dBc at 5 MHz**
- **High Third-Order Two-Tone Intermodulation (IMD3): 78 dBc at 15.1 and 16.1 MHz**
- **WCDMA Adjacent Channel Leakage Ratio (ACLR): 70 dB at 30.72 MHz**
- **Independent or Single Resistor Gain Control**
- **Dual or Interleaved Data**
- **On-Chip 1.2-V Reference**
- **Low Power: 330 mW**
- **Power-Down Mode: 15 mW**
- **Package: 48-Pin Thin Quad Flat Pack (TQFP)**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

## APPLICATIONS

- **Cellular Base Transceiver Station Transmit Channel**
  - **CDMA: W-CDMA, CDMA2000, IS-95**
  - **TDMA: GSM, IS-136, EDGE/UWC-136**
- **Medical/Test Instrumentation**
- **Arbitrary Waveform Generators (ARB)**
- **Direct Digital Synthesis (DDS)**
- **Cable Modem Termination System (CMTS)**

## DESCRIPTION

The DAC5662 is a monolithic, dual-channel 12-bit, high-speed digital-to-analog converter (DAC) with on-chip voltage reference.

Operating with update rates of up to 200 MSPS, the DAC5662 offers exceptional dynamic performance, tight gain, and offset matching characteristics that make it suitable in either I/Q baseband or direct IF communication applications.

Each DAC has a high-impedance differential-current output, suitable for single-ended or differential analog-output configurations. External resistors allow scaling the full-scale output current for each DAC separately or together, typically between 2 mA and 20 mA. An accurate on-chip voltage reference is temperature compensated and delivers a stable 1.2-V reference voltage. Optionally, an external reference may be used.

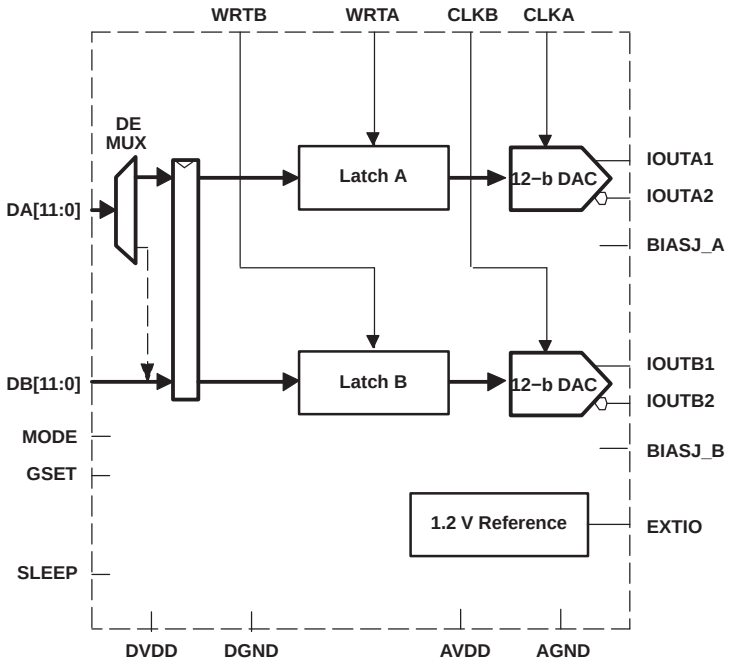
The DAC5662 has two 12-bit parallel input ports with separate clocks and data latches. For flexibility, the DAC5662 also supports multiplexed data for each DAC on one port when operating in the interleaved mode.

The DAC5662 has been specifically designed for a differential transformer coupled output with a 50-Ω doubly terminated load. For a 20-mA full-scale output current a 4:1 impedance ratio (resulting in an output power of 4 dBm) and 1:1 impedance ratio transformer (–2-dBm output power) are supported.

## DESCRIPTION (CONTINUED)

The DAC5662 is available in a 48-pin thin quad flat pack (TQFP). Pin compatibility between family members provides 12-bit (DAC5662) and 14-bit (DAC5672) resolution. Furthermore, the DAC5662 is pin compatible to the DAC2902 and AD9765 dual DACs. The device is characterized for operation over the military temperature range of –55°C to 125°C.

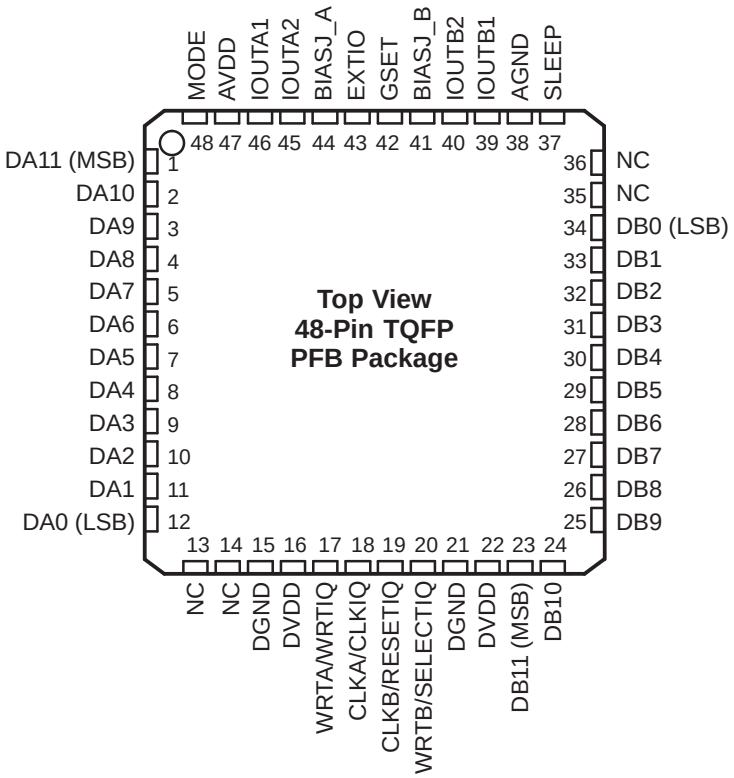
### FUNCTIONAL BLOCK DIAGRAM




### AVAILABLE OPTIONS

| $T_A$ | PACKAGED DEVICES 48-PIN TQFP |
|---|---|
| –55°C to 125°C | DAC5662MPFBREP |
| | DAC5662MPFBEP |

## DEVICE INFORMATION



## DEVICE INFORMATION (continued)

### TERMINAL FUNCTIONS

| TERMINAL | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| AGND | 38 | I | Analog ground |
| AVDD | 47 | I | Analog supply voltage |
| BIASJ_A | 44 | O | Full-scale output current bias for DACA |
| BIASJ_B | 41 | O | Full-scale output current bias for DACB |
| CLKA/CLKIQ | 18 | I | Clock input for DACA, CLKIQ in interleaved mode |
| CLKB/RESETIQ | 19 | I | Clock input for DACB, RESETIQ in interleaved mode |
| DA[11:0] | 1–12 | I | Data port A. DA11 is MSB and DA0 is LSB. |
| DB[11:0] | 23–34 | I | Data port B. DB11 is MSB and DB0 is LSB. |
| DGND | 15, 21 | I | Digital ground |
| DVDD | 16, 22 | I | Digital supply voltage |
| EXTIO | 43 | I/O | Internal reference output (bypass with 0.1 μF to AGND) or external reference input |
| GSET | 42 | I | Gain-setting mode: H = 1 resistor, L = 2 resistors. Internal pullup |
| IOUTA1 | 46 | O | DACA current output. Full scale with all bits of DA high. |
| IOUTA2 | 45 | O | DACA complementary current output. Full scale with all bits of DA low. |
| IOUTB1 | 39 | O | DACB current output. Full scale with all bits of DB high. |
| IOUTB2 | 40 | O | DACB complementary current output. Full scale with all bits of DB low. |
| MODE | 48 | I | Mode select: H = dual bus, L = interleaved. Internal pullup. |
| NC | 13, 14, 35, 36 | – | No connection |
| SLEEP | 37 | I | Sleep function control input: H = DAC in power-down mode, L = DAC in operating mode. Internal pulldown. |
| WRTA/WRTIQ | 17 | I | Input write signal for PORT A (WRTIQ in interleaving mode) |
| WRTB/SELECTIQ | 20 | I | Input write signal for PORT B (SELECTIQ in interleaving mode) |

## PFB PACKAGE THERMAL CHARACTERISTICS

| PARAMETER | POWERPAD CONNECTED TO PCB THERMAL PLANE |
|---|---|
| Thermal resistance, junction to ambient | 63.7°C/W |
| Thermal resistance, junction to case | 19.6°C/W |

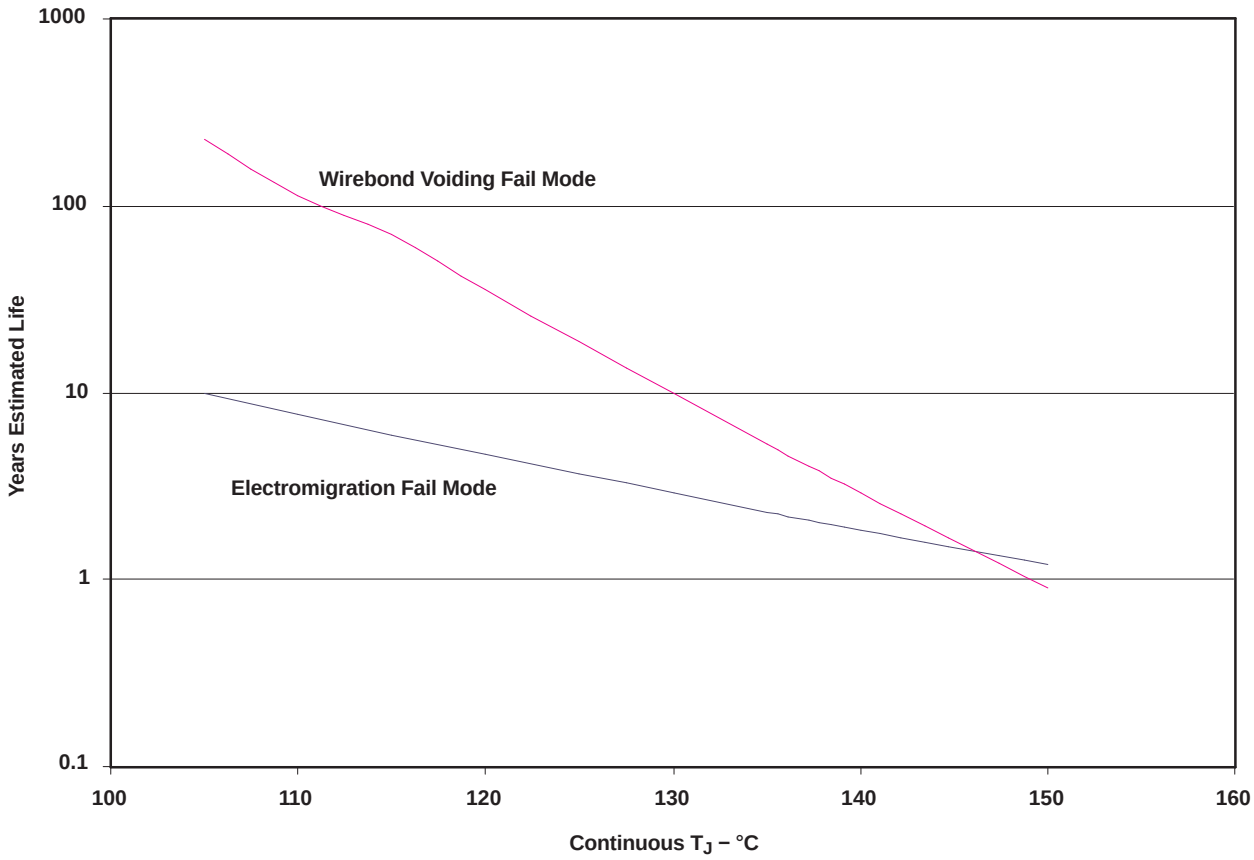



**Figure 1. DAC5662MPFB Operating Life Derating Chart**

## ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

| | | UNIT |
|---|---|---|
| Supply voltage range | AVDD(2) | –0.5 V to 4 V |
| | DVDD(3) | –0.5 V to 4 V |
| Voltage between AGND and DGND | | –0.5 V to 0.5 V |
| Voltage between AVDD and DVDD | | –0.5 V to 0.5 V |
| Supply voltage range | DA[11:0] and DB[11:0](3) | –0.5 V to DVDD + 0.5 V |
| | MODE, CLKA, CLKB, WRTA, WRTB(3) | –0.5 V to DVDD + 0.5 V |
| | IOUTA1, IOUTA2, IOUTB1, IOUTB2(2) | –1 V to AVDD + 0.5 V |
| | EXTIO, BIASJ_A, BIASJ_B, SLEEP(2) | –0.5 V to AVDD + 0.5 V |
| Peak input current (any input) | | 20 mA |
| Peak total input current (all inputs) | | –30 mA |
| Operating free-air temperature range | | –55°C to 125°C |
| Storage temperature range | | –65°C to 150°C |
| Lead temperature | 1,6 mm (1/16 in) from the case for 10 s | 260°C |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Measured with respect to AGND
(3) Measured with respect to DGND

## ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, AVDD = DVDD = 3.3 V, $I_{OUTFS}$ = 20 mA, independent gain set mode (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DC Specifications** | | | | | | |
| | Resolution | | 12 | | | Bits |
| **DC Accuracy**(1) | | | | | | |
| INL | Integral nonlinearity | 1 LSB = $IOUT_{FS}/2^{12}$, $T_A$ = 25°C | –2 | 0.3 | 2 | LSB |
| DNL | Differential nonlinearity | 1 LSB = $IOUT_{FS}/2^{12}$, $T_A$ = 25°C | –2 | 0.2 | 2 | LSB |
| **Analog Output** | | | | | | |
| | Offset error | | | 0.03 | | %FSR |
| | Gain error | With external reference | | 0.25 | | %FSR |
| | | With internal reference | | 0.5 | | %FSR |
| | Minimum full-scale output current(2) | | | 2 | | mA |
| | Maximum full-scale output current(2) | | | 20 | | mA |
| | Gain mismatch | With internal reference | –2 | 0.07 | 2 | %FSR |
| | Output voltage compliance range(3) | | –0.8 | | 1.25 | V |
| $R_O$ | Output resistance | | | 300 | | kΩ |
| $C_O$ | Output capacitance | | | 5 | | pF |
| **Reference Output** | | | | | | |
| | Reference voltage | | 1.14 | 1.2 | 1.26 | V |
| | Reference output current(4) | | | 100 | | nA |
| **Reference Input** | | | | | | |
| $V_{EXTIO}$ | Input voltage | | 0.1 | | 1.25 | V |
| $R_I$ | Input resistance | | | 1 | | MΩ |
| | Small signal bandwidth | | | 300 | | kHz |
| $C_I$ | Input capacitance | | | 100 | | pF |
| **Temperature Coefficients** | | | | | | |
| | Offset drift | | | 0 | | ppm of FSR/°C |
| | Gain drift | With external reference | | ±50 | | ppm of FSR/°C |
| | | With internal reference | | ±50 | | |
| | Reference voltage drift | | | ±20 | | ppm/°C |

(1) Measured differentially through 50 Ω to AGND.
(2) Nominal full-scale current, $I_{OUTFS}$, equals 32× the IBIAS current.
(3) The lower limit of the output compliance is determined by the CMOS process. Exceeding this limit may result in transistor breakdown, resulting in reduced reliability of the DAC5662 device. The upper limit of the output compliance is determined by the load resistors and full-scale output current. Exceeding the upper limit adversely affects distortion performance and intergral nonlinearity.
(4) Use an external buffer amplifier with high impedance input to drive any external load.

## ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, AVDD = DVDD = 3.3 V, $I_{OUTFS}$ = 20 mA, $f_{DATA}$ = 200 MSPS, $f_{OUT}$ = 1 MHz, independent gain set mode (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | |
| AVDD | Analog supply voltage | | 3 | 3.3 | 3.6 | V |
| DVDD | Digital supply voltage | | 3 | 3.3 | 3.6 | V |
| $I_{AVDD}$ | Supply current, analog | Including output current through load resistor | | 75 | 90 | mA |
| | | Sleep mode with clock | | 2.5 | 6 | |
| | | Sleep mode without clock | | 2.5 | | |
| $I_{DVDD}$ | Supply current, digital | | | 25 | 38 | mA |
| | | Sleep mode with clock | | 12.5 | 18 | |
| | | Sleep mode without clock | | <10 | | |
| | Power dissipation | | | 330 | 390 | mW |
| | | Sleep mode without clock | | 15 | | |
| | | $f_{DATA}$ = 200 MSPS, $f_{OUT}$ = 20 MHz | | 350 | | |
| APSSR | Analog power-supply rejection ratio | | –0.2 | | 0.2 | %FSR/V |
| DPSRR | Digital power-supply rejection ratio | | –0.2 | | 0.2 | %FSR/V |
| $T_A$ | Operating free-air temperature | | –55 | | 125 | °C |

## ELECTRICAL CHARACTERISTICS

AC specifications over operating free-air temperature range, AVDD = DVDD = 3.3 V, $I_{OUTFS}$ = 20 mA, independent gain set mode, differential 1:1 impedance ratio transformer coupled output, 50-Ω doubly terminated load (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Analog Output** | | | | | | |
| $f_{clk}$ | Maximum output update rate | | 200 | 275(1) | | MSPS |
| $t_s$ | Output settling time to 0.1% (DAC) | Mid-scale transition | | 20 | | ns |
| $t_r$ | Output rise time 10% to 90% (OUT) | | | 1.4 | | ns |
| $t_f$ | Output fall time 90% to 10% (OUT) | | | 1.5 | | ns |
| | Output noise | $I_{OUTFS}$ = 20 mA | | 55 | | pA/√Hz |
| | | $I_{OUTFS}$ = 2 mA | | 30 | | |
| **AC Linearity** | | | | | | |
| SFDR | Spurious-free dynamic range | 1st Nyquist zone, $T_A$ = 25°C, $f_{DATA}$ = 50 MSPS, $f_{OUT}$ = 1 MHz, $I_{OUTFS}$ = 0 dB | | 81 | | dBc |
| | | 1st Nyquist zone, $T_A$ = 25 C, $f_{DATA}$ = 50 MSPS, $f_{OUT}$ = 1 MHz, $I_{OUTFS}$ = –6 dB | | 83 | | |
| | | 1st Nyquist zone, $T_A$ = 25°C, $f_{DATA}$ = 50 MSPS, $f_{OUT}$ = 1 MHz, $I_{OUTFS}$ = –12 dB | | 81 | | |
| | | 1st Nyquist zone, $T_A$ = 25°C, $f_{DATA}$ = 100 MSPS, $f_{OUT}$ = 5 MHz | | 85 | | |
| | | 1st Nyquist zone, $T_A$ = 25°C, $f_{DATA}$ = 100 MSPS, $f_{OUT}$ = 20 MHz | | 78 | | |
| | | 1st Nyquist zone, $T_A$ = 25°C, $f_{DATA}$ = 200 MSPS, $f_{OUT}$ = 20 MHz | 66 | 71 | | |
| | | 1st Nyquist zone, $T_{min}$ = –55°C to 125°C, $f_{DATA}$ = 200 MSPS, $f_{OUT}$ = 20 MHz | 63 | 71 | | |
| | | 1st Nyquist zone, $T_A$ = 25°C, $f_{DATA}$ = 200 MSPS, $f_{OUT}$ = 41 MHz | | 68 | | |
| SNR | Signal-to-noise ratio | 1st Nyquist zone, $T_A$ = 25°C, $f_{DATA}$ = 100 MSPS, $f_{OUT}$ = 5 MHz | | 73 | | dB |
| | | 1st Nyquist zone, $T_A$ = 25°C, $f_{DATA}$ = 200 MSPS, $f_{OUT}$ = 20 MHz | | 67 | | |
| ACLR | Adjacent channel leakage ratio | W-CDMA signal with 3.84-MHz bandwidth, $f_{DATA}$ = 61.44 MSPS, IF = 15.36 MHz | | 70 | | dB |
| | | W-CDMA signal with 3.84-MHz bandwidth, $f_{DATA}$ = 122.88 MSPS, IF = 30.72 MHz | | 70 | | |
| IMD3 | Third-order two-tone intermodulation | Each tone at –6 dBFS, $T_A$ = 25°C, $f_{DATA}$ = 200 MSPS, $f_{OUT}$ = 45.4 MHz and 46.4 MHz | | 62 | | dBc |
| | | Each tone at –6 dBFS, $T_A$ = 25°C, $f_{DATA}$ = 100 MSPS, $f_{OUT}$ = 15.1 MHz and 16.1 MHz | | 78 | | |
| IMD | Four-tone intermodulation | Each tone at –12 dBFS, $T_A$ = 25°C, $f_{DATA}$ = 100 MSPS, $f_{OUT}$ = 15.6, 15.8, 16.2, and 16.4 MHz | | 77 | | dBc |
| | | Each tone at –12 dBFS, $T_A$ = 25°C, $f_{DATA}$ = 165 MSPS, $f_{OUT}$ = 68.8, 69.6, 71.2, and 72 MHz | | 56 | | |
| | | Each tone at –12 dBFS, $T_A$ = 25°C, $f_{DATA}$ = 165 MSPS, $f_{OUT}$ = 19.0, 19.1, 19.3, and 19.4 MHz | | 74 | | |
| | Channel isolation | $T_A$ = 25°C, $f_{DATA}$ = 165 MSPS, $f_{OUT}$ (CH1) = 20 MHz, $f_{OUT}$ (CH2) = 21 MHz | | 97 | | dBc |

(1) Specified by design. Not production tested.

## ELECTRICAL CHARACTERISTICS

Digital specifications over operating free-air temperature range, AVDD = DVDD = 3.3 V, $I_{OUTFS}$ = 20 mA (unless otherwise noted)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **Digital Input** | | | | | |
| $V_{IH}$ | High-level input voltage | 2 | | 3.3 | V |
| $V_{IL}$ | Low-level input voltage | 0 | | 0.8 | V |
| $I_{IH}$ | High-level input current | | 50 | | µA |
| $I_{IL}$ | Low-level input current | | 10 | | µA |
| $I_{IH(GSET)}$ | High-level input current, GSET pin | | 7 | | µA |
| $I_{IL(GSET)}$ | Low-level input current, GSET pin | | –30 | | µA |
| $I_{IH(MODE)}$ | High-level input current, MODE pin | | –30 | | µA |
| $I_{IL(MODE)}$ | Low-level input current, MODE pin | | –80 | | µA |
| $C_I$ | Input capacitance | | 5 | | pF |

## SWITCHING CHARACTERISTICS

Digital specifications over operating free-air temperature range, AVDD = DVDD = 3.3 V, $I_{OUTFS}$ = 20 mA (unless otherwise noted)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **Timing – Dual Bus Mode** | | | | | |
| $t_{su}$ | Input setup time | 1 | | | ns |
| $t_h$ | Input hold time | 1 | | | ns |
| $t_{LPH}$ | Input clock pulse high time | | 2 | | ns |
| $t_{LAT}$ | Clock latency (WRTA/B to outputs)(1) | 4 | | 4 | clk |
| $t_{PD}$ | Propagation delay time | | 1.5 | | ns |
| **Timing – Single Bus Interleaved Mode** | | | | | |
| $t_{su}$ | Input setup time | | 0.5 | | ns |
| $t_h$ | Input hold time | | 0.5 | | ns |
| $t_{LAT}$ | Clock latency (WRTA/B to outputs)(1) | 4 | | 4 | clk |
| $t_{PD}$ | Propagation delay time | | 1.5 | | ns |

(1) Specified by design

## TYPICAL CHARACTERISTICS

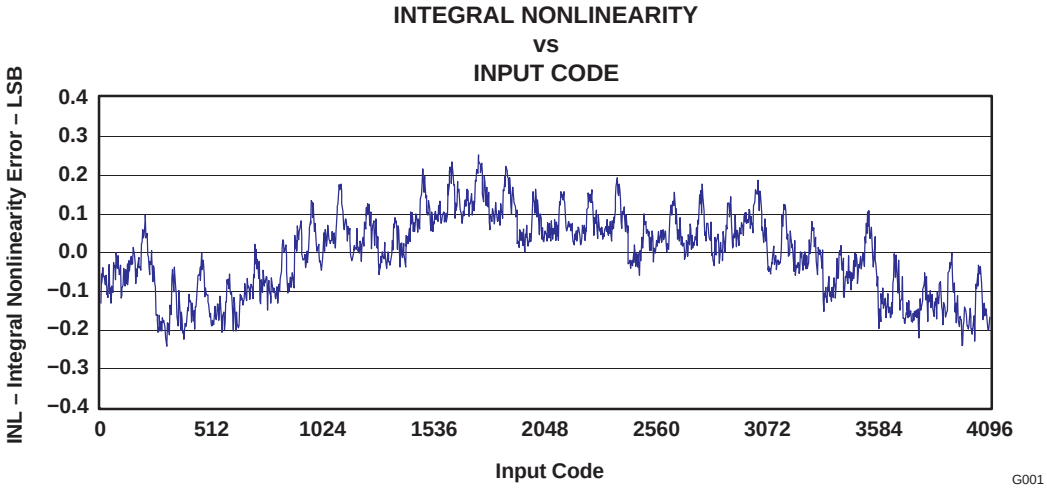



**Figure 2.**

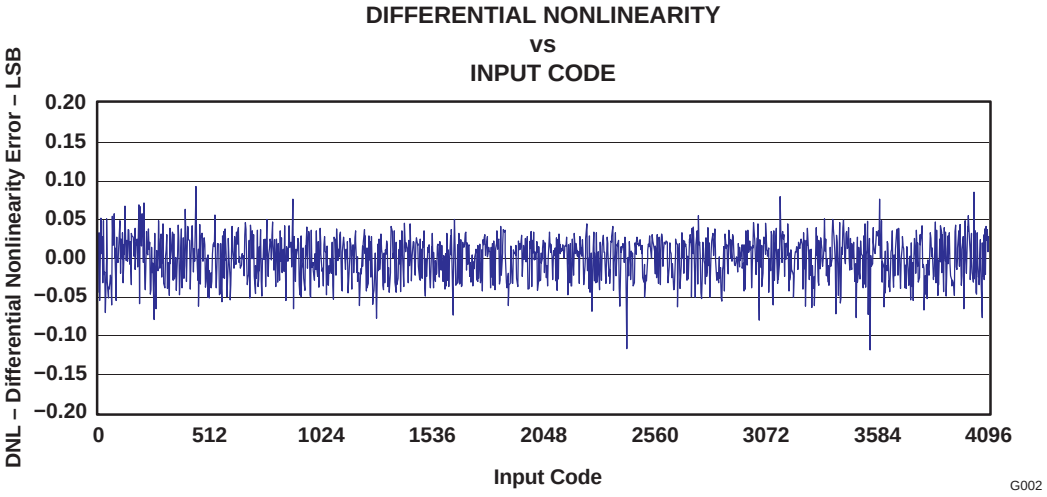



**Figure 3.**

## TYPICAL CHARACTERISTICS (continued)

SPURIOUS-FREE DYNAMIC RANGE
vs
OUTPUT FREQUENCY

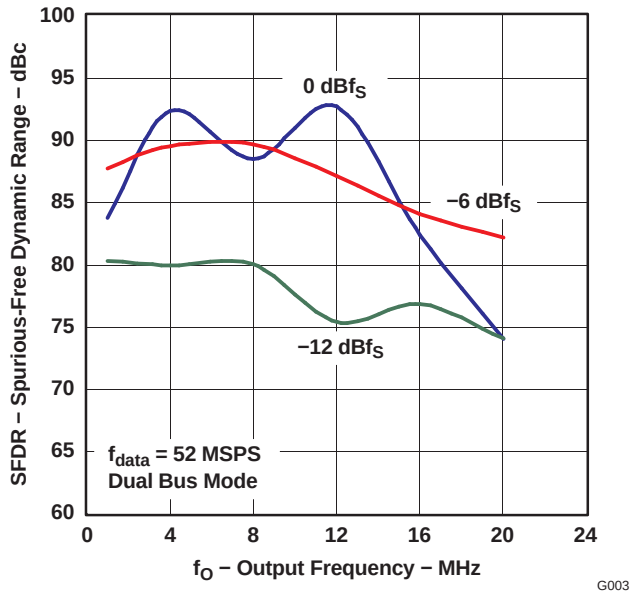



Figure 4.

SPURIOUS-FREE DYNAMIC RANGE
vs
OUTPUT FREQUENCY

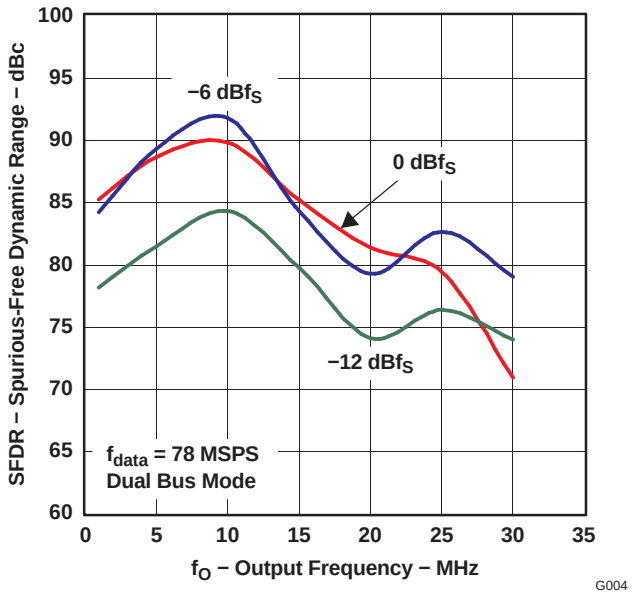



Figure 5.

SPURIOUS-FREE DYNAMIC RANGE
vs
OUTPUT FREQUENCY

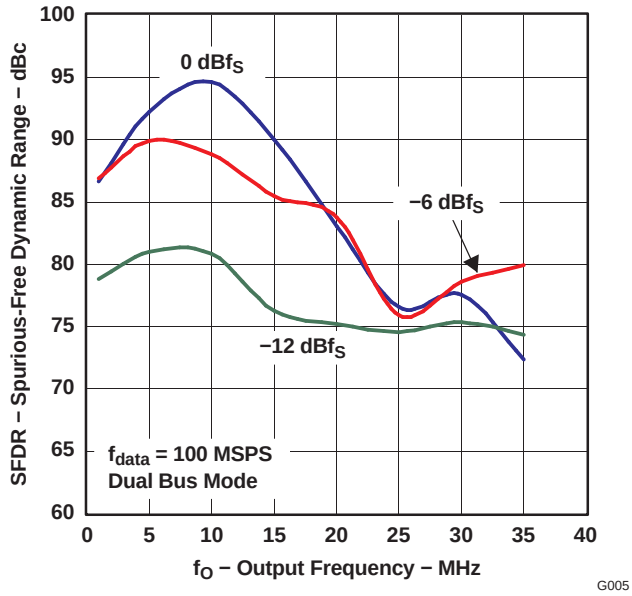



Figure 6.

SPURIOUS-FREE DYNAMIC RANGE
vs
OUTPUT FREQUENCY

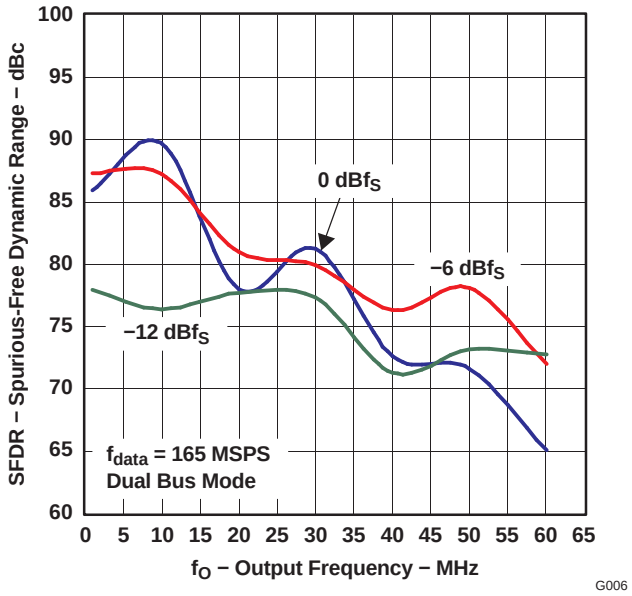



Figure 7.

## TYPICAL CHARACTERISTICS (continued)

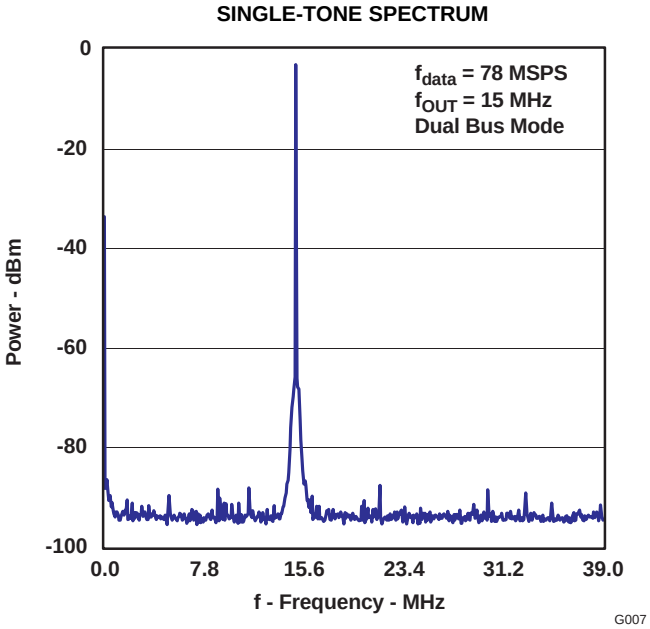



Figure 8.

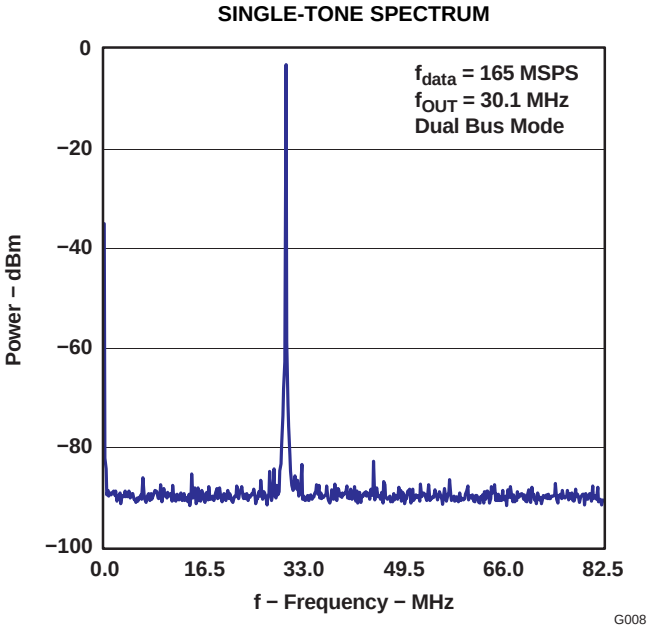



Figure 9.

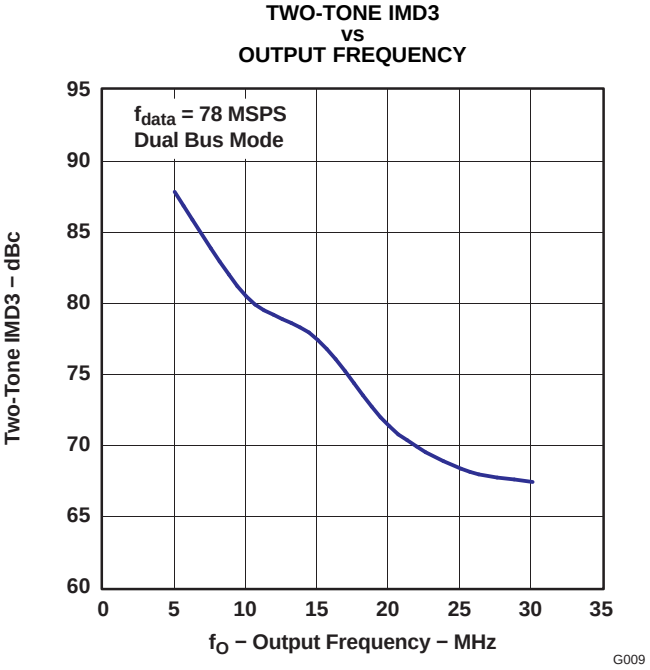



Figure 10.

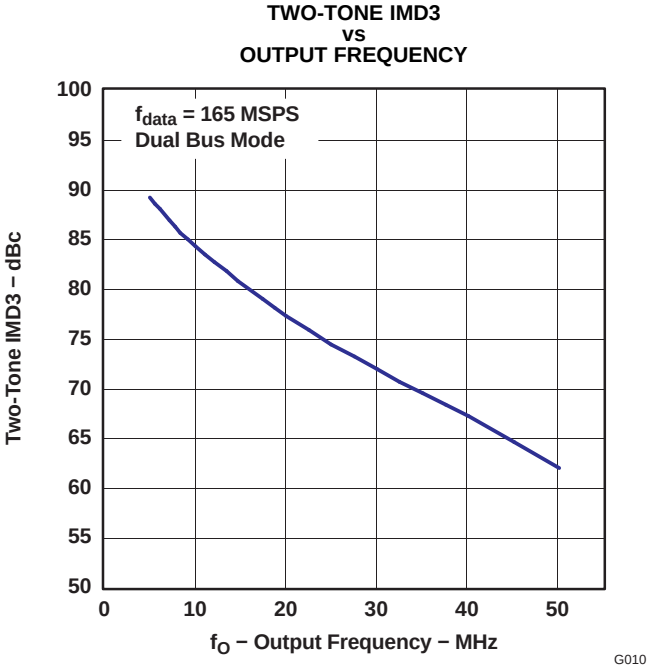



Figure 11.

## TYPICAL CHARACTERISTICS (continued)

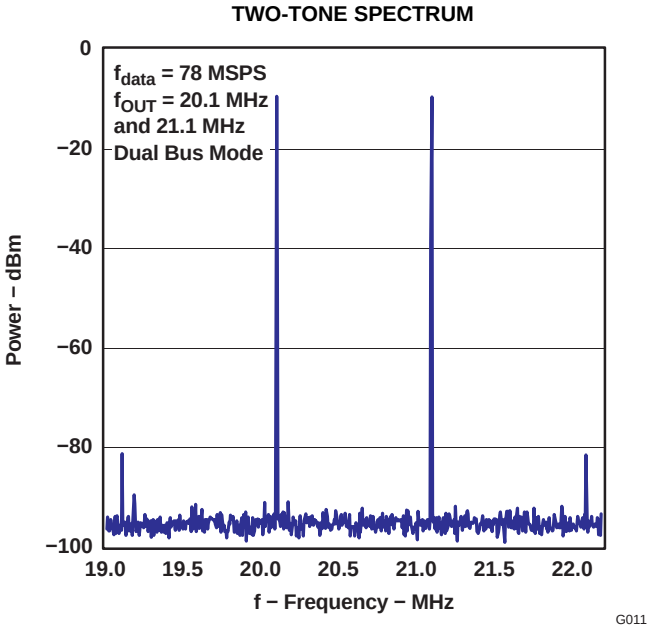



Figure 12.

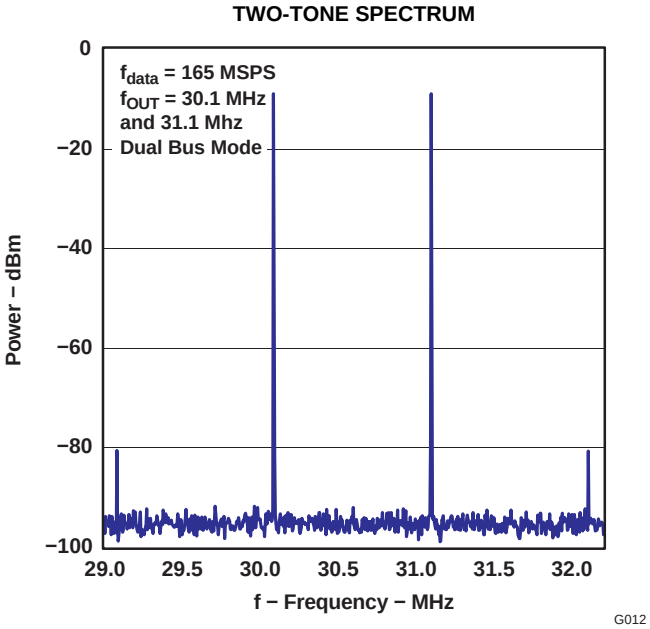



Figure 13.

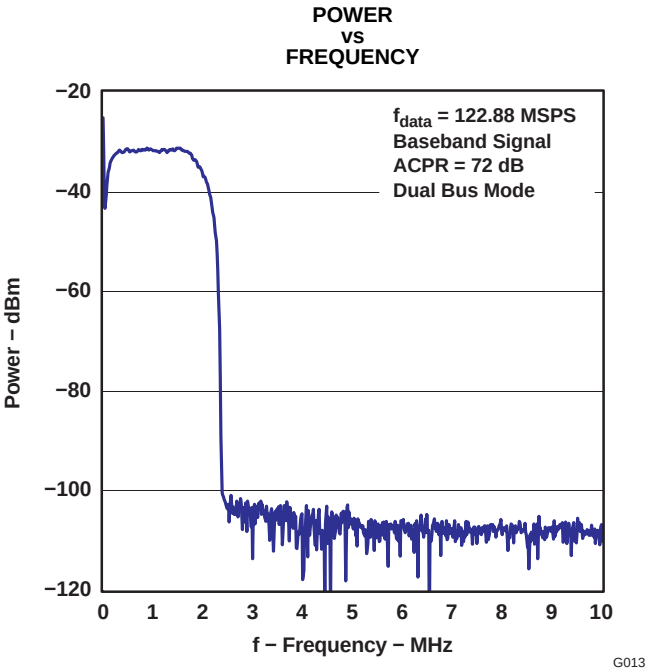



Figure 14.

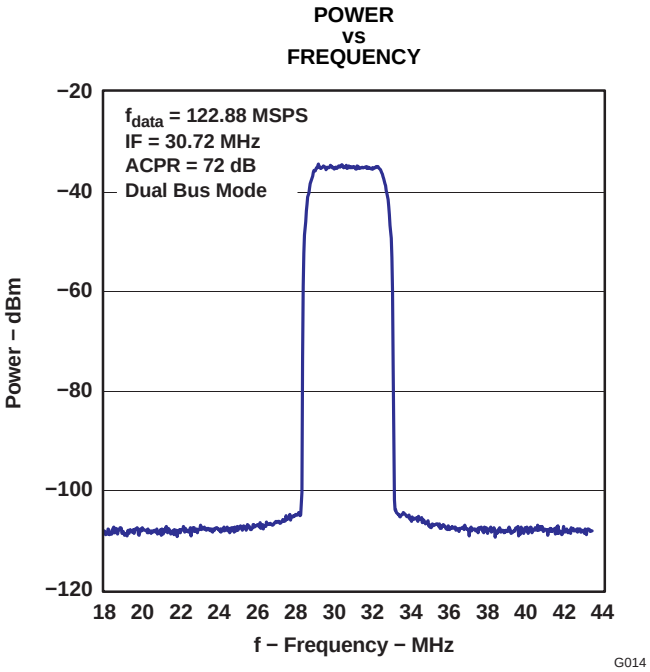



Figure 15.

## DIGITAL INPUTS AND TIMING

### Digital Inputs

The data input ports of the DAC5662 accept a standard positive coding with data bit D11 being the most significant bit (MSB). The converter outputs are specified to support a clock rate up to 200 MSPS. The best performance is typically be achieved with a symmetric duty cycle for write and clock; however, the duty cycle may vary as long as the timing specifications are met. Similarly, the setup and hold times may be chosen within their specified limits.

All digital inputs of the DAC5662 are CMOS compatible. Figure 16 and Figure 17 show schematics of the equivalent CMOS digital inputs of the DAC5662. The 12-bit digital data input follows the offset positive binary coding scheme. The DAC5662 is designed to operate with a digital supply (DVDD) of 3 V to 3.6 V.

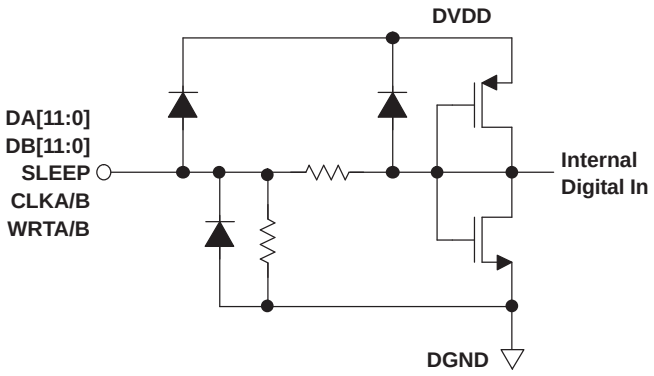



**Figure 16. CMOS/TTL Digital Equivalent Input With Internal Pulldown Resistor**

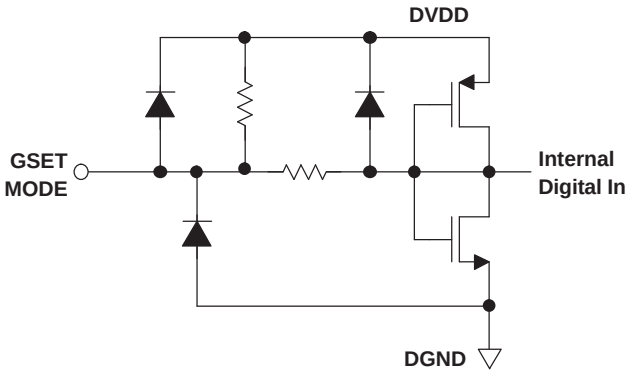



**Figure 17. CMOS/TTL Digital Equivalent Input With Internal Pullup Resistor**

### Input Interfaces

The DAC5662 features two operating modes selected by the MODE pin (see Table 1).

- For dual-bus input mode, the device essentially consists of two separate DACs. Each DAC has its own separate data input bus, clock input, and data write signal (data latch-in).
- In single-bus interleaved mode, the data should be presented interleaved at the I-channel input bus. The Q-channel input bus is not used in this mode. The clock and write input are now shared by both DACs.

**Table 1. Operating Modes**

| | | |
|---|---|---|
| **MODE PIN** | Mode pin connected to DGND | Mode pin connected to DVDD |
| **BUS INPUT** | Single-bus interleaved mode, clock and write input equal for both DACs | Dual-bus mode, DACs operate independently |

## DIGITAL INPUTS AND TIMING (continued)

### Dual-Bus Data Interface and Timing

In dual-bus mode, the MODE pin is connected to DVDD. The two converter channels within the DAC5662 consist of two independent, 12-bit, parallel data ports. Each DAC channel is controlled by its own set of write (WRTA, WRTB) and clock (CLKA, CLKB) lines. The WRT lines control the channel input latches and the CLK lines control the DAC latches. The data is first loaded into the input latch by a rising edge of the WRT line

The internal data transfer requires a correct sequence of write and clock inputs, since essentially two clock domains having equal periods (but possibly different phases) are input to the DAC5662. This is defined by a minimum requirement of the time between the rising edge of the clock and the rising edge of the write inputs. This essentially implies that the rising edge of CLK must occur at the same time or before the rising edge of the WRT signal. A minimum delay of 2 ns should be maintained if the rising edge of the clock occurs after the rising edge of the write. Note that these conditions are satisfied when the clock and write inputs are connected externally. Note that all specifications were measured with the WRT and CLK lines connected together.

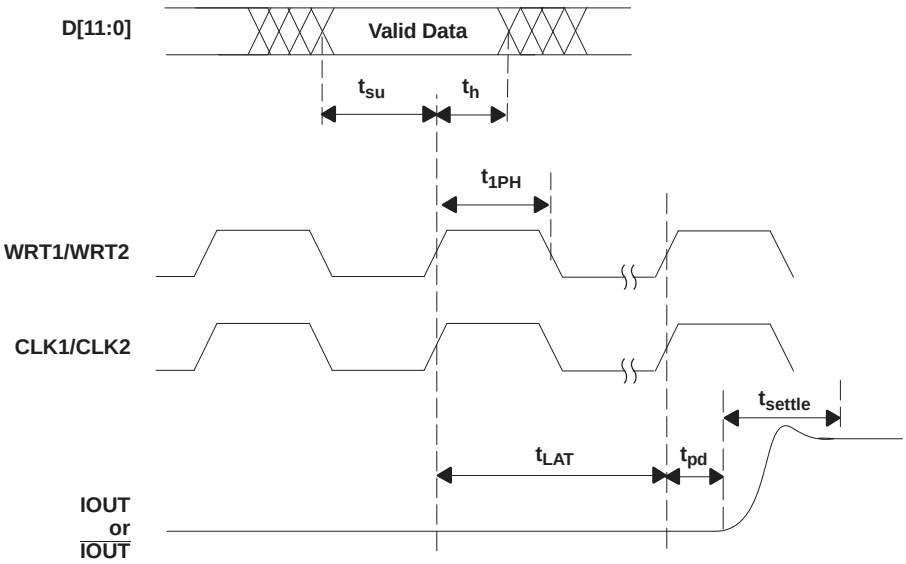



**Figure 18. Dual-Bus-Mode Operation**

### Single-Bus Interleaved Data Interface and Timing

In single-bus interleaved mode, the MODE pin is connected to DGND. Figure 19 shows the timing diagram. In interleaved mode, the I and Q channels share the write input (WRTIQ) and update clock (CLKIQ and internal CLKDACIQ). Multiplexing logic directs the input word at the I-channel input bus to either the I-channel input latch (SELECTIQ is high) or to the Q-channel input latch (SELECTIQ is low). When SELECTIQ is high, the data value in the Q-channel latch is retained by presenting the latch output data to its input again. When SELECTIQ is low, the data value in the I-channel latch is retained by presenting the latch output data to its input.

In interleaved mode, the I-channel input data rate is twice the update rate of the DAC core. As in dual-bus mode, it is important to maintain a correct sequence of write and clock inputs. The edge-triggered flip-flops latch the I- and Q-channel input words on the rising edge of the write input (WRTIQ). This data is presented to the I- and Q-DAC latches on the following falling edge of the write inputs. The DAC5662 clock input is divided by a factor of two before it is presented to the DAC latches.

Correct pairing of the I- and Q-channel data is done by RESETIQ. In interleaved mode, the clock input CLKIQ is divided by two, which would translate to a nondeterministic relation between the rising edges of the CLKIQ and CLKDACIQ. RESETIQ ensures, however, that the correct position of the rising edge of CLKDACIQ, with respect to the data at the input of the DAC latch, is determined. CLKDACIQ is disabled (low) when RESETIQ is high.

## DIGITAL INPUTS AND TIMING (continued)

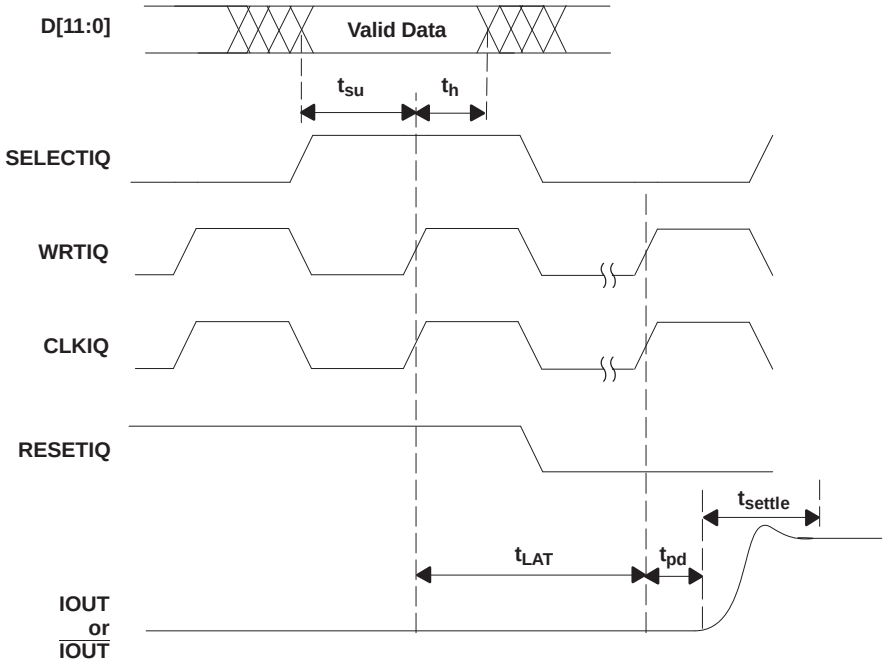



**Figure 19. Single-Bus Interleaved-Mode Operation**

# APPLICATION INFORMATION

## Theory of Operation

The architecture of the DAC5662 uses a current steering technique to enable fast switching and high update rate. The core element within the monolithic DAC is an array of segmented current sources that are designed to deliver a full-scale output current of up to 20 mA. An internal decoder addresses the differential current switches each time the DAC is updated and a corresponding output current is formed by steering all currents to either output summing node, $I_{OUT1}$ and $I_{OUT2}$. The complementary outputs deliver a differential output signal, which improves the dynamic performance through reduction of even-order harmonics, common-mode signals (noise), and double the peak-to-peak output signal swing by a factor of two, compared to single-ended operation.

The segmented architecture results in a significant reduction of the glitch energy and improves the dynamic performance (SFDR) and DNL. The current outputs maintain a high output impedance of greater than 300 kΩ.

When pin 42 (GSET) is high (one resistor mode), the full-scale output current for both DACs is determined by the ratio of the internal reference voltage (1.2 V) and an external resistor ($R_{SET}$) connected to BIASJ_A. When GSET is low (two resistor mode), the full-scale output current for each DACs is determined by the ratio of the internal reference voltage (1.2 V) and separate external resistors ($R_{SET}$) connected to BIASJ_A and BIASJ_B. The resulting $I_{REF}$ is internally multiplied by a factor of 32 to produce an effective DAC output current that can range from 2 mA to 20 mA, depending on the value of $R_{SET}$.

The DAC5662 is split into a digital and an analog portion, each of which is powered through its own supply pin. The digital section includes edge-triggered input latches and the decoder logic, while the analog section comprises the current source array with its associated switches, and the reference circuitry.

## DAC Transfer Function

Each of the DACs in the DAC5662 has a set of complementary current outputs, $I_{OUT1}$ and $I_{OUT2}$. The full-scale output current, $I_{OUTFS}$, is the summation of the two complementary output currents:

$$I_{OUTFS} = I_{OUT1} + I_{OUT2} \quad (1)$$

The individual output currents depend on the DAC code and can be expressed as:

$$I_{OUT1} = I_{OUTFS} \times \left(\frac{Code}{4096}\right) \quad (2)$$

$$I_{OUT2} = I_{OUTFS} \times \left(4095 - \frac{Code}{4096}\right) \quad (3)$$

where Code is the decimal representation of the DAC data input word. Additionally, $I_{OUTFS}$ is a function of the reference current $I_{REF}$, which is determined by the reference voltage and the external setting resistor ($R_{SET}$).

$$I_{OUTFS} = 32 \times I_{REF} = 32 \times \frac{V_{REF}}{R_{SET}} \quad (4)$$

In most cases, the complementary outputs drive resistive loads or a terminated transformer. A signal voltage develops at each output according to:

$$V_{OUT1} = I_{OUT1} \times R_{LOAD} \quad (5)$$

$$V_{OUT2} = I_{OUT2} \times R_{LOAD} \quad (6)$$

The value of the load resistance is limited by the output compliance specification of the DAC5662. To maintain specified linearity performance, the voltage for $I_{OUT1}$ and $I_{OUT2}$ should not exceed the maximum allowable compliance range.

## APPLICATION INFORMATION (continued)

The total differential output voltage is:

$$V_{OUTDIFF} = V_{OUT1} - V_{OUT2} \quad (7)$$

$$V_{OUTDIFF} = \frac{(2 \times Code - 4095)}{4096} \times I_{OUTFS} \times R_{LOAD} \quad (8)$$

### Analog Outputs

The DAC5662 provides two complementary current outputs, $I_{OUT1}$ and $I_{OUT2}$. The simplified circuit of the analog output stage representing the differential topology is shown in Figure 20. The output impedance of $I_{OUT1}$ and $I_{OUT2}$ results from the parallel combination of the differential switches, along with the current sources and associated parasitic capacitances.

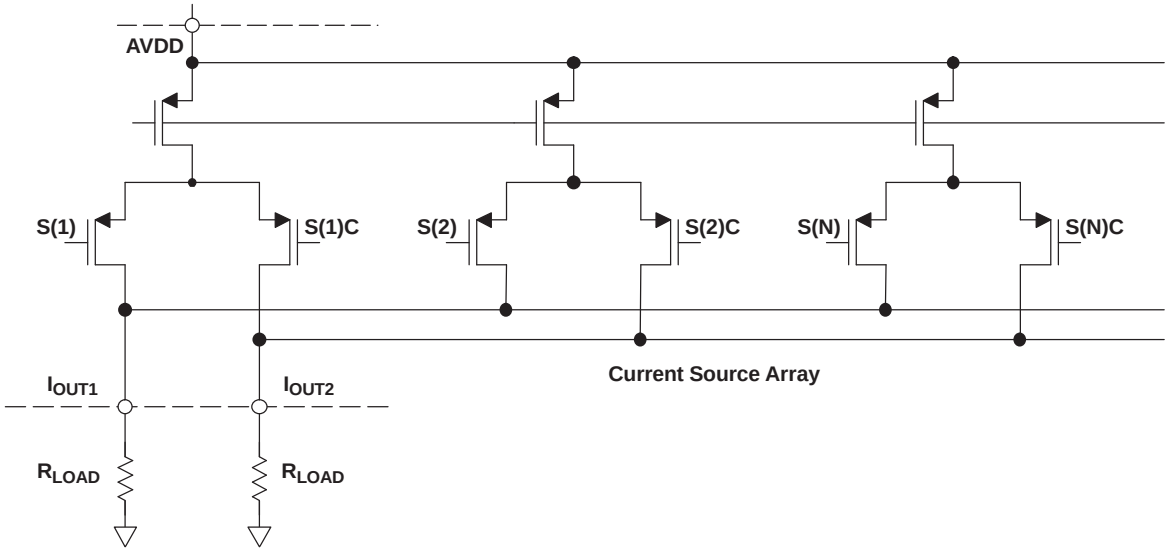



**Figure 20. Analog Outputs**

The signal voltage swing that may develop at the two outputs, $I_{OUT1}$ and $I_{OUT2}$, is limited by a negative and positive compliance. The negative limit of –1 V is given by the breakdown voltage of the CMOS process and exceeding it compromises the reliability of the DAC5662 or even causes permanent damage. With the full-scale output set to 20 mA, the positive compliance equals 1.2 V. Note that the compliance range decreases to about 1 V for a selected output current of $I_{OUTFS}$ = 2 mA. Care should be taken that the configuration of DAC5662 does not exceed the compliance range to avoid degradation of the distortion performance and integral linearity.

Best distortion performance is typically achieved with the maximum full-scale output signal limited to approximately 0.5 $V_{PP}$. This is the case for a 50-Ω doubly terminated load and a 20-mA full-scale output current. A variety of loads can be adapted to the output of the DAC5662 by selecting a suitable transformer while maintaining optimum voltage levels at $I_{OUT1}$ and $I_{OUT2}$. Furthermore, using the differential output configuration in combination with a transformer is instrumental for achieving excellent distortion performance. Common-mode errors, such as even-order harmonics or noise, can be substantially reduced. This is particularly the case with high output frequencies.

For those applications requiring the optimum distortion and noise performance, it is recommended to select a full-scale output of 20 mA. A lower full-scale range of 2 mA may be considered for applications that require low power consumption, but can tolerate a slight reduction in performance level.

## APPLICATION INFORMATION (continued)

### Output Configurations

The current outputs of the DAC5662 allow for a variety of configurations. As mentioned previously, utilizing the converter's differential outputs yield the best dynamic performance. Such a differential output circuit may consist of an RF transformer or a differential amplifier configuration. The transformer configuration is ideal for most applications with ac coupling, while operational amplifiers are suitable for a dc-coupled configuration.

The single-ended configuration may be considered for applications requiring a unipolar output voltage. Connecting a resistor from either one of the outputs to ground converts the output current into a ground-referenced voltage signal. To improve on the dc linearity by maintaining a virtual ground, an I-to-V or operational amplifier configuration may be considered.

### Differential With Transformer

Using an RF transformer provides a convenient way of converting the differential output signal into a single-ended signal while achieving excellent dynamic performance. The appropriate transformer should be carefully selected based on the output frequency spectrum and impedance requirements.

The differential transformer configuration has the benefit of significantly reducing common-mode signals, thus improving the dynamic performance over a wide range of frequencies. Furthermore, by selecting a suitable impedance ratio (winding ratio), the transformer can be used to provide optimum impedance matching while controlling the compliance voltage for the converter outputs.

Figure 21 and Figure 22 show 50-Ω doubly terminated transformer configurations with 1:1 and 4:1 impedance ratios, respectively. Note that the center tap of the primary input of the transformer has to be grounded to enable a dc-current flow. Applying a 20-mA full-scale output current leads to a 0.5-$V_{PP}$ output for a 1:1 transformer and a 1-$V_{PP}$ output for a 4:1 transformer. In general, the 1:1 transformer configuration has slightly better output distortion, but the 4:1 transformer has 6-dB higher output power.

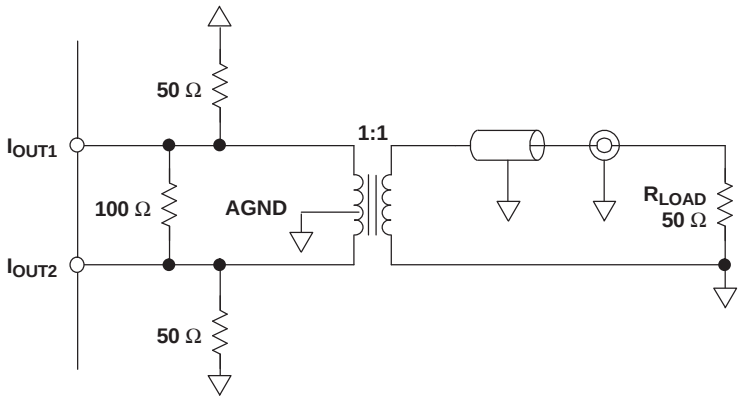



**Figure 21. Driving a Doubly-Terminated 50-Ω Cable Using a 1:1 Impedance Ratio Transformer**

## APPLICATION INFORMATION (continued)

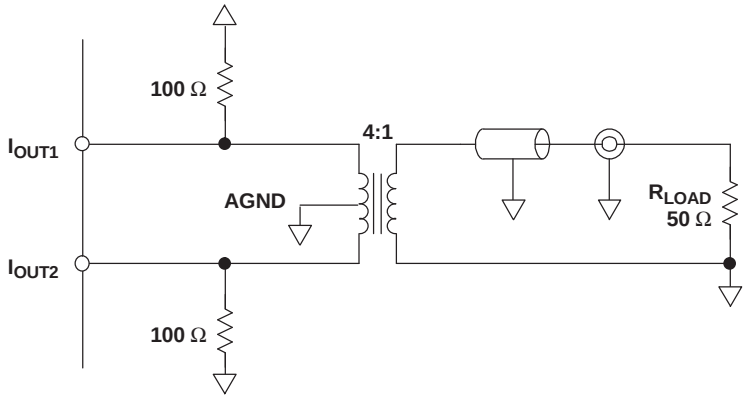



**Figure 22. Driving a Doubly-Terminated 50-Ω Cable Using a 4:1 Impedance Ratio Transformer**

### Single-Ended Configuration

Figure 23 shows the single-ended output configuration, where the output current $I_{OUT1}$ flows into an equivalent load resistance of 25 Ω. Node $I_{OUT2}$ should be connected to AGND or terminated with a resistor of 25 Ω to AGND. The nominal resistor load of 25 Ω gives a differential output swing of 1 $V_{PP}$ when applying a 20-mA full-scale output current.

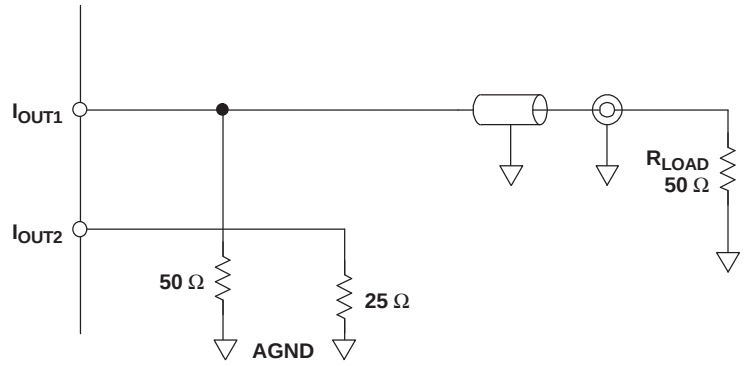



**Figure 23. Driving a Doubly-Terminated 50-Ω Cable Using a Single-Ended Output**

## APPLICATION INFORMATION (continued)

### Reference Operation

#### Internal Reference

The DAC5662 has an on-chip reference circuit which comprises a 1.2-V bandgap reference and two control amplifiers, one for each DAC. The full-scale output current, $I_{OUTFS}$, of the DAC5662 is determined by the reference voltage, $V_{REF}$, and the value of resistor $R_{SET}$. $I_{OUTFS}$ can be calculated by:

$$I_{OUTFS} = 32 \times I_{REF} = 32 \times \frac{V_{REF}}{R_{SET}} \quad (9)$$

The reference control amplifier operates as a V-to-I converter producing a reference current, $I_{REF}$, which is determined by the ratio of $V_{REF}$ and $R_{SET}$ (see Equation 9). The full-scale output current, $I_{OUTFS}$, results from multiplying $I_{REF}$ by a fixed factor of 32.

Using the internal reference, a 2-kΩ resistor value results in a full-scale output of approximately 20 mA. Resistors with a tolerance of 1% or better should be considered. Selecting higher values, the output current can be adjusted from 20 mA down to 2 mA. Operating the DAC5662 at lower than 20-mA output currents may be desirable for reasons of reducing the total power consumption, improving the distortion performance, or observing the output compliance voltage limitations for a given load condition.

It is recommended to bypass the EXTIO pin with a ceramic chip capacitor of 0.1 µF or more. The control amplifier is internally compensated and its small signal bandwidth is approximately 300 kHz.

#### External Reference

The internal reference can be disabled by simply applying an external reference voltage into the EXTIO pin that, in this case, functions as an input. The use of an external reference may be considered for applications that require higher accuracy and drift performance or to add the ability of dynamic gain control.

While a 0.1-µF capacitor is recommended to be used with the internal reference, it is optional for the external reference operation. The reference input, EXTIO, has a high input impedance (1 MΩ) and can easily be driven by various sources. Note that the voltage range of the external reference should stay within the compliance range of the reference input.

### Gain Setting Option

The full-scale output current on the DAC5662 can be set two ways — either for each of the two DAC channels independently or for both channels simultaneously. For the independent gain set mode, the GSET pin (pin 42) must be low (that is, connected to AGND). In this mode, two external resistors are required — one $R_{SET}$ connected to the BIASJ_A pin (pin 44) and the other to the BIASJ_B pin (pin 41). In this configuration, the user has the flexibility to set and adjust the full-scale output current for each DAC independently, allowing for the compensation of possible gain mismatches elsewhere within the transmit signal path.

Alternatively, bringing the GSET pin high (that is, connected to AVDD), the DAC5662 switches into the simultaneous gain set mode. Now the full-scale output current of both DAC channels is determined by only one external $R_{SET}$ resistor connected to the BIASJ_A pin. The resistor at the BIASJ_2 pin may be removed; however, this is not required since this pin is not functional in this mode and the resistor has no effect on the gain equation.

### Sleep Mode

The DAC5662 features a power-down function that can be used to reduce the total supply current to less than 3.5 mA over the specified supply range if no clock is present. Applying a logic high to the SLEEP pin initiates the power-down mode, while a logic low enables normal operation. When left unconnected, an internal active pulldown circuit enables the normal operation of the converter.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| DAC5662MPFBEP | Active | Production | TQFP (PFB) \| 48 | 250 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | DAC5662EP |
| DAC5662MPFBEP.A | Active | Production | TQFP (PFB) \| 48 | 250 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | DAC5662EP |
| DAC5662MPFBREP | Active | Production | TQFP (PFB) \| 48 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | DAC5662EP |
| DAC5662MPFBREP.A | Active | Production | TQFP (PFB) \| 48 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | DAC5662EP |
| V62/06651-01XE | Active | Production | TQFP (PFB) \| 48 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | DAC5662EP |
| V62/06651-02XE | Active | Production | TQFP (PFB) \| 48 | 250 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | DAC5662EP |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF DAC5662-EP :**

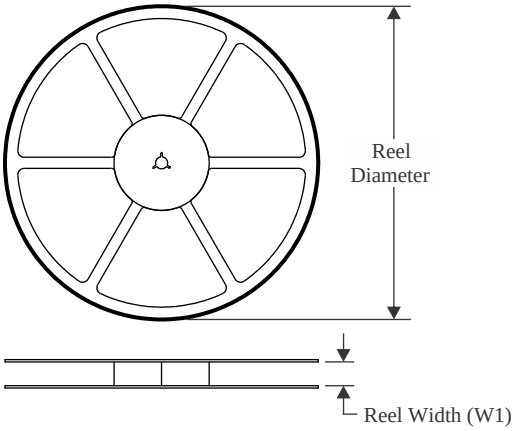
- Catalog : DAC5662

NOTE: Qualified Version Definitions:

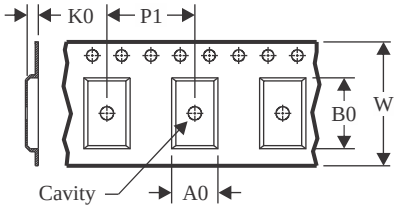
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

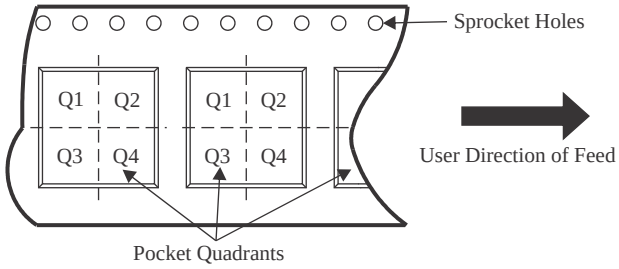



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

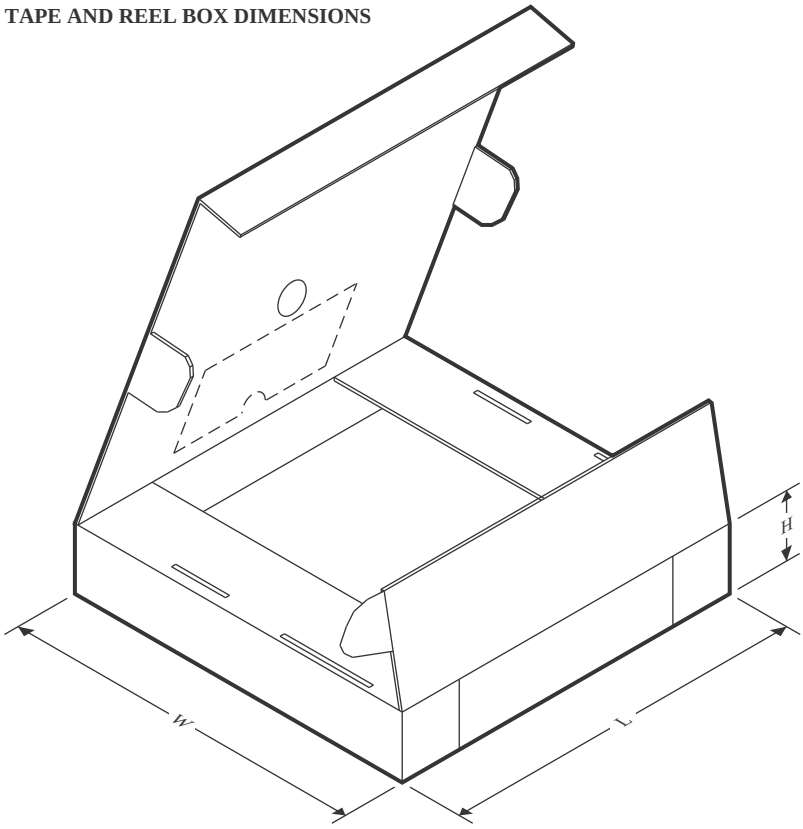
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DAC5662MPFBREP | TQFP | PFB | 48 | 1000 | 330.0 | 16.4 | 9.6 | 9.6 | 1.5 | 12.0 | 16.0 | Q2 |

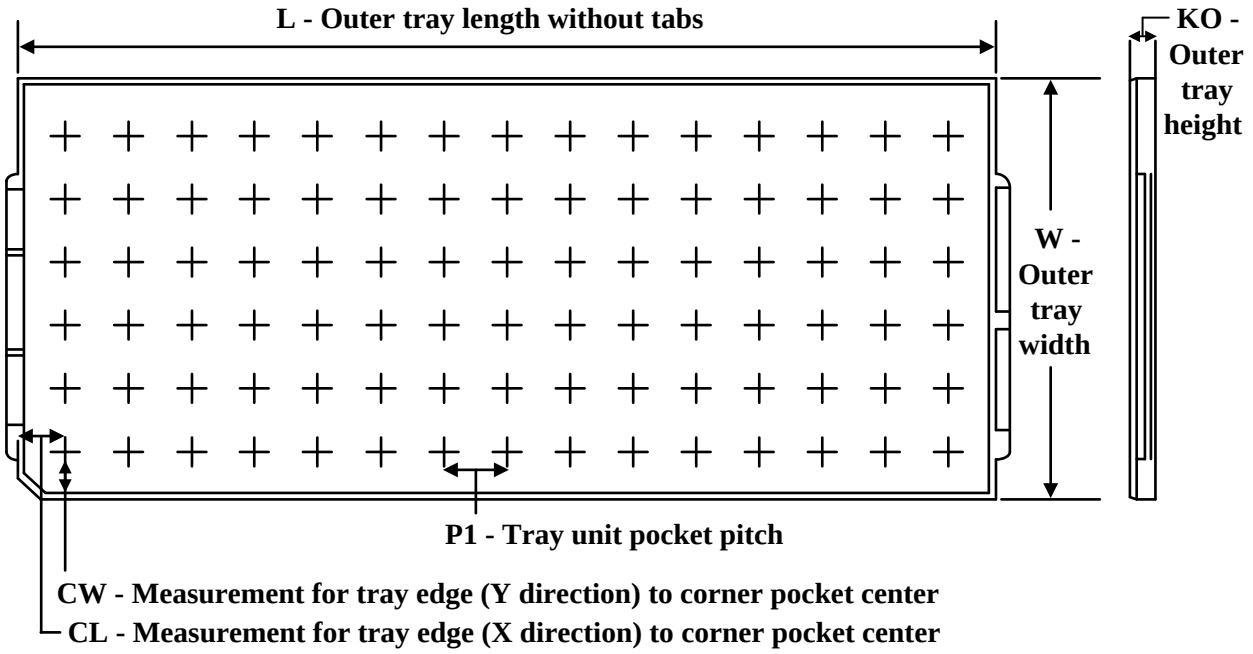
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| DAC5662MPFBREP | TQFP | PFB | 48 | 1000 | 350.0 | 350.0 | 43.0 |

## TRAY




Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

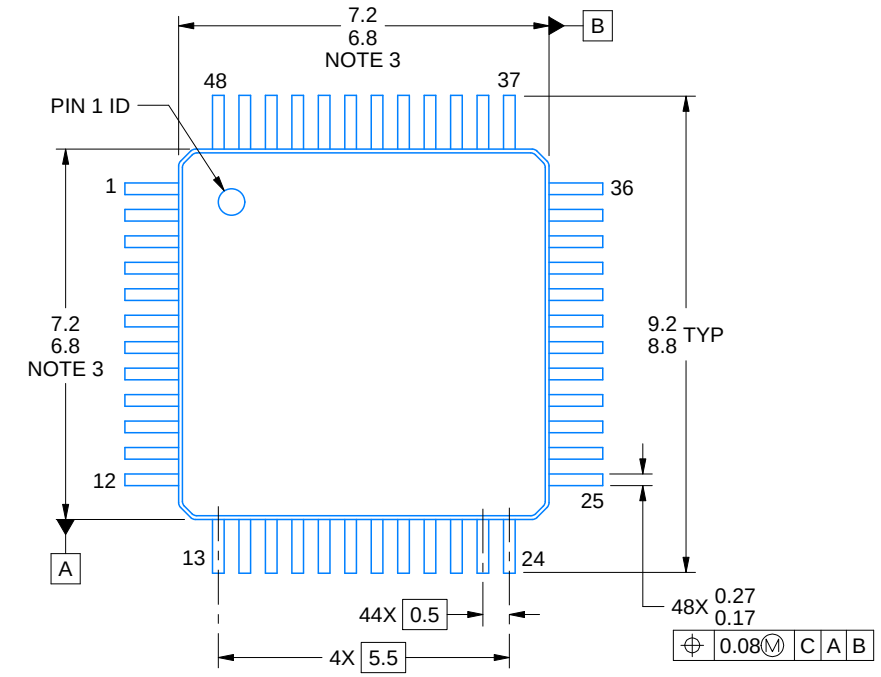
| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DAC5662MPFBEP | PFB | TQFP | 48 | 250 | 10 x 25 | 150 | 315 | 135.9 | 7620 | 12.2 | 11.1 | 11.25 |
| DAC5662MPFBEP.A | PFB | TQFP | 48 | 250 | 10 x 25 | 150 | 315 | 135.9 | 7620 | 12.2 | 11.1 | 11.25 |
| V62/06651-02XE | PFB | TQFP | 48 | 250 | 10 x 25 | 150 | 315 | 135.9 | 7620 | 12.2 | 11.1 | 11.25 |

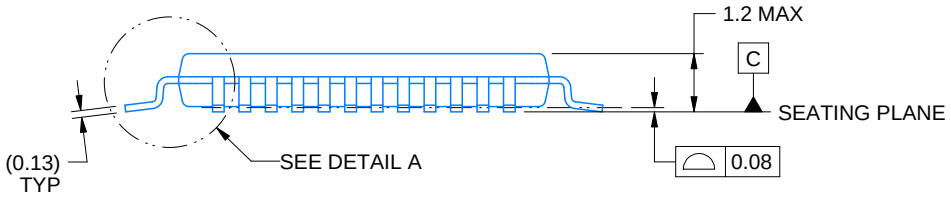
# PACKAGE OUTLINE

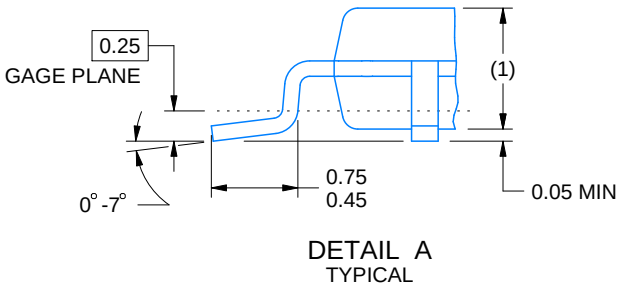
## PFB0048A

## TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK




DETAIL A
TYPICAL

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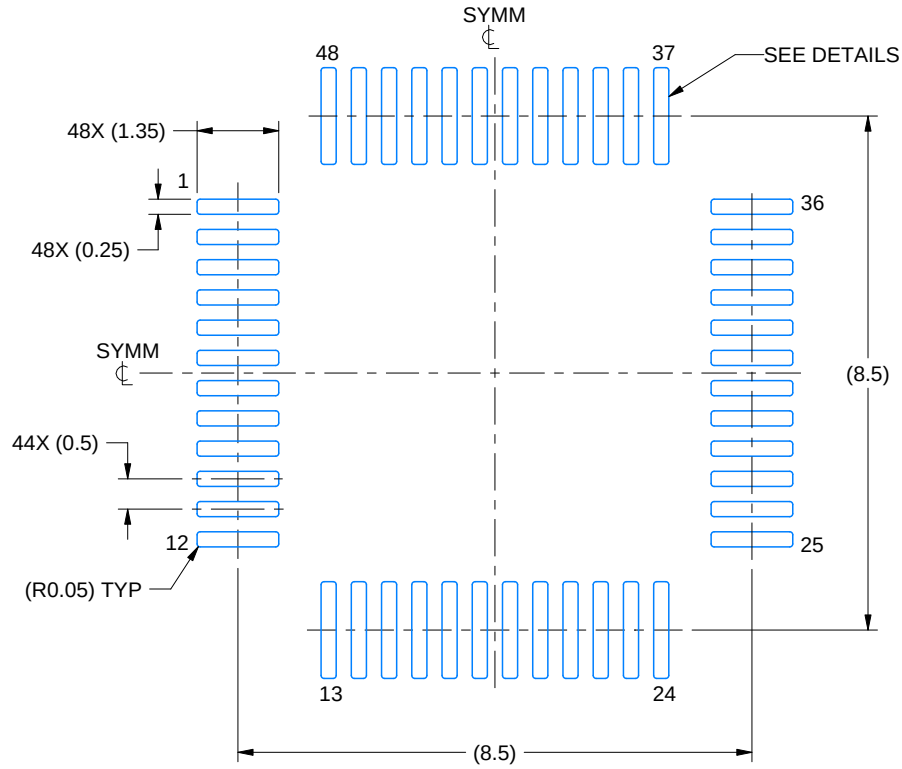
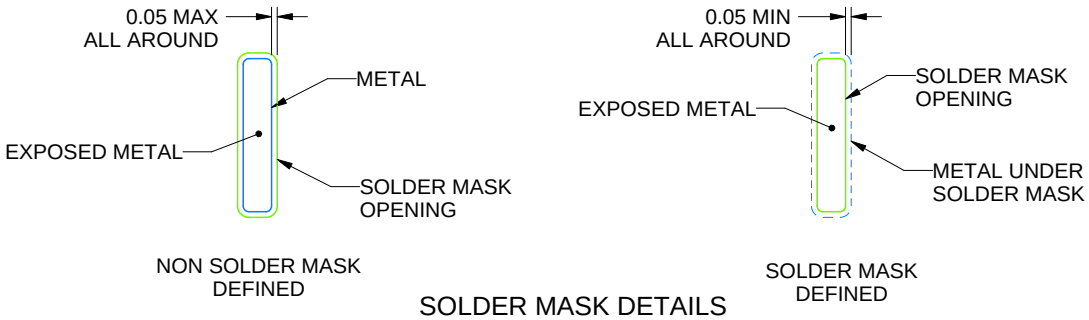
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

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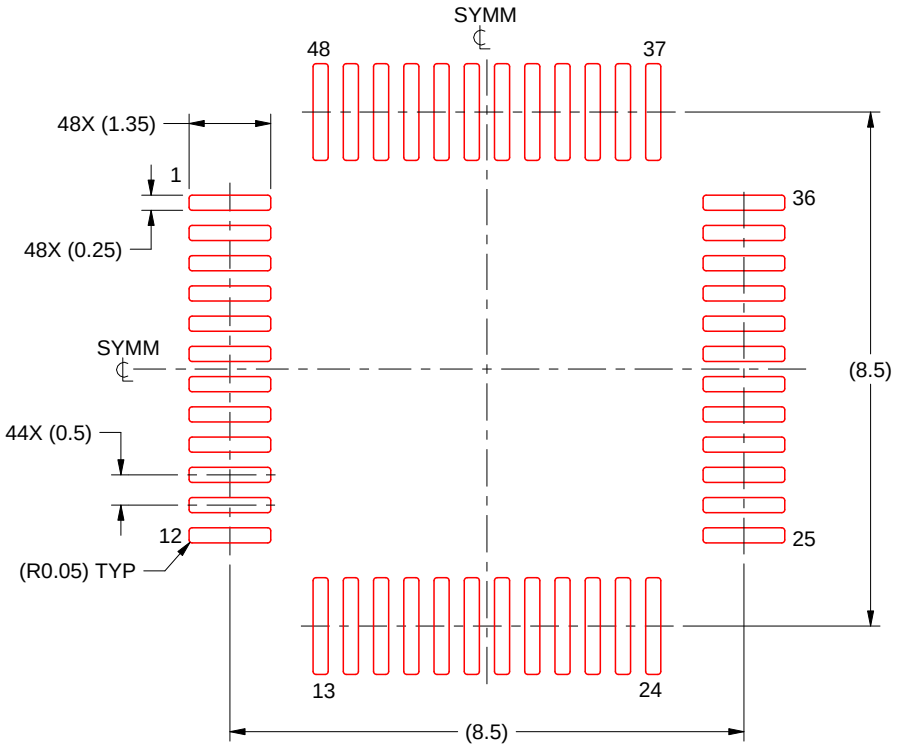
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
SCALE:8X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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