DACx1416 16-Channel, 12-Bit, 14-Bit, and 16-Bit High-Voltage Output DACs With Internal Reference

1 Features

- Performance
  - Specified monotonic at 16-bit resolution
  - INL: ±1 LSB maximum at 16-bit resolution
  - TUE: ±0.1% of FSR maximum
- Integrated 2.5V precision internal reference
  - Initial accuracy: ±2.5mV maximum
  - Low drift: 5ppm/°C typical
- Flexible output configuration
  - Output range: ±2.5V, ±5V, ±10V, ±20V
    0V to 5V, 0V to 10V, 0V to 20V or 0V to 40V
  - Differential output mode
- High drive capability: ±25mA with 1.5V from supply rails
- Three dedicated A-B toggle pins for dither signal generation
- Analog temperature output
  - Sensor gain of –4mV/°C
- 50MHz SPI-compatible serial interface
  - 4-wire mode, 1.7V to 5.5V operation
  - Daisy-chain operation
  - CRC error check
- Temperature range: –40°C to +125°C
- Small package
  - 6mm × 6mm, 40-pin VQFN

2 Applications

- Inter-DC interconnect (long-haul, submarine)
- Inter-DC interconnect (metro)
- Optical module
- Semiconductor test
- Lab and field instrumentation
- Data acquisition (DAQ)

3 Description

The 12-bit DAC61416, 14-bit DAC71416, and 16-bit DAC81416 (DACx1416) are a pin-compatible family of 16-channel, buffered, high-voltage output digital-to-analog converters (DACs). The DACx1416 include a low-drift, 2.5-V internal reference that eliminates the need for an external precision reference in most applications. These devices are specified monotonic and provide high linearity of ±1LSB INL.

A user-selectable output configuration enables full-scale bipolar output voltages of ±20V, ±10V, ±5V or ±2.5V, and full-scale unipolar output voltages of 40V, 20V, 10V or 5V. The full-scale output range for each DAC channel is independently programmable. The integrated DAC output buffers sink or source up to 25mA, and thus limit the need for additional operational amplifiers. Each pair of channels are configurable to provide a differential output with offset calibration. The three dedicated A-B toggle pins enable dither signal generation with up to three possible frequencies.

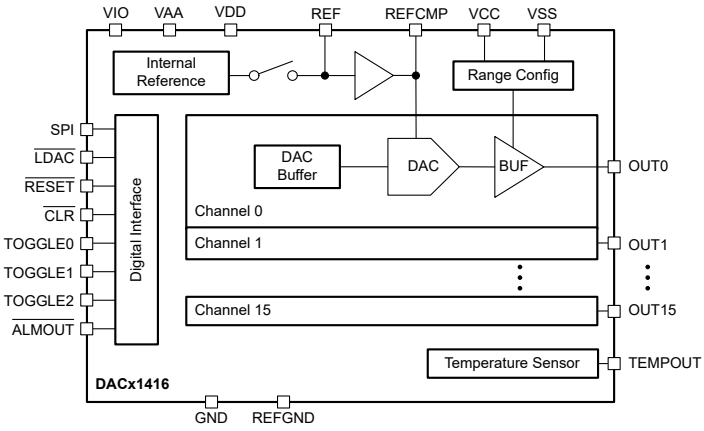
The DACx1416 incorporate a power-on-reset (POR) circuit that connects the DAC outputs to ground at power up. The outputs remain in this state until the device registers are properly configured for operation.

Communication with the DACx1416 is performed through a 4-wire serial interface that supports operation from 1.7V to 5.5V.

Device Information

PART NUMBER	RESOLUTION	PACKAGE(1)
DAC61416	12-bit	RHA (VQFN, 40)
DAC71416	14-bit	
DAC81416	16-bit	

(1) For more information, see Section 11.



Functional Block Diagram

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4 Pin Configuration and Functions

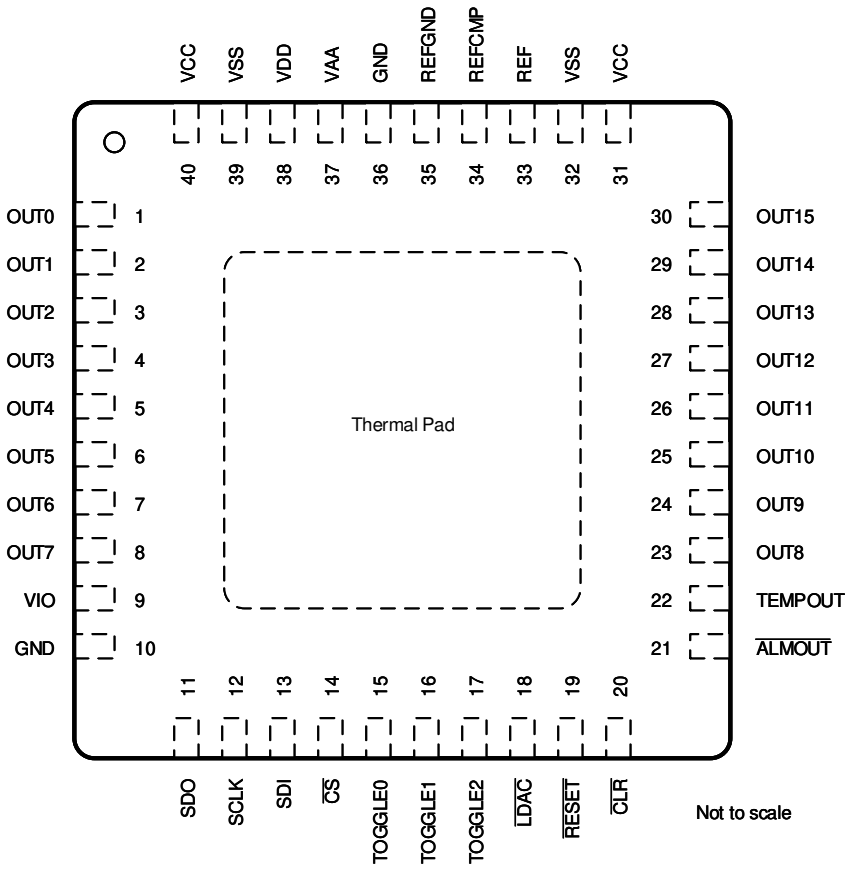

Figure 4-1. RHA Package, 40-Pin VQFN, Top View

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Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	OUT0	Output	Channel 0 analog DAC output voltage.
2	OUT1	Output	Channel 1 analog DAC output voltage.
3	OUT2	Output	Channel 2 analog DAC output voltage.
4	OUT3	Output	Channel 3 analog DAC output voltage.
5	OUT4	Output	Channel 4 analog DAC output voltage.
6	OUT5	Output	Channel 5 analog DAC output voltage.
7	OUT6	Output	Channel 6 analog DAC output voltage.
8	OUT7	Output	Channel 7 analog DAC output voltage.
9	VIO	Power	IO supply voltage. (1.7 V to 5.5 V). This pin sets the I/O operating voltage for the device.
10, 36	GND	Ground	Ground reference point for all circuitry on the device.
11	SDO	Output	Serial interface data output. Enable the SDO pin before operation by setting the SDO-EN bit. Data are clocked out of the input shift register on either rising or falling edges of the SCLK pin as specified by the FSDO bit (rising edge by default).
12	SCLK	Input	Serial interface clock.
13	SDI	Input	Serial interface data input. Data are clocked into the input shift register on each falling edge of the SCLK pin.
14	$\overline{\text{CS}}$	Input	Active low serial data enable. This input is the frame synchronization signal for the serial data. When the signal goes low, the serial interface input shift register is enabled.
15	TOGGLE0	Input	Toggle pin 0. Control signal for those DAC outputs configured for toggle operation to switch between the two DAC data registers associated with each DAC. A logic low updates the DAC output to the value set by Register A. A logic high updates the DAC output to the value set by Register B. Connect the TOGGLE0 pin to ground if unused.
16	TOGGLE1	Input	Toggle pin 1. Control signal for those DAC outputs configured for toggle operation to switch between the two DAC data registers associated with each DAC. A logic low updates the DAC output to the value set by Register A. A logic high updates the DAC output to the value set by Register B. Connect the TOGGLE1 pin to ground if unused.
17	TOGGLE2	Input	Toggle pin 2. Control signal for those DAC outputs configured for toggle operation to switch between the two DAC data registers associated with each DAC. A logic low updates the DAC output to the value set by Register A. A logic high updates the DAC output to the value set by Register B. Connect the TOGGLE2 pin to ground if unused.
18	$\overline{\text{LDAC}}$	Input	Active low synchronization signal. When the $\overline{\text{LDAC}}$ pin is low, the DAC outputs of those channels configured in synchronous mode are updated simultaneously. Connect to VIO if unused.
19	$\overline{\text{RESET}}$	Input	Active low reset input. Logic low on this pin causes the device to issue a power-on-reset event.
20	$\overline{\text{CLR}}$	Input	Active low clear input. Logic low on this pin clears all DAC outputs to the clear code. Connect to VIO if unused.
21	$\overline{\text{ALMOUT}}$	Output	$\overline{\text{ALMOUT}}$ is an open drain alarm output. An external 10-kΩ pullup resistor to a voltage no greater than V_{IO} is required.
22	TEMPOUT	Output	Analog temperature monitor output.
23	OUT8	Output	Channel 8 analog DAC output voltage.
24	OUT9	Output	Channel 9 analog DAC output voltage.
25	OUT10	Output	Channel 10 analog DAC output voltage.
26	OUT11	Output	Channel 11 analog DAC output voltage.
27	OUT12	Output	Channel 12 analog DAC output voltage.
28	OUT13	Output	Channel 13 analog DAC output voltage.
29	OUT14	Output	Channel 14 analog DAC output voltage.
30	OUT15	Output	Channel 15 analog DAC output voltage.
31, 40	VCC	Power	Output positive analog power supply (9 V to 41.5 V).
32, 39	VSS	Power	Output negative analog power supply (–21.5 V to 0 V).
33	REF	Input/Output	Reference input to the device when operating with external reference. When using internal reference, this pin is the reference output voltage pin. Connect a 150-nF capacitor to ground.
34	REFCMP	Input/Output	Reference compensation capacitor connection. Connect a 330-pF capacitor between REFCMP and REFGND.
35	REFGND	Ground	Ground reference point for the internal reference.
37	VAA	Power	Analog supply voltage (4.5 V to 5.5 V). Ensure that this pin is at the same potential as the VDD pin.
38	VDD	Power	Digital supply voltage (4.5 V to 5.5 V). Ensure that this pin is at the same potential as the VAA pin.
Thermal Pad	Thermal Pad	—	The thermal pad is located on the package underside. Connect the thermal pad to any internal PCB ground plane through multiple vias for good thermal performance.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	V_{DD} to GND	–0.3	6	V
	V_{IO} to GND	–0.3	6	V
	V_{CC} to GND	–0.3	44	V
	V_{SS} to GND	–22	0.3	V
	REFGND to GND	–0.3	0.9	V
	V_{DD} to V_{AA}	–0.3	0.3	V
	V_{CC} to V_{SS}	–0.3	44	V
Pin voltage	DAC outputs to GND	V_{SS} – 0.3	V_{CC} + 0.3	V
	TEMPOUT to GND	–0.3	V_{DD} + 0.3	V
	REF and REFCMP to GND	–0.3	V_{DD} + 0.3	V
	Digital inputs to GND	–0.3	V_{IO} + 0.3	V
	SDO to GND	–0.3	V_{IO} + 0.3	V
	$\overline{\text{ALARMOUT}}$ to GND	–0.3	6	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–60	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{AA} (1)	Analog supply voltage	4.5		5.5	V
V_{DD} (1)	Digital supply voltage	4.5		5.5	V
V_{IO}	IO supply voltage	1.7		5.5	V
V_{CC}	Output buffer positive supply voltage	9		41.5	V
V_{SS} (2)	Output buffer negative supply voltage	–21.5		0	V
$V_{CC} – V_{SS}$	Output buffer supply voltage range	9		43	V
	Digital input voltage	0		V_{IO}	V
V_{REFIN}	Reference input voltage to V_{REFGND}	2.49	2.5	2.51	V
V_{REFGND} (3)	REFGND pin voltage	0	0	0.6	V
T_A	Operating ambient temperature	–40		125	°C

(1) Ensure that V_{AA} and V_{DD} are at the same potential.
(2) V_{SS} is only connected to GND when all DAC outputs are unipolar.

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(3) If V_{REFGND} is not connected to GND, use a buffered source to drive V_{REFGND}.

5.4 Thermal Information

THERMAL METRIC(1)		DACx1416 RHA (VQFN) 40 PINS	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	26.8	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	14.1	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	3.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	3.4	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

all minimum/maximum specifications at T_A = –40°C to +125°C and all typical specifications at T_A = 25°C, V_{CC} = 9 V to 41.5 V, V_{SS} = –21.5 V to 0 V, V_{DD} = V_{AA} = 4.5 V to 5.5 V, V_{REFIN} = 2.5 V, V_{IO} = 1.7 V to 5.5 V, DAC outputs unloaded, digital inputs at V_{IO} or GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE(1)						
	Resolution	DAC81416	16			Bits
		DAC71416	14			
		DAC61416	12			
INL	Integral nonlinearity	DAC81416, all ranges, except 0 V to 40 V and ±2.5 V	–1	±0.5	1	LSB
		DAC81416, 0 V to 40 V and ±2.5-V ranges	–2	±1	2	
		DAC71416, all ranges	–1	±0.5	1	
		DAC61416, all ranges	–1	±0.5	1	
DNL	Differential nonlinearity	DAC81416, specified 16-bit monotonic	–1	±0.5	1	LSB
		DAC71416, specified 14-bit monotonic	–1	±0.5	1	
		DAC61416, specified 12-bit monotonic	–1	±0.5	1	
TUE	Total unadjusted error	All ranges, except ±2.5 V	–0.1	±0.01	0.1	%FSR
		±2.5-V range	–0.2	±0.02	0.2	
	Unipolar offset error	All unipolar ranges	–0.03	±0.015	0.03	%FSR
	Unipolar zero-code error	All unipolar ranges	0	0.04	0.1	%FSR
	Bipolar zero error	All bipolar ranges	–0.2	±0.02	0.2	%FSR
	Full-scale error	All ranges	–0.2	±0.075	0.2	%FSR
	Gain error	All ranges, except ±2.5 V	–0.1	±0.02	0.1	%FSR
		±2.5-V range	–0.2	±0.02	0.2	
	Unipolar offset error drift	All unipolar ranges		±2		ppm of FSR/°C
	Bipolar zero error drift	All bipolar ranges		±2		ppm of FSR/°C
	Gain error drift	All ranges		±2		ppm of FSR/°C
	Output voltage drift over time	T_A = 40°C, full-scale code, 1900 hours		5		ppm of FSR

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5.5 Electrical Characteristics (continued)

all minimum/maximum specifications at T_A = –40°C to +125°C and all typical specifications at T_A = 25°C, V_{CC} = 9 V to 41.5 V, V_{SS} = –21.5 V to 0 V, V_{DD} = V_{AA} = 4.5 V to 5.5 V, V_{REFIN} = 2.5 V, V_{IO} = 1.7 V to 5.5 V, DAC outputs unloaded, digital inputs at V_{IO} or GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIFFERENTIAL MODE PERFORMANCE(1)						
TUE	Total unadjusted error	All ranges	–0.1	±0.01	0.1	%FSR
		±2.5-V range	–0.2	±0.02	0.2	
	Common-mode error	All bipolar ranges, midscale code	–0.1	±0.01	0.1	%FSR
OUTPUT CHARACTERISTICS						
	Output voltage headroom	To V_{SS} and V_{CC} (–10 mA ≤ I_{OUT} ≤ 10 mA)	1			V
		To V_{SS} and V_{CC} (–15 mA ≤ I_{OUT} ≤ 15 mA)	1.5			
	Short-circuit current(2)	Full-scale output shorted to V_{SS}		40		mA
		Zero-scale output shorted to V_{CC}		40		
	Load regulation	Midscale code, –15 mA ≤ I_{OUT} ≤ 15 mA		70		µV/mA
	Maximum capacitive load(3)	R_{LOAD} = open	0		1	nF
	DC output impedance	Midscale code		0.05		Ω
		Full-scale code		40		
DYNAMIC PERFORMANCE						
	Output voltage settling time	¼ to ¾ scale and ¾ to ¼ scale settling time to ±1 LSB, ±10-V range, R_L = 5 kΩ, C_L = 200 pF		12		µs
	Slew rate	0-V to 5-V range		1		V/µs
		All other output ranges		4		
	Power-on glitch magnitude	Power-down to active DAC output, ±20 V range, midscale code, R_L = 5 kΩ, C_L = 200 pF		0.3		V
	Output noise	0.1 Hz to 10 Hz, midscale code, 0-V to 5-V range		15		μV_{PP}
	Output noise density	1 kHz, midscale code, 0-V to 5-V range		78		nV/Hz
PSRR-AC	Power supply ac rejection ratio	Midscale code, frequency = 60 Hz, amplitude = 200 mV_{PP} superimposed on V_{DD}, V_{CC} or V_{SS}		1		LSB/V
PSRR-DC	Power supply dc rejection ratio	Midscale code, V_{DD} = 5 V ± 5%, V_{CC} = 20 V, V_{SS} = –20 V		1		LSB/V
		Midscale code, V_{DD} = 5 V, V_{CC} = 20 V ± 5%, V_{SS} = –20 V		1		
		Midscale code, V_{DD} = 5 V, V_{CC} = 20 V, V_{SS} = –20 V ± 5%		1		
	Code change glitch impulse	1-LSB change around major carrier, 0-V to 5-V range		4		nV-s
	Channel-to-channel ac crosstalk	0-V to 5-V range, measured channel at midscale, full-scale swing on all other channels		4		nV-s
	Channel-to-channel dc crosstalk	0-V to 5-V range, measured channel at midscale, all other channels at full-scale		0.25		LSB
	Digital feedthrough	0-V to 5-V range, midscale code, f_{SCLK} = 1 MHz		1		nV-s

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5.5 Electrical Characteristics (continued)

all minimum/maximum specifications at T_A = –40°C to +125°C and all typical specifications at T_A = 25°C, V_{CC} = 9 V to 41.5 V, V_{SS} = –21.5 V to 0 V, V_{DD} = V_{AA} = 4.5 V to 5.5 V, V_{REFIN} = 2.5 V, V_{IO} = 1.7 V to 5.5 V, DAC outputs unloaded, digital inputs at V_{IO} or GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EXTERNAL REFERENCE INPUT						
V_{REFIN}	Reference input voltage range	To V_{REFGND}	2.49	2.5	2.51	V
	Reference input current			50		µA
	Reference input impedance			50		kΩ
	Reference input capacitance			20		pF
INTERNAL REFERENCE						
V_{REFOUT}	Reference output voltage range	T_A = 25°C	2.4975		2.5025	V
	Reference output drift			5	15	ppm/°C
	Reference output impedance			0.1		Ω
	Reference output noise	0.1 Hz to 10 Hz		12		$µV_{PP}$
	Reference output noise density	10 kHz, REF_{LOAD} = 10 nF		150		nV/Hz
	Reference load current			5		mA
	Reference load regulation	Source		80		µV/mA
	Reference line regulation			20		µV/V
	Reference output drift over time	T_A = 25°C, 1900 hours		250		µV
	Reference thermal hysteresis	First cycle		±700		µV
		Additional cycle		±50		
DIGITAL INPUTS AND OUTPUTS						
V_{IH}	High-level input voltage		0.7 × V_{IO}			V
V_{IL}	Low-level input voltage				0.3 × V_{IO}	V
	Input current			±2		µA
	Input pin capacitance			2		pF
V_{OH}	High-level output voltage	I_{OH} = 0.2 mA	V_{IO} – 0.2			V
V_{OL}	Low-level output voltage	I_{OL} = 0.2 mA			0.4	V
	Output pin capacitance			5		pF
ALARM OUTPUT						
	Output pin capacitance			5		pF
V_{OL}	Low-level output voltage	I_{LOAD} = –0.2 mA			0.4	V
TEMPERATURE OUTPUT						
$V_{TEMPOUT,0C}$	Output voltage offset at 0°C			1.34		V
	Sensor gain			–4		mV/°C

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5.5 Electrical Characteristics (continued)

all minimum/maximum specifications at T_A = –40°C to +125°C and all typical specifications at T_A = 25°C, V_{CC} = 9 V to 41.5 V, V_{SS} = –21.5 V to 0 V, V_{DD} = V_{AA} = 4.5 V to 5.5 V, V_{REFIN} = 2.5 V, V_{IO} = 1.7 V to 5.5 V, DAC outputs unloaded, digital inputs at V_{IO} or GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER REQUIREMENTS						
I_{DD}	V_{DD} supply current	Active mode, internal reference enabled, full-scale code, ±20 V output range, SPI static		0.05	0.5	mA
		Active mode, internal reference disabled, full-scale code, ±20 V output range, SPI static		0.05	0.5	mA
		Power-down mode		0.05	0.5	mA
I_{AA}	V_{AA} supply current	Active mode, internal reference enabled, full-scale code, ±20 V output range, SPI static		20	30	mA
		Active mode, internal reference disabled, full-scale code, ±20 V output range, SPI static		18	28	mA
		Power-down mode		2	85	µA
I_{CC}	V_{CC} supply current	Active mode, internal reference enabled, full-scale code, ±20 V output range, SPI static		10	25	mA
		Active mode, internal reference disabled, full-scale code, ±20 V output range, SPI static		10	25	mA
		Power-down mode		10	30	µA
I_{SS}	V_{SS} supply current	Active mode, internal reference enabled, full-scale code, ±20 V output range, SPI static	–15	–10		mA
		Active mode, internal reference disabled, full-scale code, ±20 V output range, SPI static	–15	–10		mA
		Power-down mode	–30	–10		µA
I_{IO}	V_{IO} supply current	SCLK and SDI toggling at 50 MHz		350	500	µA

(1) End point fit between codes. 16-bit: code 256 to 65280, 14-bit: code 128 to 16256, 12-bit: code 32 to 4064.
(2) Temporary overload condition protection. Junction temperature is able to exceed limits during current limit. Operation greater than the specified maximum junction temperature potentially impairs device reliability.
(3) Specified by design and characterization, not production tested.

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5.6 Timing Requirements

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
SERIAL INTERFACE - WRITE OPERATION						
$f_{(SCLK)}$	Serial clock frequency	V_{IO} = 1.7 V to 2.7 V			25	MHz
		V_{IO} = 2.7 V to 5.5 V			50	
$t_{SCLKHIGH}$	SCLK high time	V_{IO} = 1.7 V to 2.7 V	20			ns
		V_{IO} = 2.7 V to 5.5 V	10			
$t_{SCLKLOW}$	SCLK low time	V_{IO} = 1.7 V to 2.7 V	20			ns
		V_{IO} = 2.7 V to 5.5 V	10			
t_{SDIS}	SDI setup time	V_{IO} = 1.7 V to 2.7 V	10			ns
		V_{IO} = 2.7 V to 5.5 V	5			
t_{SDIH}	SDI hold time	V_{IO} = 1.7 V to 2.7 V	10			ns
		V_{IO} = 2.7 V to 5.5 V	5			
t_{CSS}	$\overline{CS}$ to SCLK falling edge setup time	V_{IO} = 1.7 V to 2.7 V	30			ns
		V_{IO} = 2.7 V to 5.5 V	15			
t_{CSH}	SCLK falling edge to $\overline{CS}$ rising edge	V_{IO} = 1.7 V to 2.7 V	10			ns
		V_{IO} = 2.7 V to 5.5 V	5			
t_{CSHIGH}	$\overline{CS}$ high time	V_{IO} = 1.7 V to 2.7 V	50			ns
		V_{IO} = 2.7 V to 5.5 V	25			
$t_{DACWAIT}$	Sequential DAC update wait time	V_{IO} = 1.7 V to 2.7 V	2.4			µs
		V_{IO} = 2.7 V to 5.5 V	2.4			
$t_{BCASTWAIT}$	Broadcast DAC update wait time	V_{IO} = 1.7 V to 2.7 V	4			µs
		V_{IO} = 2.7 V to 5.5 V	4			
SERIAL INTERFACE - READ AND DAISY CHAIN OPERATION, FSDO = 0						
$f_{(SCLK)}$	Serial clock frequency	V_{IO} = 1.7 V to 2.7 V			15	MHz
		V_{IO} = 2.7 V to 5.5 V			20	
$t_{SCLKHIGH}$	SCLK high time	V_{IO} = 1.7 V to 2.7 V	33			ns
		V_{IO} = 2.7 V to 5.5 V	25			
$t_{SCLKLOW}$	SCLK low time	V_{IO} = 1.7 V to 2.7 V	33			ns
		V_{IO} = 2.7 V to 5.5 V	25			
t_{SDIS}	SDI setup time	V_{IO} = 1.7 V to 2.7 V	10			ns
		V_{IO} = 2.7 V to 5.5 V	5			
t_{SDIH}	SDI hold time	V_{IO} = 1.7 V to 2.7 V	10			ns
		V_{IO} = 2.7 V to 5.5 V	5			
t_{CSS}	$\overline{CS}$ to SCLK falling edge setup time	V_{IO} = 1.7 V to 2.7 V	30			ns
		V_{IO} = 2.7 V to 5.5 V	20			
t_{CSH}	SCLK falling edge to $\overline{CS}$ rising edge	V_{IO} = 1.7 V to 2.7 V	8			ns
		V_{IO} = 2.7 V to 5.5 V	5			
t_{CSHIGH}	$\overline{CS}$ high time	V_{IO} = 1.7 V to 2.7 V	50			ns
		V_{IO} = 2.7 V to 5.5 V	25			
t_{SDOZD}	SDO tri-state condition to driven	V_{IO} = 1.7 V to 2.7 V	0		20	ns
		V_{IO} = 2.7 V to 5.5 V	0		20	
t_{SDODLY}	SDO output delay	V_{IO} = 1.7 V to 2.7 V	0		35	ns
		V_{IO} = 2.7 V to 5.5 V	0		20	

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5.6 Timing Requirements (continued)

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
SERIAL INTERFACE - READ AND DAISY CHAIN OPERATION, FSDO = 1						
$f_{(SCLK)}$	Serial clock frequency	V_{IO} = 1.7 V to 2.7 V			25	MHz
		V_{IO} = 2.7 V to 5.5 V			35	
$t_{SCLKHIGH}$	SCLK high time	V_{IO} = 1.7 V to 2.7 V	20			ns
		V_{IO} = 2.7 V to 5.5 V	14			
$t_{SCLKLOW}$	SCLK low time	V_{IO} = 1.7 V to 2.7 V	20			ns
		V_{IO} = 2.7 V to 5.5 V	14			
t_{SDIS}	SDI setup time	V_{IO} = 1.7 V to 2.7 V	10			ns
		V_{IO} = 2.7 V to 5.5 V	5			
t_{SDIH}	SDI hold time	V_{IO} = 1.7 V to 2.7 V	10			ns
		V_{IO} = 2.7 V to 5.5 V	5			
t_{CSS}	$\overline{CS}$ to SCLK falling edge setup time	V_{IO} = 1.7 V to 2.7 V	30			ns
		V_{IO} = 2.7 V to 5.5 V	20			
t_{CSH}	SCLK falling edge to $\overline{CS}$ rising edge	V_{IO} = 1.7 V to 2.7 V	8			ns
		V_{IO} = 2.7 V to 5.5 V	5			
t_{CSHIGH}	$\overline{CS}$ high time	V_{IO} = 1.7 V to 2.7 V	50			ns
		V_{IO} = 2.7 V to 5.5 V	25			
t_{SDOZD}	SDO tri-state condition to driven	V_{IO} = 1.7 V to 2.7 V	0		20	ns
		V_{IO} = 2.7 V to 5.5 V	0		20	
t_{SDODLY}	SDO output delay	V_{IO} = 1.7 V to 2.7 V	0		35	ns
		V_{IO} = 2.7 V to 5.5 V	0		20	
DIGITAL LOGIC						
t_{LOGDLY}	$\overline{CS}$ rising edge to $\overline{LDAC}$ or $\overline{CLR}$ falling edge delay time	VIO = 1.7 V to 2.7 V	40			ns
t_{LOGDLY}	$\overline{CS}$ rising edge to $\overline{LDAC}$ or $\overline{CLR}$ falling edge delay time	VIO = 2.7 V to 5.5 V	20			
t_{LDAC}	$\overline{LDAC}$ low time	VIO = 1.7 V to 2.7 V	20			ns
		VIO = 2.7 V to 5.5 V	10			
t_{CLR}	$\overline{CLR}$ low time	VIO = 1.7 V to 2.7 V	20			ns
		VIO = 2.7 V to 5.5 V	10			
t_{RESET}	POR reset delay	VIO = 1.7 V to 2.7 V			1	ms
		VIO = 2.7 V to 5.5 V			1	
f_{TOGGLE}	TOGGLE frequency	VIO = 1.7 V to 2.7 V			100	kHz
		VIO = 2.7 V to 5.5 V			100	

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5.7 Timing Diagrams

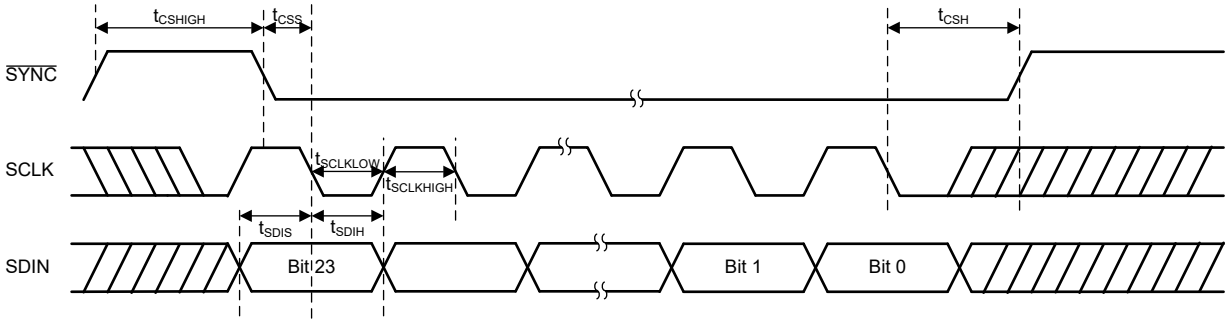

Figure 5-1. Serial Interface Write Timing Diagram

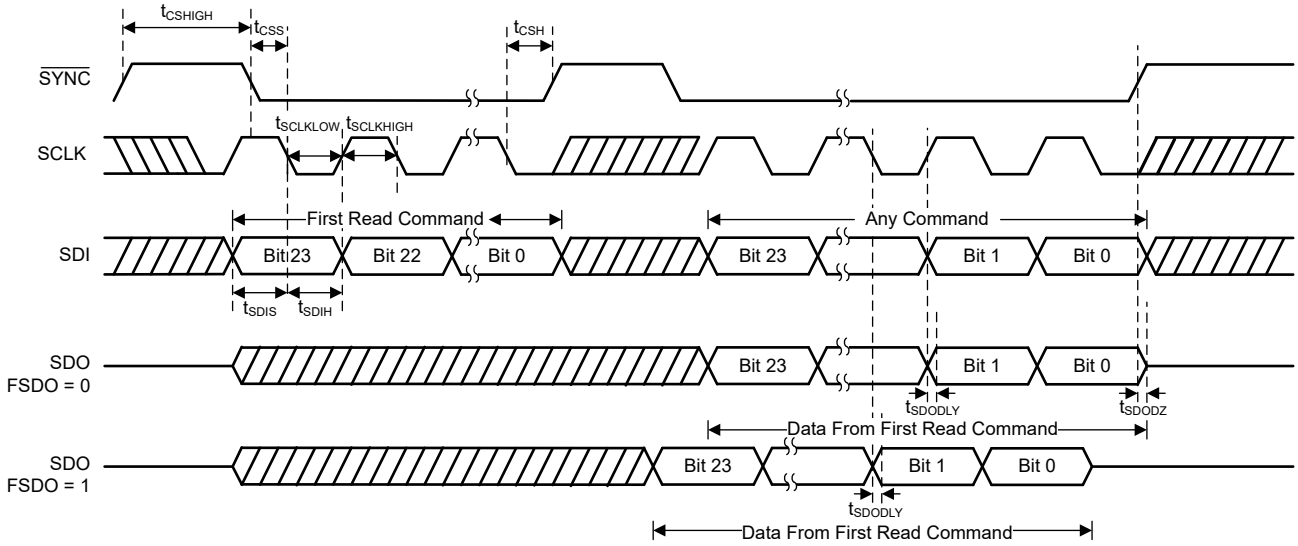

Figure 5-2. Serial Interface Read Timing Diagram

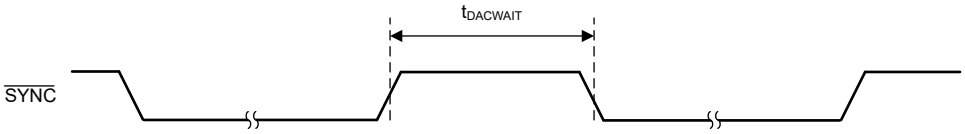

Figure 5-3. DAC Wait Time in Update Mode

5.8 Typical Characteristics

at T_A = 25°C, V_{DD} = V_{AA} = 5 V, V_{REFIN} = 2.5 V, unipolar ranges: V_{SS} = 0 V and V_{CC} ≥ V_{MAX} + 1.5 V for the DAC range, bipolar ranges: V_{SS} ≤ V_{MIN} – 1.5 V and V_{CC} ≥ V_{MAX} + 1.5 V for the DAC range, and DAC outputs unloaded (unless otherwise noted)

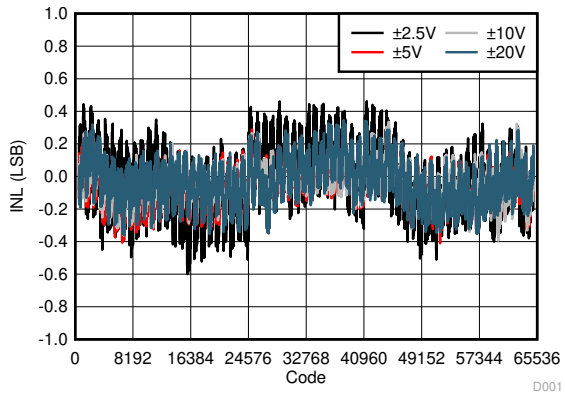

Figure 5-4. Integral Linearity Error vs Digital Input Code (Bipolar Outputs)

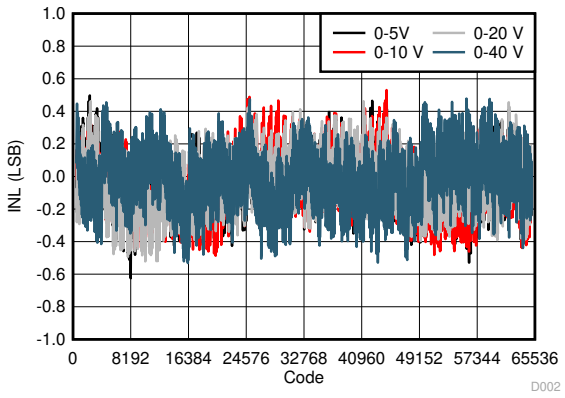

Figure 5-5. Integral Linearity Error vs Digital Input Code (Unipolar Outputs)

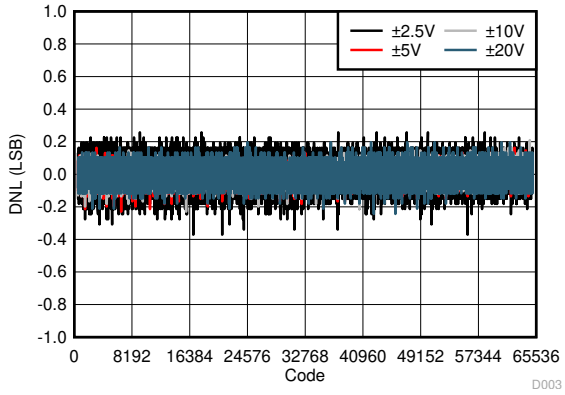

Figure 5-6. Differential Linearity Error vs Digital Input Code (Bipolar Outputs)

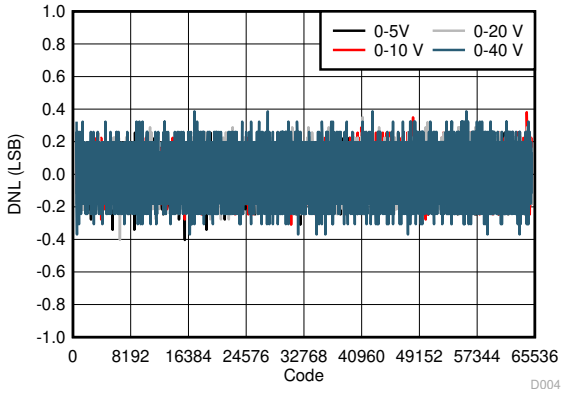

Figure 5-7. Differential Linearity Error vs Digital Input Code (Unipolar Outputs)

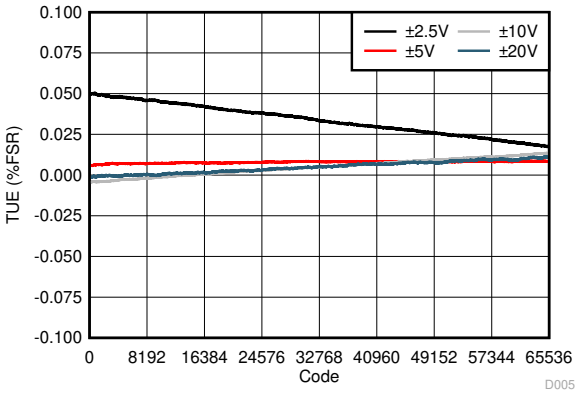

Figure 5-8. Total Unadjusted Error vs Digital Input Code (Bipolar Outputs)

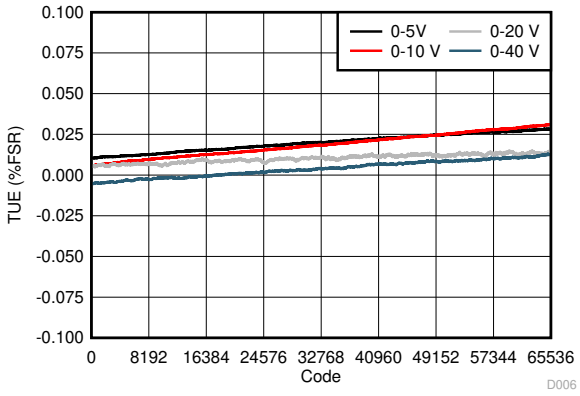

Figure 5-9. Total Unadjusted Error vs Digital Input Code (Unipolar Outputs)

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5.8 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = V_{AA} = 5 V, V_{REFIN} = 2.5 V, unipolar ranges: V_{SS} = 0 V and V_{CC} ≥ V_{MAX} + 1.5 V for the DAC range, bipolar ranges: V_{SS} ≤ V_{MIN} – 1.5 V and V_{CC} ≥ V_{MAX} + 1.5 V for the DAC range, and DAC outputs unloaded (unless otherwise noted)

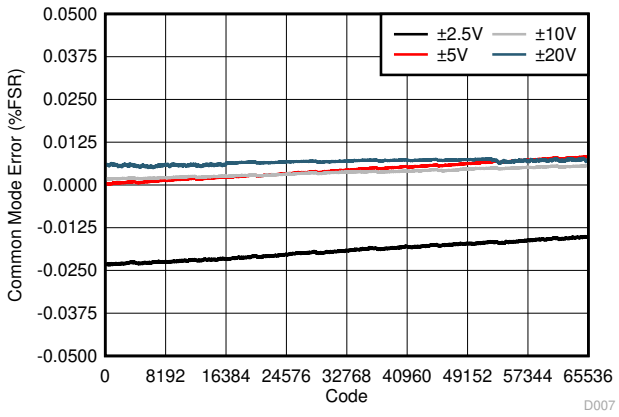


Figure 5-10. Common Mode Error vs Digital Input Code (Differential Bipolar Outputs)

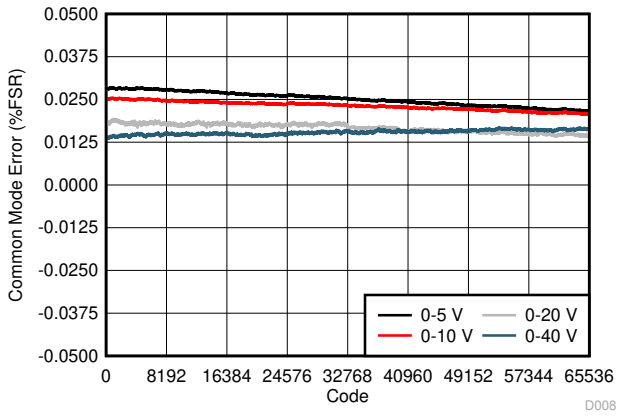
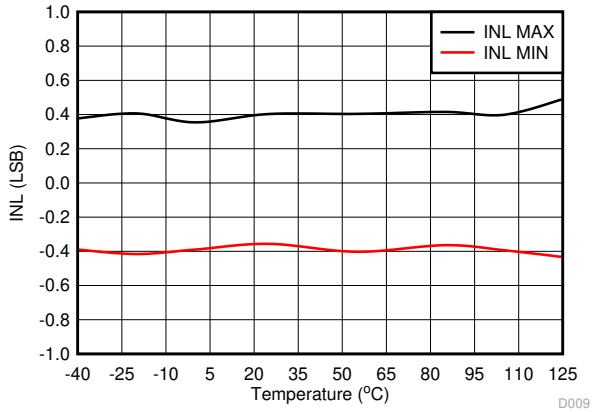
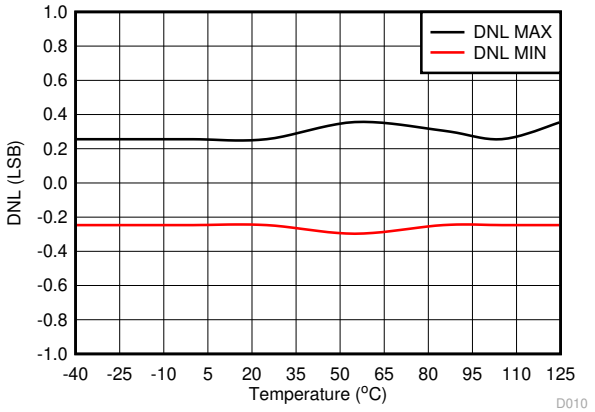


Figure 5-11. Common Mode Error vs Digital Input Code (Differential Unipolar Outputs)



±20-V output range

Figure 5-12. Integral Linearity Error vs Temperature



±20-V output range

Figure 5-13. Differential Linearity Error vs Temperature

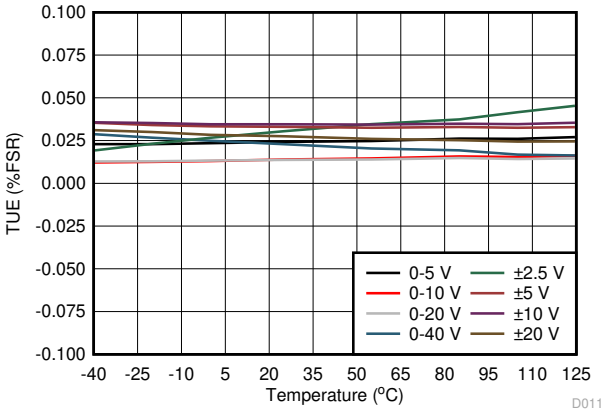


Figure 5-14. Total Unadjusted Error vs Temperature

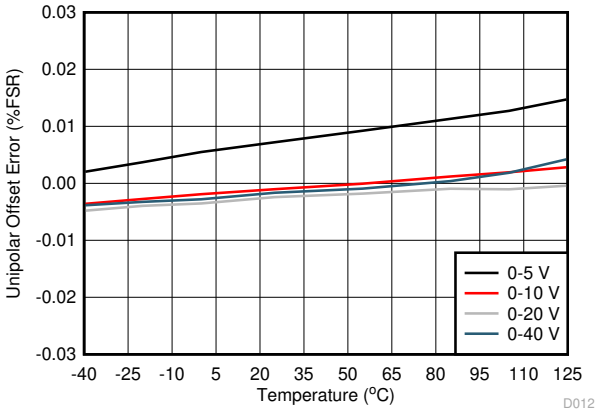


Figure 5-15. Unipolar Offset Error vs Temperature

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5.8 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = V_{AA} = 5 V, V_{REFIN} = 2.5 V, unipolar ranges: V_{SS} = 0 V and V_{CC} ≥ V_{MAX} + 1.5 V for the DAC range, bipolar ranges: V_{SS} ≤ V_{MIN} – 1.5 V and V_{CC} ≥ V_{MAX} + 1.5 V for the DAC range, and DAC outputs unloaded (unless otherwise noted)

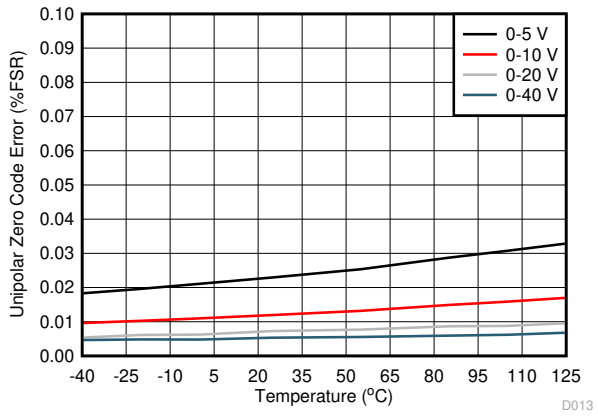

Figure 5-16. Unipolar Zero Code Error vs Temperature

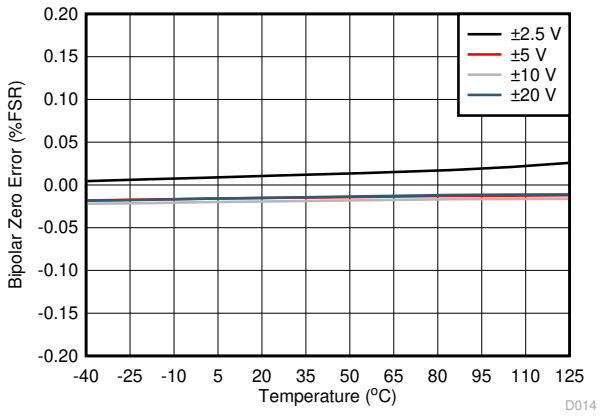

Figure 5-17. Bipolar Zero Error vs Temperature

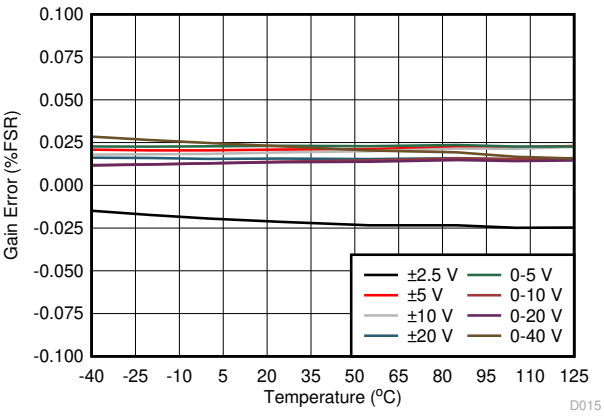

Figure 5-18. Gain Error vs Temperature

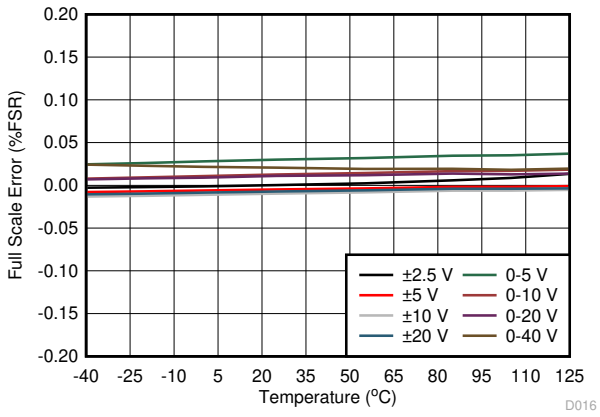

Figure 5-19. Full-Scale Error vs Temperature

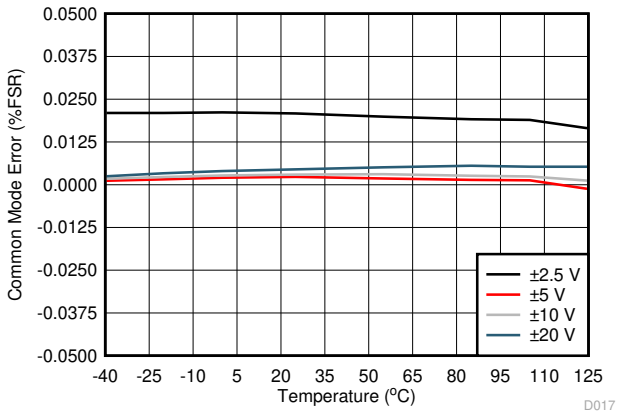

Figure 5-20. Common Mode Error vs Temperature (Differential Bipolar Outputs)

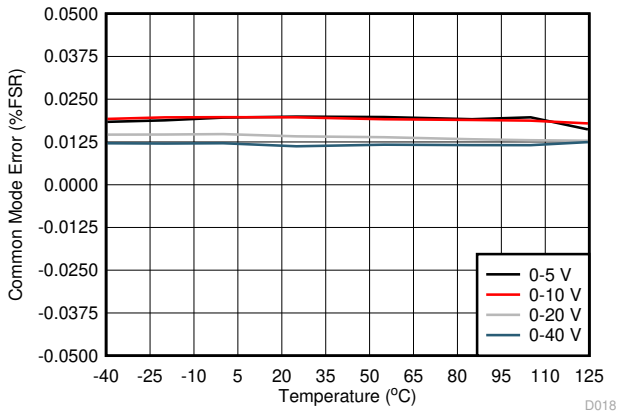

Figure 5-21. Common Mode Error vs Temperature (Differential Unipolar Outputs)

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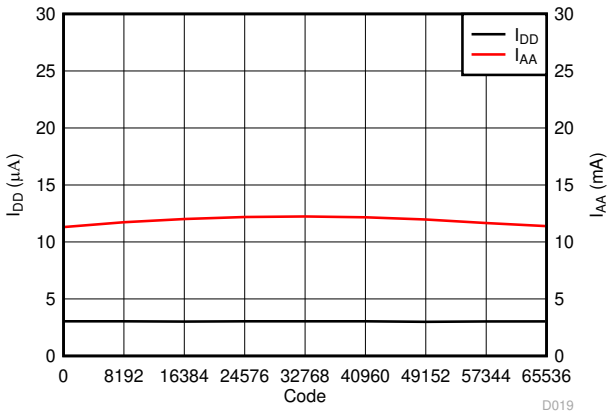
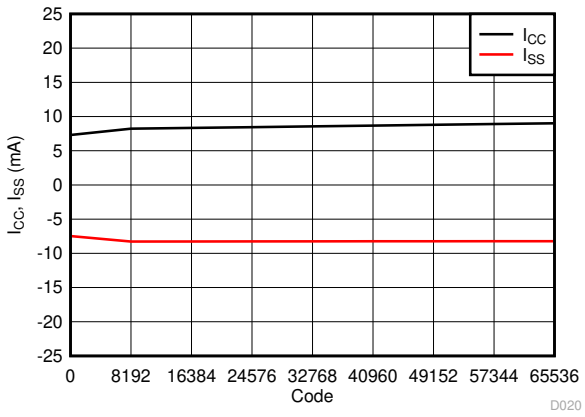
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = V_{AA} = 5 V, V_{REFIN} = 2.5 V, unipolar ranges: V_{SS} = 0 V and V_{CC} ≥ V_{MAX} + 1.5 V for the DAC range, bipolar ranges: V_{SS} ≤ V_{MIN} – 1.5 V and V_{CC} ≥ V_{MAX} + 1.5 V for the DAC range, and DAC outputs unloaded (unless otherwise noted)



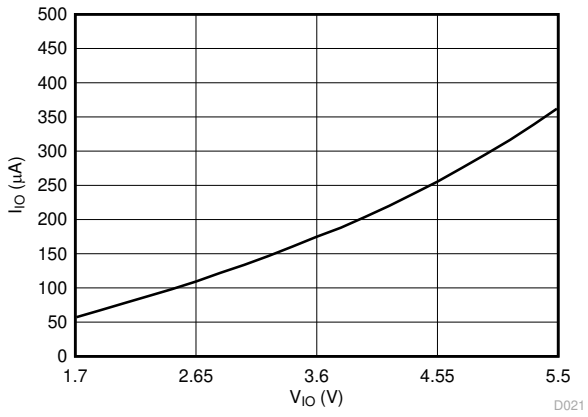
±20-V output range

Figure 5-22. Supply Current (I_{DD}, I_{AA}) vs Digital Input Code



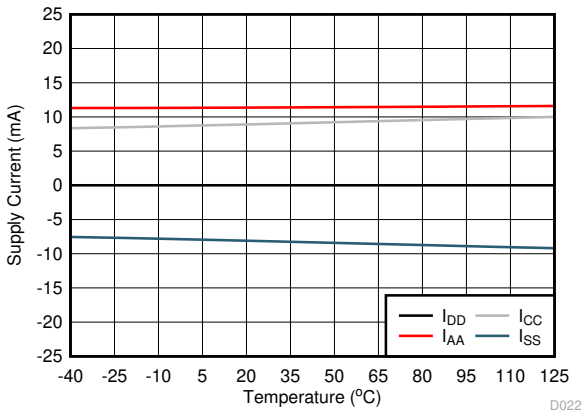
±20-V output range

Figure 5-23. Supply Current (I_{CC}, I_{SS}) vs Digital Input Code



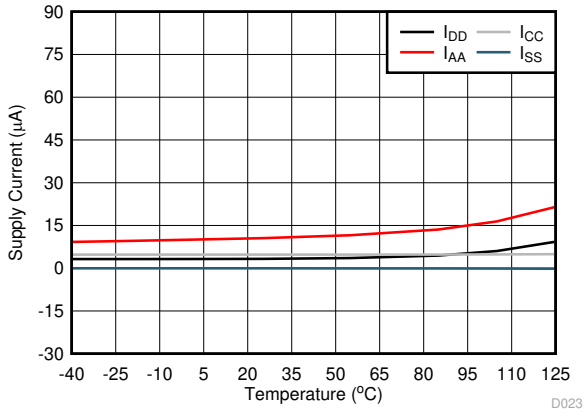
±20-V output range

Figure 5-24. Supply Current (I_{IO}) vs Supply Voltage



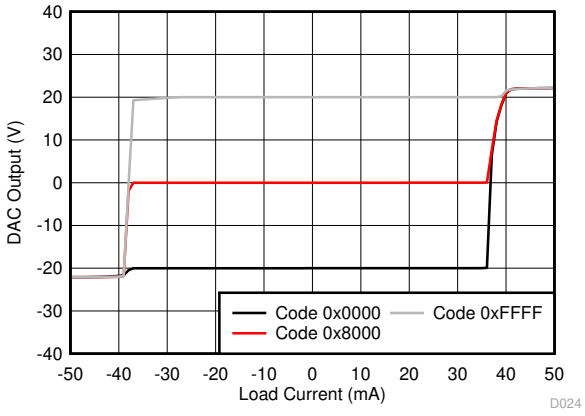
±20-V output range

Figure 5-25. Supply Current vs Temperature



±20-V output range

Figure 5-26. Power-Down Current vs Temperature

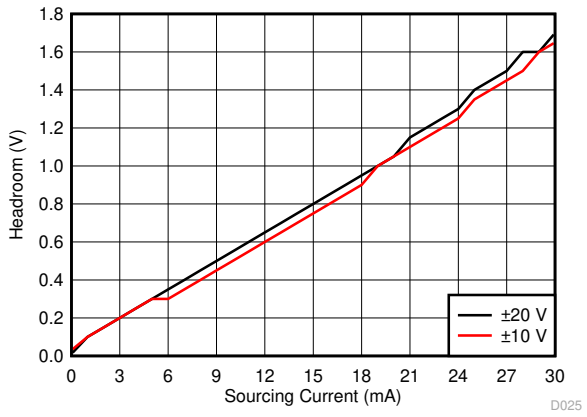


±20-V output range

Figure 5-27. Source and Sink Capability

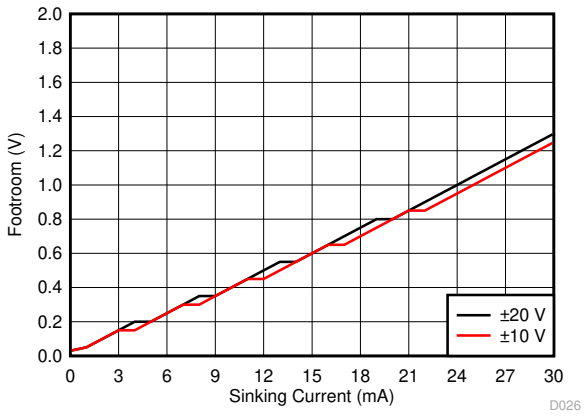
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = V_{AA} = 5 V, V_{REFIN} = 2.5 V, unipolar ranges: V_{SS} = 0 V and V_{CC} ≥ V_{MAX} + 1.5 V for the DAC range, bipolar ranges: V_{SS} ≤ V_{MIN} – 1.5 V and V_{CC} ≥ V_{MAX} + 1.5 V for the DAC range, and DAC outputs unloaded (unless otherwise noted)



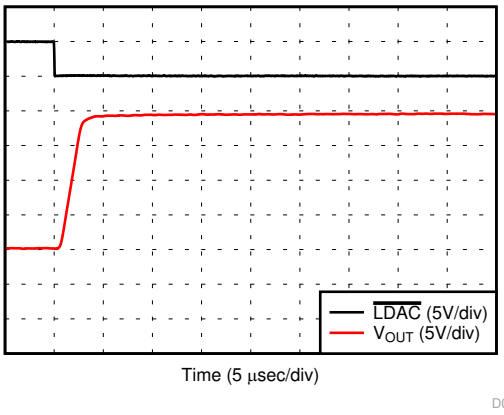
Full-scale code

Figure 5-28. V_{CC} Headroom vs Sourcing Current



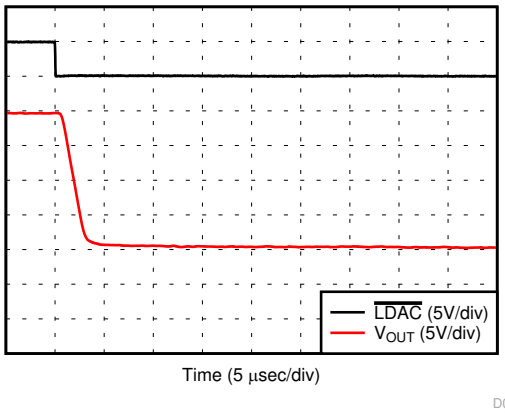
Zero code

Figure 5-29. V_{SS} Footroom vs Sinking Current



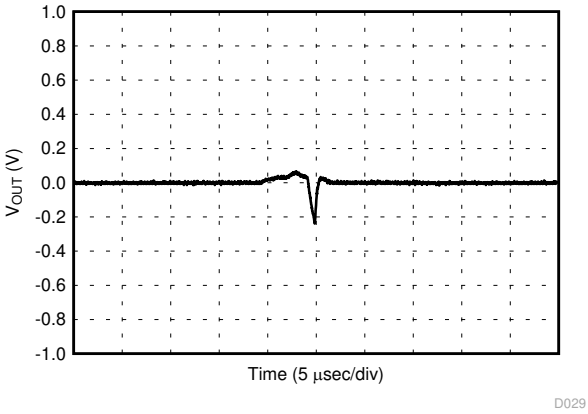
±20-V output range

Figure 5-30. Full-Scale Settling Time, Rising Edge



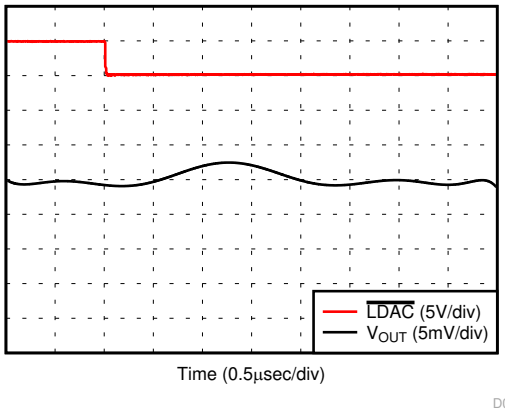
±20-V output range

Figure 5-31. Full-Scale Settling Time, Falling Edge



Power-down to active DAC mode
±20-V output range

Figure 5-32. DAC Output Enable Glitch



0-V to 5-V output range

Figure 5-33. Glitch Impulse, 1 LSB Step

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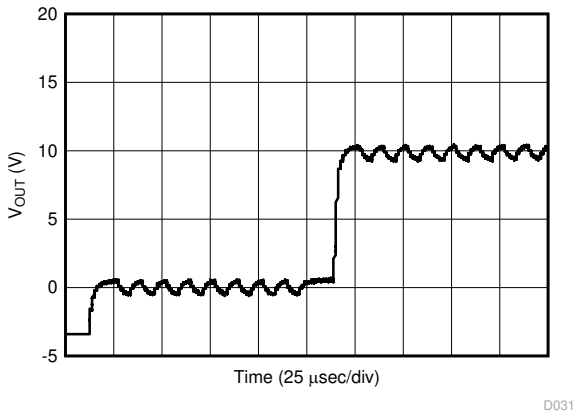
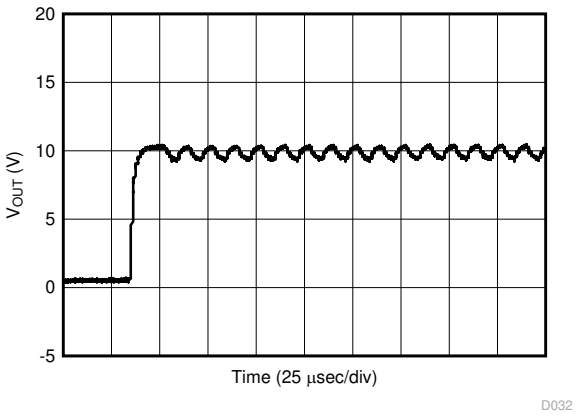
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = V_{AA} = 5 V, V_{REFIN} = 2.5 V, unipolar ranges: V_{SS} = 0 V and V_{CC} ≥ V_{MAX} + 1.5 V for the DAC range, bipolar ranges: V_{SS} ≤ V_{MIN} – 1.5 V and V_{CC} ≥ V_{MAX} + 1.5 V for the DAC range, and DAC outputs unloaded (unless otherwise noted)



±20-V output range
Toggle signal: 1 V_{PP}
DC change: midscale to 3/4 full-scale

Figure 5-34. Toggle Output Change Response



±20-V output range
Toggle signal: 1 V_{PP}
DC value: 3/4 full-scale

Figure 5-35. Toggle Enable Response

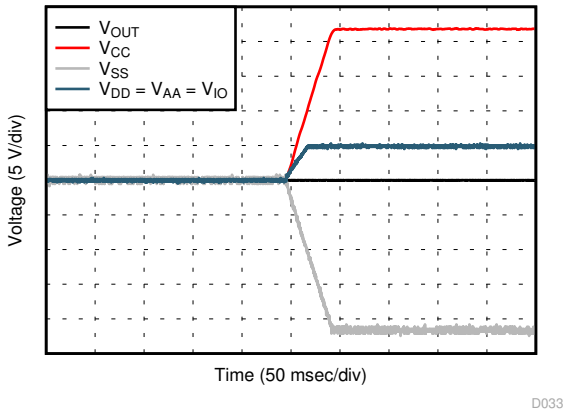


Figure 5-36. Power-Up Response

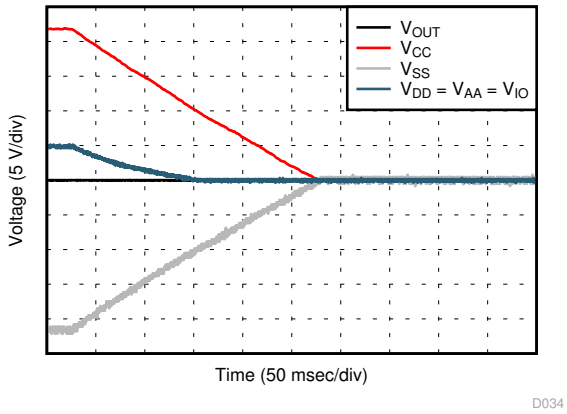
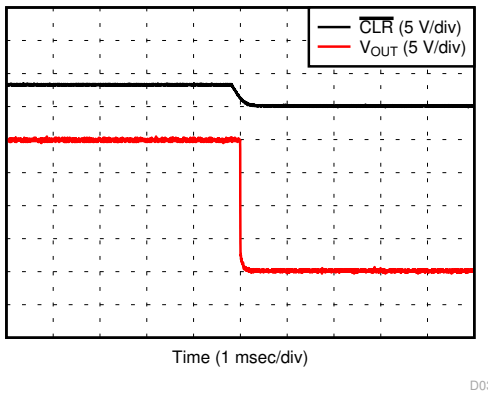
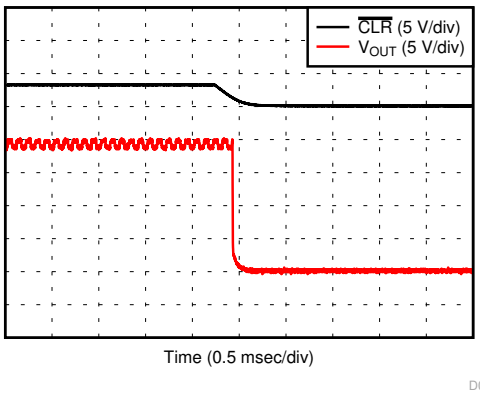


Figure 5-37. Power-Down Response



±20-V output range
Full-scale code to 0 V

Figure 5-38. Clear Command Response



±20-V output range
Toggle signal: 1 V_{PP}
DC value at 20 V

Figure 5-39. Clear Command Response in Toggle Mode

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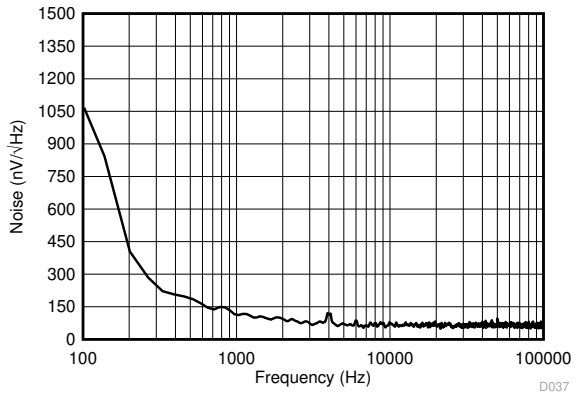
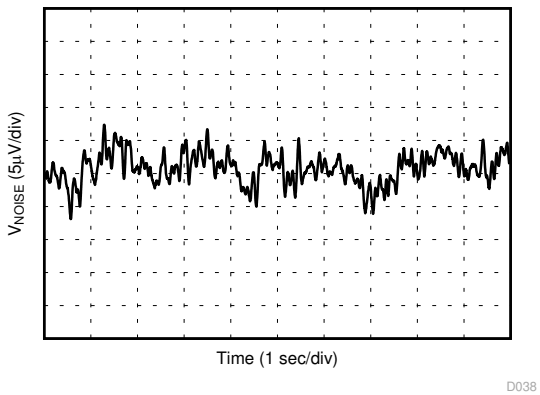
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = V_{AA} = 5 V, V_{REFIN} = 2.5 V, unipolar ranges: V_{SS} = 0 V and V_{CC} ≥ V_{MAX} + 1.5 V for the DAC range, bipolar ranges: V_{SS} ≤ V_{MIN} – 1.5 V and V_{CC} ≥ V_{MAX} + 1.5 V for the DAC range, and DAC outputs unloaded (unless otherwise noted)



0-V to 5-V output range
Midscale code

Figure 5-40. DAC Output Noise Density vs Frequency



0-V to 5-V output range
Midscale code

Figure 5-41. DAC Output Noise

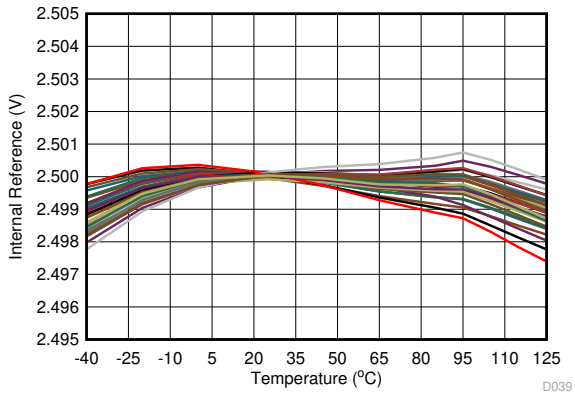


Figure 5-42. Internal Reference Voltage vs Temperature

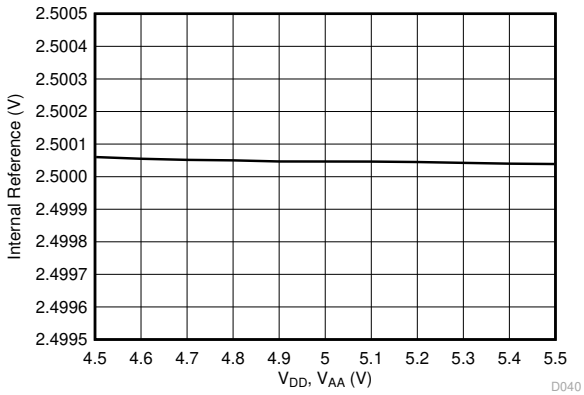


Figure 5-43. Internal Reference Voltage vs Supply Voltage

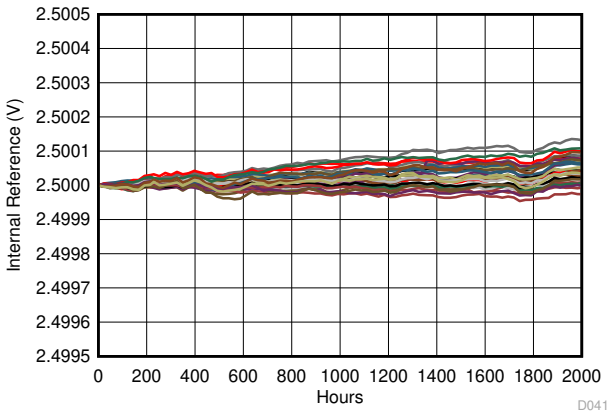


Figure 5-44. Internal Reference Voltage vs Time

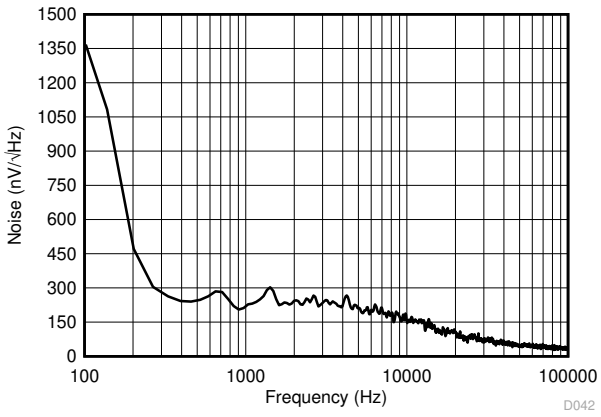


Figure 5-45. Internal Reference Noise Density vs Frequency

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5.8 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = V_{AA} = 5 V, V_{REFIN} = 2.5 V, unipolar ranges: V_{SS} = 0 V and V_{CC} ≥ V_{MAX} + 1.5 V for the DAC range, bipolar ranges: V_{SS} ≤ V_{MIN} – 1.5 V and V_{CC} ≥ V_{MAX} + 1.5 V for the DAC range, and DAC outputs unloaded (unless otherwise noted)

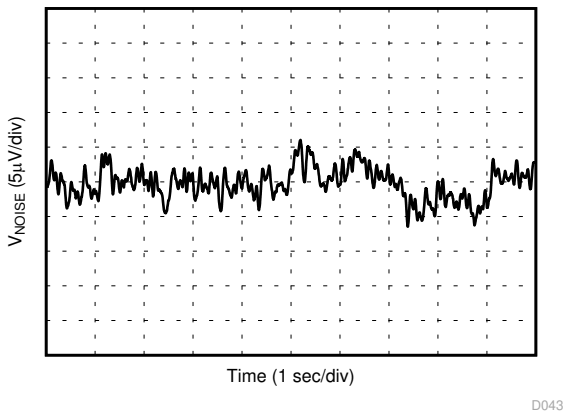


Figure 5-46. Internal Reference Noise

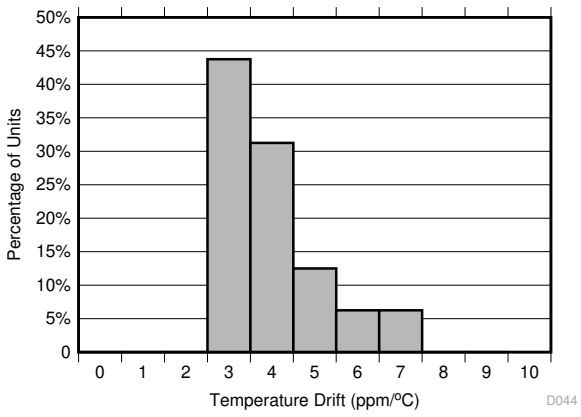


Figure 5-47. Internal Reference Temperature Drift Histogram

6 Detailed Description

6.1 Overview

The DACx1416 are a pin-compatible family of 16-channel, buffered, high-voltage output digital-to-analog converters (DACs) with 16-bit, 14-bit, and 12-bit resolution. The DACx1416 include a 2.5-V internal reference. A user-selectable output configuration enables full-scale bipolar output voltages of ±20 V, ±10 V, ±5 V or ±2.5 V, and full-scale unipolar output voltages of 40 V, 20 V, 10 V or 5 V. The full-scale output range for each DAC channel is independently programmable. In addition, each pair of DAC channels are configurable to provide a differential output. Three dedicated A-B toggle pins enable dither signal generation with up to three possible frequencies.

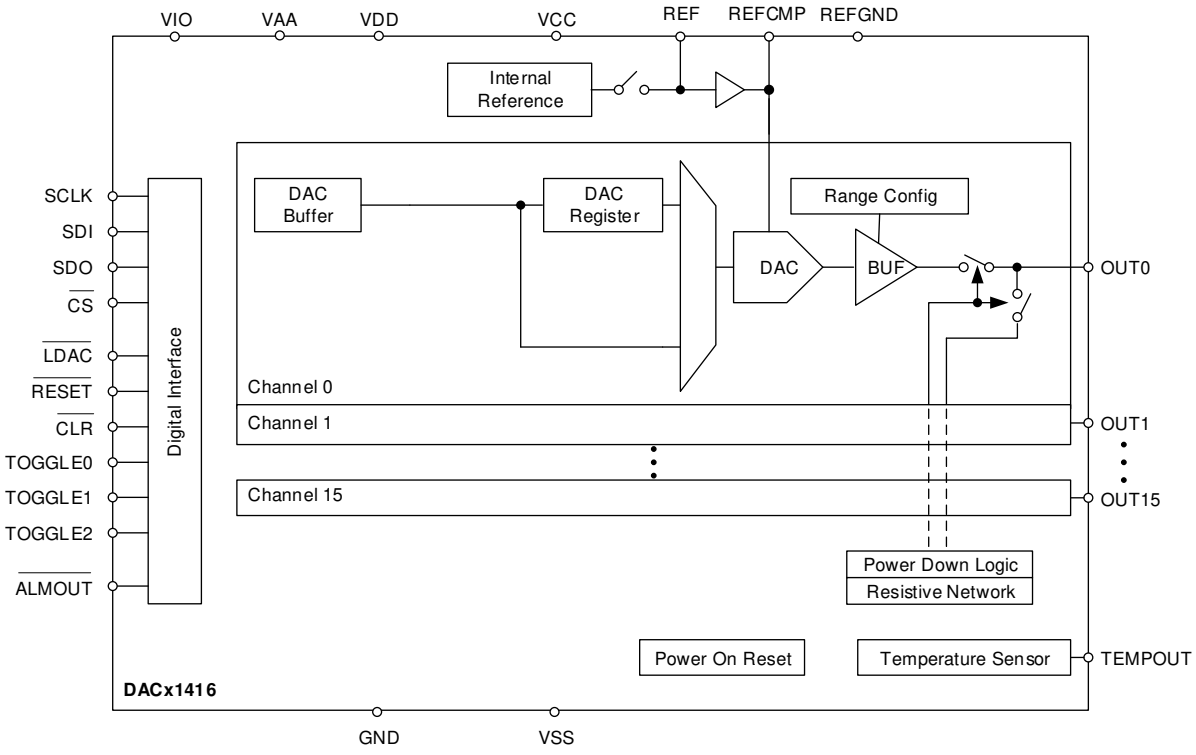
The DACx1416 operate from five supply voltages: V_{DD}, V_{AA}, V_{CC}, V_{SS} and V_{IO}.

- V_{DD} and V_{AA} are the digital and analog supplies for the DACs, internal reference, and other low voltage components. Set V_{DD} and V_{AA} to the same potential.
- V_{CC} and V_{SS} are the positive and analog supplies for the DAC output amplifiers.
- V_{IO} sets the logic levels for the digital inputs and outputs.

Communication with the DACx1416 is performed through a 4-wire serial interface that supports standalone and daisy-chain operation. The optional frame-error checking provides added robustness to the DACx1416 serial interface.

The DACx1416 incorporate a power-on-reset (POR) circuit that connects the DAC outputs to ground at power up. The outputs remain in this state until the device registers are properly configured for operation.

6.2 Functional Block Diagram



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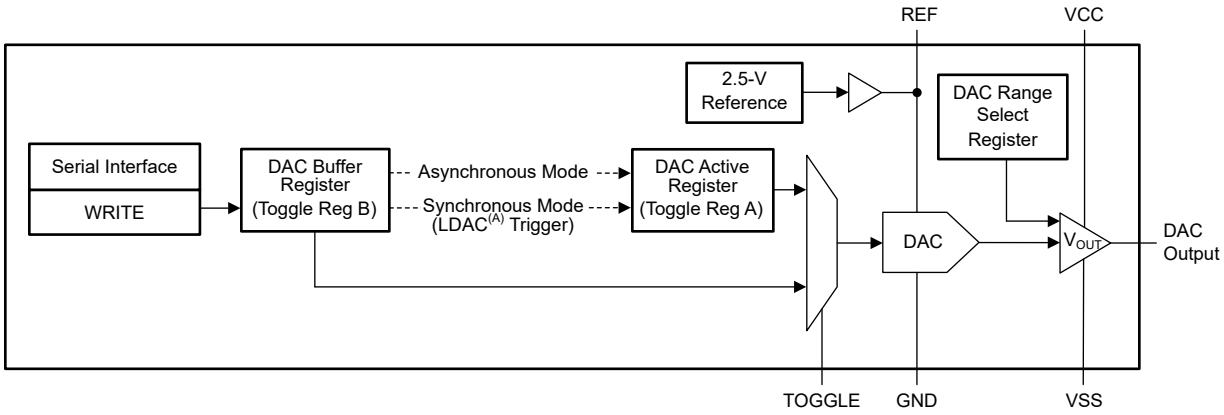
6.3 Feature Description

6.3.1 Digital-to-Analog Converter (DAC) Architecture

Each output channel in the DACx1416 consists of an R-2R ladder architecture followed by an output buffer amplifier capable of rail-to-rail operation. The output amplifiers drive 25 mA with 1.5-V headroom from either V_{CC} or V_{SS} while maintaining the specified TUE specification for the device. The full-scale output voltage for each channel are individually configurable to the following ranges:

- –20 V to +20 V
- –10 V to +10 V
- –5 V to +5 V
- –2.5 V to +2.5 V
- 0 V to 40 V
- 0 V to 20 V
- 0 V to 10 V
- 0 V to 5 V

Figure 6-1 shows a block diagram of the DAC architecture.



A. The DAC trigger is generated by either by writing 1 to the LDAC bit or by the $\overline{\text{LDAC}}$ pin in synchronous mode. In asynchronous mode, the DAC latch is transparent.

Figure 6-1. DACx1416 DAC Block Diagram

6.3.1.1 DAC Transfer Function

The input data are written to the individual DAC Data registers in straight binary format for all output ranges. The DAC transfer function is given by Equation 1.

$$V_{OUT} = \left(\frac{CODE}{2^n} \times FSR \right) + V_{MIN} \quad (1)$$

where:

- CODE is the decimal equivalent of the binary code that is loaded to the DAC register. CODE range is from 0 to $2^n - 1$.
- n is the DAC resolution in bits. Either 12 (DAC61416), 14 (DAC71416) or 16 (DAC81416).
- FSR is the DAC full-scale range. Equal to $V_{MAX} – V_{MIN}$ for the selected DAC output range.
- V_{MIN} is the lowest voltage for the selected DAC output range.

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6.3.1.2 DAC Register Structure

Data written to the DAC data registers is initially stored in the DAC buffer registers. Transfer of data from the DAC buffer registers to the active DAC registers can be configured to happen immediately (asynchronous mode) or initiated by a DAC trigger signal (synchronous mode). Once the DAC active registers are updated, the DAC outputs change to the new values.

After a power-on or reset event, all DAC registers are set to zero code, the DAC output amplifiers are powered down, and the DAC outputs are clamped to ground.

6.3.1.2.1 DAC Register Synchronous and Asynchronous Updates

The update mode for each DAC channel is determined by the status of the corresponding SYNC-EN bit. In asynchronous mode, a write to the DAC data register results in an immediate update of the DAC active register and DAC output on a $\overline{CS}$ rising edge. In synchronous mode, writing to the DAC data register does not automatically update the DAC output. Instead the update occurs only after a trigger event. A DAC trigger signal is generated either through the LDAC bit or by the $\overline{LDAC}$ pin. The synchronous update mode enables simultaneous update of multiple DAC outputs. In both update modes a minimum wait time of 2.4 µs is required between DAC output updates.

6.3.1.2.2 Broadcast DAC Register

The DAC broadcast register enables a simultaneous update of multiple DAC outputs with the same value with a single register write. Broadcast operation is only possible when all DAC channels are in single-ended mode operation. If one or more outputs are configured in differential mode the broadcast command is ignored.

Each DAC channel can be configured to update or remain unaffected by a broadcast command by setting the corresponding DAC-BRDCAST-EN bit. A register write to the BRDCAST register forces those DAC channels that are configured for broadcast operation to update the respective DAC buffer registers to this value. The DAC outputs update to the broadcast value according to the synchronous mode configuration.

6.3.1.2.3 Clear DAC Operation

The DAC outputs are set to clear mode through the $\overline{CLR}$ pin. In clear mode, each DAC data channel is set to the clear code associated with the respective configuration shown in Table 6-1. A $\overline{CLR}$ pin logic low forces all DAC channels to clear the contents of the respective buffer and active registers to the clear code, and sets the analog outputs accordingly regardless of the synchronization setting.

Table 6-1. Clear DAC Value

UNIPOLAR OR BIPOLAR RANGE	DIFFERENTIAL MODE	CLEAR CODE
Unipolar	No	Zero code
Unipolar	Yes	Midscale code
Bipolar	No	Midscale code
Bipolar	Yes	Midscale code

When a DAC is operating in toggle mode, a clear command sets both toggle registers to the clear value.

6.3.2 Internal Reference

The DAx1416 includes a precision 2.5-V band-gap reference with a typical temperature drift of 5 ppm/°C. The internal reference is externally available at the REF pin. An external buffer amplifier with a high-impedance input is required to drive any external load.

A minimum 150-nF capacitor is recommended between the reference output and GND for noise filtering. Connect a compensation capacitor (330 pF, typical) between the REFCMP pin and REFGND.

Operation from an external reference is also supported by powering down the internal reference. Apply the external reference to the REF pin.

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6.3.3 Device Reset Options

6.3.3.1 Power-On Reset (POR)

The DACx1416 includes a power-on reset function. After the supplies are established, a POR event is issued. The POR causes all registers to initialize to default values and communication with the device is valid only after a 1-ms POR delay. After a POR event, the device is set in power-down mode where all DAC channels and internal reference are powered down and the DAC output pins are connected to ground through a 10-kΩ internal resistor.

6.3.3.2 Hardware Reset

A device hardware reset event is initiated by a minimum 500 ns logic low on the $\overline{\text{RESET}}$ pin. A hardware reset initiates a POR event.

6.3.3.3 Software Reset

A device software reset event is initiated by writing the reserved code 0x1010 to SOFT-RESET in the TRIGGER register. The software reset command is triggered on the $\overline{\text{CS}}$ rising edge of the instruction. A software reset initiates a POR event.

6.3.4 Thermal Protection

Because of the device DAC channel density and high drive capability, make sure that the effects of power dissipation on the device temperature are understood and that the device temperature does not exceed the maximum junction temperature.

6.3.4.1 Analog Temperature Sensor: TEMPOUT Pin

The DACx1416 includes an analog temperature monitor with an unbuffered output voltage that is inversely proportional to the device junction temperature. The TEMPOUT pin output voltage has a temperature slope of –4 mV/°C and a 1.34-V offset as described by Equation 2.

$$V_{TEMPOUT} = \left(\frac{-4\ mV}{°C} \times T \right) + 1.34\ V \tag{2}$$

where:

- T is the device junction temperature in °C.
- $V_{TEMPOUT}$ is the temperature monitor output voltage.

6.3.4.2 Thermal Shutdown

The DACx1416 incorporates a thermal shutdown that is triggered when the die temperature exceeds 140°C. A thermal shutdown sets the TEMP-ALM bit and causes all DAC outputs to power-down, however the internal reference remains powered on. The $\overline{\text{ALMOUT}}$ pin can be configured to monitor a thermal shutdown condition by setting the TEMPALM-EN bit. Once a thermal shutdown is triggered, the device stays in shutdown even after the device temperature lowers.

The die temperature must fall below 140°C before the device can be returned to normal operation. To resume normal operation, the thermal alarm must be cleared through the ALM-RESET bit while the DAC channels are in power-down mode.

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6.4 Device Functional Modes

6.4.1 Toggle Mode

Each DAC in the device is independently configurable to operate in toggle mode. A DAC channel in toggle mode incorporates two DAC registers (Register A and Register B) and is able to be set to switch repetitively between these two values. The DACx1416 toggle mode operation is configurable to introduce a dither signal to the DAC output, to generate a periodic signal, or to implement ON/OFF signaling, among some examples.

To update the toggle registers, use the following sequence:

1. Set DAC channel in synchronous mode and disable toggle mode for that channel
2. Write the desired Register A value to the DAC data register
3. Issue a DAC trigger signal to load Register A
4. Write the desired Register B value to the DAC data register
5. Enable toggle mode to load Register B

After both registers are loaded with data, use any of the three TOGGLE[2:0] pins to switch those DACs configured for toggle operation back and forth between the contents of the two respective DAC specific registers by using an external clock or logic signal. A TOGGLE pin logic low updates the DAC output to the value set by Register A. A logic high updates the DAC output to the value set by Register B. The three TOGGLE[2:0] pins give the DACx1416 the option to operate with up to three toggle rates.

Additionally, the device is configurable for software-controlled toggle operation by setting the SOFTTOGGLE-EN bit. In this mode, use any of the three AB-TOG[2:0] bits as a toggle control signal. Setting the AB-TOG bit to 1 enables Register B and clearing this bit to 0 enables Register A.

6.4.2 Differential Mode

Each DAC pair in the device are independently configurable to operate as a differential output pair. The differential output of a *DACx-y* pair is updated by writing to the *DACx* channel. For proper operation, configure the two DAC pairs to the same output range before enabling differential mode. Figure 6-2 and Figure 6-3 show the ideal differential output voltages (V_{DIFF}) and common mode voltages (V_{CM}) for a DAC differential pair configured for ±20-V and 0 to 40-V operation, respectively.

After being configured as a differential output, set the *DACx-y* pair for toggle operation by updating the *DACx* toggle registers; see Section 6.4.1.

Imbalances between the two differential signals result in common-mode and amplitude errors. The device incorporates an offset register that enables the user to introduce a voltage offset to the *DACy* channel of the *DACx-y* differential pair to compensate for a dc offset error between the two channels. The offset compensation gives approximately a ±0.2%FSR adjustment window. Rewrite the differential DAC data register after an update to the offset register.

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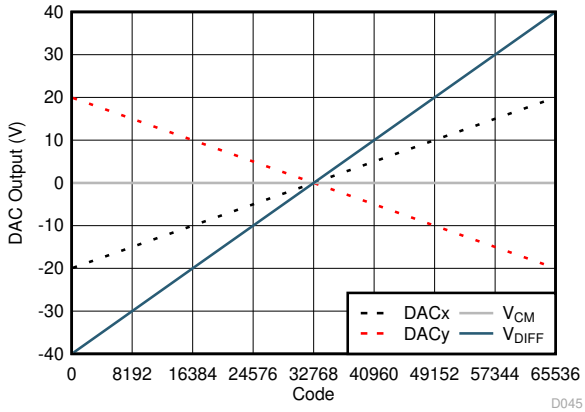

Figure 6-2. Differential Bipolar Output (16-Bit): ±20-V Output Range

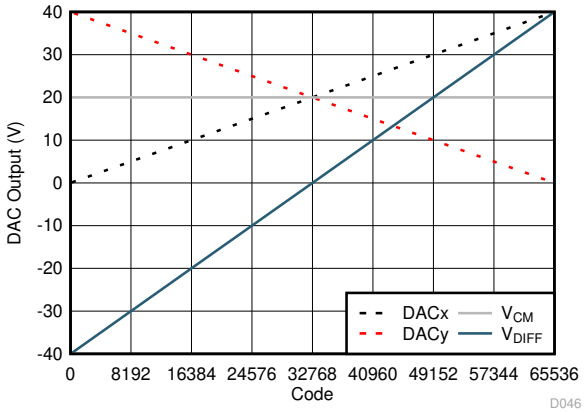

Figure 6-3. Differential Unipolar Output (16-Bit): 0-V to 40-V Output Range

6.4.3 Power-Down Mode

The DACx1416 DAC output amplifiers and internal reference power-down status are individually configured and monitored though the PWDWN registers. Setting a DAC channel in power-down mode disables the output amplifier and clamps the output pin to ground through an internal 10-kΩ resistor.

The DAC data registers are not cleared when the DAC goes into power-down, which allows the device to return to the same output voltage upon return to normal operation. The DAC data registers are able to update while in power-down mode.

After a power-on or reset event all the DAC channels and the internal reference are in power-down mode. Configure the entire device into power-down or active modes through the DEV-PWDWN bit.

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6.5 Programming

The DACx1416 family of devices is controlled through a flexible four-wire serial interface that is compatible with SPI type interfaces used on many microcontrollers and DSP controllers. The interface provides access to the DACx1416 registers and can be configured to daisy-chain multiple devices for write operations. The DACx1416 incorporates an optional error checking mode to validate SPI data communication integrity in noisy environments.

6.5.1 Stand-Alone Operation

A serial interface access cycle is initiated by asserting the $\overline{CS}$ pin low. The serial clock SCLK can be a continuous or gated clock. SDI data are clocked on SCLK falling edges. A regular serial interface access cycle is 24 bits long with error checking disabled and 32 bits long with error checking enabled, thus the $\overline{CS}$ pin must stay low for at least 24 or 32 SCLK falling edges. The access cycle ends when the $\overline{CS}$ pin is de-asserted high. If the access cycle contains less than then minimum clock edges, the communication is ignored. If the access cycle contains more than the minimum clock edges, only the first 24 or 32 bits are used by the device. When $\overline{CS}$ is high, the SCLK and SDI signals are blocked and the SDO is in a Hi-Z state.

In an error checking disabled access cycle (24-bits long) the first byte input to SDI is the instruction cycle which identifies the request as a read or write command and the 6-bit address to be accessed. The last 16 bits in the cycle form the data cycle.

Table 6-2. Serial Interface Access Cycle

BIT	FIELD	DESCRIPTION
23	RW	Identifies the communication as a read or write command to the address register. R/W = 0 sets a write operation. R/W = 1 sets a read operation.
22	x	Don't care bit.
21-16	A[5:0]	Register address. Specifies the register to be accessed during the read or write operation.
15-0	DI[15:0]	Data cycle bits. If a write command, the data cycle bits are the values to be written to the register with address A[5:0]. If a read command, the data cycle bits are don't care values.

Read operations require that the SDO pin is first enabled by setting the SDO-EN bit. A read operation is initiated by issuing a read command access cycle. After the read command, a second access cycle must be issued to get the requested data. Data are clocked out on SDO pin either on the falling edge or rising edge of SCLK according to the FSDO bit.

Table 6-3. SDO Output Access Cycle

BIT	FIELD	DESCRIPTION
23	RW	Echo RW from previous access cycle.
22	x	Echo bit 22 from previous access cycle.
21-16	A[5:0]	Echo address from previous access cycle.
15-0	DO[15:0]	Readback data requested on previous access cycle.

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6.5.1.1 Streaming Mode Operation

Since updating the sixteen channels data registers requires a large amount of data to be passed to the device, the device supports streaming mode. In streaming mode the DAC data registers can be written to the device without providing an instruction command for each data register. Streaming mode is enabled by setting the STR-EN bit. Once enabled the streaming operation is implemented by holding the $\overline{CS}$ active and continuing to shift new data into the device. The SDO pin is disabled when the STR-EN bit is enabled.

The instruction cycle includes the starting address. The device starts writing to this address and automatically increments the address as long as $\overline{CS}$ is asserted. If the last DAC data register address has been reached and $\overline{CS}$ is still asserted, the data for this address is overwritten with the new data.

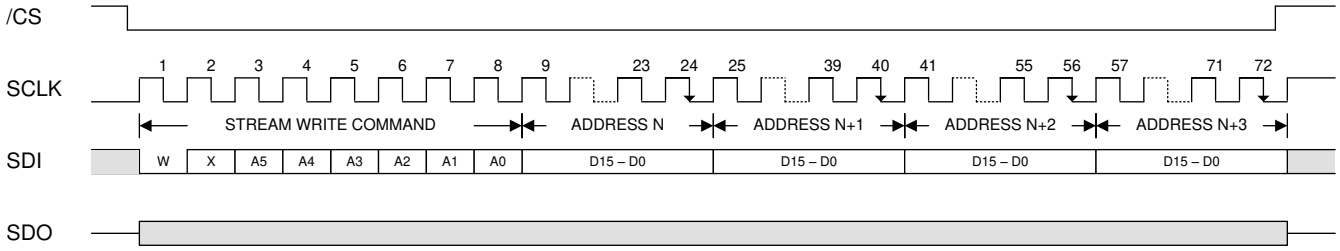

Figure 6-4. Serial Interface Streaming Cycle

6.5.2 Daisy-Chain Operation

For systems that contain more than one DACx1416 devices, the SDO pin can be used to daisy-chain them together. The SDO pin must be enabled by setting the SDO-EN bit before initiating the daisy-chain operation. Daisy-chain operation is useful in reducing the number of serial interface lines.

The first falling edge on the $\overline{CS}$ pin starts the operation cycle. If more than 24 SCLK pulses are applied while the $\overline{CS}$ pin is kept low, the data ripples out of the shift register and is clocked out on the SDO pin either on the falling edge or rising edge of SCLK according to the FSDO bit. By connecting the SDO output of the first device to the SDI input of the next device in the chain, a multiple-device interface is constructed. Each device in the system requires 24 clock pulses. As a result the total number of clock cycles must be equal to 24 × N, where N is the total number of DACx1416 devices in the daisy chain. When the serial transfer to all devices is complete the $\overline{CS}$ signal is taken high. This action transfers the data from the SPI shift registers to the internal registers of each device in the daisy chain and prevents any further data from being clocked into the input shift register. Daisy-chain operation is not supported while in streaming mode.

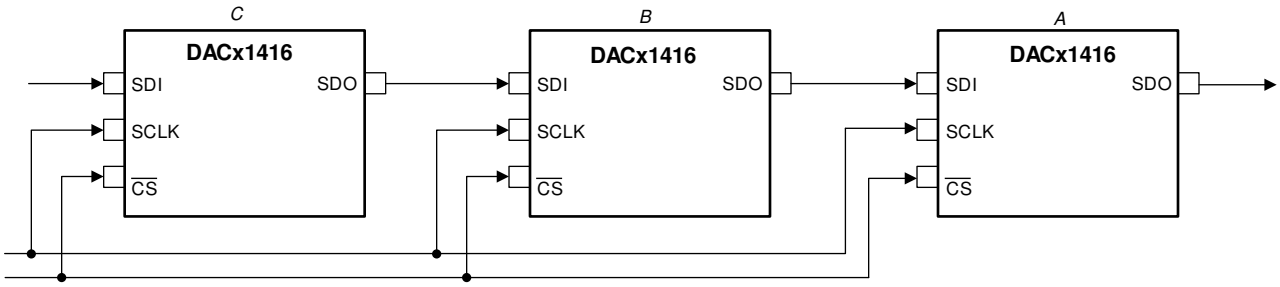

Figure 6-5. Daisy-Chain Layout

6.5.3 Frame Error Checking

If the DACx1416 are used in a noisy environment, use error checking to check the integrity of SPI data communication between the device and the host processor. To enable this feature, set the CRC-EN bit.

The error checking scheme is based on the CRC-8-ATM (HEC) polynomial $x^8 + x^2 + x + 1$ (that is, 100000111). When error checking is enabled, the serial interface access cycle width is 32 bits. The normal 24-bit SPI data are appended with an 8-bit CRC polynomial by the host processor before feeding the data to the device. In all serial interface readback operations, the CRC polynomial is output on the SDO pin as part of the 32-bit cycle.

Table 6-4. Error Checking Serial Interface Access Cycle

BIT	FIELD	DESCRIPTION
31	RW	Identifies the communication as a read or write command to the address register. R/W = 0 sets a write operation. R/W = 1 sets a read operation.
30	CRC-ERROR	Reserved bit. Set to zero.
29-24	A[5:0]	Register address. Specifies the register to be accessed during the read or write operation.
23-8	DI[15:0]	Data cycle bits. If a write command, the data cycle bits are the values to be written to the register with address A[5:0]. If a read command, the data cycle bits are don't care values.
7-0	CRC	8-bit CRC polynomial.

The DACx1416 decodes the 32-bit access cycle to compute the CRC remainder on $\overline{CS}$ rising edges. If no error exists, the CRC remainder is zero and data are accepted by the device.

A write operation failing the CRC check causes the data to be ignored by the device. After the write command, issue a second access cycle to determine the error checking results (CRC-ERROR bit) on the SDO pin.

If there is a CRC error, the CRC-ALM bit of the status register is set to 1. To monitor a CRC error, configure the $\overline{ALMOUT}$ pin by setting the CRCALM-EN bit.

Table 6-5. Write Operation Error Checking Cycle

BIT	FIELD	DESCRIPTION
31	RW	Echo RW from previous access cycle (RW = 0).
30	CRC-ERROR	Returns a 1 when a CRC error is detected, 0 otherwise.
29-24	A[5:0]	Echo address from previous access cycle.
23-8	DO[15:0]	Echo data from previous access cycle.
7-0	CRC	Calculated CRC value of bits 31:8.

A read operation must be followed by a second access cycle to get the requested data on the SDO pin. The error check result (CRC-ERROR bit) from the read command is output on the SDO pin.

As in the case of a write operation failing the CRC check, the CRC-ALM bit of the status register is set to 1 and the $\overline{ALMOUT}$ pin, if configured for CRC alerts, is set low.

Table 6-6. Read Operation Error Checking Cycle

BIT	FIELD	DESCRIPTION
31	RW	Echo RW from previous access cycle (RW = 1).
30	CRC-ERROR	Returns a 1 when a CRC error is detected, 0 otherwise.
29-24	A[5:0]	Echo address from previous access cycle.
23-8	DO[15:0]	Readback data requested on previous access cycle.
7-0	CRC	Calculated CRC value of bits 31:8.

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7 Register Maps

Table 7-1 lists the memory-mapped registers for the device. All register offset addresses not listed in Table 7-1 are considered reserved locations; do not modify these reserved register contents.

Table 7-1. DACx1416 Registers

Offset	Acronym	Register Name	Section
00h	NOP	NOP Register	Go
01h	DEVICEID	Device ID Register	Go
02h	STATUS	Status Register	Go
03h	SPICONFIG	SPI Configuration Register	Go
04h	GENCONFIG	General Configuration Register	Go
05h	BRDCONFIG	Broadcast Configuration Register	Go
06h	SYNCCONFIG	Sync Configuration Register	Go
07h	TOGGCONFIG0	DAC[15:8] Toggle Configuration Register	Go
08h	TOGGCONFIG1	DAC[7:0] Toggle Configuration Register	Go
09h	DACPWDWN	DAC Power-Down Register	Go
0Ah	DACRANGE0	DAC[15:12] Range Register	Go
0Bh	DACRANGE1	DAC[11:8] Range Register	Go
0Ch	DACRANGE2	DAC[7:4] Range Register	Go
0Dh	DACRANGE3	DAC[3:0] Range Register	Go
0Eh	TRIGGER	Trigger Register	Go
0Fh	BRDCAST	Broadcast Data Register	Go
10h	DAC0	DAC0 Data Register	Go
11h	DAC1	DAC1 Data Register	Go
12h	DAC2	DAC2 Data Register	Go
13h	DAC3	DAC3 Data Register	Go
14h	DAC4	DAC4 Data Register	Go
15h	DAC5	DAC5 Data Register	Go
16h	DAC6	DAC6 Data Register	Go
17h	DAC7	DAC7 Data Register	Go
18h	DAC8	DAC8 Data Register	Go
19h	DAC9	DAC9 Data Register	Go
1Ah	DAC10	DAC10 Data Register	Go
1Bh	DAC11	DAC11 Data Register	Go
1Ch	DAC12	DAC12 Data Register	Go
1Dh	DAC13	DAC13 Data Register	Go
1Eh	DAC14	DAC14 Data Register	Go
1Fh	DAC15	DAC15 Data Register	Go
20h	OFFSET0	DAC[14-15;12-13] Differential Offset Register	Go
21h	OFFSET1	DAC[10-11;8-9] Differential Offset Register	Go
22h	OFFSET2	DAC[6-7;4-5] Differential Offset Register	Go
23h	OFFSET3	DAC[2-3;0-1] Differential Offset Register	Go

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Complex bit access types are encoded to fit into small table cells. Table 7-2 shows the codes that are used for access types in this section.

Table 7-2. Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, the variables refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address, the variable refers to the value of a register array.

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7.1 NOP Register (Offset = 00h) [reset = 0000h]

NOP is shown in Figure 7-1 and described in Table 7-3.

Return to Summary Table.

Figure 7-1. NOP Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOP															
W-0h															

Table 7-3. NOP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	NOP	W	0h	No operation. Write 0000h for proper no-operation command.

7.2 DEVICEID Register (Offset = 01h) [reset = ----h]

DEVICEID is shown in Figure 7-2 and described in Table 7-4.

Return to Summary Table.

Figure 7-2. DEVICEID Register

15	14	13	12	11	10	9	8
DEVICEID							
R----h							
7	6	5	4	3	2	1	0
DEVICEID						VERSIONID	
R----h						R-0h	

Table 7-4. DEVICEID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	DEVICEID	R	---h	Device ID DAC81416: 29Ch DAC71416: 28Ch DAC61416: 24Ch
1-0	VERSIONID	R	0h	Version ID. Subject to change.

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7.3 STATUS Register (Offset = 02h) [reset = 0000h]

STATUS is shown in Figure 7-3 and described in Table 7-5.

Return to Summary Table.

Figure 7-3. STATUS Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					CRC-ALM	DAC-BUSY	TEMP-ALM
R-0h					R-0h	R-0h	R-0h

Table 7-5. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R	0h	This bit is reserved.
2	CRC-ALM	R	0h	CRC-ALM = 1 indicates a CRC error.
1	DAC-BUSY	R	0h	DAC-BUSY = 1 indicates DAC registers are not ready for updates.
0	TEMP-ALM	R	0h	TEMP-ALM = 1 indicates die temperature is over 140°C. A thermal alarm event forces the DAC outputs to go into power-down mode.

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7.4 SPICONFIG Register (Offset = 03h) [reset = 0AA4h]

SPICONFIG is shown in Figure 7-4 and described in Table 7-6.

Return to Summary Table.

Figure 7-4. SPICONFIG Register

15	14	13	12	11	10	9	8
RESERVED				TEMPALM-EN	DACBUSY-EN	CRCALM-EN	RESERVED
R-0h				R/W-1h	R/W-0h	R/W-1h	R-0h
7	6	5	4	3	2	1	0
RESERVED	SOFTTOGGLE-EN	DEV-PWDWN	CRC-EN	STR-EN	SDO-EN	FSDO	RESERVED
R-1h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R-0h

Table 7-6. SPICONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	This bit is reserved.
11	TEMPALM-EN	R/W	1h	When set to 1, a thermal alarm triggers the $\overline{\text{ALMOUT}}$ pin.
10	DACBUSY-EN	R/W	0h	When set to 1 the $\overline{\text{ALMOUT}}$ pin is set between DAC output updates. Contrary to other alarm events, this alarm resets automatically.
9	CRCALM-EN	R/W	1h	When set to 1, a CRC error triggers the $\overline{\text{ALMOUT}}$ pin.
8	RESERVED	R	0h	This bit is reserved.
7	RESERVED	R	1h	This bit is reserved.
6	SOFTTOGGLE-EN	R/W	0h	When set to 1 enables soft toggle operation.
5	DEV-PWDWN	R/W	1h	DEV-PWDWN = 1 sets the device in power-down mode DEV-PWDWN = 0 sets the device in active mode
4	CRC-EN	R/W	0h	When set to 1 frame error checking is enabled.
3	STR-EN	R/W	0h	When set to 1 streaming mode operation is enabled.
2	SDO-EN	R/W	1h	When set to 1 the SDO pin is operational.
1	FSDO	R/W	0h	Fast SDO bit (half-cycle speedup). When 0, SDO updates during SCLK rising edges. When 1, SDO updates during SCLK falling edges.
0	RESERVED	R	0h	This bit is reserved.

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7.5 GENCONFIG Register (Offset = 04h) [reset = 7F00h]

GENCONFIG is shown in Figure 7-5 and described in Table 7-7.

Return to Summary Table.

Figure 7-5. GENCONFIG Register

15	14	13	12	11	10	9	8
RESERVED	REF-PWDWN	RESERVED					
R-0h	R/W-1h	R-1h					
7	6	5	4	3	2	1	0
DAC-14-15-DIFF-EN	DAC-12-13-DIFF-EN	DAC-10-11-DIFF-EN	DAC-8-9-DIFF-EN	DAC-6-7-DIFF-EN	DAC-4-5-DIFF-EN	DAC-2-3-DIFF-EN	DAC-0-1-DIFF-EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-7. GENCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	This bit is reserved.
14	REF-PWDWN	R/W	1h	REF-PWDWN = 1 powers down the internal reference REF-PWDWN = 0 activates the internal reference
13-8	RESERVED	R	1h	This bit is reserved.
7	DAC-14-15-DIFF-EN	R/W	0h	When set to 1, the corresponding DAC pair is set to operate in differential mode. Rewrite the DAC data registers after enabling or disabling differential operation.
6	DAC-12-13-DIFF-EN	R/W	0h	
5	DAC-10-11-DIFF-EN	R/W	0h	
4	DAC-8-9-DIFF-EN	R/W	0h	
3	DAC-6-7-DIFF-EN	R/W	0h	
2	DAC-4-5-DIFF-EN	R/W	0h	
1	DAC-2-3-DIFF-EN	R/W	0h	
0	DAC-0-1-DIFF-EN	R/W	0h	

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7.6 BRDCONFIG Register (Offset = 05h) [reset = FFFFh]

BRDCONFIG is shown in Figure 7-6 and described in Table 7-8.

Return to Summary Table.

Figure 7-6. BRDCONFIG Register

15	14	13	12	11	10	9	8
DAC15-BRDCAST-EN	DAC14-BRDCAST-EN	DAC13-BRDCAST-EN	DAC12-BRDCAST-EN	DAC11-BRDCAST-EN	DAC10-BRDCAST-EN	DAC9-BRDCAST-EN	DAC8-BRDCAST-EN
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
7	6	5	4	3	2	1	0
DAC7-BRDCAST-EN	DAC6-BRDCAST-EN	DAC5-BRDCAST-EN	DAC4-BRDCAST-EN	DAC3-BRDCAST-EN	DAC2-BRDCAST-EN	DAC1-BRDCAST-EN	DAC0-BRDCAST-EN
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

Table 7-8. BRDCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	DAC15-BRDCAST-EN	R/W	1h	When set to 1, the corresponding DAC is set to update the respective output to the value set in the BRDCAST register. Configure all DAC channels in single-ended mode for broadcast operation. If one or more outputs are configured in differential mode, broadcast mode is ignored. When cleared to 0, the corresponding DAC output remains unaffected by a BRDCAST command.
14	DAC14-BRDCAST-EN	R/W	1h	
13	DAC13-BRDCAST-EN	R/W	1h	
12	DAC12-BRDCAST-EN	R/W	1h	
11	DAC11-BRDCAST-EN	R/W	1h	
10	DAC10-BRDCAST-EN	R/W	1h	
9	DAC9-BRDCAST-EN	R/W	1h	
8	DAC8-BRDCAST-EN	R/W	1h	
7	DAC7-BRDCAST-EN	R/W	1h	
6	DAC6-BRDCAST-EN	R/W	1h	
5	DAC5-BRDCAST-EN	R/W	1h	
4	DAC4-BRDCAST-EN	R/W	1h	
3	DAC3-BRDCAST-EN	R/W	1h	
2	DAC2-BRDCAST-EN	R/W	1h	
1	DAC1-BRDCAST-EN	R/W	1h	
0	DAC0-BRDCAST-EN	R/W	1h	

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7.7 SYNCCONFIG Register (Offset = 06h) [reset = 0000h]

SYNCCONFIG is shown in Figure 7-7 and described in Table 7-9.

Return to Summary Table.

Figure 7-7. SYNCCONFIG Register

15	14	13	12	11	10	9	8
DAC15-SYNC-EN	DAC14-SYNC-EN	DAC13-SYNC-EN	DAC12-SYNC-EN	DAC11-SYNC-EN	DAC10-SYNC-EN	DAC9-SYNC-EN	DAC8-SYNC-EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
DAC7-SYNC-EN	DAC6-SYNC-EN	DAC5-SYNC-EN	DAC4-SYNC-EN	DAC3-SYNC-EN	DAC2-SYNC-EN	DAC1-SYNC-EN	DAC0-SYNC-EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-9. SYNCCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	DAC15-SYNC-EN	R/W	0h	When set to 1, the corresponding DAC output is set to update in response to an LDAC trigger (synchronous mode). When cleared to 0, the corresponding DAC output is set to update immediately (asynchronous mode).
14	DAC14-SYNC-EN	R/W	0h	
13	DAC13-SYNC-EN	R/W	0h	
12	DAC12-SYNC-EN	R/W	0h	
11	DAC11-SYNC-EN	R/W	0h	
10	DAC10-SYNC-EN	R/W	0h	
9	DAC9-SYNC-EN	R/W	0h	
8	DAC8-SYNC-EN	R/W	0h	
7	DAC7-SYNC-EN	R/W	0h	
6	DAC6-SYNC-EN	R/W	0h	
5	DAC5-SYNC-EN	R/W	0h	
4	DAC4-SYNC-EN	R/W	0h	
3	DAC3-SYNC-EN	R/W	0h	
2	DAC2-SYNC-EN	R/W	0h	
1	DAC1-SYNC-EN	R/W	0h	
0	DAC0-SYNC-EN	R/W	0h	

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7.8 TOGGCONFIG0 Register (Offset = 07h) [reset = 0000h]

TOGGCONFIG0 is shown in Figure 7-8 and described in Table 7-10.

Return to Summary Table.

Figure 7-8. TOGGCONFIG0 Register

15	14	13	12	11	10	9	8
DAC15-AB-TOGG-EN		DAC14-AB-TOGG-EN		DAC13-AB-TOGG-EN		DAC12-AB-TOGG-EN	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
DAC11-AB-TOGG-EN		DAC10-AB-TOGG-EN		DAC9-AB-TOGG-EN		DAC8-AB-TOGG-EN	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 7-10. TOGGCONFIG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DAC15-AB-TOGG-EN	R/W	0h	Enables toggle mode operation and configures the toggle pin or soft toggle bit: 00 = Toggle mode disabled 01 = Toggle mode enabled: TOGGLE0 10 = Toggle mode enabled: TOGGLE1 11 = Toggle mode enabled: TOGGLE2
13-12	DAC14-AB-TOGG-EN	R/W	0h	
11-10	DAC13-AB-TOGG-EN	R/W	0h	
9-8	DAC12-AB-TOGG-EN	R/W	0h	
7-6	DAC11-AB-TOGG-EN	R/W	0h	
5-4	DAC10-AB-TOGG-EN	R/W	0h	
3-2	DAC9-AB-TOGG-EN	R/W	0h	
1-0	DAC8-AB-TOGG-EN	R/W	0h	

7.9 TOGGCONFIG1 Register (Offset = 08h) [reset = 0000h]

TOGGCONFIG1 is shown in Figure 7-9 and described in Table 7-11.

Return to Summary Table.

Figure 7-9. TOGGCONFIG1 Register

15	14	13	12	11	10	9	8
DAC7-AB-TOGG-EN		DAC6-AB-TOGG-EN		DAC5-AB-TOGG-EN		DAC4-AB-TOGG-EN	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
DAC3-AB-TOGG-EN		DAC2-AB-TOGG-EN		DAC1-AB-TOGG-EN		DAC0-AB-TOGG-EN	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 7-11. TOGGCONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DAC7-AB-TOGG-EN	R/W	0h	Enables toggle mode operation and configures the toggle pin or soft toggle bit: 00 = Toggle mode disabled 01 = Toggle mode enabled: TOGGLE0 10 = Toggle mode enabled: TOGGLE1 11 = Toggle mode enabled: TOGGLE2
13-12	DAC6-AB-TOGG-EN	R/W	0h	
11-10	DAC5-AB-TOGG-EN	R/W	0h	
9-8	DAC4-AB-TOGG-EN	R/W	0h	
7-6	DAC3-AB-TOGG-EN	R/W	0h	
5-4	DAC2-AB-TOGG-EN	R/W	0h	
3-2	DAC1-AB-TOGG-EN	R/W	0h	
1-0	DAC0-AB-TOGG-EN	R/W	0h	

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7.10 DACPWDWN Register (Offset = 09h) [reset = FFFFh]

DACPWDWN is shown in Figure 7-10 and described in Table 7-12.

Return to Summary Table.

Figure 7-10. DACPWDWN Register

15	14	13	12	11	10	9	8
DAC15-PWDWN	DAC14-PWDWN	DAC13-PWDWN	DAC12-PWDWN	DAC11-PWDWN	DAC10-PWDWN	DAC9-PWDWN	DAC8-PWDWN
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
7	6	5	4	3	2	1	0
DAC7-PWDWN	DAC6-PWDWN	DAC5-PWDWN	DAC4-PWDWN	DAC3-PWDWN	DAC2-PWDWN	DAC1-PWDWN	DAC0-PWDWN
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

Table 7-12. DACPWDWN Register Field Descriptions

Bit	Field	Type	Reset	Description
15	DAC15-PWDWN	R/W	1h	When set to 1, the corresponding DAC is in power-down mode and the respective output is connected to GND through a 10-kΩ internal resistor.
14	DAC14-PWDWN	R/W	1h	
13	DAC13-PWDWN	R/W	1h	
12	DAC12-PWDWN	R/W	1h	
11	DAC11-PWDWN	R/W	1h	
10	DAC10-PWDWN	R/W	1h	
9	DAC9-PWDWN	R/W	1h	
8	DAC8-PWDWN	R/W	1h	
7	DAC7-PWDWN	R/W	1h	
6	DAC6-PWDWN	R/W	1h	
5	DAC5-PWDWN	R/W	1h	
4	DAC4-PWDWN	R/W	1h	
3	DAC3-PWDWN	R/W	1h	
2	DAC2-PWDWN	R/W	1h	
1	DAC1-PWDWN	R/W	1h	
0	DAC0-PWDWN	R/W	1h	

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7.11 DACRANGEn Register (Offset = 0Ah–0Dh) [reset = 0000h]

DACRANGEn is shown in Figure 7-11 and described in Table 7-13.

Return to Summary Table.

Figure 7-11. DACRANGEn Register

15	14	13	12	11	10	9	8
DACa-RANGE[3:0]				DACb-RANGE[3:0]			
W-0h				W-0h			
7	6	5	4	3	2	1	0
DACc-RANGE[3:0]				DACd-RANGE[3:0]			
W-0h				W-0h			

Table 7-13. DACRANGEn Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	DACa-RANGE[3:0]	W	0h	Sets the output range for the corresponding DAC. 0000 = 0 V to 5 V 0001 = 0 V to 10 V 0010 = 0 V to 20 V 0100 = 0 V to 40 V 1001 = –5 V to +5 V 1010 = –10 V to +10 V 1100 = –20 V to +20 V 1110 = –2.5 V to +2.5 V All others: invalid Configure the two outputs of a differential DAC pair to the same output range before setting the outputs as a differential pair. a: 15, 11, 7 or 3; b: 14, 10, 6 or 2; c: 13, 9, 5 or 1; d: 12, 8, 4 or 0
11-8	DACb-RANGE[3:0]	W	0h	
7-4	DACc-RANGE[3:0]	W	0h	
3-0	DACd-RANGE[3:0]	W	0h	

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7.12 TRIGGER Register (Offset = 0Eh) [reset = 0000h]

TRIGGER is shown in Figure 7-12 and described in Table 7-14.

Return to Summary Table.

Figure 7-12. TRIGGER Register

15	14	13	12	11	10	9	8
RESERVED							ALM-RESET
W-0h							W-0h
7	6	5	4	3	2	1	0
AB-TOG2	AB-TOG1	AB-TOG0	LDAC	SOFT-RESET[3:0]			
W-0h	W-0h	W-0h	W-0h	W-0h			

Table 7-14. TRIGGER Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	W	0h	This bit is reserved
8	ALM-RESET	W	0h	Set this bit to 1 to clear an alarm event; not applicable for a DAC-BUSY alarm event.
7	AB-TOG2	W	0h	If soft toggle is enabled set, this bit controls the toggle between values for those DACs that have been set in toggle mode 2 in the TOGGCONFIG register. Set to 1 to update to Register B and clear to 0 for Register A.
6	AB-TOG1	W	0h	If soft toggle is enabled set, this bit controls the toggle between values for those DACs that have been set in toggle mode 1 in the TOGGCONFIG register. Set to 1 to updated to Register B and clear to 0 for Register A.
5	AB-TOG0	W	0h	If soft toggle is enabled set, this bit controls the toggle between values for those DACs that have been set in toggle mode 0 in the TOGGCONFIG register. Set to 1 to update to Register B and clear to 0 for Register A.
4	LDAC	W	0h	Set this bit to 1 to synchronously load those DACs who have been set in synchronous mode in the SYNCCONFIG register.
3-0	SOFT-RESET[3:0]	W	0h	When set to reserved code 1010, these bits reset the device to the default state.

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7.13 BRDCAST Register (Offset = 0Fh) [reset = 0000h]

BRDCAST is shown in Figure 7-13 and described in Table 7-15.

Return to Summary Table.

Figure 7-13. BRDCAST Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BRDCAST-DATA[15:0]															
W-0h															

Table 7-15. BRDCAST Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	BRDCAST-DATA[15:0]	W	0h	Writing to the BRDCAST register forces the DAC channels that are set to broadcast in the BRDCONFIG register to update the respective register data to the new data in the BRDCAST register. Data are MSB aligned in straight-binary format as follows: DAC81416: { DATA[15:0] } DAC71416: { DATA[13:0], x, x } DAC61416: { DATA[11:0], x, x, x, x} x – Don't care bits

7.14 DACn Register (Offset = 10h–1Fh) [reset = 0000h]

DACn is shown in Figure 7-14 and described in Table 7-16.

Return to Summary Table.

Figure 7-14. DACn Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DACn-DATA[15:0]															
W-0h															

Table 7-16. DACn Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DACn-DATA[15:0]	W	0h	Stores the 16-, 14-, or 12-bit data to be loaded to DACn in MSB-aligned, straight-binary format. In differential DAC mode, data are loaded into the lowest-valued DAC in the DAC pair (in pair DAC*xy*, data are loaded into DAC*x* and writes to DAC*y* are ignored). Data use the following format: DAC81416: { DATA[15:0] } DAC71416: { DATA[13:0], x, x } DAC61416: { DATA[11:0], x, x, x, x} x – Don't care bits

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7.15 OFFSETn Register (Offset = 20h–23h) [reset = 0000h]

OFFSETn is shown in Figure 7-15 and described in Table 7-17.

Return to Summary Table.

Figure 7-15. OFFSETn Register

15	14	13	12	11	10	9	8
OFFSETab[7:0]							
R/W-0h							
7	6	5	4	3	2	1	0
OFFSETcd[7:0]							
R/W-0h							

Table 7-17. OFFSETn Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	OFFSETab[7:0]	R/W	0h	Provides offset adjustment to DAC*y* in the differential DAC*x-y* pair in 2's complement format. Data use the following format: • DAC81416: – Format: { OFFSET[7:0] } – Range: –128 LSB to +127 LSB • DAC71416: – Format: { OFFSET[5:0], x, x } – Range: –32 LSB to +31 LSB • DAC61416: – Format: { OFFSET[3:0], x, x, x, x} – Range: –8 LSB to +7 LSB x – Don't care bits Rewrite the differential DAC data register after updating the offset register. ab: 14-15, 10-11, 6-7 or 2-3; cd: 12-13, 8-9, 4-5 or 0-1
7-0	OFFSETcd[7:0]	R/W	0h	

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

One of the primary applications of the DACx1416 family is Mach Zehnder Modulator (MZM) biasing, employed in Optical Line Cards and Optical Modules. With high-voltage, high-current and differential output features, the DACx1416 family can be used for biasing both $LiNbO_3$ and InP type modulators. With the help of the toggle mode and multiple corresponding input pins, the required dither waveform for such applications can be generated without involving SPI programming. The small package size and integrated reference minimize the total footprint of such applications.

8.2 Typical Application

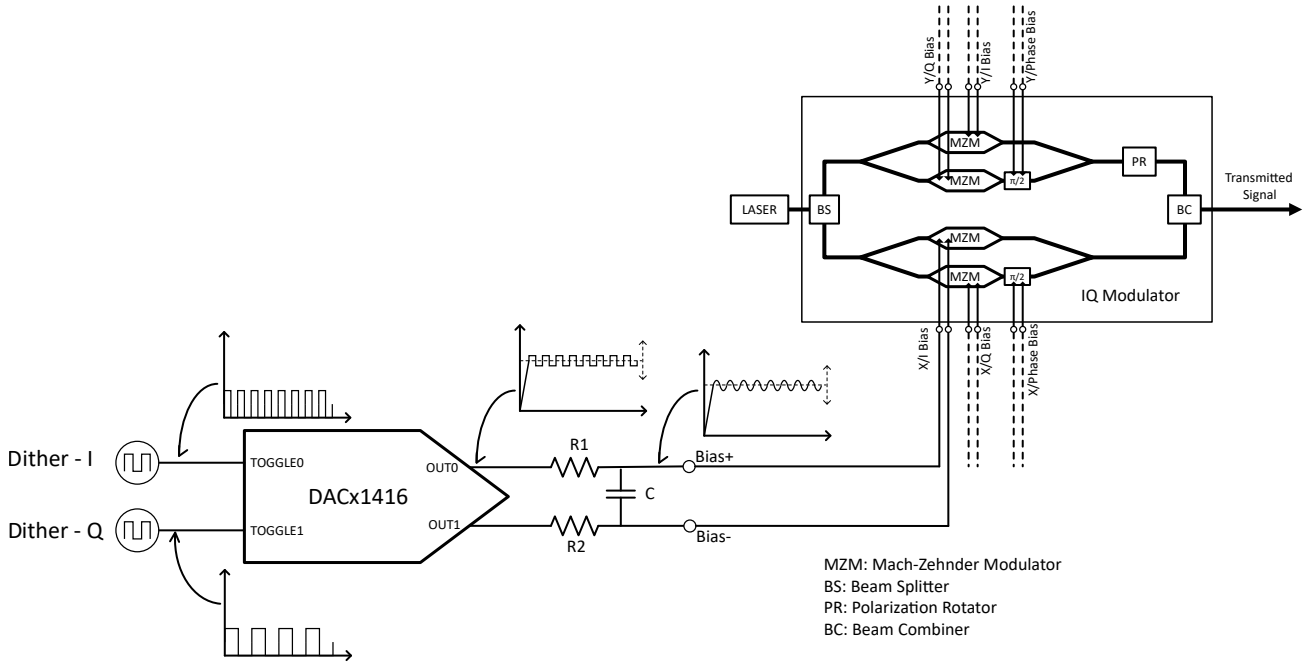

Figure 8-1. Biasing a Mach Zehnder Modulator

8.2.1 Design Requirements

Designing biasing circuits that are made to match both types of MZM technologies ($LiNbO_3$ and InP) requires high voltage and current ranges; see Table 8-1. The Optical Internetworking Forum (OIF) recommends four differential IQ bias and two differential phase bias inputs; see Figure 8-1. This differential signaling scheme helps minimize crosstalk and noise between channels, which otherwise potentially results in a complicated bias control algorithm. While an ideal dither tone is a sine wave, generating a sine wave is cumbersome in a largely digital circuit domain. A square wave is relatively easier to generate through digital circuits, and is also usable, provided that the bandwidth of this dither signal is less than the low cutoff frequency of the receiver (that is, 100 kHz or 1 MHz as per OIF). Passive RC filters with a cutoff frequency less than 100 kHz are usable at the DAC output for $LiNbO_3$ modulators, which have a very small bias current requirement. For InP modulators that are mainly used with optical modules, typically requiring a receiver low cutoff frequency of MHz, choose RC values so that the power dissipation across the resistors is small.

For smooth detection of the dither signal at the MZM output, use two orthogonal dither frequency sources for the *I* and *Q* arms. The amplitude of the dither waveform is typically 0.5% to 2.5% of the dc bias voltage, which is mainly governed by the design implementation.

Table 8-1. Requirements of MZM Biasing Circuit

PARAMETER	VALUE
DC range	Up to ±18 V
Dither amplitude	40 mV to 500 mV
Dither frequency	100 Hz to 100 kHz
Dither shape	Sine or square
Bias current	Up to 25 mA (for InP MZM)
Number of dither frequencies	2
Output type	Differential (6 pairs)

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8.2.2 Detailed Design Procedure

Figure 8-1 provides the simplified circuit diagram for biasing a MZM for a *Dither-type Bias Control* circuit. As shown, this circuit requires four differential input pairs for IQ biasing, and two differential input pairs for phase biasing. To bias a $LiNbO_3$ MZM, the voltage can be as high as ±18 V, whereas the current requirement is of the order of few micro amperes. The low cutoff frequency of the receiver is typically 100 kHz, and hence, the bandwidth of the dither signals is well below this frequency. Be aware that only the IQ bias inputs require the dither signal, and not the phase bias. The DACx1416 features a toggle mode wherein the outputs can be configured to provide a square wave imposed on a dc bias. This mode requires setting the HIGH and LOW codes for the square wave and the transition happens in sync with the selected toggle input pin. The pseudocode to achieve the dither output using the toggle function is provided below.

```
//SYNTAX: WRITE <REGISTER NAME>,<DATA>
//Power-on Device, Disable Soft-toggle
WRITE SPICONFIG,0x0A84
//Select Range for all 12 channels as ±10V
WRITE DACRANGE2, 0xAAAA
WRITE DACRANGE3, 0xAAAA
WRITE DACRANGE4, 0xAAAA
//Power-on DAC Channels 0 - 11
WRITE DACPWDWN,0xF000
//Write HIGH code to Register A of all IQ Bias Differential Pairs
WRITE DAC0,0xXXXX
WRITE DAC2,0xXXXX
WRITE DAC4,0xXXXX
WRITE DAC6,0xXXXX
//Write Data to Phase Bias Channels
WRITE DAC8,0xXXXX
WRITE DAC10,0xXXXX
//Enable Sync for All Differential Pairs
WRITE SYNCCONFIG,0x0FFF
//Enable Software LDAC
WRITE TRIGGER,0x0002
//Write LOW code to Register B of all IQ Bias Differential Pairs
WRITE DAC_DATA0,0xXXXX
WRITE DAC_DATA0,0xXXXX
WRITE DAC_DATA0,0xXXXX
WRITE DAC_DATA0,0xXXXX
//Turn Toggle Mode ON for All IQ Differential Pairs
//DAC11-10:Y/Phase Bias , DAC9-8:Y/I Bias - TOGG0, DAC7-6:Y/Q Bias - TOGG 1
//DAC5-4:Y/Phase Bias , DAC3-2:Y/I Bias - TOGG0, DAC1-0:Y/Q Bias - TOGG 1
WRITE TOGGCONFIG0,0x0005
WRITE TOGGCONFIG1,0xA05A
//Method to Modify the DC Value of Any IQ Differential Pair
//Turn Off Toggle Mode for that Channel (e.g. DAC0-1)
WRITE TOGGCONFIG1,0xA050
//Turn Off Sync for the Channel
WRITE SYNCCONFIG,0x0FFC
//Write HIGH code to Register A of the Channel Pair
WRITE DAC0,0xXXXX
//Turn On Sync for the Channel Pair
WRITE SYNCCONFIG,0x0FFF
//Turn On Toggle for the Channel Pair
WRITE TOGGCONFIG1,0xA05A
```

The dither frequencies are able to be set at 1 kHz and 2 kHz so that a single-pole RC low-pass filter provides sufficient attenuation at 100 kHz. For example, when R1 = R2 = 10 kΩ and C = 0.01 µF, an attenuation of approximately 40 dB is obtained at 100 kHz.

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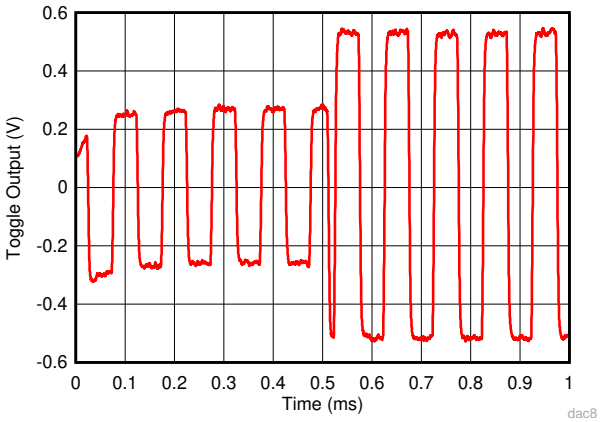
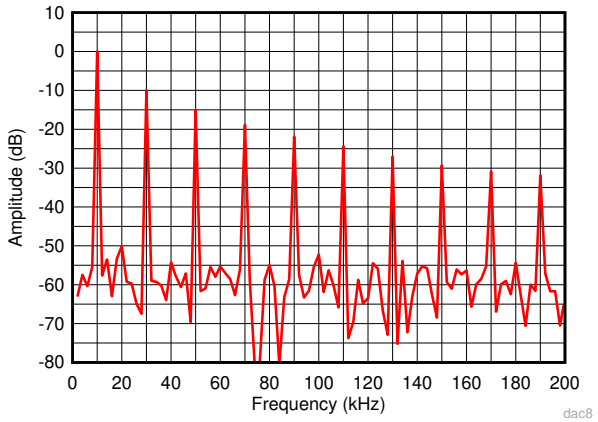
8.2.3 Application Curves



Toggle frequency = 10 kHz

Figure 8-2. Toggle AC Amplitude Transition



Toggle frequency = 10 kHz, no filter at output

Figure 8-3. Frequency Spectrum of Toggle Output

8.3 Power Supply Recommendations

The DACx1416 require five power supply inputs: VIO, VDD, VAA, VCC and VSS. Ensure that VDD and VAA are at the same level. Assuming VIO and VDD/VAA are different, there are four separate power-supply sources required.

Place a 0.1-µF ceramic capacitor close to each power-supply pin. Be aware that VCC and VSS have two pins each. In addition, a 4.7-µF or 10-µF bulk capacitor is recommended for each power supply; tantalum or aluminum types are good options for the bulk capacitors.

There is no sequencing requirement for the power supplies. As the DAC output range is configurable, ensure that the power-supplies have enough headroom to achieve linearity at codes close to the power-supply rails. When sourcing or sinking current from or to the DAC output, consider the heat dissipation. For example, a typical application of MZM bias with 25-mA load current from or to 12 channels with a 2.5-V power-supply headroom creates a power dissipation across the DAC of (12 × 2.5 × 25 mA) = 0.75 W. The thermal design to dissipate the power in this example potentially involves inclusion of heat sinks to avoid thermal shutdown of the device.

8.4 Layout

8.4.1 Layout Guidelines

The pin configuration of the DACx1416 is designed so that the analog, digital, and power pins are spatially separated from each other, which makes the PCB layout simple. Figure 8-4 shows an example layout. As evident, every power supply pin has a 0.1-µF capacitor close to the pin. Lay out the analog and digital signals away from each other, or on different PCB layers. Provide an unbroken reference plane (either ground or VIO) for the digital signals. Ensure that the higher frequency signals, such as SCLK and SDI, have appropriate impedance termination to address signal integrity.

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8.4.2 Layout Example

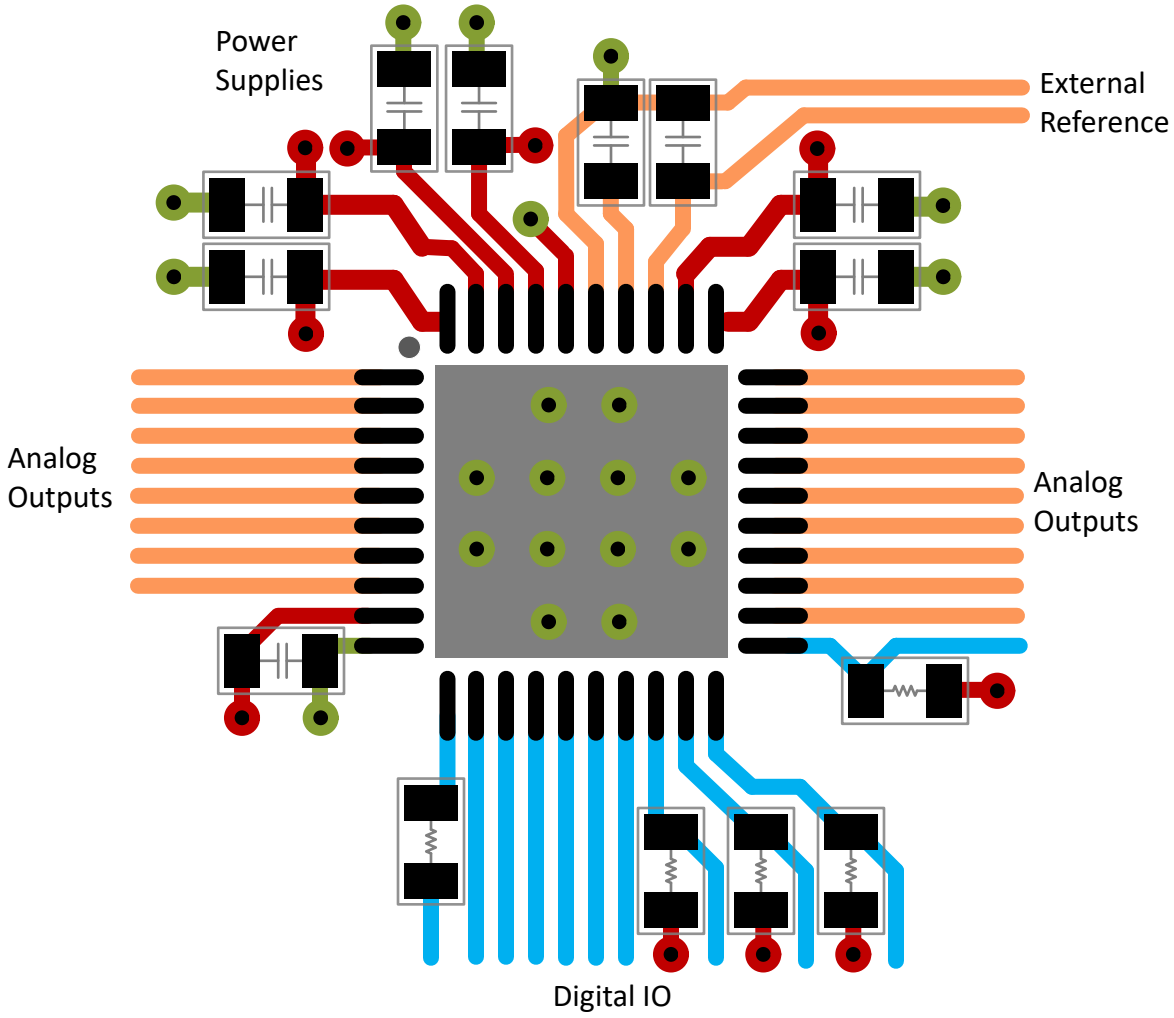

Figure 8-4. Example Layout

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

For development support, see the following: DAC81416 Evaluation Module

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, DAC81416EVM User's Guide
- Texas Instruments, *DACx1416 Delivers Optimized Solution to Mach Zehnder Modulator Biasing* application note
- Texas Instruments, *Programmable Voltage Output With Sense Connections Circuit* application note

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.5 Trademarks

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9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (June 2021) to Revision C (August 2025)	Page
• Added Figure 5-3, *DAC Wait Time in Update Mode*	11
• Updated minimum wait time for DAC output update in *DAC Register Synchronous and Asynchronous Updates*	22
• Added clarification about SDO state during streaming mode to *Streaming Mode Operation*	27
• Changed BRDCAST-DATA and DACn-DATA from R/W to W	29

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Changes from Revision A (November 2018) to Revision B (June 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated formatting and minor editorial issues for clarity	1

Changes from Revision * (July 2018) to Revision A (November 2018)	Page
• Changed DAC81416 from Advance Information to Production Data	1
• Changed DAC71416 and DAC61416 from Product Preview to Production Data	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC61416RHAR	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	DAC61416
DAC61416RHAR.A	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	DAC61416
DAC61416RHAT	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	DAC61416
DAC61416RHAT.A	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	DAC61416
DAC71416RHAR	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	DAC71416
DAC71416RHAR.A	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	DAC71416
DAC71416RHAT	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	DAC71416
DAC71416RHAT.A	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	DAC71416
DAC81416RHAR	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	DAC81416
DAC81416RHAR.A	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	DAC81416
DAC81416RHAT	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	DAC81416
DAC81416RHAT.A	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	DAC81416

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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GENERIC PACKAGE VIEW

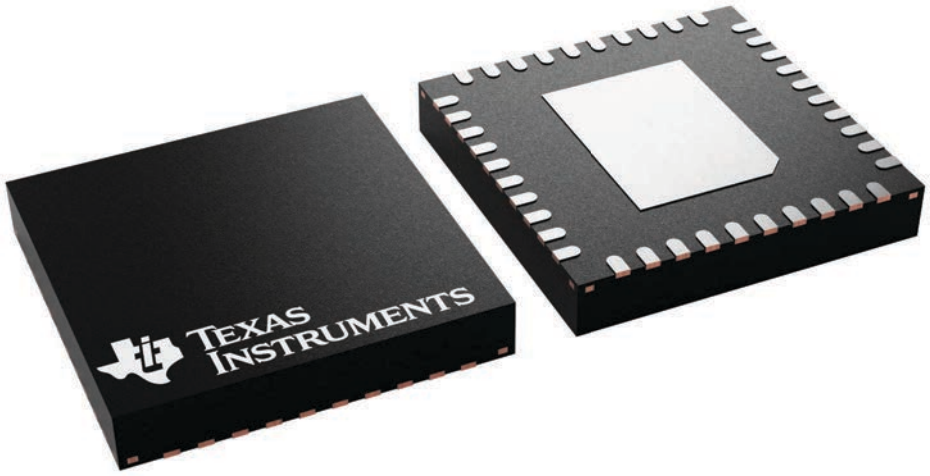
RHA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



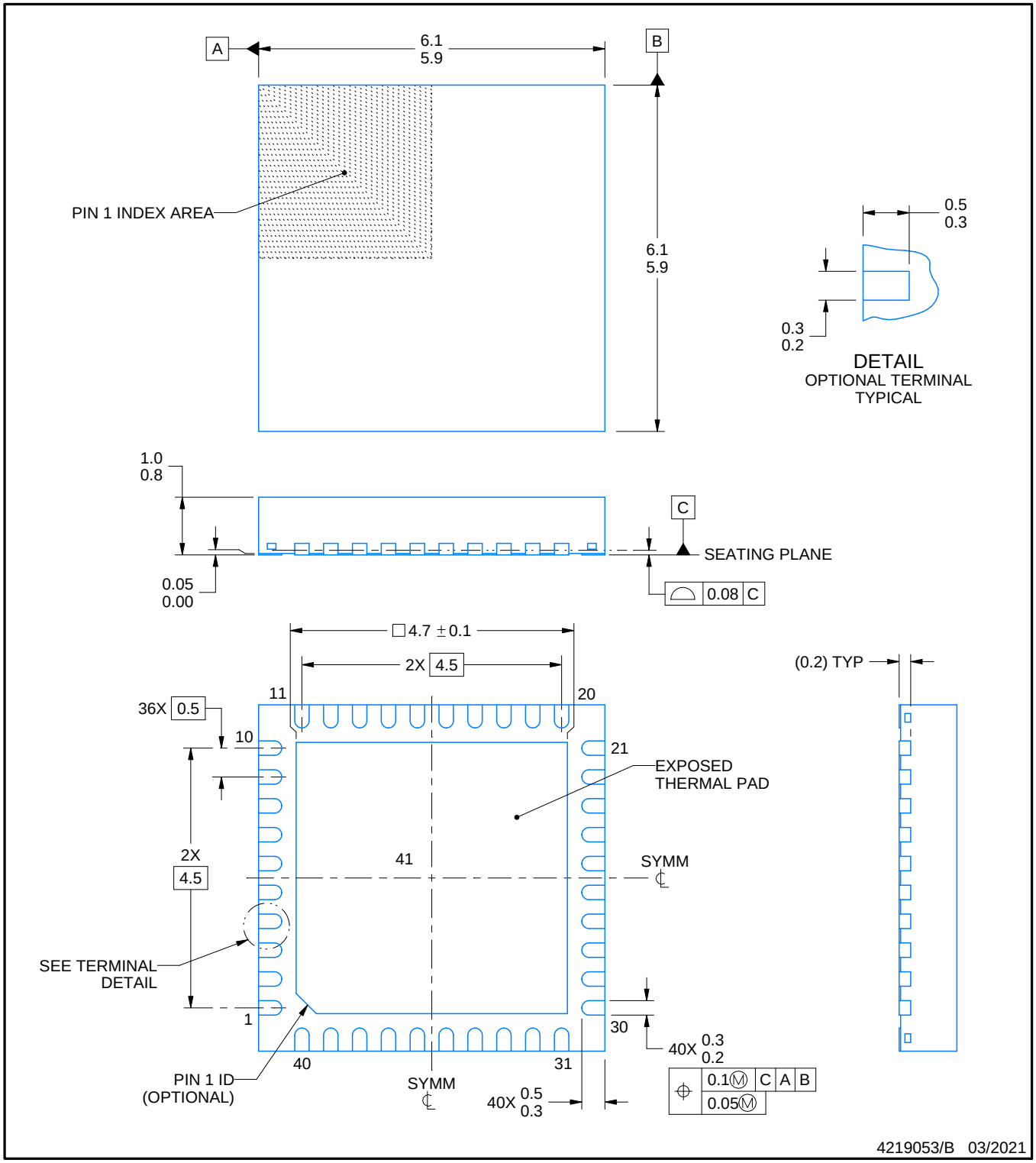
4225870/A

RHA0040C

PACKAGE OUTLINE

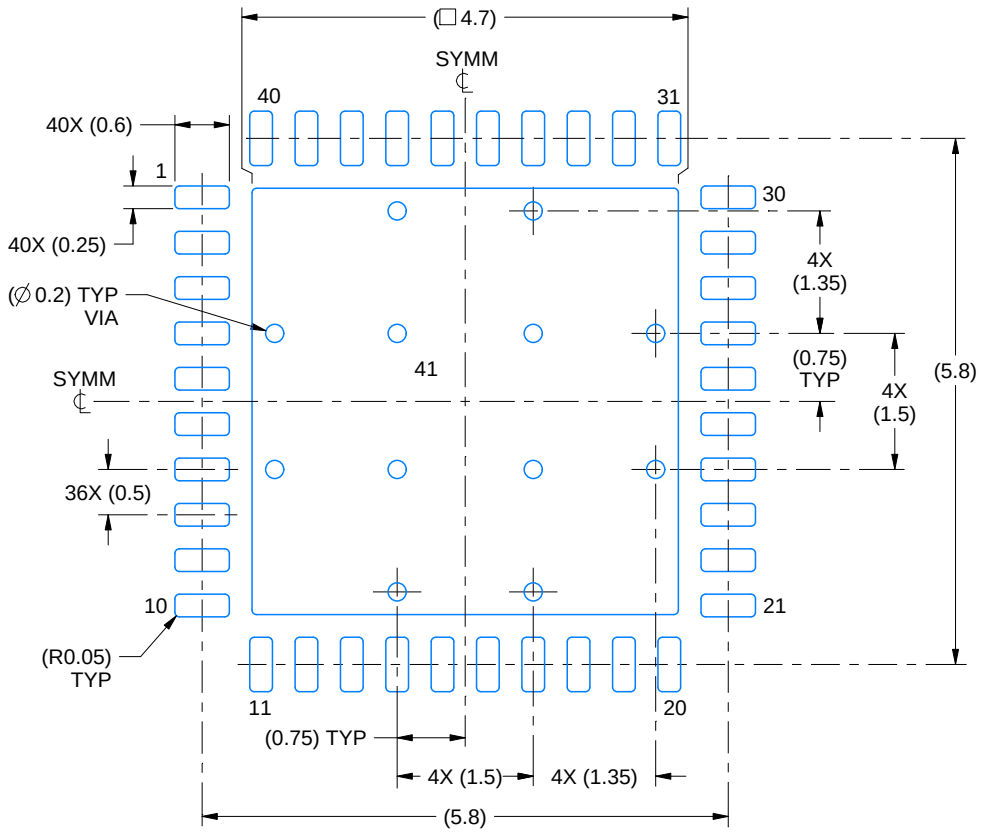
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

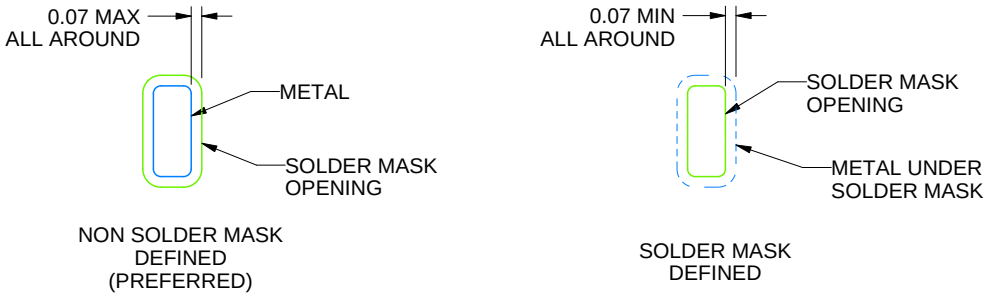


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:12X

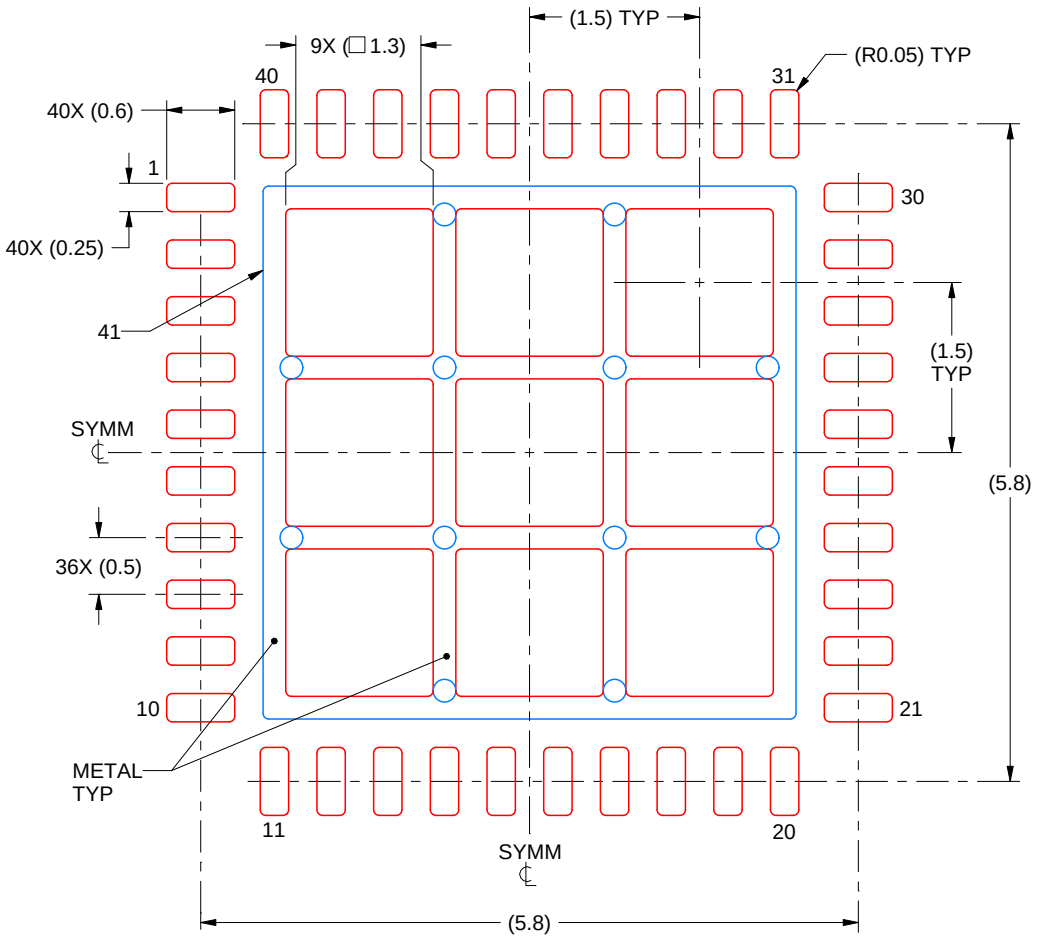


SOLDER MASK DETAILS

4219053/B 03/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
69% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

4219053/B 03/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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