

# DDS39RF12 and DDS39RFS12, 12GSPS to 24GSPS, Dual and Single Channel, Multi-Nyquist Direct Digital Synthesizer (DDS)

## 1 Features

- 16-bit, 12 to 24GSPS, multi-Nyquist DAC cores
- Maximum input data rate:
  - 16-bit, single channel complex I/Q: 775MSPS
  - 16-bit, dual channel complex I/Q: 388MSPS
- Output bandwidth (-3dB): 12GHz
- Performance at  $f_{OUT} = 2.997\text{GHz}$ , DES2XL mode, DEM and Dither off
  - Noise floor (small signal): -154dBFS/Hz
  - SFDR (-0.1dBFS): 68dBc
  - IMD3 (-7dBFS each tone): -74dBc
  - Additive phase noise, 10kHz offset: -138dBc/Hz
- Four Integrated digital up-converters (DUC)
  - Interpolation: 4x, 6x, 8x, 12x ... 256x
  - Complex baseband DUC for I/Q output
  - Complex to real up conversion for dual channel direct RF sampling
  - 64-bit frequency resolution NCOs
- Fast reconfiguration interface for fast frequency hopping
  - 4-bit data with 200MHz clock
  - 60ns reconfiguration (32-bit frequency)
  - Any frequency hopping with phase coherence
- JESD204C Interface
  - Up to 2 Lanes at up to 12.8Gbps each
  - Class C-S, subclass-1 compatible
  - Internal AC coupling capacitors
- SYSREF Windowing for automatic SYSREF timing calibration

## 2 Applications

- [Satellite communications \(SATCOM\)](#)
- Phased array antenna systems
- Synthetic aperture radar (SAR) exciter
- [Wireless communications testers](#)
- [Arbitrary waveform generator \(AWG\)](#)
- Agile, low phase noise LO generation

## 3 Description

DDS39RF12 and 'RFS12 are a family of dual and single channel direct digital synthesizers with 16-bit resolution digital-to-analog converters (DAC). The high sampling rate, output frequency range, 64-bit NCO frequency resolution and any frequency hopping with phase coherence makes the device capable of arbitrary waveform generation (AWG) and direct digital synthesis (DDS).

The devices can also be used as interpolating DACs for narrowband direct RF sampling or complex baseband signal generation. The maximum input data rate is 775MSPS for a single channel or 388MSPS for two channels. The devices can generate signals of up to 620MHz signal bandwidth (16-bit input resolution) at carrier frequencies exceeding 10GHz enabling direct sampling through C-band and into X-band.

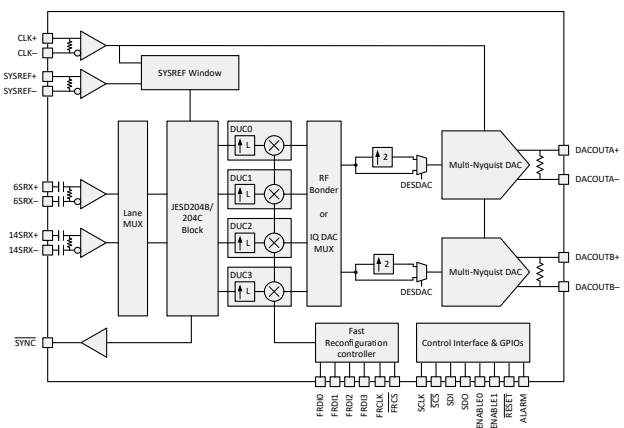
A JESD204B and JESD204C compatible serial interface has 2 receiver pairs capable of up to 12.8Gbps each. The interface is JESD204B and JESD204C subclass-1 compliant for deterministic latency and multi-device synchronization through the use of SYSREF.

### Package Information

| PART NUMBER             | PACKAGE <sup>(1)</sup> | PACKAGE SIZE <sup>(2)</sup> |
|-------------------------|------------------------|-----------------------------|
| DDS39RF12<br>DDS39RFS12 | FCBGA (256)            | 17mm x 17mm,<br>1mm pitch   |

(1) For more information, see [Section 11](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



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## 4 Device Comparison

| Part Number    | No. Channels | Maximum Sample Rate<br>(Single /Dual Edge) | Radiation Tolerance |         | JESD Interface     |
|----------------|--------------|--------------------------------------------|---------------------|---------|--------------------|
|                |              |                                            | SEL/SEFI            | TID     |                    |
| DAC39RF10      | 2            | 10.24/20.48GSPS                            | NA                  | NA      | Yes                |
| DAC39RFS10     | 1            | 10.24/20.48GSPS                            | NA                  | NA      | Yes                |
| DAC39RF12      | 2            | 12/24GSPS                                  | NA                  | NA      | Yes                |
| DAC39RFS12     | 1            | 12/24GSPS                                  | NA                  | NA      | Yes                |
| DAC39RF10-EP   | 2            | 10.4/20.8GSPS                              | NA                  | NA      | Yes                |
| DAC39RFS10-EP  | 1            | 10.4/20.8GSPS                              | NA                  | NA      | Yes                |
| DAC39RF10-SP   | 2            | 10.4/20.8GSPS                              | 12 MeV              | 300krad | Yes                |
| DAC39RFS10-SP  | 1            | 10.4/20.8GSPS                              | 120MeV              | 300krad | Yes                |
| DAC39RF10-SEP  | 2            | 10.4/20.8GSPS                              | 43MeV               | 30krad  | Yes                |
| DAC39RFS10-SEP | 1            | 10.4/20.8GSPS                              | 43MeV               | 30krad  | Yes                |
| DDS39RF12      | 2            | 12/24GSPS                                  | NA                  | NA      | 2 lanes only       |
| DDS39RFS12     | 1            | 12/24GSPS                                  | NA                  | NA      | 2 lanes only       |
| DDS39RF10      | 2            | 10.24/20.48GSPS                            | NA                  | NA      | 2 lanes only       |
| DDS39RFS10     | 1            | 10.24/20.48GSPS                            | NA                  | NA      | 2 lanes only       |
| DAC39RF10EF    | 2            | 10.24/20.48GSPS                            | NA                  | NA      | Input rate limited |
| DAC39RFS10EF   | 1            | 10.24/20.48GSPS                            | NA                  | NA      | Input rate limited |

## 5 Pin Configuration and Functions

|   | 1      | 2    | 3    | 4      | 5     | 6      | 7      | 8      | 9     | 10     | 11       | 12       | 13       | 14      | 15     | 16      |   |
|---|--------|------|------|--------|-------|--------|--------|--------|-------|--------|----------|----------|----------|---------|--------|---------|---|
| A | DGND   | DGND | DGND | DGND   | DGND  | DGND   | DGND   | DGND   | DGND  | AGND   | AGND     | DACOUTA+ | DACOUTA- | AGND    | VSSCLK | VSSCLK  | A |
| B | DGND   | DGND | DGND | DGND   | DGND  | DGND   | DGND   | DGND   | DGND  | AGND   | AGND     | AGND     | AGND     | AGND    | VSSCLK | VSSCLK  | B |
| C | DGND   | DGND | VDDT | VDDT   | VDDT  | DGND   | VDDT   | VDDT   | DGND  | AGND   | VEEAM18  | VEEAM18  | VEEAM18  | AGND    | VSSCLK | VSSCLK  | C |
| D | DGND   | DGND | VDDT | TXEN1  | TXEN0 | RESETB | SDO    | SDI    | VDDIO | AGND   | VEEAM18  | VEEAM18  | VEEAM18  | AGND    | VSSCLK | CLK+    | D |
| E | DGND   | DGND | DGND | FRDI0  | FRDI1 | SCANEN | SCSB   | SCLK   | VDDIO | VSSCLK | VSSCLK   | VDDCLK10 | VSSCLK   | VSSCLK  | VSSCLK | CLK-    | E |
| F | 6SRX+  | DGND | VDDT | FRCLK  | FRDI2 | DGND   | VDDDIG | VDDEA  | VDDEA | VDDL1A | VDDCLK10 | VSSCLK   | VSSCLK   | VSSCLK  | VSSCLK | VSSCLK  | F |
| G | 6SRX-  | DGND | VDDT | FRCSB  | FRDI3 | VDDT   | DGND   | VDDDIG | DGND  | VSSCLK | VSSCLK   | VSSCLK   | AGND     | VDDA18A | AGND   | AGND    | G |
| H | DGND   | DGND | DGND | ALARM  | VDDT  | DGND   | VDDDIG | DGND   | DGND  | VDDL1A | VDDCLK10 | VDDCLK18 | VDDCLK18 | VDDA18A | AGND   | RBIAS-  | H |
| J | DGND   | DGND | DGND | SYNCB  | VDDT  | DGND   | VDDDIG | DGND   | DGND  | VDDL1B | VDDCLK10 | VDDSYS18 | VDDSYS18 | VDDA18B | EXTREF | RBIAS+  | J |
| K | 14SRX+ | DGND | VDDT | VDDR18 | DGND  | VDDT   | DGND   | VDDDIG | DGND  | VSSCLK | VSSCLK   | VSSCLK   | AGND     | VDDA18B | AGND   | AGND    | K |
| L | 14SRX- | DGND | VDDT | VDDR18 | DGND  | DGND   | VDDDIG | VDDEB  | VDDEB | VDDL1B | VDDCLK10 | VSSCLK   | VSSCLK   | VSSCLK  | VSSCLK | VSSCLK  | L |
| M | DGND   | DGND | DGND | VDDR18 | RTEST | VDDT   | DGND   | VDDDIG | DGND  | VSSCLK | VSSCLK   | VDDCLK10 | VSSCLK   | VSSCLK  | VSSCLK | SYSREF+ | M |
| N | DGND   | DGND | VDDT | VDDR18 | DGND  | ATEST  | VDDDIG | DGND   | VQPS  | AGND   | VEEBM18  | VEEBM18  | VEEBM18  | AGND    | VSSCLK | SYSREF- | N |
| P | DGND   | DGND | VDDT | VDDT   | VDDT  | DGND   | VDDT   | VDDT   | VQPS  | AGND   | VEEBM18  | VEEBM18  | VEEBM18  | AGND    | VSSCLK | VSSCLK  | P |
| R | DGND   | DGND | DGND | DGND   | DGND  | DGND   | DGND   | DGND   | DGND  | AGND   | AGND     | AGND     | AGND     | AGND    | VSSCLK | VSSCLK  | R |
| T | DGND   | DGND | DGND | DGND   | DGND  | DGND   | DGND   | DGND   | DGND  | AGND   | AGND     | DACOUTB+ | DACOUTB- | AGND    | VSSCLK | VSSCLK  | T |
|   | 1      | 2    | 3    | 4      | 5     | 6      | 7      | 8      | 9     | 10     | 11       | 12       | 13       | 14      | 15     | 16      |   |

**Figure 5-1. FCBGA Package, 256-Ball Flip Chip BGA with 1mm pitch ( Top View)**

**Table 5-1. Pin Functions**

| PIN                                  |     | TYPE | DESCRIPTION                                                                                                                                                                              |
|--------------------------------------|-----|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME                                 | NO. |      |                                                                                                                                                                                          |
| DAC Outputs                          |     |      |                                                                                                                                                                                          |
| DACOUTA-                             | A13 | O    | DAC channel A analog output negative terminal. Output voltage must comply with DAC compliance voltage to maintain specified performance.                                                 |
| DACOUTA+                             | A12 | O    | DAC channel A analog output positive terminal. Output voltage must comply with DAC compliance voltage to maintain specified performance.                                                 |
| DACOUTB-                             | T13 | O    | DAC channel B analog output negative terminal. Output voltage must comply with DAC compliance voltage to maintain specified performance. <i>Not available in single channel devices.</i> |
| DACOUTB+                             | T12 | O    | DAC channel B analog output positive terminal. Output voltage must comply with DAC compliance voltage to maintain specified performance. <i>Not available in single channel devices.</i> |
| Differential Clock and SYSREF Inputs |     |      |                                                                                                                                                                                          |
| CLK-                                 | E16 | I    | Device clock input negative terminal. There is an internal 100Ω differential termination between CLK+ and CLK-. This input is self-biased and should be AC coupled to the clock source.  |
| CLK+                                 | D16 | I    | Device clock input positive terminal. There is an internal 100Ω differential termination between CLK+ and CLK-. This input is self-biased and should be AC coupled to the clock source.  |
| SYSREF-                              | N16 | I    | Differential JESD204C SYSREF input negative terminal. There is an internal 100Ω differential termination between SYSREF+ and SYSREF-.                                                    |
| SYSREF+                              | M16 | I    | Differential JESD204C SYSREF input negative terminal. There is an internal 100Ω differential termination between SYSREF+ and SYSREF-.                                                    |
| SerDes Interface                     |     |      |                                                                                                                                                                                          |
| 6SRX-                                | G1  | I    | Serdes Lane 6 negative input. Includes in package AC-coupling series capacitor and 100Ω internal termination to 6SRX+.                                                                   |
| 6SRX+                                | F1  | I    | Serdes Lane 6 positive input. Includes in package AC-coupling series capacitor and 100Ω internal termination to 6SRX-.                                                                   |
| 14SRX-                               | L1  | I    | Serdes Lane 14 negative input. Includes in package AC-coupling series capacitor and 100Ω internal termination to 14SRX+.                                                                 |
| 14SRX+                               | K1  | I    | Serdes Lane 14 positive input. Includes in package AC-coupling series capacitor and 100Ω internal termination to 14SRX-.                                                                 |
| GPIO Functions                       |     |      |                                                                                                                                                                                          |
| ALARM                                | H4  | O    | ALARM pin is asserted when an internal unmasked alarm is detected. Alarm mask is set by ALM_MASK register.                                                                               |
| FRCLK                                | F4  | I    | Fast reconfiguration interface clock.                                                                                                                                                    |
| FRCS                                 | G4  | I    | Fast reconfiguration interface chip select. Internal pullup.                                                                                                                             |
| FRDI0                                | E4  | I    | Fast reconfiguration interface data bit 0.                                                                                                                                               |
| FRDI1                                | E5  | I    | Fast reconfiguration interface data bit 1.                                                                                                                                               |
| FRDI2                                | F5  | I    | Fast reconfiguration interface data bit 2.                                                                                                                                               |
| FRDI3                                | G5  | I    | Fast reconfiguration interface data bit 3.                                                                                                                                               |
| RESET                                | D6  | I    | Device reset input, active low. Must be toggled after power up. Internal pullup.                                                                                                         |
| SCANEN                               | E6  | I    | TI use only, can be left unconnected. Internal pulldown.                                                                                                                                 |
| SCLK                                 | E8  | I    | Serial programming interface (SPI) clock input.                                                                                                                                          |
| SCS                                  | E7  | I    | Serial programming interface (SPI) device select input, active low. Internal pullup.                                                                                                     |
| SDI                                  | D8  | I    | Serial programming interface (SPI) data input.                                                                                                                                           |
| SDO                                  | D7  | O    | Serial programming interface (SPI) data output. High impedance when not reading out SPI data.                                                                                            |
| SYNC                                 | J4  | O    | JESD204C SYNC output, active low.                                                                                                                                                        |

**Table 5-1. Pin Functions (continued)**

| PIN              |                                                                            | TYPE | DESCRIPTION                                                                                                                                                                                                                                                                                                 |
|------------------|----------------------------------------------------------------------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME             | NO.                                                                        |      |                                                                                                                                                                                                                                                                                                             |
| TXEN0            | D5                                                                         | I    | Transmit enable for channel A active high input. This pin must be enabled using register <a href="#">USE_TX_EN0</a> . The DAC output is forced to midcode (0x0000 in 2's complement) when transmission is disabled. Internal pullup.                                                                        |
| TXEN1            | D4                                                                         | I    | Transmit enable for channel B active high input. This pin must be enabled using register <a href="#">USE_TX_EN1</a> . The DAC output is forced to midcode (0x0000 in 2's complement) when transmission is disabled. Internal pullup.                                                                        |
| Analog functions |                                                                            |      |                                                                                                                                                                                                                                                                                                             |
| ATEST            | N6                                                                         | O    | Analog test pin for TI use. Should be left disconnected.                                                                                                                                                                                                                                                    |
| EXTREF           | J15                                                                        | I/O  | Reference voltage output or input, determined by the <a href="#">EXTREF_EN</a> register field. If the internal reference is used, the ball should be tied through 0.1uF to AGND.                                                                                                                            |
| RBIAS-           | H16                                                                        | O    | Full-scale output current bias is set by the resistor tied from this terminal to RBIAS+.                                                                                                                                                                                                                    |
| RBIAS+           | J16                                                                        | O    | Full-scale output current bias is set by the resistor tied from this terminal to RBIAS-.                                                                                                                                                                                                                    |
| RTEST            | M5                                                                         | O    | TI use only. Tie to AGND.                                                                                                                                                                                                                                                                                   |
| Power Supplies   |                                                                            |      |                                                                                                                                                                                                                                                                                                             |
| VDDA18A          | G14 H14                                                                    | I    | 1.8V supply voltage for DAC channel A. Can be combined with VDDA18B, but may degrade channel-to-channel crosstalk (XTALK).                                                                                                                                                                                  |
| VDDA18B          | J14 K14                                                                    | I    | 1.8V supply voltage for DAC channel B. Can be combined with VDDA18A, but may degrade channel-to-channel crosstalk (XTALK).                                                                                                                                                                                  |
| VDDCLK10         | F11 H11 J11 L11<br>E12 M12                                                 | I    | 1V supply voltage for internal sampling clock distribution path. Noise or spurs on this supply may degrade phase noise performance. Recommended to separate from VDDDIG and VDDA for best performance.                                                                                                      |
| VDDCLK18         | H12 H13                                                                    | I    | 1.8V supply voltage for clock (CLK+/-) input buffer. Noise or spurs on this supply may degrade phase noise performance.                                                                                                                                                                                     |
| VDDDIG           | F7 H7 J7 L7 N7<br>G8 K8 M8                                                 | I    | 1V supply voltage for digital block. Recommended to separate from VDDA and VDDCLK for best performance.                                                                                                                                                                                                     |
| VDDEA            | F8 F9                                                                      | I    | 1V supply voltage for channel A DAC encoder. Recommended to separate from VDDDIG for best performance. Can be combined with VDDEB.                                                                                                                                                                          |
| VDDEB            | L8 L9                                                                      | I    | 1V supply voltage for channel B DAC encoder. Recommended to separate from VDDDIG for best performance. Can be combined with VDDEA.                                                                                                                                                                          |
| VDDIO            | D9 E9                                                                      | I    | 1.8V supply for CMOS input and output terminals.                                                                                                                                                                                                                                                            |
| VDDL A           | F10 H10                                                                    | I    | 1V supply for DAC analog latch for channel A. Separate from VDDL B for best channel-to-channel crosstalk (XTALK). Must be separated from VDDDIG for best performance.                                                                                                                                       |
| VDDL B           | J10 L10                                                                    | I    | 1V supply for DAC analog latch for channel B. Separate from VDDL A for best channel-to-channel crosstalk (XTALK). Must be separated from VDDDIG for best performance.                                                                                                                                       |
| VDDR18           | K4 L4 M4 N4                                                                | I    | 1.8V Supply voltage for SerDes receivers.                                                                                                                                                                                                                                                                   |
| VDDSYS18         | J12 J13                                                                    | I    | 1.8V supply voltage for SYSREF (SYSREF+/-) input buffer. Can be combined with VDDCLK18 when SYSREF is disabled during normal operation. This supply should be separate from VDDCLK18 when SYSREF is run continuously during operation to avoid noise and spur coupling and reduced phase noise performance. |
| VDDT             | C3 D3 F3 G3 K3<br>L3 N3 P3 C4 P4<br>C5 H5 J5 P5 G6<br>K6 M6 C7 P7 C8<br>P8 | I    | 1V Supply voltage for SerDes termination.                                                                                                                                                                                                                                                                   |
| VEEAM18          | C11 D11 C12 D12<br>C13 D13                                                 | I    | -1.8V supply voltage for DAC current source bias for channel A. Can be combined with VEEBM18, but may degrade channel-to-channel crosstalk (XTALK).                                                                                                                                                         |
| VEEBM18          | N11 P11 N12 P12<br>N13 P13                                                 | I    | -1.8V supply voltage for DAC current source bias for channel B. Can be combined with VEEAM18, but may degrade channel-to-channel crosstalk (XTALK).                                                                                                                                                         |
| VQPS             | N9 P9                                                                      | I    | TI use only. Can be tied to DGND during normal operation.                                                                                                                                                                                                                                                   |
| Grounds          |                                                                            |      |                                                                                                                                                                                                                                                                                                             |

**Table 5-1. Pin Functions (continued)**

| PIN    |                                                                                                                                                                                                                                                                                                    | TYPE | DESCRIPTION     |
|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-----------------|
| NAME   | NO.                                                                                                                                                                                                                                                                                                |      |                 |
| AGND   | A10 B10 C10 D10<br>N10 P10 R10<br>T10 A11 B11 R11<br>T11 B12 R12 B13<br>G13 K13 R13<br>A14 B14 C14 D14<br>N14 P14 R14 T14<br>G15 H15 K15<br>G16 K16                                                                                                                                                | -    | Analog ground.  |
| DGND   | A1 B1 C1 D1 E1<br>H1 J1 M1 N1 P1<br>R1 T1 A2 B2 C2<br>D2 E2 F2 G2 H2<br>J2 K2 L2 M2 N2<br>P2 R2 T2 A3 B3<br>E3 H3 J3 M3 R3<br>T3 A4 B4 R4 T4<br>A5 B5 K5 L5 N5<br>R5 T5 A6 B6 C6<br>F6 H6 J6 L6 P6<br>R6 T6 A7 B7 G7<br>K7 M7 R7 T7 A8<br>B8 H8 J8 N8 R8<br>T8 A9 B9 C9 G9<br>H9 J9 K9 M9 R9<br>T9 | -    | Digital ground. |
| VSSCLK | E10 G10 K10<br>M10 E11 G11 K11<br>M11 F12 G12 K12<br>L12 E13 F13 L13<br>M13 E14 F14 L14<br>M14 A15 B15<br>C15 D15 E15 F15<br>L15 M15 N15 P15<br>R15 T15 A16 B16<br>C16 F16 L16 P16<br>R16 T16                                                                                                      | -    | Clock ground.   |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

| PARAMETER                                                                                                                                                           | TEST CONDITIONS                                                                              | MIN  | MAX           | UNIT |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------|------|---------------|------|
| Supply voltage range                                                                                                                                                | Supply voltage range, VDDA18A, VDDA18B <sup>(2)</sup>                                        | -0.3 | 2.45          | V    |
|                                                                                                                                                                     | Supply voltage range, VEEAM18, VEEBM18 <sup>(2)</sup>                                        | -2.0 | 0.3           | V    |
|                                                                                                                                                                     | Supply voltage range, VDDCLK18, VDDSYS18 <sup>(3)</sup>                                      | -0.3 | 2.45          | V    |
|                                                                                                                                                                     | Supply voltage range, VDDL B, VDDL A, VDDCLK10 <sup>(3)</sup>                                | -0.3 | 1.3           | V    |
|                                                                                                                                                                     | Supply voltage range, VDDIO, VQPS, VDDR18 <sup>(4)</sup>                                     | -0.3 | 2.45          | V    |
|                                                                                                                                                                     | Supply voltage range, VDDDIG, VDDEB, VDDEA, VDDT <sup>(4)</sup>                              | -0.3 | 1.3           | V    |
| Voltage between any combination of AGND, DGND and VSSCLK                                                                                                            | Voltage between any combination of AGND, DGND and VSSCLK                                     | -0.1 | 0.1           | V    |
| Voltage applied to input pins                                                                                                                                       | CLK+, CLK-, SYSREF+, SYSREF- <sup>(3)</sup>                                                  | -0.3 | VDDCLK18+0.3  | V    |
|                                                                                                                                                                     | 6SRX-/+, 14SRX-/± AC Voltage                                                                 |      | 1.6           |      |
|                                                                                                                                                                     | 6SRX-/+, 14SRX-/± DC Voltage to GND                                                          | -5   | 5             |      |
|                                                                                                                                                                     | SCLK, SCS, SDI, RESET, SYNC, SCANEN, TXEN[0:1], FRDI[0:3], FRCLK, FRC S, SYNC <sup>(4)</sup> | -0.3 | VDDIO+0.3     |      |
|                                                                                                                                                                     | EXTREF <sup>(2)</sup>                                                                        | -0.3 | VDDA18A + 0.3 |      |
| Voltage at output pins                                                                                                                                              | DACOUTA+, DACOUTA- <sup>(2)</sup>                                                            | -0.3 | VDDA18A + 0.5 | V    |
|                                                                                                                                                                     | DACOUTB+, DACOUTB- <sup>(2)</sup>                                                            | -0.3 | VDDA18B + 0.5 |      |
|                                                                                                                                                                     | ATEST, RBIAS-/± <sup>(2)</sup>                                                               | -0.5 | VDDA18B + 0.3 |      |
|                                                                                                                                                                     | SDI, SDO, ALARM <sup>(4)</sup>                                                               | -0.5 | VDDIO + 0.3   |      |
| Peak input current (any input)                                                                                                                                      |                                                                                              | -20  | 20            | mA   |
| Peak total input current (sum of absolute value of all currents forced in or out, not including power supply current and DACOUTA+, DACOUTA-, DACOUTB+ and DACOUTB-) |                                                                                              |      | 30            | mA   |
| Junction temperature, T <sub>J</sub>                                                                                                                                |                                                                                              |      | 150           | °C   |
| Storage temperature, T <sub>stg</sub>                                                                                                                               |                                                                                              | -65  | 150           | °C   |

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#). Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Measured to AGND.
- (3) Measured to VSSCLK.
- (4) Measured to DGND.

### 6.2 ESD Ratings

|                    |                         |                                                                                 | VALUE | UNIT |
|--------------------|-------------------------|---------------------------------------------------------------------------------|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>     | 1000  | V    |
|                    |                         | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins <sup>(2)</sup> | 250   |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                      |                                           |                                                | MIN   | NOM  | MAX   | UNIT                  |
|----------------------|-------------------------------------------|------------------------------------------------|-------|------|-------|-----------------------|
| Supply voltage range | VDDA18A, VDDA18B <sup>(1)</sup>           |                                                | 1.71  | 1.8  | 1.89  | V                     |
|                      | VEEAM18, VEEBM18 <sup>(1)</sup>           |                                                | -1.89 | -1.8 | -1.71 | V                     |
|                      | VDDCLK18, VDDSYS18, VDDR18 <sup>(2)</sup> |                                                | 1.71  | 1.8  | 1.89  | V                     |
|                      | VDDL18, VDDL2, VDDCLK10 <sup>(2)</sup>    |                                                | 0.95  | 1    | 1.05  | V                     |
|                      | VDDIO <sup>(3)</sup>                      |                                                | 1.71  | 1.8  | 1.89  | V                     |
|                      | VQPS <sup>(3)</sup>                       |                                                | 0     | 0    | 1.89  | V                     |
|                      | VDDDIG, VDDEB, VDDEA, VDDT <sup>(3)</sup> |                                                | 0.95  | 1    | 1.05  | V                     |
| V <sub>CMI</sub>     | Input common mode voltage                 | CLK+, CLK- <sup>(2) (4)</sup>                  |       | 0.4  |       | V                     |
| V <sub>CMI</sub>     | Input common mode voltage                 | SYSREF+, SYSREF- <sup>(2) (4)</sup>            | 0     | 0.4  | 1.0   | V                     |
| V <sub>ID</sub>      | Input differential peak-to-peak voltage   | SYSREF+ to SYSREF-                             | 800   | 1000 | 2000  | mV <sub>PP-DIFF</sub> |
|                      |                                           | CLK+ to CLK-, f <sub>CLK</sub> < 5GHz          | 800   | 1000 | 1400  | mV <sub>PP-DIFF</sub> |
|                      |                                           | CLK+ to CLK-, 5GHz < f <sub>CLK</sub> < 7.5GHz | 800   | 1000 | 1800  | mV <sub>PP-DIFF</sub> |
|                      |                                           | CLK+ to CLK-, f <sub>CLK</sub> > 7.5GHz        | 800   | 1000 | 2000  | mV <sub>PP-DIFF</sub> |
| DC <sub>MIN</sub>    | CLK+/- duty cycle minimum                 |                                                |       | 45   |       | %                     |
| DC <sub>MAX</sub>    | CLK+/- duty cycle maximum                 |                                                |       | 55   |       | %                     |

(1) Measured to AGND.

(2) Measured to VSSCLK.

(3) Measured to DGND.

(4) SYSREF+/- termination has two options. In option 1 the inputs are weakly self-biased to the optimal common mode voltage, which is appropriate for AC coupling. In option 2, each input terminal is connected through 50Ohms to ground, which is appropriate to level shift from a higher common mode voltage.

## 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | 17mmx17mm FC-BGA | UNIT |
|-------------------------------|----------------------------------------------|------------------|------|
|                               |                                              | 256 PINS         |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 15.8             | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 0.9              | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 4.2              | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 0.4              | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 4.2              | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics - DC Specifications

Typical values at  $T_A = +25^\circ\text{C}$ , minimum and maximum values over operating free-air temperature range, typical supply voltages, 2 channels, DDS Mode,  $F_{\text{CLK}} = 12\text{ GHz}$ ,  $F_{\text{OUT}} = 2997\text{ MHz}$ , NRZ mode,  $I_{\text{FSSWITCH}} = 20.5\text{ mA}$ , unless otherwise noted.

| PARAMETER                                                  |                                                              | TEST CONDITIONS                                                                                                                                                                                               | MIN              | TYP              | MAX    | UNIT |
|------------------------------------------------------------|--------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|------------------|--------|------|
| DC ACCURACY                                                |                                                              |                                                                                                                                                                                                               |                  |                  |        |      |
| BITS                                                       | DAC core resolution                                          |                                                                                                                                                                                                               | 16               |                  |        | bits |
| DNL                                                        | Differential nonlinearity                                    |                                                                                                                                                                                                               | ±2.2             |                  |        | LSB  |
| INL                                                        | Integral nonlinearity                                        |                                                                                                                                                                                                               | ±9               |                  |        | LSB  |
| DAC ANALOG OUTPUT (DACOUTA+, DACOUTA–, DACOUTB+, DACOUTB–) |                                                              |                                                                                                                                                                                                               |                  |                  |        |      |
| I <sub>FS_SWITCH</sub>                                     | Switched full scale output current                           | 3.6-kΩ resistor from RBIAS+ to RBIAS–, <a href="#">COARSE_CUR_A</a> / <a href="#">COARSE_CUR_B</a> = 0xF and <a href="#">FINE_CUR_A</a> / <a href="#">FINE_CUR_B</a> = default, <a href="#">CUR_2X_EN</a> = 1 | 41               |                  | mA     |      |
|                                                            |                                                              | 3.6-kΩ resistor from RBIAS+ to RBIAS–, <a href="#">COARSE_CUR_A</a> / <a href="#">COARSE_CUR_B</a> = 0xF and <a href="#">FINE_CUR_A</a> / <a href="#">FINE_CUR_B</a> = default                                | 20.5             |                  |        |      |
|                                                            |                                                              | 3.6-kΩ resistor from RBIAS+ to RBIAS–, <a href="#">COARSE_CUR_A</a> / <a href="#">COARSE_CUR_B</a> = 0x0 and <a href="#">FINE_CUR_A</a> / <a href="#">FINE_CUR_B</a> = default, <a href="#">CUR_2X_EN</a> = 1 | 11               |                  |        |      |
|                                                            |                                                              | 3.6-kΩ resistor from RBIAS+ to RBIAS–, <a href="#">COARSE_CUR_A</a> / <a href="#">COARSE_CUR_B</a> = 0x0 and <a href="#">FINE_CUR_A</a> / <a href="#">FINE_CUR_B</a> = default                                | 5.5              |                  |        |      |
| I <sub>STATIC</sub>                                        | Static output current per pin                                | 3.6-kΩ resistor from RBIAS+ to RBIAS–, <a href="#">COARSE_CUR_A</a> / <a href="#">COARSE_CUR_B</a> = 0xF and <a href="#">FINE_CUR_A</a> / <a href="#">FINE_CUR_B</a> = default                                | 4.8              |                  | mA     |      |
| I <sub>FSDRIFT</sub>                                       | Full scale output current temperature drift                  | 3.6-kΩ resistor from RBIAS+ to RBIAS–, <a href="#">COARSE_CUR_A</a> / <a href="#">COARSE_CUR_B</a> = 0xF and <a href="#">FINE_CUR_A</a> / <a href="#">FINE_CUR_B</a> = default                                | –8.6             |                  | µA/°C  |      |
|                                                            |                                                              |                                                                                                                                                                                                               | –0.3             |                  | PPM/°C |      |
| I <sub>FSERROR</sub>                                       | Full scale current error                                     | 3.6-kΩ resistor from RBIAS+ to RBIAS–, <a href="#">COARSE_CUR_A</a> / <a href="#">COARSE_CUR_B</a> = 0xF and <a href="#">FINE_CUR_A</a> / <a href="#">FINE_CUR_B</a> = default                                | ±0.1             |                  | %      |      |
| I <sub>MIDOFFERR</sub>                                     | Mid Code Offset Error                                        | Mid Code offset                                                                                                                                                                                               | ±0.02            |                  | %FSR   |      |
| V <sub>COMP</sub>                                          | Output compliance voltage range                              | Measured from DACOUTA+, DACOUTA–, DACOUTB+ or DACOUTB– to AGND                                                                                                                                                | VDDA18 A/B – 0.5 | VDDA18 A/B + 0.5 | V      |      |
| C <sub>OUT</sub>                                           | Output capacitance                                           | Single-ended capacitance to ground                                                                                                                                                                            | 0.25             |                  | pF     |      |
| R <sub>TERM</sub>                                          | Output differential termination resistance                   |                                                                                                                                                                                                               | 102              |                  | Ω      |      |
| R <sub>TERMDRIFT</sub>                                     | Output differential termination resistance temperature coeff |                                                                                                                                                                                                               | –9.6             |                  | mΩ/°C  |      |
|                                                            |                                                              |                                                                                                                                                                                                               | –42              |                  | PPM/°C |      |
| CLOCK AND SYSREF INPUTS (CLK+, CLK–, SYSREF+, SYSREF–)     |                                                              |                                                                                                                                                                                                               |                  |                  |        |      |
| R <sub>T</sub>                                             | Internal differential termination resistance                 |                                                                                                                                                                                                               | 100              |                  | Ω      |      |
| C <sub>IN</sub>                                            | Internal differential input capacitance                      |                                                                                                                                                                                                               | 0.5              |                  | pF     |      |

## 6.5 Electrical Characteristics - DC Specifications (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , minimum and maximum values over operating free-air temperature range, typical supply voltages, 2 channels, DDS Mode,  $F_{\text{CLK}} = 12\text{ GHz}$ ,  $F_{\text{OUT}} = 2997\text{ MHz}$ , NRZ mode,  $I_{\text{FSSWITCH}} = 20.5\text{ mA}$ , unless otherwise noted.

| PARAMETER                                                                                                                             |                                                                                              | TEST CONDITIONS                                                                                | MIN                 | TYP     | MAX  | UNIT                        |
|---------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------|---------------------|---------|------|-----------------------------|
| <b>REFERENCE VOLTAGE</b>                                                                                                              |                                                                                              |                                                                                                |                     |         |      |                             |
| $V_{\text{REF}}$                                                                                                                      | Reference output voltage                                                                     |                                                                                                |                     | 0.9     |      | V                           |
| $V_{\text{REF-DRIFT}}$                                                                                                                | Absolute Value of Reference output voltage drift over temperature                            |                                                                                                |                     | 45      |      | ppm/ $^\circ\text{C}$       |
| $I_{\text{REF}}$                                                                                                                      | Maximum reference output current sourcing capability for EXTREF ball with internal reference |                                                                                                |                     | 100     |      | nA                          |
| <b>JESD204C SERDES INTERFACE ( 6SRX+/-, 14SRX+/-)</b>                                                                                 |                                                                                              |                                                                                                |                     |         |      |                             |
| $V_{\text{SRDIFF}}$                                                                                                                   | SerDes Receiver Input Amplitude                                                              |                                                                                                | 50                  |         | 1200 | mVppdiff                    |
| $V_{\text{SRCOM}}$                                                                                                                    | SerDes Input Common Mode                                                                     |                                                                                                | Internal AC coupled |         |      |                             |
| $Z_{\text{SRdiff}}$                                                                                                                   | SerDes Internal Differential Termination                                                     |                                                                                                |                     | 100     |      | $\Omega$                    |
| <b>CMOS INTERFACE (ALARM, SCLK, <math>\overline{\text{SCS}}</math>, SDI, SDO, RESET, FRDI[0:3], FRCLK, FRCS, SYNC, TXENABLE[0:1])</b> |                                                                                              |                                                                                                |                     |         |      |                             |
| $I_{\text{IH}}$                                                                                                                       | High level input current (with pulldowns)                                                    | SCANEN <sup>(1)</sup>                                                                          |                     |         | 200  | $\mu\text{A}$               |
| $I_{\text{IH}}$                                                                                                                       | High level input current (without pulldowns)                                                 | $\overline{\text{SCS}}$ , RESET, FRCS, TXEN[0:1], FRDI[0:3], FRCLK, SDI, SCLK <sup>(1)</sup>   |                     |         | 2    | $\mu\text{A}$               |
| $I_{\text{IL}}$                                                                                                                       | Low level input current (with pullups)                                                       | $\overline{\text{SCS}}$ , RESET, FRCS, TXEN[0:1] <sup>(1)</sup>                                | -200                |         |      | $\mu\text{A}$               |
| $I_{\text{IL}}$                                                                                                                       | Low level input current (without pullups)                                                    | SCANEN, FRDI[0:3], FRCLK, SDI, SCLK <sup>(1)</sup>                                             | -3                  |         |      | $\mu\text{A}$               |
| $C_{\text{I}}$                                                                                                                        | Input capacitance                                                                            | Input capacitance                                                                              |                     | 3       |      | pF                          |
| $V_{\text{IH}}$                                                                                                                       | High level input voltage                                                                     | SCLK, $\overline{\text{SCS}}$ , SDI, RESET, FRDI[0:3], FRCLK, FRCS, SCANEN, TXEN[0:1]          | 0.7 x VDDIO1<br>8   |         |      | V                           |
| $V_{\text{IL}}$                                                                                                                       | Low level input voltage                                                                      |                                                                                                | 0.3 x VDDIO1<br>8   |         |      | V                           |
| $V_{\text{OH}}$                                                                                                                       | High level output voltage                                                                    | ALARM, SDO, $\overline{\text{SYNC}}$ , $I_{\text{LOAD}} = -400\text{ }\mu\text{A}$             | 1.55                |         |      | V                           |
| $V_{\text{OL}}$                                                                                                                       | Low level output voltage                                                                     | ALARM, SDO, $\overline{\text{SYNC}}$ , $I_{\text{LOAD}} = 400\text{ }\mu\text{A}$              |                     |         | 0.2  | V                           |
| <b>TEMPERATURE SENSOR</b>                                                                                                             |                                                                                              |                                                                                                |                     |         |      |                             |
| Res                                                                                                                                   | Resolution                                                                                   |                                                                                                |                     | 1       |      | $^\circ\text{C}/\text{LSB}$ |
| Range                                                                                                                                 | Digital Range                                                                                |                                                                                                | -50                 |         | 150  | $^\circ\text{C}$            |
| $T_{\text{ERROR}}$                                                                                                                    | Temperature Error                                                                            | $T_A = 25^\circ\text{C}$ , device powered down except for temperature sensor and SPI interface |                     | $\pm 5$ |      | $^\circ\text{C}$            |

(1) With no IO supply voltage offset in connecting device.

## 6.6 Electrical Characteristics - AC Specifications

Typical values at  $T_A = +25^\circ\text{C}$ , minimum and maximum values over operating free-air temperature range, typical supply voltages,  $F_{\text{CLK}} = 12\text{ GHz}$ , DDS Mode,  $I_{\text{FS\_SWITCH}} = 20.5\text{ mA}$ , single tone amplitude = 0 dBFS, SE DEM and Dither (DEM\_ADJ = 1 below 750 MHz and DEM\_ADJ = 0 above 750 MHz), unless otherwise noted.  $F_{\text{DAC}} = F_{\text{CLK}}$  in NRZ and RF modes and  $F_{\text{DAC}} = 2 \cdot F_{\text{CLK}}$  in DES2XL/H modes.

| PARAMETER                              |                                                                                                                          | TEST CONDITIONS                                                                                           | MIN | TYP   | MAX | UNIT |
|----------------------------------------|--------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------|-----|-------|-----|------|
| MODE INDEPENDENT PARAMETERS            |                                                                                                                          |                                                                                                           |     |       |     |      |
| F <sub>CLK</sub>                       | DAC clock rate                                                                                                           |                                                                                                           | 0.8 |       | 12  | GHz  |
| BW                                     | Analog output bandwidth (–3 dB)                                                                                          | Excluding sinx/x response. Useable bandwidth may exceed the –3 dB point. I <sub>FS_SWITCH</sub> = 20.5 mA |     | 12.15 |     | GHz  |
|                                        |                                                                                                                          | Excluding sinx/x response. Useable bandwidth may exceed the –3 dB point. I <sub>FS_SWITCH</sub> = 41 mA   |     | 11.95 |     |      |
| Crosstalk                              | Isolation between channel A (DACOUTA+/-) and channel B (DACOUTB+/-), f <sub>OUT</sub> = -25 MHz offset on victim channel | f <sub>OUT</sub> = 97 MHz, NRZ mode                                                                       |     | 92    |     | dBc  |
|                                        |                                                                                                                          | f <sub>OUT</sub> = 1897 MHz, NRZ mode                                                                     |     | 97    |     | dBc  |
|                                        |                                                                                                                          | f <sub>OUT</sub> = 3897 MHz, NRZ mode                                                                     |     | 84    |     | dBc  |
|                                        |                                                                                                                          | f <sub>OUT</sub> = 5897 MHz, RF mode                                                                      |     | 80    |     | dBc  |
|                                        |                                                                                                                          | f <sub>OUT</sub> = 7897 MHz, RF mode                                                                      |     | 74    |     | dBc  |
| DAC OUTPUT TIME DOMAIN CHARACTERISTICS |                                                                                                                          |                                                                                                           |     |       |     |      |
| t <sub>RISE</sub>                      | 10% to 90% <sup>(1)</sup>                                                                                                | JMODE 6, 1x Interpolation                                                                                 |     | 41    |     | ps   |
| t <sub>FALL</sub>                      | 90% to 10% <sup>(1)</sup>                                                                                                | JMODE 6, 1x Interpolation                                                                                 |     | 41    |     | ps   |
| f <sub>CLK</sub> DC Feedthrough        | Relative to fullscale sinewave at 1 GHz                                                                                  | NRZ Mode, f <sub>OUT</sub> = DC (mid-code), DEM/Dither off                                                |     | 61    |     | dBc  |
|                                        |                                                                                                                          | NRZ Mode, f <sub>OUT</sub> = DC (mid-code), DEM/Dither on                                                 |     | 65    |     | dBc  |
|                                        |                                                                                                                          | DES2XL Mode, f <sub>OUT</sub> = DC (mid-code), DEM/Dither off                                             |     | 62    |     | dBc  |
|                                        |                                                                                                                          | DES2XL Mode, f <sub>OUT</sub> = DC (mid-code), DEM/Dither on                                              |     | 67    |     | dBc  |
| 2*f <sub>CLK</sub> DC Feedthrough      | Relative to fullscale sinewave at 1 GHz                                                                                  | DES2XL Mode, f <sub>OUT</sub> = DC (mid-code), DEM/Dither off                                             |     | 86    |     | dBc  |
|                                        |                                                                                                                          | DES2XL Mode, f <sub>OUT</sub> = DC (mid-code), DEM/Dither on                                              |     | 84    |     | dBc  |

## 6.6 Electrical Characteristics - AC Specifications (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , minimum and maximum values over operating free-air temperature range, typical supply voltages,  $F_{\text{CLK}} = 12\text{ GHz}$ , DDS Mode,  $I_{\text{FS\_SWITCH}} = 20.5\text{ mA}$ , single tone amplitude = 0 dBFS, SE DEM and Dither (DEM\_ADJ = 1 below 750 MHz and DEM\_ADJ = 0 above 750 MHz), unless otherwise noted.  $F_{\text{DAC}} = F_{\text{CLK}}$  in NRZ and RF modes and  $F_{\text{DAC}} = 2 \cdot F_{\text{CLK}}$  in DES2XL/H modes.

| PARAMETER                                                       |                                                                                                             | TEST CONDITIONS                    | MIN | TYP  | MAX | UNIT |
|-----------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------|------------------------------------|-----|------|-----|------|
| <b>12 GSPS, DUAL or SINGLE CHANNEL MODE, DDS Mode, NRZ MODE</b> |                                                                                                             |                                    |     |      |     |      |
| $P_{\text{OUT}}$                                                | Output power into 100 $\Omega$ load, $I_{\text{FS\_SWITCH}} = 20.5\text{ mA}^{(2)}$                         | $f_{\text{OUT}} = 97\text{ MHz}$   |     | 1.1  |     | dBm  |
|                                                                 |                                                                                                             | $f_{\text{OUT}} = 997\text{ MHz}$  |     | 0.6  |     | dBm  |
|                                                                 |                                                                                                             | $f_{\text{OUT}} = 1997\text{ MHz}$ |     | 0.3  |     | dBm  |
|                                                                 |                                                                                                             | $f_{\text{OUT}} = 2997\text{ MHz}$ |     | -0.3 |     | dBm  |
|                                                                 |                                                                                                             | $f_{\text{OUT}} = 3997\text{ MHz}$ |     | -2.2 |     | dBm  |
|                                                                 |                                                                                                             | $f_{\text{OUT}} = 4997\text{ MHz}$ |     | -3.2 |     | dBm  |
|                                                                 | Output power into 100 $\Omega$ load, $I_{\text{FS\_SWITCH}} = 41\text{ mA}^{(2)}$                           | $f_{\text{OUT}} = 97\text{ MHz}$   |     | 7.0  |     | dBm  |
|                                                                 |                                                                                                             | $f_{\text{OUT}} = 997\text{ MHz}$  |     | 6.5  |     | dBm  |
|                                                                 |                                                                                                             | $f_{\text{OUT}} = 1997\text{ MHz}$ |     | 6.2  |     | dBm  |
|                                                                 |                                                                                                             | $f_{\text{OUT}} = 2997\text{ MHz}$ |     | 5.6  |     | dBm  |
|                                                                 |                                                                                                             | $f_{\text{OUT}} = 3997\text{ MHz}$ |     | 3.7  |     | dBm  |
|                                                                 |                                                                                                             | $f_{\text{OUT}} = 4997\text{ MHz}$ |     | 2.6  |     | dBm  |
| SFDR                                                            | Spurious free dynamic range (SFDR) across $0 - F_{\text{DAC}}/2$ , $I_{\text{FS\_SWITCH}} = 20.5\text{ mA}$ | $f_{\text{OUT}} = 97\text{ MHz}$   |     | 78   |     | dBc  |
|                                                                 |                                                                                                             | $f_{\text{OUT}} = 997\text{ MHz}$  |     | 67   |     | dBc  |
|                                                                 |                                                                                                             | $f_{\text{OUT}} = 1997\text{ MHz}$ |     | 66   |     | dBc  |
|                                                                 |                                                                                                             | $f_{\text{OUT}} = 2997\text{ MHz}$ |     | 60   |     | dBc  |
|                                                                 |                                                                                                             | $f_{\text{OUT}} = 3997\text{ MHz}$ |     | 62   |     | dBc  |
|                                                                 |                                                                                                             | $f_{\text{OUT}} = 4997\text{ MHz}$ |     | 55   |     | dBc  |
|                                                                 | Spurious free dynamic range (SFDR) across $0 - F_{\text{DAC}}/2$ , $I_{\text{FS\_SWITCH}} = 41\text{ mA}$   | $f_{\text{OUT}} = 97\text{ MHz}$   |     | 71   |     | dBc  |
|                                                                 |                                                                                                             | $f_{\text{OUT}} = 997\text{ MHz}$  |     | 51   |     | dBc  |
|                                                                 |                                                                                                             | $f_{\text{OUT}} = 1997\text{ MHz}$ |     | 45   |     | dBc  |
|                                                                 |                                                                                                             | $f_{\text{OUT}} = 2997\text{ MHz}$ |     | 48   |     | dBc  |
|                                                                 |                                                                                                             | $f_{\text{OUT}} = 3997\text{ MHz}$ |     | 51   |     | dBc  |
|                                                                 |                                                                                                             | $f_{\text{OUT}} = 4997\text{ MHz}$ |     | 51   |     | dBc  |
| HD2                                                             | Second harmonic (HD2), $0 - F_{\text{DAC}}/2$ , $I_{\text{FS\_SWITCH}} = 20.5\text{ mA}$                    | $f_{\text{OUT}} = 97\text{ MHz}$   |     | -78  |     | dBc  |
|                                                                 |                                                                                                             | $f_{\text{OUT}} = 997\text{ MHz}$  |     | -74  |     | dBc  |
|                                                                 |                                                                                                             | $f_{\text{OUT}} = 1997\text{ MHz}$ |     | -70  |     | dBc  |
|                                                                 |                                                                                                             | $f_{\text{OUT}} = 2997\text{ MHz}$ |     | -66  |     | dBc  |
|                                                                 |                                                                                                             | $f_{\text{OUT}} = 3997\text{ MHz}$ |     | -64  |     | dBc  |
|                                                                 |                                                                                                             | $f_{\text{OUT}} = 4997\text{ MHz}$ |     | -55  |     | dBc  |
|                                                                 | Second harmonic (HD2), $0 - F_{\text{DAC}}/2$ , $I_{\text{FS\_SWITCH}} = 41\text{ mA}$                      | $f_{\text{OUT}} = 97\text{ MHz}$   |     | -66  |     | dBc  |
|                                                                 |                                                                                                             | $f_{\text{OUT}} = 997\text{ MHz}$  |     | -68  |     | dBc  |
|                                                                 |                                                                                                             | $f_{\text{OUT}} = 1997\text{ MHz}$ |     | -64  |     | dBc  |
|                                                                 |                                                                                                             | $f_{\text{OUT}} = 2997\text{ MHz}$ |     | -59  |     | dBc  |
|                                                                 |                                                                                                             | $f_{\text{OUT}} = 3997\text{ MHz}$ |     | -59  |     | dBc  |
|                                                                 |                                                                                                             | $f_{\text{OUT}} = 4997\text{ MHz}$ |     | -52  |     | dBc  |

## 6.6 Electrical Characteristics - AC Specifications (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , minimum and maximum values over operating free-air temperature range, typical supply voltages,  $F_{\text{CLK}} = 12\text{ GHz}$ , DDS Mode,  $I_{\text{FS\_SWITCH}} = 20.5\text{ mA}$ , single tone amplitude = 0 dBFS, SE DEM and Dither (DEM\_ADJ = 1 below 750 MHz and DEM\_ADJ = 0 above 750 MHz), unless otherwise noted.  $F_{\text{DAC}} = F_{\text{CLK}}$  in NRZ and RF modes and  $F_{\text{DAC}} = 2 \cdot F_{\text{CLK}}$  in DES2XL/H modes.

| PARAMETER               |                                                                                           | TEST CONDITIONS                                         | MIN | TYP  | MAX | UNIT |
|-------------------------|-------------------------------------------------------------------------------------------|---------------------------------------------------------|-----|------|-----|------|
| HD3                     | Third harmonic (HD3), 0 - $F_{\text{DAC}}/2$ , $I_{\text{FS\_SWITCH}} = 20.5\text{ mA}$   | $f_{\text{OUT}} = 97\text{ MHz}$                        |     | -90  |     | dBc  |
|                         |                                                                                           | $f_{\text{OUT}} = 997\text{ MHz}$                       |     | -67  |     | dBc  |
|                         |                                                                                           | $f_{\text{OUT}} = 1997\text{ MHz}$                      |     | -68  |     | dBc  |
|                         |                                                                                           | $f_{\text{OUT}} = 2997\text{ MHz}$                      |     | -63  |     | dBc  |
|                         |                                                                                           | $f_{\text{OUT}} = 3997\text{ MHz}$                      |     | -66  |     | dBc  |
|                         |                                                                                           | $f_{\text{OUT}} = 4997\text{ MHz}$                      |     | -75  |     | dBc  |
|                         | Third harmonic (HD3), 0 - $F_{\text{DAC}}/2$ , $I_{\text{FS\_SWITCH}} = 41\text{ mA}$     | $f_{\text{OUT}} = 97\text{ MHz}$                        |     | -73  |     | dBc  |
|                         |                                                                                           | $f_{\text{OUT}} = 997\text{ MHz}$                       |     | -55  |     | dBc  |
|                         |                                                                                           | $f_{\text{OUT}} = 1997\text{ MHz}$                      |     | -49  |     | dBc  |
|                         |                                                                                           | $f_{\text{OUT}} = 2997\text{ MHz}$                      |     | -47  |     | dBc  |
|                         |                                                                                           | $f_{\text{OUT}} = 3997\text{ MHz}$                      |     | -49  |     | dBc  |
|                         |                                                                                           | $f_{\text{OUT}} = 4997\text{ MHz}$                      |     | -52  |     | dBc  |
| SFDR <sub>NONHD23</sub> | non-HD2/3 SFDR, $I_{\text{FS\_SWITCH}} = 20.5\text{ mA}$                                  | $f_{\text{OUT}} = 97\text{ MHz}$                        |     | 94   |     | dBc  |
|                         |                                                                                           | $f_{\text{OUT}} = 997\text{ MHz}$                       |     | 87   |     | dBc  |
|                         |                                                                                           | $f_{\text{OUT}} = 1997\text{ MHz}$                      |     | 92   |     | dBc  |
|                         |                                                                                           | $f_{\text{OUT}} = 2997\text{ MHz}$                      |     | 91   |     | dBc  |
|                         |                                                                                           | $f_{\text{OUT}} = 3997\text{ MHz}$                      |     | 89   |     | dBc  |
|                         |                                                                                           | $f_{\text{OUT}} = 4997\text{ MHz}$                      |     | 86   |     | dBc  |
|                         | non-HD2/3 SFDR, $I_{\text{FS\_SWITCH}} = 41\text{ mA}$                                    | $f_{\text{OUT}} = 97\text{ MHz}$                        |     | 87   |     | dBc  |
|                         |                                                                                           | $f_{\text{OUT}} = 997\text{ MHz}$                       |     | 72   |     | dBc  |
|                         |                                                                                           | $f_{\text{OUT}} = 1997\text{ MHz}$                      |     | 73   |     | dBc  |
|                         |                                                                                           | $f_{\text{OUT}} = 2997\text{ MHz}$                      |     | 74   |     | dBc  |
|                         |                                                                                           | $f_{\text{OUT}} = 3997\text{ MHz}$                      |     | 74   |     | dBc  |
|                         |                                                                                           | $f_{\text{OUT}} = 4997\text{ MHz}$                      |     | 72   |     | dBc  |
| IMD3                    | Third-order two tone intermodulation distortion, $I_{\text{FS\_SWITCH}} = 20.5\text{ mA}$ | $f_{\text{OUT}} = 97 \pm 10\text{ MHz}$ , -7dBFS/tone   |     | -100 |     | dBc  |
|                         |                                                                                           | $f_{\text{OUT}} = 997 \pm 10\text{ MHz}$ , -7dBFS/tone  |     | -73  |     | dBc  |
|                         |                                                                                           | $f_{\text{OUT}} = 1997 \pm 10\text{ MHz}$ , -7dBFS/tone |     | -75  |     | dBc  |
|                         |                                                                                           | $f_{\text{OUT}} = 2997 \pm 10\text{ MHz}$ , -7dBFS/tone |     | -71  |     | dBc  |
|                         |                                                                                           | $f_{\text{OUT}} = 3997 \pm 10\text{ MHz}$ , -7dBFS/tone |     | -65  |     | dBc  |
|                         |                                                                                           | $f_{\text{OUT}} = 4997 \pm 10\text{ MHz}$ , -7dBFS/tone |     | -61  |     | dBc  |
|                         | Third-order two tone intermodulation distortion, $I_{\text{FS\_SWITCH}} = 41\text{ mA}$   | $f_{\text{OUT}} = 97 \pm 10\text{ MHz}$ , -7dBFS/tone   |     | -87  |     | dBc  |
|                         |                                                                                           | $f_{\text{OUT}} = 997 \pm 10\text{ MHz}$ , -7dBFS/tone  |     | -61  |     | dBc  |
|                         |                                                                                           | $f_{\text{OUT}} = 1997 \pm 10\text{ MHz}$ , -7dBFS/tone |     | -58  |     | dBc  |
|                         |                                                                                           | $f_{\text{OUT}} = 2997 \pm 10\text{ MHz}$ , -7dBFS/tone |     | -52  |     | dBc  |
|                         |                                                                                           | $f_{\text{OUT}} = 3997 \pm 10\text{ MHz}$ , -7dBFS/tone |     | -51  |     | dBc  |
|                         |                                                                                           | $f_{\text{OUT}} = 4997 \pm 10\text{ MHz}$ , -7dBFS/tone |     | -47  |     | dBc  |

## 6.6 Electrical Characteristics - AC Specifications (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , minimum and maximum values over operating free-air temperature range, typical supply voltages,  $F_{\text{CLK}} = 12\text{ GHz}$ , DDS Mode,  $I_{\text{FS\_SWITCH}} = 20.5\text{ mA}$ , single tone amplitude = 0 dBFS, SE DEM and Dither (DEM\_ADJ = 1 below 750 MHz and DEM\_ADJ = 0 above 750 MHz), unless otherwise noted.  $F_{\text{DAC}} = F_{\text{CLK}}$  in NRZ and RF modes and  $F_{\text{DAC}} = 2 \cdot F_{\text{CLK}}$  in DES2XL/H modes.

| PARAMETER |                                                                                                                  | TEST CONDITIONS                                                                                               | MIN | TYP  | MAX | UNIT    |
|-----------|------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------|-----|------|-----|---------|
| NSD       | Noise spectral density, large signal, sinusoidal output, $I_{\text{FS\_SWITCH}} = 20.5\text{ mA}$ <sup>(3)</sup> | $f_{\text{OUT}} = 97\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$                                        |     | -158 |     | dBc/Hz  |
|           |                                                                                                                  | $f_{\text{OUT}} = 997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$                                       |     | -158 |     | dBc/Hz  |
|           |                                                                                                                  | $f_{\text{OUT}} = 1997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$                                      |     | -154 |     | dBc/Hz  |
|           |                                                                                                                  | $f_{\text{OUT}} = 2997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$                                      |     | -151 |     | dBc/Hz  |
|           |                                                                                                                  | $f_{\text{OUT}} = 3997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$                                      |     | -149 |     | dBc/Hz  |
|           |                                                                                                                  | $f_{\text{OUT}} = 4997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$                                      |     | -147 |     | dBc/Hz  |
| NSD       | Noise spectral density, large signal, sinusoidal output, $I_{\text{FS\_SWITCH}} = 41\text{ mA}$ <sup>(3)</sup>   | $f_{\text{OUT}} = 97\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$                                        |     | -158 |     | dBc/Hz  |
|           |                                                                                                                  | $f_{\text{OUT}} = 997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$                                       |     | -157 |     | dBc/Hz  |
|           |                                                                                                                  | $f_{\text{OUT}} = 1997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$                                      |     | -154 |     | dBc/Hz  |
|           |                                                                                                                  | $f_{\text{OUT}} = 2997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$                                      |     | -151 |     | dBc/Hz  |
|           |                                                                                                                  | $f_{\text{OUT}} = 3997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$                                      |     | -148 |     | dBc/Hz  |
|           |                                                                                                                  | $f_{\text{OUT}} = 4997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$                                      |     | -147 |     | dBc/Hz  |
| NSD       | Noise spectral density, small signal, sinusoidal output, $I_{\text{FS\_SWITCH}} = 20.5\text{ mA}$ <sup>(3)</sup> | $A_{\text{OUT}} = -20\text{ dBFS}$ , $f_{\text{OUT}} = 97\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$   |     | -155 |     | dBFS/Hz |
|           |                                                                                                                  | $A_{\text{OUT}} = -20\text{ dBFS}$ , $f_{\text{OUT}} = 997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$  |     | -157 |     | dBFS/Hz |
|           |                                                                                                                  | $A_{\text{OUT}} = -20\text{ dBFS}$ , $f_{\text{OUT}} = 1997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$ |     | -155 |     | dBFS/Hz |
|           |                                                                                                                  | $A_{\text{OUT}} = -20\text{ dBFS}$ , $f_{\text{OUT}} = 2997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$ |     | -153 |     | dBFS/Hz |
|           |                                                                                                                  | $A_{\text{OUT}} = -20\text{ dBFS}$ , $f_{\text{OUT}} = 3997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$ |     | -152 |     | dBFS/Hz |
|           |                                                                                                                  | $A_{\text{OUT}} = -20\text{ dBFS}$ , $f_{\text{OUT}} = 4997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$ |     | -150 |     | dBFS/Hz |
| NSD       | Noise spectral density, small signal, sinusoidal output, $I_{\text{FS\_SWITCH}} = 41\text{ mA}$ <sup>(3)</sup>   | $A_{\text{OUT}} = -20\text{ dBFS}$ , $f_{\text{OUT}} = 97\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$   |     | -156 |     | dBFS/Hz |
|           |                                                                                                                  | $A_{\text{OUT}} = -20\text{ dBFS}$ , $f_{\text{OUT}} = 997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$  |     | -158 |     | dBFS/Hz |
|           |                                                                                                                  | $A_{\text{OUT}} = -20\text{ dBFS}$ , $f_{\text{OUT}} = 1997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$ |     | -156 |     | dBFS/Hz |
|           |                                                                                                                  | $A_{\text{OUT}} = -20\text{ dBFS}$ , $f_{\text{OUT}} = 2997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$ |     | -154 |     | dBFS/Hz |
|           |                                                                                                                  | $A_{\text{OUT}} = -20\text{ dBFS}$ , $f_{\text{OUT}} = 3997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$ |     | -152 |     | dBFS/Hz |
|           |                                                                                                                  | $A_{\text{OUT}} = -20\text{ dBFS}$ , $f_{\text{OUT}} = 4997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$ |     | -150 |     | dBFS/Hz |

## 6.6 Electrical Characteristics - AC Specifications (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , minimum and maximum values over operating free-air temperature range, typical supply voltages,  $F_{\text{CLK}} = 12\text{ GHz}$ , DDS Mode,  $I_{\text{FS\_SWITCH}} = 20.5\text{ mA}$ , single tone amplitude = 0 dBFS, SE DEM and Dither (DEM\_ADJ = 1 below 750 MHz and DEM\_ADJ = 0 above 750 MHz), unless otherwise noted.  $F_{\text{DAC}} = F_{\text{CLK}}$  in NRZ and RF modes and  $F_{\text{DAC}} = 2 \cdot F_{\text{CLK}}$  in DES2XL/H modes.

| PARAMETER |                                                                                                    | TEST CONDITIONS                                                                       | MIN | TYP  | MAX | UNIT   |
|-----------|----------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|-----|------|-----|--------|
| PN        | Additive DAC phase noise, external clock contribution subtracted out, NRZ mode, DEM and Dither off | $f_{\text{CLK}} = 12\text{ GHz}$ , $f_{\text{OUT}} = 997\text{ MHz}$ , 100 Hz offset  |     | -121 |     | dBc/Hz |
|           |                                                                                                    | $f_{\text{CLK}} = 12\text{ GHz}$ , $f_{\text{OUT}} = 997\text{ MHz}$ , 1 KHz offset   |     | -132 |     | dBc/Hz |
|           |                                                                                                    | $f_{\text{CLK}} = 12\text{ GHz}$ , $f_{\text{OUT}} = 997\text{ MHz}$ , 10 kHz offset  |     | -143 |     | dBc/Hz |
|           |                                                                                                    | $f_{\text{CLK}} = 12\text{ GHz}$ , $f_{\text{OUT}} = 997\text{ MHz}$ , 100 kHz offset |     | -153 |     | dBc/Hz |
|           |                                                                                                    | $f_{\text{CLK}} = 12\text{ GHz}$ , $f_{\text{OUT}} = 997\text{ MHz}$ , 1 MHz offset   |     | -159 |     | dBc/Hz |
|           |                                                                                                    | $f_{\text{CLK}} = 12\text{ GHz}$ , $f_{\text{OUT}} = 997\text{ MHz}$ , 10 MHz offset  |     | -165 |     | dBc/Hz |
|           |                                                                                                    | $f_{\text{CLK}} = 12\text{ GHz}$ , $f_{\text{OUT}} = 997\text{ MHz}$ , 100 MHz offset |     | -167 |     | dBc/Hz |

## 6.6 Electrical Characteristics - AC Specifications (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , minimum and maximum values over operating free-air temperature range, typical supply voltages,  $F_{\text{CLK}} = 12\text{ GHz}$ , DDS Mode,  $I_{\text{FS\_SWITCH}} = 20.5\text{ mA}$ , single tone amplitude = 0 dBFS, SE DEM and Dither (DEM\_ADJ = 1 below 750 MHz and DEM\_ADJ = 0 above 750 MHz), unless otherwise noted.  $F_{\text{DAC}} = F_{\text{CLK}}$  in NRZ and RF modes and  $F_{\text{DAC}} = 2 \cdot F_{\text{CLK}}$  in DES2XL/H modes.

| PARAMETER                                                      | TEST CONDITIONS                                                               | MIN                                                                                             | TYP  | MAX | UNIT |
|----------------------------------------------------------------|-------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------|------|-----|------|
| <b>12 GSPS, DUAL or SINGLE CHANNEL MODE, DDS Mode, RF MODE</b> |                                                                               |                                                                                                 |      |     |      |
| $P_{\text{OUT}}$                                               | Output power with 2:1 balun and 50 $\Omega$ load                              | $f_{\text{OUT}} = 6997\text{ MHz}$                                                              | -2.2 |     | dBm  |
|                                                                |                                                                               | $f_{\text{OUT}} = 7997\text{ MHz}$ , $I_{\text{FS\_SWITCH}} = 41\text{ mA}$                     | 3.0  |     | dBm  |
|                                                                |                                                                               | $f_{\text{OUT}} = 7997\text{ MHz}$                                                              | -2.4 |     | dBm  |
|                                                                |                                                                               | $f_{\text{OUT}} = 8997\text{ MHz}$                                                              | -5.0 |     | dBm  |
|                                                                |                                                                               | $f_{\text{OUT}} = 10997\text{ MHz}$                                                             | -8.5 |     | dBm  |
| SFDR                                                           | Spurious free dynamic range (SFDR) across $F_{\text{DAC}}/2 - F_{\text{DAC}}$ | $f_{\text{OUT}} = 6997\text{ MHz}$                                                              | 57   |     | dBc  |
|                                                                |                                                                               | $f_{\text{OUT}} = 7997\text{ MHz}$ , $I_{\text{FS\_SWITCH}} = 41\text{ mA}$                     | 43   |     | dBc  |
|                                                                |                                                                               | $f_{\text{OUT}} = 7997\text{ MHz}$                                                              | 55   |     | dBc  |
|                                                                |                                                                               | $f_{\text{OUT}} = 8997\text{ MHz}$                                                              | 52   |     | dBc  |
|                                                                |                                                                               | $f_{\text{OUT}} = 10997\text{ MHz}$                                                             | 55   |     | dBc  |
| HD2                                                            | 2nd Harmonic Distortion in $F_{\text{DAC}}/2 - F_{\text{DAC}}$                | $f_{\text{OUT}} = 6997\text{ MHz}$                                                              | -61  |     | dBc  |
|                                                                |                                                                               | $f_{\text{OUT}} = 7997\text{ MHz}$ , $I_{\text{FS\_SWITCH}} = 41\text{ mA}$                     | -59  |     | dBc  |
|                                                                |                                                                               | $f_{\text{OUT}} = 7997\text{ MHz}$                                                              | -57  |     | dBc  |
|                                                                |                                                                               | $f_{\text{OUT}} = 8997\text{ MHz}$                                                              | -52  |     | dBc  |
|                                                                |                                                                               | $f_{\text{OUT}} = 10997\text{ MHz}$                                                             | -65  |     | dBc  |
| HD3                                                            | 3rd Harmonic Distortion in $F_{\text{DAC}}/2 - F_{\text{DAC}}$                | $f_{\text{OUT}} = 6997\text{ MHz}$                                                              | -57  |     | dBc  |
|                                                                |                                                                               | $f_{\text{OUT}} = 7997\text{ MHz}$ , $I_{\text{FS\_SWITCH}} = 41\text{ mA}$                     | -43  |     | dBc  |
|                                                                |                                                                               | $f_{\text{OUT}} = 7997\text{ MHz}$                                                              | -67  |     | dBc  |
|                                                                |                                                                               | $f_{\text{OUT}} = 8997\text{ MHz}$                                                              | -60  |     | dBc  |
|                                                                |                                                                               | $f_{\text{OUT}} = 10997\text{ MHz}$                                                             | -55  |     | dBc  |
| $\text{SFDR}_{\text{NONHD23}}$                                 | non-HD2/3 SFDR across $F_{\text{DAC}}/2 - F_{\text{DAC}}$                     | $f_{\text{OUT}} = 6997\text{ MHz}$                                                              | 78   |     | dBc  |
|                                                                |                                                                               | $f_{\text{OUT}} = 7997\text{ MHz}$ , $I_{\text{FS\_SWITCH}} = 41\text{ mA}$                     | 73   |     | dBc  |
|                                                                |                                                                               | $f_{\text{OUT}} = 7997\text{ MHz}$                                                              | 73   |     | dBc  |
|                                                                |                                                                               | $f_{\text{OUT}} = 8997\text{ MHz}$                                                              | 76   |     | dBc  |
|                                                                |                                                                               | $f_{\text{OUT}} = 10997\text{ MHz}$                                                             | 71   |     | dBc  |
| IMD3                                                           | Third-order two tone intermodulation distortion                               | $f_{\text{OUT}} = 6997 \pm 10\text{ MHz}$ , -7dBFS/tone                                         | -55  |     | dBc  |
|                                                                |                                                                               | $f_{\text{OUT}} = 7997 \pm 10\text{ MHz}$ , -7dBFS/tone, $I_{\text{FS\_SWITCH}} = 41\text{ mA}$ | -45  |     | dBc  |
|                                                                |                                                                               | $f_{\text{OUT}} = 7997 \pm 10\text{ MHz}$ , -7dBFS/tone                                         | -58  |     | dBc  |
|                                                                |                                                                               | $f_{\text{OUT}} = 8997 \pm 10\text{ MHz}$ , -7dBFS/tone                                         | -65  |     | dBc  |
|                                                                |                                                                               | $f_{\text{OUT}} = 10997 \pm 10\text{ MHz}$ , -7dBFS/tone                                        | -54  |     | dBc  |

## 6.6 Electrical Characteristics - AC Specifications (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , minimum and maximum values over operating free-air temperature range, typical supply voltages,  $F_{\text{CLK}} = 12\text{ GHz}$ , DDS Mode,  $I_{\text{FS\_SWITCH}} = 20.5\text{ mA}$ , single tone amplitude = 0 dBFS, SE DEM and Dither (DEM\_ADJ = 1 below 750 MHz and DEM\_ADJ = 0 above 750 MHz), unless otherwise noted.  $F_{\text{DAC}} = F_{\text{CLK}}$  in NRZ and RF modes and  $F_{\text{DAC}} = 2 \cdot F_{\text{CLK}}$  in DES2XL/H modes.

| PARAMETER |                                                                        | TEST CONDITIONS                                                                                                                                        | MIN | TYP  | MAX | UNIT    |
|-----------|------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------|-----|------|-----|---------|
| NSD       | Noise spectral density, large signal, sinusoidal output <sup>(3)</sup> | $f_{\text{OUT}} = 6997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$                                                                               |     | -146 |     | dBc/Hz  |
|           |                                                                        | $f_{\text{OUT}} = 7997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$ , $I_{\text{FS\_SWITCH}} = 41\text{ mA}$                                      |     | -146 |     | dBc/Hz  |
|           |                                                                        | $f_{\text{OUT}} = 7997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$                                                                               |     | -145 |     | dBc/Hz  |
|           |                                                                        | $f_{\text{OUT}} = 8997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$                                                                               |     | -144 |     | dBc/Hz  |
|           |                                                                        | $f_{\text{OUT}} = 10997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$                                                                              |     | -141 |     | dBc/Hz  |
| NSD       | Noise spectral density, small signal, sinusoidal output <sup>(3)</sup> | $A_{\text{OUT}} = -20\text{ dBFS}$ , $f_{\text{OUT}} = 6997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$                                          |     | -149 |     | dBFS/Hz |
|           |                                                                        | $A_{\text{OUT}} = -20\text{ dBFS}$ , $f_{\text{OUT}} = 7997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$ , $I_{\text{FS\_SWITCH}} = 41\text{ mA}$ |     | -151 |     | dBFS/Hz |
|           |                                                                        | $A_{\text{OUT}} = -20\text{ dBFS}$ , $f_{\text{OUT}} = 7997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$                                          |     | -149 |     | dBFS/Hz |
|           |                                                                        | $A_{\text{OUT}} = -20\text{ dBFS}$ , $f_{\text{OUT}} = 8997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$                                          |     | -148 |     | dBFS/Hz |
|           |                                                                        | $A_{\text{OUT}} = -20\text{ dBFS}$ , $f_{\text{OUT}} = 10997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$                                         |     | -146 |     | dBFS/Hz |
| FLATNESS  | Flatness of Nyquist zone                                               | Maximum output power to minimum output power, measured from 10% to 90% of 2nd Nyquist zone, including $\sin x/x$ response with balun                   |     | 2.4  |     | dB      |

## 6.6 Electrical Characteristics - AC Specifications (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , minimum and maximum values over operating free-air temperature range, typical supply voltages,  $F_{\text{CLK}} = 12\text{ GHz}$ , DDS Mode,  $I_{\text{FS\_SWITCH}} = 20.5\text{ mA}$ , single tone amplitude = 0 dBFS, SE DEM and Dither (DEM\_ADJ = 1 below 750 MHz and DEM\_ADJ = 0 above 750 MHz), unless otherwise noted.  $F_{\text{DAC}} = F_{\text{CLK}}$  in NRZ and RF modes and  $F_{\text{DAC}} = 2 \cdot F_{\text{CLK}}$  in DES2XL/H modes.

| PARAMETER                                                             |                                                                                                                            | TEST CONDITIONS                     | MIN | TYP  | MAX | UNIT |
|-----------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------|-------------------------------------|-----|------|-----|------|
| <b>24 GSPS, DUAL or SINGLE CHANNEL MODE, DDS Mode, DES2XL/H MODES</b> |                                                                                                                            |                                     |     |      |     |      |
| $P_{\text{OUT}}$                                                      | Output power with 2:1 balun and 50 $\Omega$ load, $I_{\text{FS\_SWITCH}} = 20.5\text{ mA}$                                 | $f_{\text{OUT}} = 97\text{ MHz}$    |     | 1.0  |     | dBm  |
|                                                                       |                                                                                                                            | $f_{\text{OUT}} = 997\text{ MHz}$   |     | 0.7  |     | dBm  |
|                                                                       |                                                                                                                            | $f_{\text{OUT}} = 1997\text{ MHz}$  |     | 0.6  |     | dBm  |
|                                                                       |                                                                                                                            | $f_{\text{OUT}} = 2997\text{ MHz}$  |     | 0.4  |     | dBm  |
|                                                                       |                                                                                                                            | $f_{\text{OUT}} = 3997\text{ MHz}$  |     | -1.0 |     | dBm  |
|                                                                       |                                                                                                                            | $f_{\text{OUT}} = 5997\text{ MHz}$  |     | -1.3 |     | dBm  |
|                                                                       |                                                                                                                            | $f_{\text{OUT}} = 6997\text{ MHz}$  |     | -0.3 |     | dBm  |
|                                                                       |                                                                                                                            | $f_{\text{OUT}} = 7997\text{ MHz}$  |     | -1.1 |     | dBm  |
|                                                                       |                                                                                                                            | $f_{\text{OUT}} = 8997\text{ MHz}$  |     | -4.2 |     | dBm  |
|                                                                       |                                                                                                                            | $f_{\text{OUT}} = 10997\text{ MHz}$ |     | -8.4 |     | dBm  |
| $P_{\text{OUT}}$                                                      | Output power with 2:1 balun and 50 $\Omega$ load, $I_{\text{FS\_SWITCH}} = 41\text{ mA}$                                   | $f_{\text{OUT}} = 97\text{ MHz}$    |     | 7.1  |     | dBm  |
|                                                                       |                                                                                                                            | $f_{\text{OUT}} = 997\text{ MHz}$   |     | 6.7  |     | dBm  |
|                                                                       |                                                                                                                            | $f_{\text{OUT}} = 1997\text{ MHz}$  |     | 6.5  |     | dBm  |
|                                                                       |                                                                                                                            | $f_{\text{OUT}} = 2997\text{ MHz}$  |     | 6.2  |     | dBm  |
|                                                                       |                                                                                                                            | $f_{\text{OUT}} = 3997\text{ MHz}$  |     | 4.9  |     | dBm  |
|                                                                       |                                                                                                                            | $f_{\text{OUT}} = 5997\text{ MHz}$  |     | 4.5  |     | dBm  |
|                                                                       |                                                                                                                            | $f_{\text{OUT}} = 6997\text{ MHz}$  |     | 5.3  |     | dBm  |
|                                                                       |                                                                                                                            | $f_{\text{OUT}} = 7997\text{ MHz}$  |     | 4.3  |     | dBm  |
|                                                                       |                                                                                                                            | $f_{\text{OUT}} = 8997\text{ MHz}$  |     | 1.2  |     | dBm  |
|                                                                       |                                                                                                                            | $f_{\text{OUT}} = 10997\text{ MHz}$ |     | -3.1 |     | dBm  |
| SFDR                                                                  | Spurious free dynamic range (SFDR) across $0 - F_{\text{DAC}}/4$ , $I_{\text{FS\_SWITCH}} = 20.5\text{ mA}$                | $f_{\text{OUT}} = 97\text{ MHz}$    |     | 77   |     | dBc  |
|                                                                       |                                                                                                                            | $f_{\text{OUT}} = 997\text{ MHz}$   |     | 66   |     | dBc  |
|                                                                       |                                                                                                                            | $f_{\text{OUT}} = 1997\text{ MHz}$  |     | 64   |     | dBc  |
|                                                                       |                                                                                                                            | $f_{\text{OUT}} = 2997\text{ MHz}$  |     | 67   |     | dBc  |
|                                                                       |                                                                                                                            | $f_{\text{OUT}} = 3997\text{ MHz}$  |     | 74   |     | dBc  |
|                                                                       | Spurious free dynamic range (SFDR) across $F_{\text{DAC}}/4 - F_{\text{DAC}}/2$ , $I_{\text{FS\_SWITCH}} = 20.5\text{ mA}$ | $f_{\text{OUT}} = 5997\text{ MHz}$  |     | 71   |     | dBc  |
|                                                                       |                                                                                                                            | $f_{\text{OUT}} = 6997\text{ MHz}$  |     | 64   |     | dBc  |
|                                                                       |                                                                                                                            | $f_{\text{OUT}} = 7997\text{ MHz}$  |     | 56   |     | dBc  |
|                                                                       |                                                                                                                            | $f_{\text{OUT}} = 8997\text{ MHz}$  |     | 51   |     | dBc  |
|                                                                       |                                                                                                                            | $f_{\text{OUT}} = 10997\text{ MHz}$ |     | 55   |     | dBc  |
|                                                                       | Spurious free dynamic range (SFDR) across $0 - F_{\text{DAC}}/4$ , $I_{\text{FS\_SWITCH}} = 41\text{ mA}$                  | $f_{\text{OUT}} = 97\text{ MHz}$    |     | 71   |     | dBc  |
|                                                                       |                                                                                                                            | $f_{\text{OUT}} = 997\text{ MHz}$   |     | 50   |     | dBc  |
|                                                                       |                                                                                                                            | $f_{\text{OUT}} = 1997\text{ MHz}$  |     | 43   |     | dBc  |
|                                                                       |                                                                                                                            | $f_{\text{OUT}} = 2997\text{ MHz}$  |     | 57   |     | dBc  |
|                                                                       |                                                                                                                            | $f_{\text{OUT}} = 3997\text{ MHz}$  |     | 74   |     | dBc  |
|                                                                       | Spurious free dynamic range (SFDR) across $F_{\text{DAC}}/4 - F_{\text{DAC}}/2$ , $I_{\text{FS\_SWITCH}} = 41\text{ mA}$   | $f_{\text{OUT}} = 5997\text{ MHz}$  |     | 70   |     | dBc  |
|                                                                       |                                                                                                                            | $f_{\text{OUT}} = 6997\text{ MHz}$  |     | 63   |     | dBc  |
|                                                                       |                                                                                                                            | $f_{\text{OUT}} = 7997\text{ MHz}$  |     | 56   |     | dBc  |
|                                                                       |                                                                                                                            | $f_{\text{OUT}} = 8997\text{ MHz}$  |     | 50   |     | dBc  |
|                                                                       |                                                                                                                            | $f_{\text{OUT}} = 10997\text{ MHz}$ |     | 41   |     | dBc  |

## 6.6 Electrical Characteristics - AC Specifications (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , minimum and maximum values over operating free-air temperature range, typical supply voltages,  $F_{\text{CLK}} = 12\text{ GHz}$ , DDS Mode,  $I_{\text{FS\_SWITCH}} = 20.5\text{ mA}$ , single tone amplitude = 0 dBFS, SE DEM and Dither (DEM\_ADJ = 1 below 750 MHz and DEM\_ADJ = 0 above 750 MHz), unless otherwise noted.  $F_{\text{DAC}} = F_{\text{CLK}}$  in NRZ and RF modes and  $F_{\text{DAC}} = 2 \cdot F_{\text{CLK}}$  in DES2XL/H modes.

| PARAMETER          |                                                                                                                               | TEST CONDITIONS                     | MIN | TYP | MAX | UNIT |
|--------------------|-------------------------------------------------------------------------------------------------------------------------------|-------------------------------------|-----|-----|-----|------|
| IMG <sub>DES</sub> | $F_{\text{DAC}}/2 - F_{\text{OUT}}$ DES Image,<br>$I_{\text{FS\_SWITCH}} = 20.5\text{ mA}$                                    | $f_{\text{OUT}} = 97\text{ MHz}$    |     | -73 |     | dBc  |
|                    |                                                                                                                               | $f_{\text{OUT}} = 997\text{ MHz}$   |     | -64 |     | dBc  |
|                    |                                                                                                                               | $f_{\text{OUT}} = 1997\text{ MHz}$  |     | -58 |     | dBc  |
|                    |                                                                                                                               | $f_{\text{OUT}} = 2997\text{ MHz}$  |     | -51 |     | dBc  |
|                    |                                                                                                                               | $f_{\text{OUT}} = 3997\text{ MHz}$  |     | -46 |     | dBc  |
|                    |                                                                                                                               | $f_{\text{OUT}} = 5997\text{ MHz}$  |     | -45 |     | dBc  |
|                    |                                                                                                                               | $f_{\text{OUT}} = 6997\text{ MHz}$  |     | -34 |     | dBc  |
|                    |                                                                                                                               | $f_{\text{OUT}} = 7997\text{ MHz}$  |     | -38 |     | dBc  |
|                    |                                                                                                                               | $f_{\text{OUT}} = 8997\text{ MHz}$  |     | -33 |     | dBc  |
|                    |                                                                                                                               | $f_{\text{OUT}} = 10997\text{ MHz}$ |     | -29 |     | dBc  |
|                    | $F_{\text{DAC}}/2 - F_{\text{OUT}}$ DES Image,<br>$I_{\text{FS\_SWITCH}} = 41\text{ mA}$                                      | $f_{\text{OUT}} = 97\text{ MHz}$    |     | -92 |     | dBc  |
|                    |                                                                                                                               | $f_{\text{OUT}} = 997\text{ MHz}$   |     | -72 |     | dBc  |
|                    |                                                                                                                               | $f_{\text{OUT}} = 1997\text{ MHz}$  |     | -66 |     | dBc  |
|                    |                                                                                                                               | $f_{\text{OUT}} = 2997\text{ MHz}$  |     | -58 |     | dBc  |
|                    |                                                                                                                               | $f_{\text{OUT}} = 3997\text{ MHz}$  |     | -52 |     | dBc  |
|                    |                                                                                                                               | $f_{\text{OUT}} = 5997\text{ MHz}$  |     | -52 |     | dBc  |
|                    |                                                                                                                               | $f_{\text{OUT}} = 6997\text{ MHz}$  |     | -37 |     | dBc  |
|                    |                                                                                                                               | $f_{\text{OUT}} = 7997\text{ MHz}$  |     | -39 |     | dBc  |
|                    |                                                                                                                               | $f_{\text{OUT}} = 8997\text{ MHz}$  |     | -33 |     | dBc  |
|                    |                                                                                                                               | $f_{\text{OUT}} = 10997\text{ MHz}$ |     | -27 |     | dBc  |
| HD2                | Spurious free dynamic range (SFDR)<br>across $0 - F_{\text{DAC}}/4$ , $I_{\text{FS\_SWITCH}} = 20.5\text{ mA}$                | $f_{\text{OUT}} = 97\text{ MHz}$    |     | -77 |     | dBc  |
|                    |                                                                                                                               | $f_{\text{OUT}} = 997\text{ MHz}$   |     | -79 |     | dBc  |
|                    |                                                                                                                               | $f_{\text{OUT}} = 1997\text{ MHz}$  |     | -72 |     | dBc  |
|                    |                                                                                                                               | $f_{\text{OUT}} = 2997\text{ MHz}$  |     | -67 |     | dBc  |
|                    |                                                                                                                               | $f_{\text{OUT}} = 3997\text{ MHz}$  |     | -72 |     | dBc  |
|                    | Spurious free dynamic range (SFDR)<br>across $F_{\text{DAC}}/4 - F_{\text{DAC}}/2$ , $I_{\text{FS\_SWITCH}} = 20.5\text{ mA}$ | $f_{\text{OUT}} = 5997\text{ MHz}$  |     | -72 |     | dBc  |
|                    |                                                                                                                               | $f_{\text{OUT}} = 6997\text{ MHz}$  |     | -64 |     | dBc  |
|                    |                                                                                                                               | $f_{\text{OUT}} = 7997\text{ MHz}$  |     | -56 |     | dBc  |
|                    |                                                                                                                               | $f_{\text{OUT}} = 8997\text{ MHz}$  |     | -51 |     | dBc  |
|                    |                                                                                                                               | $f_{\text{OUT}} = 10997\text{ MHz}$ |     | -65 |     | dBc  |
|                    | Spurious free dynamic range (SFDR)<br>across $0 - F_{\text{DAC}}/4$ , $I_{\text{FS\_SWITCH}} = 41\text{ mA}$                  | $f_{\text{OUT}} = 97\text{ MHz}$    |     | -71 |     | dBc  |
|                    |                                                                                                                               | $f_{\text{OUT}} = 997\text{ MHz}$   |     | -75 |     | dBc  |
|                    |                                                                                                                               | $f_{\text{OUT}} = 1997\text{ MHz}$  |     | -69 |     | dBc  |
|                    |                                                                                                                               | $f_{\text{OUT}} = 2997\text{ MHz}$  |     | -57 |     | dBc  |
|                    |                                                                                                                               | $f_{\text{OUT}} = 3997\text{ MHz}$  |     | -76 |     | dBc  |
|                    | Spurious free dynamic range (SFDR)<br>across $F_{\text{DAC}}/4 - F_{\text{DAC}}/2$ , $I_{\text{FS\_SWITCH}} = 41\text{ mA}$   | $f_{\text{OUT}} = 5997\text{ MHz}$  |     | -72 |     | dBc  |
|                    |                                                                                                                               | $f_{\text{OUT}} = 6997\text{ MHz}$  |     | -65 |     | dBc  |
|                    |                                                                                                                               | $f_{\text{OUT}} = 7997\text{ MHz}$  |     | -57 |     | dBc  |
|                    |                                                                                                                               | $f_{\text{OUT}} = 8997\text{ MHz}$  |     | -51 |     | dBc  |
|                    |                                                                                                                               | $f_{\text{OUT}} = 10997\text{ MHz}$ |     | -63 |     | dBc  |

## 6.6 Electrical Characteristics - AC Specifications (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , minimum and maximum values over operating free-air temperature range, typical supply voltages,  $F_{\text{CLK}} = 12\text{ GHz}$ , DDS Mode,  $I_{\text{FS\_SWITCH}} = 20.5\text{ mA}$ , single tone amplitude = 0 dBFS, SE DEM and Dither (DEM\_ADJ = 1 below 750 MHz and DEM\_ADJ = 0 above 750 MHz), unless otherwise noted.  $F_{\text{DAC}} = F_{\text{CLK}}$  in NRZ and RF modes and  $F_{\text{DAC}} = 2 \cdot F_{\text{CLK}}$  in DES2XL/H modes.

| PARAMETER               |                                                                                                                            | TEST CONDITIONS                     | MIN | TYP | MAX | UNIT |
|-------------------------|----------------------------------------------------------------------------------------------------------------------------|-------------------------------------|-----|-----|-----|------|
| HD3                     | Spurious free dynamic range (SFDR) across $0 - F_{\text{DAC}}/4$ , $I_{\text{FS\_SWITCH}} = 20.5\text{ mA}$                | $f_{\text{OUT}} = 97\text{ MHz}$    |     | -88 |     | dBc  |
|                         |                                                                                                                            | $f_{\text{OUT}} = 997\text{ MHz}$   |     | -66 |     | dBc  |
|                         |                                                                                                                            | $f_{\text{OUT}} = 1997\text{ MHz}$  |     | -64 |     | dBc  |
|                         |                                                                                                                            | $f_{\text{OUT}} = 2997\text{ MHz}$  |     | -82 |     | dBc  |
|                         |                                                                                                                            | $f_{\text{OUT}} = 3997\text{ MHz}$  |     | -90 |     | dBc  |
|                         | Spurious free dynamic range (SFDR) across $F_{\text{DAC}}/4 - F_{\text{DAC}}/2$ , $I_{\text{FS\_SWITCH}} = 20.5\text{ mA}$ | $f_{\text{OUT}} = 5997\text{ MHz}$  |     | -85 |     | dBc  |
|                         |                                                                                                                            | $f_{\text{OUT}} = 6997\text{ MHz}$  |     | -80 |     | dBc  |
|                         |                                                                                                                            | $f_{\text{OUT}} = 7997\text{ MHz}$  |     | -85 |     | dBc  |
|                         |                                                                                                                            | $f_{\text{OUT}} = 8997\text{ MHz}$  |     | -69 |     | dBc  |
|                         | Spurious free dynamic range (SFDR) across $0 - F_{\text{DAC}}/4$ , $I_{\text{FS\_SWITCH}} = 41\text{ mA}$                  | $f_{\text{OUT}} = 97\text{ MHz}$    |     | -73 |     | dBc  |
|                         |                                                                                                                            | $f_{\text{OUT}} = 997\text{ MHz}$   |     | -50 |     | dBc  |
|                         |                                                                                                                            | $f_{\text{OUT}} = 1997\text{ MHz}$  |     | -44 |     | dBc  |
|                         |                                                                                                                            | $f_{\text{OUT}} = 2997\text{ MHz}$  |     | -76 |     | dBc  |
|                         | Spurious free dynamic range (SFDR) across $F_{\text{DAC}}/4 - F_{\text{DAC}}/2$ , $I_{\text{FS\_SWITCH}} = 41\text{ mA}$   | $f_{\text{OUT}} = 3997\text{ MHz}$  |     | -78 |     | dBc  |
|                         |                                                                                                                            | $f_{\text{OUT}} = 5997\text{ MHz}$  |     | -81 |     | dBc  |
|                         |                                                                                                                            | $f_{\text{OUT}} = 6997\text{ MHz}$  |     | -67 |     | dBc  |
|                         |                                                                                                                            | $f_{\text{OUT}} = 7997\text{ MHz}$  |     | -75 |     | dBc  |
|                         |                                                                                                                            | $f_{\text{OUT}} = 8997\text{ MHz}$  |     | -72 |     | dBc  |
| SFDR <sub>NONHD23</sub> | non-HD2/3 SFDR in $0 - F_{\text{DAC}}/4$ , $I_{\text{FS\_SWITCH}} = 20.5\text{ mA}$                                        | $f_{\text{OUT}} = 97\text{ MHz}$    |     | 93  |     | dBc  |
|                         |                                                                                                                            | $f_{\text{OUT}} = 997\text{ MHz}$   |     | 85  |     | dBc  |
|                         |                                                                                                                            | $f_{\text{OUT}} = 1997\text{ MHz}$  |     | 89  |     | dBc  |
|                         |                                                                                                                            | $f_{\text{OUT}} = 2997\text{ MHz}$  |     | 84  |     | dBc  |
|                         |                                                                                                                            | $f_{\text{OUT}} = 3997\text{ MHz}$  |     | 84  |     | dBc  |
|                         | non-HD2/3 SFDR in $F_{\text{DAC}}/4 - F_{\text{DAC}}/2$ , $I_{\text{FS\_SWITCH}} = 20.5\text{ mA}$                         | $f_{\text{OUT}} = 5997\text{ MHz}$  |     | 82  |     | dBc  |
|                         |                                                                                                                            | $f_{\text{OUT}} = 6997\text{ MHz}$  |     | 79  |     | dBc  |
|                         |                                                                                                                            | $f_{\text{OUT}} = 7997\text{ MHz}$  |     | 77  |     | dBc  |
|                         |                                                                                                                            | $f_{\text{OUT}} = 8997\text{ MHz}$  |     | 77  |     | dBc  |
|                         | non-HD2/3 SFDR in $0 - F_{\text{DAC}}/4$ , $I_{\text{FS\_SWITCH}} = 41\text{ mA}$                                          | $f_{\text{OUT}} = 10997\text{ MHz}$ |     | 70  |     | dBc  |
|                         |                                                                                                                            | $f_{\text{OUT}} = 97\text{ MHz}$    |     | 87  |     | dBc  |
|                         |                                                                                                                            | $f_{\text{OUT}} = 997\text{ MHz}$   |     | 70  |     | dBc  |
|                         |                                                                                                                            | $f_{\text{OUT}} = 1997\text{ MHz}$  |     | 86  |     | dBc  |
|                         | non-HD2/3 SFDR in $F_{\text{DAC}}/4 - F_{\text{DAC}}/2$ , $I_{\text{FS\_SWITCH}} = 41\text{ mA}$                           | $f_{\text{OUT}} = 2997\text{ MHz}$  |     | 79  |     | dBc  |
|                         |                                                                                                                            | $f_{\text{OUT}} = 3997\text{ MHz}$  |     | 77  |     | dBc  |
|                         |                                                                                                                            | $f_{\text{OUT}} = 5997\text{ MHz}$  |     | 77  |     | dBc  |
|                         |                                                                                                                            | $f_{\text{OUT}} = 6997\text{ MHz}$  |     | 75  |     | dBc  |
|                         |                                                                                                                            | $f_{\text{OUT}} = 7997\text{ MHz}$  |     | 67  |     | dBc  |
|                         |                                                                                                                            | $f_{\text{OUT}} = 8997\text{ MHz}$  |     | 75  |     | dBc  |
|                         |                                                                                                                            | $f_{\text{OUT}} = 10997\text{ MHz}$ |     | 60  |     | dBc  |

## 6.6 Electrical Characteristics - AC Specifications (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , minimum and maximum values over operating free-air temperature range, typical supply voltages,  $F_{\text{CLK}} = 12\text{ GHz}$ , DDS Mode,  $I_{\text{FS\_SWITCH}} = 20.5\text{ mA}$ , single tone amplitude = 0 dBFS, SE DEM and Dither (DEM\_ADJ = 1 below 750 MHz and DEM\_ADJ = 0 above 750 MHz), unless otherwise noted.  $F_{\text{DAC}} = F_{\text{CLK}}$  in NRZ and RF modes and  $F_{\text{DAC}} = 2 \cdot F_{\text{CLK}}$  in DES2XL/H modes.

| PARAMETER |                                                                                                                  | TEST CONDITIONS                                                           | MIN | TYP  | MAX | UNIT   |
|-----------|------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------|-----|------|-----|--------|
| IMD3      | Third-order two tone intermodulation distortion, $I_{\text{FS\_SWITCH}} = 20.5\text{ mA}$                        | $f_{\text{OUT}} = 97 \pm 10\text{ MHz}$ , -7dBFS/tone                     |     | -100 |     | dBc    |
|           |                                                                                                                  | $f_{\text{OUT}} = 997 \pm 10\text{ MHz}$ , -7dBFS/tone                    |     | -74  |     | dBc    |
|           |                                                                                                                  | $f_{\text{OUT}} = 1997 \pm 10\text{ MHz}$ , -7dBFS/tone                   |     | -75  |     | dBc    |
|           |                                                                                                                  | $f_{\text{OUT}} = 2997 \pm 10\text{ MHz}$ , -7dBFS/tone                   |     | -74  |     | dBc    |
|           |                                                                                                                  | $f_{\text{OUT}} = 3997 \pm 10\text{ MHz}$ , -7dBFS/tone                   |     | -67  |     | dBc    |
|           |                                                                                                                  | $f_{\text{OUT}} = 5997 \pm 10\text{ MHz}$ , -7dBFS/tone                   |     | -64  |     | dBc    |
|           |                                                                                                                  | $f_{\text{OUT}} = 6997 \pm 10\text{ MHz}$ , -7dBFS/tone                   |     | -55  |     | dBc    |
|           |                                                                                                                  | $f_{\text{OUT}} = 7997 \pm 10\text{ MHz}$ , -7dBFS/tone                   |     | -58  |     | dBc    |
|           |                                                                                                                  | $f_{\text{OUT}} = 8997 \pm 10\text{ MHz}$ , -7dBFS/tone                   |     | -64  |     | dBc    |
|           |                                                                                                                  | $f_{\text{OUT}} = 10997 \pm 10\text{ MHz}$ , -7dBFS/tone                  |     | -55  |     | dBc    |
|           | Third-order two tone intermodulation distortion, $I_{\text{FS\_SWITCH}} = 41\text{ mA}$                          | $f_{\text{OUT}} = 97 \pm 10\text{ MHz}$ , -7dBFS/tone                     |     | -87  |     | dBc    |
|           |                                                                                                                  | $f_{\text{OUT}} = 997 \pm 10\text{ MHz}$ , -7dBFS/tone                    |     | -61  |     | dBc    |
|           |                                                                                                                  | $f_{\text{OUT}} = 1997 \pm 10\text{ MHz}$ , -7dBFS/tone                   |     | -53  |     | dBc    |
|           |                                                                                                                  | $f_{\text{OUT}} = 2997 \pm 10\text{ MHz}$ , -7dBFS/tone                   |     | -55  |     | dBc    |
|           |                                                                                                                  | $f_{\text{OUT}} = 3997 \pm 10\text{ MHz}$ , -7dBFS/tone                   |     | -56  |     | dBc    |
|           |                                                                                                                  | $f_{\text{OUT}} = 5997 \pm 10\text{ MHz}$ , -7dBFS/tone                   |     | -54  |     | dBc    |
|           |                                                                                                                  | $f_{\text{OUT}} = 6997 \pm 10\text{ MHz}$ , -7dBFS/tone                   |     | -40  |     | dBc    |
|           |                                                                                                                  | $f_{\text{OUT}} = 7997 \pm 10\text{ MHz}$ , -7dBFS/tone                   |     | -41  |     | dBc    |
|           |                                                                                                                  | $f_{\text{OUT}} = 8997 \pm 10\text{ MHz}$ , -7dBFS/tone                   |     | -44  |     | dBc    |
|           |                                                                                                                  | $f_{\text{OUT}} = 10997 \pm 10\text{ MHz}$ , -7dBFS/tone                  |     | -46  |     | dBc    |
| NSD       | Noise spectral density, large signal, sinusoidal output, $I_{\text{FS\_SWITCH}} = 20.5\text{ mA}$ <sup>(3)</sup> | $f_{\text{OUT}} = 97\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$    |     | -157 |     | dBc/Hz |
|           |                                                                                                                  | $f_{\text{OUT}} = 997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$   |     | -155 |     | dBc/Hz |
|           |                                                                                                                  | $f_{\text{OUT}} = 1997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$  |     | -152 |     | dBc/Hz |
|           |                                                                                                                  | $f_{\text{OUT}} = 2997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$  |     | -151 |     | dBc/Hz |
|           |                                                                                                                  | $f_{\text{OUT}} = 3997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$  |     | -149 |     | dBc/Hz |
|           |                                                                                                                  | $f_{\text{OUT}} = 5997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$  |     | -148 |     | dBc/Hz |
|           |                                                                                                                  | $f_{\text{OUT}} = 6997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$  |     | -146 |     | dBc/Hz |
|           |                                                                                                                  | $f_{\text{OUT}} = 7997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$  |     | -146 |     | dBc/Hz |
|           |                                                                                                                  | $f_{\text{OUT}} = 8997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$  |     | -144 |     | dBc/Hz |
|           |                                                                                                                  | $f_{\text{OUT}} = 10997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$ |     | -140 |     | dBc/Hz |

## 6.6 Electrical Characteristics - AC Specifications (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , minimum and maximum values over operating free-air temperature range, typical supply voltages,  $F_{\text{CLK}} = 12\text{ GHz}$ , DDS Mode,  $I_{\text{FS\_SWITCH}} = 20.5\text{ mA}$ , single tone amplitude = 0 dBFS, SE DEM and Dither (DEM\_ADJ = 1 below 750 MHz and DEM\_ADJ = 0 above 750 MHz), unless otherwise noted.  $F_{\text{DAC}} = F_{\text{CLK}}$  in NRZ and RF modes and  $F_{\text{DAC}} = 2 \cdot F_{\text{CLK}}$  in DES2XL/H modes.

| PARAMETER |                                                                                                                  | TEST CONDITIONS                                                                                                | MIN | TYP  | MAX | UNIT    |
|-----------|------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------|-----|------|-----|---------|
| NSD       | Noise spectral density, large signal, sinusoidal output, $I_{\text{FS\_SWITCH}} = 41\text{ mA}$ <sup>(3)</sup>   | $f_{\text{OUT}} = 97\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$                                         |     | -157 |     | dBc/Hz  |
|           |                                                                                                                  | $f_{\text{OUT}} = 997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$                                        |     | -156 |     | dBc/Hz  |
|           |                                                                                                                  | $f_{\text{OUT}} = 1997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$                                       |     | -153 |     | dBc/Hz  |
|           |                                                                                                                  | $f_{\text{OUT}} = 2997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$                                       |     | -151 |     | dBc/Hz  |
|           |                                                                                                                  | $f_{\text{OUT}} = 3997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$                                       |     | -150 |     | dBc/Hz  |
|           |                                                                                                                  | $f_{\text{OUT}} = 5997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$                                       |     | -148 |     | dBc/Hz  |
|           |                                                                                                                  | $f_{\text{OUT}} = 6997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$                                       |     | -147 |     | dBc/Hz  |
|           |                                                                                                                  | $f_{\text{OUT}} = 7997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$                                       |     | -146 |     | dBc/Hz  |
|           |                                                                                                                  | $f_{\text{OUT}} = 8997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$                                       |     | -144 |     | dBc/Hz  |
|           |                                                                                                                  | $f_{\text{OUT}} = 10997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$                                      |     | -140 |     | dBc/Hz  |
| NSD       | Noise spectral density, small signal, sinusoidal output, $I_{\text{FS\_SWITCH}} = 20.5\text{ mA}$ <sup>(3)</sup> | $A_{\text{OUT}} = -20\text{ dBFS}$ , $f_{\text{OUT}} = 97\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$    |     | -155 |     | dBFS/Hz |
|           |                                                                                                                  | $A_{\text{OUT}} = -20\text{ dBFS}$ , $f_{\text{OUT}} = 997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$   |     | -157 |     | dBFS/Hz |
|           |                                                                                                                  | $A_{\text{OUT}} = -20\text{ dBFS}$ , $f_{\text{OUT}} = 1997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$  |     | -155 |     | dBFS/Hz |
|           |                                                                                                                  | $A_{\text{OUT}} = -20\text{ dBFS}$ , $f_{\text{OUT}} = 2997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$  |     | -153 |     | dBFS/Hz |
|           |                                                                                                                  | $A_{\text{OUT}} = -20\text{ dBFS}$ , $f_{\text{OUT}} = 3997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$  |     | -153 |     | dBFS/Hz |
|           |                                                                                                                  | $A_{\text{OUT}} = -20\text{ dBFS}$ , $f_{\text{OUT}} = 5997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$  |     | -151 |     | dBFS/Hz |
|           |                                                                                                                  | $A_{\text{OUT}} = -20\text{ dBFS}$ , $f_{\text{OUT}} = 6997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$  |     | -150 |     | dBFS/Hz |
|           |                                                                                                                  | $A_{\text{OUT}} = -20\text{ dBFS}$ , $f_{\text{OUT}} = 7997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$  |     | -150 |     | dBFS/Hz |
|           |                                                                                                                  | $A_{\text{OUT}} = -20\text{ dBFS}$ , $f_{\text{OUT}} = 8997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$  |     | -149 |     | dBFS/Hz |
|           |                                                                                                                  | $A_{\text{OUT}} = -20\text{ dBFS}$ , $f_{\text{OUT}} = 10997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$ |     | -146 |     | dBFS/Hz |

## 6.6 Electrical Characteristics - AC Specifications (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , minimum and maximum values over operating free-air temperature range, typical supply voltages,  $F_{\text{CLK}} = 12\text{ GHz}$ , DDS Mode,  $I_{\text{FS\_SWITCH}} = 20.5\text{ mA}$ , single tone amplitude = 0 dBFS, SE DEM and Dither (DEM\_ADJ = 1 below 750 MHz and DEM\_ADJ = 0 above 750 MHz), unless otherwise noted.  $F_{\text{DAC}} = F_{\text{CLK}}$  in NRZ and RF modes and  $F_{\text{DAC}} = 2 \cdot F_{\text{CLK}}$  in DES2XL/H modes.

| PARAMETER |                                                                                                                | TEST CONDITIONS                                                                                                | MIN | TYP  | MAX | UNIT    |
|-----------|----------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------|-----|------|-----|---------|
| NSD       | Noise spectral density, small signal, sinusoidal output, $I_{\text{FS\_SWITCH}} = 41\text{ mA}$ <sup>(3)</sup> | $A_{\text{OUT}} = -20\text{ dBFS}$ , $f_{\text{OUT}} = 97\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$    |     | -156 |     | dBFS/Hz |
|           |                                                                                                                | $A_{\text{OUT}} = -20\text{ dBFS}$ , $f_{\text{OUT}} = 997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$   |     | -158 |     | dBFS/Hz |
|           |                                                                                                                | $A_{\text{OUT}} = -20\text{ dBFS}$ , $f_{\text{OUT}} = 1997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$  |     | -156 |     | dBFS/Hz |
|           |                                                                                                                | $A_{\text{OUT}} = -20\text{ dBFS}$ , $f_{\text{OUT}} = 2997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$  |     | -155 |     | dBFS/Hz |
|           |                                                                                                                | $A_{\text{OUT}} = -20\text{ dBFS}$ , $f_{\text{OUT}} = 3997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$  |     | -153 |     | dBFS/Hz |
|           |                                                                                                                | $A_{\text{OUT}} = -20\text{ dBFS}$ , $f_{\text{OUT}} = 5997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$  |     | -152 |     | dBFS/Hz |
|           |                                                                                                                | $A_{\text{OUT}} = -20\text{ dBFS}$ , $f_{\text{OUT}} = 6997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$  |     | -152 |     | dBFS/Hz |
|           |                                                                                                                | $A_{\text{OUT}} = -20\text{ dBFS}$ , $f_{\text{OUT}} = 7997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$  |     | -152 |     | dBFS/Hz |
|           |                                                                                                                | $A_{\text{OUT}} = -20\text{ dBFS}$ , $f_{\text{OUT}} = 8997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$  |     | -151 |     | dBFS/Hz |
|           |                                                                                                                | $A_{\text{OUT}} = -20\text{ dBFS}$ , $f_{\text{OUT}} = 10997\text{ MHz}$ , 70-MHz offset from $f_{\text{OUT}}$ |     | -150 |     | dBFS/Hz |
| PN        | Additive DAC phase noise, external clock contribution subtracted out, DES mode, DEM and Dither off             | $f_{\text{CLK}} = 12\text{ GHz}$ , $f_{\text{OUT}} = 997\text{ MHz}$ , 100 Hz offset                           |     | -128 |     | dBc/Hz  |
|           |                                                                                                                | $f_{\text{CLK}} = 12\text{ GHz}$ , $f_{\text{OUT}} = 997\text{ MHz}$ , 1 KHz offset                            |     | -137 |     | dBc/Hz  |
|           |                                                                                                                | $f_{\text{CLK}} = 12\text{ GHz}$ , $f_{\text{OUT}} = 997\text{ MHz}$ , 10 kHz offset                           |     | -148 |     | dBc/Hz  |
|           |                                                                                                                | $f_{\text{CLK}} = 12\text{ GHz}$ , $f_{\text{OUT}} = 997\text{ MHz}$ , 100 kHz offset                          |     | -158 |     | dBc/Hz  |
|           |                                                                                                                | $f_{\text{CLK}} = 12\text{ GHz}$ , $f_{\text{OUT}} = 997\text{ MHz}$ , 1 MHz offset                            |     | -166 |     | dBc/Hz  |
|           |                                                                                                                | $f_{\text{CLK}} = 12\text{ GHz}$ , $f_{\text{OUT}} = 997\text{ MHz}$ , 10 MHz offset                           |     | -167 |     | dBc/Hz  |
|           |                                                                                                                | $f_{\text{CLK}} = 12\text{ GHz}$ , $f_{\text{OUT}} = 997\text{ MHz}$ , 100 MHz offset                          |     | -170 |     | dBc/Hz  |
| PN        | Additive DAC phase noise, external clock contribution subtracted out, DES mode, DEM and Dither off             | $f_{\text{CLK}} = 8\text{ GHz}$ , $f_{\text{OUT}} = 997\text{ MHz}$ , 100 Hz offset                            |     | -127 |     | dBc/Hz  |
|           |                                                                                                                | $f_{\text{CLK}} = 8\text{ GHz}$ , $f_{\text{OUT}} = 997\text{ MHz}$ , 1 KHz offset                             |     | -136 |     | dBc/Hz  |
|           |                                                                                                                | $f_{\text{CLK}} = 8\text{ GHz}$ , $f_{\text{OUT}} = 997\text{ MHz}$ , 10 kHz offset                            |     | -147 |     | dBc/Hz  |
|           |                                                                                                                | $f_{\text{CLK}} = 8\text{ GHz}$ , $f_{\text{OUT}} = 997\text{ MHz}$ , 100 kHz offset                           |     | -157 |     | dBc/Hz  |
|           |                                                                                                                | $f_{\text{CLK}} = 8\text{ GHz}$ , $f_{\text{OUT}} = 997\text{ MHz}$ , 1 MHz offset                             |     | -165 |     | dBc/Hz  |
|           |                                                                                                                | $f_{\text{CLK}} = 8\text{ GHz}$ , $f_{\text{OUT}} = 997\text{ MHz}$ , 10 MHz offset                            |     | -167 |     | dBc/Hz  |
|           |                                                                                                                | $f_{\text{CLK}} = 8\text{ GHz}$ , $f_{\text{OUT}} = 997\text{ MHz}$ , 100 MHz offset                           |     | -169 |     | dBc/Hz  |

(1) Measured single ended into 50Ω load

- (2) A  $100\Omega$  load is equivalent to a 2:1 with  $50\Omega$  single ended load
- (3) NSD can be improved by disabling DEM and DITHER.

## 6.7 Electrical Characteristics - Power Consumption

Typical values at  $T_A = +25^\circ\text{C}$ , minimum and maximum values over operating free-air temperature range, typical supply voltages, 2 channels, DDS Mode,  $F_{\text{CLK}} = 12\text{ GHz}$ ,  $F_{\text{OUT}} = 2997\text{ MHz}$ , NRZ mode,  $I_{\text{FSSWITCH}} = 20.5\text{ mA}$ , unless otherwise noted.

| PARAMETER           |                                                                 | TEST CONDITIONS                                                                                                                                                                                         | MIN | TYP  | MAX | UNIT |
|---------------------|-----------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|------|-----|------|
| $I_{\text{VDDA18}}$ | 1.8-V combined supply current for VDDA18A and VDDA18B           | Power Mode 1: Dual DACs, 1 DUC shared to both DACs, DDS Mode, $F_{\text{DAC}} = 12\text{ GSPS}$ , $F_{\text{OUT}} = 2997\text{ MHz}$ , NRZ mode (dual channel version only)                             |     | 86   |     | mA   |
| $I_{\text{VDDIO}}$  | 1.8-V supply current for VDDIO                                  |                                                                                                                                                                                                         |     | 1    |     |      |
| $I_{\text{VDDCSR}}$ | 1.8-V combined supply current for VDDCLK18, VDDSYS18 and VDDR18 |                                                                                                                                                                                                         |     | 92   |     |      |
| $I_{\text{VDDL}}$   | 1.0-V combined supply current for VDDLb, VDDLd                  |                                                                                                                                                                                                         |     | 363  |     |      |
| $I_{\text{VDDCLK}}$ | 1.0-V supply current for VDDCLK10                               |                                                                                                                                                                                                         |     | 569  |     |      |
| $I_{\text{DVDD}}$   | 1.0-V supply current for VDDDIG, VDDT, VDDEB and VDDEA          |                                                                                                                                                                                                         |     | 1356 |     |      |
| $I_{\text{VEE}}$    | –1.8-V combined supply current for VEEAM18 and VEEBM18          |                                                                                                                                                                                                         |     | 123  |     |      |
| $P_{\text{DIS}}$    | Total power dissipation                                         |                                                                                                                                                                                                         |     | 2831 |     | mW   |
| $I_{\text{VDDA18}}$ | 1.8-V combined supply current for VDDA18A and VDDA18B           | Power Mode 2: Dual DACs, 1 DUC per DAC, DDS Mode, $F_{\text{DAC}} = 12\text{ GSPS}$ , $F_{\text{OUT1}} = 2997\text{ MHz}$ , $F_{\text{OUT2}} = 3997\text{ MHz}$ , NRZ mode (dual channel version only)  |     | 86   |     | mA   |
| $I_{\text{VDDIO}}$  | 1.8-V supply current for VDDIO                                  |                                                                                                                                                                                                         |     | 1    |     |      |
| $I_{\text{VDDCSR}}$ | 1.8-V combined supply current for VDDCLK18, VDDSYS18 and VDDR18 |                                                                                                                                                                                                         |     | 92   |     |      |
| $I_{\text{VDDL}}$   | 1.0-V combined supply current for VDDLb, VDDLd                  |                                                                                                                                                                                                         |     | 366  |     |      |
| $I_{\text{VDDCLK}}$ | 1.0-V supply current for VDDCLK10                               |                                                                                                                                                                                                         |     | 569  |     |      |
| $I_{\text{DVDD}}$   | 1.0-V supply current for VDDDIG, VDDT, VDDEB and VDDEA          |                                                                                                                                                                                                         |     | 1529 |     |      |
| $I_{\text{VEE}}$    | –1.8-V combined supply current for VEEAM18 and VEEBM18          |                                                                                                                                                                                                         |     | 123  |     |      |
| $P_{\text{DIS}}$    | Total power dissipation                                         |                                                                                                                                                                                                         |     | 3007 |     | mW   |
| $I_{\text{VDDA18}}$ | 1.8-V combined supply current for VDDA18A and VDDA18B           | Power Mode 3: Dual DACs, 2 DUCs per DAC, DDS Mode, $F_{\text{DAC}} = 12\text{ GSPS}$ , $F_{\text{OUT1}} = 2997\text{ MHz}$ , $F_{\text{OUT2}} = 3997\text{ MHz}$ , NRZ mode (dual channel version only) |     | 86   |     | mA   |
| $I_{\text{VDDIO}}$  | 1.8-V supply current for VDDIO                                  |                                                                                                                                                                                                         |     | 1    |     |      |
| $I_{\text{VDDCSR}}$ | 1.8-V combined supply current for VDDCLK18, VDDSYS18 and VDDR18 |                                                                                                                                                                                                         |     | 93   |     |      |
| $I_{\text{VDDL}}$   | 1.0-V combined supply current for VDDLb, VDDLd                  |                                                                                                                                                                                                         |     | 365  |     |      |
| $I_{\text{VDDCLK}}$ | 1.0-V supply current for VDDCLK10                               |                                                                                                                                                                                                         |     | 570  |     |      |
| $I_{\text{DVDD}}$   | 1.0-V supply current for VDDDIG, VDDT, VDDEB and VDDEA          |                                                                                                                                                                                                         |     | 1756 |     |      |
| $I_{\text{VEE}}$    | –1.8-V combined supply current for VEEAM18 and VEEBM18          |                                                                                                                                                                                                         |     | 123  |     |      |
| $P_{\text{DIS}}$    | Total power dissipation                                         |                                                                                                                                                                                                         |     | 3235 |     | mW   |

## 6.7 Electrical Characteristics - Power Consumption (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , minimum and maximum values over operating free-air temperature range, typical supply voltages, 2 channels, DDS Mode,  $F_{\text{CLK}} = 12\text{ GHz}$ ,  $F_{\text{OUT}} = 2997\text{ MHz}$ , NRZ mode,  $I_{\text{FSSWITCH}} = 20.5\text{ mA}$ , unless otherwise noted.

| PARAMETER           |                                                                 | TEST CONDITIONS                                                                                                                                                                                                           | MIN | TYP  | MAX | UNIT |
|---------------------|-----------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|------|-----|------|
| $I_{\text{VDDA18}}$ | 1.8-V combined supply current for VDDA18A and VDDA18B           | Power Mode 4: Dual DACs, 2 DUCs per DAC, JMODE 6, 64x interpolation, $F_{\text{DAC}} = 12\text{ GSPS}$ , $F_{\text{OUT1}} = 2997\text{ MHz}$ , $F_{\text{OUT2}} = 3997\text{ MHz}$ , NRZ mode (dual channel version only) |     | 86   |     | mA   |
| $I_{\text{VDDIO}}$  | 1.8-V supply current for VDDIO                                  |                                                                                                                                                                                                                           |     | 1    |     |      |
| $I_{\text{VDDCSR}}$ | 1.8-V combined supply current for VDDCLK18, VDDSYS18 and VDDR18 |                                                                                                                                                                                                                           |     | 112  |     |      |
| $I_{\text{VDDL}}$   | 1.0-V combined supply current for VDDLb, VDDLdA                 |                                                                                                                                                                                                                           |     | 355  |     |      |
| $I_{\text{VDDCLK}}$ | 1.0-V supply current for VDDCLK10                               |                                                                                                                                                                                                                           |     | 571  |     |      |
| $I_{\text{DVDD}}$   | 1.0-V supply current for VDDDIG, VDDT, VDDEB and VDDEA          |                                                                                                                                                                                                                           |     | 2734 |     |      |
| $I_{\text{VEE}}$    | –1.8-V combined supply current for VEEAM18 and VEEBM18          |                                                                                                                                                                                                                           |     | 123  |     |      |
| $P_{\text{DIS}}$    | Total power dissipation                                         |                                                                                                                                                                                                                           |     | 4238 |     | mW   |
| $I_{\text{VDDA18}}$ | 1.8-V combined supply current for VDDA18A and VDDA18B           | Power Mode 5: Single channel device (DDS39RFS12), 1 DUC, DDS Mode, $F_{\text{DAC}} = 12\text{ GSPS}$ , $F_{\text{OUT}} = 2997\text{ MHz}$ , DES mode                                                                      |     | 58   |     | mA   |
| $I_{\text{VDDIO}}$  | 1.8-V supply current for VDDIO                                  |                                                                                                                                                                                                                           |     | 1    |     |      |
| $I_{\text{VDDCSR}}$ | 1.8-V combined supply current for VDDCLK18, VDDSYS18 and VDDR18 |                                                                                                                                                                                                                           |     | 93   |     |      |
| $I_{\text{VDDL}}$   | 1.0-V combined supply current for VDDLb, VDDLdA                 |                                                                                                                                                                                                                           |     | 182  |     |      |
| $I_{\text{VDDCLK}}$ | 1.0-V supply current for VDDCLK10                               |                                                                                                                                                                                                                           |     | 353  |     |      |
| $I_{\text{DVDD}}$   | 1.0-V supply current for VDDDIG, VDDT, VDDEB and VDDEA          |                                                                                                                                                                                                                           |     | 896  |     |      |
| $I_{\text{VEE}}$    | –1.8-V combined supply current for VEEAM18 and VEEBM18          |                                                                                                                                                                                                                           |     | 71   |     |      |
| $P_{\text{DIS}}$    | Total power dissipation                                         |                                                                                                                                                                                                                           |     | 1837 |     | mW   |
| $I_{\text{VDDA18}}$ | 1.8-V combined supply current for VDDA18A and VDDA18B           | Power Mode 6: Single channel device (DDS39RFS12), 2 DUCs, DDS Mode, $F_{\text{DAC}} = 12\text{ GSPS}$ , $F_{\text{OUT}} = 2997\text{ MHz}$ , NRZ mode                                                                     |     | 58   |     | mA   |
| $I_{\text{VDDIO}}$  | 1.8-V supply current for VDDIO                                  |                                                                                                                                                                                                                           |     | 1    |     |      |
| $I_{\text{VDDCSR}}$ | 1.8-V combined supply current for VDDCLK18, VDDSYS18 and VDDR18 |                                                                                                                                                                                                                           |     | 93   |     |      |
| $I_{\text{VDDL}}$   | 1.0-V combined supply current for VDDLb, VDDLdA                 |                                                                                                                                                                                                                           |     | 183  |     |      |
| $I_{\text{VDDCLK}}$ | 1.0-V supply current for VDDCLK10                               |                                                                                                                                                                                                                           |     | 353  |     |      |
| $I_{\text{DVDD}}$   | 1.0-V supply current for VDDDIG, VDDT, VDDEB and VDDEA          |                                                                                                                                                                                                                           |     | 1048 |     |      |
| $I_{\text{VEE}}$    | –1.8-V combined supply current for VEEAM18 and VEEBM18          |                                                                                                                                                                                                                           |     | 71   |     |      |
| $P_{\text{DIS}}$    | Total power dissipation                                         |                                                                                                                                                                                                                           |     | 1985 |     | mW   |

## 6.7 Electrical Characteristics - Power Consumption (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , minimum and maximum values over operating free-air temperature range, typical supply voltages, 2 channels, DDS Mode,  $F_{CLK} = 12\text{ GHz}$ ,  $F_{OUT} = 2997\text{ MHz}$ , NRZ mode,  $I_{FSSWITCH} = 20.5\text{ mA}$ , unless otherwise noted.

| PARAMETER    |                                                                 | TEST CONDITIONS                                                                                                                                                         | MIN | TYP  | MAX | UNIT |
|--------------|-----------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|------|-----|------|
| $I_{VDDA18}$ | 1.8-V combined supply current for VDDA18A and VDDA18B           | Power Mode 7: Single channel device (DDS39RFS12), 4 DUCS, DDS Mode, $F_{DAC} = 12\text{ GSPS}$ , $F_{OUT1} = 2997\text{ MHz}$ , $F_{OUT2} = 3997\text{ MHz}$ , NRZ mode |     | 58   |     | mA   |
| $I_{VDDIO}$  | 1.8-V supply current for VDDIO                                  |                                                                                                                                                                         |     | 1    |     |      |
| $I_{VDDCSR}$ | 1.8-V combined supply current for VDDCLK18, VDDSYS18 and VDDR18 |                                                                                                                                                                         |     | 93   |     |      |
| $I_{VDDL}$   | 1.0-V combined supply current for VDDLb, VDDL A                 |                                                                                                                                                                         |     | 182  |     |      |
| $I_{VDDCLK}$ | 1.0-V supply current for VDDCLK10                               |                                                                                                                                                                         |     | 354  |     |      |
| $I_{DVDD}$   | 1.0-V supply current for VDDDIG, VDDT, VDDEB and VDDEA          |                                                                                                                                                                         |     | 1255 |     |      |
| $I_{VEE}$    | –1.8-V combined supply current for VEEAM18 and VEEBM18          |                                                                                                                                                                         |     | 71   |     |      |
| $P_{DIS}$    | Total power dissipation                                         |                                                                                                                                                                         |     | 2192 |     | mW   |
| $I_{VDDA18}$ | 1.8-V combined supply current for VDDA18A and VDDA18B           | Power Mode 8: Single channel device (DDS39RFS12), 4 DUCs, JMODE 7, 64x Interpolation, $F_{DAC} = 24\text{ GSPS}$ , $F_{OUT} = 7997\text{ MHz}$ , DES mode               |     | 58   |     | mA   |
| $I_{VDDIO}$  | 1.8-V supply current for VDDIO                                  |                                                                                                                                                                         |     | 1    |     |      |
| $I_{VDDCSR}$ | 1.8-V combined supply current for VDDCLK18, VDDSYS18 and VDDR18 |                                                                                                                                                                         |     | 112  |     |      |
| $I_{VDDL}$   | 1.0-V combined supply current for VDDLb, VDDL A                 |                                                                                                                                                                         |     | 178  |     |      |
| $I_{VDDCLK}$ | 1.0-V supply current for VDDCLK10                               |                                                                                                                                                                         |     | 354  |     |      |
| $I_{DVDD}$   | 1.0-V supply current for VDDDIG, VDDT, VDDEB and VDDEA          |                                                                                                                                                                         |     | 2150 |     |      |
| $I_{VEE}$    | –1.8-V combined supply current for VEEAM18 and VEEBM18          |                                                                                                                                                                         |     | 70   |     |      |
| $P_{DIS}$    | Total power dissipation                                         |                                                                                                                                                                         |     | 3118 |     | mW   |
| $P_{DIS}$    | Total power dissipation                                         | Power Mode 14: Sleep, MODE[1:0] = 0b11.                                                                                                                                 |     | 171  |     | mW   |

## 6.8 Timing Requirements

Typical values at  $T_A = +25^\circ\text{C}$ , minimum and maximum values over operating free-air temperature range, typical supply voltages,  $f_{\text{CLK}} = 12\text{ GHz}$ ,  $I_{\text{FS\_SWITCH}} = 20.5\text{ mA}$ , single tone amplitude = 0 dBFS, Dither and DEM enabled, unless otherwise noted.

|                                  |                                                                                                                                                                     | MIN                                                              | NOM   | MAX                                    | UNIT                 |
|----------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------|-------|----------------------------------------|----------------------|
| <b>INPUT CLOCK (CLK+, CLK-)</b>  |                                                                                                                                                                     |                                                                  |       |                                        |                      |
| $f_{\text{CLK}}$                 | Input clock frequency                                                                                                                                               | 800                                                              |       | 12000                                  | MHz                  |
| <b>SYSREF (SYSREF+, SYSREF-)</b> |                                                                                                                                                                     |                                                                  |       |                                        |                      |
| $t_{\text{SYSREF\_LOW}}$         | SYSREF Low Timing                                                                                                                                                   |                                                                  |       | $5 \cdot t_{\text{CLK}} + 1\text{ ns}$ |                      |
| $t_{\text{SYSREF\_HIGH}}$        | SYSREF High Timing                                                                                                                                                  |                                                                  |       | $5 \cdot t_{\text{CLK}} + 1\text{ ns}$ |                      |
| $t_{\text{INV(SYSREF)}}$         | Width of invalid SYSREF capture region of $\text{CLK}\pm$ period, indicating setup or hold time violation, as measured by SYSREF_POS status register <sup>(1)</sup> |                                                                  | 13    |                                        | ps                   |
| $t_{\text{INV(TEMP)}}$           | Drift of invalid SYSREF capture region over temperature, positive number indicates a shift toward MSB of SYSREF_POS register                                        |                                                                  | -0.05 |                                        | ps/ $^\circ\text{C}$ |
| $t_{\text{INV(VA11)}}$           | Drift of invalid SYSREF capture region over VDDSYS18 supply voltage, positive number indicates a shift toward MSB of SYSREF_POS register                            |                                                                  | 0.19  |                                        | ps/mV                |
| $t_{\text{STEP(SP)}}$            | Delay of SYSREF_POS LSB                                                                                                                                             | SYSREF_ZOOM = 0                                                  |       | 20                                     | ps                   |
|                                  |                                                                                                                                                                     | SYSREF_ZOOM = 1                                                  |       | 9                                      |                      |
| $\text{DC(SYSREF)}$              | SYSREF duty cycle (asserted) when using a periodic SYSREF signal                                                                                                    | SYSREF duty cycle (asserted) when using a periodic SYSREF signal |       | 50% 55%                                |                      |
| $t_{\text{(PH\_SYS)}}$           | Minimum SYSREF $\pm$ assertion duration after SYSREF $\pm$ rising edge event                                                                                        |                                                                  | 8     |                                        | ns                   |
| <b>RESET</b>                     |                                                                                                                                                                     |                                                                  |       |                                        |                      |
| $t_{\text{RESET}}$               | Minimum RESET pulse width                                                                                                                                           |                                                                  | 100   |                                        | ns                   |
| <b>TXENABLE</b>                  |                                                                                                                                                                     |                                                                  |       |                                        |                      |
| $t_{\text{TXENABLE\_LOW}}$       | TXENABLE Low Time                                                                                                                                                   |                                                                  | 102   |                                        | clock cycles         |

- (1) Use SYSREF\_POS to select an optimal SYSREF\_SEL value for the SYSREF capture, see the [SYSREF Position Detector](#) section for more information on SYSREF windowing. The invalid region, specified by  $t_{\text{INV(SYSREF)}}$ , indicates the portion of the  $\text{CLK}\pm$  period( $t_{\text{CLK}}$ ), as measured by SYSREF\_SEL, that may result in a setup and hold violation. Verify that the timing skew between SYSREF $\pm$  and  $\text{CLK}\pm$  over system operating conditions from the nominal conditions (that used to find optimal SYSREF\_SEL) does not result in the invalid region occurring at the selected SYSREF\_SEL position in SYSREF\_POS, otherwise a temperature dependent SYSREF\_SEL selection may be needed to track the skew between  $\text{CLK}\pm$  and SYSREF $\pm$ .

## 6.9 Switching Characteristics

Typical values at  $T_A = +25^\circ\text{C}$ , minimum and maximum values over operating free-air temperature range, typical supply voltages,  $f_{\text{CLK}} = 12\text{ GHz}$ ,  $I_{\text{FS\_SWITCH}} = 20.5\text{ mA}$ , single tone amplitude = 0 dBFS, Dither and DEM enabled, unless otherwise noted.

| PARAMETER                                   |                                                                | TEST CONDITIONS                                                | MIN                   | TYP    | MAX        | UNIT |
|---------------------------------------------|----------------------------------------------------------------|----------------------------------------------------------------|-----------------------|--------|------------|------|
| JESD204C SERDES INTERFACE 6SRX-/+, 14SRX-/+ |                                                                |                                                                |                       |        |            |      |
| f <sub>SERDES</sub>                         | SERDES bit rate <sup>(4)</sup>                                 |                                                                | .78125                |        | 12.8       | Gbps |
| UI                                          | Unit Interval                                                  |                                                                | 78.125                |        | 1280       | ps   |
| LATENCY                                     |                                                                |                                                                |                       |        |            |      |
| T <sub>DAC</sub>                            | DAC clock period                                               |                                                                | 1 / f <sub>CLK</sub>  |        |            | s    |
| t <sub>PD(RX)</sub>                         | Serdes RX analog propagation delay                             | Serdes RX analog propagation delay                             | 215                   |        |            | ps   |
| t <sub>PDI</sub>                            | Input clock rising edge cross-over to output sample cross-over | Input clock rising edge cross-over to output sample cross-over | 500                   |        |            | ps   |
| t <sub>DACLAT</sub>                         | Digital path latency from SYSREF rising edge to DAC output     |                                                                | See XLS Calculator    |        |            |      |
| t <sub>RELEASE</sub>                        | Latency from SYSREF rising edge to elastic buffer release      |                                                                | See XLS Calculator    |        |            |      |
| t <sub>RXIN</sub>                           | Latency from SERDES Input to elastic buffer release            |                                                                | See XLS Calculator    |        |            |      |
| t <sub>TXEN_OUTPUT</sub>                    | TXENABLE rising edge to data output of DAC                     | FAST_TX_EN = 0                                                 | varies <sup>(1)</sup> |        | CLK Cycles |      |
|                                             |                                                                | FAST_TX_EN=1 and QUIET_TX_DISABLE=0                            | 93                    |        |            |      |
|                                             |                                                                | FAST_TX_EN=1 and QUIET_TX_DISABLE=1                            | 133                   |        |            |      |
| t <sub>TXEN_MUTE</sub>                      | TXENABLE falling edge to DAC output muted                      | QUIET_TX_DISABLE=0                                             | 93                    |        |            |      |
|                                             |                                                                | QUIET_TX_DISABLE=1                                             | 133                   |        |            |      |
| t <sub>TXEN_PW</sub>                        | Required TXENABLE pulse width                                  | FAST_TX_EN = 0 <sup>(2)</sup>                                  | 102                   |        |            |      |
|                                             |                                                                | FAST_TX_EN = 1 <sup>(3)</sup>                                  | 20                    |        |            |      |
| SERIAL PROGRAMMING INTERFACE                |                                                                |                                                                |                       |        |            |      |
| F <sub>s_c</sub>                            | serial clock frequency                                         |                                                                |                       | 15.625 |            | MHz  |
| F <sub>s_cts</sub>                          | serial clock frequency temp sensor                             | TS_TEMP register read                                          |                       | 1      |            | MHz  |
| t <sub>P</sub>                              | serial clock period                                            |                                                                | 64                    |        |            | ns   |
| t <sub>PH</sub>                             | serial clock pulse width high                                  |                                                                | 32                    |        |            | ns   |
| t <sub>PL</sub>                             | serial clock pulse width low                                   |                                                                | 32                    |        |            | ns   |
| t <sub>SU</sub>                             | SDI setup time                                                 |                                                                | 30                    |        |            | ns   |
| t <sub>H</sub>                              | SDI hold time                                                  |                                                                | 3                     |        |            | ns   |
| t <sub>IZ</sub>                             | SDI TRI-STATE                                                  |                                                                |                       | 3      |            | ns   |
| t <sub>ODZ</sub>                            | SDO driven to TRI-STATE                                        | 200 fF load                                                    |                       | 5      |            | ns   |
| t <sub>OZD</sub>                            | SDO TRI-STATE to driven                                        | 200 fF load                                                    |                       | 3      |            | ns   |
| t <sub>OD</sub>                             | SDO output delay                                               | 200 fF load                                                    |                       | 3      |            | ns   |
| t <sub>CSS</sub>                            | SCS setup                                                      |                                                                | 30                    |        |            | ns   |
| t <sub>CSH</sub>                            | SCS hold                                                       |                                                                | 3                     |        |            | ns   |
| t <sub>RS</sub>                             | RESET setup to serial clock                                    | RESET high                                                     | 30                    |        |            | ns   |
| t <sub>RH</sub>                             | RESET hold to serial clock                                     | RESET high                                                     | 30                    |        |            | ns   |
| t <sub>IAG</sub>                            | Inter-access gap                                               |                                                                | 30                    |        |            | ns   |
| FAST RECONFIGURATION (FR) INTERFACE         |                                                                |                                                                |                       |        |            |      |
| F <sub>FRCLK</sub>                          | FRCLK frequency                                                |                                                                |                       | 200    |            | MHz  |
| t <sub>FRCLK_P</sub>                        | FRCLK period                                                   |                                                                | 5                     |        |            | ns   |
| t <sub>FRCLK_PH</sub>                       | FRCLK pulse width high                                         |                                                                | 2                     |        |            | ns   |

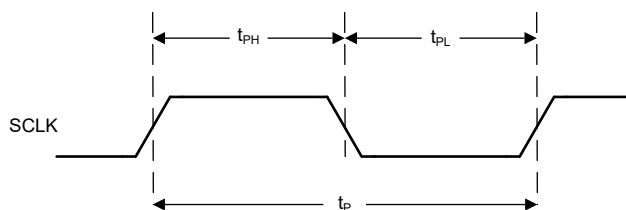
## 6.9 Switching Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , minimum and maximum values over operating free-air temperature range, typical supply voltages,  $f_{\text{CLK}} = 12\text{ GHz}$ ,  $I_{\text{FS\_SWITCH}} = 20.5\text{ mA}$ , single tone amplitude = 0 dBFS, Dither and DEM enabled, unless otherwise noted.

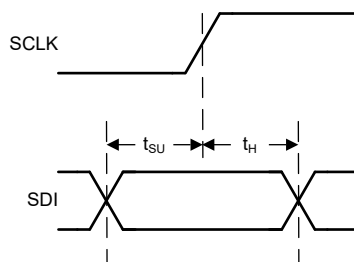
| PARAMETER              |                       | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|-----------------------|-----------------|-----|-----|-----|------|
| $t_{\text{FRCLK\_PL}}$ | FRCLK pulse width low |                 | 2   |     |     | ns   |
| $t_{\text{FRDI\_SU}}$  | FRDI setup time       |                 | 1   |     |     | ns   |
| $t_{\text{FRDI\_H}}$   | FRDI hold time        |                 | 1   |     |     | ns   |
| $t_{\text{FRCS\_SU}}$  | FRCS setup time       |                 | 1   |     |     | ns   |
| $t_{\text{FRCS\_H}}$   | FRCS hold time        |                 | 1   |     |     | ns   |
| $t_{\text{FR\_IAG}}$   | Inter-access gap      |                 | 1   |     |     | ns   |

- (1) The delay depends on how long it takes the JESD link to start up and the mode dependent device latency. Add the link layer startup time and the mode dependent latency ( $T_{\text{DAC\_LAT}}$ ) from the latency calculator spreadsheet.
- (2) Pulse durations less than this produce undefined behavior.
- (3) Pulse durations less than this may have no effect on the output.
- (4) 8b/10b encoding required for < 2 Gbps

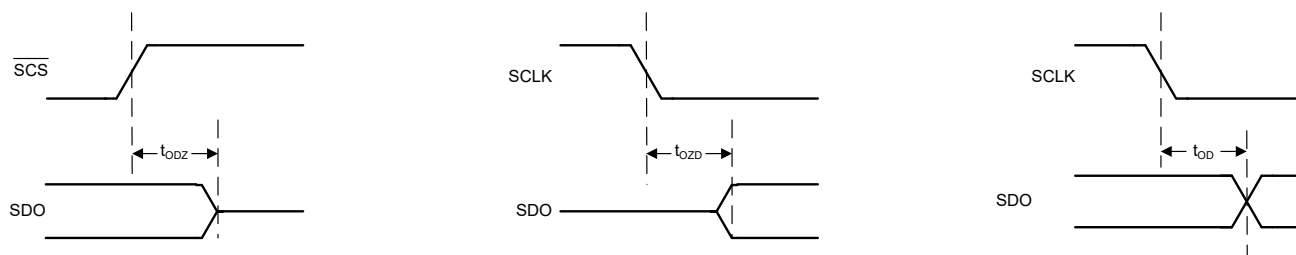
## 6.10 SPI and FRI Timing Diagrams



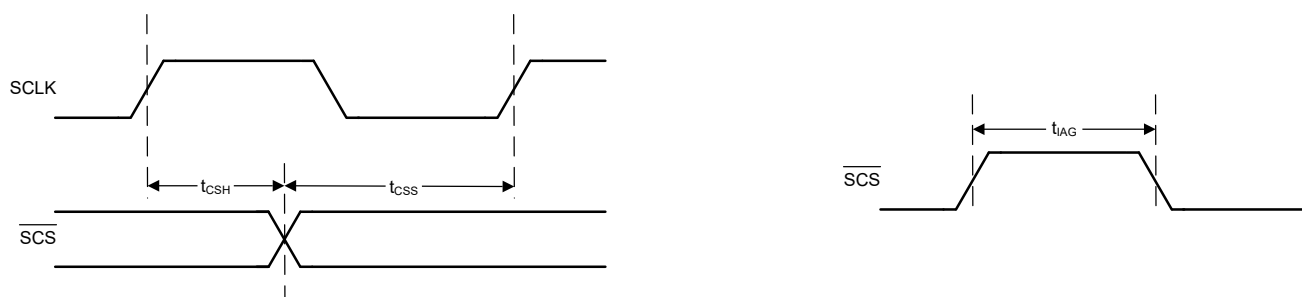
**Figure 6-1. SPI Clock Timing Diagram**



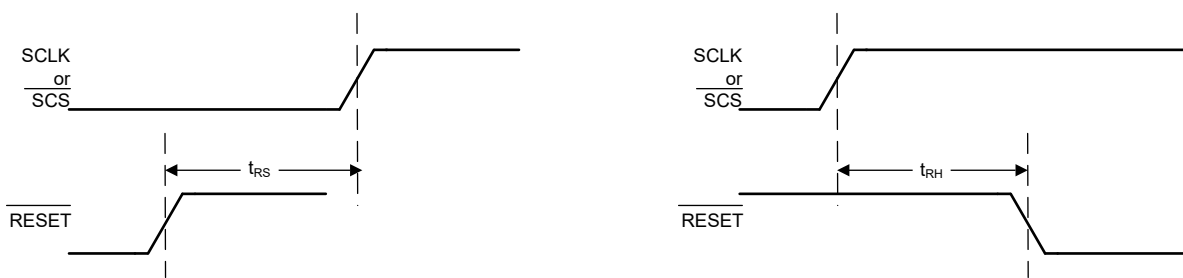
**Figure 6-2. SPI Data Input Timing Diagram**



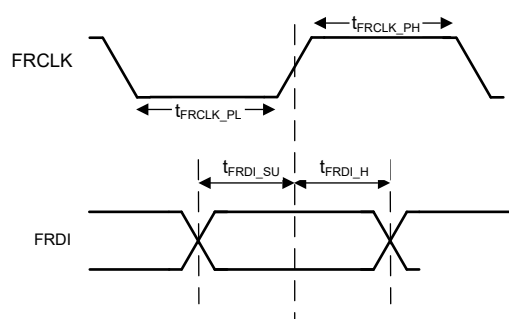
**Figure 6-3. SPI Data Output Timing Diagram**



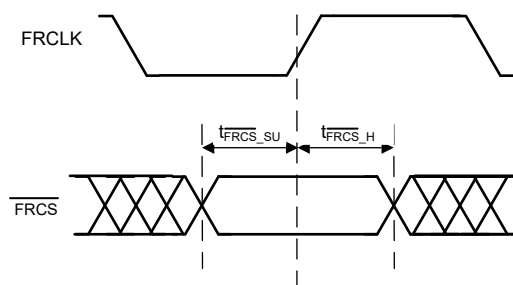
**Figure 6-4. SPI Chip Select Timing Diagram**



**Figure 6-5. RESET Timing Diagram**



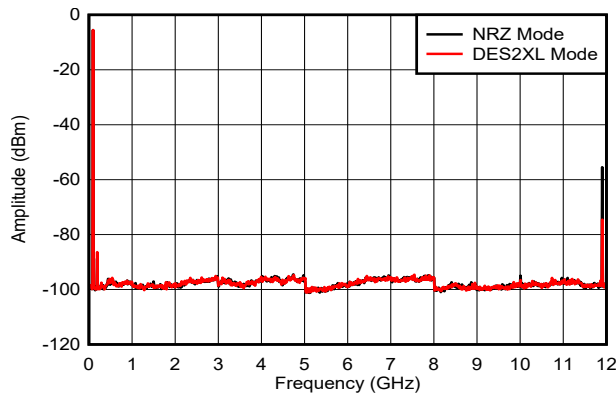
**Figure 6-6. FRDI Timing Diagram**



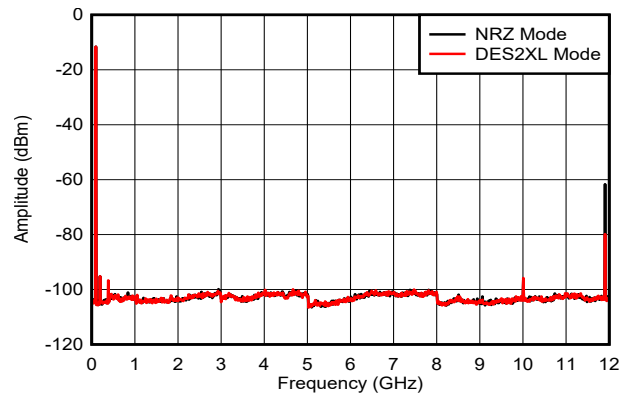
**Figure 6-7.  $\overline{\text{FRCS}}$  Timing Diagram**

## 6.11 Typical Characteristics: Single Tone Spectra

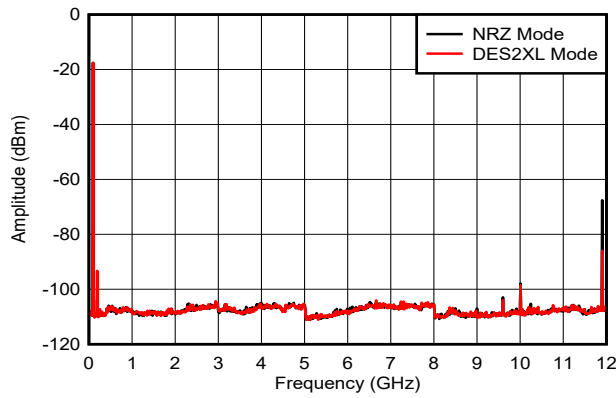
Typical values at  $T_A = +25^\circ\text{C}$ , minimum and maximum values over operating free-air temperature range, typical supply voltages,  $f_{\text{CLK}} = 12\text{GHz}$ ,  $I_{\text{FS\_SWITCH}} = 20.5\text{mA}$ , Dither and DEM enabled, unless otherwise noted.



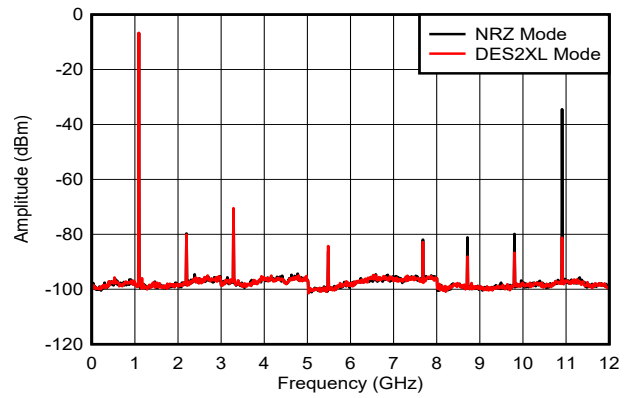
**Figure 6-8.  $f_{\text{OUT}} = 97\text{MHz}$ , 0dBFS**



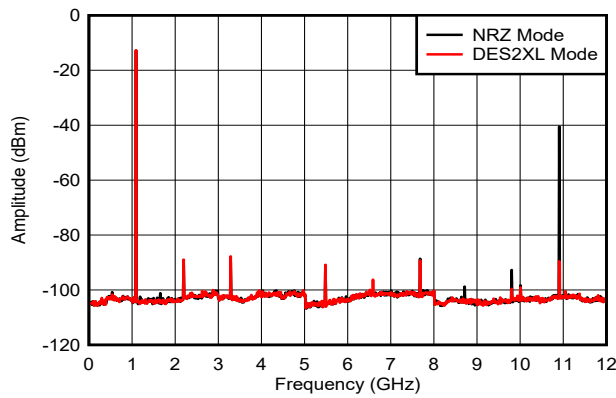
**Figure 6-9.  $f_{\text{OUT}} = 97\text{MHz}$ , -6dBFS**



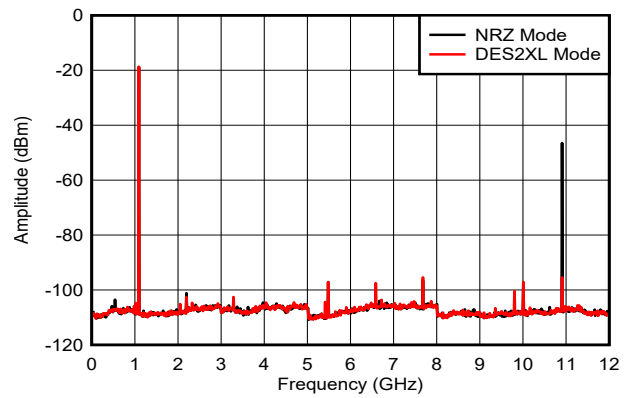
**Figure 6-10.  $f_{\text{OUT}} = 97\text{MHz}$ , -12dBFS**



**Figure 6-11.  $f_{\text{OUT}} = 1097\text{MHz}$ , 0dBFS**



**Figure 6-12.  $f_{\text{OUT}} = 1097\text{MHz}$ , -6dBFS**



**Figure 6-13.  $f_{\text{OUT}} = 1097\text{MHz}$ , -12dBFS**

## 6.11 Typical Characteristics: Single Tone Spectra (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , minimum and maximum values over operating free-air temperature range, typical supply voltages,  $f_{\text{CLK}} = 12\text{GHz}$ ,  $I_{\text{FS\_SWITCH}} = 20.5\text{mA}$ , Dither and DEM enabled, unless otherwise noted.

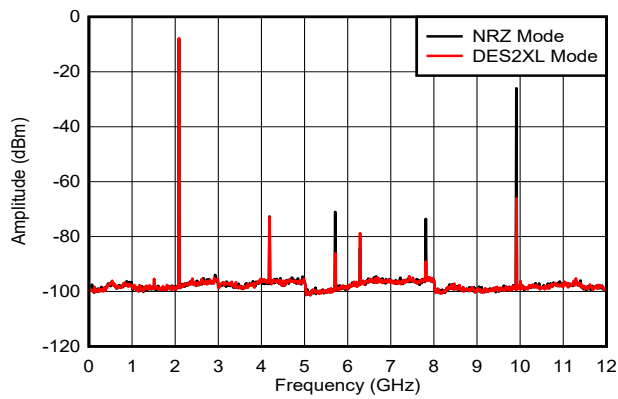


Figure 6-14.  $f_{\text{OUT}} = 2097\text{MHz}$ , 0dBFS

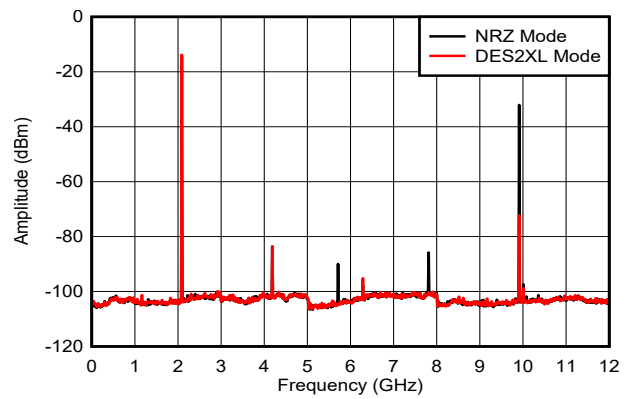


Figure 6-15.  $f_{\text{OUT}} = 2097\text{MHz}$ , -6dBFS

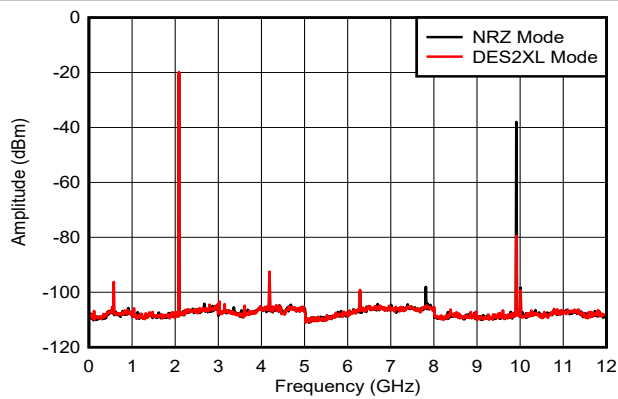


Figure 6-16.  $f_{\text{OUT}} = 2097\text{MHz}$ , -12dBFS

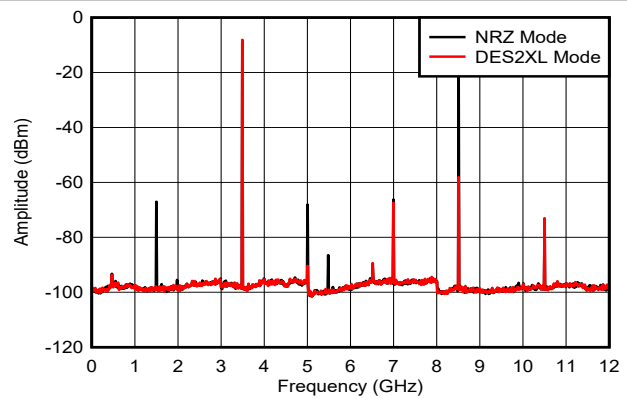


Figure 6-17.  $f_{\text{OUT}} = 3497\text{MHz}$ , 0dBFS

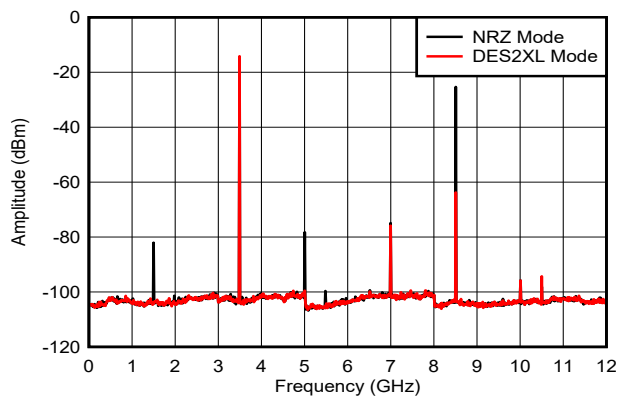


Figure 6-18.  $f_{\text{OUT}} = 3497\text{MHz}$ , -6dBFS

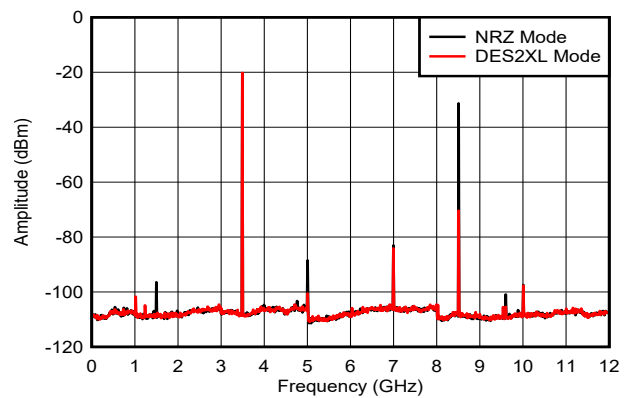
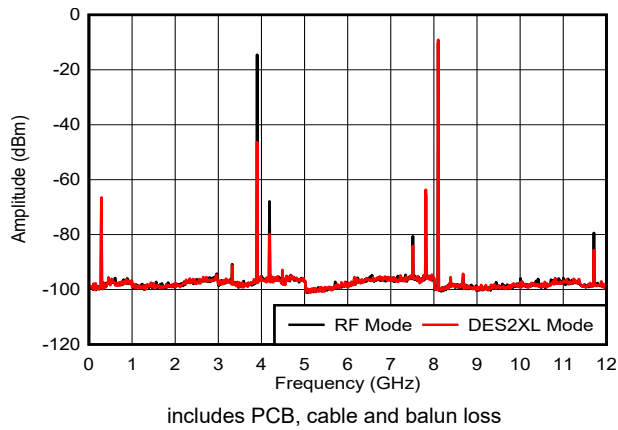


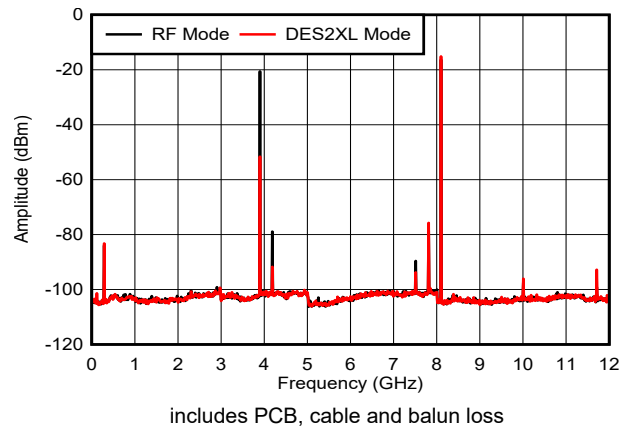
Figure 6-19.  $f_{\text{OUT}} = 3497\text{MHz}$ , -12dBFS

## 6.11 Typical Characteristics: Single Tone Spectra (continued)

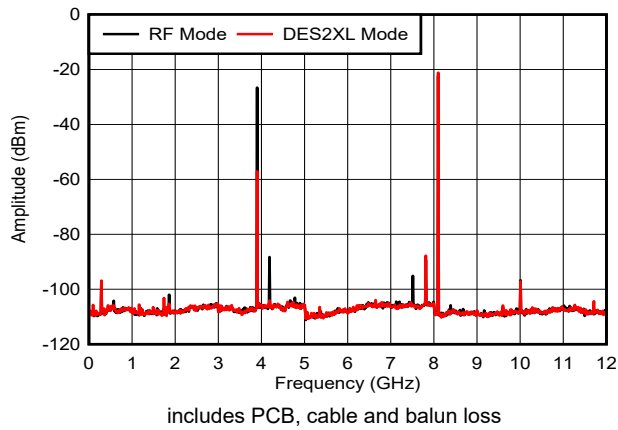
Typical values at  $T_A = +25^\circ\text{C}$ , minimum and maximum values over operating free-air temperature range, typical supply voltages,  $f_{\text{CLK}} = 12\text{GHz}$ ,  $I_{\text{FS\_SWITCH}} = 20.5\text{mA}$ , Dither and DEM enabled, unless otherwise noted.



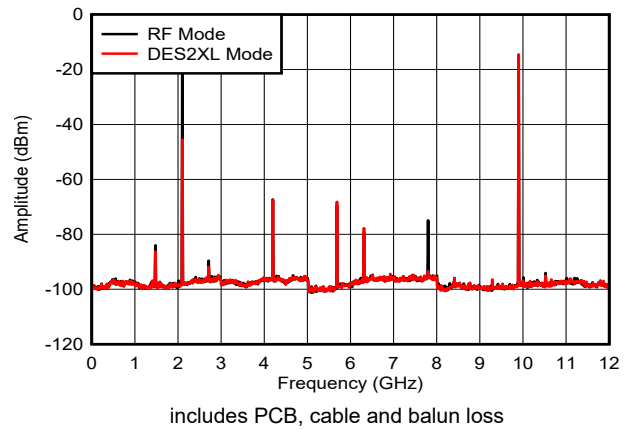
**Figure 6-20.  $f_{\text{OUT}} = 8097\text{MHz}$ , 0dBFS**



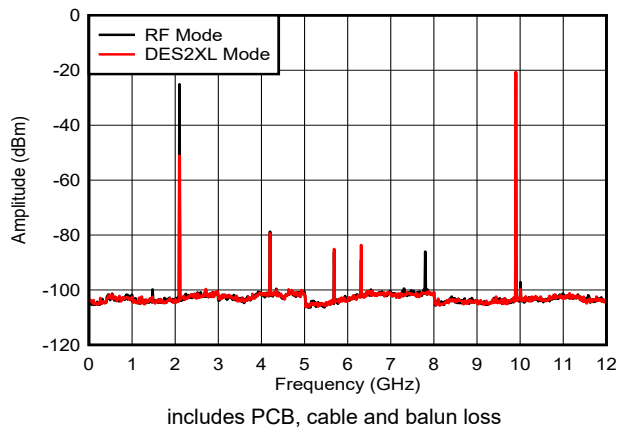
**Figure 6-21.  $f_{\text{OUT}} = 8097\text{MHz}$ , -6dBFS**



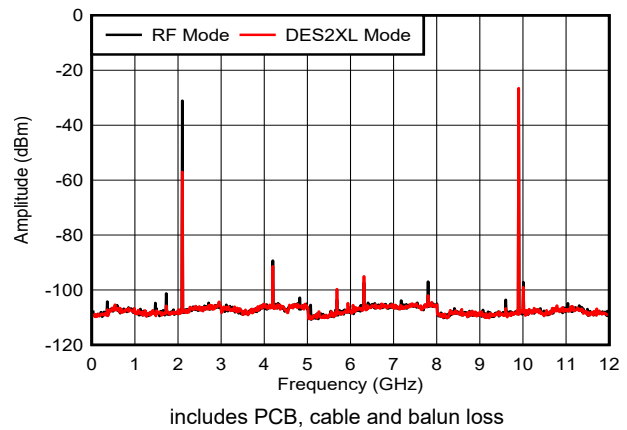
**Figure 6-22.  $f_{\text{OUT}} = 8097\text{MHz}$ , -12dBFS**



**Figure 6-23.  $f_{\text{OUT}} = 9897\text{MHz}$ , 0dBFS**



**Figure 6-24.  $f_{\text{OUT}} = 9897\text{MHz}$ , -6dBFS**



**Figure 6-25.  $f_{\text{OUT}} = 9897\text{MHz}$ , -12dBFS**

## 6.12 Typical Characteristics: Dual Tone Spectra

Typical values at  $T_A = +25^\circ\text{C}$ , minimum and maximum values over operating free-air temperature range, typical supply voltages,  $f_{\text{CLK}} = 10.24\text{GHz}$ ,  $I_{\text{FS\_SWITCH}} = 20.5\text{mA}$ , Dither and DEM enabled, unless otherwise noted.

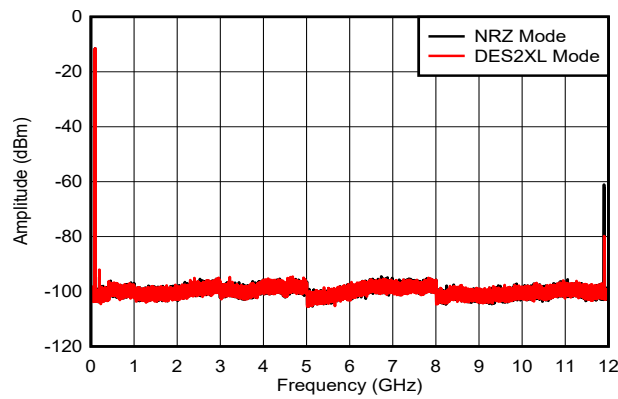


Figure 6-26. Dual Tone,  $f_{\text{OUT}} = 97\text{MHz}$ , 0dBFS

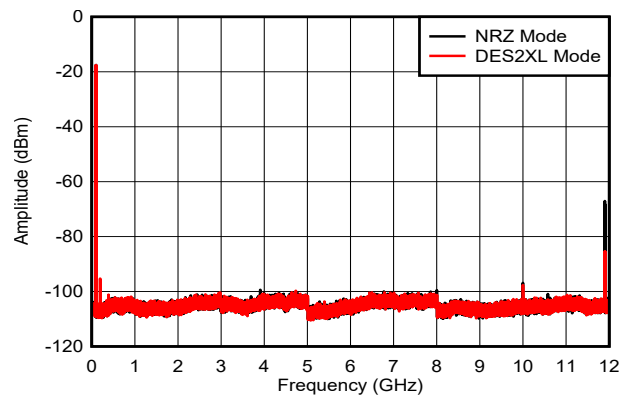


Figure 6-27. Dual Tone,  $f_{\text{OUT}} = 97\text{MHz}$ , -6dBFS

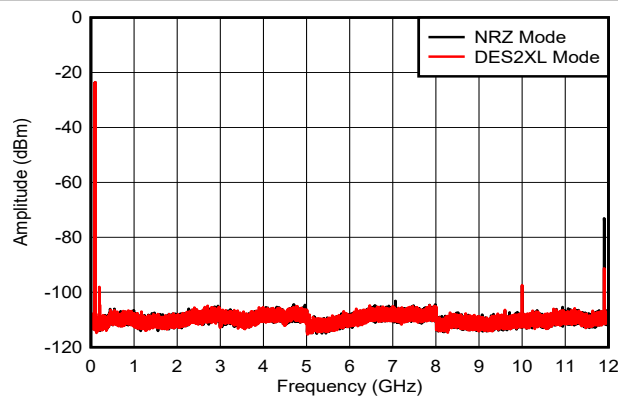


Figure 6-28. Dual Tone,  $f_{\text{OUT}} = 97\text{MHz}$ , -12dBFS

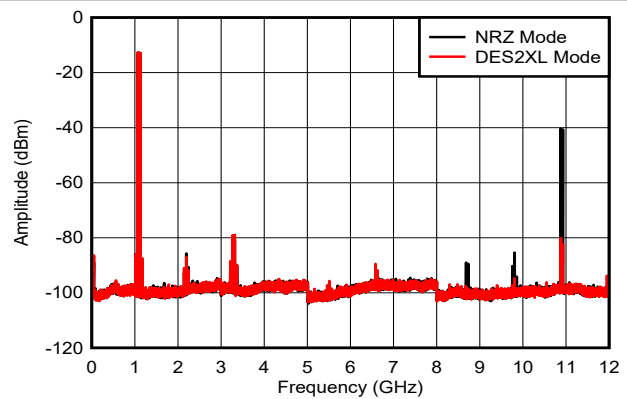


Figure 6-29. Dual Tone,  $f_{\text{OUT}} = 1097\text{MHz}$ , 0dBFS

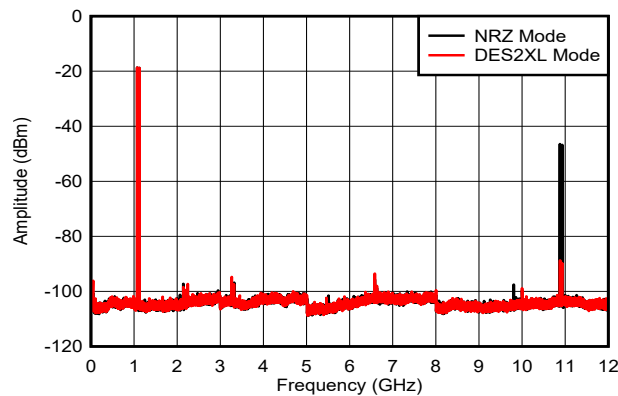


Figure 6-30. Dual Tone,  $f_{\text{OUT}} = 1097\text{MHz}$ , -6dBFS

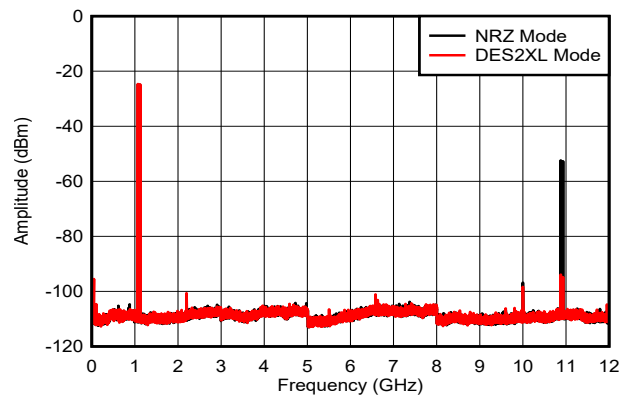
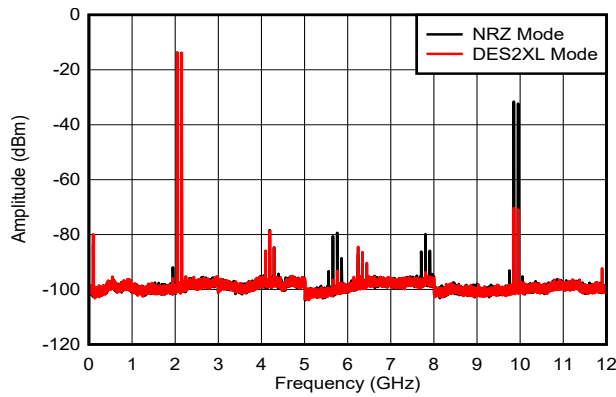


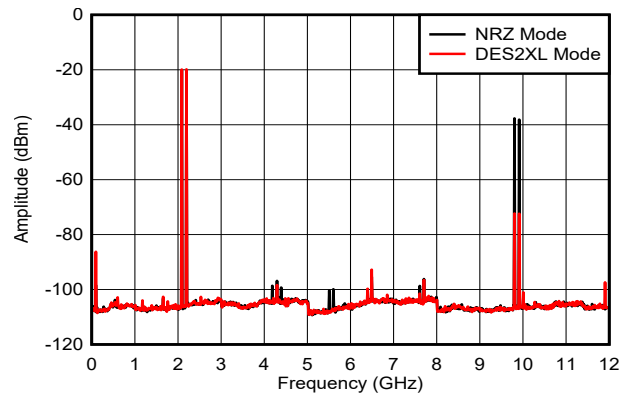
Figure 6-31. Dual Tone,  $f_{\text{OUT}} = 1097\text{MHz}$ , -12dBFS

## 6.12 Typical Characteristics: Dual Tone Spectra (continued)

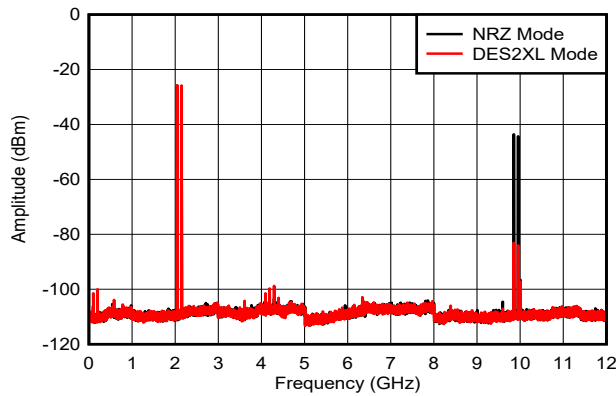
Typical values at  $T_A = +25^\circ\text{C}$ , minimum and maximum values over operating free-air temperature range, typical supply voltages,  $f_{\text{CLK}} = 10.24\text{GHz}$ ,  $I_{\text{FS\_SWITCH}} = 20.5\text{mA}$ , Dither and DEM enabled, unless otherwise noted.



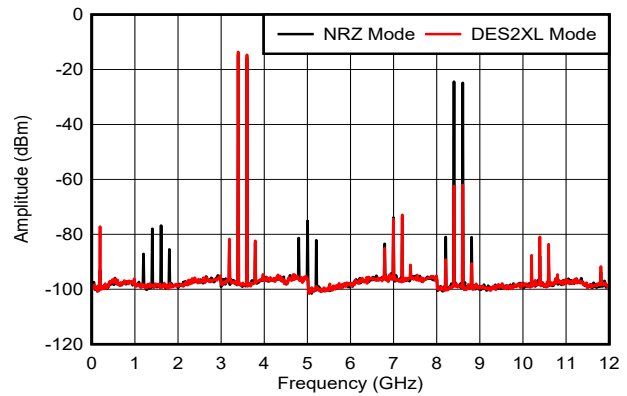
**Figure 6-32. Dual Tone,  $f_{\text{OUT}} = 2097\text{MHz}$ , 0dBFS**



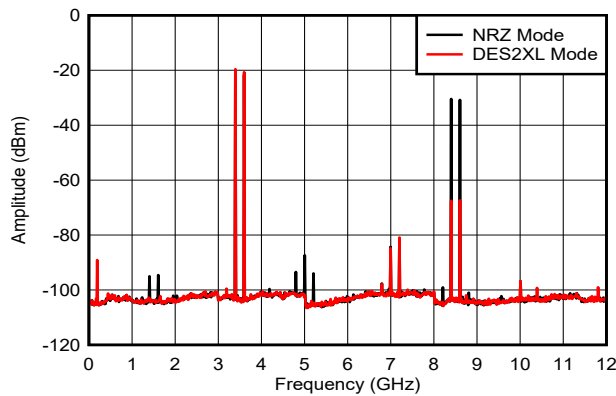
**Figure 6-33. Dual Tone,  $f_{\text{OUT}} = 2097\text{MHz}$ , -6dBFS**



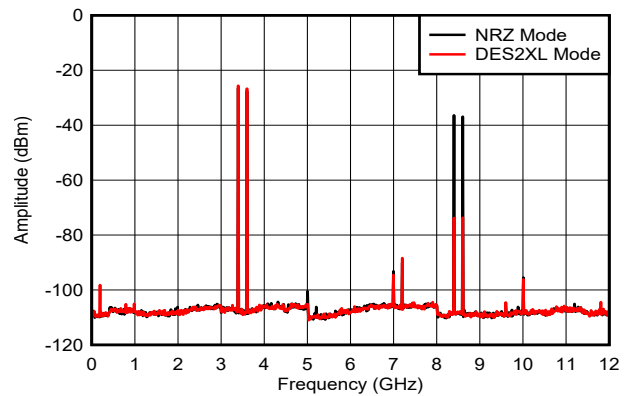
**Figure 6-34. Dual Tone,  $f_{\text{OUT}} = 2097\text{MHz}$ , -12dBFS**



**Figure 6-35. Dual Tone,  $f_{\text{OUT}} = 3497\text{MHz}$ , 0dBFS**



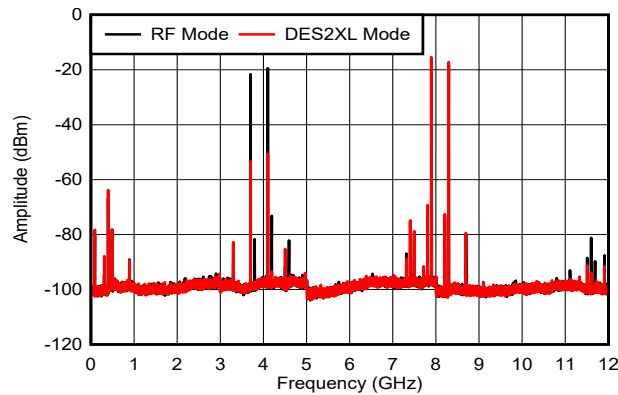
**Figure 6-36. Dual Tone,  $f_{\text{OUT}} = 3497\text{MHz}$ , -6dBFS**



**Figure 6-37. Dual Tone,  $f_{\text{OUT}} = 3497\text{MHz}$ , -12dBFS**

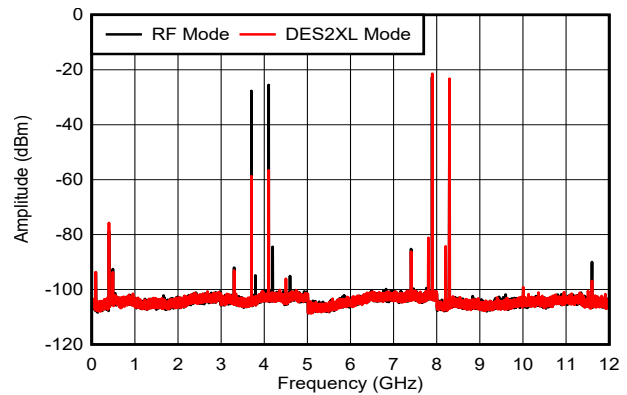
## 6.12 Typical Characteristics: Dual Tone Spectra (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , minimum and maximum values over operating free-air temperature range, typical supply voltages,  $f_{\text{CLK}} = 10.24\text{GHz}$ ,  $I_{\text{FS\_SWITCH}} = 20.5\text{mA}$ , Dither and DEM enabled, unless otherwise noted.



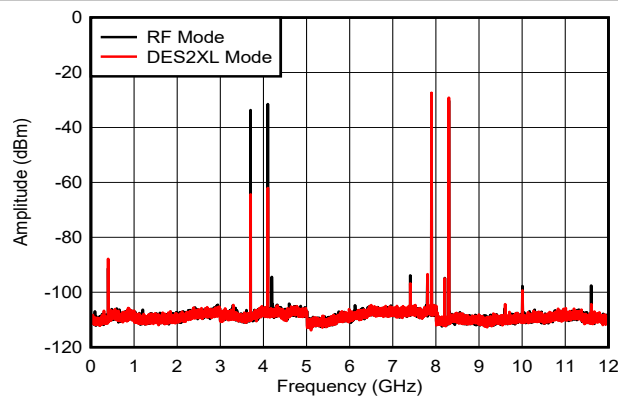
400MHz tone spacing, includes PCB, cable and balun loss

**Figure 6-38. Dual Tone,  $f_{\text{OUT}} = 8097\text{MHz}$ , 0dBFS**



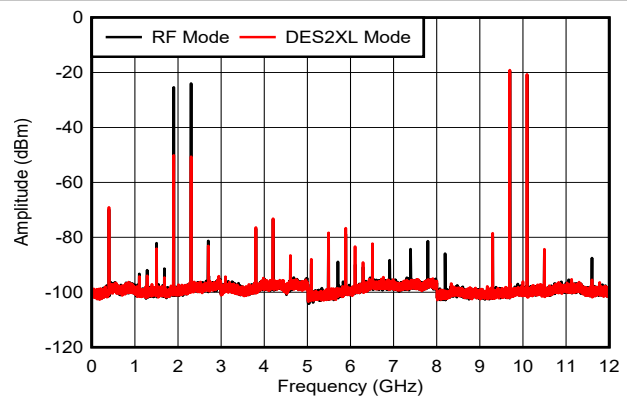
400MHz tone spacing, includes PCB, cable and balun loss

**Figure 6-39. Dual Tone,  $f_{\text{OUT}} = 8097\text{MHz}$ , -6dBFS**



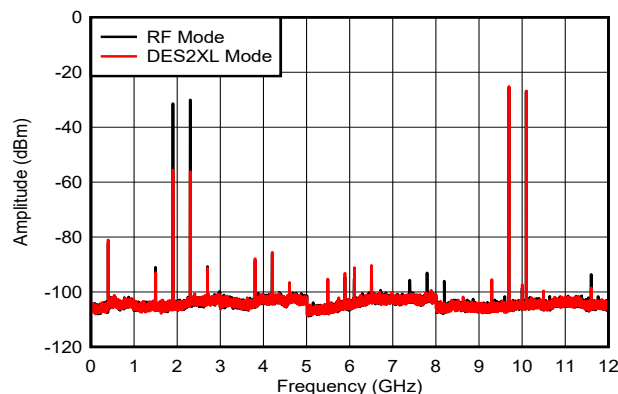
400MHz tone spacing, includes PCB, cable and balun loss

**Figure 6-40. Dual Tone,  $f_{\text{OUT}} = 8097\text{MHz}$ , -12dBFS**



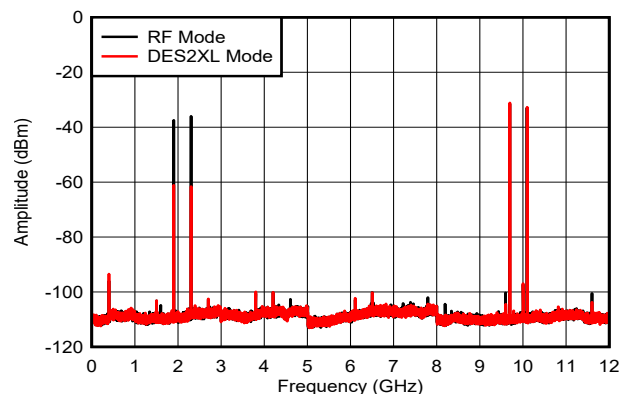
400MHz tone spacing, includes PCB, cable and balun loss

**Figure 6-41. Dual Tone,  $f_{\text{OUT}} = 9897\text{MHz}$ , 0dBFS**



400MHz tone spacing, includes PCB, cable and balun loss

**Figure 6-42. Dual Tone,  $f_{\text{OUT}} = 9897\text{MHz}$ , -6dBFS**

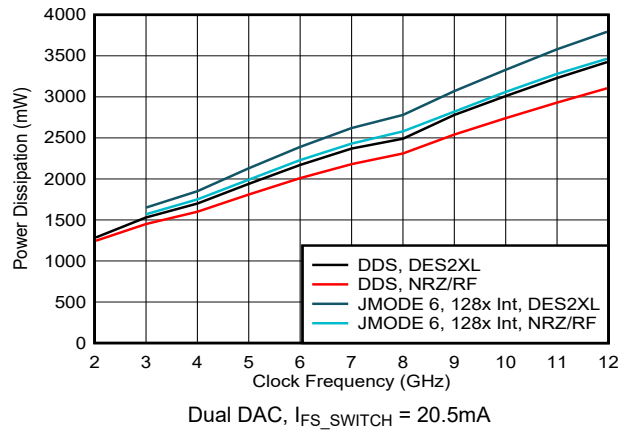


400MHz tone spacing, includes PCB, cable and balun loss

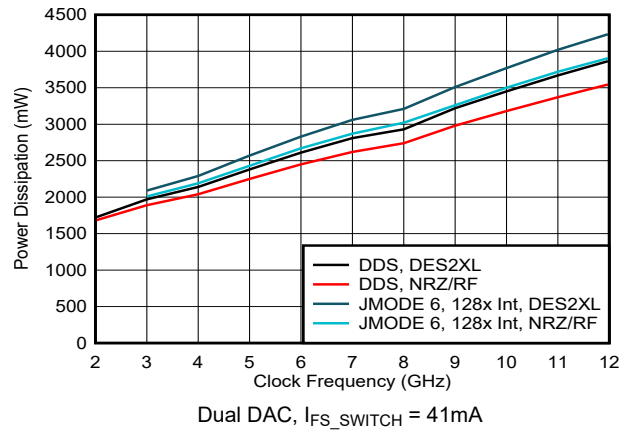
**Figure 6-43. Dual Tone,  $f_{\text{OUT}} = 9897\text{MHz}$ , -12dBFS**

## 6.13 Typical Characteristics: Power Dissipation and Supply Currents

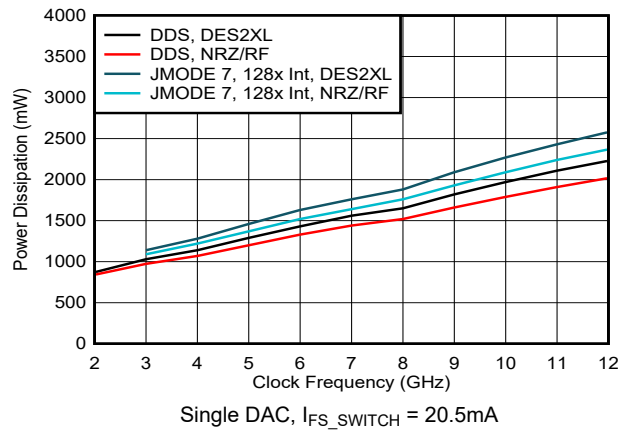
Typical values at  $T_A = +25^\circ\text{C}$  and nominal supply voltages,  $I_{FS\_SWITCH} = 20.5\text{mA}$ , 2 DACs = DDS39RF12, 1 DAC = DDS39RFS12, except where noted.



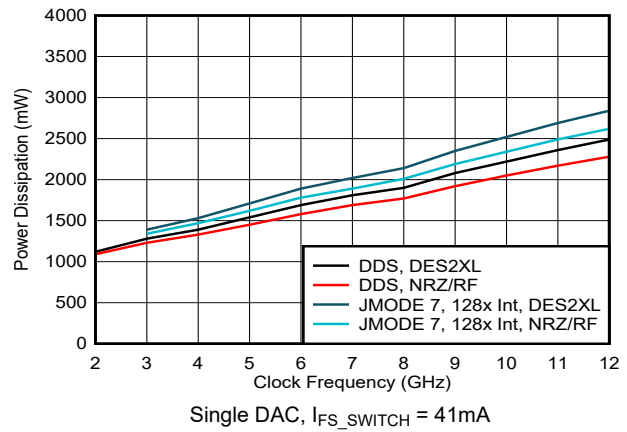
**Figure 6-44. Power Dissipation vs Clock Frequency and Digital Mode**



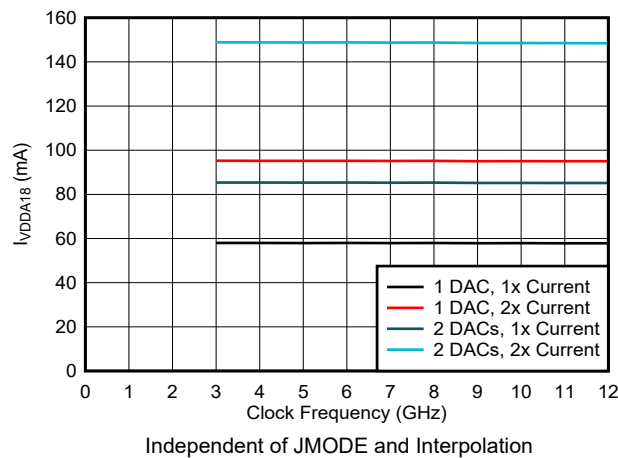
**Figure 6-45. Power Dissipation vs Clock Frequency and Digital Mode**



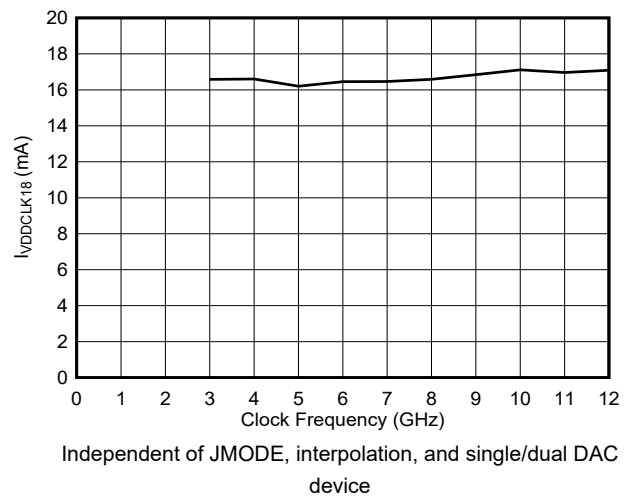
**Figure 6-46. Power Dissipation vs Clock Frequency and Digital Mode**



**Figure 6-47. Power Dissipation vs Clock Frequency and Digital Mode**



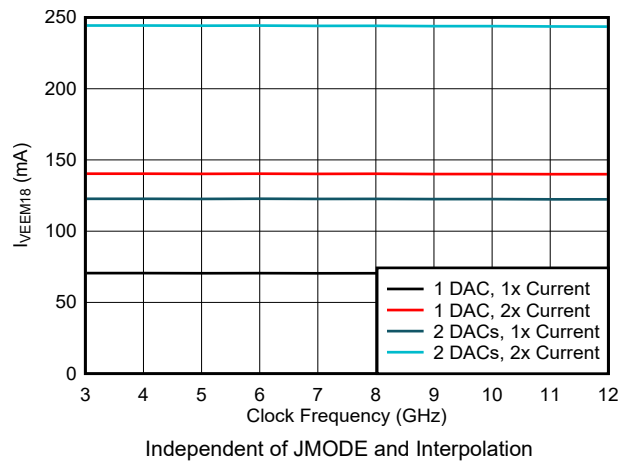
**Figure 6-48. VDDA18 Current vs Clock Frequency and DAC Mode**



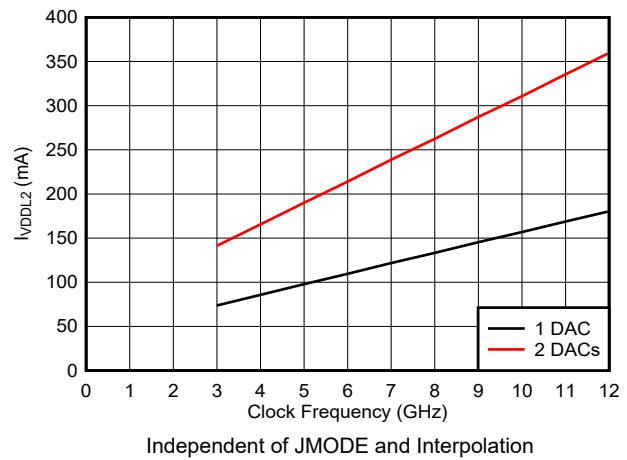
**Figure 6-49. VDDCLK18 Current vs Clock Frequency**

## 6.13 Typical Characteristics: Power Dissipation and Supply Currents (continued)

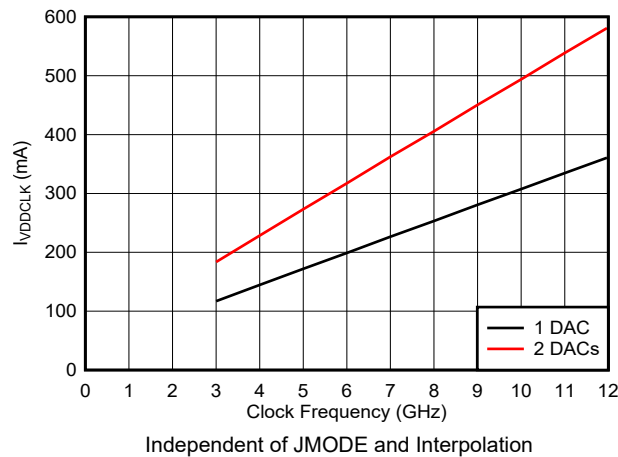
Typical values at  $T_A = +25^\circ\text{C}$  and nominal supply voltages,  $I_{FS\_SWITCH} = 20.5\text{mA}$ , 2 DACs = DDS39RF12, 1 DAC = DDS39RFS12, except where noted.



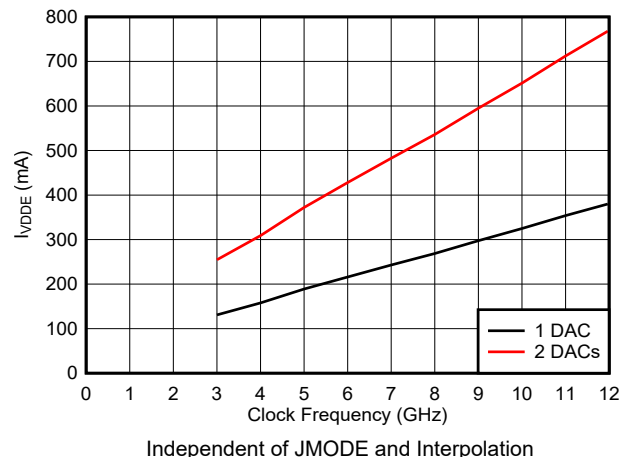
**Figure 6-50. VEEM18 Current vs Clock Frequency and Output Current**



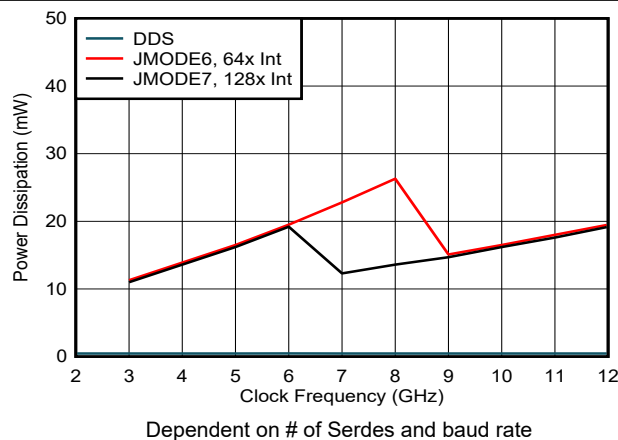
**Figure 6-51. VDDLx Current vs Clock Frequency**



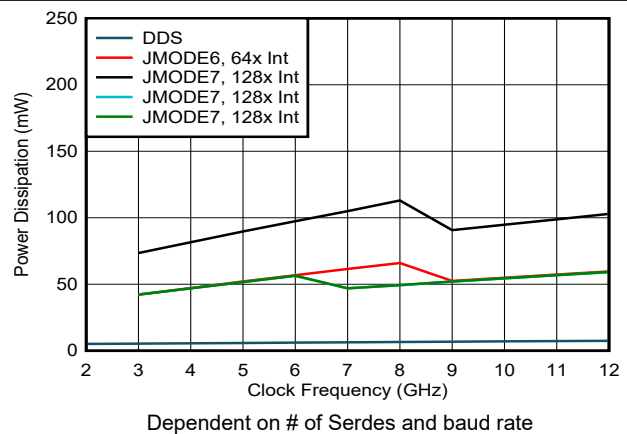
**Figure 6-52. VDDCLK Current vs Clock Frequency**



**Figure 6-53. VDDE Current vs Clock Frequency**



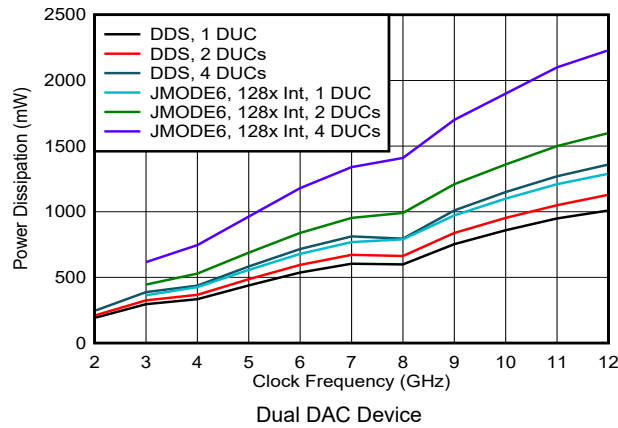
**Figure 6-54. VDDR18 Current vs Clock Frequency and Interface Mode**



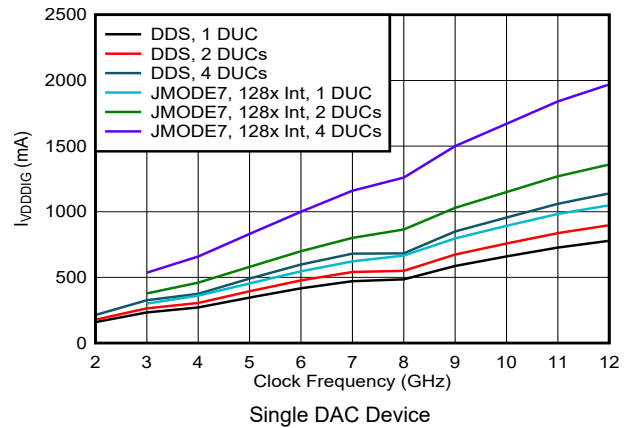
**Figure 6-55. VDDT Current vs Clock Frequency and Interface Mode**

## 6.13 Typical Characteristics: Power Dissipation and Supply Currents (continued)

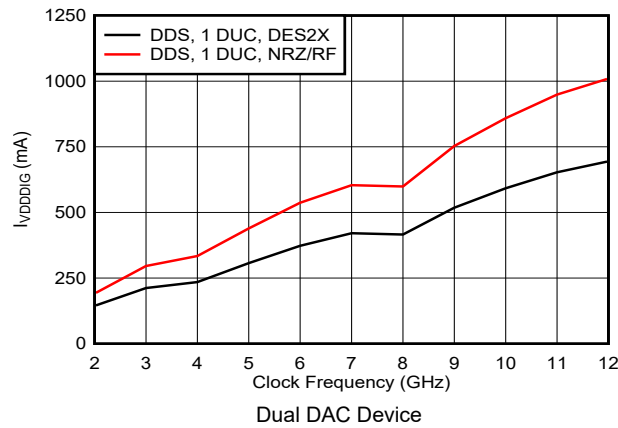
Typical values at  $T_A = +25^\circ\text{C}$  and nominal supply voltages,  $I_{FS\_SWITCH} = 20.5\text{mA}$ , 2 DACs = DDS39RF12, 1 DAC = DDS39RFS12, except where noted.



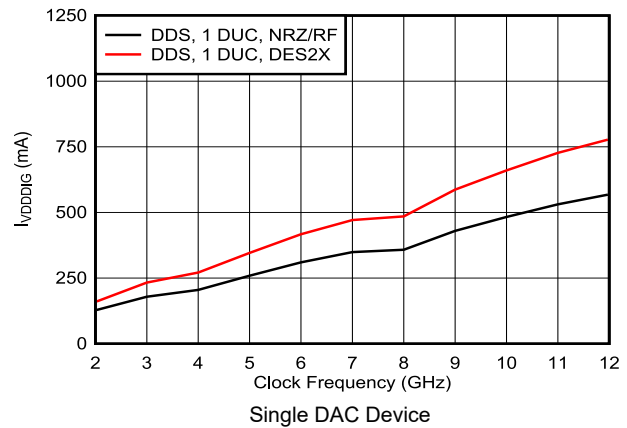
**Figure 6-56. VDDDIG Current vs Clock Frequency and Digital Mode**



**Figure 6-57. VDDDIG Current vs Clock Frequency and Digital Mode**



**Figure 6-58. VDDDIG Current vs Clock Frequency and DAC Mode**



**Figure 6-59. VDDDIG Current vs Clock Frequency and DAC Mode**

## 7 Detailed Description

### 7.1 Overview

DDS39RF12 and 'RFS12 are a family of dual and single channel direct digital synthesizers with 16-bit resolution digital-to-analog converters (DAC). The high sampling rate, output frequency range, 64-bit NCO frequency resolution and any frequency hopping with phase coherence makes the device capable of arbitrary waveform generation (AWG) and direct digital synthesis (DDS). The devices can also be used as non-interpolating or interpolating DACs for narrowband direct RF sampling or complex baseband signal generation. The maximum input data rate is 750MSPS for a single channel or 325MSPS for two channels. The devices can generate signals of up to 600MHz signal bandwidth (16-bit input resolution) at carrier frequencies exceeding 10GHz enabling direct sampling through C-band and into X-band.

The 64-bit NCO frequency resolution and infinite frequency hopping with phase coherence, continuity and reset options makes the device ideally suited for arbitrary waveform generation (AWG) and direct digital synthesis (DDS).

A JESD204C compatible serial interface with 8b/10b and 64b/66b encoding options has 2 receiver pairs capable of up to 12.8Gbps. The interface is JESD204C subclass-1 compliant for deterministic latency and multi-device synchronization through the use of SYSREF. The SYSREF Windowing feature allows for automatic SYSREF timing calibration.

### 7.2 Functional Block Diagrams

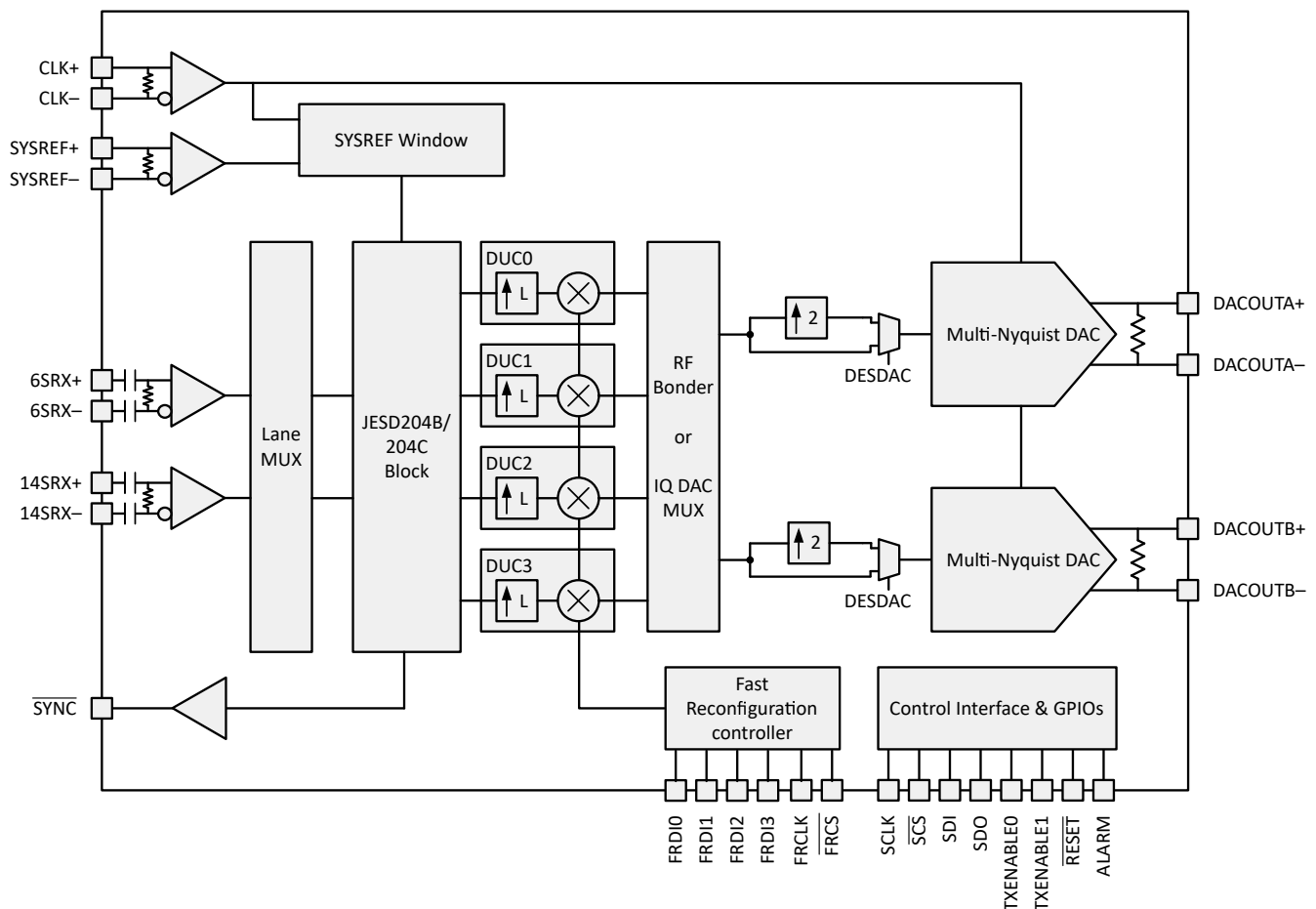
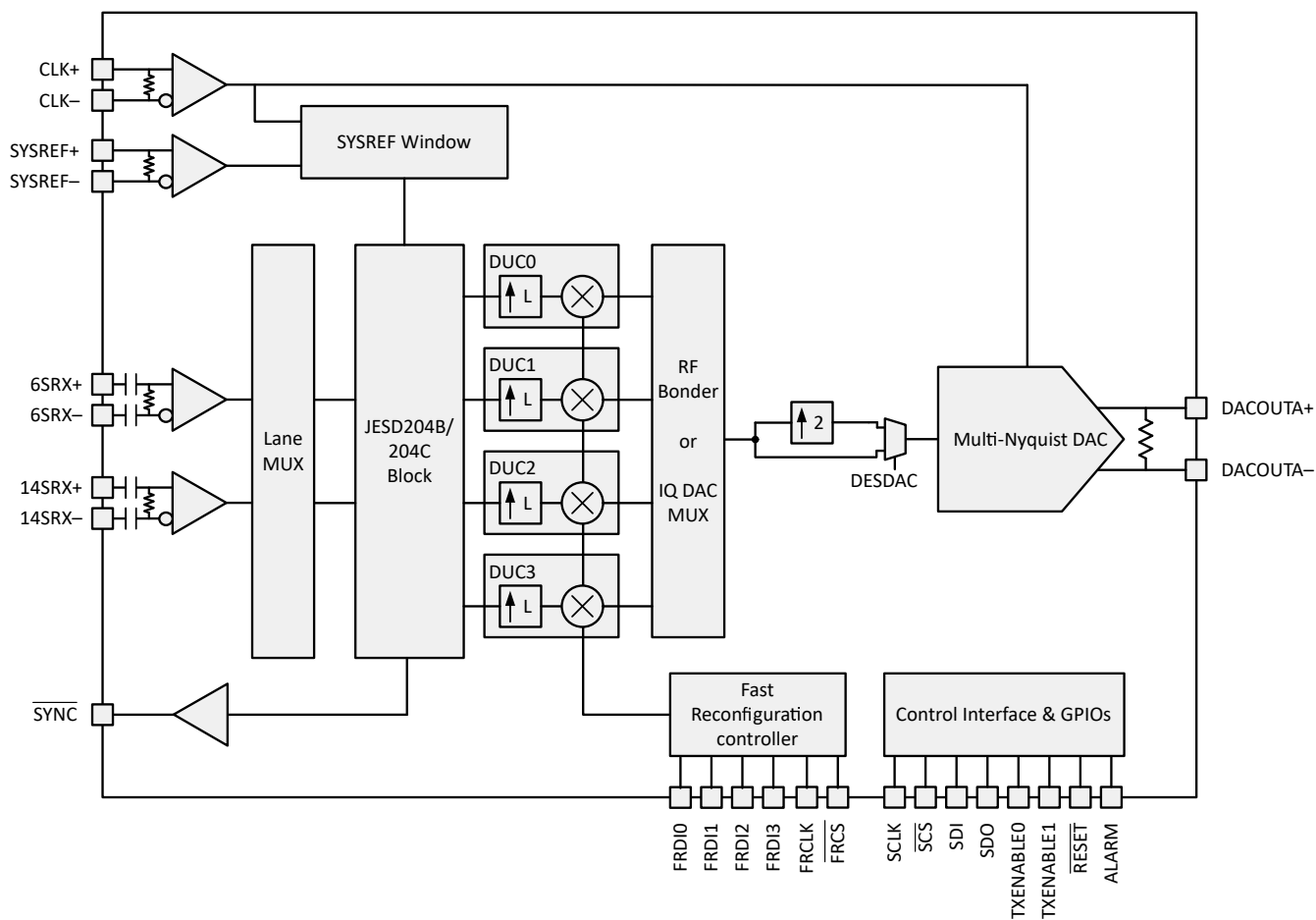


Figure 7-1. Dual Channel Device



**Figure 7-2. Single Channel Device**

## 7.3 Feature Description

This section describes the analog and digital features of the device.

### 7.3.1 DAC Output Modes

The DDS39RF12 and 'RFS12 consists of a multi-Nyquist DAC core capable of direct transmission through the third Nyquist zone. The high output frequency capabilities are enabled by specific output switching waveforms that alter the output waveform, changing the frequency response of the DAC to enhance the DAC images in alternate Nyquist zones. The desired switching waveforms can be selected through the serial interface. A list of modes along with their properties and uses are provided in [Table 7-1](#). The responses shown in this section do not consider the effect of the DAC analog bandwidth or external passive or active signal chain components.

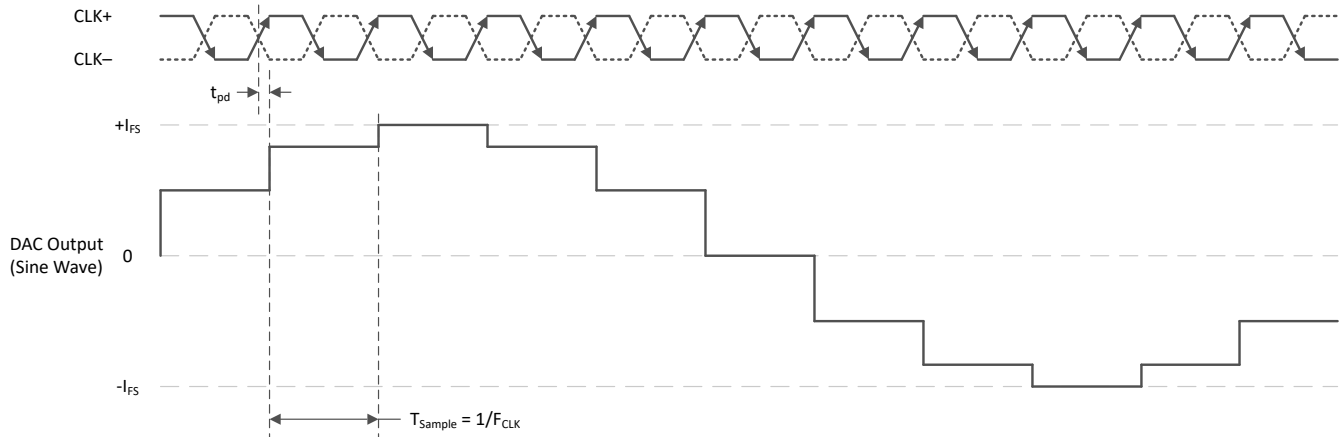
**Table 7-1. Summary of Multi-Nyquist Output Modes and Uses**

| DAC OUTPUT MODE          | PASSES DC | Optimal Frequency Range | PEAK OUTPUT POWER <sup>(1)</sup> | Other                                   |
|--------------------------|-----------|-------------------------|----------------------------------|-----------------------------------------|
| Non-return-to-zero (NRZ) | Yes       | 0 - $F_{CLK}/2$         | 0 dBFS                           |                                         |
| Return-to-zero (RTZ)     | Yes       | 0 - $F_{CLK}$           | -6 dBFS                          |                                         |
| Radio Frequency (RF)     | No        | $F_{CLK}/2$ - $F_{CLK}$ | -2.8 dBFS                        |                                         |
| Dual Edge Sampling (DES) | Yes       | 0 - $F_{CLK}$           | 0 dBFS                           | Duty cycle image at $F_{CLK} - F_{OUT}$ |

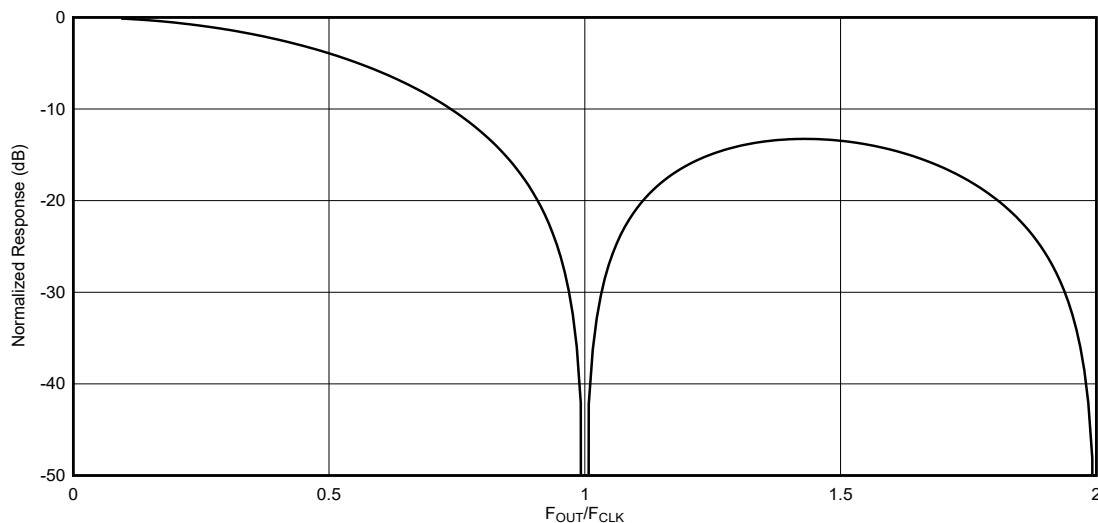
(1) Peak power here does not include the effect of analog output bandwidth due to parasitic passive components or external components

### 7.3.1.1 NRZ Mode

Non-return-to-zero (NRZ) mode is the standard zero-order hold mode. The timing diagram for NRZ mode is given in Figure 7-3. The sample is output from the DAC on the CLK rising edge and held until the rising edge. This output waveform can be thought of as a rectangular filter in time domain resulting in a sinc response in the frequency domain. The result is a frequency response that has significant power loss in the 2<sup>nd</sup> and 3<sup>rd</sup> Nyquist zones and a null at the sampling rate and is meant for 1<sup>st</sup> Nyquist zone operation only. A plot of the frequency response of NRZ mode is shown in Figure 7-4.



**Figure 7-3. NRZ Mode Timing Diagram**



**Figure 7-4. NRZ Mode Output Frequency Response**

### 7.3.1.2 RTZ Mode

Return-to-zero (RTZ) mode is similar to the standard zero-order hold mode used by DACs; however, the response adds a return-to-zero pulse for the second half of the sample period. The timing diagram for RTZ mode is given in Figure 7-5. This output waveform can be thought of as a rectangular filter in time domain that is half the length of that which is used in NRZ mode, resulting in a sinc response that is expanded by two times in the frequency domain. The result is a frequency response with less power loss in the 2<sup>nd</sup> Nyquist zone and a null at twice the sampling rate. It can be used for 1<sup>st</sup> and 2<sup>nd</sup> Nyquist zone applications. The return-to-zero pulse provides flatter response through the first Nyquist zone at a tradeoff of 6dB lower peak power. A plot of the frequency response of RTZ mode is shown in Figure 7-6.

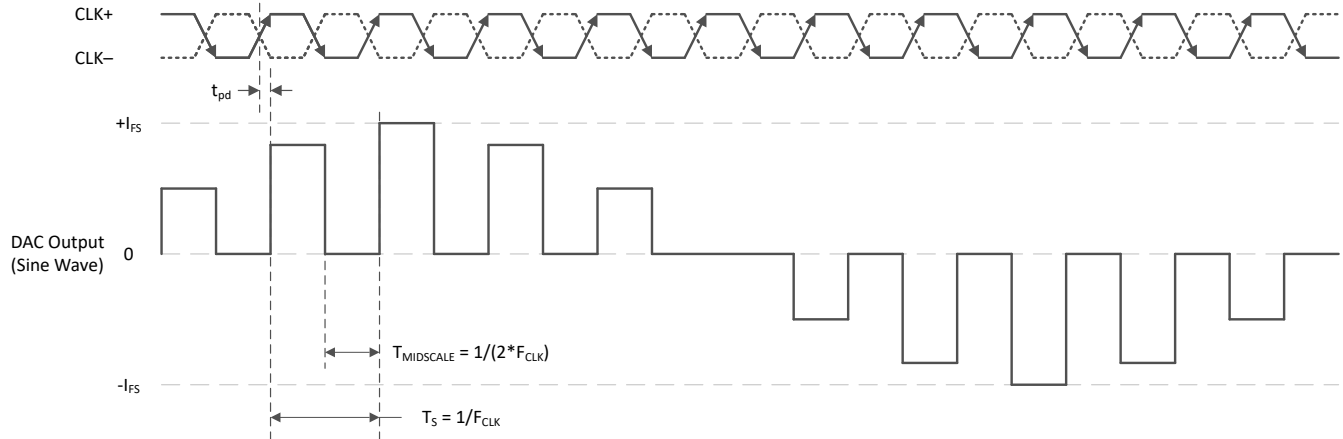


Figure 7-5. RTZ Mode Timing Diagram

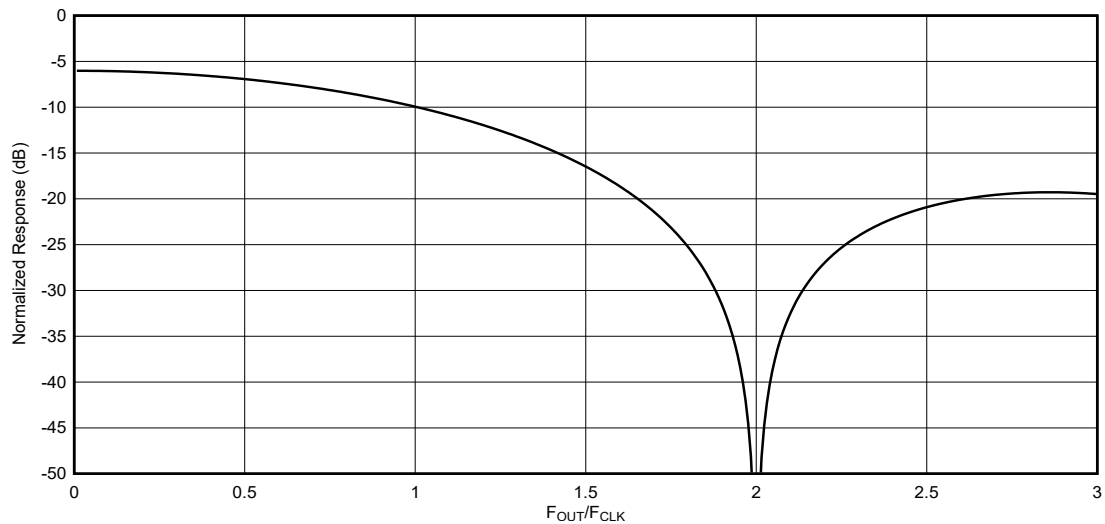
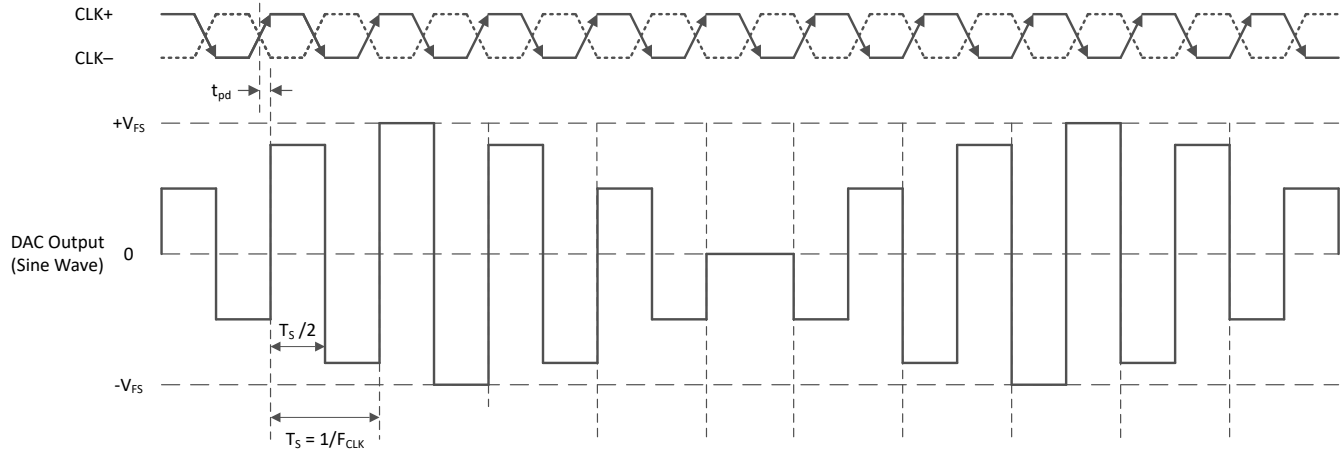


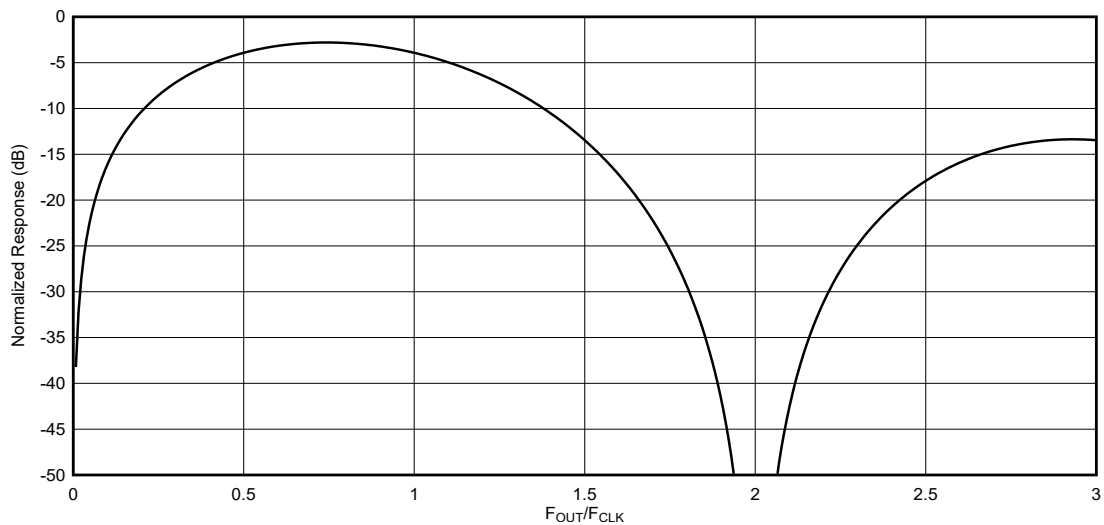
Figure 7-6. RTZ Mode Output Frequency Response

### 7.3.1.3 RF Mode

RF mode adds a mixing function to the DAC output by inverting the sample halfway through the sample period. The result is a sinc response that peaks and provides maximum flatness in the 2<sup>nd</sup> Nyquist zone. The timing diagram for RF mode is given in Figure 7-7. A plot of the frequency response of RF mode is shown in Figure 7-8.



**Figure 7-7. RF Mode Timing Diagram**

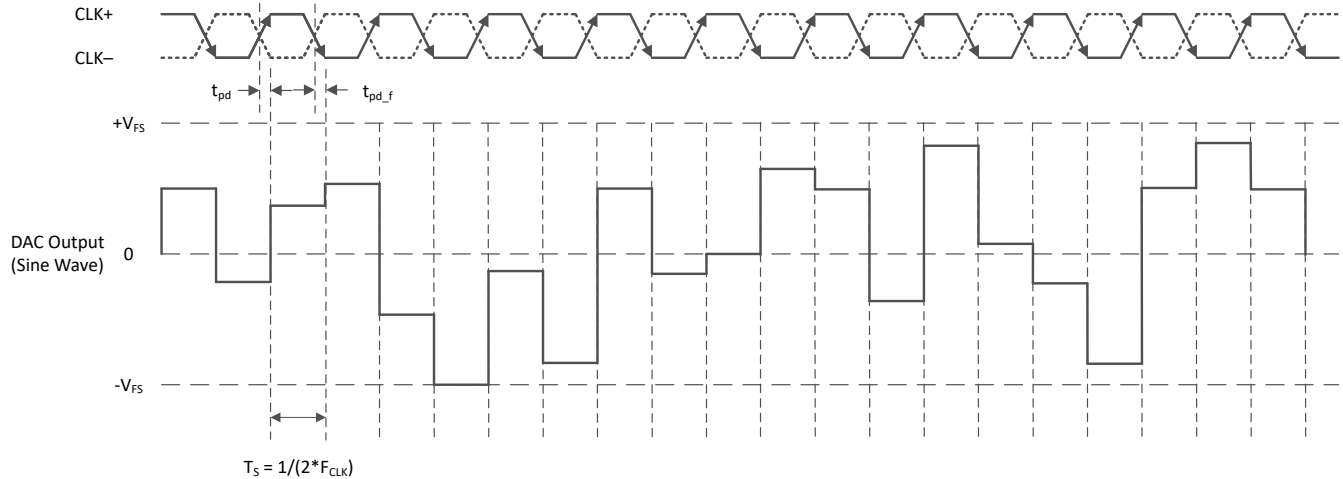


**Figure 7-8. RF Mode Output Frequency Response**

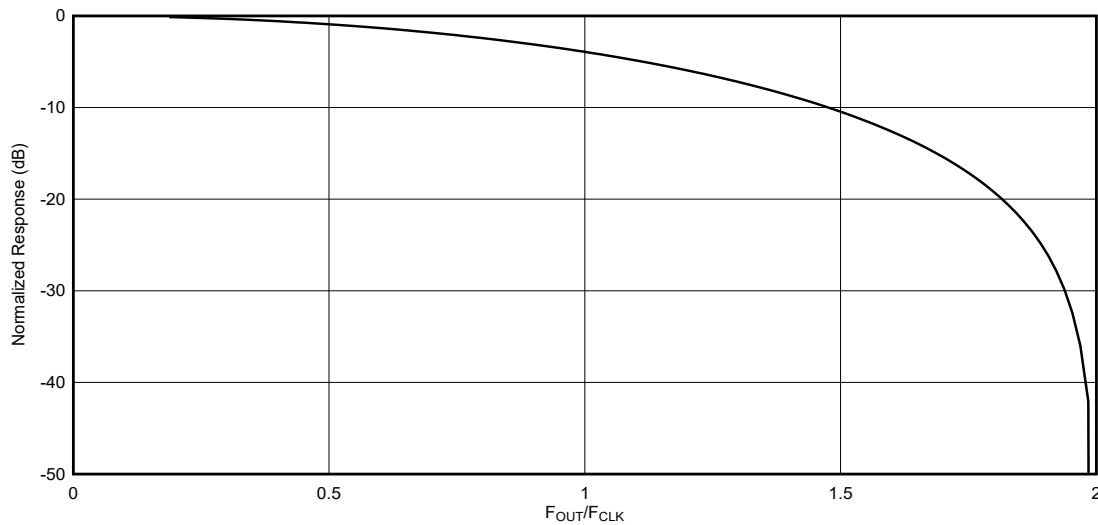
#### 7.3.1.4 DES Mode

Dual edge sampling (DES) mode outputs unique samples on both the rising and falling edge of CLK, doubling the sample rate for the same clock frequency. An extra digital interpolate by 2 stage is included in the device to enable a double sample rate.

An non-50% CLK duty cycle results in an image of the signal at  $F_{CLK} - F_{OUT}$ . Compared to NRZ mode with the same clock frequency, DES mode provides significant reduction in the image amplitude, reducing filter requirements. DES2XL uses an low pass 2x interpolation filter to increase from the single edge sample rate to dual edge sample rate, and supports output frequencies between 0 -  $0.4 \cdot F_{CLK}$ . DES2XH uses a high pass interpolation filter, supporting output frequencies between  $0.6 - 1.0 \cdot F_{CLK}$  with the same signal BW as DES2XL.



**Figure 7-9. DES Mode Timing Diagram**



**Figure 7-10. DES Output Frequency Response**

### 7.3.2 DAC Core

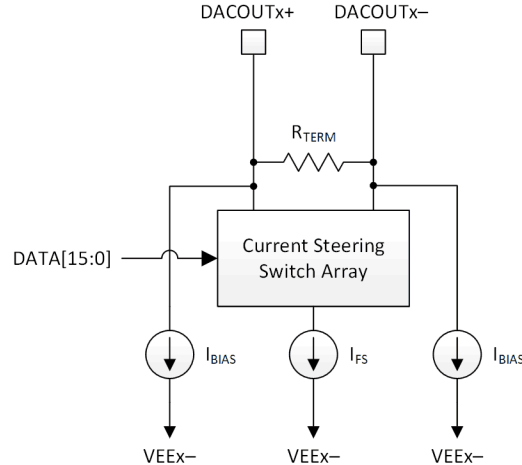
The device has two 16-bit DAC cores.

#### 7.3.2.1 DAC Output Structure

The DAC core analog output structure is shown in [Figure 7-11](#) for one DAC channel. There is a differential termination resistance between the two current output pins, DACOUTx±. The current steering switch array connects to the output pins and steers current between the output pins based on the digital code. A constant DC current bias,  $I_{BIAS}$ , draws current from both outputs regardless of the digital code. The  $I_{BIAS}$  current is:

$$3\text{mA} \times 2^{\text{CUR\_2X\_EN}} (\text{COARSE\_CUR\_x} + 5)/20 \quad (1)$$

With a 3.6kΩ resistor from RBIAS+ to RBIAS-.



**Figure 7-11. Analog Output Structure**

Examples of conversions from digital codes to currents on the IOUTx± outputs are given in Table 7-2. The currents shown in Table 7-2 include both the current steered portion and the bias currents on each leg.

**Table 7-2. Example Digital Code to Analog Current Conversions**

| DIGITAL CODE | 2'S COMPLEMENT      | OFFSET BINARY       | I <sub>DACOUTx+</sub>                  | I <sub>DACOUTx-</sub>                  | I <sub>DACOUTx+</sub> – I <sub>DACOUTx-</sub> |
|--------------|---------------------|---------------------|----------------------------------------|----------------------------------------|-----------------------------------------------|
| 32767        | 0111 1111 1111 1111 | 1111 1111 1111 1111 | $0.9999847 \times I_{FS} + I_{BIAS}$   | $0.0000153 \times I_{FS} + I_{BIAS}$   | $0.9999694 \times I_{FS}$                     |
| 16384        | 0100 0000 0000 0000 | 1100 0000 0000 0000 | $\frac{3}{4} \times I_{FS} + I_{BIAS}$ | $\frac{1}{4} \times I_{FS} + I_{BIAS}$ | $\frac{1}{2} \times I_{FS}$                   |
| 0            | 0000 0000 0000 0000 | 0000 0000 0000 0000 | $\frac{1}{2} \times I_{FS} + I_{BIAS}$ | $\frac{1}{2} \times I_{FS} + I_{BIAS}$ | 0                                             |
| -16384       | 1100 0000 0000 0000 | 0100 0000 0000 0000 | $\frac{1}{4} \times I_{FS} + I_{BIAS}$ | $\frac{3}{4} \times I_{FS} + I_{BIAS}$ | $-\frac{1}{2} \times I_{FS}$                  |
| -32768       | 1000 0000 0000 0000 | 0000 0000 0000 0000 | $I_{BIAS}$                             | $I_{FS} + I_{BIAS}$                    | $-I_{FS}$                                     |

### 7.3.2.2 Full-Scale Current Adjustment

The total DAC output current is set through the external R<sub>BIAS</sub> resistor and the COARSE\_CUR\_A or COARSE\_CUR\_B and the FINE\_CUR\_A or FINE\_CUR\_B registers. There is a switched fullscale current and a static fullscale current. The switched current is divided between DACOUTA/B+ and DACOUTA/B- in proportion to the digital signal value at the DAC. The static current is fixed at the output of each ball DACOUTA/B+ and DACOUTA/B-.

The equation for the DAC switched output current is

$$I_{FSSWITCH} = \frac{3.6k\Omega}{R_{BIAS}} \times (5mA + 1mA * COARSE + 0.0156mA * FINE) \times 2^{CUR\_2X\_EN} \quad (2)$$

where

- R<sub>bias</sub> is the external bias resistor
- COARSE is the value of the register COARSE\_CUR\_A or COARSE\_CUR\_B (0 to 15)
- FINE is the value of register FINE\_CUR\_A or FINE\_CUR\_B (0 to 63)
- CUR\_2X\_EN is the value of register CUR\_2X\_EN (0 or 1)

The static current is a fixed fraction of the switched current

$$I_{FSSTATIC} = 0.235 \times I_{FSSWITCH} \quad (3)$$

With a 3.6kΩ bias resistor, COARSE\_CUR\_A or COARSE\_CUR\_B = 15 and FINE\_CUR\_A or FINE\_CUR\_B = 31, I<sub>FSSWITCHED</sub> is ~ 20.5mA and I<sub>FSSTATIC</sub> ~ 4.82mA (on each ball + and -). Enabling CUR\_2X\_EN doubles the currents.

### 7.3.3 DEM and Dither

The device contains two optional features to improve non-linearity due to current segment and switch timing mismatch: Dynamic element Mixing (DEM) and dither.

The DAC core consists of

1. Thermometer encoded current sources/switches representing the upper MSBs
2. Thermometer encoded current sources/switches representing the middle bits (called ULSBs)
3. Binary weighted current sources/switches representing the lower LSBs.
4. Additional current sources/switches for dithering

DEM randomizes which MSB and ULSB current sources/switches are used to generate the output, which whitens the non-linearity due to mismatches between the current sources and switch timing. The [DEM\\_DACA/B](#) and [DEM\\_ADJ](#) registers control the frequency and amplitude of the shift in current sources/segments.

Dither add or subtracts 8 different digital code values to the digital data which are then canceled by switching additional current sources with the same amplitude. The digital data path is expanded so the full 16-bit range is maintained. The [DITH\\_DACA/B](#) registers control the frequency of the dither.

Using DEM generally improves low order harmonics near fullscale. Dither generally improves higher order harmonics near fullscale and all harmonics at lower digital amplitudes. Both DEM and dither increase the noise floor (both amplitude and phase) of the output due to the whitening of the non-linearity and the additional switching activity. This is reduced by DEM and dither settings with lower switching activity, that is. data dependent or reduced activity DEM. However, data dependent or reduced activity DEM is less effective at higher output frequencies. For data sheet specification testing in *Electrical Characteristics - AC Specifications*, data dependent DEM (DEM\_ADJ = 1) is used below 750MHz and normal activity DEM (DEM\_ADJ = 0) above 750MHz, but different settings (including disabling DEM and/or dither) can be tested and the best chosen based on the specific use case.

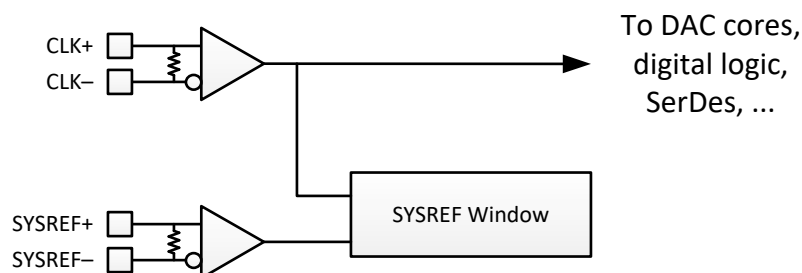
### 7.3.4 Offset Adjustment

The device allows an offset adjustment to the signal at the DAC output. The offset adjustment does NOT take away from the full 16-bit digital range of the DAC data.

The offset is set by the [DAC\\_OFS\[0\]](#) or [DAC\\_OFS\[1\]](#) register values for DACA and DACB, respectively. If dithering is enabled (see register [DEM\\_DITH](#)), the value is saturated to the range of  $\pm 128$ . If dithering is disabled, the value is saturated to the range  $\pm 3968$ . This makes sure that the primary DAC range will never be exceeded.

### 7.3.5 Clocking Subsystem

The device requires a clock running at a frequency equal to the DAC core sampling rate in NRZ, RTZ and RF modes, or at half of the DAC core sampling rate in DES mode. The clocking subsystem is shown in [Figure 7-12](#).



**Figure 7-12. Device Clocking Subsystem**

#### 7.3.5.1 SYSREF Frequency Requirements

The SYSREF input period must be an integer multiple of all clocks in the part, including the LMFC/LEMC. The following table depicts the requirements for the SYSREF period:

**Table 7-3. Requirements for SYSREF period**

| Requirements on SYSREF Period                                                                                                                            | Reason                                                                                                      |
|----------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------|
| SYSREF period must be a multiple of 16 CLK cycles.                                                                                                       | DAC Encoder/DEM always operates with a $F_{DAC}/16$ clock that is aligned to SYSREF.                        |
| SYSREF period must be a multiple of $LT$ CLK cycles. This constraint does not apply to DDS mode ( $DDS\_EN=1$ ).                                         | Makes sure the SYSREF period is a multiple of the input sample period.                                      |
| SYSREF period must be a multiple of $4*LT*S/F$ CLK cycles. This constraint does not apply to DDS mode ( $DDS\_EN=1$ ).                                   | Makes sure the SYSREF period is a multiple of the effective link layer clock period.                        |
| SYSREF period must be a multiple of $LT*S*K$ CLK cycles. This constraint does not apply to Subclass 0 mode ( $SUBCLASS=0$ ) or DDS mode ( $DDS\_EN=1$ ). | Makes sure that SYSREF period is a multiple of the LMFC/LEMC period. Note that $K=256*E/F$ in 64b/66b mode. |

### 7.3.5.2 SYSREF Position Detector and Sampling Position Selection (SYSREF Windowing)

The SYSREF Windowing block is used to first detect the position of SYSREF relative to the input clock  $CLK\pm$  rising edge. Based on the window information, an optimum SYSREF sampling time is selected to maximize setup and hold timing margins relative to the input clock. In many cases, a single SYSREF sampling position [SYSREF\\_SEL](#) is sufficient to meet timing for all systems (device-to-device variation) and conditions (temperature and voltage variations). However, this feature can also be used by the system to expand the timing window by tracking the movement of SYSREF as operating conditions change or to remove system-to-system variation at production test by finding a unique optimal value at nominal conditions for each system.

This section describes proper usage of the SYSREF Windowing block ([SYSREF\\_RECV\\_SLEEP](#) must be programmed to 0). First, apply the device clock and SYSREF to the device. The location of SYSREF relative to the device clock cycle is determined and stored in the [SYSREF\\_POS](#) field. Each bit of [SYSREF\\_POS](#) represents a potential SYSREF sampling position. If a bit in [SYSREF\\_POS](#) is set to 1, then the corresponding SYSREF sampling position has a potential setup or hold violation. Upon determining the valid SYSREF sampling positions (the positions of [SYSREF\\_POS](#) that are set to 0) the desired sampling position can be chosen by setting [SYSREF\\_SEL](#) to the value corresponding to that [SYSREF\\_POS](#) position. In general, the middle sampling position between two setup and hold instances is chosen. The determination of [SYSREF\\_SEL](#) is performed at the nominal operating conditions of the system (temperature and supply voltage) to provide maximum margin for operating condition variations. This process can be performed at final test and the optimal [SYSREF\\_SEL](#) setting can be stored for use at every system power up. Further, [SYSREF\\_POS](#) can be used to characterize the skew between  $CLK\pm$  and  $SYSREF\pm$  over operating conditions for a system by sweeping the system temperature and supply voltages. For systems that have large variations in  $CLK\pm$  to  $SYSREF\pm$  skew, this characterization can be used to track the optimal SYSREF sampling position as system operating conditions change. In general, a single value can be found that meets timing over all conditions for well-matched systems, such as those where  $CLK\pm$  and  $SYSREF\pm$  come from a single clocking device.

The step size between each [SYSREF\\_POS](#) sampling position can be adjusted using [SYSREF\\_ZOOM](#). When [SYSREF\\_ZOOM](#) is set to 0, the delay steps are coarser. When [SYSREF\\_ZOOM](#) is set to 1, the delay steps are finer. See the electrical specifications table for delay step sizes when [SYSREF\\_ZOOM](#) is enabled and disabled. In general, [SYSREF\\_ZOOM](#) is recommended to always be used ([SYSREF\\_ZOOM](#) = 1) unless a transition region (defined by 1's in [SYSREF\\_POS](#)) is not observed, which can be the case for low clock rates. Bits 0 and 19 of [SYSREF\\_POS](#) are always 1 because there is insufficient information to determine if these settings are close to a timing violation, although the actual valid window can extend beyond these sampling positions. The value programmed into [SYSREF\\_SEL](#) is the decimal number representing the desired bit location in [SYSREF\\_POS](#). [Table 7-4](#) lists some example [SYSREF\\_POS](#) readings and the optimal [SYSREF\\_SEL](#) settings. Although 20 sampling positions are provided by the [SYSREF\\_POS](#) status register, [SYSREF\\_SEL](#) only allows selection of the first 16 sampling positions, corresponding to [SYSREF\\_POS](#) bits 0 to 15. The additional [SYSREF\\_POS](#) status bits are intended only to provide additional knowledge of the SYSREF valid window. In general, lower values of [SYSREF\\_SEL](#) are selected because of delay variation over supply voltage, however in the fourth example a value of 14 provides additional margin and can be selected instead.

If [SYSREF\\_PS\\_EN](#) is set to 0, only the last SYSREF edge is used for the [SYSREF\\_POS](#) values. Setting [SYSREF\\_PS\\_EN](#) to 1 enables an "infinite persistence" mode, where if any SYSREF edge since

**SYSREF\_PS\_EN** is enabled has a 1 in a position, the **SYSREF\_POS** value is set to one. This provides worst case values for **SYSREF\_POS** to select the optimum **SYSREF\_SEL** setting.

**Table 7-4. Examples of SYSREF\_POS Readings and SYSREF\_SEL Selections**

| SYSREF_POS[19:0]                |                                            |                                              | OPTIMAL SYSREF_SEL SETTING |
|---------------------------------|--------------------------------------------|----------------------------------------------|----------------------------|
| 0x092[3:0]<br>(positions 19-16) | 0x091[7:0] <sup>(1)</sup> (positions 15-8) | 0x090[7:0] <sup>(1)</sup><br>(positions 7-0) |                            |
| b1000                           | b01100000                                  | b00011001                                    | 8 or 9                     |
| b1000                           | b00000000                                  | b00110001                                    | 12                         |
| b1000                           | b01100000                                  | b00000001                                    | 6 or 7                     |
| b1000                           | b00000011                                  | b00000001                                    | 4 or 14                    |
| b1100                           | b01100011                                  | b00011001                                    | 6                          |

(1) Underlined 0 indicates the bits that are selected, as given in the last column of this table.

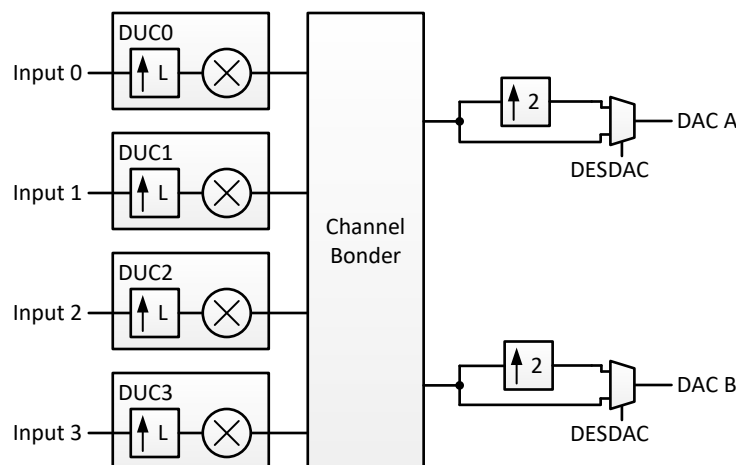
To use SYSREF Windowing:

1. Apply SYSREF and CLK
2. Set **SYSREF\_RECV\_SLEEP** = 0 and **SYSREF\_ZOOM** = 1
3. If persistence is desired, set **SYSREF\_PS\_EN** = 1 and allow many SYSREF transitions for **SYSREF\_POS** to build.
4. Read **SYSREF\_POS** and determine a proper setting for **SYSREF\_SEL**, as shown above. If a proper sampling point cannot be determined, set **SYSREF\_ZOOM** = 0 and retry.
5. Once a proper value for **SYSREF\_SEL** is applied, program **SYSREF\_PROC\_EN** = 1 and **SYSREF\_ALIGN\_EN** = 1.
6. SYSREF is now being properly processed by the device and the user can proceed to use the JESD204C interface (or other functionality) that relies on SYSREF.
7. SYSREF may need to be adjusted over large temperature or supply voltage swings, depending on the input clock frequency. The SYSREF invalid window dependence on temperature ( $t_{INV(TEMP)}$ ) and VA11 supply voltage ( $t_{INV(VA11)}$ ) is given in [Section 6.8](#). To adjust **SYSREF\_SEL** to track shifts in SYSREF relative to the input clock, the following steps can be looped (that is, in background during operation of the JESD204C link):
  - a. If persistence is desired, clear and then set **SYSREF\_PS\_EN**, and allow many SYSREF transitions for the **SYSREF\_POS** data to build.
  - b. Read **SYSREF\_POS** and determine a new value for **SYSREF\_SEL** (but do not program it yet). The procedure to incrementally adjust **SYSREF\_SEL** should prefer values that are closer to the previous **SYSREF\_SEL** value rather than selecting the smallest valid **SYSREF\_SEL** value. This helps make sure that the original valid window is selected and tracked rather than selecting a different window which would cause clock realignment to occur.
  - c. Program **SYSREF\_PROC\_EN** = 0. Write the new **SYSREF\_SEL** value, and then set **SYSREF\_PROC\_EN** = 1. The new **SYSREF\_SEL** value is now used by the device.
  - d. Wait for some period of time, then return to step 7a above.

### 7.3.6 Digital Signal Processing Blocks

The digital signal processing blocks are shown in [Figure 7-13](#). The device includes four digital up-converter (DUC) blocks supporting four complex (IQ) input streams that can be combined at different RF frequencies. The four DUCs can be flexibly assigned and summed together for either DAC output in the channel bonder. The final signal processing block is a extra interpolate by 2 filter for use with DES2XL/H mode.

[Table 7-5](#) and [Table 7-6](#) list the available modes for single channel and dual channel outputs, respectively.



**Figure 7-13. DUC Block with real output**

**Table 7-5. DSP Modes with Single Output Signal**

| Input Steams | LT (Interpolation) | NCO_EN | DUC_FORMAT | DAC_SRC0 value     | MXMODE0/1           | Description                                                                                                    |
|--------------|--------------------|--------|------------|--------------------|---------------------|----------------------------------------------------------------------------------------------------------------|
| 1            | 1                  | 0      | Real       | 0x1                | NRZ, RTZ, RF, DES2x | Single channel mode (no up-conversion).                                                                        |
| 2, 4, 6 or 8 | 2-256x             | 1      | Real       | 0x1, 0x3, 0x7, 0xF | NRZ, RTZ, RF, DES2x | 1-4 DUC channels with single real output<br>DAC_SRC0 settings are for 1, 2, 3, or 4 DUC channels respectively. |

These modes only produce one output signal, so only one DAC is required. The table shows the programming to use DACA (MXMODE1 should be set to disabled). The user may elect to use DACB instead by programming DAC\_SRC1 and MXMODE1 (and setting MXMODE0 to disabled). The user may also program DAC\_SRC1=DAC\_SRC0 and MXMODE1=MXMODE0 and then tie the DAC outputs together to get more output power.

**Table 7-6. DSP Modes with Dual Output Signal**

| Input Steams | LT (Interpolation) | NCO_EN | DUC_FORMAT | DAC_SRC0 value | DAC_SRC1 value | MXMODE0/1           | Description                                                                                       |
|--------------|--------------------|--------|------------|----------------|----------------|---------------------|---------------------------------------------------------------------------------------------------|
| 2            | 1                  | 0      | N/A        | 0x1            | 0x2            | NRZ, RTZ, RF, DES2x | Dual channel mode (no up-conversion)                                                              |
| 2, 4, 6 or 8 | 2-256x             | 1      | Real       | any bits set   | any bits set   | NRZ, RTZ, RF, DES2x | 1-4 DUC channels with two real outputs                                                            |
| 2            | 2-256x             | 1 or 0 | Complex    | 0x1            | 0x4            | NRZ, RTZ, RF, DES2x | 1 DUC channel with complex output:<br>DACA outputs real samples<br>DACB outputs imaginary samples |
| 4            | 2-256x             | 1 or 0 | Complex    | 0x3            | 0xC            | NRZ, RTZ, RF, DES2x | 2 DUC channels with complex output                                                                |

These modes produce two output signals (and uses both DACs). The user may elect to swap the values programmed into DAC\_SRC0 and DAC\_SRC1 to swap the output signals. Typically MXMODE0 and MXMODE1 are set to the same setting, however this is not required.

### 7.3.6.1 Digital Upconverter (DUC)

Each DUC interpolates the I and Q signals by factors ranging from LT = 2, 3, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128, 192 and 256. The resulting up-converted baseband I/Q signal is then multiplied by a complex sinusoid generated by the numerically controlled oscillator (NCO) to mix the signal to the desired carrier frequency for output from the DAC. The interpolation factors supported vs the number of DUCs enabled is listed in Table 7-7.

**Table 7-7. Supported Interpolation Factors vs Number of DUCs Enabled**

| Number of Streams (JESD_M) | Interpolation Factors Supported (LT) | DUCs Enabled           |
|----------------------------|--------------------------------------|------------------------|
| 2                          | 2-256x                               | DUC0                   |
| 4                          | 4-256x                               | DUC0, DUC1             |
| 6                          | 8-256x                               | DUC0, DUC1, DUC2       |
| 8                          | 8-256x                               | DUC0, DUC1, DUC2, DUC3 |

The NCOs and mixer can be bypassed, essentially setting the frequency and phase to 0, in which case the I input passes to the I output and the Q input passes to the Q output.

#### 7.3.6.1.1 Interpolation Filters

The first operation of the DUC is to interpolate the input signal to a higher data rate. The available interpolation options are summarized in [Table 7-8](#). The sampling rate of the input signal is multiplied by the specified interpolation amount to determine the DAC output rate, subject to the maximum sample rate for the DDS39RF12 and 'RFS12. These rates do not include the optional 2x interpolation for DES mode. For interpolations rates 6x and below, a reduced number of DUC channels are available.

**Table 7-8. Summary of Interpolation Options**

| INTERPOLATION | Maximum Number of DUC channels |
|---------------|--------------------------------|
| 2x            | 1                              |
| 3x            | 1                              |
| 4x            | 2                              |
| 6x            | 2                              |
| 8x            | 4                              |
| 12x           | 4                              |
| 16x           | 4                              |
| 24x           | 4                              |
| 32x           | 4                              |
| 48x           | 4                              |
| 64x           | 4                              |
| 96x           | 4                              |
| 128x          | 4                              |
| 192x          | 4                              |
| 256x          | 4                              |

Each DUC contains multiple 2x or 3x interpolating filters. The filter coefficients for each filter are listed in [Table 7-9](#) and the filters used for each interpolation factor are shown in [Table 7-10](#). The interpolation filter composite responses are given in [Figure 7-14](#) to [Figure 7-42](#). The filters are designed to provide a passband bandwidth of 80% on the input bandwidth and passband ripple less than 0.01 dB. The stopband attenuation is greater than 90 dB for any signal within the passband.

**Table 7-9. Interpolation Filter Coefficients**

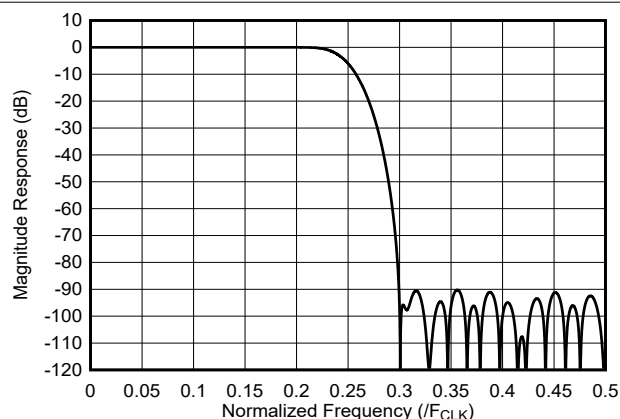
| Filter | Coefficients (Center Tap in Bold)                                                                                                                                                                                                       |
|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| fir1   | [6 0 -19 0 47 0 -100 0 192 0 -342 0 572 0 -914 0 1409 0 -2119 0 3152 0 -4729 0 7420 0 -13334 0 41527 <b>65536</b> 41527 0 -13334 0 7420 0 -4729 0 3152 0 -2119 0 1409 0 -914 0 572 0 -342 0 192 0 -100 0 47 0 -19 0 6]*2 <sup>-16</sup> |
| fir2   | [-12 0 84 0 -336 0 1006 0 -2691 0 10141 <b>16384</b> 10141 0 -2691 0 1006 0 -336 0 84 0 -12]*2 <sup>-14</sup>                                                                                                                           |
| fir3   | [29 0 -214 0 1209 <b>2048</b> 1209 0 -214 0 29]*2 <sup>-11</sup>                                                                                                                                                                        |
| fir4   | [3 0 -25 0 150 <b>256</b> 150 0 -25 0 3]*2 <sup>-8</sup>                                                                                                                                                                                |
| fir5   | [-1 0 9 <b>16</b> 9 0 -1]*2 <sup>-4</sup>                                                                                                                                                                                               |

**Table 7-9. Interpolation Filter Coefficients (continued)**

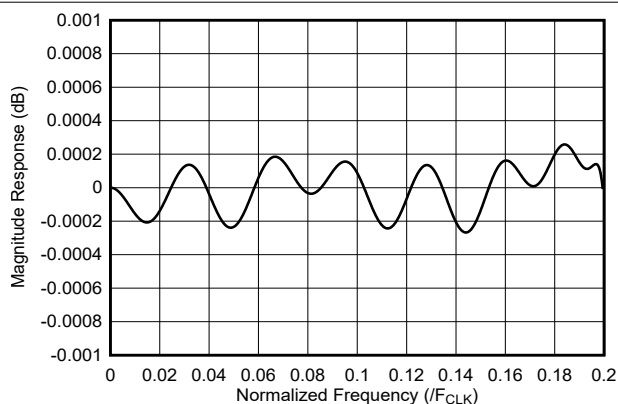
| Filter | Coefficients (Center Tap in Bold)                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| fir_3x | -38 -38 0 83 117 0 -214 -281 0 464 584 0 -900 -1102 0 1612 1929 0 -2713 -3190 0 4346 5040 0 -6699 -7684 0 10023 11408 0 -14701 -16661 0 21389 24260 0 -31417 -35960 0 48101 56540 0 -82781 -105224 0 215190 432780 <b>524288</b> 432780 215190 0 -105224 -82781 0 56540 48101 0 -35960 -31417 0 24260 21389 0 -16661 -14701 0 11408 10023 0 -7684 -6699 0 5040 4346 0 -3190 -2713 0 1929 1612 0 -1102 -900 0 584 464 0 -281 -214 0 117 83 0 -38 -38 ]*2 <sup>-19</sup> |

**Table 7-10. Filters Used vs. DUC Interpolation Factor**

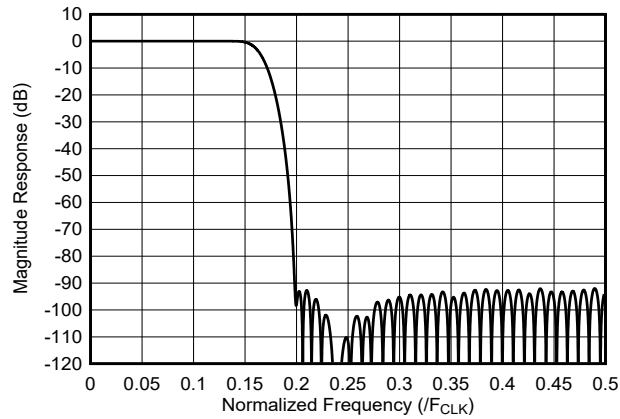
| DUC Interpolation Factor (L <sub>DUC</sub> ) | Filters Used in DUC    |                        |                        |                        |                        |                        |                        |                        |
|----------------------------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|
|                                              | 1 <sup>st</sup> Filter | 2 <sup>nd</sup> Filter | 3 <sup>rd</sup> Filter | 4 <sup>th</sup> Filter | 5 <sup>th</sup> Filter | 6 <sup>th</sup> Filter | 7 <sup>th</sup> Filter | 8 <sup>th</sup> Filter |
| 2x                                           | fir1                   |                        |                        |                        |                        |                        |                        |                        |
| 3x                                           | fir_3x                 |                        |                        |                        |                        |                        |                        |                        |
| 4x                                           | fir1                   | fir2                   |                        |                        |                        |                        |                        |                        |
| 6x                                           | fir_3x                 | fir2                   |                        |                        |                        |                        |                        |                        |
| 8x                                           | fir1                   | fir2                   | fir3                   |                        |                        |                        |                        |                        |
| 12x                                          | fir_3x                 | fir2                   | fir3                   |                        |                        |                        |                        |                        |
| 16x                                          | fir1                   | fir2                   | fir3                   | fir4                   |                        |                        |                        |                        |
| 24x                                          | fir_3x                 | fir2                   | fir3                   | fir4                   |                        |                        |                        |                        |
| 32x                                          | fir1                   | fir2                   | fir3                   | fir4                   | fir5                   |                        |                        |                        |
| 48x                                          | fir_3x                 | fir2                   | fir3                   | fir4                   | fir5                   |                        |                        |                        |
| 64x                                          | fir1                   | fir2                   | fir3                   | fir4                   | fir5                   | fir5                   |                        |                        |
| 96x                                          | fir_3x                 | fir2                   | fir3                   | fir4                   | fir5                   | fir5                   |                        |                        |
| 128x                                         | fir1                   | fir2                   | fir3                   | fir4                   | fir4                   | fir5                   | fir5                   |                        |
| 192x                                         | fir_3x                 | fir2                   | fir3                   | fir4                   | fir4                   | fir5                   | fir5                   |                        |
| 256x                                         | fir1                   | fir2                   | fir3                   | fir4                   | fir4                   | fir4                   | fir5                   | fir5                   |



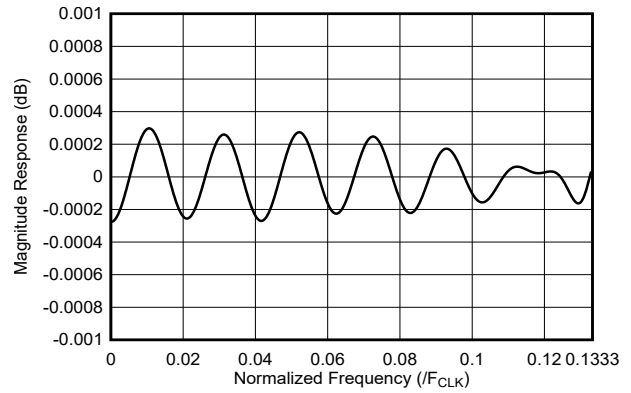
**Figure 7-14. 2x Interpolation Filter Response**



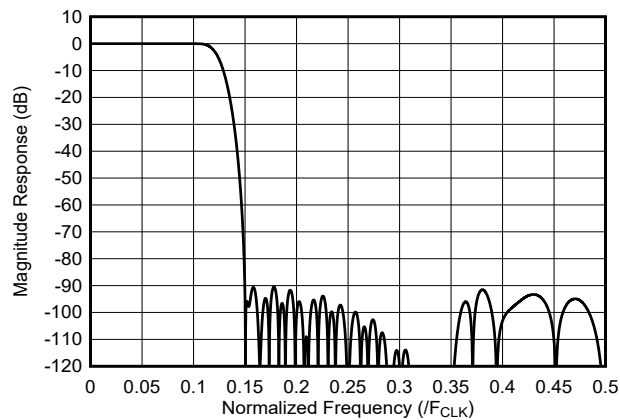
**Figure 7-15. 2x Interpolation Filter Passband Response**



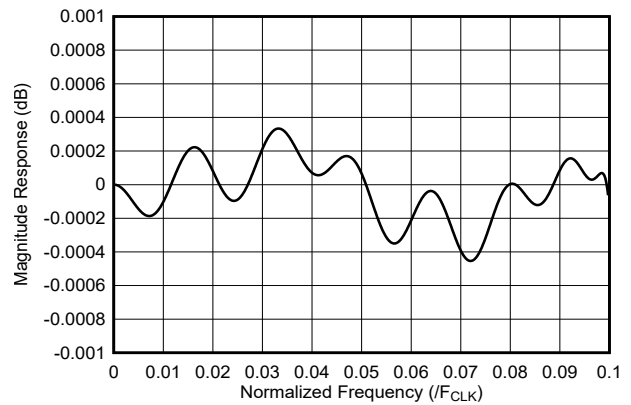
**Figure 7-16. 3x Interpolation Filter Response**



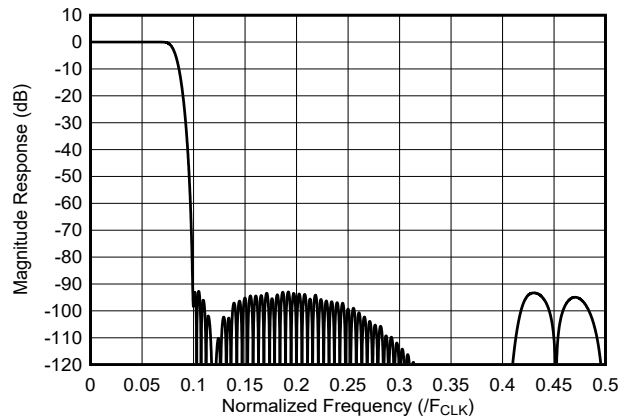
**Figure 7-17. 3x Interpolation Filter Passband Response**



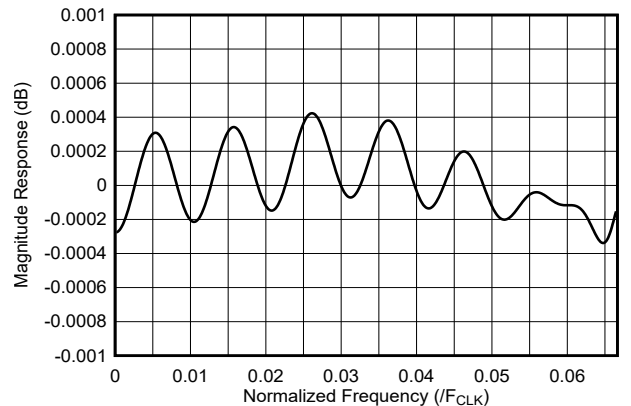
**Figure 7-18. 4x Interpolation Filter Response**



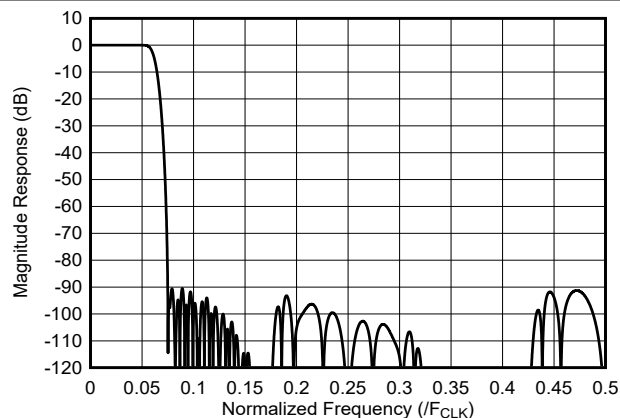
**Figure 7-19. 4x Interpolation Filter Passband Response**



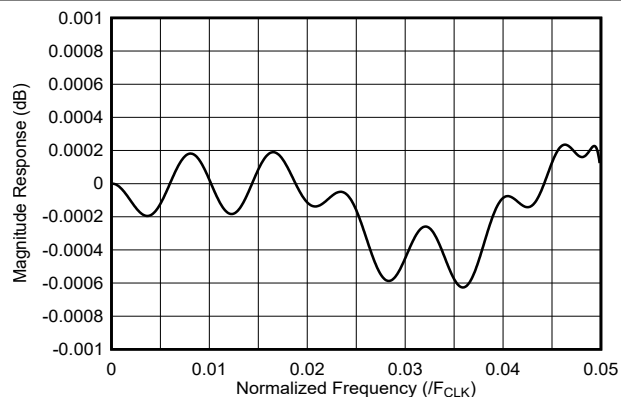
**Figure 7-20. 6x Interpolation Filter Response**



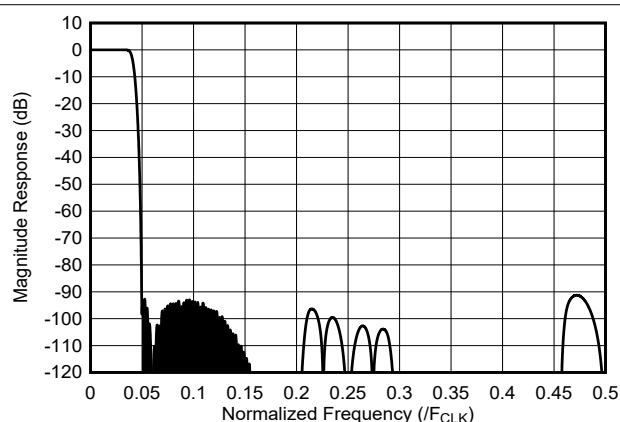
**Figure 7-21. 6x Interpolation Filter Passband Response**



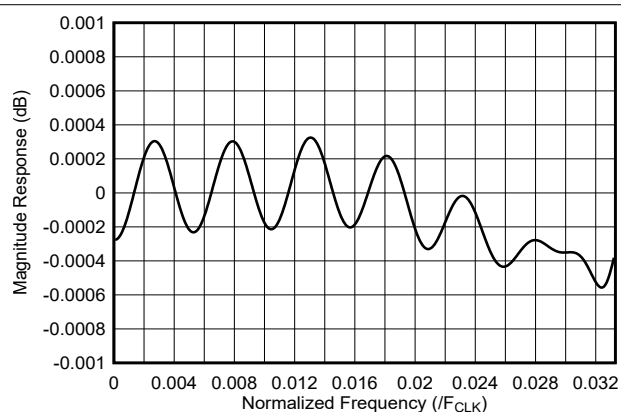
**Figure 7-22. 8x Interpolation Filter Response**



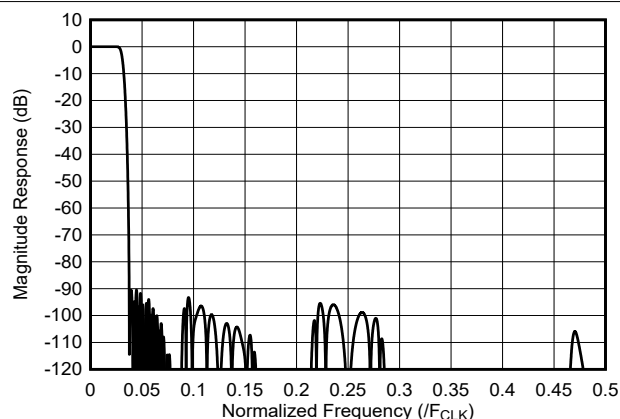
**Figure 7-23. 8x Interpolation Filter Passband Response**



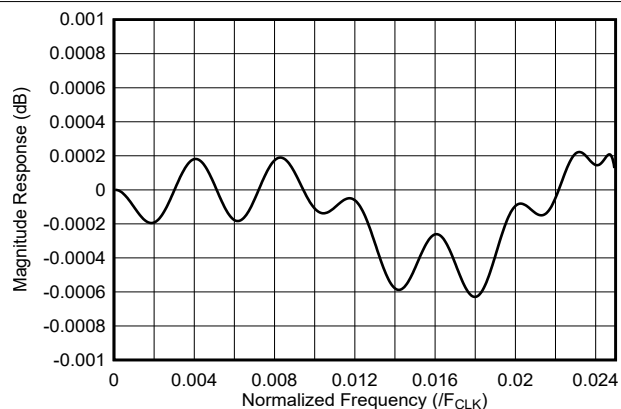
**Figure 7-24. 12x Interpolation Filter Response**



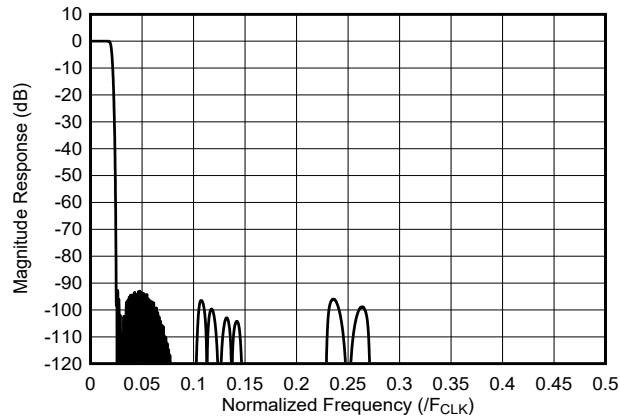
**Figure 7-25. 12x Interpolation Filter Passband Response**



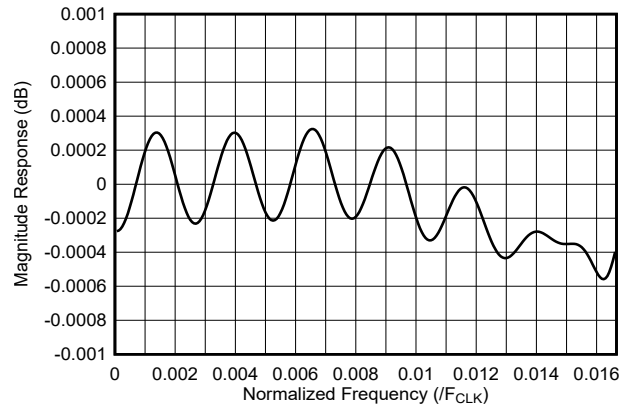
**Figure 7-26. 16x Interpolation Filter Response**



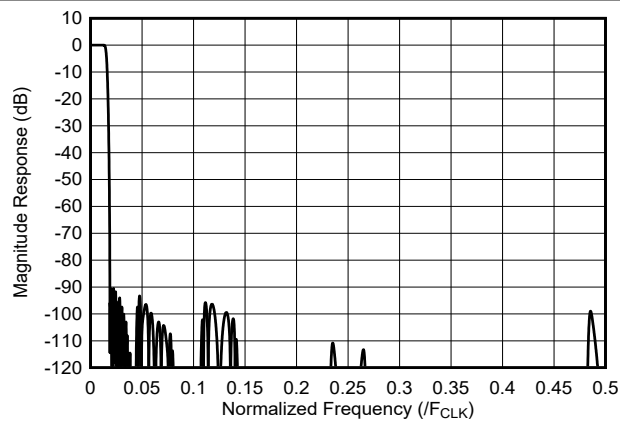
**Figure 7-27. 16x Interpolation Filter Passband Response**



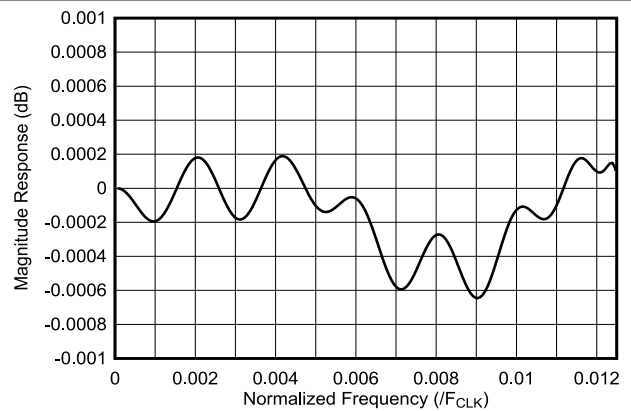
**Figure 7-28. 24x Interpolation Filter Response**



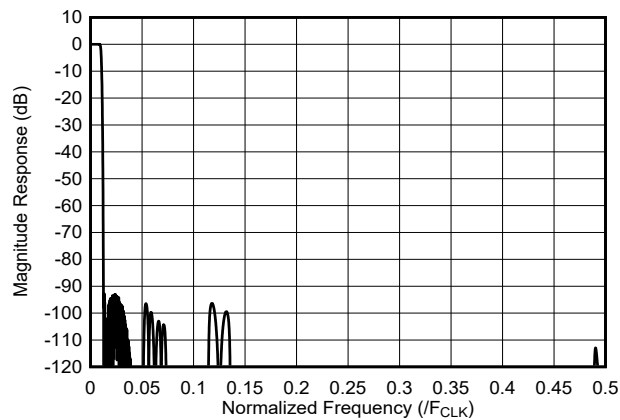
**Figure 7-29. 24x Interpolation Filter Passband Response**



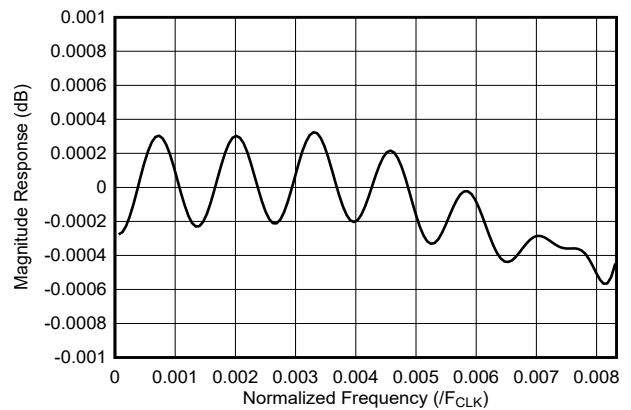
**Figure 7-30. 32x Interpolation Filter Response**



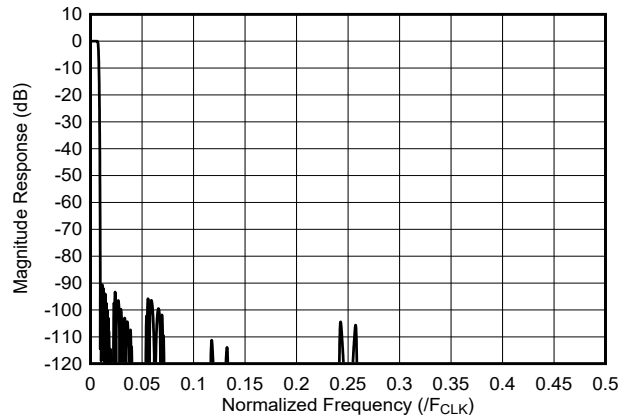
**Figure 7-31. 32x Interpolation Filter Passband Response**



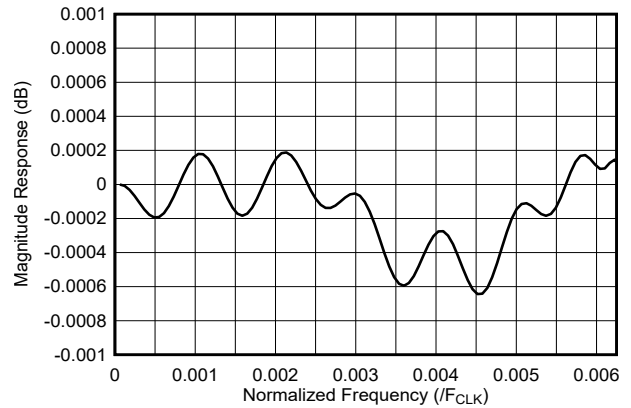
**Figure 7-32. 48x Interpolation Filter Response**



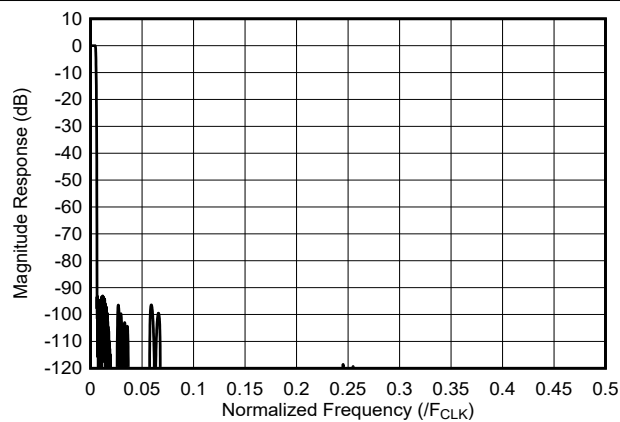
**Figure 7-33. 48x Interpolation Filter Passband Response**



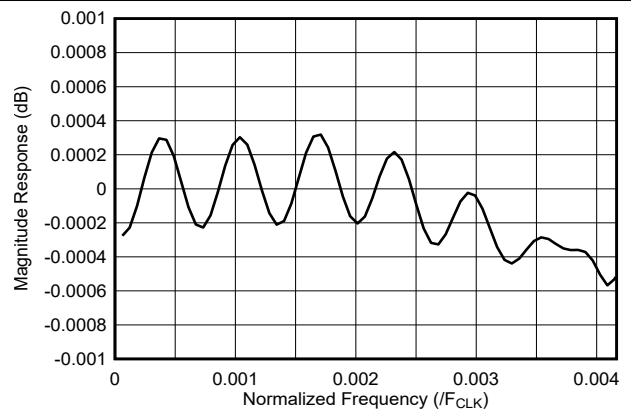
**Figure 7-34. 64x Interpolation Filter Response**



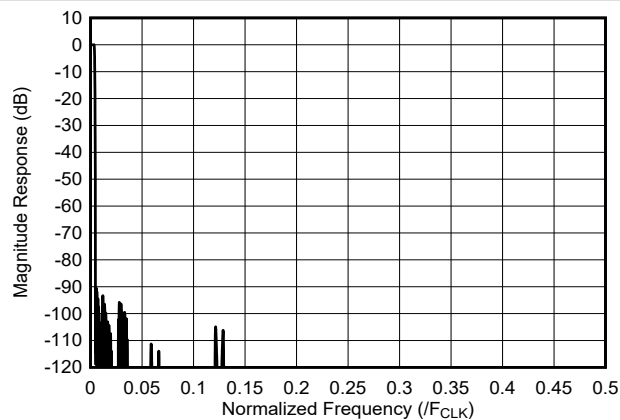
**Figure 7-35. 64x Interpolation Filter Passband Response**



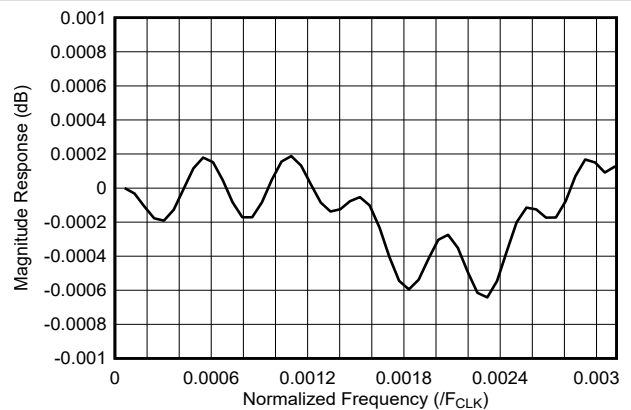
**Figure 7-36. 96x Interpolation Filter Response**



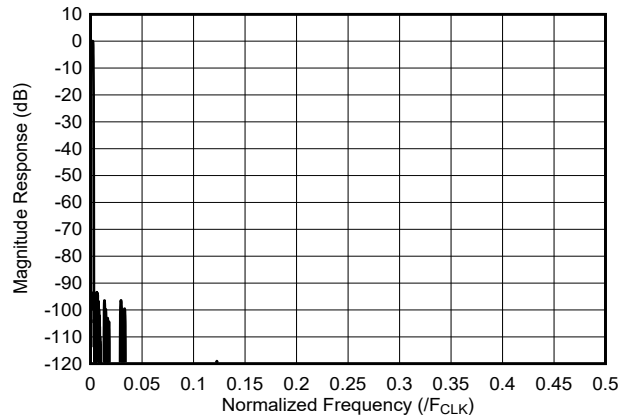
**Figure 7-37. 96x Interpolation Filter Passband Response**



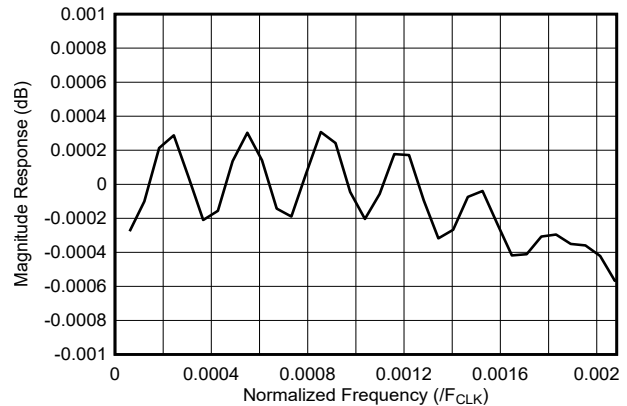
**Figure 7-38. 128x Interpolation Filter Response**



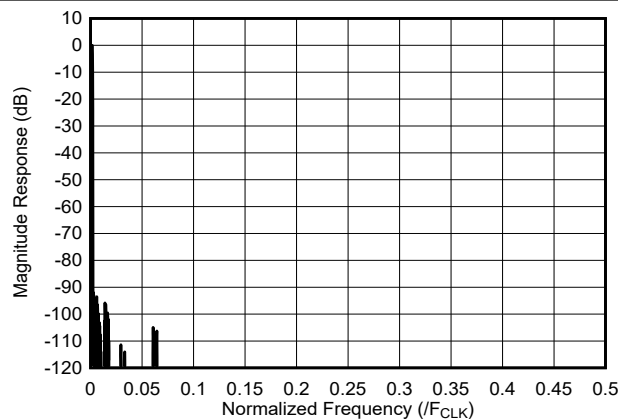
**Figure 7-39. 128x Interpolation Filter Passband Response**



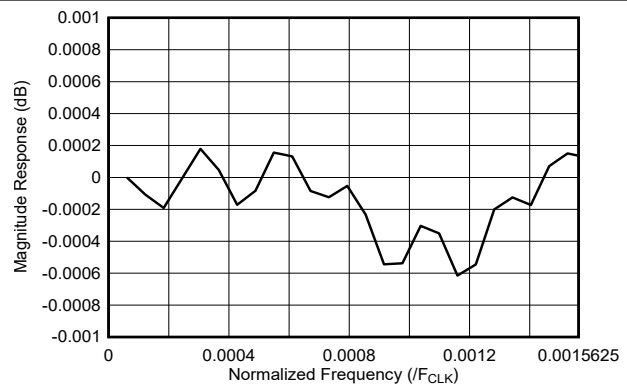
**Figure 7-40. 192x Interpolation Filter Response**



**Figure 7-41. 192x Interpolation Filter Passband Response**



**Figure 7-42. 256x Interpolation Filter Response**



**Figure 7-43. 256x Interpolation Filter Passband Response**

#### 7.3.6.1.2 Numerically Controlled Oscillator (NCO)

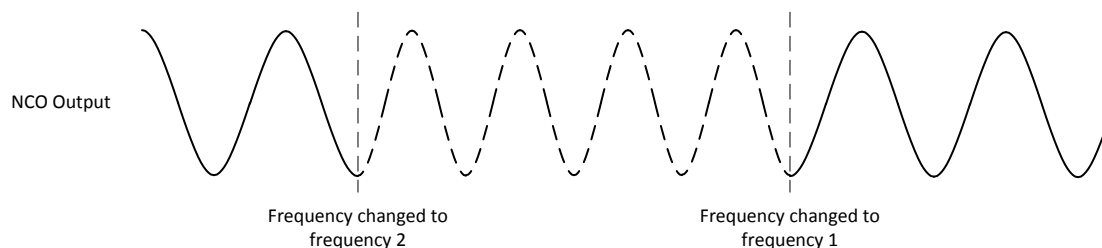
Each DUC has an NCO block that is capable of phase continuous frequency hopping and phase coherent frequency hopping through a NCO with 64-bit frequency and 16-bit phase words. The NCO provides the complex sinusoid that is used for the complex mixing operation. The NCOs can also be used with DDS mode to generate a tone without using the DUC filter path.

The NCO updates modes are either Phase-continuous (see [Phase-continuous NCO Update Mode](#)), Phase-coherent (see [Phase-coherent NCO Update Mode](#) or Phase-sync (see [Phase-sync NCO Update Mode](#)).

The NCO frequency is written to the NCO frequency word register setting through either the standard SPI interface or through the Fast Reconfiguration (FR) interface, which allows for faster frequency updates. The frequency update occurs either as soon as the new frequency word is written or once triggered by the chosen trigger source. Available trigger sources are a SPI register, the SYSREF signal or by replacing the LSB of the I input signal with a sync signal (determined by the NCO\_SYNC\_SRC register).

##### 7.3.6.1.2.1 Phase-Continuous NCO Update Mode

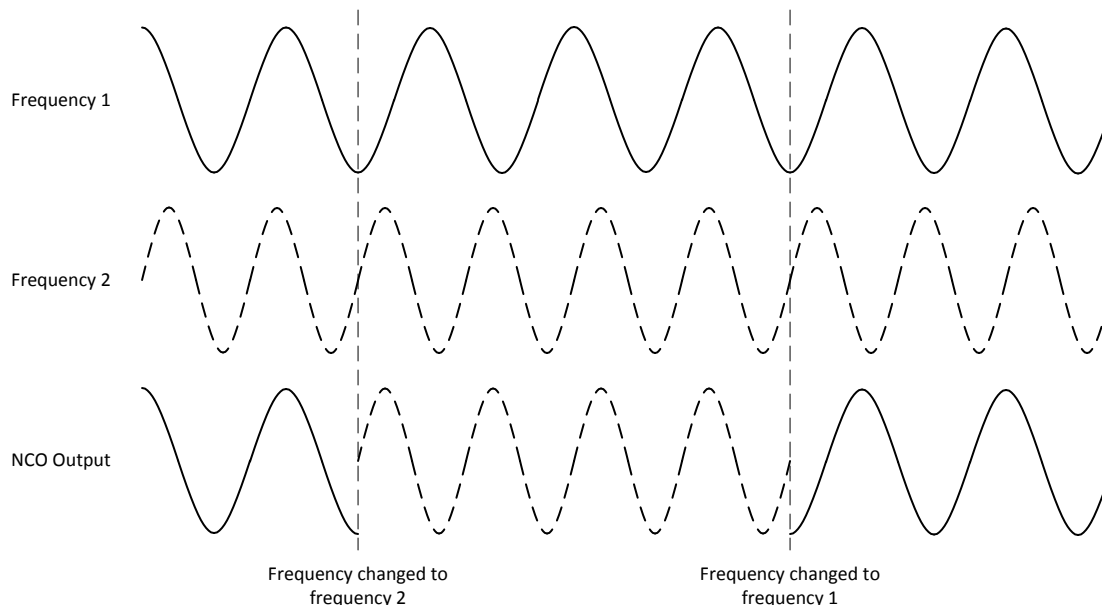
In phase-continuous NCO update mode, the phase frequency is updated without reset of the phase accumulator, which maintains the current sinusoid phase when changing frequency to reduce discontinuities in the output response. Phase Continuous NCO Mode operation is demonstrated in [Figure 7-44](#) and selected by programming `NCO_CONT` = 1 and `NCO_AR` = 0.



**Figure 7-44. Example Phase Continuous NCO Mode Operation**

#### 7.3.6.1.2.2 Phase-coherent NCO Update Mode

The phase-coherent NCO update mode, the frequency word is updated and is multiplied by a counter to update the accumulator. This allows the phase for a particular frequency to be "coherent" with the previous usage of the frequency as if the NCO had never been tuned away from that frequency. Since the phase information is maintained by the counter, any frequency can be phase coherent. Phase Coherent NCO Mode operation is demonstrated in [Figure 7-45](#) and selected by programming `NCO_CONT` = 0 and `NCO_AR` = 0. If alignment between multiple devices is required, then `NCO_AR` must be programmed to 1 during the initial NCO synchronization to align the master accumulator for all devices.



**Figure 7-45. Example Phase Coherent NCO Mode Operation**

#### 7.3.6.1.2.3 Phase-sync NCO Update Mode

In Phase-sync NCO update mode, the frequency word is updated (if it changed) and the accumulator is reset. This mode can be used to align the NCOs across multiple devices by providing a synchronization signal simultaneously across all devices. This mode is selected by programming `NCO_AR` = 1.

#### 7.3.6.1.2.4 NCO Synchronization

Many systems required synchronization between DAC channels including the phase of the internal NCOs when using digital up-conversion features. Further, frequency hopping systems may have additional requirements for synchronized frequency hopping to maintain NCO synchronization during changes in NCO frequency. The device has a number of ways to update NCO changes. These include:

- Synchronization through the LSB of the "I" input of DUC0 in the JESD204C input data stream
- Synchronization through SYSREF
- Update through SPI\_SYNC register bit
- Update on the rising edge of FRCS of the FRI interface if the FRS bit is set.

The method used for NCO synchronization is controlled through the register setting.

The JESD204C LSB approach allows the synchronization information to be embedded in the input data and can therefore be easily controlled by the data source (that is, FPGA). By controlling the timing of the synchronization bit across multiple devices, multi-device synchronization can be achieved.

Synchronization by issuing a SYSREF pulse requires a DC coupled SYSREF interface and the ability to issue a single SYSREF pulse unless the NCO frequency is an integer multiple of the SYSREF frequency. Many systems will use AC coupled SYSREF signals which eliminates the ability to reliably issue a single SYSREF pulse. Careful timing of the SPI interface, especially for very slow SYSREF signals (< 10 MHz), may make masking and unmasking of SYSREF at multiple devices possible, however it is not characterized since the SPI path is asynchronous.

With SPI\_SYNC synchronization, all NCOs within the device can be updated simultaneously.

#### 7.3.6.1.2.4.1 JESD204C LSB Synchronization

The NCO blocks can be synchronized using the LSB of the "I" input of the DUC0 channel on the JESD204C interface in complex input JMODES. Control bits that replace the LSB of the data samples are used to reset the NCO phase or an NCO frequency change. Table 7-11 show how the SYNC bit replaces the I sample LSB when using LSB replacement. The LSB replacement mode is enabled when the SPI\_SYNC register bit is high while NCO\_SYNC\_SRC is set to 3. To trigger the event, the LSB must be low for 4 or more consecutive samples, and then high for 4 consecutive samples. The sync coincides with the 4<sup>th</sup> high sample arriving at the DUC0 input. When using the SPI interface to update the NCO frequency word, the user must set SPI\_SYNC back to 0 to change back to the LSB representing I sample data. When using the FR interface to update the NCO, the LSB changes back to representing the I sample data after the synchronization event is triggered.

**Table 7-11. Bit Assignment using LSB Replacement**

| BIT      | 15      | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0    |
|----------|---------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|------|
| I Sample | I[15:1] |    |    |    |    |    |   |   |   |   |   |   |   |   |   | Sync |
| Q Sample | Q[15:0] |    |    |    |    |    |   |   |   |   |   |   |   |   |   |      |

#### 7.3.6.1.2.5 NCO Mode Programming

Table 7-13 and Table 7-12 show the register programming for the different NCO modes. Each NCO[n] can have separate mode selection.

**Table 7-12. NCO Programming: SPI Usage (FR\_EN = 0)**

| NCO_AR[n] | NCO_CONT[n] | Mode             |
|-----------|-------------|------------------|
| 0         | 0           | Phase Coherent   |
|           | 1           | Phase Continuous |
| 1         | 0           | Phase Reset      |
|           | 1           |                  |

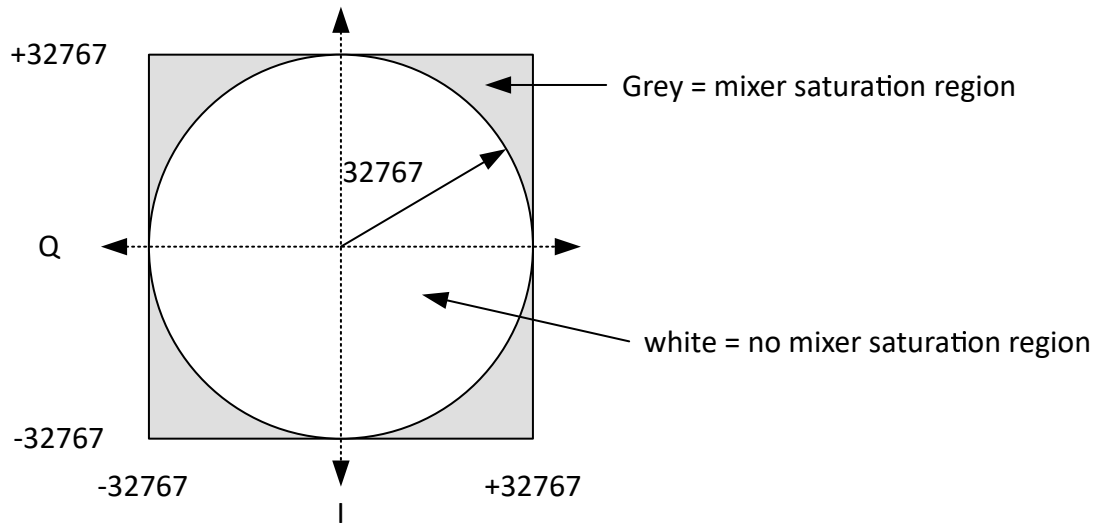
**Table 7-13. NCO Programming: FRI Usage (FR\_EN = 1)**

| FR_NCO_AR[n] | NCO_CONT[n] | Mode             |
|--------------|-------------|------------------|
| 0            | 0           | Phase Coherent   |
|              | 1           | Phase Continuous |
| 1            | 0           | Phase Reset      |
|              | 1           |                  |

#### 7.3.6.1.3 Mixer Scaling

The DUC mixer support complex to complex or complex to real mixing of the complex interpolated input signal with the NCO frequency. The scaling in the mixer is exactly 1:1, so a fullscale 16-bit (absolute amplitude = 32767) complex tone results in a fullscale real or complex tone at the output. If the input absolute value of the

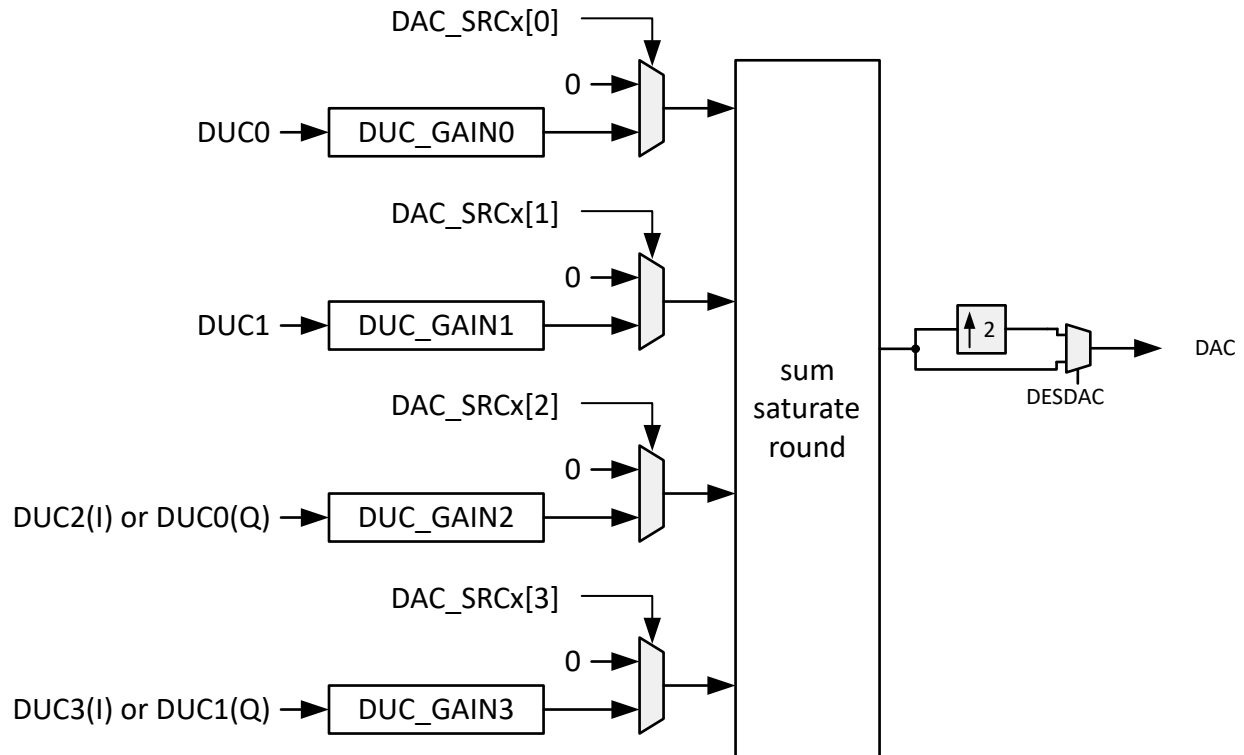
complex amplitude exceeds 32767 the mixer saturates, resulting in a corrupted waveform. This is illustrated in Figure 7-46, which shows the valid circular region in white and invalid corners in grey.



**Figure 7-46. Mixer Saturation Region for the 16-bit Complex Input**

#### 7.3.6.2 Channel Bonder

The channel bonder sits after the DUC blocks and is used to combine the outputs of the DUCs. A block diagram for one DAC channel is shown in Figure 7-47. The DUC outputs can be scaled by 1 (0 dB), 0.5 (-6 dB) or 0.25 (-12 dB) as set by the DUC\_GAIN registers to prevent saturation when summing the signals. The signals are summed at full precision as determined by the settings of the DAC\_SRC registers, and then saturation and rounding occurs on the combined signal. When the DUC outputs are real, up to four DUCs are available to be combined for each DAC. When the DUC outputs are complex, only two DUCs are available per DAC. The channel bonder can combine any combination of the real or complex DUC outputs for each DAC.



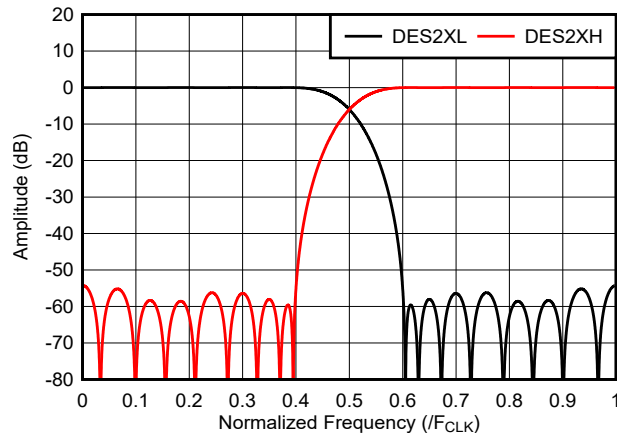
**Figure 7-47. Channel Bonder Block Diagram**

### 7.3.6.3 DES Interpolator

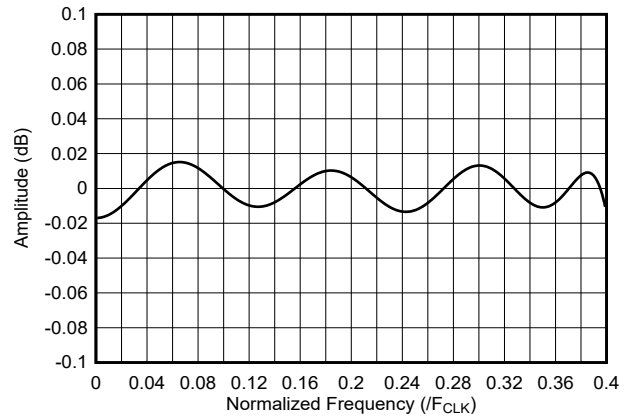
The output of the summation block or the non-interpolated input signal can optionally be interpolated by 2x by the DES interpolator to double the sample rate for DES2XL and DES2XH output modes. The DES interpolator has a passband bandwidth of 80%, stopband attenuation of 54dB and ripple less than  $\pm 0.02\text{dB}$ . The DES interpolator can operate as high pass (DES2XH) or low pass (DES2XL) with an inverted spectrum. The DES2X filter coefficients are listed in [Table 7-14](#) and the responses are shown in [Figure 7-48](#), with the passband ripple for DES2XL shown in [Figure 7-49](#). The sample rate after interpolation is  $2 \cdot f_{\text{CLK}}$  due to having samples on both the rising and falling edges, so the x-axis in [Figure 7-48](#) covers the Nyquist zone.

**Table 7-14. DES2X Filter Coefficients**

| Filter | Coefficients (center tap is in bold)                                                                                                                                                    |
|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DES2X  | $[-9 \ 0 \ 19 \ 0 \ -39 \ 0 \ 70 \ 0 \ -122 \ 0 \ 211 \ 0 \ -403 \ 0 \ 1293 \ \mathbf{2048} \ 1293 \ 0 \ -403 \ 0 \ 211 \ 0 \ -122 \ 0 \ 70 \ 0 \ -39 \ 0 \ 19 \ 0 \ -9] \cdot 2^{-11}$ |



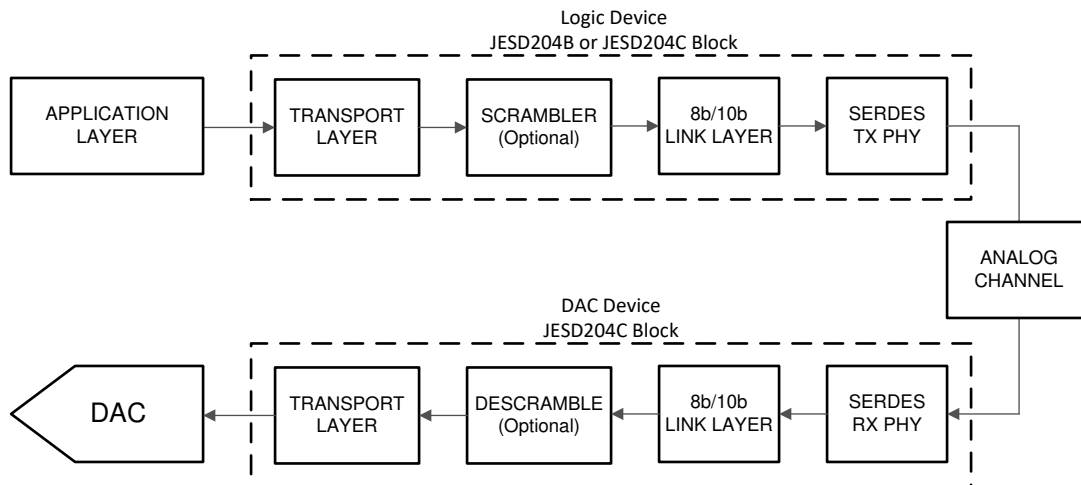
**Figure 7-48. DES Interpolator Frequency Response**



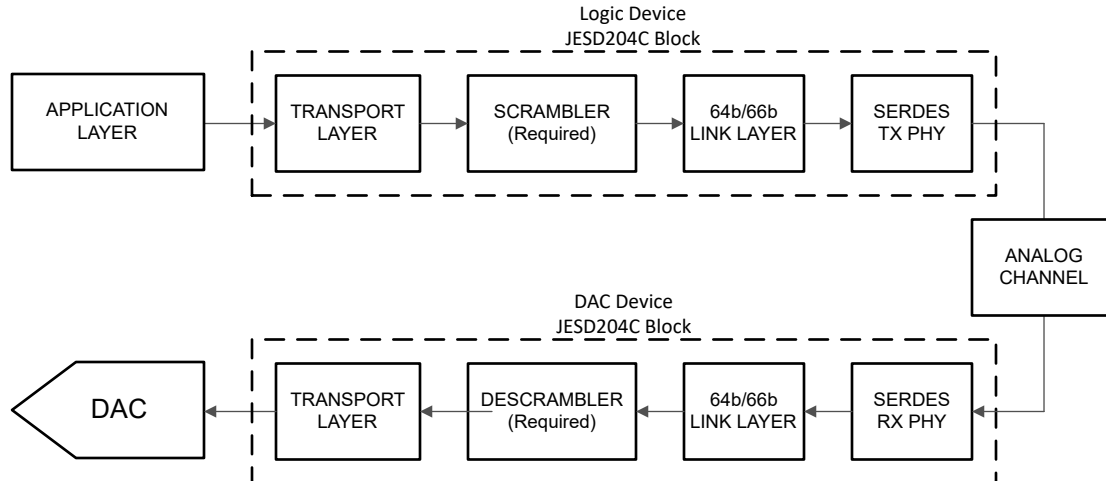
**Figure 7-49. DES Interpolator Frequency Response (Passband)**

### 7.3.7 JESD204C Interface

The devices use a JESD204C high-speed serial interface to transfer data from the logic device to the receiving DAC. The device serial lanes are capable of operating with both 8b/10b encoding and 64b/66b encoding. The JESD204C formats using 8b/10b encoding are backwards compatible with existing JESD204B receivers. A maximum of 2 lanes can be used to lower lane rates for interfacing with speed limited logic devices. There are a few differences between 8b/10b and 64b/66b encoding, which is highlighted throughout this section. [Figure 7-50](#) shows a simplified block diagram of the 8b/10b encoded JESD204C interface and [Figure 7-51](#) shows a simplified block diagram of the 64b/66b encoded JESD204C interface.



**Figure 7-50. Simplified JESD204C Interface Diagram with 8b/10b Encoding**



**Figure 7-51. Simplified JESD204C Interface Diagram with 64b/66b Encoding**

Not all optional features of JESD204C are supported by the device. The list of features that are supported and the features that are not supported is provided in [Table 7-15](#)

**Table 7-15. Declaration of Supported JESD204C Features**

| LETTER IDENTIFIER | FEATURE                                                                                         | SUPPORTED BY DEVICE? |
|-------------------|-------------------------------------------------------------------------------------------------|----------------------|
| a                 | 8b/10b link layer                                                                               | Yes                  |
| b                 | 64b/66b link layer                                                                              | Yes                  |
| c                 | 64b/80b link layer                                                                              | No                   |
| d                 | The command channel when using 64b/66b or 64b/80b link layer                                    | No                   |
| e                 | Forward error correction (FEC) when using the 64b/66b or 64b/80b link layer                     | No                   |
| f                 | CRC3 when using the 64b/66b or 64b/80b link layer                                               | No                   |
| g                 | A physical SYNC pin when using the 8b/10b link layer                                            | Yes                  |
| h                 | Subclass 0                                                                                      | Yes                  |
| i                 | Subclass 1                                                                                      | Yes                  |
| j                 | Subclass 2                                                                                      | No                   |
| k                 | Lane alignment within a single link                                                             | Yes                  |
| l                 | Subclass 1 with support for lane alignment on a multipoint link by means of the MULTIREF signal | No                   |
| m                 | SYNC interface timing compatible with JESD204A                                                  | Yes                  |
| n                 | SYNC interface timing compatible with JESD204B                                                  | Yes                  |

The various signals used in the JESD204C interface and the associated device pin names are summarized briefly in [Table 7-16](#) for reference.

**Table 7-16. Summary of JESD204C Signals**

| SIGNAL NAME | DEVICE PIN NAMES | DESCRIPTION                                                                                           |
|-------------|------------------|-------------------------------------------------------------------------------------------------------|
| Data        | 6SRX±, 14SRX±    | High-speed serialized data after 8b/10b or 64b/66b encoding that is received by the SerDes receivers. |

**Table 7-16. Summary of JESD204C Signals (continued)**

| SIGNAL NAME              | DEVICE PIN NAMES         | DESCRIPTION                                                                                                                                                                   |
|--------------------------|--------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $\overline{\text{SYNC}}$ | $\overline{\text{SYNC}}$ | Link initialization signal (handshake), toggles low to start code group synchronization (CGS) process. Not used for 64B/66B encoding modes.                                   |
| Device clock             | CLK+, CLK–               | DAC sampling clock, also used for clocking digital logic and SerDes receivers.                                                                                                |
| SYSREF                   | SYSREF+, SYSREF–         | System timing reference used to deterministically reset the internal local multiframe clock (LMFC) or local extended multiblock clock (LEMC) counters in each JESD204C device |

### 7.3.7.1 Deviation from JESD204C Standard

JESD204C section 4.3.4 requires subclass 1 devices to be able to measure the amount of device clock cycles by which the detected active edge of the SYSREF signal deviates from its expected position and not to re-align the LMFC/LEMC if the deviation from the expected position is less than a programmable number of device clock cycles. This design does not contain this feature, but is compliant with JESD204B in this regard. The LMFC and other supporting clocks are aligned to the detected SYSREF if the JESD204C subsystem and SYSREF processor are enabled (and SYSREF\_ALIGN\_EN=1).

### 7.3.7.2 Transport Layer

In the transmitter (logic device) the transport layer takes samples from the application layer and maps the samples into octets inside of frames. The frames are then mapped onto the available SerDes lanes. In the receiver (DAC) the transport layer performs the inverse operation to extract samples from the serialized data. The mapping of octets into frames and frames onto lanes is defined by the transport layer settings such as L, M, F, S, N and N'. An octet is 8 bits (before 8b/10b or 64b/66b encoding), a frame consists of F octets and the frames are mapped onto L lanes. Samples are N bits, but sent as N' bits across the link. The samples come from M converters and there are S samples per converter per frame cycle.

There are a number of predefined transport layer modes in the device that are defined in [JESD204C Interface Modes](#). The various configuration parameters for JESD204C block are defined in [JESD204C Interface Parameter Definitions](#).

The link layer further maps the frames into multiframe.

### 7.3.7.3 Scrambler and Descrambler

A data descrambler is available in the DAC device to descramble the data after reception. Scrambling is used to remove the possibility of spectral peaks in the transmitted data due to repetitive data streams. The scrambler is optional for 8b/10b encoded mode, however it is mandatory for 64b/66b encoded mode to have sufficient spectral content for clock recovery and adaptive equalization. The scrambler operates on the data before encoding, such that the 8b/10b scrambler scrambles the 8-bit octets before 10-bit encoding and the 64b/66b scrambler scrambles the 64-bit block before the sync header insertion (66-bit encoding). The JESD204C receiver automatically synchronizes its descrambler to the incoming scrambled data stream. For 8b/10b encoding, the initial lane alignment sequence (ILAS) is never scrambled. The descrambler can be enabled by setting SCR for 8b/10b encoding mode, but it is automatically enabled in 64b/66b mode. The scrambling polynomial is different for 8b/10b encoding and 64b/66b encoding schemes as defined by the JESD204C standard.

### 7.3.7.4 Link Layer

The link layer serves multiple purposes in JESD204C for both 8b/10b and 64b/66b encoding modes, however there are some differences in implementation for each encoding scheme. In general, the link layer responsibilities include scrambling of the data (see [Scrambler and Descrambler](#)), establishing the code (8b/10b)

or block (64b/66b) boundaries and the multiframe (8b/10b) or multiblock (64b/66b) boundaries to deskew the SerDes lanes, initializing the link, encoding the data, and monitoring the health of the link.

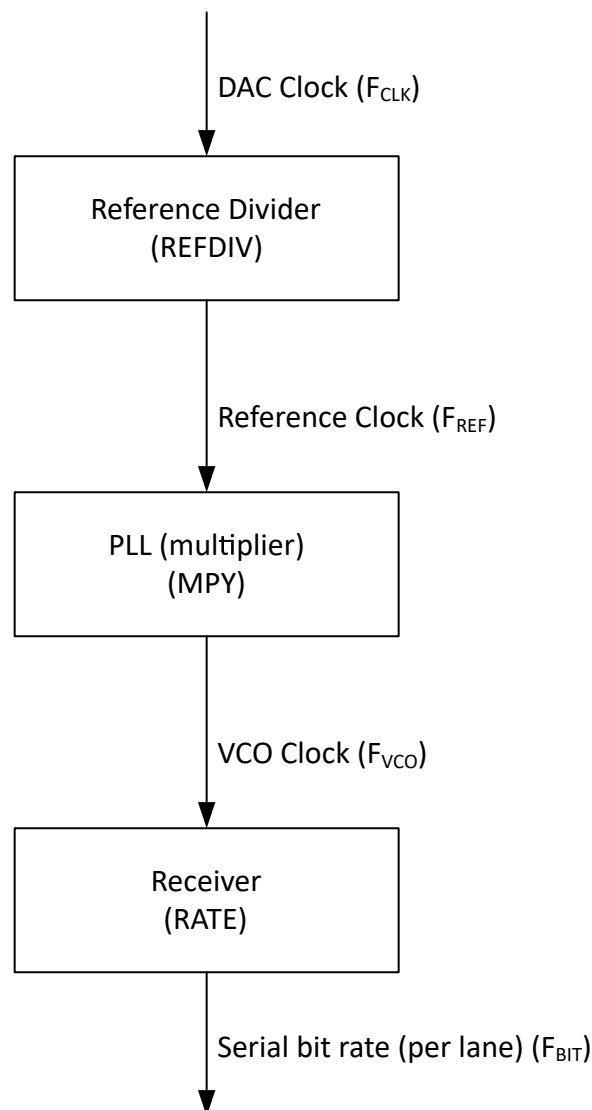
### 7.3.7.5 Physical Layer

The devices JESD204C physical layer contains 16 SerDes receivers. Each SerDes lane has a Continuous Time Linear Equalizer (CTLE) for channel loss equalization.

### 7.3.7.6 Serdes PLL Control

The Serdes receivers work over a wide frequency range if various parameters are altered. Before setting **JESD\_EN**, the user must program various parameters for the Serdes receivers to work. The parameters are adjusted to maintain all these constraints:

1. The VCO clock frequency ( $F_{VCO}$ ) must be between 1.5625 GHz and 3.2 GHz.
2. When the VCO clock frequency ( $F_{VCO}$ ) is below 2.17 GHz, **VRANGE** must be set.
3. The **REFDIV**, **MPY** and **RATE** settings are all associated with a frequency change. The product of all the frequency changes must match the R value for the selected **JMODE**.
4. Settings with a higher PLL reference clock (and smaller **MPY** multiplier) are preferred.



**Figure 7-52. Serdes Clock Frequency Generation**

**Table 7-17. PLL Configuration Table for 8b/10b Encoding Modes**

| R decimal (fraction) | CLK Range (F <sub>CLK</sub> ) (GHz) | Register Values to Program |      |      |                             | Actual Frequency Multipliers |     |      | Lane Bit Rate (Gbps) |
|----------------------|-------------------------------------|----------------------------|------|------|-----------------------------|------------------------------|-----|------|----------------------|
|                      |                                     | REFDIV                     | MPY  | RATE | VRANGE                      | REFDIV                       | MPY | RATE |                      |
| 0.3125 (40/128)      | 2.5-5.12                            | 0x08                       | 0x14 | 0x3  | F <sub>CLK</sub> <3.472GHz  | 1/8                          | 5   | 0.5  | 0.78125 – 1.6        |
| 0.3125 (40/128)      | 5.0-10.24                           | 0x10                       | 0x14 | 0x2  | F <sub>CLK</sub> <6.994GHz  | 1/16                         | 5   | 1    | 1.5625 – 3.2         |
| 0.3125 (40/128)      | 10.0-12.8                           | 0x20                       | 0x14 | 0x1  | 1                           | 1/32                         | 5   | 2    | 3.125 – 4.0          |
| 0.4167 (40/96)       | 1.88-3.84                           | 0x06                       | 0x14 | 0x3  | F <sub>CLK</sub> <2.604GHz  | 1/6                          | 5   | 0.5  | 0.78125 – 1.6        |
| 0.4167 (40/96)       | 3.75-7.68                           | 0x0C                       | 0x14 | 0x2  | F <sub>CLK</sub> <5.208GHz  | 1/12                         | 5   | 1    | 1.5625 – 3.2         |
| 0.4167 (40/96)       | 7.50-12.8                           | 0x18                       | 0x14 | 0x1  | F <sub>CLK</sub> <10.416GHz | 1/24                         | 5   | 2    | 3.125 – 5.333        |
| 0.625 (40/64)        | 1.25-2.56                           | 0x04                       | 0x14 | 0x3  | F <sub>CLK</sub> <1.736GHz  | 1/4                          | 5   | 0.5  | 0.78125 – 1.6        |
| 0.625 (40/64)        | 2.5-5.12                            | 0x08                       | 0x14 | 0x2  | F <sub>CLK</sub> <3.472GHz  | 1/8                          | 5   | 1    | 1.5625 – 3.2         |
| 0.625 (40/64)        | 5.00-10.24                          | 0x10                       | 0x14 | 0x1  | F <sub>CLK</sub> <6.994GHz  | 1/16                         | 5   | 2    | 3.125 – 6.4          |
| 0.625 (40/64)        | 10.00-12.8                          | 0x20                       | 0x14 | 0x0  | 1                           | 1/32                         | 5   | 4    | 6.25 – 8.0           |
| 0.833 (40/48)        | 0.94-1.92                           | 0x03                       | 0x14 | 0x3  | F <sub>CLK</sub> <1.302GHz  | 1/3                          | 5   | 0.5  | 0.78125 – 1.6        |
| 0.833 (40/48)        | 1.88-3.84                           | 0x06                       | 0x14 | 0x2  | F <sub>CLK</sub> <2.604GHz  | 1/6                          | 5   | 1    | 1.5625 – 3.2         |
| 0.833 (40/48)        | 3.75-7.68                           | 0x0C                       | 0x14 | 0x1  | F <sub>CLK</sub> <5.208GHz  | 1/12                         | 5   | 2    | 3.125 – 6.4          |
| 0.833 (40/48)        | 7.50-12.8                           | 0x18                       | 0x14 | 0x0  | F <sub>CLK</sub> <10.416GHz | 1/24                         | 5   | 4    | 6.25 – 10.667        |
| 1 (40/40)            | 0.781-1.6                           | 0x02                       | 0x10 | 0x3  | F <sub>CLK</sub> <1.085GHz  | 1/2                          | 4   | 0.5  | 0.78125 – 1.6        |
| 1 (40/40)            | 1.5625-3.2                          | 0x04                       | 0x10 | 0x2  | F <sub>CLK</sub> <2.17GHz   | 1/4                          | 4   | 1    | 1.5625 – 3.2         |
| 1 (40/40)            | 3.125-6.4                           | 0x08                       | 0x10 | 0x1  | F <sub>CLK</sub> <4.34GHz   | 1/8                          | 4   | 2    | 3.125 – 6.4          |
| 1 (40/40)            | 6.25-12.8                           | 0x10                       | 0x10 | 0x0  | F <sub>CLK</sub> <8.68GHz   | 1/16                         | 4   | 4    | 6.25 – 12.8          |
| 1.25 (40/32)         | 0.625-1.28                          | 0x02                       | 0x14 | 0x3  | F <sub>CLK</sub> <0.868GHz  | 1/2                          | 5   | 0.5  | 0.78125 – 1.6        |
| 1.25 (40/32)         | 1.25-2.56                           | 0x04                       | 0x14 | 0x2  | F <sub>CLK</sub> <1.736GHz  | 1/4                          | 5   | 1    | 1.5625 – 3.2         |
| 1.25 (40/32)         | 2.5-5.12                            | 0x08                       | 0x14 | 0x1  | F <sub>CLK</sub> <3.472GHz  | 1/8                          | 5   | 2    | 3.125 – 6.4          |
| 1.25 (40/32)         | 5.0-10.24                           | 0x10                       | 0x14 | 0x0  | F <sub>CLK</sub> <6.994GHz  | 1/16                         | 5   | 4    | 6.25 – 12.8          |
| 1.667 (40/24)        | 0.47-0.96                           | 0x03                       | 0x28 | 0x3  | F <sub>CLK</sub> <0.651GHz  | 1/3                          | 10  | 0.5  | 0.78125 – 1.6        |
| 1.667 (40/24)        | 0.94-1.92                           | 0x03                       | 0x14 | 0x2  | F <sub>CLK</sub> <1.302GHz  | 1/3                          | 5   | 1    | 1.5625 – 3.2         |
| 1.667 (40/24)        | 1.88-3.84                           | 0x06                       | 0x14 | 0x1  | F <sub>CLK</sub> <2.604GHz  | 1/6                          | 5   | 2    | 3.125 – 6.4          |
| 1.667 (40/24)        | 3.75-7.68                           | 0x0C                       | 0x14 | 0x0  | F <sub>CLK</sub> <5.208GHz  | 1/12                         | 5   | 4    | 6.25 – 12.8          |
| 2 (40/20)            | 0.781-1.6                           | 0x02                       | 0x10 | 0x2  | F <sub>CLK</sub> <1.085GHz  | 1/2                          | 4   | 1    | 1.5625 – 3.2         |
| 2 (40/20)            | 1.5625-3.2                          | 0x04                       | 0x10 | 0x1  | F <sub>CLK</sub> <2.17GHz   | 1/4                          | 4   | 2    | 3.125 – 6.4          |
| 2 (40/20)            | 3.125-6.4                           | 0x08                       | 0x10 | 0x0  | F <sub>CLK</sub> <4.34GHz   | 1/8                          | 4   | 4    | 6.25 – 12.8          |
| 2.5 (40/16)          | 0.625-1.28                          | 0x02                       | 0x14 | 0x2  | F <sub>CLK</sub> <0.868GHz  | 1/2                          | 5   | 1    | 1.5625 – 3.2         |
| 2.5 (40/16)          | 1.25-2.56                           | 0x04                       | 0x14 | 0x1  | F <sub>CLK</sub> <1.736GHz  | 1/4                          | 5   | 2    | 3.125 – 6.4          |
| 2.5 (40/16)          | 2.5-5.12                            | 0x08                       | 0x14 | 0x0  | F <sub>CLK</sub> <3.472GHz  | 1/8                          | 5   | 4    | 6.25 – 12.8          |
| 3.3333 (40/12)       | 0.47 – 0.96                         | 0x03                       | 0x28 | 0x2  | F <sub>CLK</sub> <0.651GHz  | 1/3                          | 10  | 1    | 1.5625 – 3.2         |
| 3.3333 (40/12)       | 0.94 – 1.92                         | 0x03                       | 0x14 | 0x1  | F <sub>CLK</sub> <1.302GHz  | 1/3                          | 5   | 2    | 3.125 – 6.4          |
| 3.3333 (40/12)       | 1.88 – 3.84                         | 0x06                       | 0x14 | 0x0  | F <sub>CLK</sub> <2.604GHz  | 1/6                          | 5   | 4    | 6.25 – 12.8          |
| 4 (40/10)            | 0.781 – 1.6                         | 0x02                       | 0x10 | 0x1  | F <sub>CLK</sub> <1.085GHz  | 1/2                          | 4   | 2    | 3.125 – 6.4          |
| 4 (40/10)            | 1.5625 – 3.2                        | 0x04                       | 0x10 | 0x0  | F <sub>CLK</sub> <2.17GHz   | 1/4                          | 4   | 4    | 6.25 – 12.8          |
| 5 (40/8)             | 0.625-1.28                          | 0x02                       | 0x14 | 0x1  | F <sub>CLK</sub> <0.868GHz  | 1/2                          | 5   | 2    | 3.125 – 6.4          |
| 5 (40/8)             | 1.25-2.56                           | 0x04                       | 0x14 | 0x0  | F <sub>CLK</sub> <1.736GHz  | 1/4                          | 5   | 4    | 6.25 – 12.8          |

**Table 7-18. PLL Configuration Table for 64b/66b Encoding Modes**

| R decimal (fraction) | CLK Range (F <sub>CLK</sub> ) (GHz) | Register Values to Program |      |      |                             | Actual Frequency Multipliers |      |      | Lane Bit Rate (F <sub>BIT</sub> ) (Gbps) |
|----------------------|-------------------------------------|----------------------------|------|------|-----------------------------|------------------------------|------|------|------------------------------------------|
|                      |                                     | REFDIV                     | MPY  | RATE | VRANGE                      | REFDIV                       | MPY  | RATE |                                          |
| 0.515625 (33/64)     | 6.06 – 12.41                        | 0x20                       | 0x21 | 0x1  | F <sub>CLK</sub> <8.417GHz  | 1/32                         | 8.25 | 2    | 3.125 – 6.4                              |
| 0.6875 (33/48)       | 4.55 – 9.31                         | 0x18                       | 0x21 | 0x1  | F <sub>CLK</sub> <6.313GHz  | 1/24                         | 8.25 | 2    | 3.125 – 6.4                              |
| 0.6875 (33/48)       | 9.09 – 12.8                         | 0x30                       | 0x21 | 0x0  | F <sub>CLK</sub> <12.625GHz | 1/48                         | 8.25 | 4    | 6.25 – 8.8                               |
| 0.825 (33/40)        | 3.79 – 7.76                         | 0x14                       | 0x21 | 0x1  | F <sub>CLK</sub> <5.261GHz  | 1/20                         | 8.25 | 2    | 3.125 – 6.4                              |
| 0.825 (33/40)        | 7.58 – 12.8                         | 0x28                       | 0x21 | 0x0  | F <sub>CLK</sub> <10.521GHz | 1/40                         | 8.25 | 4    | 6.25 – 10.56                             |
| 1.03125 (33/32)      | 3.03 – 6.21                         | 0x10                       | 0x21 | 0x1  | F <sub>CLK</sub> <4.208GHz  | 1/16                         | 8.25 | 2    | 3.125 – 6.4                              |
| 1.03125 (33/32)      | 6.06 – 12.41                        | 0x20                       | 0x21 | 0x0  | F <sub>CLK</sub> <8.417GHz  | 1/32                         | 8.25 | 4    | 6.25 – 12.8                              |
| 1.375 (33/24)        | 2.27 – 4.65                         | 0x0C                       | 0x21 | 0x1  | F <sub>CLK</sub> <3.156GHz  | 1/12                         | 8.25 | 2    | 3.125 – 6.4                              |
| 1.375 (33/24)        | 4.55 – 9.31                         | 0x18                       | 0x21 | 0x0  | F <sub>CLK</sub> <6.313GHz  | 1/24                         | 8.25 | 4    | 6.25 – 12.8                              |
| 1.65 (33/20)         | 1.89 – 3.88                         | 0x0A                       | 0x21 | 0x1  | F <sub>CLK</sub> <2.630GHz  | 1/10                         | 8.25 | 2    | 3.125 – 6.4                              |
| 1.65 (33/20)         | 3.79 – 7.76                         | 0x14                       | 0x21 | 0x0  | F <sub>CLK</sub> <5.261GHz  | 1/20                         | 8.25 | 4    | 6.25 – 12.8                              |

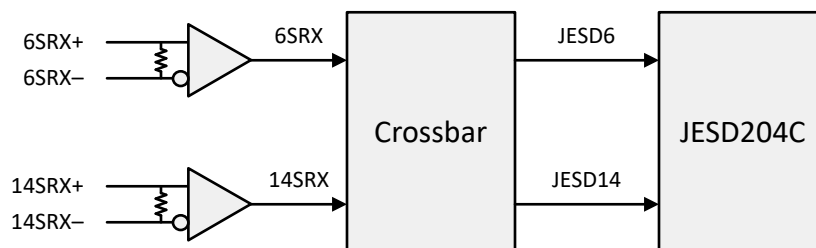
**Table 7-18. PLL Configuration Table for 64b/66b Encoding Modes (continued)**

| R decimal (fraction) | CLK Range (F <sub>CLK</sub> ) (GHz) | Register Values to Program |      |      |                             | Actual Frequency Multipliers |      |      | Lane Bit Rate (F <sub>BIT</sub> ) (Gbps) |
|----------------------|-------------------------------------|----------------------------|------|------|-----------------------------|------------------------------|------|------|------------------------------------------|
|                      |                                     | REFDIV                     | MPY  | RATE | VRANGE                      | REFDIV                       | MPY  | RATE |                                          |
| 2.0625 (33/16)       | 1.52 – 3.10                         | 0x08                       | 0x21 | 0x1  | F <sub>CLK</sub> < 2.104GHz | 1/8                          | 8.25 | 2    | 3.125 – 6.4                              |
| 2.0625 (33/16)       | 3.03 – 6.21                         | 0x10                       | 0x21 | 0x0  | F <sub>CLK</sub> < 4.208GHz | 1/16                         | 8.25 | 4    | 6.25 – 12.8                              |
| 2.75 (33/12)         | 1.14 – 2.33                         | 0x06                       | 0x21 | 0x1  | F <sub>CLK</sub> < 1.578GHz | 1/6                          | 8.25 | 2    | 3.125 – 6.4                              |
| 2.75 (33/12)         | 2.27 – 4.65                         | 0x0C                       | 0x21 | 0x0  | F <sub>CLK</sub> < 3.156GHz | 1/12                         | 8.25 | 4    | 6.25 – 12.8                              |
| 3.3 (33/10)          | 0.95 – 1.94                         | 0x05                       | 0x21 | 0x1  | F <sub>CLK</sub> < 1.315GHz | 1/5                          | 8.25 | 2    | 3.125 – 6.4                              |
| 3.3 (33/10)          | 1.89 – 3.88                         | 0x0A                       | 0x21 | 0x0  | F <sub>CLK</sub> < 2.630GHz | 1/10                         | 8.25 | 4    | 6.25 – 12.8                              |
| 4.125 (33/8)         | 0.76 – 1.55                         | 0x04                       | 0x21 | 0x1  | F <sub>CLK</sub> < 1.052GHz | 1/4                          | 8.25 | 2    | 3.125 – 6.4                              |
| 4.125 (33/8)         | 1.52 – 3.10                         | 0x08                       | 0x21 | 0x0  | F <sub>CLK</sub> < 2.104GHz | 1/8                          | 8.25 | 4    | 6.25 – 12.8                              |

### 7.3.7.7 Serdes Crossbar

The device includes a crossbar immediately after coming out of the PHY that allows mapping of signals between lanes to simplify PCB routing between the Tx and Rx which could save PCB complexity or shorten the traces (reduce loss). See LANE\_SEL *n*.

The physical layer lanes (6SRX±, 14SRX±) must be routed to the appropriate JESD204C lanes (JESD0 to JESD15) based on the lanes defined in the bit packing diagrams shown in [JESD204C Format Diagrams](#).



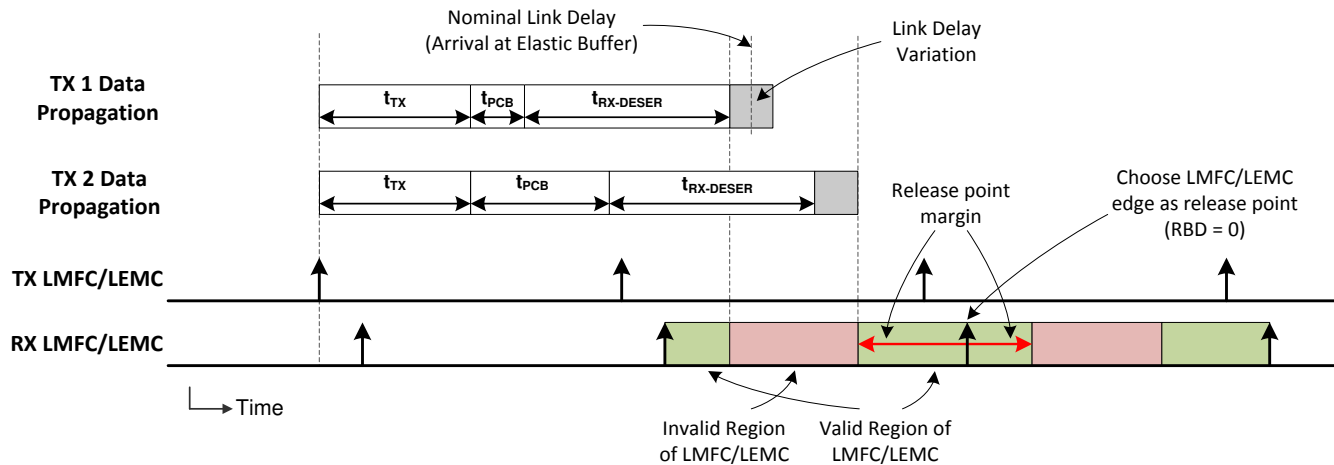
**Figure 7-53. Crossbar Block Diagram**

### 7.3.7.8 Multi-Device Synchronization and Deterministic Latency

JESD204C subclass 1 outlines a method to achieve deterministic latency across the serial link. If two devices achieve the same deterministic latency then the devices are considered synchronized. This latency must be achieved from system startup to startup to be deterministic. There are two key requirements to achieve deterministic latency. The first is proper capture of SYSREF. SYSREF resets the LMFC counter in each device to act as a known timing reference.

The second requirement is to choose a proper elastic buffer release point in the receiver. The converter device is the receiver (RX) in the JESD204C link and the logic device is the transmitter (TX). The elastic buffer is the key block for achieving deterministic latency and does so by absorbing variations in the propagation delays of the serialized data as the data travels from the transmitter to the receiver. A proper release point is one that provides sufficient margin against delay variations. Choosing a proper release point requires knowing the average arrival time of data at the elastic buffer, referenced to an LMFC edge, and the total expected delay variation for all devices. With this information the region of invalid release points within the LMFC period can be defined, which stretches from the minimum to maximum delay for all lanes. Essentially, the designer must make sure that the data for all lanes arrives at all devices after the previous release point occurs and before the next release point occurs. The invalid region can also be found experimentally - see [Programming RBD](#).

[Figure 7-54](#) provides a simplified timing diagram that demonstrates this requirement. In this figure, the data for two transmitters (ADC or logic device) is shown. The second transmitter (TX 2) has a longer routing distance ( $t_{PCB}$ ) and results in a longer link delay than the first transmitter (TX 1). First, the invalid region of the LMFC period is marked off as determined by the data arrival times for all devices. Then, the release point is set by using the release buffer delay (RBD) parameter to shift the release point an appropriate number of quad-octet steps from the LMFC edge so that the release point occurs within the valid region of the LMFC cycle. In the case of [Figure 7-54](#), the LMFC edge (RBD = 0) is a good choice for the release point because there is sufficient margin on each side of the valid region.



**Figure 7-54. LMFC Valid Region Definition for Elastic Buffer Release Point Selection**

The TX and RX LMFC do not necessarily need to be phase aligned, but knowledge of their phase is important for proper elastic buffer release point selection. Also, the elastic buffer release point occurs within every LMFC cycle, but the buffers only release when all lanes have arrived. Therefore, the total link delay can exceed a single LMFC period; see [JESD204B multi-device synchronization: Breaking down the requirements](#) for more information.

#### 7.3.7.8.1 Programming RBD

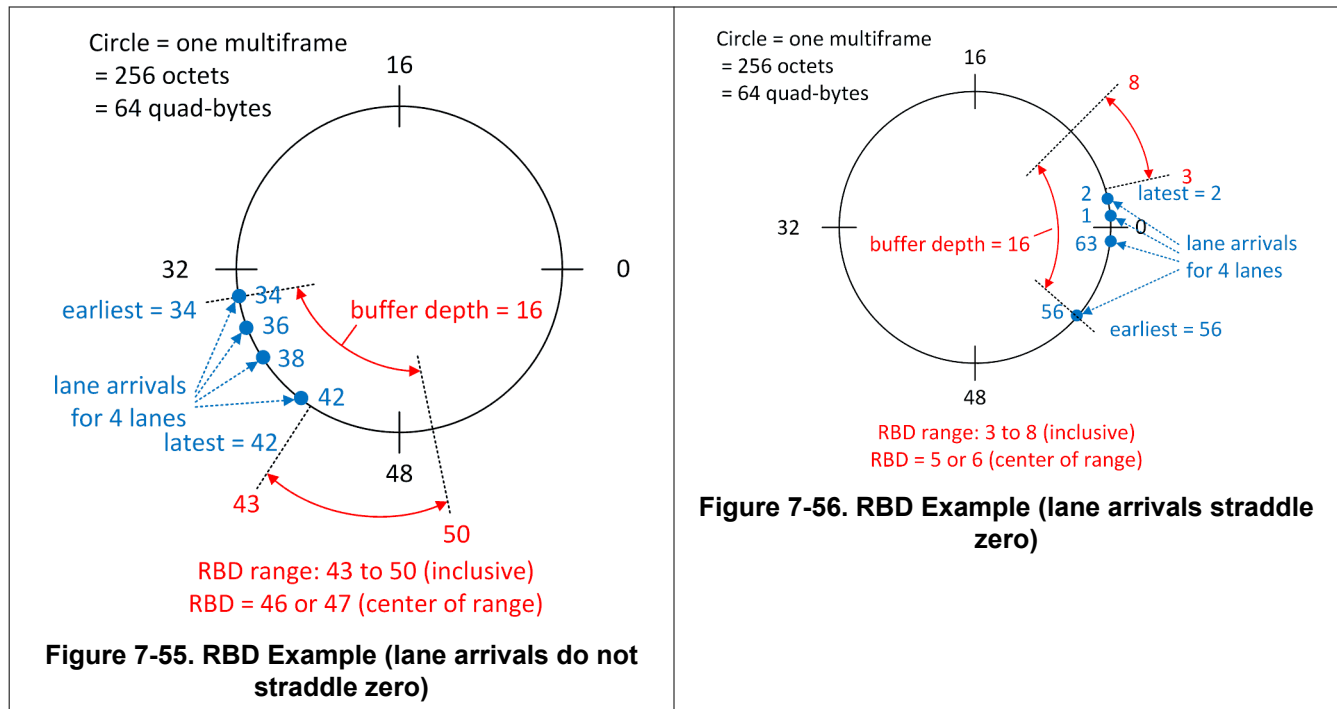
The range of values for RBD depends on the phase delta between the Rx and Tx LMFC/LEMC, as well as link latencies in the Tx, channel, and Rx. Therefore, do not provide a pre-determined RBD value that is appropriate for all systems. The LANE\_ARR registers are provided to help the user measure lane arrival times and select an appropriate RBD value for the system. For deterministic latency, the RBD value can be selected during system prototyping and stored in system firmware. Calculating RBD each time the system is turned on can result in non-deterministic latency.

The arrival times are reported in units of quad-bytes and are measured with respect to a modulo-64 reference counter that increments for each quad-byte received (per lane). The reference counter is aligned (reset) by SYSREF.

Since the lane arrival times are modulo-values, it is important to use arithmetic that accounts for the modulus (the *latest* arriving lane might actually have a *smaller* LANE\_ARR value than the earliest arriving lane). [Figure 7-55](#) and [Figure 7-56](#) depict the RBD calculation graphically to emphasize this. The lane arrival times are mapped onto a circle with a circumference of 64 quad-bytes which corresponds to the modulo-64 counter used to measure lane arrival times.

The earliest usable RBD value is equal to the latest LANE\_ARR value plus 1 (modulo 64). The latest usable RBD value is equal to the earliest LANE\_ARR value plus the buffer depth (modulo 64) (the buffer depth is 16 quad-octets, except when  $K \times F = 32$ , then the buffer depth is reduced to 8 quad-octets). Note that the latest, usable RBD value causes the earliest arriving lane to overwrite buffer data on the same clock cycle that the data is being read out (this is acceptable and does not cause overflow).

Choosing an RBD value in the middle of the usable range maximizes the skew tolerance; however, the user can choose a value closer to the latest arriving lane if lower latency is desired.



#### 7.3.7.9 Operation in Subclass 0 Systems

The device can operate with subclass 0 compatibility provided that multi-DAC synchronization and deterministic latency are not required. With these limitations, the device can operate without the application of SYSREF. The internal LMFC is automatically self-generated with unknown starting phase. RBD does not need to be programmed as the elastic buffer is released automatically just after the latest arriving lane begins to write to the elastic buffer. SYNC is used as normal to initiate the CGS and ILAS.

#### 7.3.7.10 Link Reset

The entire link layer for all lanes is reset any time:

- There is a gearbox FIFO underflow/overflow detected (LANE\_ERR[0]) on a lane used by the JESD link
- There is an elastic buffer overflow detected (EB\_ERR) on a lane used by the JESD link
- The JESD link goes down (JESD\_LINK\_DOWN\_ALM)
- SYSREF causes clock divider or LMFC/LEMC realignment (REALIGNED)
- The JTimer expires (JTIMER\_EXPIRED\_ALM)

#### 7.3.8 Alarm Generation

The alarm pin is useful for notifying the host controller of events that may require intervention. Any active alarms in the SYS\_ALM register asserts the alarm output if they are not masked in the ALM\_MASK register.

### 7.4 Device Functional Modes

This section describes the functional modes of the device. Some of the features in this section have been discussed in further detail in [Feature Description](#).

#### 7.4.1 DUC and DDS Modes

The device contains a DUC mode and a direct digital synthesis (DDS) mode. The data path mode uses complex (I and Q) data from the JESD interface, interpolates and upconverts it in the DUCs, sums the DUC outputs and generates the analog signal in the DAC. In DDS mode, the DUC NCOs are used directly to generate tones without requiring input data.

The list below summarized how DDS mode differs from DUC mode:

1. Interpolation filters are not enabled
2. JESD204C interface is not enabled
3. NCOs use less power (no complex mixing)
4. AMP register supplies unique amplitudes for each DUC (DDS) channel, allowing DDS channels to generate tones to cancel harmonic tones in the DAC output. For example, DDS channel 0 could produce a fundamental tone, channel 1 could produce a tone to cancel HD2, and channel 2 could produce a tone to cancel HD3.
5. The JMODE and DUC\_L registers are ignored and the SYSREF period constraints imposed by the JESD204C system and interpolation filters are removed. See [Table 7-3](#).

## 7.4.2 JESD204C Interface Modes

Each operational mode has a limited set of available interface formats (number of lanes, resolution).

### 7.4.2.1 JESD204C Interface Modes

The device JESD204C modes are configured with the parameters defined in [Table 7-19](#), [Table 7-20](#) and [Table 7-21](#).

**Table 7-19. JESD204C Interface Parameter Definitions**

| Parameter | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| JMODE     | JESD204C mode number. The user configures this parameter to choose a supported mode. Most other parameters are derived from this setting. See <a href="#">Table 7-22</a> .                                                                                                                                                                                                                                                                                                                                                                                 |
| LS        | Lanes per sample stream. This is derived from JMODE. See <a href="#">Table 7-22</a> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| LT        | Ratio of clock to input sample rate. $LT = F_{CLK} / F_{INPUT}$ . Not that DES2X mode does not affect the value of LT. Interpolation factor 1-256x is programmed in the DUC_L register.                                                                                                                                                                                                                                                                                                                                                                    |
| Lx        | Maximum number of lanes used for a given JMODE. The link scales down the number of active lanes (L) depending on how many channels are enabled. See JESD_M register.                                                                                                                                                                                                                                                                                                                                                                                       |
| Mx        | Maximum number of streams for a given JMODE. Mx is computed automatically according to <a href="#">Table 7-22</a> . The user can specify the actual number of streams (M) using the JESD_M register.                                                                                                                                                                                                                                                                                                                                                       |
| R         | Number of bits transmitted per lane per CLK cycle. Derived from JMODE and LT (see <a href="#">Table 7-22</a> ). Based on R, the user must program REFDIV, MPY, and RATE registers. Additionally, the maximum CLK frequency is a function of R.                                                                                                                                                                                                                                                                                                             |
| SI        | Sample Interleaving/Increment Factor. A value of 1 indicates that the standard transport layer mapping from the JESD204C standard is used (samples are mapped linearly from 0 to S-1). A value greater than 1 indicates that an alternate mapping is used as follows: Map samples starting with sample 0, incrementing the index by SI. Repeat this as many times as necessary to map all S samples, starting each repetition at an index that is one larger than the previous repetition. See JESD Format Diagrams <a href="#">JESD Format Diagrams</a> . |
| KR        | For 8b/10b operation, KR defines the legal values of K (frames per multiframe). The legal values are restricted to facilitate upset immunity of the elastic buffer. The multiframe length is restricted to a multiple of the elastic buffer depth of 64 characters (buffer depth is reduced to 32 characters if K=32 and F=1). For 8b/10b modes, K is programmed via the KM1 register.                                                                                                                                                                     |

**Table 7-20. JESD204C Link Parameters**

| Parameter | Description                                                                               | ILAS Field Name | Value for this device <sup>(1)</sup>   |
|-----------|-------------------------------------------------------------------------------------------|-----------------|----------------------------------------|
| ADJCNT    | DAC LMFC adjustment                                                                       | ADJCNT[3:0]     | n/a                                    |
| ADJDIR    | DAC LMFC adjustment direction                                                             | ADJDIR[0]       | n/a                                    |
| BID       | Bank ID                                                                                   | BID[3:0]        | n/a                                    |
| CF        | Number of control words per frame                                                         | CF[4:0]         | 0                                      |
| CS        | Number. of control bits per sample                                                        | CS[1:0]         | 0                                      |
| DID       | Device identification number                                                              | DID[7:0]        | n/a                                    |
| F         | Number of octets per frame (per lane)                                                     | F[7:0]          | See <a href="#">Table 7-22</a>         |
| HD        | High Density Format                                                                       | HD[0]           | See <a href="#">Table 7-22</a>         |
| JESDV     | JESD204 Version                                                                           | JESDV[2:0]      | n/a                                    |
| K         | Number of frames per multiframe                                                           | K[7:0]          | Set by <a href="#">KM1</a> register    |
| L         | Number of lanes per link                                                                  | L[4:0]          | ceiling(M/Mx*Lx)                       |
| LID       | Lane identification no.                                                                   | LID[4:0]        | n/a                                    |
| M         | Number of sample streams per link (see <sup>(1)</sup> )                                   | M[7:0]          | Set by <a href="#">JESD_M</a> register |
| N         | Bits per sample (before adding control or tail bits) for JESD204C interface.              | N[4:0]          | See <a href="#">Table 7-22</a>         |
| N'        | Total number of bits per sample (including control and tail bits) for JESD204C interface. | N'[4:0]         | See <a href="#">Table 7-22</a>         |
| PHADJ     | Phase adjustment request to DAC                                                           | PHADJ[0]        | n/a                                    |
| S         | Number of samples per stream per frame                                                    | S[4:0]          | See <a href="#">Table 7-22</a>         |
| SCR       | Scrambling enabled                                                                        | SCR[0]          | Set by <a href="#">SCR</a> register    |
| SUBCLASSV | Device Subclass Version                                                                   | SUBCLASSV[2:0]  | n/a                                    |
| RES1      | Reserved field 1                                                                          | RES1[7:0]       | n/a                                    |
| RES2      | Reserved field 2                                                                          | RES2[7:0]       | n/a                                    |
| CHKSUM    | Checksum (sum of all above fields, modulo 256)                                            | FCHK[7:0]       | n/a                                    |

(1) In 8b/10b modes, the transmitter may send link configuration octets during the ILAS. The values sent by the transmitter are not checked by this receiver, and they do not need to match the operational values of the receiver.

**Table 7-21. Link Parameters (applicable in 64b/66b encoding only)**

| Parameter | Description                                                             | Value for this device <sup>(1)</sup> |
|-----------|-------------------------------------------------------------------------|--------------------------------------|
| E         | Number of multi-blocks per extended multi-block (64b/66b encoding only) | 1                                    |

Each supported mode is assigned a mode number which can be programmed into the JMODE register with the parameters listed in [Table 7-22](#).

- At minimum interpolation rate

**Table 7-22. JESD Interface Modes**

| JMODE | Encoding | Max Input Sample Rate per Stream (MSPS)#n<br>one# | MAX Serdes Baud Rate (Gbps) | R = F <sub>BIT</sub> / F <sub>CLK</sub> | N  | Mx = Max # Streams | Ls = Lanes/ Stream | Lx = Max # Lanes | LT = Interpolation |     | JESD Format |   |    |    | KR          |
|-------|----------|---------------------------------------------------|-----------------------------|-----------------------------------------|----|--------------------|--------------------|------------------|--------------------|-----|-------------|---|----|----|-------------|
|       |          |                                                   |                             |                                         |    |                    |                    |                  | MIN                | MAX | F           | S | HD | SI |             |
| 4     | 8b/10b   | 640                                               | 12.8                        | 20/LT                                   | 16 | 2                  | 1                  | 2                | 4                  | 64  | 2           | 1 | 0  | 1  | 32, 64, 128 |
|       | 64b/66b  | 775.8                                             | 12.8                        | 16.5/LT                                 |    |                    |                    |                  |                    |     |             |   |    |    |             |
| 5     | 8b/10b   | 320                                               | 12.8                        | 40/LT                                   | 16 | 4                  | ½                  | 2                | 8                  | 128 | 4           | 1 | 0  | 1  | 16,32,64    |
|       | 64b/66b  | 387.9                                             | 12.8                        | 33/LT                                   |    |                    |                    |                  |                    |     |             |   |    |    |             |
| 6     | 8b/10b   | 160                                               | 12.8                        | 80/LT                                   | 16 | 8                  | ¼                  | 2                | 16                 | 256 | 8           | 1 | 0  | 1  | 8,16,32     |
|       | 64b/66b  | 193.9                                             | 12.8                        | 66/LT                                   |    |                    |                    |                  |                    |     |             |   |    |    |             |
| 7     | 8b/10b   | 80                                                | 12.8                        | 160/LT                                  | 16 | 8                  | ⅙                  | 1                | 32                 | 256 | 16          | 1 | 0  | 1  | 4,8,16      |
|       | 64b/66b  | 97.0                                              | 12.8                        | 132/LT                                  |    |                    |                    |                  |                    |     |             |   |    |    |             |

#### 7.4.2.2 JESD204C Format Diagrams

The following sub-sections depict each output format, showing how samples and tail bits are mapped to the lanes. Any lanes that are not shown in the output format tables are unused. Each table depicts exactly one frame. Tail bits are discarded and ignored by the transport layer. All diagrams are with respect to the logical lane numbers which can be arbitrarily mapped to the external physical lanes using LANE\_SEL<sub>n</sub>.

**Table 7-23. Format Notation Description**

| Notation | Description                                                                                                                 |
|----------|-----------------------------------------------------------------------------------------------------------------------------|
| T        | Tail bits (used for some 12-bit modes)                                                                                      |
| CH0_I[n] | In-Phase samples for channel 0. Can also be considered as “channel A” when the input isn’t considered to be complex data.   |
| CH0_Q[n] | Quadrature samples for channel 0. Can also be considered as “channel B” when the input isn’t considered to be complex data. |
| CH1_I[n] | In-Phase samples for channel 1.                                                                                             |
| CH1_Q[n] | Quadrature samples for channel 1.                                                                                           |
| CH2_I[n] | In-Phase samples for channel 2.                                                                                             |
| CH2_Q[n] | Quadrature samples for channel 2.                                                                                           |
| CH3_I[n] | In-Phase samples for channel 3.                                                                                             |
| CH3_Q[n] | Quadrature samples for channel 3.                                                                                           |

In all of the above notations, n indicates the sample number. Some JESD204C modes have S=1 (one sample per stream per frame). In those cases, “[n]” is omitted in the descriptions.

##### 7.4.2.2.1 16-bit Formats

**Table 7-24. JMODE 4 (16-bit, 1 lane per stream, 8 streams maximum)**

| Octet  | 0     |   | 1 |   |
|--------|-------|---|---|---|
| Nibble | 0     | 1 | 2 | 3 |
| Lane 0 | CH0_I |   |   |   |
| Lane 1 | CH0_Q |   |   |   |

**Table 7-25. JMODE 5 (16-bit, 1/2 lane per stream, 8 streams maximum)**

| Octet  | 0     |   | 1 |   | 2     |   | 3 |   |
|--------|-------|---|---|---|-------|---|---|---|
| Nibble | 0     | 1 | 2 | 3 | 4     | 5 | 6 | 7 |
| Lane 0 | CH0_I |   |   |   | CH0_Q |   |   |   |
| Lane 1 | CH1_I |   |   |   | CH1_Q |   |   |   |

**Table 7-26. JMODE 6 (16-bit, 1/4 lane per stream, 8 streams maximum)**

| Octet  | 0     |   | 1 |   | 2     |   | 3 |   | 4     |   | 5  |    | 6     |    | 7  |    |
|--------|-------|---|---|---|-------|---|---|---|-------|---|----|----|-------|----|----|----|
| Nibble | 0     | 1 | 2 | 3 | 4     | 5 | 6 | 7 | 8     | 9 | 10 | 11 | 12    | 13 | 14 | 15 |
| Lane 0 | CH0_I |   |   |   | CH0_Q |   |   |   | CH1_I |   |    |    | CH1_Q |    |    |    |
| Lane 1 | CH2_I |   |   |   | CH2_Q |   |   |   | CH3_I |   |    |    | CH3_Q |    |    |    |

**Table 7-27. JMODE 7 (16-bit, 1/8 lane per stream, 8 streams maximum)**

| Octet  | 0     | 1 | 2 | 3 | 4     | 5 | 6 | 7 | 8     | 9 | 10 | 11 | 12    | 13 | 14 | 15 |
|--------|-------|---|---|---|-------|---|---|---|-------|---|----|----|-------|----|----|----|
| Nibble | 0     | 1 | 2 | 3 | 4     | 5 | 6 | 7 | 8     | 9 | 10 | 11 | 12    | 13 | 14 | 15 |
| Lane 0 | CH0_I |   |   |   | CH0_Q |   |   |   | CH1_I |   |    |    | CH1_Q |    |    |    |
| Lane 1 | CH2_I |   |   |   | CH2_Q |   |   |   | CH3_I |   |    |    | CH3_Q |    |    |    |

### 7.4.3 NCO Synchronization Latency

There are two deterministic methods for synchronizing the NCO (frequency or phase change, accumulator reset): through an LSB of the JESD204C interface or via SYSREF. The latency parameters for each synchronization method are listed in [Table 7-28](#).

Using SYSREF as the Synchronization source, the latency parameter  $T_{\text{SYSREF\_NCO}}$  is the time between the moment SYSREF is sampled high by CLK and the arrival of the NCO change at the DAC output. The alignment to the data path samples can be calculated by the Excel spreadsheet latency calculator discussed in [Section 7.4.4](#).

When using the JESD204C interface LSB, the latency parameter  $T_{\text{JSYNC\_NCO}}$  is the difference in time of the NCO synchronization event relative to the corresponding data sample aligned with the LSB.  $T_{\text{JSYNC\_NCO}}$  is deterministic, but for some modes depends on the alignment of the LSB rising edge to the multiframe boundary (see [Table 7-29](#)).

**Table 7-28. NCO Synchronization Latency Parameters**

| Latency Parameter        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Value                          |
|--------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------|
| $T_{\text{SYSREF\_NCO}}$ | Latency from SYSREF sampled high (by CLK) to DAC output reacting to an NCO synchronization event (that was triggered by SYSREF).                                                                                                                                                                                                                                                                                                                                                                      | 477.5 CLK cycles               |
| $T_{\text{JSYNC\_NCO}}$  | The latency through the interpolation filter(s) to the NCO minus the latency of the LSB that synchronizes the NCO. Applies only when using the LSB of the input data to synchronize the NCO. To make input sample $n$ be the first sample to be mixed with a new NCO frequency or phase, the LSB should be brought high on sample $n' = n + T_{\text{JSYNC\_NCO}}/\text{LT}$ . Note that $n'$ may not be an integer as the synchronization path is not always a whole number of input sample periods. | See <a href="#">Table 7-29</a> |

**Table 7-29.  $T_{\text{JSYNC\_NCO}}$  vs. LT**

| Interpolation Factor (LT) | $T_{\text{JSYNC\_NCO}}$ [CLK cycles] <sup>(1)</sup>                            |
|---------------------------|--------------------------------------------------------------------------------|
| 2                         | -144, -142, -140, -138, -136, -134, -132, -130                                 |
| 3                         | -89, -86, -83, -81, -80, -78, -77, -75, -74, -72, -71, -69, -68, -66, -63, -60 |
| 4                         | -36, -32, -28, -24                                                             |
| 6                         | 34, 40, 42, 46, 48, 52, 54, 60                                                 |
| 8                         | 86, 94                                                                         |
| 12                        | 186, 194, 198, 206                                                             |
| 16                        | 290                                                                            |
| 24                        | 458, 466                                                                       |
| 32                        | 648                                                                            |
| 48                        | 968                                                                            |
| 64                        | 1396                                                                           |
| 96                        | 2036                                                                           |
| 128                       | 2932                                                                           |
| 192                       | 4212                                                                           |

**Table 7-29. T<sub>JSYNC\_NCO</sub> vs. LT (continued)**

| Interpolation Factor (LT) | T <sub>JSYNC_NCO</sub> [CLK cycles] <sup>(1)</sup> |
|---------------------------|----------------------------------------------------|
| 256                       | 6004                                               |

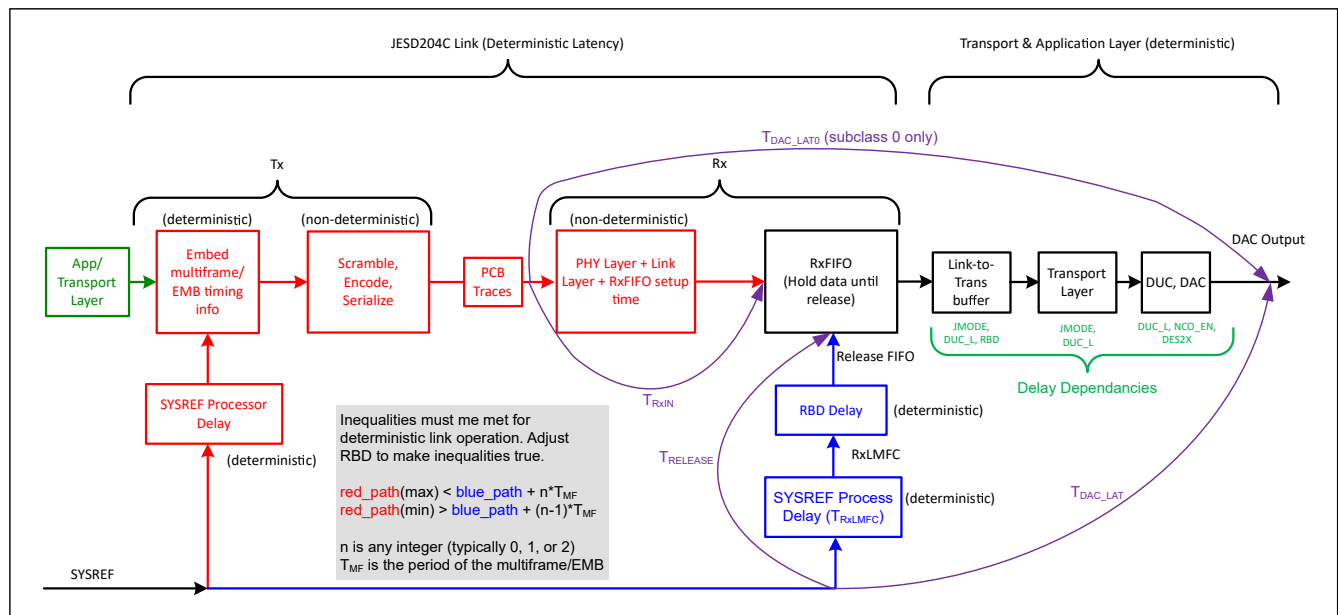
(1) When multiple values are listed, it indicates that T<sub>JSYNC\_NCO</sub> depends on when the LSB rises with respect to the multiframe boundary.

#### 7.4.4 Data Path Latency

There are several difference latencies defined for the device as shown in Figure 7-57 and listed in Table 7-30. The latency within the device is dependent on the mode of operation, including JMODE, Interpolation factor, RBD setting, NCO usage and DES setting. An Excel spreadsheet calculator is provided by TI to calculate the device latency in different modes of operation.

In JESD204C subclass 0 operation, the latency from Serdes input to DAC output is called T<sub>DAC\_LAT0</sub> and is not deterministic and a minimum and maximum range is provided in the Excel spreadsheet calculator.

In JESD204C subclass 1 operation, the latency T<sub>DAC\_LAT</sub> from the SYSREF input to DAC output is deterministic and is provided in the Excel spreadsheet calculator. The JESD204C link latency is deterministic as long as SYSREF is sampled reliably and the RBD value is set properly.



**Figure 7-57. Definition of Device Latencies**

**Table 7-30. Latency Definitions**

| Latency Parameter     | Definition                                                                                                                                                                                                    |
|-----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| T <sub>RELEASE</sub>  | Latency from the rising edge of CLK that follows the rising edge of SYSREF to release event for elastic buffer. (subclass 1 only).                                                                            |
| T <sub>DAC_LAT</sub>  | Latency from the rising edge of CLK that follows the rising edge of SYSREF to the time of the first sample at the DAC output of the multiframe/extended multiblock launched by SYSREF (subclass 1 only).      |
| T <sub>RxIN</sub>     | Latency from the receiver data inputs to the elastic buffer input, including the minimum setup time of the elastic buffer. This is non-deterministic, so a minimum and maximum limit are provided.            |
| T <sub>DAC_LAT0</sub> | Latency from receiver data inputs (multiframe/EMB boundary) to first sample of a multiframe launched on DAC output. This is non-deterministic, so a minimum and maximum limit are provided (subclass 0 only). |

## 7.5 Programming

The device contains two programming interfaces: a SPI interface and a Fast Reconfiguration (FR) interface for fast programming of NCO frequency and phase.

### 7.5.1 Using the Standard SPI Interface

The standard SPI interface is accessed using the following four pins: serial clock (SCLK), serial data in (SDI), serial data out (SDO), and serial interface chip-select ( $\overline{\text{SCS}}$ ). Register access is enabled through the  $\overline{\text{SCS}}$  pin.

#### 7.5.1.1 $\overline{\text{SCS}}$

This signal must be asserted low to access a register through the serial interface. Setup and hold times with respect to the SCLK must be observed.

#### 7.5.1.2 SCLK

Serial data input is accepted at the rising edge of this signal. SCLK has no minimum frequency requirement.

#### 7.5.1.3 SDI

Each register access requires a specific 24-bit pattern at this input. This pattern consists of a read-and-write (R/W) bit, register address, and register value. The data are shifted in MSB first and multi-byte registers are always in little-endian format (least significant byte stored at the lowest address). Setup and hold times with respect to the SCLK must be observed (see the Switching Characteristics table).

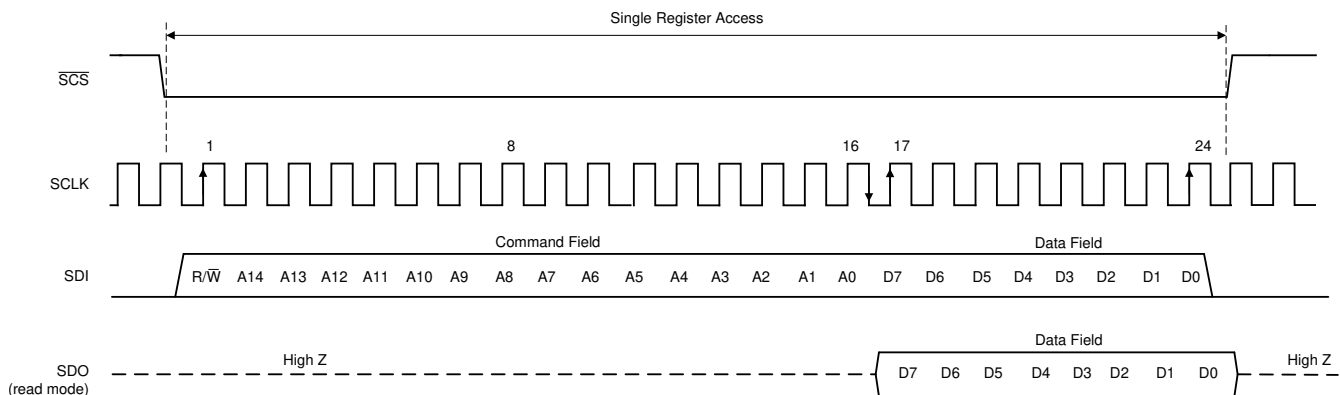
#### 7.5.1.4 SDO

The SDO signal provides the output data requested by a read command. This output is high impedance during write bus cycles and during the read bit and register address portion of read bus cycles.

#### 7.5.1.5 Serial Interface Protocol

As shown in Figure 7-58, each register access consists of 24 bits. The first bit is high for a read and low for a write.

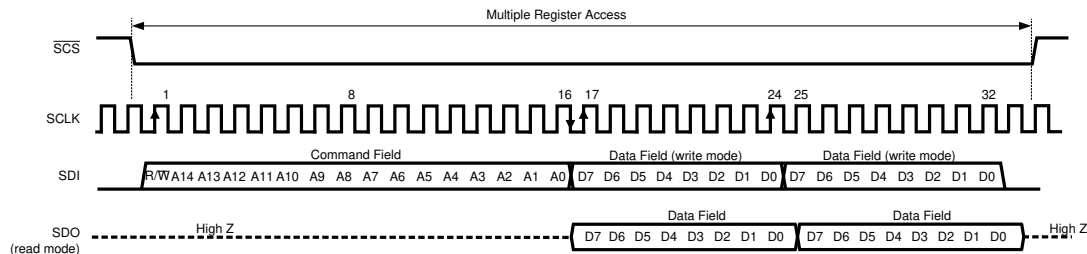
The next 15 bits are the address of the register that is to be written to. During write operations, the last eight bits are the data written to the addressed register. During read operations, the last eight bits on SDI are ignored and, during this time, the SDO outputs the data from the addressed register. Figure 7-58 shows the serial protocol details.



**Figure 7-58. Serial Interface Protocol: Single Read and Write**

### 7.5.1.6 Streaming Mode

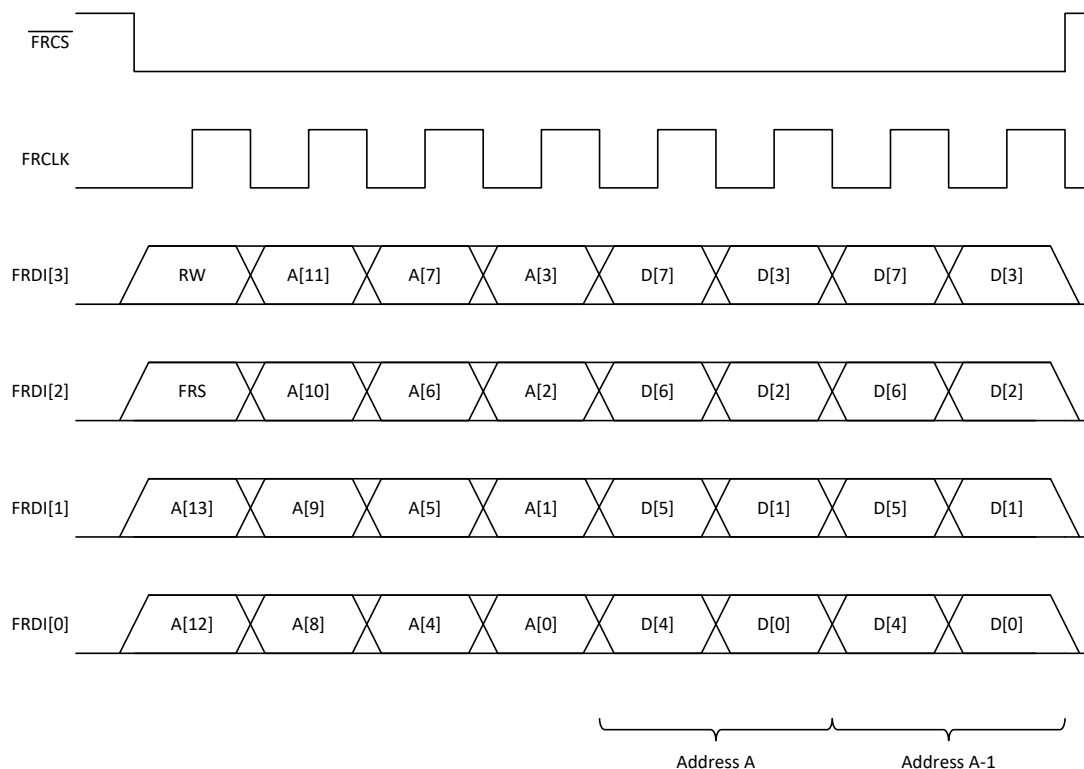
The serial interface supports streaming reads and writes. In this mode, the initial 24 bits of the transaction specifies the access type, register address, and data value as normal. Additional clock cycles of write or read data are immediately transferred, as long as the  $\overline{\text{SCS}}$  input is maintained in the asserted (logic low) state. The register address auto increments (default) or decrements for each subsequent 8-bit transfer of the streaming transaction. The **ASCEND** bit (register 000h, bit 5) controls whether the address value ascends (increments) or descends (decrements). [Figure 7-59](#) shows the streaming mode transaction details.



**Figure 7-59. Serial Interface Protocol: Streaming Read and Write**

### 7.5.2 Using the Fast Reconfiguration Interface

The FR interface provides fast write-only access to configure NCO frequencies and synchronization. The FR interface is similar to the SPI interface, but 4 bits are sent per clock cycle. The FR timing diagram is shown in [Figure 7-60](#). It uses a R/W bit (always Write for this device), a transaction sync bit (FRS), and 14-bits of address followed by some number of data bytes. The address is decremented after each data byte (consistent with little-endian). The interface is byte addressable and data is committed after each byte. The FR interface takes 4-bits (one nibble) per clock. For multi-nibble fields, data is sent most-significant nibble first. When the transaction sync bit (FRS) is set, the synchronization event specified in the **NCO\_SYNC\_SRC** register field occurs at the rising edge of  $\overline{\text{FRCS}}$ . Transactions ended before the completion of the first data byte may not trigger the sync event.



**Figure 7-60. FR Interface Timing Diagram**

The FR interface registers are listed in [Table 7-31](#). There are two registers that can change the NCO frequency - FR\_FREQ[3:0] is 64-bits for each NCO and changes the entire frequency word. FR\_FREQS[3:0] is 32-bits for each NCO and changes only the upper 32-bits of the frequency word, providing for faster frequency changes.

**Table 7-31. FR Interface Registers**

| Address       | Name          | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|---------------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x00FF        | FR_NCO_AR     | FR NCO Accumulator Reset (default: 0x0f)<br>[7:4] RESERVED<br>[3:0] FR_NCO_AR For each bit FR_NCO_AR[n], if set, the accumulator for NCO <sub>n</sub> is reset on every sync event specified by NCO_SYNC_SRC.<br>Note: This register has no effect when FR_EN=0.                                                                                                                                                                                                                                                                                                                                     |
| 0x0100-0x011F | FR_FREQ[3:0]  | FR 64-bit Frequency for NCO Accumulator (default for FR_FREQ[n]=0x00)<br>The frequency setting for FR_FREQ[0] is at the lowest address.<br>[63:0] FR_FREQ[n] This register is used instead of FREQ[n] when FR_EN=1.<br>Changes to the upper 32-bits of this register also change FR_FREQS[n].<br>Note: Changes to this register do not take effect until the next sync event specified by NCO_SYNC_SRC.<br>Note: This register has no effect when FR_EN=0.                                                                                                                                           |
| 0x0120-0x0127 | FR_PHASE[3:0] | FR Phase for NCO Accumulator (default for FR_PHASE[n]=0x0000)<br>The phase setting for FR_PHASE[0] is at the lowest address.<br>[15:0] FR_PHASE[n] This register is used instead of PHASE[n] when FR_EN=1.<br>Note: Changes to this register do not take effect until the next sync event specified by NCO_SYNC_SRC.<br>Note: This register has no effect when FR_EN=0.                                                                                                                                                                                                                              |
| 0x0128-0x0137 | FR_FREQS[3:0] | FR 32-bit Frequency for NCO Accumulator (default for FR_FREQS[n]=0x00)<br>The frequency setting for FR_FREQS[0] is at the lowest address.<br>[31:0] FR_FREQS[n] This register is used instead of FREQ[n] when FR_EN=1.<br>Changes to this register also change the upper 32-bits of FR_FREQ[n]. This register only controls the upper 32-bits of the frequency. The lower 32-bits of the frequency are always controlled by FR_FREQ[n].<br>Note: Changes to this register do not take effect until the next sync event specified by NCO_SYNC_SRC.<br>Note: This register has no effect when FR_EN=0. |

### 7.5.3 SPI Register Map

Table 7-32 lists the SPI registers. All register offset addresses not listed in Table 7-32 should be considered as reserved locations and the register contents should not be modified. Reserved register fields in addresses with non-reserved R/W fields always return the default/reset value during read, not the written value.

**Table 7-32. SPI Registers**

| Offset        | Acronym           | Register Name                             | Section            |
|---------------|-------------------|-------------------------------------------|--------------------|
| 0x0000        | CONFIG_A          | Configuration A                           | <a href="#">Go</a> |
| 0x0002        | DEVICE_CONFIG     | Device Configuration                      | <a href="#">Go</a> |
| 0x0003        | CHIP_TYPE         | Chip Type                                 | <a href="#">Go</a> |
| 0x0004        | CHIP_ID           | Chip Identification                       | <a href="#">Go</a> |
| 0x0006        | CHIP_VERSION      | Chip Version                              | <a href="#">Go</a> |
| 0x000C        | VENDOR_ID         | Vendor Identification                     | <a href="#">Go</a> |
| 0x0010-0x007F | RESERVED          |                                           |                    |
| 0x0080        | SYSREF_CTRL       | SYSREF Control                            | <a href="#">Go</a> |
| 0x0081-0x008F | RESERVED          |                                           |                    |
| 0x0090-0x0092 | SYSREF_POS        | SYSREF Capture Position                   | <a href="#">Go</a> |
| 0x0093-0x009F | RESERVED          |                                           |                    |
| 0x00A0        | SYSREF_ALIGN      | SYSREF Alignment Control                  | <a href="#">Go</a> |
| 0x00A1        | SYSREF_TERM       | SYSREF Termination Configuration          | <a href="#">Go</a> |
| 0x00A2-0x00FF | RESERVED          |                                           |                    |
| 0x0100        | JESD_EN           | JESD204C Subsystem Enable                 | <a href="#">Go</a> |
| 0x0101        | JMODE             | JESD204C Mode                             | <a href="#">Go</a> |
| 0x0102        | JESD_M            | JESD204C Number of Streams                | <a href="#">Go</a> |
| 0x0103        | JCTRL             | JESD204C Control                          | <a href="#">Go</a> |
| 0x0104        | SHMODE            | JESD204C Sync Word Mode                   | <a href="#">Go</a> |
| 0x0105        | KM1               | JESD204C K Parameter                      | <a href="#">Go</a> |
| 0x0106        | RBD               | JESD204C Release Buffer Delay             | <a href="#">Go</a> |
| 0x0107        | JESD_STATUS       | JESD204C System Status Register           | <a href="#">Go</a> |
| 0x0108        | REFDIV            | JESD204C Reference Divider                | <a href="#">Go</a> |
| 0x0109        | MPY               | JESD204C PLL Multiplier                   | <a href="#">Go</a> |
| 0x010A        | RATE              | JESD204C Receive Rate                     | <a href="#">Go</a> |
| 0x010B        | LB_VRANGE         | JESD204C VCO Range                        | <a href="#">Go</a> |
| 0x010C-0x011F | RESERVED          |                                           |                    |
| 0x0120        | JSYNC_N           | JESD204C Manual Sync Request              | <a href="#">Go</a> |
| 0x0121        | JTEST             | JESD204C Test Control                     | <a href="#">Go</a> |
| 0x0122-0x0123 | RESERVED          | RESERVED                                  |                    |
| 0x0124        | JTIMER            | JESD204C Watchdog Timer                   | <a href="#">Go</a> |
| 0x0125-0x0126 | RESERVED          |                                           |                    |
| 0x0127        | SYNC_EPW          | JESD204C SYNC Error Report Pulse Width    | <a href="#">Go</a> |
| 0x0128        | CRC_TH            | JESD204C CRC Error Thresholds             | <a href="#">Go</a> |
| 0x0129-0x012B | RESERVED          |                                           |                    |
| 0x012C        | LANE_ARSTAT       | Lane Arrival Status                       | <a href="#">Go</a> |
| 0x012D        | RESERVED          |                                           |                    |
| 0x012E-0x012F | LANE_INV          | PHY Lane Inversion                        | <a href="#">Go</a> |
| 0x0130-0x013F | LANE_SEL[15:0]    | PHY Lane Select for Logical Lane <i>n</i> | <a href="#">Go</a> |
| 0x0140-0x014F | LANE_ARR[15:0]    | Lane <i>n</i> Arrival Time                | <a href="#">Go</a> |
| 0x0150-0x015F | LANE_STATUS[15:0] | Lane <i>n</i> Status                      | <a href="#">Go</a> |

**Table 7-32. SPI Registers (continued)**

| Offset        | Acronym           | Register Name                                    | Section            |
|---------------|-------------------|--------------------------------------------------|--------------------|
| 0x0160-0x016F | LANE_ERR[15:0]    | Lane <i>n</i> Error Flags                        | <a href="#">Go</a> |
| 0x0170-0x017F | FIFO_STATUS[15:0] | Gearbox FIFO Status for Logical Lane <i>n</i>    | <a href="#">Go</a> |
| 0x0180-0x0189 | RESERVED          |                                                  |                    |
| 0x018A-0x019F | RESERVED          |                                                  |                    |
| 0x01A0        | BER_EN            | BER Measurement Control                          | <a href="#">Go</a> |
| 0x01A1-0x01AF | RESERVED          |                                                  |                    |
| 0x01B0-0x01BF | BER_CNT[15:0]     | BER Error Count for Lane <i>n</i>                | <a href="#">Go</a> |
| 0x01C0        | RESERVED          |                                                  |                    |
| 0x01C1        | JPHY_CTRL         | SerDes PHY Control                               | <a href="#">Go</a> |
| 0x01C2        | EQ_CTRL           | SerDes Equalizer Control                         | <a href="#">Go</a> |
| 0x01C3        | EQZERO            | SerDes Equalizer Zero                            | <a href="#">Go</a> |
| 0x01D0-0x01DF | LANE_EQ[15:0]     | SerDes Equalizer Level for Lane <i>n</i>         | <a href="#">Go</a> |
| 0x01E0-0x01EF | LANE_EQS[15:0]    | SerDes Equalizer Status for Lane <i>n</i>        | <a href="#">Go</a> |
| 0x1F0         | ESRUN             | SerDes Eye-Scan Run Control                      | <a href="#">Go</a> |
| 0x01F1        | ES_CTRL           | SerDes Eye-Scan Control                          | <a href="#">Go</a> |
| 0x01F2        | ESPO              | SerDes Eye-Scan Phase Offset                     | <a href="#">Go</a> |
| 0x01F3        | ESVO              | SerDes Eye-Scan Voltage Offset                   | <a href="#">Go</a> |
| 0x01F4        | ES_BIT_SELECT     | SerDes Eye-Scan Bit Select                       | <a href="#">Go</a> |
| 0x01F5        | ESCOUNT_CLR       | SerDes Error Counter Clear                       | <a href="#">Go</a> |
| 0x01F6-0x01F7 | ESDONE            | SerDes Eye-Scan Process Done                     | <a href="#">Go</a> |
| 0x01F8-0x01FF | RESERVED          |                                                  |                    |
| 0x0200-0x020F | ESVO_S[15:0]      | SerDes Eye-Scan Voltage Offset for Lane <i>n</i> | <a href="#">Go</a> |
| 0x0210-0x022F | ECOUNT[15:0]      | SerDes Error/Mismatch Count for Lane <i>n</i>    | <a href="#">Go</a> |
| 0x0230-0x0233 | RESERVED          |                                                  |                    |
| 0x0234        | LOS_TH            | SerDes Loss-of_Signal Threshold                  | <a href="#">Go</a> |
| 0x0235        | EQCNTSZ           | SerDes Equalizer Counter Size                    | <a href="#">Go</a> |
| 0x0236-0x0237 | RESERVED          |                                                  |                    |
| 0x0238        | CDRLOCK           | SerDes CDR Lock/Freeze                           | <a href="#">Go</a> |
| 0x0239        | CDRPHASE          | SerDes CDR Phase Status                          | <a href="#">Go</a> |
| 0x023A-0x024F | RESERVED          |                                                  |                    |
| 0x0250        | PLL_STATUS        | SerDes PLL Status                                | <a href="#">Go</a> |
| 0x0251-0x0252 | RESERVED          |                                                  |                    |
| 0x0253        | JESD_RST          | JESD Reset                                       | <a href="#">Go</a> |
| 0x0254-0x02AF | RESERVED          |                                                  |                    |
| 0x02B0        | EXTREF_EN         | Enable External Reference                        | <a href="#">Go</a> |
| 0x02B1        | CUR_2X_EN         | DAC Current Doubler Enable                       | <a href="#">Go</a> |
| 0x02B2-0x02C1 | RESERVED          |                                                  |                    |
| 0x02C2-0x02CE | RESERVED          |                                                  |                    |
| 0x02CF        | DAC_OFS_CHG_BLK   | DAC Offset Adjustment Change Block               | <a href="#">Go</a> |
| 0x02D0-0x02DF | RESERVED          |                                                  |                    |
| 0x02E0        | DP_EN             | Datapath Enable                                  | <a href="#">Go</a> |
| 0x02E1        | DUC_L             | DUC Interpolation Factor                         | <a href="#">Go</a> |
| 0x02E2        | DUC_GAIN          | DUC Gain                                         | <a href="#">Go</a> |
| 0x02E3        | DUC_FORMAT        | DUC Output Format                                | <a href="#">Go</a> |
| 0x02E4        | DAC_SRC           | DAC Source                                       | <a href="#">Go</a> |

**Table 7-32. SPI Registers (continued)**

| Offset        | Acronym      | Register Name                                            | Section            |
|---------------|--------------|----------------------------------------------------------|--------------------|
| 0x02E5-0x02E7 | RESERVED     |                                                          |                    |
| 0x02E8        | MXMODE       | DAC Output Mode                                          | <a href="#">Go</a> |
| 0x02E9        | RESERVED     |                                                          |                    |
| 0x02EA        | TRUNC_HLSB   | Truncation Half LSB Offset                               | <a href="#">Go</a> |
| 0x02EB-0x02F7 | RESERVED     |                                                          |                    |
| 0x02F8        | TX_EN_SEL    | Transmitter Enable Control Selection                     | <a href="#">Go</a> |
| 0x02F9        | TX_EN        | Transmitter Enable Configuration                         | <a href="#">Go</a> |
| 0x02FA-0x02FF | RESERVED     |                                                          |                    |
| 0x0300        | NCO_CTRL     | NCO Control                                              | <a href="#">Go</a> |
| 0x0301        | NCO_CONT     | NCO Phase Continuous Mode                                | <a href="#">Go</a> |
| 0x0302        | NCO_SYNC     | NCO Synchronization Configuration                        | <a href="#">Go</a> |
| 0x0303        | NCO_AR       | NCO Accumulator Reset                                    | <a href="#">Go</a> |
| 0x0304        | SPI_SYNC     | SPI Sync                                                 | <a href="#">Go</a> |
| 0x0305        | NCO_SS       | NCO Continuous Self-Sync Mode                            | <a href="#">Go</a> |
| 0x0306-0x0317 | RESERVED     |                                                          |                    |
| 0x0318-0x031F | AMP[3:0]     | DDS Amplitude                                            | <a href="#">Go</a> |
| 0x0320-0x0327 | FREQ[0]      | Frequency for NCO0 Accumulator                           | <a href="#">Go</a> |
| 0x0328-0x032F | FREQ[1]      | Frequency for NCO1 Accumulator                           | <a href="#">Go</a> |
| 0x0330-0x0337 | FREQ[2]      | Frequency for NCO2 Accumulator                           | <a href="#">Go</a> |
| 0x0338-0x033F | FREQ[3]      | Frequency for NCO3 Accumulator                           | <a href="#">Go</a> |
| 0x0340-0x0347 | PHASE[3:0]   | Phase for NCO <sub>n</sub> Accumulator                   | <a href="#">Go</a> |
| 0x0348-0x0377 | RESERVED     |                                                          |                    |
| 0x0378-0x037F | AMP_R[3:0]   | Readback for Amplitude Word for NCO <sub>n</sub>         | <a href="#">Go</a> |
| 0x0380-0x039F | FREQ_R[3:0]  | Readback for Frequency for NCO <sub>n</sub> Accumulator  | <a href="#">Go</a> |
| 0x03A0-0x03A7 | PHASE_R[3:0] | Readback for Phase Word for NCO <sub>n</sub> Accumulator | <a href="#">Go</a> |
| 0x03A8-0x03DF | RESERVED     |                                                          |                    |
| 0x03E0        | FR_FRS_R     | Readback for FR Synchronization                          | <a href="#">Go</a> |
| 0x03E1        | FR_NCO_AR_R  | Readback for FR NCO Accumulator Reset                    | <a href="#">Go</a> |
| 0x03E2-0x03FF | RESERVED     |                                                          |                    |
| 0x0400        | TS_TEMP      | Temperature Reading in Celsius                           | <a href="#">Go</a> |
| 0x0401        | TS_SLEEP     | Temperature Sensor Sleep                                 | <a href="#">Go</a> |
| 0x0402-0x040F | RESERVED     |                                                          |                    |
| 0x0410        | SYNC_STATUS  | Synchronization Status                                   | <a href="#">Go</a> |
| 0x0411-0x042F | RESERVED     |                                                          |                    |
| 0x0430        | SYS_ALM      | System Alarm Status                                      | <a href="#">Go</a> |
| 0x0431        | ALM_MASK     | Alarm Mask                                               | <a href="#">Go</a> |
| 0x0432        | MUTE_MASK    | DAC Mute Mask                                            | <a href="#">Go</a> |
| 0x0433        | MUTE_REC     | DAC Mute Recovery                                        | <a href="#">Go</a> |
| 0x0434-0x05FF | RESERVED     |                                                          |                    |
| 0x0600        | FUSE_STATUS  | Fuse Status                                              | <a href="#">Go</a> |
| 0x0601-0x0722 | RESERVED     |                                                          |                    |
| 0x0723        | FINE_CUR_A   | Fine Bias Current Control for DACA                       | <a href="#">Go</a> |
| 0x0724        | COARSE_CUR_A | Coarse Bias Current Control for DACA                     | <a href="#">Go</a> |
| 0x0725        | FINE_CUR_B   | Fine Bias Current Control for DACB                       | <a href="#">Go</a> |
| 0x0726        | COARSE_CUR_B | Coarse Bias Current Control for DACB                     | <a href="#">Go</a> |

**Table 7-32. SPI Registers (continued)**

| Offset        | Acronym  | Register Name          | Section            |
|---------------|----------|------------------------|--------------------|
| 0x0727        | DEM_ADJ  | DEM Adjust             | <a href="#">Go</a> |
| 0x0728        | RESERVED |                        |                    |
| 0x0729        | DEM_DITH | DEM and DITHER Control | <a href="#">Go</a> |
| 0x72A-0x072D  | DAC_OFS  | DAC_Offset_Adjustment  | <a href="#">Go</a> |
| 0x72E - 0x7FF | RESERVED |                        |                    |

### 7.5.3.1 CONFIG\_A Register (Offset = 0h) [reset = 30h]

CONFIG\_A is shown in [Figure 7-61](#) and described in [Table 7-33](#).

Return to the [Register Summary Table](#).

Configuration A (default: 0x30)

**Figure 7-61. CONFIG\_A Register**

| 7          | 6        | 5      | 4        | 3        | 2 | 1 | 0 |
|------------|----------|--------|----------|----------|---|---|---|
| SOFT_RESET | RESERVED | ASCEND | RESERVED | RESERVED |   |   |   |
| R/W-0h     | R/W-0h   | R/W-1h | R/W-1h   | R/W-0h   |   |   |   |

**Table 7-33. CONFIG\_A Register Field Descriptions**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                    |
|-----|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | SOFT_RESET | R/W  | 0h    | Writing a 1 to this bit causes a full reset of the chip and all SPI registers (including CONFIG_A). This bit is self-clearing and will always read zero. After writing this bit, the part may take up to 5 ns to reset. During this time, do not perform any SPI transactions. |
| 6   | RESERVED   | R/W  | 0h    |                                                                                                                                                                                                                                                                                |
| 5   | ASCEND     | R/W  | 1h    | 0 : Address is decremented during streaming reads/writes<br>1 : Address is incremented during streaming reads/writes (default)                                                                                                                                                 |
| 4   | RESERVED   | R    | 1h    | Always read 1.                                                                                                                                                                                                                                                                 |
| 3-0 | RESERVED   | R/W  | 0h    |                                                                                                                                                                                                                                                                                |

### 7.5.3.2 DEVICE\_CONFIG Register (Offset = 2h) [reset = 00h]

DEVICE\_CONFIG is shown in [Figure 7-62](#) and described in [Table 7-34](#).

Return to the [Register Summary Table](#).

Device Configuration (default: 0x00)

**Figure 7-62. DEVICE\_CONFIG Register**

| 7        | 6 | 5 | 4 | 3 | 2 | 1      | 0 |
|----------|---|---|---|---|---|--------|---|
| RESERVED |   |   |   |   |   | MODE   |   |
| R/W-0h   |   |   |   |   |   | R/W-0h |   |

**Table 7-34. DEVICE\_CONFIG Register Field Descriptions**

| Bit | Field    | Type | Reset | Description |
|-----|----------|------|-------|-------------|
| 7-2 | RESERVED | R/W  | 0h    |             |

**Table 7-34. DEVICE\_CONFIG Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                    |
|-----|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1-0 | MODE  | R/W  | 0h    | 0 : Normal operation (default)<br>1 : Reserved<br>2 : Reserved<br>3 : Full power down. The user should follow the recommendations in <a href="#">Section 8.1.6</a> in this mode to avoid reliability concerns. |

**7.5.3.3 CHIP\_TYPE Register (Offset = 3h) [reset = 04h]**

CHIP\_TYPE is shown in [Figure 7-63](#) and described in [Table 7-35](#).

Return to the [Register Summary Table](#).

Chip Type (read-only: 0x04)

**Figure 7-63. CHIP\_TYPE Register**

|          |   |   |   |           |   |   |   |
|----------|---|---|---|-----------|---|---|---|
| 7        | 6 | 5 | 4 | 3         | 2 | 1 | 0 |
| RESERVED |   |   |   | CHIP_TYPE |   |   |   |
| R/W-0h   |   |   |   | R-4h      |   |   |   |

**Table 7-35. CHIP\_TYPE Register Field Descriptions**

| Bit | Field     | Type | Reset | Description                                                       |
|-----|-----------|------|-------|-------------------------------------------------------------------|
| 7-4 | RESERVED  | R/W  | 0h    |                                                                   |
| 3-0 | CHIP_TYPE | R    | 4h    | Always returns 0x4, indicating that the part is a high speed DAC. |

**7.5.3.4 CHIP\_ID Register (Offset = 4h) [reset = 003Bh]**

CHIP\_ID is shown in [Figure 7-64](#) and described in [Table 7-36](#).

Return to the [Register Summary Table](#).

Chip Identification (read-only)

**Figure 7-64. CHIP\_ID Register**

|         |    |    |    |    |    |   |   |
|---------|----|----|----|----|----|---|---|
| 15      | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CHIP_ID |    |    |    |    |    |   |   |
| R-0h    |    |    |    |    |    |   |   |
| 7       | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| CHIP_ID |    |    |    |    |    |   |   |
| R-3Bh   |    |    |    |    |    |   |   |

**Table 7-36. CHIP\_ID Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                        |
|------|---------|------|-------|--------------------------------------------------------------------|
| 15-0 | CHIP_ID | R    | 003Bh | Always returns 0x003B indicating it is the DAC39RF10 device family |

**7.5.3.5 CHIP\_VERSION Register (Offset = 6h) [reset = 02h]**

CHIP\_VERSION is shown in [Figure 7-65](#) and described in [Table 7-37](#).

Return to the [Register Summary Table](#).

Chip Version (read-only)

**Figure 7-65. CHIP\_VERSION Register**

|              |   |   |   |   |   |   |   |
|--------------|---|---|---|---|---|---|---|
| 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CHIP_VERSION |   |   |   |   |   |   |   |
| R-2h         |   |   |   |   |   |   |   |

**Table 7-37. CHIP\_VERSION Register Field Descriptions**

| Bit | Field        | Type | Reset | Description          |
|-----|--------------|------|-------|----------------------|
| 7-0 | CHIP_VERSION | R    | 02h   | 1: PG1.0<br>2: PG2.0 |

#### 7.5.3.6 VENDOR\_ID Register (Offset = Ch) [reset = 0451h]

VENDOR\_ID is shown in [Figure 7-66](#) and described in [Table 7-38](#).

Return to the [Register Summary Table](#).

Vendor Identification (default: 0x0451)

**Figure 7-66. VENDOR\_ID Register**

|           |    |    |    |    |    |   |   |
|-----------|----|----|----|----|----|---|---|
| 15        | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| VENDOR_ID |    |    |    |    |    |   |   |
| R-04h     |    |    |    |    |    |   |   |
| 7         | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| VENDOR_ID |    |    |    |    |    |   |   |
| R-51h     |    |    |    |    |    |   |   |

**Table 7-38. VENDOR\_ID Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description  |
|------|-----------|------|-------|--------------|
| 15-0 | VENDOR_ID | R    | 451h  | TI vendor ID |

#### 7.5.3.7 SYSREF\_CTRL Register (Offset = 0080h) [reset = 40h]

SYSREF\_CTRL is shown in [Figure 7-67](#) and described in [Table 7-39](#).

Return to the [Register Summary Table](#).

SYSREF Control

**Figure 7-67. SYSREF\_CTRL Register**

|                    |                       |                  |                 |            |   |   |   |
|--------------------|-----------------------|------------------|-----------------|------------|---|---|---|
| 7                  | 6                     | 5                | 4               | 3          | 2 | 1 | 0 |
| SYSREF_PRO<br>C_EN | SYSREF_REC<br>V_SLEEP | SYSREF_PS_E<br>N | SYSREF_ZOO<br>M | SYSREF_SEL |   |   |   |
| R/W-0b             | R/W-1b                | R/W-0b           | R/W-0b          | R/W-0h     |   |   |   |

**Table 7-39. SYSREF\_CTRL Register Field Descriptions**

| Bit | Field             | Type | Reset | Description                                                                                                                                                                                                                                                                                                          |
|-----|-------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | SYSREF_PROC_EN    | R/W  | 0h    | When set, this bit enables the SYSREF processor. When this is enabled, the system receives and processes each new SYSREF edge. User should always clear SYSREF_RECV_SLEEP before setting this bit. This bit is provided to allow the SYSREF receiver to stabilize before allowing the SYSREF to come to the digital. |
| 6   | SYSREF_RECV_SLEEP | R/W  | 1b    | Clear this bit to enable the SYSREF receiver circuit. User should always clear SYSREF_PROC_EN before setting this bit.                                                                                                                                                                                               |

**Table 7-39. SYSREF\_CTRL Register Field Descriptions (continued)**

| Bit | Field        | Type | Reset | Description                                                                                                                                                                                                                |
|-----|--------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5   | SYSREF_PS_EN | R/W  | 0b    | When set, SYSREF_POS will contain 1's for all positions that have been detected as near the SYSREF edge since this bit was set. When cleared, SYSREF_POS will only contain 1's for the last SYSREF edge that was detected. |
| 4   | SYSREF_ZOOM  | R/W  | 0b    | Set this bit to "zoom" in the SYSREF strobe status (impacts SYSREF_POS and the step size of SYSREF_SEL).                                                                                                                   |
| 3-0 | SYSREF_SEL   | R/W  | 0b    | Set this field to select which SYSREF delay to use. Set this based on the results returned by SYSREF_POS.                                                                                                                  |

### 7.5.3.8 SYSREF\_POS Register (Offset = 90h) [reset = NA]

SYSREF\_POS is shown in [Figure 7-68](#) and described in [Table 7-40](#).

Return to the [Register Summary Table](#).

SYSREF Position Capture

**Figure 7-68. SYSREF\_POS Register**

|            |    |    |    |            |    |    |    |
|------------|----|----|----|------------|----|----|----|
| 23         | 22 | 21 | 20 | 19         | 18 | 17 | 16 |
| RESERVED   |    |    |    | SYSREF_POS |    |    |    |
| R          |    |    |    | R          |    |    |    |
| 15         | 14 | 13 | 12 | 11         | 10 | 9  | 8  |
| SYSREF_POS |    |    |    |            |    |    |    |
| R          |    |    |    |            |    |    |    |
| 7          | 6  | 5  | 4  | 3          | 2  | 1  | 0  |
| SYSREF_POS |    |    |    |            |    |    |    |
| R          |    |    |    |            |    |    |    |

**Table 7-40. SYSREF\_POS Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                     |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23-20 | Reserved   | R    | 0x0   | Reserved                                                                                                                                                                        |
| 19-0  | SYSREF_POS | R    | NA    | Returns a 20-bit status value that indicates the position of the SYSREF edge with respect to CLK. Use this to determine the proper programming for SYSREF_SEL, and SYSREF_ZOOM. |

### 7.5.3.9 SYSREF\_ALIGN Register (Offset = 00A0h) [reset = 00h]

SYSREF\_ALIGN is shown in [Figure 7-69](#) and described in [Table 7-41](#).

Return to the [Register Summary Table](#).

SYSREF Alignment Control

**Figure 7-69. SYSREF\_ALIGN Register**

|          |   |   |   |   |   |                 |   |
|----------|---|---|---|---|---|-----------------|---|
| 7        | 6 | 5 | 4 | 3 | 2 | 1               | 0 |
| RESERVED |   |   |   |   |   | SYSREF_ALIGN_EN |   |
| R/W-00h  |   |   |   |   |   | R/W-0b          |   |

**Table 7-41. SYSREF\_ALIGN Register Field Descriptions**

| Bit | Field    | Type | Reset | Description |
|-----|----------|------|-------|-------------|
| 7-1 | RESERVED | R/W  | 00h   | Reserved    |

**Table 7-41. SYSREF\_ALIGN Register Field Descriptions (continued)**

| Bit | Field           | Type | Reset | Description                                                                                                                                |
|-----|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | SYSREF_ALIGN_EN | R/W  | 0b    | When this bit is set, the chip realigns to each detected SYSREF edge. This affects both the external clock divider and the JESD subsystem. |

#### **SYSREF\_TERM Register (Offset = 00A1h) [reset = 00h]**

SYSREF\_TERM is shown in [Figure 7-70](#) and described in [Table 7-42](#).

Return to the [Register Summary Table](#).

SYSREF Termination Configuration

**Figure 7-70. SYSREF\_TERM Register**

|          |   |   |   |   |   |   |                    |
|----------|---|---|---|---|---|---|--------------------|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0                  |
| RESERVED |   |   |   |   |   |   | SYSREF_RECV_LVPECL |
| R/W-00h  |   |   |   |   |   |   | R/W-0b             |

**Table 7-42. SYSREF\_TERM Register Field Descriptions**

| Bit | Field              | Type | Reset | Description                                                                                                                          |
|-----|--------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 7-1 | RESERVED           | R/W  | 00h   | Reserved                                                                                                                             |
| 0   | SYSREF_RECV_LVPECL | R/W  | 0b    | 0: SYSREF termination is 100 Ohm differential with Vcm of 0.4V<br>1: SYSREF termination is singled ended 50 Ohm to GND (LVPECL mode) |

#### **7.5.3.10 JESD\_EN Register (Offset = 0100h) [reset = 00h]**

JESD\_EN is shown in [Figure 7-71](#) and described in [Table 7-43](#).

Return to the [Register Summary Table](#).

JESD204C Subsystem Enable

**Figure 7-71. JESD\_EN Register**

|          |   |   |   |   |   |   |         |
|----------|---|---|---|---|---|---|---------|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0       |
| RESERVED |   |   |   |   |   |   | JESD_EN |
| R/W-00h  |   |   |   |   |   |   | R/W-0b  |

**Table 7-43. JESD\_EN Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                 |
|-----|----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-1 | RESERVED | R/W  | 00h   |                                                                                                                                                                                                                                                                                                             |
| 0   | JESD_EN  | R/W  | 0b    | 0 : Disable JESD204C interface<br>1 : Enable JESD204C interface<br>When JESD_EN=0, the JESD204C subsystem is held in reset and the SERDES PHY is disabled. The LMFC/LEMC counter is also held in reset, so SYSREF will not align the LMFC/LEMC.<br>Note: This register should only be changed when DP_EN=0. |

#### **7.5.3.11 JMODE Register (Offset = 0101h) [reset = 00h]**

JMODE is shown in [Figure 7-72](#) and described in [Table 7-44](#).

Return to the [Register Summary Table](#).

## JESD204C Mode

**Figure 7-72. JMODE Register**

| 7        | 6 | 5 | 4           | 3 | 2 | 1 | 0 |
|----------|---|---|-------------|---|---|---|---|
| RESERVED |   |   | JMODE       |   |   |   |   |
| R/W-00b  |   |   | R/W-000000b |   |   |   |   |

**Table 7-44. JMODE Register Field Descriptions**

| Bit | Field    | Type | Reset   | Description                                                                                                                         |
|-----|----------|------|---------|-------------------------------------------------------------------------------------------------------------------------------------|
| 7-6 | RESERVED | R/W  | 00b     |                                                                                                                                     |
| 5-0 | JMODE    | RW   | 000000b | Specify the JESD204C interface mode. See <a href="#">Table 7-22</a> .<br>Note: This register should only be changed when JESD_EN=0. |

### 7.5.3.12 JESD\_M Register (Offset = 0102h) [reset = 01h]

JESD\_M is shown in [Figure 7-73](#) and described in [Table 7-45](#).

Return to the [Register Summary Table](#).

## JESD204C Number of Streams

**Figure 7-73. JESD\_M Register**

| 7      | 6 | 5 | 4 | 3      | 2 | 1 | 0 |
|--------|---|---|---|--------|---|---|---|
|        |   |   |   | JESD_M |   |   |   |
| R/W-0h |   |   |   | R/W-1h |   |   |   |

**Table 7-45. JESD\_M Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-----|----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-4 | RESERVED | R/W  | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 3-0 | JESD_M   | R/W  | 1h    | Specify the number of sample streams to enable (JESD204C M parameter). The supported settings for JESD_M depend on the DUC interpolation (DUC_L) and Mx.<br><b>L<sub>DUC</sub>: Supported Settings for JESD_M</b><br>1x: 1 or 2 (but never larger than Mx)<br>2x or 3x: 2 (but never larger than Mx)<br>4x or 6x: 2 or 4 (but never larger than Mx)<br>8x or higher: 2, 4, 6 or 8 (but never larger than Mx)<br>See <a href="#">Table 7-22</a> for the Mx value associated with each JMODE. The number of lanes enabled (L) is computed as: L=ceiling(M/Mx*Lx). An I/Q pair counts as two streams. For example, when inputting 4 IQ streams, program JESD_M=8.<br>Note: This register should only be changed when JESD_EN=0 and DP_EN=0. |

### 7.5.3.13 JCTRL Register (Offset = 0103h) [reset = 03h]

JCTRL is shown in [Figure 7-74](#) and described in [Table 7-46](#).

Return to the [Register Summary Table](#).

JESD204C Control. This register should only be changed when JESD\_EN = 0.

**Figure 7-74. JCTRL Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|---|---|---|---|---|---|---|---|

**Figure 7-74. JCTRL Register (continued)**

|          |         |          |        |          |         |        |
|----------|---------|----------|--------|----------|---------|--------|
| RESERVED | TI_MODE | SUBCLASS | JENC   | RESERVED | SFORMAT | SCR    |
| R/W-0b   | R/W-0b  | R/W-0b   | R/W-0b | R/W-00b  | R/W-1b  | R/W-1b |

**Table 7-46. JCTRL Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                |
|-----|----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | RESERVED | R/W  | 0b    |                                                                                                                                                                                                                                                                                                                                                            |
| 6   | TI_MODE  | R/W  | 0b    | 0 : JESD204C standard mode (default)<br>1 : TI Mode - set this when using TI FPGA transmitter IP                                                                                                                                                                                                                                                           |
| 5   | SUBCLASS | R/W  | 0b    | Specify how the elastic buffer is released:<br>0 : Subclass 0 operation (default). Release the elastic buffer immediately once all lanes have starting writing to the buffer.<br>1 : Subclass 1 operation. Release the elastic buffer on a release opportunity defined by the LMFC/LEMC and RBD.                                                           |
| 4   | JENC     | R/W  | 0b    | 0 : Use 8b/10b link layer<br>1 : Use 64b/66b link layer                                                                                                                                                                                                                                                                                                    |
| 3-2 | RESERVED | R/W  | 0b    |                                                                                                                                                                                                                                                                                                                                                            |
| 1   | SFORMAT  | R/W  | 1b    | Input sample format for JESD204C samples<br>0 : Offset binary<br>1 : Signed 2's complement (default)                                                                                                                                                                                                                                                       |
| 0   | SCR      | R/W  | 1b    | 0 : 8b/10b Scrambler disabled<br>1 : 8b/10b Scrambler enabled (default)<br>The 8b/10b scrambler is recommended to improve spurious noise and make sure that certain sample payloads cannot prevent the JESD204C receiver from detecting incorrect code-group or lane alignment. This register has no effect on 64b/66b modes (which are always scrambled). |

#### 7.5.3.14 SHMODE Register (Offset = 0104h) [reset = 00h]

SHMODE is shown in [Figure 7-75](#) and described in [Table 7-47](#).

Return to the [Register Summary Table](#).

JESD204C Sync Word Mode

**Figure 7-75. SHMODE Register**

|          |   |   |   |   |   |         |   |
|----------|---|---|---|---|---|---------|---|
| 7        | 6 | 5 | 4 | 3 | 2 | 1       | 0 |
| RESERVED |   |   |   |   |   | SHMODE  |   |
| R/W-0b   |   |   |   |   |   | R/W-00b |   |

**Table 7-47. SHMODE Register Field Descriptions**

| Bit | Field    | Type | Reset | Description |
|-----|----------|------|-------|-------------|
| 7-2 | RESERVED | R/W  | 00h   |             |

**Table 7-47. SHMODE Register Field Descriptions (continued)**

| Bit | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-----|--------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1-0 | SHMODE | R/W  | 00b   | Select the mode for the 64b/66b sync word (32 bits of data per multi-block). This only applies when JENC=1 (64b/66b mode).<br>0 : Enable CRC-12 checking (JESD204C Table 41) (default setting)<br>1 : RESERVED<br>2 : RESERVED<br>3 : RESERVED<br>Note: This device does not support any JESD204C command features. All command fields are ignored by the receiver.<br>Note: This register should only be changed when JESD_EN=0. |

### 7.5.3.15 KM1 Register (Offset = 0105h) [reset = 1Fh]

KM1 is shown in [Figure 7-76](#) and described in [Table 7-48](#).

Return to the [Register Summary Table](#).

JESD204C K Parameter (minus 1)

**Figure 7-76. KM1 Register**

|         |   |   |   |   |   |   |   |
|---------|---|---|---|---|---|---|---|
| 7       | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| KM1     |   |   |   |   |   |   |   |
| R/W-1Fh |   |   |   |   |   |   |   |

**Table 7-48. KM1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-----|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-0 | KM1   | R/W  | 1Fh   | K is the number of frames per multiframe, and K-1 shall be programmed here when using the 8b/10b link layer (see JENC). Depending on the JMODE setting, there are constraints on the legal values of K (see <a href="#">Table 7-22</a> and KR). Programming an illegal value for K will cause the link to malfunction.<br>The default value is KM1=31, which corresponds to K=32.<br>Note: For modes using the 64b/66b link layer, the KM1 register is ignored. The effective value of K is 256*E/F.<br>Note: This register should only be changed when JESD_EN=0. |

### 7.5.3.16 RBD Register (Offset = 106h) [reset = 00h]

RBD is shown in [Figure 7-77](#) and described in [Table 7-49](#).

Return to the [Register Summary Table](#).

JESD204C Release Buffer Delay

**Figure 7-77. RBD Register**

|          |   |             |   |   |   |   |   |
|----------|---|-------------|---|---|---|---|---|
| 7        | 6 | 5           | 4 | 3 | 2 | 1 | 0 |
| RESERVED |   | RBD         |   |   |   |   |   |
| R/W-0b   |   | R/W-000000b |   |   |   |   |   |

**Table 7-49. RBD Register Field Descriptions**

| Bit | Field    | Type | Reset | Description |
|-----|----------|------|-------|-------------|
| 7-6 | RESERVED | R/W  | 00b   |             |

**Table 7-49. RBD Register Field Descriptions (continued)**

| Bit | Field | Type | Reset   | Description                                                                                                                                                                                                                                                                                                                    |
|-----|-------|------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5-0 | RBD   | R/W  | 000000b | This register shifts the elastic buffer release opportunities. Increasing RBD by 1 delays the release opportunities by 4 bytes (octets). The legal RBD range is 0 to $K \cdot F/4 - 1$ . For 64b/66b modes, the legal RBD range is 0 to 63. See Programming RBD.<br>Note: This register should only be changed when JESD_EN=0. |

### 7.5.3.17 JESD\_STATUS Register (Offset = 0107h) [reset = NA]

JESD\_STATUS is shown in [Figure 7-78](#) and described in [Table 7-50](#).

Return to the [Register Summary Table](#).

JESD204C / System Status

**Figure 7-78. JESD\_STATUS Register**

|        |         |             |           |         |            |          |   |
|--------|---------|-------------|-----------|---------|------------|----------|---|
| 7      | 6       | 5           | 4         | 3       | 2          | 1        | 0 |
| EB_ERR | LINK_UP | JSYNC_STATE | REALIGNED | ALIGNED | PLL_LOCKED | RESERVED |   |
| R/W1C  | R       | R           | R/W1C     | R       | R          | R        |   |

**Table 7-50. JESD\_STATUS Register Field Descriptions**

| Bit | Field       | Type  | Reset | Description                                                                                                                                                                                                                                                                                                                                               |
|-----|-------------|-------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | EB_ERR      | R/W1C | NA    | Elastic buffer experienced underflow/overflow. Check RBD. Write a 1 to clear this bit.                                                                                                                                                                                                                                                                    |
| 6   | LINK_UP     | R     | NA    | When set, indicates that the JESD204C link is up (elastic buffer released).                                                                                                                                                                                                                                                                               |
| 5   | JSYNC_STATE | R     | NA    | Returns the state of the JESD204C $\overline{\text{SYNC}}$ signal.<br>0 : $\overline{\text{SYNC}}$ asserted<br>1 : $\overline{\text{SYNC}}$ de-asserted                                                                                                                                                                                                   |
| 4   | REALIGNED   | R/W1C | NA    | When any clock dividers or the LMFC/LEMC counters are realigned by SYSREF, this bit gets set. Write a 1 to clear this bit. The behavior of this bit is undefined when SUBCLASS=0.                                                                                                                                                                         |
| 3   | ALIGNED     | R     | NA    | When set, indicates that the last SYSREF pulse was consistent with the SYSREF-associated clock dividers (including the LMFC/LEMC). This bit is read-only (cannot be cleared via SPI). After JESD_EN is set, the part may require up to 7 SYSREF pulses to achieve full alignment and set this bit. The behavior of this bit is undefined when SUBCLASS=0. |
| 2   | PLL_LOCKED  | R     | NA    | When high, indicates that all enabled SerDes PLLs are locked.                                                                                                                                                                                                                                                                                             |
| 1-0 | RESERVED    | R     | NA    |                                                                                                                                                                                                                                                                                                                                                           |

### 7.5.3.18 REFDIV Register (Offset = 0108h) [reset = 30h]

REFDIV is shown in [Figure 7-79](#) and described in [Table 7-51](#).

Return to the [Register Summary Table](#).

JESD204C Reference Divider

**Figure 7-79. REFDIV Register**

|   |   |   |   |   |   |   |   |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|

**Figure 7-79. REFDIV Register (continued)**

|          |         |
|----------|---------|
| RESERVED | REFDIV  |
| R/W-0b   | R/W-30h |

**Table 7-51. REFDIV Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                |
|-----|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-6 | RESERVED | R/W  | 00b   |                                                                                                                                                                                                                                                                                            |
| 5-0 | REFDIV   | R/W  | 30h   | Specifies the frequency divisor to generate the PHY PLL reference clock (FREF) from the DAC clock (F <sub>CLK</sub> ). See PLL Control.<br>The following values are legal: 2, 3, 4, 5, 6, 8, 10, 12, 16, 20, 24, 32, 40, 48. All other values are reserved and produce undefined behavior. |

### 7.5.3.19 MPY Register (Offset = 0109h) [reset = 14h]

MPY is shown in [Figure 7-80](#) and described in [Table 7-52](#).

Return to the [Register Summary Table](#).

JESD204C PLL Multiplier

**Figure 7-80. MPY Register**

|         |   |   |   |   |   |   |   |
|---------|---|---|---|---|---|---|---|
| 7       | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MPY     |   |   |   |   |   |   |   |
| R/W-14h |   |   |   |   |   |   |   |

**Table 7-52. MPY Register Field Descriptions**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                     |
|-----|-------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-0 | MPY   | R/W  | 14h   | Specifies the PLL frequency multiplier for the PHY. See PLL Control.<br>The following values are allowed for this design:<br><b>MPY: Frequency Multiplier</b><br>16 (0x10): 4<br>20 (0x14): 5<br>33 (0x21): 8.25<br>40 (0x28): 10<br>Note: This register should only be changed when JESD_EN=0. |

### 7.5.3.20 RATE Register (Offset = 010Ah) [reset = 00h]

RATE is shown in [Figure 7-81](#) and described in [Table 7-53](#).

Return to the [Register Summary Table](#).

JESD204C Receive Rate

**Figure 7-81. RATE Register**

|          |   |   |   |   |   |         |   |
|----------|---|---|---|---|---|---------|---|
| 7        | 6 | 5 | 4 | 3 | 2 | 1       | 0 |
| RESERVED |   |   |   |   |   | RATE    |   |
| R/W-00h  |   |   |   |   |   | R/W-00b |   |

**Table 7-53. RATE Register Field Descriptions**

| Bit | Field    | Type | Reset | Description |
|-----|----------|------|-------|-------------|
| 7-2 | RESERVED | R/W  | 00h   |             |

**Table 7-53. RATE Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                        |
|-----|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1-0 | RATE  | R/W  | 00b   | Controls the frequency multiplier from the PHY PLL to the serial line rate. See PLL Control. Affects all lanes.<br><b>RATE: Multiplier</b><br>00b: 4<br>01b: 2<br>10b: 1<br>11b: 0.5<br>Note: This register should only be changed when JESD_EN=0. |

#### 7.5.3.21 LB\_VRANGE Register (Offset = 010Bh) [reset = 00h]

LB\_VRANGE is shown in [Figure 7-82](#) and described in [Table 7-54](#).

Return to the [Register Summary Table](#).

JESD204C PLL VCO Range. Note: This register should only be changed when JESD\_EN=0.

**Figure 7-82. LB\_VRANGE Register**

|          |   |   |   |   |   |   |        |
|----------|---|---|---|---|---|---|--------|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0      |
| RESERVED |   |   |   |   |   |   | VRANGE |
| R/W-0h   |   |   |   |   |   |   | R/W-0b |

**Table 7-54. LB\_VRANGE Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                      |
|-----|----------|------|-------|----------------------------------------------------------------------------------|
| 7-1 | RESERVED | R/W  | 00h   |                                                                                  |
| 0   | VRANGE   | R/W  | 0b    | This bit must be set if the PLL/VCO frequency is below 2.17GHz. See PLL Control. |

#### 7.5.3.22 JSYNC\_N Register (Offset = 0120h) [reset = 01h]

JSYNC\_N is shown in [Figure 7-67](#) and described in [Table 7-39](#).

Return to the [Register Summary Table](#).

JESD204C Manual Sync Request

**Figure 7-83. JSYNC\_N Register**

|          |   |   |   |   |   |   |         |
|----------|---|---|---|---|---|---|---------|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0       |
| RESERVED |   |   |   |   |   |   | JSYNC_N |
| R/W-00h  |   |   |   |   |   |   | R/W1C   |

**Table 7-55. JSYNC\_N Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                       |
|-----|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-1 | RESERVED | R/W  | 00h   |                                                                                                                                                                                   |
| 0   | JSYNC_N  | R/W  | 1b    | Set this bit to 0 to manually assert the $\overline{\text{SYNC}}$ signal. For normal operation, leave this bit set to 1.<br>Note: Behavior of JSYNC_N=0 is undefined when JENC=1. |

#### 7.5.3.23 JTEST Register (Offset = 0121h) [reset = 00h]

JTEST is shown in [Figure 7-84](#) and described in [Table 7-56](#).

Return to the [Register Summary Table](#).

JESD204C Test Control

**Figure 7-84. JTEST Register**

| 7        | 6 | 5 | 4 | 3       | 2 | 1 | 0 |
|----------|---|---|---|---------|---|---|---|
| RESERVED |   |   |   | JTEST   |   |   |   |
| R/W-000b |   |   |   | R/W-00h |   |   |   |

**Table 7-56. JTEST Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                  |
|-----|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-5 | RESERVED | R/W  | 0h    |                                                                                                                                                                                                                                                                                                                                              |
| 4-0 | JTEST    | R/W  | 0b    | <p>PRBS Test Modes:</p> <p>0 : Test mode disabled. Normal operation (default)</p> <p>1 : PRBS7 test mode</p> <p>2 : PRBS9 test mode</p> <p>3 : PRBS15 test mode</p> <p>4 : PRBS31 test mode</p> <p>5-31: RESERVED</p> <p>When a PRBS test mode is enabled, see BER_EN.</p> <p>Note: This register should only be changed when JESD_EN=0.</p> |

#### 7.5.3.24 JTIMER Register (Offset = 0124h) [reset = 00h]

JTIMER is shown in [Figure 7-85](#) and described in [Table 7-57](#).

Return to the [Register Summary Table](#).

Note: This register should only be changed when JESD\_EN=0.

JESD204C Watchdog Timer

**Figure 7-85. JTIMER Register**

| 7      | 6        | 5      | 4 | 3        | 2        | 1 | 0 |
|--------|----------|--------|---|----------|----------|---|---|
| JTPLL  | RESERVED | JTR    |   | RESERVED | JTT      |   |   |
| R/W-0b | R/W-0b   | R/W-0b |   | R/W-0b   | R/W-000b |   |   |

**Table 7-57. JTIMER Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                    |
|-----|----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | JTPLL    | R/W  | 1b    | When this bit is set, the SerDes PLL is also reset when the watchdog timer expires. When this bit is 0, only the SerDes receiver is reset.                                                                                                                                                                                                     |
| 6   | RESERVED | R/W  | 0b    |                                                                                                                                                                                                                                                                                                                                                |
| 5-4 | JTR      | R/W  | 00b   | <p>This register determines how much the watchdog counter is decremented when the link is up and CRC_FAULT is not set.</p> <p><b>JTR : Watchdog Counter Decrement : Approximate Link Uptime % required to prevent the SerDes from being reset</b></p> <p>0 : 1 : 99.25%</p> <p>1 : 2 : 98.46%</p> <p>2 : 8 : 94.12%</p> <p>3 : 16 : 88.89%</p> |
| 3   | RESERVED | R/W  | 0b    |                                                                                                                                                                                                                                                                                                                                                |

**Table 7-57. JTIMER Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-----|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2-0 | JTT   | R/W  | 0b    | <p>JESD204C watchdog counter threshold. When the watchdog counter reaches the threshold defined by JTT, the PHY layer is reset (including the PHY PLL(s) if JTPLL=1) and the watchdog timer is reset. Larger values of JTT cause the watchdog timer to take longer to intervene.</p> <p>JTT : Watchdog Counter Threshold : Counter Duration [assuming <math>F_{CLK} = 10.24 \text{ GHz}</math>]</p> <p>0 : &lt;Watchdog Timer Disabled&gt; : &lt;disabled&gt;</p> <p>1 : <math>2^{17}</math> : 102.4 <math>\mu\text{s}</math></p> <p>2 : <math>2^{19}</math> : 409.6 <math>\mu\text{s}</math></p> <p>3 : <math>2^{32}</math> : 1.63 ms</p> <p>4 : <math>2^{23}</math> : 6.55 ms</p> <p>5-7 : RESERVED : RESERVED</p> <p>Note: The watchdog may not detect link up events shorter than <math>2^{10}</math> (1024) CLK cycles.</p> |

#### 7.5.3.25 SYNC\_EPW Register (Offset = 0127h) [reset = 00h]

SYNC\_EPW is shown in [Figure 7-86](#) and described in [Table 7-58](#).

Return to the [Register Summary Table](#).

JESD204C SYNC Error Report Pulse Width

**Figure 7-86. SYNC\_EPW Register**

|          |   |   |   |   |          |   |   |
|----------|---|---|---|---|----------|---|---|
| 7        | 6 | 5 | 4 | 3 | 2        | 1 | 0 |
| RESERVED |   |   |   |   | SYNC_EPW |   |   |
| R/W-00h  |   |   |   |   | R/W-000b |   |   |

**Table 7-58. SYNC\_EPW Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-----|----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-3 | RESERVED | R/W  | 00h   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 2-0 | SYNC_EPW | R/W  | 000b  | <p>Specifies the pulse width of <math>\overline{\text{SYNC}}</math> that is used for reporting errors to the transmitter. When an error is detected that does not require link resynchronization, <math>\overline{\text{SYNC}}</math> is asserted for SYNC_EPW link clock cycles (equal to <math>4 \times \text{SYNC\_EPW}</math> character durations). To disable error reporting over <math>\overline{\text{SYNC}}</math>, set SYNC_EPW=0. The legal range for SYNC_EPW is 0 to 7.</p> <p>Note: This register should only be changed when JESD_EN= 0.</p> |

#### 7.5.3.26 CRC\_TH Register (Offset = 0128h) [reset = 00h]

CRC\_TH is shown in [Figure 7-87](#) and described in [Table 7-59](#).

Return to the [Register Summary Table](#).

JESD204C CRC Error Thresholds

**Figure 7-87. CRC\_TH Register**

|          |   |   |   |             |   |            |   |
|----------|---|---|---|-------------|---|------------|---|
| 7        | 6 | 5 | 4 | 3           | 2 | 1          | 0 |
| RESERVED |   |   |   | CRC_ERR_REC |   | CFC_ERR_TH |   |
| R/W-0h   |   |   |   | R/W-00b     |   | R/W-00b    |   |

**Figure 7-87. CRC\_TH Register (continued)**

**Table 7-59. CRC\_TH Register Field Descriptions**

| Bit | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                                             |
|-----|-------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-4 | RESERVED    | R/W  | 0h    |                                                                                                                                                                                                                                                                                                         |
| 3-2 | CRC_ERR_REC | R/W  | 0b    | Specify how many contiguous, error-free multiblocks must be received to reset the CRC error counter (and un-trigger the CRC alarm if triggered).<br>0 : 1 multiblock<br>1 : 4 multiblocks<br>2 : 16 multiblocks<br>3 : 64 multiblocks                                                                   |
| 1-0 | CRC_ERR_TH  | R/W  | 0b    | Specify how many multi-blocks must have CRC errors to trigger the CRC alarm. The receiver counts each error, but if a run of error-free multi-blocks occurs (as specified by CRC_ERR_REC), the error counter resets.<br>0 : 1 multiblock<br>1 : 2 multiblocks<br>2 : 4 multiblocks<br>3 : 8 multiblocks |

Note: For each lane, the internal signal, CRC\_FAULT, is set if the number of multi-blocks with CRC errors exceeds the threshold set by CRC\_ERR\_TH without a run of contiguous, error-free multi-blocks specified by CRC\_ERR\_REC. CRC\_FAULT is cleared when a run of contiguous, error-free multi-blocks specified by CRC\_ERR\_REC is detected.

Note: This register should only be changed when JESD\_EN=0.

#### 7.5.3.27 LANE\_ARSTAT Register (Offset = 012Ch) [reset = NA]

LANE\_ARSTAT is shown in [Figure 7-88](#) and described in [Table 7-60](#).

Return to the [Register Summary Table](#).

Lane Arrival Status

**Figure 7-88. LANE\_ARSTAT Register**

|          |   |   |   |   |   |   |              |
|----------|---|---|---|---|---|---|--------------|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0            |
| RESERVED |   |   |   |   |   |   | LANE_ARR_RDY |
| R/W-00h  |   |   |   |   |   |   | R            |

**Table 7-60. LANE\_ARSTAT Register Field Descriptions**

| Bit | Field        | Type | Reset | Description                                                                                                                                                                                                                                            |
|-----|--------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-1 | RESERVED     | R/W  | 00h   |                                                                                                                                                                                                                                                        |
| 0   | LANE_ARR_RDY | R    | NA    | This bit is set when lane arrival times are captured and available for read in LANE_ARR. Lane arrival data is captured when all lanes are ready and the chip attempts to release the elastic buffer. This bit is cleared when JESD_EN=0 or JESD_RST=1. |

#### 7.5.3.28 LANE\_INV Register (Offset = 012Eh) [reset = 0000h]

LANE\_INV is shown in [Figure 7-89](#) and described in [Table 7-61](#).

Return to the [Register Summary Table](#).

## SerDes Lane Inversion

### Note

Only lanes 6 and 14 are connected on DDS devices. All other lanes are disconnected.

**Figure 7-89. LANE\_INV Register**

|                |    |    |    |    |    |   |   |
|----------------|----|----|----|----|----|---|---|
| 15             | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| LANE_INV[15:8] |    |    |    |    |    |   |   |
| R/W-00h        |    |    |    |    |    |   |   |
| 7              | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| LANE_INV[7:0]  |    |    |    |    |    |   |   |
| R/W-00h        |    |    |    |    |    |   |   |

**Table 7-61. LANE\_INV Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                               |
|------|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15-0 | LANE_INV | R/W  | 0000h | Program LANE_INV[n]=1 to invert the bitstream through physical lane n. Use this if the differential pair is swapped between the transmitter and receiver. |

### 7.5.3.29 LANE\_SEL[15:0] Register (Offset = 0130h) [reset for LANE\_SEL[ n ]= n ]

LANE\_SEL[15:0] forms a crossbar switch, and is a set of 16 registers for specifying which physical lane is bound to logical lane *n*. LANE\_SEL[15:0] is shown in [Figure 7-90](#) and described in [Table 7-62](#).

Return to the [Register Summary Table](#).

SerDes Lane Select for Logical Lane *n* (*n* = 0 - 15). LANE\_SEL[0] is at the lowest address.

### Note

Only lanes 6 and 14 are connected on DDS devices. All other lanes are disconnected.

**Figure 7-90. LANE\_SEL[15:0] Register**

|          |   |   |   |               |   |   |   |
|----------|---|---|---|---------------|---|---|---|
| 7        | 6 | 5 | 4 | 3             | 2 | 1 | 0 |
| RESERVED |   |   |   | LANE_SEL[n]   |   |   |   |
| R/W-0h   |   |   |   | R/W- <i>n</i> |   |   |   |

**Table 7-62. LANE\_SEL[15:0] Register Field Descriptions**

| Bit | Field       | Type | Reset    | Description                                                                                                                                                                                                                                                                                                      |
|-----|-------------|------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-4 | RESERVED    | R/W  | 0h       |                                                                                                                                                                                                                                                                                                                  |
| 3-0 | LANE_SEL[n] | R/W  | <i>n</i> | Specify which physical lane (0 to 15) is bound to logical lane <i>n</i> . To bind physical lane <i>p</i> to logical lane <i>n</i> , program LANE_SEL[n]= <i>p</i> . For example, to bind logical lane 0 to physical lane 3, program LANE_SEL[0]=3.<br>Note: This register should only be changed when JESD_EN=0. |

### 7.5.3.30 LANE\_ARR[15:0] Register (Offset = 0140h) [Read only, reset = NA]

LANE\_ARR[15:0] is a set of 16 registers for measuring the arrival time of lane *n*. LANE\_ARR[15:0] is shown in [Figure 7-91](#) and described in [Table 7-63](#).

Return to the [Register Summary Table](#).

SerDes Lane *n* Arrival Time (*n* = 0 - 15). LANE\_ARR[0] is at the lowest address.

**Note**

Only lanes 6 and 14 are connected on DDS devices. All other lanes are disconnected.

**Figure 7-91. LANE\_ARR[15:0] Register**

|          |   |   |             |   |   |   |   |
|----------|---|---|-------------|---|---|---|---|
| 7        | 6 | 5 | 4           | 3 | 2 | 1 | 0 |
| RESERVED |   |   | LANE_ARR[n] |   |   |   |   |
| R-00b    |   |   | R           |   |   |   |   |

**Table 7-63. LANE\_ARR[15:0] Register Field Descriptions**

| Bit | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-----|-------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-6 | RESERVED    | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 5-0 | LANE_ARR[n] | R    | NA    | Returns the arrival time of lane <i>n</i> with respect to the internal LMFC/LEMC that is established by SYSREF. The value returned can be between 0 and 63 (inclusive), regardless of the multiframe/EMB length. These registers are valid only when LANE_ARR_RDY = 1. See <a href="#">Programming RBD</a> .<br>Note: The lane arrival data is captured when attempting to release the elastic buffer and LANE_ARR_RDY=0. All values are from the same release attempt.<br>Note: It may be necessary to use JESD_RST when starting the link to get accurate lane arrival values. |

### 7.5.3.31 LANE\_STATUS[15:0] Register (Offset = 0150h) [Read only, reset = NA]

LANE\_STATUS[15:0] is a set of 16 registers showing the status of lane *n*. LANE\_STATUS[15:0] is shown in [Figure 7-92](#) and described in [Table 7-64](#).

Return to the [Register Summary Table](#).

SerDes Lane *n* Status (*n* = 0 - 15). LANE\_STATUS[0] is at the lowest address.

**Note**

Only lanes 6 and 14 are connected on DDS devices. All other lanes are disconnected.

**Figure 7-92. LANE\_STATUS[15:0] Register**

|          |   |   |   |   |                |   |   |
|----------|---|---|---|---|----------------|---|---|
| 7        | 6 | 5 | 4 | 3 | 2              | 1 | 0 |
| RESERVED |   |   |   |   | LANE_STATUS[n] |   |   |
| R-00h    |   |   |   |   | R              |   |   |

**Table 7-64. LANE\_STATUS[15:0] Register Field Descriptions**

| Bit | Field         | Type | Reset | Description                                                                                           |
|-----|---------------|------|-------|-------------------------------------------------------------------------------------------------------|
| 7-3 | RESERVED      | R    | 00h   |                                                                                                       |
| 2   | F_EMB_SYNC[n] | R    | NA    | Returns 1 if logical lane <i>n</i> has frame or EMB synchronization.                                  |
| 1   | CG_BK_SYNC[n] | R    | NA    | Returns 1 if logical lane <i>n</i> has code-group or block synchronization.                           |
| 0   | SIG_DET[n]    | R    | NA    | Returns 1 if logical lane <i>n</i> is detecting a data signal (using loss-of-signal detector in PHY). |

### 7.5.3.32 LANE\_ERR[15:0] Register (Offset = 0160h) [reset = 00h]

LANE\_ERR[15:0] is a set of 16 registers reporting errors for lane *n*. LANE\_ERR[15:0] is shown in [Figure 7-93](#) and described in [Table 7-65](#).

Return to the [Register Summary Table](#).

SerDes Lane  $n$  Error Flags ( $n = 0 - 15$ ). LANE\_ERR[0] is at the lowest address.

**Note**

Only lanes 6 and 14 are connected on DDS devices. All other lanes are disconnected.

**Figure 7-93. LANE\_ERR[15:0] Register**

|             |   |   |   |   |   |   |   |
|-------------|---|---|---|---|---|---|---|
| 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LANE_ERR[n] |   |   |   |   |   |   |   |
| R/W1C       |   |   |   |   |   |   |   |

**Table 7-65. LANE\_ERR[15:0] Register Field Descriptions**

| Bit | Field       | Type  | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-----|-------------|-------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-0 | LANE_ERR[n] | R/W1C | 00h   | <p>Sticky bits indicating various errors on lane <math>n</math>. A bit is set to indicate an error. Write a 1 to clear a bit.</p> <p>[7] Alignment character found at unexpected location (8b/10b) or (extended)-multi-block pilot signal not in expected location (64b/66b)</p> <p>[6] Multi-frame, multi-block, or extended-multi-block alignment lost.</p> <p>[5] Frame alignment was lost (8b/10b only) or CRC_FAULT=1 (64b/66b).</p> <p>[4] Code-group or block synchronization was lost.</p> <p>[3] RESERVED</p> <p>[2] Not-in-table or unexpected control character (8b/10b) or CRC (64b/66b) error occurred.</p> <p>[1] Disparity error (8b/10b) or invalid sync header (64b/66b) occurred.</p> <p>[0] Gearbox FIFO overflowed or underflowed. As long as the write clock frequency is correct the gearbox write clock can drift at least 3UI after this flag without causing data corruption.</p> <p>Note: Lane Error Flags for extra or disabled lanes are undefined.</p> <p>Note: LANE_ERR[6:1] are only detected for 8b/10b operation while sync_n=1</p> |

### 7.5.3.33 FIFO\_STATUS[15:0] Register (Offset = 0170h) [Read only, reset = NA]

FIFO\_STATUS[15:0] is a set of 16 registers showing the status of lane  $n$ . LANE\_STATUS[15:0] is shown in [Figure 7-94](#) and described in [Table 7-66](#).

Return to the [Register Summary Table](#).

SerDes Lane  $n$  Status ( $n = 0 - 15$ ). FIFO\_STATUS[0] is at the lowest address.

**Note**

Only lanes 6 and 14 are connected on DDS devices. All other lanes are disconnected.

**Figure 7-94. FIFO\_STATUS[15:0] Register**

|          |   |   |   |          |   |   |   |
|----------|---|---|---|----------|---|---|---|
| 7        | 6 | 5 | 4 | 3        | 2 | 1 | 0 |
| RESERVED |   |   |   | PDIFF[n] |   |   |   |
| R-000b   |   |   |   | R        |   |   |   |

**Table 7-66. FIFO\_STATUS[15:0] Register Field Descriptions**

| Bit | Field    | Type | Reset | Description |
|-----|----------|------|-------|-------------|
| 7-5 | RESERVED | R    | 000b  |             |

**Table 7-66. FIFO\_STATUS[15:0] Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-----|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4-0 | PDIFF[n] | R    | NA    | <p>This register returns the difference between the write and read pointers inside the gearbox FIFO for logical lane n.</p> <p>For 8b/10b, values from 0-14 will be returned. For 64b/66b, values from 0-16 will be returned.</p> <p>The values at the ends of the range (0 &amp; 14 for 8b/10b or 0 &amp; 16 for 64b/66b) indicate error positions that will cause the Gearbox FIFO overflow/underflow flag to be set in LANE_ERR. In both cases, 1 indicates minimum setup and the max value minus 1 indicates minimum hold.</p> <p>Values are measured in the read clock. The tread size is approximately <math>\frac{1}{2}</math> of the effective link layer clock period (<math>0.5 / (LCR * FDR)</math>). In terms of UI:</p> <ul style="list-style-type: none"> <li>In 8b/10b mode, the nominal tread size is 20UI. The nominal tread size for the final tread (14) is <math>380UI \pm 20UI</math>.</li> <li>In 64b/66b mode, the nominal tread size is 16.5UI. The nominal tread size for the final tread (16) is <math>412.5UI \pm 16.5UI</math>.</li> </ul> <p>The PDIFF[n] value for disabled lanes and lanes enabled by EXTRA_LANE are undefined.</p> |

#### 7.5.3.34 BER\_EN Register (Offset = 01A0h) [reset = 00h]

BER\_EN is shown in [Figure 7-95](#) and described in [Table 7-67](#).

Return to the [Register Summary Table](#).

BER Measurement Control

**Figure 7-95. BER\_EN Register**

|          |   |   |   |   |   |   |        |
|----------|---|---|---|---|---|---|--------|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0      |
| RESERVED |   |   |   |   |   |   | BER_EN |
| R/W-0b   |   |   |   |   |   |   | R/W-0b |

**Table 7-67. BER\_EN Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                         |
|-----|----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-1 | RESERVED | R/W  | 00h   |                                                                                                                                                                                                                                                                                                                                                                                     |
| 0   | BER_EN   | R/W  | 0b    | <p>BER (bit-error-rate) test enable. After setting up the receiver parameters, the user can program JTEST to a PRBS mode, set JESD_EN, and then set BER_EN to enable the BER counters (see BER_CNTn). To clear and restart the counters, program BER_EN to 0 and then back to 1. The BER logic will self-synchronize to the incoming PRBS data after the rising edge of BER_EN.</p> |

#### 7.5.3.35 BER\_CNT Register (Offset = 01B0h) [reset = NA, read only]

BER\_CNT is shown in [Figure 7-96](#) and described in [Table 7-68](#).

Return to the [Register Summary Table](#).

BER Error Count for Lane n. Lane 0 is a the lowest address

**Figure 7-96. BER\_CNT Register**

|            |   |   |   |   |   |   |   |
|------------|---|---|---|---|---|---|---|
| 7          | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BER_CNT[n] |   |   |   |   |   |   |   |

**Figure 7-96. BER\_CNT Register (continued)**

R/W-0b

**Table 7-68. BER\_CNT Register Field Descriptions**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-----|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-0 | BER_CNT[n] | R/W  | 0h    | Returns the number of bit errors detected on lane n. This value will saturate at 255. The BER for lane n can be computed as follows:<br>BER = BER_CNT[n] / FBIT / TBER<br>Where TBER is the number of seconds that has elapsed from when BER_EN was set to when BER_CNT[n] was read. TBER is measured by the host system or clock.<br>Example: If BER_CNT[n] returns 2, and FBIT is 12.8Gbps, and TBER is 3600 seconds, the bit-error-rate is 2/12.8e9/3600 = 43e-15<br>Note: The error counters on disabled lanes and lanes enabled by EXTRA_LANE are undefined. |

### 7.5.3.36 JPHY\_CTRL Register (Offset = 01C1h) [reset = 43h]

JPHY\_CTRL is shown in [Figure 7-97](#) and described in [Table 7-69](#).

Return to the [Register Summary Table](#).

JESD204C SerDes Control. Note: This register should only be changed when JESD\_EN = 0.

**Figure 7-97. JPHY\_CTRL Register**

| 7        | 6        | 5 | 4 | 3        | 2 | 1      | 0      |
|----------|----------|---|---|----------|---|--------|--------|
| RESERVED | CDR      |   |   | RESERVED |   | OC_EN  | LOS_EN |
| R/W-0b   | R/W-100b |   |   | R/W-0b   |   | R/W-1b | R/W-1b |

**Table 7-69. JPHY\_CTRL Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                              |
|-----|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | RESERVED | R/W  | 0b    |                                                                                                                                                                                                                                                                                                                                                                          |
| 6-4 | CDR      | R/W  | 100b  | Control CDR (clock-data-recovery) setting. The default value should be appropriate, but other settings can be used to adjust the tracking rate or reduce CDR power consumption. The 2nd order modes are for tracking a frequency offset when the Tx and Rx do not share a common reference clock. This is not applicable to JESD204C. See <a href="#">CDR Settings</a> . |
| 3-2 | RESERVED | R/W  | 00b   |                                                                                                                                                                                                                                                                                                                                                                          |
| 1   | OC_EN    | R/W  | 1b    | Enable offset compensation/calibration for all lanes.                                                                                                                                                                                                                                                                                                                    |
| 0   | LOS_EN   | R/W  | 1b    | Enable loss-of-signal detector for all lanes.                                                                                                                                                                                                                                                                                                                            |

**Table 7-70. CDR Settings**

| CDR         | Vote Threshold | Tracking Rate [ppm] | Order           | Settling Time [UI] | Activity % |
|-------------|----------------|---------------------|-----------------|--------------------|------------|
| 0           | 15             | 313                 | 2 <sup>nd</sup> | 36                 | 83         |
| 1           | 7              | 607                 | 2 <sup>nd</sup> | 36                 | 70         |
| 2           | 3              | 723                 | 2 <sup>nd</sup> | 36                 | 50         |
| 3           | 1              | 868                 | 2 <sup>nd</sup> | 36                 | 25         |
| 4 (default) | 15             | 96                  | 1 <sup>st</sup> | 36                 | 83         |
| 5           | 3              | 289                 | 1 <sup>st</sup> | 36                 | 50         |
| 6           | 1              | 434                 | 1 <sup>st</sup> | 36                 | 25         |

**Table 7-70. CDR Settings (continued)**

| CDR | Vote Threshold | Tracking Rate [ppm] | Order           | Settling Time [UI] | Activity % |
|-----|----------------|---------------------|-----------------|--------------------|------------|
| 7   | 7              | 13                  | 1 <sup>st</sup> | 1524               | 5          |

### 7.5.3.37 EQ\_CTRL Register (Offset = 01C2h) [reset = 00h]

EQ\_CTRL is shown in [Figure 7-98](#) and described in [Table 7-71](#).

Return to the [Register Summary Table](#).

SerDes Equalizer Control

**Figure 7-98. EQ\_CTRL Register**

| 7        | 6 | 5 | 4      | 3       | 2      | 1       | 0 |
|----------|---|---|--------|---------|--------|---------|---|
| RESERVED |   |   | EQ_OVR | EQZ_OVR | EQHLD  | EQMODE  |   |
| R/W-000b |   |   | R/W-0b | R/W-0b  | R/W-0b | R/W-00b |   |

**Table 7-71. EQ\_CTRL Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                                                                             |
|-----|----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-5 | RESERVED | R/W  | 000b  |                                                                                                                                                                                                                                                                         |
| 4   | EQ_OVR   | R/W  | 0b    | When EQMODE=1, you can program EQ_OVR=1 to over-ride the equalizer level using the EQLEVEL[n] registers. Affects all lanes.                                                                                                                                             |
| 3   | EQZ_OVR  | R/W  | 0b    | Set this bit to enable the EQZERO register (to override the equalizer's zero frequency). When EQZ_OVR=0, the frequency is set based on the RATE register. Affects all lanes.                                                                                            |
| 2   | EQHLD    | R/W  | 0b    | When the equalizer is in fully-adaptive mode (EQMODE=1 and EQ_OVR=0), programming EQHLD will freeze (hold) the adaptation loop (for all lanes).                                                                                                                         |
| 1-0 | EQMODE   | R/W  | 00b   | Sets the equalizer mode (for all lanes): See Equalizer.<br>0: Equalizer disabled. Flat response with maximum gain.<br>1: Equalizer enabled. The equalizer is fully adaptive if EQ_OVR=0.<br>2: Precursor equalization analysis.<br>3: Postcursor equalization analysis. |

### 7.5.3.38 EQZERO Register (Offset = 01C3h) [reset = 00h]

EQZERO is shown in [Figure 7-99](#) and described in [Table 7-72](#).

Return to the [Register Summary Table](#).

SerDes Equalizer Zero.

**Figure 7-99. EQZERO Register**

| 7        | 6 | 5 | 4       | 3 | 2 | 1 | 0 |
|----------|---|---|---------|---|---|---|---|
| RESERVED |   |   | EQZERO  |   |   |   |   |
| R/W-000b |   |   | R/W-00h |   |   |   |   |

**Table 7-72. EQZERO Register Field Descriptions**

| Bit | Field    | Type | Reset | Description |
|-----|----------|------|-------|-------------|
| 7-5 | RESERVED | R/W  | 000b  |             |

**Table 7-72. EQZERO Register Field Descriptions (continued)**

| Bit | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-----|--------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4-0 | EQZERO | R/W  | 00h   | When EQZ_OVR=1, this field over-rides the equalizer's zero frequency (for all lanes). When EQZ_OVR=0, the zero frequency is set automatically based on the RATE setting.<br>0x1F: 365 MHz (default setting for full and half-rate, RATE = 0 or 1)<br>0x1E: 275 MHz<br>0x1D: 195 MHz<br>0x1B: 140 MHz (default setting for quarter-rate mode, RATE = 2)<br>0x19: 105 MHz<br>0x10: 75 MHz<br>0x08: 55 MHz (default setting for eighth-rate, RATE = 3)<br>0x00: 50 MHz |

### 7.5.3.39 LANE\_EQ[15:0] Register (Offset = 01D0h) [reset = 08h]

LANE\_EQ[15:0] is shown in [Figure 7-100](#) and described in [Table 7-73](#).

Return to the [Register Summary Table](#).

SerDes Equalizer Level for Physical Lane [n]. LANE\_EQ[0] is at the lowest address.

#### Note

Only lanes 6 and 14 are connected on DDS devices. All other lanes are disconnected.

**Figure 7-100. LANE\_EQ[15:0] Register**

|          |            |   |            |   |   |   |   |
|----------|------------|---|------------|---|---|---|---|
| 7        | 6          | 5 | 4          | 3 | 2 | 1 | 0 |
| RESERVED | EQBOOST[n] |   | EQLEVEL[n] |   |   |   |   |
| R/W-0b   | R/W-00b    |   | R/W-00h    |   |   |   |   |

**Table 7-73. LANE\_EQ[15:0] Register Field Descriptions**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                      |
|-----|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | RESERVED   | R/W  | 0b    |                                                                                                                                                                                                  |
| 6-5 | EQBOOST[n] | R/W  | 00b   | Controls EQ boost for physical lane n.<br><b>EQBOOST : GAIN Boost : BW Change : Power Increase</b><br>0 : 0dB : 0% : 0mW<br>1 : 2dB : -30% : 0mW<br>2 : 4dB : +10% : 5mW<br>3 : 6dB : -20% : 5mW |
| 4-0 | EQLEVEL[n] | R/W  | 00h   | When EQ_OVR=1, this field controls the equalization level for lane n. The valid range is from 0 (least equalization) to 16 (most equalization).                                                  |

### 7.5.3.40 LANE\_EQS[15:0] Register (Offset = 01E0h) [reset = NA, read only]

LANE\_EQS[15:0] is shown in [Figure 7-101](#) and described in [Table 7-74](#).

Return to the [Register Summary Table](#).

Serdes Equalizer Status for Physical Lane n

#### Note

Only lanes 6 and 14 are connected on DDS devices. All other lanes are disconnected.

**Figure 7-101. LANE\_EQS[15:0] Register**

| 7        | 6         | 5          | 4            | 3 | 2 | 1 | 0 |
|----------|-----------|------------|--------------|---|---|---|---|
| RESERVED | EQOVER[n] | EQUNDER[n] | EQLEVEL_S[n] |   |   |   |   |
| R        | R         | R          | R            |   |   |   |   |

**Table 7-74. LANE\_EQS[15:0] Register Field Descriptions**

| Bit | Field        | Type | Reset | Description                                                                                                                                                                                                   |
|-----|--------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | RESERVED     | R    |       |                                                                                                                                                                                                               |
| 6   | EQOVER[n]    | R    |       | EQOVER status for PHY lane <i>n</i> pre/post cursor analysis. See <a href="#">Pre/Post Cursor Analysis Procedure</a> .                                                                                        |
| 5   | EQUNDER[n]   | R    |       | EQUNDER status for PHY lane <i>n</i> pre/post cursor analysis. See <a href="#">Pre/Post Cursor Analysis Procedure</a> .                                                                                       |
| 4   | EQLEVEL_S[n] | R    |       | This field returns the equalizer level currently in effect for lane <i>n</i> . This is the count of the number of bits set in the thermometer encoded value from the strx EQLEVEL_S field for lane <i>n</i> . |

#### 7.5.3.41 ESRUN Register (Offset = 01F0h) [reset = 00h]

ESRUN is shown in [Figure 7-102](#) and described in [Table 7-75](#).

Return to the [Register Summary Table](#).

Eye-Scan Run Control

**Figure 7-102. ESRUN Register**

| 7        | 6 | 5 | 4 | 3 | 2 | 1      | 0 |
|----------|---|---|---|---|---|--------|---|
| RESERVED |   |   |   |   |   | ESRUN  |   |
| R/W-00h  |   |   |   |   |   | R/W-0b |   |

**Table 7-75. ESRUN Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                                               |
|-----|----------|------|-------|-----------------------------------------------------------------------------------------------------------|
| 7-1 | RESERVED | R/W  | 00h   |                                                                                                           |
| 0   | ESRUN    | R/W  | 0b    | After setting up eye-scan, set ESRUN=1 to run the eye-scan test. See <a href="#">Eye Scan Procedure</a> . |

#### 7.5.3.42 ES\_CTRL Register (Offset = 01F1h) [reset = 00h]

ES\_CTRL is shown in [Figure 7-103](#) and described in [Table 7-76](#).

Return to the [Register Summary Table](#). Note: Only change this register while ESRUN=0.

Eye-Scan Control

**Figure 7-103. ES\_CTRL Register**

| 7        | 6 | 5       | 4 | 3      | 2 | 1 | 0 |
|----------|---|---------|---|--------|---|---|---|
| RESERVED |   | ESLEN   |   | ES     |   |   |   |
| R/W-00b  |   | R/W-00b |   | R/W-0h |   |   |   |

**Table 7-76. ES\_CTRL Register Field Descriptions**

| Bit | Field   | Type | Reset | Description |
|-----|---------|------|-------|-------------|
| 7-6 | ES_CTRL | R/W  | 00b   |             |

**Table 7-76. ES\_CTRL Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5-4 | ESLEN | R/W  | 00b   | Specify the length of the eye-scan test. Larger values will give more consistent results, but will take longer.<br><b>ESLEN : Number of Samples Analyzed</b><br>0 : 127<br>1 : 1032<br>2 : 8191<br>3 : 65535<br>Note: Many eye-scan modes only analyze zeros (or ones). Since they don't analyze every sample, those modes will take longer to complete compared to a mode that analyzes all samples.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 3-0 | ES    | R/W  | 0h    | Specify the eye-scan mode. Applies to all lanes.<br>ES : Eye-Scan Mode<br>0 : Eye-scan disabled (default)<br>1 : Compare. Counts mismatches between the normal sampler and the eye-scan sampler. Analyzes zeros and ones.<br>2 : Compare zeros. Same as ES=1, but only analyzes zeros.<br>3 : Compare ones. Same as ES=1, but only analyzes ones.<br>4 : Count ones. Increments ECOUNTn when the eye-scan sample is 1.<br>5-7 : RESERVED<br>8 : Average zero. Adjusts ESVO_Sn to the average voltage for a zero.<br>9 : Outer zero. Adjusts ESVO_Sn to the lowest voltage for a zero.<br>10 : Inner zero. Adjusts ESVO_Sn to the highest voltage for a zero.<br>11 : RESERVED<br>12 : Average one. Adjusts ESVO_Sn to the average voltage for a one.<br>13 : Outer one. Adjusts ESVO_Sn to the highest voltage for a one.<br>14 : Inner one. Adjusts ESVO_Sn to the lowest voltage for a one.<br>15 : RESERVED |

#### 7.5.3.43 ESPO Register (Offset = 01F2h) [reset = 00h]

ESPO is shown in [Figure 7-104](#) and described in [Table 7-77](#).

Return to the [Register Summary Table](#).

Eye-Scan Phase Offset

**Figure 7-104. ESPO Register**

|          |         |   |   |   |   |   |   |
|----------|---------|---|---|---|---|---|---|
| 7        | 6       | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | ESPO    |   |   |   |   |   |   |
| R/W-0b   | R/W-00h |   |   |   |   |   |   |

**Table 7-77. ESPO Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                                                                  |
|-----|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | RESERVED | R/W  | 0h    |                                                                                                                                                                                                                                                              |
| 6-0 | ESPO     | R/W  | 0b    | Eye-scan phase offset for all lanes. This adjusts the sampling instant of the eye-scan sampler compared to the normal sampler. This is a signed value from -64 to +63 and the step size is 1/32th of a UI.<br>Note: Only change this register while ESRUN=0. |

#### 7.5.3.44 ESVO Register (Offset = 01F3h) [reset = 00h]

ESVO is shown in [Figure 7-105](#) and described in [Table 7-78](#).

Return to the [Register Summary Table](#).

Eye-Scan Voltage Offset

**Figure 7-105. ESVO Register**

| 7        | 6 | 5 | 4       | 3 | 2 | 1 | 0 |
|----------|---|---|---------|---|---|---|---|
| RESERVED |   |   | ESVO    |   |   |   |   |
| R/W-00b  |   |   | R/W-00h |   |   |   |   |

**Table 7-78. ESVO Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                        |
|-----|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-6 | RESERVED | R/W  | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 5-0 | ESVO     | R/W  | 00h   | Eye-scan voltage offset for all lanes. This adjusts the voltage threshold of the eye-scan sampler. This is a signed value from -32 to +31. The step size is about 10mV (giving an adjustment range of about -320mV to +310mV). This field is ignored for eye-scan modes that adjust the voltage offset automatically and return a result on ESVO_S[n].<br>Note: This register should only be changed when ESRUN=0. |

#### 7.5.3.45 ES\_BIT\_SELECT Register (Offset = 01F4h) [reset = 00h]

ES\_BIT\_SELECT is shown in [Figure 7-106](#) and described in [Table 7-79](#).

Return to the [Register Summary Table](#).

Eye-Scan Bit Select.

**Figure 7-106. ES\_BIT\_SELECT Register**

| 7        | 6 | 5 | 4             | 3 | 2 | 1 | 0 |
|----------|---|---|---------------|---|---|---|---|
| RESERVED |   |   | ES_BIT_SELECT |   |   |   |   |
| R/W-000b |   |   | R/W-00h       |   |   |   |   |

**Table 7-79. ES\_BIT\_SELECT Register Field Descriptions**

| Bit | Field         | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|-----|---------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-5 | RESERVED      | R/W  | 000b  |                                                                                                                                                                                                                                                                                                                                                                                                    |
| 4-0 | ES_BIT_SELECT | R/W  | 00h   | Eye-scan only runs on every 20th bit. This field specifies which bit position the eye-scan runs on (valid range is 0 to 19). Eye-scans may be run with all possible values of ES_BIT_SELECT and the results combined. Alternatively, results can be kept separate to see the effects of any duty cycle distortion / repetitive jitter.<br>Note: This register should only be changed when ESRUN=0. |

#### 7.5.3.46 ECOUNT\_CLR Register (Offset = 01F5h) [reset = 00h]

ECOUNT\_CLR is shown in [Figure 7-107](#) and described in [Table 7-80](#).

Return to the [Register Summary Table](#).

SerDes Error Counter Clear

**Figure 7-107. ECOUNT\_CLR Register**

|          |   |   |   |   |   |   |            |
|----------|---|---|---|---|---|---|------------|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0          |
| RESERVED |   |   |   |   |   |   | ECOUNT_CLR |
| R/W-00h  |   |   |   |   |   |   | R/W-0b     |

**Table 7-80. ECOUNT\_CLR Register Field Descriptions**

| Bit | Field      | Type | Reset | Description                                                    |
|-----|------------|------|-------|----------------------------------------------------------------|
| 7-1 | RESERVED   | R/W  | 00h   |                                                                |
| 0   | ECOUNT_CLR | R/W  | 0b    | Program this to a 1 and then to 0 to clear the ECOUNT counters |

#### 7.5.3.47 ESDONE Register (Offset = 01F6h) [reset = NA, read-only]

ESDONE is shown in [Figure 7-108](#) and described in [Table 7-81](#).

Return to the [Register Summary Table](#).

Eye-Scan Process Done

#### Note

Only lanes 6 and 14 are connected on DDS devices. All other lanes are disconnected.

**Figure 7-108. ESDONE Register**

|              |   |   |   |   |   |   |   |
|--------------|---|---|---|---|---|---|---|
| 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ESDONE[15:8] |   |   |   |   |   |   |   |
| R            |   |   |   |   |   |   |   |
| ESDONE[7:0]  |   |   |   |   |   |   |   |
| R            |   |   |   |   |   |   |   |

**Table 7-81. ESDONE Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                                                                                                                                               |
|------|--------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15-0 | ESDONE[15:0] | R    | NA    | ESDONE[n] returns a 1 to indicate that the eye-scan procedure is completed on physical lane <i>n</i> . You must make sure that ESDONE[n] returns 1 before reading ESVO_S[n] or ECOUNT[n]. |

#### 7.5.3.48 ESVO\_S[15:0] Register (Offset = 0200h) [reset = NA, read-only]

ESVO\_S[15:0] is shown in [Figure 7-109](#) and described in [Table 7-82](#).

Return to the [Register Summary Table](#).

Eye-Scan Voltage Offset for SerDes lane *n*, *n* = 0 - 15. ESVO\_S[0] is at the lowest address.

#### Note

Only lanes 6 and 14 are connected on DDS devices. All other lanes are disconnected.

**Figure 7-109. ESVO\_S[15:0] Register**

|          |   |           |   |   |   |   |   |
|----------|---|-----------|---|---|---|---|---|
| 7        | 6 | 5         | 4 | 3 | 2 | 1 | 0 |
| RESERVED |   | ESVO_S[n] |   |   |   |   |   |
| R        |   | R         |   |   |   |   |   |

**Table 7-82. ESVO\_S[15:0] Register Field Descriptions**

| Bit | Field    | Type | Reset | Description |
|-----|----------|------|-------|-------------|
| 7-6 | RESERVED | R    | NA    |             |

**Table 7-82. ESVO\_S[15:0] Register Field Descriptions (continued)**

| Bit | Field     | Type | Reset | Description                                                                                                                                                                                   |
|-----|-----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5-0 | ESVO_S[n] | R    | NA    | Returns the voltage offset result from the eye-scan on physical lane <i>n</i> . Applies to eye-scan modes that compute the voltage offset automatically. Only valid when ESDONE[n] returns 1. |

#### 7.5.3.49 ESCOUNT[15:0] Register (Offset = 0210h) [reset = NA, read-only]

ESCOUNT[15:0] is shown in [Figure 7-110](#) and described in [Table 7-83](#).

Return to the [Register Summary Table](#).

Eye-Scan Voltage Offset for SerDes lane *n*, *n* = 0 - 15. ESCOUNT[0] is at the lowest address.

##### Note

Only lanes 6 and 14 are connected on DDS devices. All other lanes are disconnected.

**Figure 7-110. ESCOUNT[15:0] Register**

|                  |   |   |   |   |   |   |   |
|------------------|---|---|---|---|---|---|---|
| 7                | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ESCOUNT[15:8][n] |   |   |   |   |   |   |   |
| R                |   |   |   |   |   |   |   |
| ESCOUNT[7:0][n]  |   |   |   |   |   |   |   |
| R                |   |   |   |   |   |   |   |

**Table 7-83. ESCOUNT[15:0] Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                   |
|------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| 15-0 | ESCOUNT[n] | R    | NA    | Returns the mismatch count for physical lane <i>n</i> (applies to eye-scan modes that count mismatches). Only valid when ESDONE[n] returns 1. |

#### 7.5.3.50 LOS\_TH Register (Offset = 0234h) [reset = 08h]

LOS\_TH is shown in [Figure 7-111](#) and described in [Table 7-84](#).

Return to the [Register Summary Table](#).

SerDes Loss-of-signal Theshold

**Figure 7-111. LOS\_TH Register**

|          |   |   |   |        |   |   |   |
|----------|---|---|---|--------|---|---|---|
| 7        | 6 | 5 | 4 | 3      | 2 | 1 | 0 |
| RESERVED |   |   |   | LOS_TH |   |   |   |
| R/W-0h   |   |   |   | R/W-0h |   |   |   |

**Table 7-84. LOS\_TH Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                          |
|-----|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-4 | RESERVED | R/W  | 0h    |                                                                                                                                                                                      |
| 3-0 | LOS_TH   | R/W  | 0h    | Specifies the threshold for the loss-of-signal detector. Applies when LOS_EN=1. Affects all lanes.<br>LOS_TH : Approximate Threshold (mV)<br>0, 1 : RESERVED<br>2 - 15 : 15*(LOS_TH) |

### 7.5.3.51 EQCNTSZ Register (Offset = 0235h) [reset = 00h]

EQCNTSZ is shown in [Figure 7-112](#) and described in [Table 7-85](#).

Return to the [Register Summary Table](#).

SerDes Equalizer Counter Size

**Figure 7-112. EQCNTSZ Register**

|        |   |   |   |        |   |   |   |
|--------|---|---|---|--------|---|---|---|
| 7      | 6 | 5 | 4 | 3      | 2 | 1 | 0 |
| R/W-0h |   |   |   | R/W-0h |   |   |   |

**Table 7-85. EQCNTSZ Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-----|----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-4 | RESERVED | R/W  | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 3-0 | EQCNTSZ  | R/W  | 0h    | Equalizer counter size: Adjusts how many votes must be accumulated to cause the adaptive equalizer gain to change. Affects all lanes. This is for debug purposes only and the user should generally not need to change this setting.<br>EQCNTSZ : Equalizer Vote Counter Size (votes required to adjust gain)<br>0 : (default) 511<br>1 : RESERVED<br>2 : 1<br>3 : 3<br>4 : 7<br>5 : 15<br>6 : 31<br>7 : 63<br>8 : 127<br>9 : 255<br>10-15 : RESERVED |

### 7.5.3.52 CDRLOCK Register (Offset = 0238h) [reset = 00h]

CDRLOCK is shown in [Figure 7-113](#) and described in [Table 7-86](#).

Return to the [Register Summary Table](#).

SerDes CDR Lock/Freeze.

**Figure 7-113. CDRLOCK Register**

|          |   |   |   |   |   |         |   |
|----------|---|---|---|---|---|---------|---|
| 7        | 6 | 5 | 4 | 3 | 2 | 1       | 0 |
| RESERVED |   |   |   |   |   | CDRLOCK |   |
| R/W-00h  |   |   |   |   |   | R/W-0b  |   |

**Table 7-86. CDRLOCK Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                                                                                              |
|-----|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-1 | RESERVED | R/W  | 00h   |                                                                                                                                                          |
| 0   | CDRLOCK  | R/W  | 0b    | When set, the CDR is frozen and no longer tracks. When the CDR is operating in first-order mode, set CDRLOCK to freeze the CDRPHASE value to inspect it. |

### 7.5.3.53 CDRPHASE Register (Offset = 0239h) [reset = NA, read-only]

CDRPHASE is shown in [Figure 7-114](#) and described in [Table 7-87](#).

Return to the [Register Summary Table](#).

SerDes CDR Phase Status

**Figure 7-114. CDRPHASE Register**

|          |   |   |   |   |   |   |   |
|----------|---|---|---|---|---|---|---|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CDRPHASE |   |   |   |   |   |   |   |
| R        |   |   |   |   |   |   |   |

**Table 7-87. CDRPHASE Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                |
|-----|----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-0 | CDRPHASE | R    |       | Returns the current CDR phase value for the lane specified by RXDLANE. It is recommended to set CDRLOCK=1 before reading this register. The format is gray-coded. Refer to CDRPHASE Status for the coding. |

### 7.5.3.54 PLL\_STATUS Register (Offset = 0250h) [reset = NA, read only]

PLL\_STATUS is shown in [Figure 7-67](#) and described in [Table 7-39](#).

Return to the [Register Summary Table](#).

SerDes PLL Status

**Figure 7-115. PLL\_STATUS Register**

|              |   |   |   |               |   |   |   |
|--------------|---|---|---|---------------|---|---|---|
| 7            | 6 | 5 | 4 | 3             | 2 | 1 | 0 |
| PLL_LOCK_STS |   |   |   | PLL_LOCK_LOST |   |   |   |
| R-0h         |   |   |   | R/W1C-0h      |   |   |   |

**Table 7-88. PLL\_STATUS Register Field Descriptions**

| Bit | Field         | Type  | Reset | Description                                                                                                                                                                                                                                                                                                                                                                |
|-----|---------------|-------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-4 | PLL_LOCK_STS  | R     | 0h    | This field returns the LOCK signal from all four SerDes macros (3:0). This field can be used for functional (fault) testing of the PLL lock detectors.                                                                                                                                                                                                                     |
| 3-0 | PLL_LOCK_LOST | R/W1C | 0h    | PLL_LOCK_LOST[n] is set whenever the LOCK signal from a SerDes PLL is low.<br>bit 0: lanes 0 - 3<br>bit 1: lanes 4 - 7<br>bit 2: lanes 8 - 11<br>bit 3: lanes 12 - 15<br>This bit is sticky (remains set even if the PLL acquires lock). Write 1 to clear a bit. These bits are for debug purposes and allow the SPI to monitor if any SerDes PLL loses lock even briefly. |

### 7.5.3.55 JESD\_RST Register (Offset = 0253h) [reset = 0x00]

JESD\_RST is shown in [Figure 7-116](#) and described in [Table 7-89](#).

Return to the [Register Summary Table](#).

JESD Reset

**Figure 7-116. JESD\_RST Register**

|   |   |   |   |   |   |   |
|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|

**Figure 7-116. JESD\_RST Register (continued)**

|          |          |
|----------|----------|
| RESERVED | JESD_RST |
| R/W-00h  | R/W-0h   |

**Table 7-89. JESD\_RST Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-----|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-1 | RESERVED | R/W  | 00h   | RESERVED                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 0   | JESD_RST | R/W  | 0b    | When set, this bit holds the digital portion of the JESD circuitry in reset but does not affect the physical lane. It may be necessary to set this bit prior to setting JESD_EN = 1 and then clear this bit at a later time to start processing the JESD data. This allows the supply to settle from the large change in power that occurs when starting the PHY and JESD clocks. This is especially important if the user plans to use the LANE_ARR values, since these values are captured only the first time the elastic buffer attempts to release. |

#### 7.5.3.56 EXTREF\_EN Register (Offset = 02B0h) [reset = 00h]

EXTREF\_EN is shown in [Figure 7-117](#) and described in [Table 7-90](#).

Return to the [Register Summary Table](#).

Enable External Reference

**Figure 7-117. EXTREF\_EN Register**

|          |   |   |   |   |   |   |           |
|----------|---|---|---|---|---|---|-----------|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0         |
| RESERVED |   |   |   |   |   |   | EXTREF_EN |
| R/W-00h  |   |   |   |   |   |   | R/W-0b    |

**Table 7-90. EXTREF\_EN Register Field Descriptions**

| Bit | Field     | Type | Reset | Description                                                                          |
|-----|-----------|------|-------|--------------------------------------------------------------------------------------|
| 7-1 | RESERVED  | R/W  | 00h   |                                                                                      |
| 0   | EXTREF_EN | R/W  | 0b    | Setting this bit enable the use of an external reference voltage on the EXTREF ball. |

#### CUR\_2X\_EN Register (Offset = 02B1h) [reset = 00h]

CUR\_2X\_EN is shown in [Figure 7-118](#) and described in [Table 7-91](#).

Return to the [Register Summary Table](#).

DAC Current Doubler Enable

**Figure 7-118. CUR\_2X\_EN Register**

|          |   |   |   |   |   |   |           |
|----------|---|---|---|---|---|---|-----------|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0         |
| RESERVED |   |   |   |   |   |   | CUR_2X_EN |
| R/W-00h  |   |   |   |   |   |   | R/W-0b    |

**Table 7-91. CUR\_2X\_EN Register Field Descriptions**

| Bit | Field     | Type | Reset | Description                                      |
|-----|-----------|------|-------|--------------------------------------------------|
| 7-1 | RESERVED  | R/W  | 00h   |                                                  |
| 0   | CUR_2X_EN | R/W  | 0b    | Setting this bit doubles the DAC output current. |

### 7.5.3.57 DAC\_OFS\_CHG\_BLK Register (Offset = 02CFh) [reset = 00h]

DAC\_OFS\_CHG\_BLK is shown in [Figure 7-119](#) and described in [Table 7-92](#).

Return to the [Register Summary Table](#).

DAC Offset Adjustment Change Block

**Figure 7-119. DAC\_OFS\_CHG\_BLK Register**

| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0               |
|----------|---|---|---|---|---|---|-----------------|
| RESERVED |   |   |   |   |   |   | DAC_OFS_CHG_BLK |
| R/W-00h  |   |   |   |   |   |   | R/W-0b          |

**Table 7-92. DAC\_OFS\_CHG\_BLK Register Field Descriptions**

| Bit | Field           | Type | Reset | Description                                                                                                                                                                                                                                     |
|-----|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-1 |                 | R/W  | 00h   |                                                                                                                                                                                                                                                 |
| 0   | DAC_OFS_CHG_BLK | R/W  | 0b    | When set, changes to DAC_OFS[n] are not propagated to the high-speed clocks and both DACs continue to use their current value. When this is changed from 1 to 0 the new DAC_OFS[n] values will be applied to both DACs in the same clock cycle. |

### 7.5.3.58 DP\_EN Register (Offset = 02E0h) [reset = 00h]

DP\_EN is shown in [Figure 7-120](#) and described in [Table 7-93](#).

Return to the [Register Summary Table](#).

Datapath Enable.

**Figure 7-120. DP\_EN Register**

| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0      |
|----------|---|---|---|---|---|---|--------|
| RESERVED |   |   |   |   |   |   | DP_EN  |
| R/W-00h  |   |   |   |   |   |   | R/W-0b |

**Table 7-93. DP\_EN Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                                                                      |
|-----|----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-1 | RESERVED | R/W  | 00h   |                                                                                                                                                                                                                                                                  |
| 0   | DP_EN    | R/W  | 0b    | Setting this bit enables datapath operation. When cleared, the datapath is held in reset. This bit should be set after the chip is configured for proper operation.<br>Note: This register should only be changed from 0 to 1 when <a href="#">FUSE_DONE=1</a> . |

### 7.5.3.59 DUC\_L Register (Offset = 02E1h) [reset = 00h]

DUC\_L is shown in [Figure 7-121](#) and described in [Table 7-94](#).

Return to the [Register Summary Table](#).

DUC Interpolation Factor.

**Figure 7-121. DUC\_L Register**

| 7        | 6 | 5 | 4 | 3      | 2 | 1 | 0 |
|----------|---|---|---|--------|---|---|---|
| RESERVED |   |   |   | DUC_L  |   |   |   |
| R/W-0h   |   |   |   | R/W-0h |   |   |   |

**Table 7-94. DUC\_L Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                         |
|-----|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-4 | RESERVED | R/W  | 0h    |                                                                                                                                                                                                                                                                                                     |
| 3-0 | DUC_L    | R/W  | 0h    | <p>DUC Interpolation Factor</p> <p>0: 1x<br/>1: 2x<br/>2: 3x<br/>3: 4x<br/>4: 6x<br/>5: 8x<br/>6: 12x<br/>7: 16x<br/>8: 24x<br/>9: 32x<br/>10: 48x<br/>11: 64x<br/>12: 96x<br/>13: 128x<br/>14: 192x<br/>15: 256x</p> <p>Note: This register should only be changed when JESD_EN=0 and DP_EN=0.</p> |

#### 7.5.3.60 DUC\_GAIN Register (Offset = 02E2h) [reset = 00h]

DUC\_GAIN is shown in [Figure 7-122](#) and described in [Table 7-95](#).

Return to the [Register Summary Table](#).

**Figure 7-122. DUC\_GAIN Register**

|           |   |           |   |           |   |           |   |
|-----------|---|-----------|---|-----------|---|-----------|---|
| 7         | 6 | 5         | 4 | 3         | 2 | 1         | 0 |
| DUC_GAIN3 |   | DUC_GAIN2 |   | DUC_GAIN1 |   | DUC_GAIN0 |   |
| R/W-00b   |   | R/W-00b   |   | R/W-00b   |   | R/W-00b   |   |

**Table 7-95. DUC\_GAIN Register Field Descriptions**

| Bit | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-----|-----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-6 | DUC_GAIN3 | R/W  | 00b   | <p>DUC_GAIN<sub>n</sub> adjusts the gain of DUC<sub>n</sub> (in the channel bonder)</p> <p>0: 0dB<br/>1: -6dB<br/>2: -12dB<br/>3: RESERVED</p> <p>Note: When the DUCs are configured for complex output (DUC_FORMAT=1), DUC2 and DUC3 cannot be used. In that case, DUC_GAIN2 and DUC_GAIN3 adjust the gain of the imaginary outputs of DUC0 and DUC1 respectively.</p> <p>Note: This register should only be changed when DP_EN=0.</p> |
| 5-4 | DUC_GAIN2 | R/W  | 00b   |                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 3-2 | DUC_GAIN1 | R/W  | 00b   |                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 1-0 | DUC_GAIN0 | R/W  | 00b   |                                                                                                                                                                                                                                                                                                                                                                                                                                         |

#### 7.5.3.61 DUC\_FORMAT Register (Offset = 02E3h) [reset = 00h]

DUC\_FORMAT is shown in [Figure 7-123](#) and described in [Table 7-96](#).

Return to the [Register Summary Table](#).

## DUC Output Format

**Figure 7-123. DUC\_FORMAT Register**

| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0          |
|----------|---|---|---|---|---|---|------------|
| RESERVED |   |   |   |   |   |   | DUC_FORMAT |
| R/W-00h  |   |   |   |   |   |   | R/W-0b     |

**Table 7-96. DUC\_FORMAT Register Field Descriptions**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                                                         |
|-----|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-1 | RESERVED   | R/W  | 00h   |                                                                                                                                                                                                                                                                     |
| 0   | DUC_FORMAT | R/W  | 0b    | 0: DUC outputs are real (DUC mixer converts complex to real by discarding the imaginary part). Up to 4 DUCs can be enabled.<br>1: DUC outputs are complex. Up to 2 DUCs can be enabled (DUC0 and DUC1).<br>Note: This register should only be changed when DP_EN=0. |

### 7.5.3.62 DAC\_SRC Register (Offset = 02E4h) [reset = 00h]

DAC\_SRC is shown in [Figure 7-124](#) and described in [Table 7-97](#).

Return to the [Register Summary Table](#).

#### DAC Source

**Figure 7-124. DAC\_SRC Register**

| 7        | 6 | 5 | 4 | 3        | 2 | 1 | 0 |
|----------|---|---|---|----------|---|---|---|
| DAC_SRC1 |   |   |   | DAC_SRC0 |   |   |   |
| R/W-0h   |   |   |   | R/W-0h   |   |   |   |

**Table 7-97. DAC\_SRC Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-----|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-4 | DAC_SRC1 | R/W  | 0h    | When the DUCs are disabled ( $LT \leq 1$ ), DAC_SRCn selects which input stream is sent to DACn. When the DUCs are enabled ( $LT \geq 2$ ), DAC_SRCn controls which DUC outputs are routed (summed) to DACn (and the meaning of the bits depends on DUC_FORMAT). Signals Routed to DACn when DAC_SRCn[m] is set:<br>LT=0.5 or 1 (DUCs disabled)<br>DAC_SRCn[0]: Input Stream 0 (I)<br>DAC_SRCn[1]: Input Stream 1 (Q)<br>DAC_SRCn[2]: n/a<br>DAC_SRCn[3]: n/a<br>LT is 2 or higher (DUCs enabled) Register Bit<br>DAC_SRCn[x] : DUC_FORMAT=0 (real) : DUC_FORMAT=1 (complex)<br>DAC_SRCn[0] : DUC0 (real) : DUC0 (real)<br>DAC_SRCn[1] : DUC1 (real) : DUC1 (real)<br>DAC_SRCn[2] : DUC2 (real) : DUC0 (imag)<br>DAC_SRCn[3] : DUC3 (real) : DUC1 (imag)<br>If more than one signal is routed to the same DAC, the signals are summed together. Use DUC_GAIN to avoid saturation in this case. While it is possible to sum a real output with an imaginary output, no practical application requires that, so it is not tested or supported. When $LT=0.5$ or $1$ , no summing is supported. Only DAC_SRCn[0] or DAC_SRCn[1] should be set<br>Note: This register should only be changed when DP_EN=0. |
| 3-0 | DAC_SRC0 | R/W  | 0b    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |

### 7.5.3.63 MXMODE Register (Offset = 02E8h) [reset = 00h]

MXMODE is shown in [Figure 7-125](#) and described in [Table 7-98](#).

Return to the [Register Summary Table](#).

DAC Output Mode. Note: This register should only be changed when DP\_EN=0.

**Figure 7-125. MXMODE Register**

| 7        | 6        | 5 | 4 | 3        | 2        | 1 | 0 |
|----------|----------|---|---|----------|----------|---|---|
| RESERVED | MXMODE1  |   |   | RESERVED | MXMODE0  |   |   |
| R/W-0b   | R/W-000b |   |   | R/W-0b   | R/W-000b |   |   |

**Table 7-98. MXMODE Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-----|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | RESERVED | R/W  | 0b    |                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 6-4 | MXMODE1  | R/W  | 000b  | Specify the DAC pulse format for DACB.<br>0: Normal mode (non-return-to-zero or NRZ) (sinc nulls at $n \cdot FS$ )<br>1: RF Mode (return to inverse or RTI) (sinc nulls at DC and $2n \cdot FS$ )<br>2: Return-to-Zero (RTZ) (sinc nulls at $2n \cdot FS$ )<br>3: DES2X – Samples provided by the DES interpolator (low-pass mode)<br>4: DES2XH – Samples provided by the DES interpolator (high-pass mode)<br>6: Disabled – DACA is disabled<br>7: RESERVED |
| 3   | RESERVED | R/W  | 0b    |                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

**Table 7-98. MXMODE Register Field Descriptions (continued)**

| Bit | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-----|---------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2-0 | MXMODE0 | R/W  | 0b    | Specify the DAC pulse format for DACA.<br>0: Normal mode (non-return-to-zero or NRZ) (sinc nulls at n*FS)<br>1: RF Mode (return to inverse or RTI) (sinc nulls at DC and 2n*FS)<br>2: Return-to-Zero (RTZ) (sinc nulls at 2n*FS)<br>3: DES2X – Samples provided by the DES interpolator (low-pass mode)<br>4: DES2XH – Samples provided by the DES interpolator (high-pass mode)<br>6: Disabled – DACA is disabled<br>7: RESERVED |

#### 7.5.3.64 TRUNC\_HLSB Register (Offset = 02EAh) [reset = 00h]

TRUNC\_HLSB is shown in [Figure 7-126](#) and described in [Table 7-99](#).

Return to the [Register Summary Table](#).

Truncation Half LSB Offset

**Figure 7-126. TRUNC\_HLSB Register**

|          |   |   |   |   |   |   |            |
|----------|---|---|---|---|---|---|------------|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0          |
| RESERVED |   |   |   |   |   |   | TRUNC_HLSB |
| R/W-00h  |   |   |   |   |   |   | R/W-0b     |

**Table 7-99. TRUNC\_HLSB Register Field Descriptions**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                |
|-----|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-1 |            | R/W  | 0h    |                                                                                                                                                                                                                                                                            |
| 0   | TRUNC_HLSB | R/W  | 0b    | adds ½ LSB offset for < 16-bit resolution modes or devices. For a mode or device with < 16-bit output resolution, setting this bit adds a 1/2 LSB offset to reduce the average offset introduced by truncation.<br>Note: This register should only be changed when DP_EN=0 |

#### 7.5.3.65 TX\_EN\_SEL Register (Offset = 02F8h) [reset = 03h]

TX\_EN\_SEL is shown in [Figure 7-127](#) and described in [Table 7-100](#).

Return to the [Register Summary Table](#).

Transmitter Enable Control Selection.

**Figure 7-127. TX\_EN\_SEL Register**

|          |   |   |   |                      |            |            |            |
|----------|---|---|---|----------------------|------------|------------|------------|
| 7        | 6 | 5 | 4 | 3                    | 2          | 1          | 0          |
| RESERVED |   |   |   | QUIET_TX_DIS<br>ABLE | FAST_TX_EN | USE_TX_EN1 | USE_TX_EN0 |
| R/W-0h   |   |   |   | R/W-0b               | R/W-0b     | R/W-1b     | R/W-1b     |

**Table 7-100. TX\_EN\_SEL Register Field Descriptions**

| Bit | Field    | Type | Reset | Description |
|-----|----------|------|-------|-------------|
| 7-4 | RESERVED | R/W  | 0h    |             |

**Table 7-100. TX\_EN\_SEL Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-----|------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3   | QUIET_TX_DISABLE | R/W  | 0b    | 0: Transmission is disabled after DEM and dither by sending a static aging safe code. For some configurations and frequencies, the outputs will have higher noise than a static mid-scale code would normally have. However, this mode has the lowest latency from transmit enable to DAC output.<br>1: When transmission is disabled, the input to DEM and dither is muted to minimize the output noise. This increases the latency from transmit enable to DAC output by 56 DAC clocks<br>Note: This bit may only be set when FAST_TX_EN=1. |
| 2   | FAST_TX_EN       | R/W  | 0b    | 0: When the transmit enables are both low, JESD and datapath clocks are shutdown to save power. When transmission is re-enabled the outputs remain muted until valid data is available at the output.<br>1: No power saving is performed and transmit enables can be used independently. Latency from transmit enable to DAC outputs is reduced in this mode.                                                                                                                                                                                 |
| 1   | USE_TX_EN1       | R/W  | 1b    | 0: DACB is controlled by the TXEN1 ball. In this mode, TX_EN1 register is ignored.<br>1: DACB is controlled by the <a href="#">TX_EN1</a> register. In this mode the TXEN1 ball input does not affect the transmit enable for DACB.<br><b>Note: USE_TX_EN1 and USE_TX_EN0 should be programmed to the same value (individual channel control is not supported).</b>                                                                                                                                                                           |
| 0   | USE_TX_EN0       | R/W  | 1b    | 0: DACA is controlled by the TXEN0 ball. In this mode, TX_EN0 register is ignored.<br>1: DACA is controlled by the <a href="#">TX_EN0</a> register. In this mode the TXEN0 ball input does not affect the transmit enable for DACA.<br><b>Note: USE_TX_EN1 and USE_TX_EN0 should be programmed to the same value (individual channel control is not supported).</b>                                                                                                                                                                           |

### 7.5.3.66 TX\_EN Register (Offset = 02F9h) [reset = 03h]

TX\_EN is shown in [Figure 7-128](#) and described in [Table 7-101](#).

Return to the [Register Summary Table](#).

Transmitter Enable Control

**Figure 7-128. TX\_EN Register**

| 7       | 6 | 5 | 4 | 3 | 2 | 1      | 0      |
|---------|---|---|---|---|---|--------|--------|
|         |   |   |   |   |   | TX_EN1 | TX_EN0 |
| R/W-00h |   |   |   |   |   | R/W-1b | R/W-1b |

**Table 7-101. TX\_EN Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                  |
|-----|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-2 | RESERVED | R/W  | 00h   |                                                                                                                                                                                              |
| 1   | TX_EN1   | R/W  | 1b    | When USE_TX_EN1 = 1, this bit controls the transmit enable for DACB.<br><b>Note: TX_EN1 and TX_EN0 should be programmed to the same value (individual channel control is not supported).</b> |

**Table 7-101. TX\_EN Register Field Descriptions (continued)**

| Bit | Field  | Type | Reset | Description                                                                                                                                                                                 |
|-----|--------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | TX_EN0 | R/W  | 1b    | When USE_TX_EN0 = 1, this bit controls the transmit enable for DACA<br><i>Note: TX_EN1 and TX_EN0 should be programmed to the same value (individual channel control is not supported).</i> |

**7.5.3.67 NCO\_CTRL Register (Offset = 0300h) [reset = 00h]**

NCO\_CTRL is shown in [Figure 7-129](#) and described in [Table 7-102](#).

Return to the [Register Summary Table](#). Note: This register should only be changed when DP\_EN=0.

NCO Enable

**Figure 7-129. NCO\_CTRL Register**

|        |          |   |   |        |        |        |   |
|--------|----------|---|---|--------|--------|--------|---|
| 7      | 6        | 5 | 4 | 3      | 2      | 1      | 0 |
| FR_EN  | RESERVED |   |   | NCO_SC | DDS_EN | NCO_EN |   |
| R/W-0b | R/W-0h   |   |   | R/W-0b | R/W-0b | R/W-0b |   |

**Table 7-102. NCO\_CTRL Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                                                                      |
|-----|----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | FR_EN    | R/W  | 0b    | When set, the Fast Reconfiguration (FR) interface is enabled and NCO frequency, phase, dither, and accumulator reset is controlled by the FR registers rather than the SPI registers.                                                                            |
| 6-3 | RESERVED | R/W  | 0h    |                                                                                                                                                                                                                                                                  |
| 2   | NCO_SC   | R/W  | 0b    | Self-Coherent NCO Mode: When this bit is set, all NCOs use the reference counter from the NCO in DDS/DUC channel 0. This is typically used along with the <a href="#">NCO_SS</a> register. This only impacts phase-coherent mode ( <a href="#">NCO_CONT</a> =0). |
| 1   | DDS_EN   | R/W  | 0b    | When set, all DUCs are configured for DDS operation once DP_EN is set. See DDS Operation in <a href="#">Section 7.4.1</a> for details.                                                                                                                           |
| 0   | NCO_EN   | R/W  | 0b    | When set, DUC samples are mixed with the NCO.                                                                                                                                                                                                                    |

**7.5.3.68 NCO\_CONT Register (Offset = 0301h) [reset = 00h]**

NCO\_CONT is shown in [Figure 7-130](#) and described in [Table 7-103](#).

Return to the [Register Summary Table](#).

NCO Phase Continuous Mode

**Figure 7-130. NCO\_CONT Register**

|          |   |   |   |          |   |   |   |
|----------|---|---|---|----------|---|---|---|
| 7        | 6 | 5 | 4 | 3        | 2 | 1 | 0 |
| RESERVED |   |   |   | NCO_CONT |   |   |   |
| R/W-0h   |   |   |   | R/W-0h   |   |   |   |

**Table 7-103. NCO\_CONT Register Field Descriptions**

| Bit | Field    | Type | Reset | Description |
|-----|----------|------|-------|-------------|
| 7-4 | RESERVED | R/W  | 0h    |             |

**Table 7-103. NCO\_CONT Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-----|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3-0 | NCO_CONT | R/W  | 0h    | For each bit NCO_CONT[n], if set, NCO <sub>n</sub> operates in phase-continuous mode. This means that frequency changes occur without seeding the phase accumulator. If the bit is clear, NCO <sub>n</sub> operates in phase-coherent mode. During frequency changes, the phase accumulator is seeded from a main counter. This means that if changing from frequency A to B and then back to A, the phase returns to what it would have been if the change never occurred. Note: This register should only be changed when DP_EN=0. |

### 7.5.3.69 NCO\_SYNC Register (Offset = 0302h) [reset = 00h]

NCO\_SYNC is shown in [Figure 7-131](#) and described in [Table 7-104](#).

Return to the [Register Summary Table](#).

NCO Synchronization Configuration

**Figure 7-131. NCO\_SYNC Register**

|          |   |   |   |   |   |              |   |
|----------|---|---|---|---|---|--------------|---|
| 7        | 6 | 5 | 4 | 3 | 2 | 1            | 0 |
| RESERVED |   |   |   |   |   | NCO_SYNC_SRC |   |
| R/W-00h  |   |   |   |   |   | R/W-00b      |   |

**Table 7-104. NCO\_SYNC Register Field Descriptions**

| Bit | Field    | Type | Reset | Description |
|-----|----------|------|-------|-------------|
| 7-2 | RESERVED | R/W  | 00h   |             |

**Table 7-104. NCO\_SYNC Register Field Descriptions (continued)**

| Bit | Field        | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-----|--------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1-0 | NCO_SYNC_SRC | R/W  | 00b   | <p>If FR_EN=0:</p> <p>This register determines how NCO synchronization events will be triggered. This includes both accumulator resets specified by NCO_AR and the application of changes to NCO_DITH_EN, FREQ, and PHASE.</p> <p>0: Setting SPI_SYNC will immediately perform specified events. (All will occur in the same clock cycle.)</p> <p>1: Setting SPI_SYNC will cause the specified events to occur on the next SYSREF rising edge.</p> <p>2: While SPI_SYNC is high, the specified events will occur on every SYSREF rising edge.</p> <p>3: While SPI_SYNC is high, the LSb of the "I" input to DUC0 will cause the specified events. To trigger the event, the LSb must be low for 4 or more consecutive samples and then high for 4 consecutive samples. The sync will occur coincident with the 4th high sample arriving at the DUC0 input.</p> <p>If FR_EN=1:</p> <p>This register determines how NCO synchronization events will be triggered. This includes both accumulator resets specified by FR_NCO_AR and the application of changes to FR_NCO_DITH_EN, FR_FREQ, FR_FREQS, and FR_PHASE.</p> <p>0: If FRS is set, the specified events is performed at the rising edge of FRCS. (All will occur in the same clock cycle.)</p> <p>1: Reserved</p> <p>2: RESERVED</p> <p>3: If FRS is set, the LSb of the "I" input to DUC0 will cause the specified events following the rising edge of FRCS. To trigger the event, the LSb must be low for 4 or more consecutive samples and then high for 4 consecutive samples. The sync will occur coincident with the 4th high sample arriving at the DUC0 input. While waiting for the LSb trigger, zero will be used for the LSb data. The LSb will immediately return to being used as data after the 4th consecutive high sample.</p> <p>Note: This register should only be changed when SPI_SYNC=0 and the FR interface is idle (FRCS=1).</p> |

### 7.5.3.70 NCO\_AR Register (Offset = 0303h) [reset = 0Fh]

NCO\_AR is shown in [Figure 7-132](#) and described in [Table 7-105](#).

Return to the [Register Summary Table](#).

NCO Accumulator Reset

**Figure 7-132. NCO\_AR Register**

|          |   |   |   |        |   |   |   |
|----------|---|---|---|--------|---|---|---|
| 7        | 6 | 5 | 4 | 3      | 2 | 1 | 0 |
| RESERVED |   |   |   | NCO_AR |   |   |   |
| R/W-0h   |   |   |   | R/W-0h |   |   |   |

**Table 7-105. NCO\_AR Register Field Descriptions**

| Bit | Field    | Type | Reset | Description |
|-----|----------|------|-------|-------------|
| 7-4 | RESERVED | R/W  | 0h    |             |

**Table 7-105. NCO\_AR Register Field Descriptions (continued)**

| Bit | Field  | Type | Reset | Description                                                                                                                                                                                           |
|-----|--------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3-0 | NCO_AR | R/W  | 0h    | For each bit NCO_AR[n], if set, the accumulator for NCO <sub>n</sub> will be reset on every sync event specified by <a href="#">NCO_SYNC_SRC</a> .<br>Note: This register has no effect when FR_EN=1. |

#### 7.5.3.71 SPI\_SYNC Register (Offset = 0304h) [reset = 00h]

SPI\_SYNC is shown in [Figure 7-133](#) and described in [Table 7-106](#).

Return to the [Register Summary Table](#).

SPI Sync Bit

**Figure 7-133. SPI\_SYNC Register**

|          |   |   |   |   |   |   |          |
|----------|---|---|---|---|---|---|----------|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0        |
| RESERVED |   |   |   |   |   |   | SPI_SYNC |
| R/W-00h  |   |   |   |   |   |   | R/W-0b   |

**Table 7-106. SPI\_SYNC Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                   |
|-----|----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-1 | RESERVED | R/W  | 00h   |                                                                                                                                                                                                                                                                                                                                                                               |
| 0   | SPI_SYNC | R/W  | 0b    | Writing '1' to this register when it is '0' will trigger synchronization events that are bound to this register (see <a href="#">NCO_SYNC_SRC</a> ). This register will return the last value written.<br>Note: Whether this register is edge or level sensitive depends on the setting for <a href="#">NCO_SYNC_SRC</a> .<br>Note: This register has no effect when FR_EN=1. |

#### NCO\_SS Register (Offset = 0305h) [reset = 00h]

NCO\_SS is shown in [Figure 7-134](#) and described in [Table 7-107](#).

Return to the [Register Summary Table](#).

NCO\_SS Bit

**Figure 7-134. NCO\_SS Register**

|          |   |   |   |   |   |   |        |
|----------|---|---|---|---|---|---|--------|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0      |
| RESERVED |   |   |   |   |   |   | NCO_SS |
| R/W-00h  |   |   |   |   |   |   | R/W-0b |

**Table 7-107. NCO\_SS Register Field Descriptions**

| Bit | Field    | Type | Reset | Description |
|-----|----------|------|-------|-------------|
| 7-1 | RESERVED | R/W  | 00h   |             |

**Table 7-107. NCO\_SS Register Field Descriptions (continued)**

| Bit | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-----|--------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | NCO_SS | R/W  | 0b    | <p>When this bit is set, all NCOs will continuously self-synchronize every 256 DAC clock cycles.</p> <p>NCO_SS can be changed while the NCOs are operating (DP_EN=1). To write a new FREQ, AMP, or PHASE value, clear NCO_SS first, and then set it again after the new values are written. All values go into effect simultaneously on all NCOs.</p> <p>The user should make sure that NCO_AR=0 whenever NCO_SS=1 (otherwise the NCO accumulators and/or reference counters keep getting reset).</p> <p>If the user also sets <a href="#">NCO_SC=1</a> and <a href="#">NCO_CONT=0</a>, then all four NCOs maintain coherency with each other under radiation, but there may be no coherence with an external component. Each NCO accumulator is continuously seeded from the reference counter in DUC/DDS channel 0. This feature can be used to generate coherent harmonic tones to cancel out harmonic distortion in the DAC.</p> |

**AMP[3:0] Register (Offset = 0318h) [reset = 0000h]**

AMP[3:0] is described in [Table 7-108](#). AMP[0] starts at address 0x0318, AMP[1] at address 0x031A, AMP[2] at address 0x031C and AMP[3] at address 0x031E.

Return to the [Register Summary Table](#).

**Table 7-108. AMP[3:0] Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|------|----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15-0 | AMP[3:0] | R/W  | 0000h | <p>Specifies the DDS amplitude for DDS channel n. 16-bit signed value. This register only applies to DDS Operation.</p> <p>Note: Changes to this register do not take effect until the next sync event specified by <a href="#">NCO_SYNC_SRC</a>.</p> <p>Note: This register should only be changed when DP_EN=0 or updates to the NCOs are scheduled to occur away from the change. (See <a href="#">NCO_SYNC</a>.)FREQ[0] Register (Offset = 0320h) [reset = 0000000000000000h]</p> |

FREQ[0] is described in [Table 7-109](#).

Return to the [Register Summary Table](#).

FREQ for NCO0 Accumulator.

**Table 7-109. FREQ[0] Register Field Descriptions**

| Bit  | Field   | Type | Reset                         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|------|---------|------|-------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 63-0 | FREQ[0] | R/W  | 0000<br>0000<br>0000<br>0000h | <p>The NCO frequency (<math>F_{NCO}</math>) is:</p> $F_{NCO} = \text{FREQ}[0] * 2^{-64} * F_{CLK}$ <p>where <math>F_{CLK}</math> is the sample frequency of the DAC. FREQ[0] is the integer value of this register. This register can be interpreted as signed or unsigned (both interpretations are valid).<br/>Use this equation to determine the value to program:<br/> <math display="block">\text{FREQ}[0] = 2^{64} * F_{NCO} / F_{CLK}</math> <p>Note: Changes to this register do not take effect until the next sync event specified by <a href="#">NCO_SYNC_SRC</a>.<br/> <p>Note: This register should only be changed when DP_EN=0 or updates to the NCOs are scheduled to occur away from the change. (See <a href="#">NCO_SYNC</a>.)<br/> <p>Note: This register has no effect when FR_EN=1.</p> </p></p></p> |

#### 7.5.3.73 FREQ[1] Register (Offset = 0328h) [reset = 0000000000000000h]

FREQ[1] is described in [Table 7-110](#).

Return to the [Register Summary Table](#).

FREQ for NCO1 Accumulator.

**Table 7-110. FREQ[1] Register Field Descriptions**

| Bit  | Field   | Type | Reset                         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|------|---------|------|-------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 63-0 | FREQ[1] | R/W  | 0000<br>0000<br>0000<br>0000h | <p>The NCO frequency (<math>F_{NCO}</math>) is:</p> $F_{NCO} = \text{FREQ}[1] * 2^{-64} * F_{CLK}$ <p>where <math>F_{CLK}</math> is the sample frequency of the DAC. FREQ[1] is the integer value of this register. This register can be interpreted as signed or unsigned (both interpretations are valid).<br/>Use this equation to determine the value to program:<br/> <math display="block">\text{FREQ}[1] = 2^{64} * F_{NCO} / F_{CLK}</math> <p>Note: Changes to this register do not take effect until the next sync event specified by <a href="#">NCO_SYNC_SRC</a>.<br/> <p>Note: This register should only be changed when DP_EN=0 or updates to the NCOs are scheduled to occur away from the change. (See <a href="#">NCO_SYNC</a>.)<br/> <p>Note: This register has no effect when FR_EN=1.</p> </p></p></p> |

#### 7.5.3.74 FREQ[2] Register (Offset = 0330h) [reset = 0000000000000000h]

FREQ[2] is described in [Table 7-111](#).

Return to the [Register Summary Table](#).

FREQ for NCO2 Accumulator.

**Table 7-111. FREQ[2] Register Field Descriptions**

| Bit  | Field   | Type | Reset                         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|------|---------|------|-------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 63-0 | FREQ[2] | R/W  | 0000<br>0000<br>0000<br>0000h | <p>The NCO frequency (<math>F_{NCO}</math>) is:</p> $F_{NCO} = \text{FREQ}[2] * 2^{-64} * F_{CLK}$ <p>where <math>F_{CLK}</math> is the sample frequency of the DAC. FREQ[2] is the integer value of this register. This register can be interpreted as signed or unsigned (both interpretations are valid).</p> <p>Use this equation to determine the value to program:</p> $\text{FREQ}[2] = 2^{64} * F_{NCO} / F_{CLK}$ <p>Note: Changes to this register do not take effect until the next sync event specified by <a href="#">NCO_SYNC_SRC</a>.</p> <p>Note: This register should only be changed when DP_EN=0 or updates to the NCOs are scheduled to occur away from the change. (See <a href="#">NCO_SYNC</a>.)</p> <p>Note: This register has no effect when FR_EN=1.</p> |

### 7.5.3.75 FREQ[3] Register (Offset = 0338h) [reset = 0000000000000000h]

FREQ[3] is described in [Table 7-112](#).

Return to the [Register Summary Table](#).

FREQ for NCO3 Accumulator.

**Table 7-112. FREQ[3] Register Field Descriptions**

| Bit  | Field   | Type | Reset                         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|------|---------|------|-------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 63-0 | FREQ[3] | R/W  | 0000<br>0000<br>0000<br>0000h | <p>The NCO frequency (<math>F_{NCO}</math>) is:</p> $F_{NCO} = \text{FREQ}[3] * 2^{-64} * F_{CLK}$ <p>where <math>F_{CLK}</math> is the sample frequency of the DAC. FREQ[3] is the integer value of this register. This register can be interpreted as signed or unsigned (both interpretations are valid).</p> <p>Use this equation to determine the value to program:</p> $\text{FREQ}[3] = 2^{64} * F_{NCO} / F_{CLK}$ <p>Note: Changes to this register do not take effect until the next sync event specified by <a href="#">NCO_SYNC_SRC</a>.</p> <p>Note: This register should only be changed when DP_EN=0 or updates to the NCOs are scheduled to occur away from the change. (See <a href="#">NCO_SYNC</a>.)</p> <p>Note: This register has no effect when FR_EN=1.</p> |

### 7.5.3.76 PHASE0 Register (Offset = 0340h) [reset = 0000h]

PHASE0 is described in [Table 7-113](#).

Return to the [Register Summary Table](#).

Phase for NCO0 Accumulator.

**Table 7-113. PHASE0 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|--------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15-0 | PHASE0 | R/W  | 0h    | <p>Phase is added late so this register can be written during operation to change the phase without needing to reset the NCO.</p> <p>This value is left justified into a 32-bit field and then added to the phase accumulator. The phase (in radians) is <math>\text{PHASE0} * 2^{-16} * 2\pi</math>.</p> <p>This register can be interpreted as signed or unsigned.</p> <p>Note: Changes to this register do not take effect until the next sync event specified by <a href="#">NCO_SYNC_SRC</a>.</p> <p>Note: This register should only be changed when DP_EN=0 or updates to the NCOs are scheduled to occur away from the change. (See <a href="#">NCO_SYNC</a>.)</p> <p>Note: This register has no effect when FR_EN=1.</p> |

### 7.5.3.77 PHASE1 Register (Offset = 0342h) [reset = 0000h]

PHASE1 is described in [Table 7-114](#).

Return to the [Register Summary Table](#).

Phase for NCO1 Accumulator.

**Table 7-114. PHASE1 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|--------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15-0 | PHASE1 | R/W  | 0h    | <p>Phase is added late so this register can be written during operation to change the phase without needing to reset the NCO.</p> <p>This value is left justified into a 32-bit field and then added to the phase accumulator. The phase (in radians) is <math>\text{PHASE1} * 2^{-16} * 2\pi</math>.</p> <p>This register can be interpreted as signed or unsigned.</p> <p>Note: Changes to this register do not take effect until the next sync event specified by <a href="#">NCO_SYNC_SRC</a>.</p> <p>Note: This register should only be changed when DP_EN=0 or updates to the NCOs are scheduled to occur away from the change. (See <a href="#">NCO_SYNC</a>.)</p> <p>Note: This register has no effect when FR_EN=1.</p> |

### 7.5.3.78 PHASE2 Register (Offset = 0344h) [reset = 0000h]

PHASE2 is described in [Table 7-115](#).

Return to the [Register Summary Table](#).

Phase for NCO2 Accumulator.

**Table 7-115. PHASE2 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|------|--------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15-0 | PHASE2 | R/W  | 0h    | <p>Phase is added late so this register can be written during operation to change the phase without needing to reset the NCO.</p> <p>This value is left justified into a 32-bit field and then added to the phase accumulator. The phase (in radians) is <math>\text{PHASE2} * 2^{-16} * 2\pi</math>.</p> <p>This register can be interpreted as signed or unsigned.</p> <p>Note: Changes to this register do not take effect until the next sync event specified by <a href="#">NCO_SYNC_SRC</a>.</p> <p>Note: This register should only be changed when <math>\text{DP\_EN}=0</math> or updates to the NCOs are scheduled to occur away from the change. (See <a href="#">NCO_SYNC</a>.)</p> <p>Note: This register has no effect when <math>\text{FR\_EN}=1</math>.</p> |

### 7.5.3.79 PHASE3 Register (Offset = 0346h) [reset = 0000h]

PHASE3 is described in [Table 7-116](#).

Return to the [Register Summary Table](#).

Phase for NCO3 Accumulator.

**Table 7-116. PHASE3 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|------|--------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15-0 | PHASE3 | R/W  | 0h    | <p>Phase is added late so this register can be written during operation to change the phase without needing to reset the NCO.</p> <p>This value is left justified into a 32-bit field and then added to the phase accumulator. The phase (in radians) is <math>\text{PHASE3} * 2^{-16} * 2\pi</math>.</p> <p>This register can be interpreted as signed or unsigned.</p> <p>Note: Changes to this register do not take effect until the next sync event specified by <a href="#">NCO_SYNC_SRC</a>.</p> <p>Note: This register should only be changed when <math>\text{DP\_EN}=0</math> or updates to the NCOs are scheduled to occur away from the change. (See <a href="#">NCO_SYNC</a>.)</p> <p>Note: This register has no effect when <math>\text{FR\_EN}=1</math>.</p> |

### AMP\_R[3:0] Register (Offset = 0378h) [reset = NA]

AMP\_R[3:0] is described in [Table 7-117](#). AMP\_R[0] starts at address offset 0x0378, AMP\_R[1] at address offset 0x37A, AMP\_R[2] at address offset 0x37C and AMP\_R[3] at address offset 0x37E

Return to the [Register Summary Table](#).

**Table 7-117. AMP\_R[3:0] Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                    |
|------|----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15-0 | AMP_R[n] | R    | NA    | <p>This provides a readback of the amplitude setting that is currently in use by the DDS channel n. Format is 16-bit signed. This register is only applicable when <math>\text{DDS\_EN}=1</math>. When <math>\text{DDS\_EN}=0</math>, the return value is undefined. The value is sampled as each byte is read, so it may return incoherent data if the amplitude changes during readback.</p> |

### 7.5.3.80 FREQ\_R0 Register (Offset = 0380h) [reset = NA, read-only]

FREQ\_R0 is described in [Table 7-118](#).

Return to the [Register Summary Table](#).

Readback for Frequency for NCO0

**Table 7-118. FREQ\_R0 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                |
|------|---------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 63-0 | FREQ_R0 | R    | NA    | This provides a readback of the FREQ setting that is currently in used by the system for NCO0. The value is sampled as each byte is read, so it may return incoherent data if the operating value changes during readback. |

#### 7.5.3.81 FREQ\_R1 Register (Offset = 0388h) [reset = NA, read-only]

FREQ\_R1 is described in [Table 7-119](#).

Return to the [Register Summary Table](#).

Readback for Frequency for NCO1

**Table 7-119. FREQ\_R1 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                |
|------|---------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 63-0 | FREQ_R1 | R    | NA    | This provides a readback of the FREQ setting that is currently in used by the system for NCO1. The value is sampled as each byte is read, so it may return incoherent data if the operating value changes during readback. |

#### 7.5.3.82 FREQ\_R2 Register (Offset = 0390h) [reset = NA, read-only]

FREQ\_R2 is described in [Table 7-120](#).

Return to the [Register Summary Table](#).

Readback for Frequency for NCO2

**Table 7-120. FREQ\_R2 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                |
|------|---------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 63-0 | FREQ_R2 | R    | NA    | This provides a readback of the FREQ setting that is currently in used by the system for NCO2. The value is sampled as each byte is read, so it may return incoherent data if the operating value changes during readback. |

#### 7.5.3.83 FREQ\_R3 Register (Offset = 0398h) [reset = NA, read-only]

FREQ\_R3 is described in [Table 7-121](#).

Return to the [Register Summary Table](#).

Readback for Frequency for NCO3

**Table 7-121. FREQ\_R3 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                |
|------|---------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 63-0 | FREQ_R3 | R    | NA    | This provides a readback of the FREQ setting that is currently in used by the system for NCO3. The value is sampled as each byte is read, so it may return incoherent data if the operating value changes during readback. |

### 7.5.3.84 PHASE\_R0 Register (Offset = 03A0h) [reset = NA, read-only]

PHASE\_R0 is described in [Table 7-122](#).

Return to the [Register Summary Table](#).

Readback for Phase Word for NCO0

**Table 7-122. PHASE\_R0 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                 |
|------|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15-0 | PHASE_R0 | R/W  | 0h    | This provides a readback of the PHASE setting that is currently in used by the system for NCO0. The value is sampled as each byte is read, so it may return incoherent data if the operating value changes during readback. |

### 7.5.3.85 PHASE\_R1 Register (Offset = 03A2h) [reset = NA, read-only]

PHASE\_R1 is described in [Table 7-123](#).

Return to the [Register Summary Table](#).

Readback for Phase Word for NCO1

**Table 7-123. PHASE\_R1 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                 |
|------|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15-0 | PHASE_R1 | R/W  | NA    | This provides a readback of the PHASE setting that is currently in used by the system for NCO1. The value is sampled as each byte is read, so it may return incoherent data if the operating value changes during readback. |

### 7.5.3.86 PHASE\_R2 Register (Offset = 03A4h) [reset = NA, read-only]

PHASE\_R2 is described in [Table 7-124](#).

Return to the [Register Summary Table](#).

Readback for Phase Word for NCO2

**Table 7-124. PHASE\_R2 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                 |
|------|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15-0 | PHASE_R2 | R/W  | NA    | This provides a readback of the PHASE setting that is currently in used by the system for NCO2. The value is sampled as each byte is read, so it may return incoherent data if the operating value changes during readback. |

### 7.5.3.87 PHASE\_R3 Register (Offset = 03A6h) [reset = NA, read-only]

PHASE\_R3 is described in [Table 7-125](#).

Return to the [Register Summary Table](#).

Readback for Phase Word for NCO3

**Table 7-125. PHASE\_R3 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                 |
|------|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15-0 | PHASE_R3 | R/W  | NA    | This provides a readback of the PHASE setting that is currently in used by the system for NCO3. The value is sampled as each byte is read, so it may return incoherent data if the operating value changes during readback. |

### 7.5.3.88 FR\_FRS\_R Register (Offset = 03E0h) [reset = NA, read-only]

FR\_FRS\_R is shown in [Figure 7-135](#) and described in [Table 7-126](#).

Return to the [Register Summary Table](#).

Readback for FR Synchrononization

**Figure 7-135. FR\_FRS\_R Register**

|          |   |          |   |   |   |   |   |
|----------|---|----------|---|---|---|---|---|
| 7        | 6 | 5        | 4 | 3 | 2 | 1 | 0 |
| FR_FRS_R |   | RESERVED |   |   |   |   |   |
| R        |   | R        |   |   |   |   |   |

**Table 7-126. FR\_FRS\_R Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                                                                                                            |
|-----|----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | FR_FRS_R | R    | NA    | This provides readback for the value of FRS in the last transaction.<br>Note: This value is not synchronized and should only be read while the FR interface is static. |
| 6-0 | RESERVED | R    | NA    |                                                                                                                                                                        |

### 7.5.3.89 FR\_NCO\_AR\_R Register (Offset = 03E1h) [reset = NA, read-only]

FR\_NCO\_AR\_R is shown in [Figure 7-136](#) and described in [Table 7-127](#).

Return to the [Register Summary Table](#).

Readback for FR NCO Accumulator Reset

**Figure 7-136. FR\_NCO\_AR\_R Register**

|          |   |   |   |             |   |   |   |
|----------|---|---|---|-------------|---|---|---|
| 7        | 6 | 5 | 4 | 3           | 2 | 1 | 0 |
| RESERVED |   |   |   | FR_NCO_AR_R |   |   |   |
| R        |   |   |   | R           |   |   |   |

**Table 7-127. FR\_NCO\_AR\_R Register Field Descriptions**

| Bit | Field       | Type | Reset | Description                                                                                                                                                                |
|-----|-------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-4 | RESERVED    | R    | NA    |                                                                                                                                                                            |
| 3-0 | FR_NCO_AR_R | R    | NA    | This provides readback for the last value that was written to FR_NCO_AR.<br>Note: This value is not synchronized and should only be read while the FR interface is static. |

### 7.5.3.90 TS\_TEMP Register (Offset = 0400h) [reset = NA, read-only]

TS\_TEMP is shown in [Figure 7-137](#) and described in [Table 7-128](#).

Return to the [Register Summary Table](#).

Temperature Reading in Celsius

**Figure 7-137. TS\_TEMP Register**

|         |   |   |   |   |   |   |   |
|---------|---|---|---|---|---|---|---|
| 7       | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TS_TEMP |   |   |   |   |   |   |   |
| R       |   |   |   |   |   |   |   |

**Table 7-128. TS\_TEMP Register Field Descriptions**

| Bit | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                     |
|-----|---------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-0 | TS_TEMP | R    | NA    | Returns the temperature sensor reading. This returns an unsigned value from 0 to 255. Subtract 80 from this value to get degrees Celsius. For example, a value of 110 indicates 30C.<br>See Temperature Sensor.<br>Note: Reads of this register require slower SPI timing. See <a href="#">Switching Characteristics</a> .<br>Note: This register will not return valid data unless TS_SLEEP=0. |

### 7.5.3.91 TS\_SLEEP Register (Offset = 0401h) [reset = 00h]

TS\_SLEEP is shown in [Figure 7-138](#) and described in [Table 7-129](#).

Return to the [Register Summary Table](#).

Temperature Sensor Sleep

**Figure 7-138. TS\_SLEEP Register**

|          |   |   |   |   |   |   |          |
|----------|---|---|---|---|---|---|----------|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0        |
| RESERVED |   |   |   |   |   |   | TS_SLEEP |
| R/W-00h  |   |   |   |   |   |   | R/W-0b   |

**Table 7-129. TS\_SLEEP Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                              |
|-----|----------|------|-------|------------------------------------------------------------------------------------------|
| 7-1 | RESERVED | R/W  | 00h   |                                                                                          |
| 0   | TS_SLEEP | R/W  | 0b    | If temperature conversions are not needed, set this bit to sleep the temperature sensor. |

### 7.5.3.92 SYNC\_STATUS Register (Offset = 0410h) [reset = NA]

SYNC\_STATUS is shown in [Figure 7-139](#) and described in [Table 7-130](#).

Return to the [Register Summary Table](#).

Synchronization Status

**Figure 7-139. SYNC\_STATUS Register**

|          |   |   |   |               |             |              |            |
|----------|---|---|---|---------------|-------------|--------------|------------|
| 7        | 6 | 5 | 4 | 3             | 2           | 1            | 0          |
| RESERVED |   |   |   | CLK_REALIGNED | CLK_ALIGNED | NCO_SYNC_DET | SYSREF_DET |
| R        |   |   |   | R/W1C         | R           | R/W1C        | R/W1C      |

**Table 7-130. SYNC\_STATUS Register Field Descriptions**

| Bit | Field         | Type  | Reset | Description                                                                                                                                                                                                                                                                                                                             |
|-----|---------------|-------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-4 | RESERVED      | R/W   | NA    |                                                                                                                                                                                                                                                                                                                                         |
| 3   | CLK_REALIGNED | R/W1C | NA    | This bit is set any time the clock dividers associated with SYSREF (excluding LMFC/LEMC) are realigned to SYSREF. This bit is useful to confirm the internally sampled SYSREF signal has a correct and stable period in DDS mode (or for debug purposes in JESD204C mode). Write a 1 to clear this bit.                                 |
| 2   | CLK_ALIGNED   | R     | NA    | When set, indicates that the last SYSREF pulse was consistent with the SYSREF-associated clock dividers (except for the LMFC/LEMC). Since the LMFC/LEMC does not affect this bit, it is appropriate to use in DDS mode, but can also be used when the JESD204C interface is enabled. This bit is read-only (cannot be cleared via SPI). |

**Table 7-130. SYNC\_STATUS Register Field Descriptions (continued)**

| Bit | Field        | Type  | Reset | Description                                                                                           |
|-----|--------------|-------|-------|-------------------------------------------------------------------------------------------------------|
| 1   | NCO_SYNC_DET | R/W1C | NA    | This bit is set any time one or more NCOs receives a sync event. Write a 1 to clear this bit.         |
| 0   | SYSREF_DET   | R/W1C | NA    | This bit is set when a SYSREF is detected. Write a 1 to clear the bit and allow it to be re-detected. |

### 7.5.3.93 SYS\_ALM Register (Offset = 0430h) [reset = NA, read/write 1 to clear]

SYS\_ALM is shown in [Figure 7-140](#) and described in [Table 7-131](#).

Return to the [Register Summary Table](#).

System Alarm Status

**Figure 7-140. SYS\_ALM Register**

| 7                  | 6                  | 5            | 4        | 3 | 2 | 1          | 0          |
|--------------------|--------------------|--------------|----------|---|---|------------|------------|
| JESD_LINK_DOWN_ALM | JTIMER_EXPIRED_ALM | JESD_CRC_ALM | RESERVED |   |   | SYSRST_ALM | SYSREF_ALM |
| R/W1C              | R/W1C              | R/W1C        | R        |   |   | R/W1C      | R/W1C      |

**Table 7-131. SYS\_ALM Register Field Descriptions**

| Bit | Field              | Type  | Reset | Description                                                                                                                                                                      |
|-----|--------------------|-------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | JESD_LINK_DOWN_ALM | R/W1C |       | This bit is set any time LINK_UP transitions from 1 to 0 while JESD_EN=1. Write 1 to clear the alarm.                                                                            |
| 6   | JTIMER_EXPIRED_ALM | R/W1C |       | This bit is set if the JESD link has been down (LINK_UP=0 while JESD_EN=1) longer than allowed by JTIMER. Write 1 to clear the alarm.                                            |
| 5   | JESD_CRC_ALM       | R/W1C |       | This bit is set any time CRC_FAULT is detected on an enabled lane. Applies only to 64b/66b modes. Write 1 to clear the alarm.                                                    |
| 4-2 | RESERVED           | R     |       |                                                                                                                                                                                  |
| 1   | SYSRST_ALM         | R/W1C |       | This bit is set any time the chip is reset due to the RESET <sub>ball</sub> , power on reset, or SOFT_RESET. Write 1 to clear the alarm.                                         |
| 0   | SYSREF_ALM         | R/W1C |       | This bit is set any time a SYSREF edge is detected at an incorrect alignment by either the clock dividers or by the JESD Subsystem (when JESD_EN=1). Write 1 to clear the alarm. |

### 7.5.3.94 ALM\_MASK Register (Offset = 0431h) [reset = 00h]

ALM\_MASK is shown in [Figure 7-141](#) and described in [Table 7-132](#).

Return to the [Register Summary Table](#).

Alarm Mask

**Figure 7-141. ALM\_MASK Register**

| 7                   | 6                   | 5             | 4        | 3 | 2 | 1 | 0               |
|---------------------|---------------------|---------------|----------|---|---|---|-----------------|
| JESD_LINK_DOWN_MASK | JTIMER_EXPIRED_MASK | JESD_CRC_MASK | RESERVED |   |   |   | SYSREF_ALM_MASK |
| R/W-0b              | R/W-0b              | R/W-0b        | R/W-0h   |   |   |   | R/W-0b          |

**Table 7-132. ALM\_MASK Register Field Descriptions**

| Bit | Field               | Type | Reset | Description                                                                                            |
|-----|---------------------|------|-------|--------------------------------------------------------------------------------------------------------|
| 7   | JESD_LINK_DOWN_MASK | R/W  | 0h    | When set, alarms from the JESD_LINK_DOWN_ALM register are masked and will not impact the alarm output. |

**Table 7-132. ALM\_MASK Register Field Descriptions (continued)**

| Bit | Field               | Type | Reset | Description                                                                                            |
|-----|---------------------|------|-------|--------------------------------------------------------------------------------------------------------|
| 6   | JTIMER_EXPIRED_MASK | R/W  | 0b    | When set, alarms from the JTIMER_EXPIRED_ALM register are masked and will not impact the alarm output. |
| 5   | JESD_CRC_MASK       | R/W  | 0b    | When set, alarms from the JESD_CRC_ALM register are masked and will not impact the alarm output.       |
| 4-1 | RESERVED            | R/W  | 0h    |                                                                                                        |
| 0   | SYSREF_ALM_MASK     | R/W  | 0b    | When set, alarms from the SYSREF_ALM register are masked and will not impact the alarm output.         |

### 7.5.3.95 MUTE\_MASK Register (Offset = 0432h) [reset = 21h]

MUTE\_MASK is shown in [Figure 7-142](#) and described in [Table 7-133](#).

Return to the [Register Summary Table](#).

DAC Mute Mask

**Figure 7-142. MUTE\_MASK Register**

|          |   |                    |   |          |   |   |                  |
|----------|---|--------------------|---|----------|---|---|------------------|
| 7        | 6 | 5                  | 4 | 3        | 2 | 1 | 0                |
| RESERVED |   | JESD_CRC_MUTE_MASK |   | RESERVED |   |   | SYSREF_MUTE_MASK |
| R/W-00b  |   | R/W-1b             |   | R/W-0h   |   |   | R/W-1b           |

**Table 7-133. MUTE\_MASK Register Field Descriptions**

| Bit | Field              | Type | Reset | Description                                                                          |
|-----|--------------------|------|-------|--------------------------------------------------------------------------------------|
| 7-6 | RESERVED           | R/W  | 00b   |                                                                                      |
| 5   | JESD_CRC_MUTE_MASK | R/W  | 1b    | JESD CRC alarms will mute the DACs according to JESD_CRC_REC unless this bit is set. |
| 4-1 | RESERVED           | R/W  | 0h    |                                                                                      |
| 0   | SYSREF_MUTE_MASK   | R/W  | 1b    | Alarms from the SYSREF_ALM register will mute the DACs unless this bit is set.       |

### 7.5.3.96 MUTE\_REC Register (Offset = 0433h) [reset = A0h]

MUTE\_REC is shown in [Figure 7-143](#) and described in [Table 7-134](#).

Return to the [Register Summary Table](#).

DAC Mute Recovery

**Figure 7-143. MUTE\_REC Register**

|                    |          |              |   |          |   |   |   |
|--------------------|----------|--------------|---|----------|---|---|---|
| 7                  | 6        | 5            | 4 | 3        | 2 | 1 | 0 |
| JESD_LINK_DOWN_REC | RESERVED | JESD_CRC_REC |   | RESERVED |   |   |   |
| R/W-1b             | R/W-0b   | R/W-1b       |   | R/W-00h  |   |   |   |

**Table 7-134. MUTE\_REC Register Field Descriptions**

| Bit | Field              | Type | Reset | Description                                                                                                                 |
|-----|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------|
| 7-6 | JESD_LINK_DOWN_REC | R/W  | 1b    | 0: DAC will remain muted until the JESD_LINK_DOWN_ALM = 0.<br>1: DAC will unmute automatically when the JESD link recovers. |
| 6   | RESERVED           | R/W  | 0b    |                                                                                                                             |

**Table 7-134. MUTE\_REC Register Field Descriptions (continued)**

| Bit | Field              | Type | Reset | Description                                                                                                                                                 |
|-----|--------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5   | JESD_CRC_MUTE_MASK | R/W  | 1b    | This bit is only used if JESD_CRC_MUTE_MASK = 0.<br>0: DAC will remain muted until the JESD_CRC_ALM=0<br>1: DAC will unmute automatically when CRC_FAULT=0. |
| 4-0 | RESERVED           | R/W  | 0h    |                                                                                                                                                             |

### 7.5.3.97 FUSE\_STATUS Register (Offset = 0600h) [reset = NA]

FUSE\_STATUS is shown in [Figure 7-142](#) and described in [Table 7-133](#).

Return to the [Register Summary Table](#).

Fuse Status

**Figure 7-144. FUSE\_STATUS Register**

|          |   |   |   |   |   |   |           |
|----------|---|---|---|---|---|---|-----------|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0         |
| RESERVED |   |   |   |   |   |   | FUSE_DONE |
| R-NA     |   |   |   |   |   |   | R-NA      |

**Table 7-135. FUSE\_STATUS Register Field Descriptions**

| Bit | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                    |
|-----|-----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-1 | RESERVED  | R    | NA    |                                                                                                                                                                                                                                                                                                                |
| 0   | FUSE_DONE | R    | NA    | Returns '1' when the fuse controller is idle, meaning the controller has completed the fuse auto-load sequence. The sequence takes less than 523,000 CLK cycles to complete, or FUSE_DONE can be polled until it is '1'.<br>When FUSE_DONE is '0' the user should not read or write any fuse-backed registers. |

### 7.5.3.98 FINE\_CUR\_A Register (Offset = 0723h) [reset = varies]

FINE\_CUR\_A is shown in [Figure 7-145](#) and described in [Table 7-136](#).

Return to the [Register Summary Table](#).

Fine Bias Current Control for DACA

**Figure 7-145. FINE\_CUR\_A Register**

|          |   |            |   |   |   |   |   |
|----------|---|------------|---|---|---|---|---|
| 7        | 6 | 5          | 4 | 3 | 2 | 1 | 0 |
| RESERVED |   | FINE_CUR_A |   |   |   |   |   |
| R-00b    |   | R/W-varies |   |   |   |   |   |

**Table 7-136. FINE\_CUR\_A Register Field Descriptions**

| Bit | Field      | Type | Reset  | Description                                                                                                                                    |
|-----|------------|------|--------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-6 | RESERVED   | R    | 00b    |                                                                                                                                                |
| 5-0 | FINE_CUR_A | R/W  | varies | Fine current control setting for DAC A. See <a href="#">Section 7.3.2.2</a> . The default values varies to match output current specification. |

### 7.5.3.99 COARSE\_CUR\_A Register (Offset = 0724h) [reset = 0Fh]

COARSE\_CUR\_A is shown in [Figure 7-146](#) and described in [Table 7-137](#).

Return to the [Register Summary Table](#).

Coarse Bias Current Control for DACA

**Figure 7-146. COARSE\_CUR\_A Register**

| 7                | 6 | 5 | 4 | 3            | 2 | 1 | 0 |
|------------------|---|---|---|--------------|---|---|---|
| DAC0_CBIAS_SLEEP |   |   |   | COARSE_CUR_A |   |   |   |
| R/W-0h           |   |   |   | R/W-0xF      |   |   |   |

**Table 7-137. COARSE\_CUR\_A Register Field Descriptions**

| Bit | Field            | Type | Reset | Description                                                                                                     |
|-----|------------------|------|-------|-----------------------------------------------------------------------------------------------------------------|
| 7-4 | DAC0_CBIAS_SLEEP | R/W  | 0h    | DAC coarse current setting during sleep. See discussion for DC coupled outputs in <a href="#">Section 8.1.6</a> |
| 3-0 | COARSE_CUR_A     | R/W  | 0xF   | Coarse current control setting for DAC A. See <a href="#">Section 7.3.2.2</a> .                                 |

### 7.5.3.100 FINE\_CUR\_B Register (Offset = 0725h) [reset = varies]

FINE\_CUR\_B is shown in [Figure 7-147](#) and described in [Table 7-138](#).

Return to the [Register Summary Table](#).

Fine Bias Current Control for DAC B

**Figure 7-147. FINE\_CUR\_B Register**

| 7        | 6 | 5          | 4 | 3 | 2 | 1 | 0 |
|----------|---|------------|---|---|---|---|---|
| RESERVED |   | FINE_CUR_B |   |   |   |   |   |
| R-00b    |   | R/W-varies |   |   |   |   |   |

**Table 7-138. FINE\_CUR\_B Register Field Descriptions**

| Bit | Field      | Type | Reset  | Description                                                                                                                                    |
|-----|------------|------|--------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-6 | RESERVED   | R    | 00b    |                                                                                                                                                |
| 5-0 | FINE_CUR_B | R/W  | varies | Fine current control setting for DAC B. See <a href="#">Section 7.3.2.2</a> . The default values varies to match output current specification. |

### 7.5.3.101 COARSE\_CUR\_B Register (Offset = 0726h) [reset = 0Fh]

COARSE\_CUR\_B is shown in [Figure 7-148](#) and described in [Table 7-139](#).

Return to the [Register Summary Table](#).

Coarse Bias Current Control for DACB

**Figure 7-148. COARSE\_CUR\_B Register**

| 7                | 6 | 5 | 4 | 3            | 2 | 1 | 0 |
|------------------|---|---|---|--------------|---|---|---|
| DAC1_CBIAS_SLEEP |   |   |   | COARSE_CUR_B |   |   |   |
| R/W-0h           |   |   |   | R/W-0xF      |   |   |   |

**Table 7-139. COARSE\_CUR\_B Register Field Descriptions**

| Bit | Field            | Type | Reset | Description                                                                                                     |
|-----|------------------|------|-------|-----------------------------------------------------------------------------------------------------------------|
| 7-4 | DAC1_CBIAS_SLEEP | R/W  | 0h    | DAC coarse current setting during sleep. See discussion for DC coupled outputs in <a href="#">Section 8.1.6</a> |
| 3-0 | COARSE_CUR_B     | R/W  | 0xF   | Coarse current control setting for DAC B. See <a href="#">Section 7.3.2.2</a> .                                 |

### 7.5.3.102 DEM\_ADJ Register (Offset = 0727h) [reset = 11h]

DEM\_ADJ is shown in [Figure 7-148](#) and described in [Table 7-139](#).

Return to the [Register Summary Table](#)

DEM Adjust

**Table 7-140. Single Edge DEM Adjust**

| 7        | 6 | 5 | 4 | 3        | 2 | 1 | 0 |
|----------|---|---|---|----------|---|---|---|
| DEM_ADJ1 |   |   |   | DEM_ADJ0 |   |   |   |
| R/W-0x1  |   |   |   | R/W-0x1  |   |   |   |

**Table 7-141. DEM\_ADJ Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                               |
|-----|----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-4 | DEM_ADJ1 | R/W  | 0x1   | Adjust DEM behavior for single-edge data-independent DEM for DAC1. This register has no effect unless DAC1 is configured for single-edge data-independent DEM. Only 0 to 3 are valid settings, 4 through 15 are reserved. |
| 3-0 | DEM_ADJ0 | R/W  | 0x1   | Adjust DEM behavior for single-edge data-independent DEM for DAC0. This register has no effect unless DAC0 is configured for single-edge data-independent DEM. Only 0 to 3 are valid settings, 4 through 15 are reserved. |

### 7.5.3.103 DEM\_DITH Register (Offset = 0729h) [reset = 00h]

DEM\_DITH is shown in [Figure 7-149](#) and described in [Table 7-142](#).

Return to the [Register Summary Table](#).

DAC DEM and Dither Control

**Figure 7-149. DEM\_DITH Register**

| 7        | 6 | 5        | 4 | 3           | 2 | 1           | 0 |
|----------|---|----------|---|-------------|---|-------------|---|
| DEM_DACB |   | DEM_DACA |   | DITHER_DACB |   | DITHER_DACA |   |
| R/W-00b  |   | R/W-00b  |   | R/W-00b     |   | R/W-00b     |   |

**Table 7-142. DEM\_DITH Register Field Descriptions**

| Bit | Field       | Type | Reset | Description                                                                                                                                                                         |
|-----|-------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-6 | DEM_DACB    | R/W  | 00b   | 0 : Enable single-edge, data-independent DEM for DACB<br>1 : Enable dual-edge, data-independent DEM for DACB<br>2 : Enable data-dependent DEM for DACB<br>3 : DEM disabled for DACB |
| 5-4 | DEM_DACA    | R/W  | 00b   | 0 : Enable single-edge, data-independent DEM for DACA<br>1 : Enable dual-edge, data-independent DEM for DACA<br>2 : Enable data-dependent DEM for DACA<br>3 : DEM disabled for DACA |
| 3-2 | DITHER_DACB | R/W  | 00b   | 0 : Enable single-edge dithering for DACB<br>1 : Enable dual-edge dithering for DACB<br>2 : RESERVED<br>3 : Dithering disabled for DACB                                             |

**Table 7-142. DEM\_DITH Register Field Descriptions (continued)**

| Bit | Field       | Type | Reset | Description                                                                                                                             |
|-----|-------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------|
| 1-0 | DITHER_DACA | R/W  | 00b   | 0 : Enable single-edge dithering for DACA<br>1 : Enable dual-edge dithering for DACA<br>2 : RESERVED<br>3 : Dithering disabled for DACA |

#### 7.5.3.104 DAC\_OFS[0:1] Register (Offset = 072Ah) [reset = 00h]

DAC\_OFS[0:1] is described in [Table 7-143](#).

Return to the [Register Summary Table](#).

DAC Offset Control. DAC\_OFS[0] is at the lowest address.

**Table 7-143. DAC\_OFS[0:1] Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15-13 | Reserved   | R/W  | 000b  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 12-0  | DAC_OFS[n] | R/W  | 00b   | Offset adjustment for DACn (n = 0 or 1). The value in this register is added to the DACn output. This is a 2's complement, 13-bit signed value. The LSB weight is one DAC LSB.<br><br>The value programmed into this register passes through a saturation function to limit the adjustment to what is possible. If dithering is enabled on DACn (see <a href="#">DEM_DITH</a> ), DAC_OFS[n] is saturated to the range +/- 128. If dithering is disabled on DACn, the saturation range is +/-3968.<br><br>See <a href="#">Section 7.3.4</a> .<br><br>Note: This value should only be changed when DP_EN=0 or DAC_OFS_CHG_BLK=1. |

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

#### 8.1.1 Startup Procedure for DUC/Bypass Mode

The list below is the startup procedure for the device:

1. Power up the device with ball **RESET** asserted using the procedure in [Section 8.3.1](#).
2. Apply CLK and then de-assert RESET.
3. Wait for fuse values to be loaded (register **FUSE\_DONE** returns 1).
4. Set up all the operational parameters (registers can be programmed in any order):
  - a. Program interpolation factor in the **DUC\_L** register.
  - b. Determine the total interpolation factor (**LT**), which is needed in the next steps.  $LT = DUC\_L$ .
  - c. Determine many sample streams are needed and program the **JESD\_M** register.
  - d. Select a JESD204C mode from [Table 7-22](#). Make sure the selected mode supports the value of **LT** computed previously and the desired link layer encoding. Also make sure the mode supports the number of desired streams set in the **JESD\_M** register. Program the mode number into the **JMODE** register.
  - e. Program the **JENC** register to select 8b/10b or 64b/66b operation.
  - f. Compute the value of **R** using [Table 7-22](#) and the **LT** value computed earlier.
  - g. Using [Table 7-17](#) (8b/10b) or [Table 7-18](#) (64b/66b), identify a row that matches the **R** value and DAC clock frequency. Program **REFDIV**, **MPY**, **RATE** and **VRANGE** according to the tables.
  - h. If necessary, program **LANE\_SELn** to bind the physical lanes 6 and 14 to logical lanes 0 and 1. Program **LANE\_INV** if necessary to account for any lane inversion (differential pairs swapped on PCB).
  - i. Program other common settings according to your desired usage (SUBCLASS, SFORMAT, SCR in **JCTRL**).
  - j. If using 8b/10b encoding, program the **KM1** register to set the K parameter. KM1 must match the link partner. Be sure to honor the constraint imposed by the **KR** parameter from [Table 7-22](#).
  - k. If subclass 1 operation is desired (SUBCLASS=1), you must also program **RBD**. Determine the appropriate value for **RBD** by referring to: [Programming RBD](#).
  - l. Optional Serdes parameters can also be programmed if necessary (that is, **JPHY\_CNTL**, **EQ\_CNTL**, **EQZERO**, **LANE\_EQn**).
  - m. Program any DAC or DUC related registers, for example the **DAC\_SRC** register to route data to your desired DACs and configure **MXMODE** to set the DAC output mode.
5. Program the transmitter (link partner, that is, FPGA or ASIC), and instruct the transmitter to begin transmission.
6. Program **JESD\_EN**=1 to start up the receiver.
7. Program **DP\_EN**=1 to enable the datapath. This is required to allow data to flow to the DAC. If only JESD204C diagnostics are performed, you can leave **DP\_EN** at 0.
8. Wait for the VDDDIG supply voltage to re-stabilize as the supply current transient can result in a dip in the supply voltage. 80 microseconds is sufficient, but this can be optimized based on actual measurements.
9. If **SUBCLASS**=1, SYSREF is necessary to establish the LMFC/LEMC phase in the receiver. Follow this procedure:
  - a. Using two separate transactions, program **SYSREF\_RECV\_SLEEP**=0 and then **SYSREF\_PROC\_EN**=1 (both in register **SYSREF\_CNTL**).
  - b. Program **SYSREF\_SEL** to a known good value (see [SYSREF Windowing](#) for details on how to calculate **SYSREF\_SEL** using the SYSREF windowing function).
  - c. Program **SYSREF\_ALIGN\_EN**=1.

- d. Apply at least five SYSREF pulses to the SYSREF input. The period of each SYSREF cycle must meet the requirements in [Table 7-3](#).
10. Read the [JESD\\_STATUS](#) register to confirm operation of the link (LINK\_UP field in [JESD\\_STATUS](#) = 1). If the LINK\_UP field returns 0, verify these items:
  - a. If the PLL\_LOCKED field in [JESD\\_STATUS](#) returns 0, verify the correct PLL settings ([REFDIV](#), [MPY](#), [RATE](#) and [VRANGE](#)). Verify the CLK frequency is correct.
  - b. If [SUBCLASS](#) = 1, and the ALIGNED field in [JESD\\_STATUS](#) returns 0, verify SYSREF has been applied and the SYSREF processor is enabled [SYSREF\\_PROC\\_EN](#).
  - c. If above are not the problem, then read the [LANE\\_STATUSn](#) (only read registers for logical lanes 0 to L-1). Identify if some lanes cannot acquire code group or block synchronization. If so, verify the transmitter has been programmed correctly. Verify [LANE\\_SELn](#) is programmed correctly. Consider performing PHY tests to verify/optimize PHY operation (PRBS testing using [JTEST](#), eye-scan testing, or equalizer optimization).
11. If coherency between multiple NCOs is required, the NCOs must be re-synchronized using one of the methods described in section [NCO Synchronization](#) for multi-device/deterministic synchronization, or using [SPI\\_SYNC](#) with [NCO\\_SYNC\\_SRC](#) if only internal NCO phase is required.
12. To configure the part for a different mode, set [DP\\_EN](#)=0 and [JESD\\_EN](#)=0. Then return to step 4.

### 8.1.2 Startup Procedure for DDS Mode

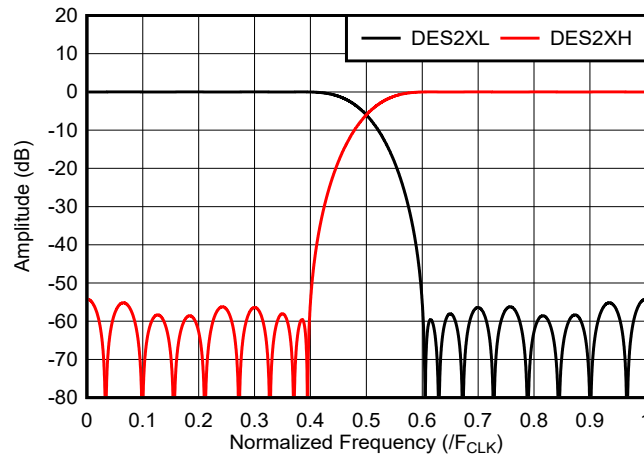
The DUC channels can operate in DDS mode by setting the [DDS\\_EN](#) register before setting [DP\\_EN](#).

To use DDS mode, perform these steps:

1. Program [DDS\\_EN](#)=1 (the DDS isn't enabled until [DP\\_EN](#) is set)
2. Program [JESD\\_M](#) to 2, 4, 6, or 8 to enable 1, 2, 3, or 4 DDS channels respectively
3. Program initial values for [AMP](#), [FREQ](#), and [PHASE](#)
4. There is no need to program [NCO\\_EN](#) (it's implied by [DDS\\_EN](#)=1)
5. Program [DUC\\_FORMAT](#)=1 if complex output is desired. If [DUC\\_FORMAT](#)=1, [JESD\\_M](#) must be set to 2 or 4 (1 or 2 channels).
6. Program [DAC\\_SRC](#) to bind DUC (DDS) channels to DACs
7. Leave [JESD\\_EN](#)=0
8. Program [DP\\_EN](#)=1
9. Wait for the VDDDIG supply voltage to re-stabilize as the supply current transient can result in a dip in the supply voltage. 80 microseconds is sufficient, but this can be optimized based on actual measurements.
10. If coherency between multiple NCO's is required, the NCO's must be re-synchronized using one of the methods described in section [NCO Synchronization](#) for multi-device/deterministic synchronization, or using [SPI\\_SYNC](#) with [NCO\\_SYNC\\_SRC](#) if only internal NCO phase is required.
11. The DUC channels now run in DDS mode and begin outputting tones. Use [AMP](#), [FREQ](#), and [PHASE](#) to update the waveform parameters. You must re-synchronize the NCOs to apply new values to the NCOs. Use [AMP\\_R](#), [FREQ\\_R](#), and [PHASE\\_R](#) to inspect the values that are currently in effect.
12. Other NCO settings also apply to DDS mode such as [NCO\\_AR](#), and [NCO\\_CONT](#). The NCOs can be synchronized in the same fashion as DUC mode.

### 8.1.3 Understanding Dual Edge Sampling Modes

Dual edge sampling modes (DES2XL/H) outputs unique samples on both the rising and falling edge of CLK, doubling the sample rate for the same clock frequency compared to NRZ, RTZ or RF modes. DES2XL/H modes generate the falling edge samples by digital interpolation. The 2x DES interpolator has an 80% passband bandwidth, 55dB stopband attenuation and can be configured as low pass or high pass (The response is shown in [Figure 8-1](#)). The DES interpolator is lowpass in DES2XL mode, passing the signal below  $0.4 \cdot F_{CLK}$  and removing the image above  $0.6 \cdot F_{CLK}$ . IN DES2XH mode signals above  $0.6 \cdot F_{CLK}$  are passed and the image below  $0.4 \cdot F_{CLK}$  is removed. In the transition band between  $0.4 \cdot F_{CLK}$  and  $0.6 \cdot F_{CLK}$ , the passband is attenuated by up to 6dB and the image attenuation is significantly reduced.



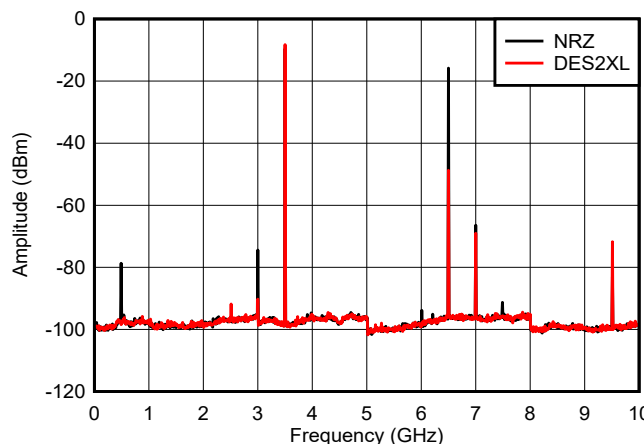
**Figure 8-1. DES Interpolator Frequency Response**

A non-50% CLK duty cycle results in an image of the signal at  $F_{CLK} - F_{OUT}$ . The amplitude of the image in DES2XL/H modes compared to NRZ/RF modes is shown in [Figure 8-2](#). DES2XL provides 30+dB suppression over NRZ mode and DES2XH 20 to 30 dB suppression over RF mode. This reduces the analog filtering required after the DAC to remove the unwanted images.

**Figure 8-2. DES2XL/H Image compare to NRZ and RF Modes**

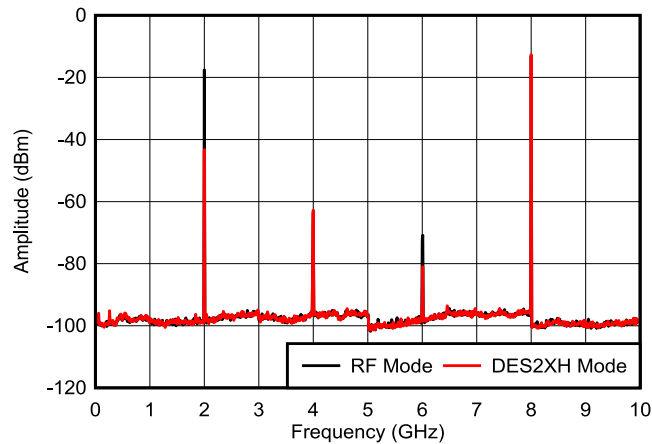
The input clock frequency and input data rate is the same for NRZ, RF, RTZ, DES2XL and DES2XH modes - only the output waveform generated by the DAC is changed (See [Section 7.3.1](#)). Changing between modes only requires a different setting of the [MXMODE](#) register.

[Figure 8-3](#) shows a comparison of DES2XL and NRZ mode for a fullscale tone at 3497MHz with 10GSPS clock frequency. In addition to the reduction of the image at  $F_{CLK} - F_{OUT} = 6743\text{MHz}$ , DES2XL mode can also suppress harmonics that in NRZ mode fold back below  $F_{CLK}/2$ . In the plot, HD2 has an image at 3006MHz that is -65dBc in NRZ mode and -80dBc in DES2XL mode. Likewise, the HD3 image at 491MHz improves from -70dBc in NRZ mode to better than -90dBc in DES2XL mode. SFDR between 0 and  $F_{CLK}/2$  is limited by HD2 and therefore improves from 65 to 80dBc. Note that the non-linearity specifications for DES2XL mode in [Section 6](#) are measured between 0 to  $F_{CLK}/2$  (as is NRZ mode), and for DES2XH mode between  $F_{CLK}/2$  and  $F_{CLK}$ .



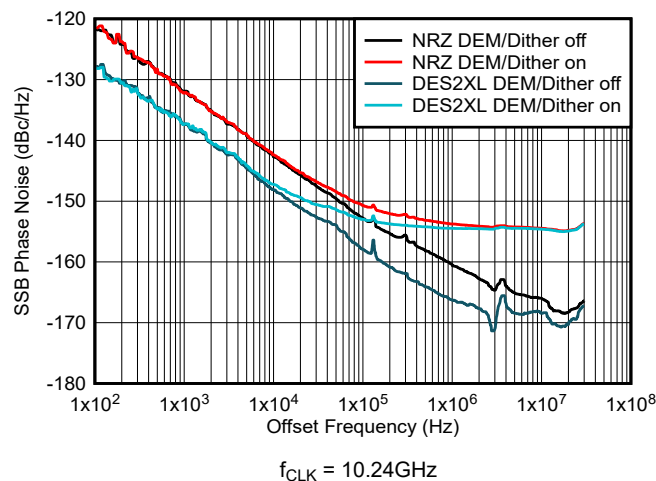
**Figure 8-3. Output Spectra Comparing DES2XL and NRZ Modes**

RF and DES2XH mode behave similarly. [Figure 8-4](#) shows a tone at 7997MHz with 10GHz clock in RF and DES2XH modes. HD2 and HD3 have folded frequencies around 6GHz in NRZ mode, these are suppressed > 10dB in DES2XH mode.



**Figure 8-4. Output Spectra Comparing DES2XH and RF Modes**

One additional benefit of DES2XL compared to NRZ mode is an improvement in additive phase noise of approximately 6dB in the  $1/f$  region of the offset frequency (see Figure 8-5). This is due to DES2XL using both the rising and falling edges of the clock, which cancels some common mode noise in the clock path. Since RF mode also uses the falling edge to generate the inverse sample, there is no significant difference between RF mode and DES2XH mode.



**Figure 8-5. Phase Noise vs Offset Frequency at 1GHz**

There are 3 small disadvantages of DES2XL and DES2XH modes to be aware of:

1. the attenuation of the signal in the transition band of the DES interpolation filter between  $0.4 \cdot f_{CLK}$  and  $0.6 \cdot f_{CLK}$
2. An increased latency of 97 clock cycles. or 9.7ns with a 10GHz clock, due to the DES interpolation filter
3. An increase in power of 250mW with a 10GHz clock, due to the DES interpolation filter

#### 8.1.4 Eye Scan Procedure

The PHY layer contains features for generating eye diagrams. A variety of different modes are supported (see ES register for list of modes). The following sections describe how to generate eye-scan data from the part and some approaches for building an eye-diagram.

1. Configure the part for JESD204C operation by following the steps in the [Startup Procedure for DUC Mode](#). Return here after setting JESD\_EN=1. Eye-scan can be run with JESD204C bitstreams, but can also work with general PRBS input stimulus. Eye-scan is run on all enabled physical lanes simultaneously.
2. Program [ES](#) to the desired eye-scan mode.
3. If [ES](#) is less than 8, you must program [ESVO](#) to the desired voltage offset. For other modes, the eye-scan logic automatically adjusts the voltage offset of the eye-scan sampler.
4. Program [ESPO](#) to the desired phase offset.
5. Program [ES\\_BIT\\_SELECT](#) to a value from 0 to 19. Eye-scan analyzes every 20<sup>th</sup> received bit (decimate-by-20). [ES\\_BIT\\_SELECT](#) adjusts this decimation phase. For random stimulus, this does not impact the results. If the input has repeating patterns, this can affect the results.
6. Program [ESLEN](#) to the desired number of samples. Higher settings give more consistent results.
7. Set [ECOUNT\\_CLR](#) = 1 then set [ECOUNT\\_CLR](#) to clear the error counter. This step is recommended, but can be skipped if desired (e.g. to add up counts from multiple eye scan runs). This can also be skipped if [ECOUNT](#) won't be used (for modes with ES of 8 or greater)
8. Program [ESRUN](#) = 1 to start the scan.
9. Poll [ESDONE](#) until [ESDONE](#) returns 1 for each of the lanes you want to run eye-scan on.
10. If the selected eye-scan mode modified the eye-scan voltage offset (inner/outer/average modes), read [ESVO\\_S](#) to get the inner/outer/average eye boundary. For other eye-scan modes, read [ECOUNT](#) to return the number of mismatches (or matches) recorded.
11. Program [ESRUN](#) = 0.
12. Return to step 2 to run another eye-scan data collection process. The receiver can remain enabled during multiple iterations of steps 2-12.

There are two basic approaches to build an eye diagram using the eye-scan feature.

1. 1. Fast approach using [ESVO\\_S](#):
  - a. Repeat the procedure above for each valid value of [ESPO](#). For each value of [ESPO](#), run an inner-eye analysis of zeros and ones. This locates the maximum zero ( $ESVO_{max0}$ ) and minimum one ( $ESVO_{min1}$ ) for each value of [ESPO](#).
  - b. All the cells of the eye between  $ESVO_{max0}$  and  $ESVO_{min1}$  (inclusive) can be colored black, and all other cells colored white.
  - c. Additional detail can be added to the eye-diagram by including outer and/or average analysis (see [ES](#)). For example, the [ESVO\\_S](#) values produced from average analysis can be colored red, while all other values between and including the inner and outer values colored white.
2. Detailed approach using [ECOUNT](#):
  - a. select an eye-scan mode that counts mismatches. Repeat the procedure outlined above for each valid value of [ESVO](#) and [ESPO](#).
  - b. After each run, record the value of [ECOUNT](#) (resetting [ECOUNT](#) before each run).
  - c. Each eye-scan run corresponds to one cell of the eye-diagram. [ESPO](#) is the x-coordinate of the cell. [ESVO](#) is the y-coordinate of the cell. The intensity of the cell is proportional to  $ECOUNT/Nsamples$ , where  $Nsamples$  is the number of analyzed samples per run (determined by [ESLEN](#)).
  - d. This approach takes much more time to run, but can provide a more granular eye-diagram.

### 8.1.5 Pre/Post Cursor Analysis Procedure

Pre/Post Cursor Analysis can be used to determine an optimum setting for pre-emphasis in the transmitter.

1. Program [JESD\\_EN](#) = 0 if necessary. Program [EQMODE](#) = 1. Program [JESD\\_EN](#) = 1 and allow sufficient time for the equalizer to adapt and settle. You can read [EQLEVEL\\_S](#) multiple times to verify the value is stable or toggling between adjacent values.
2. Set [EQHOLD](#) = 1 to lock the equalizer (disable adaptation). This also causes [EQOVER](#) and [EQUNDER](#) fields to become low.
3. Wait at least 48UI, and proportionally longer if the CDR activity is less than 100% so the 1 on [EQHOLD](#) is sampled and acted upon. The SPI is slow enough that no explicit delay is necessary.

4. Set **EQMODE** to 2 or 3 to select pre or post cursor analysis respectively. With a separate SPI transaction, set **EQHOLD** = 0. The equalization characteristics of the received signal are analyzed (the equalizer response continues to be locked).
5. Wait at least 150,000UI to allow time for the analysis to occur, proportionately longer if the CDR activity is less than 100%
6. Examine **EQOVER** and **EQUNDER** for results of analysis:
  - a. **EQOVER** high indicates the signal is over equalized;
  - b. **EQUNDER** high indicates the signal is under equalized;
7. Set **EQHOLD** = 1
8. Adjust the transmitter pre-emphasis and repeat steps 3 thru 7 if required.
9. Set **EQMODE** = 1, and with a separate SPI transaction, set **EQHOLD** = 0 to exit analysis mode and return to normal adaptive equalization.

### 8.1.6 Sleep and Disable Modes

There are several methods to power down or temporarily disable the DAC outputs. To prevent asymmetric aging of the device circuits, in some options a low level output from the DACs is maintained. [Table 8-1](#) lists the options for sleep or disabling the DAC outputs.

The most power is saved in full power down, which is enable by setting the **MODE** register to 0x3. In this mode a low level output signal is maintained to prevent asymmetric aging. Returning to full operation from full power down takes 100's of microseconds.

One or both DAC outputs can be disabled by setting the corresponding **MXMODE** register to 0x6. This saves some power and the DAC outputs a low level signal to prevent asymmetric aging. If only one channel is disabled, low level spurs from the disabled channel can feed into the active channel, creating spurs around -80 dBFS.

The TX ENABLE function, either through the **TXEN0/1** balls or **TX\_EN** registers, provides a method to quickly disable the DAC output by forcing the digital code to 0 (midscale) (see [Section 6.9](#) for the TX ENABLE latency). When the **QUITE\_TX\_ENABLE** register is 0, a low level signal is still maintained at the output to prevent saturation. When **QUITE\_TX\_ENABLE** is 1, if data independent DEM and Dither is enable, this prevents asymmetric aging. If DEM and dither are disabled or DEM is set to data dependent DEM, the DAC can degrade over the lifetime of the device if a significant fraction of the lifetime is spent in this mode. The degradation is channel specific, only affecting the channel that is disabled.

**Table 8-1. DAC Sleep and Output Disable Options**

| Option                               | MXMODE | TX_EN | QUIET_TX_DISABLE | DEM  | DITHER | Low level output | long term degradation | Power Savings |
|--------------------------------------|--------|-------|------------------|------|--------|------------------|-----------------------|---------------|
| Device Full Power Down (MODE = 0b11) | -      | -     | -                | -    | -      | yes              | no                    | Most          |
| DAC disable                          | 6      | 1     | -                | -    | -      | yes              | no                    | Some          |
| TX Enable                            | any    | 0     | 0                | -    | -      | yes              | no                    | Least         |
| TX Enable                            | 0-5    | 0     | 1                | 0,1  | 0,1    | no               | no                    | Least         |
| TX Enable                            | 0-5    | 0     | 1                | 2, 3 | 3      | no               | yes                   | Least         |
| TX Enable                            | 6      | 0     | 1                | 0,1  | 0,1    | no               | no                    | Least         |
| TX Enable                            | 6      | 0     | 1                | 2,3  | 3      | no               | yes                   | Least         |

When the DAC is in full power down, the common mode voltage at the DAC output during sleep needs to be maintained below 2V. For AC coupled outputs, the bias is usually provided by an inductor or a balun center tap to 1.8V which forces the common mode also to 1.8V. For DC coupled output, which are typically terminated through a resistor to a voltage above 1.8V (for example, 2.3V), sufficient DAC output current must be provided to reduce the common mode voltage to less than 2V. This is achieved by programming **DACx\_CBIAS\_SLEEP** ([Address 0x724 bits 7:4](#) for DACA and [Address 0x726 bits 7:4](#) for DACB) according to the following equation:

$$DAC\_CBIAS\_SLEEP = \text{ceil} \left( \frac{2 \cdot \frac{V_{BIAS} - V_{OUT\_CM\_SLEEP}}{R_{TERM}} - 7.36mA}{1.47mA} \right) \quad (4)$$

where:

- $V_{OUT\_SLEEP}$  is the DAC output common mode in sleep ( $\leq 2V$ )
- $V_{BIAS}$  is the external DC bias
- $R_{TERM}$  is the external bias resistor/termination to  $V_{BIAS}$
- $\text{ceil}$  is the ceiling operator (integer round up)

## 8.2 Typical Application

### 8.2.1 S-Band Radar Transmitter

#### 8.2.2 Design Requirements

S-band covers a frequency range of 2GHz to 4GHz. For this example, use a radar with signal bandwidth of 200MHz and a center frequency of 3.2GHz.

Doppler radars use the frequency shift in the returned signal to measure the velocity of object. Large reflected signals from for example ground clutter mix with the TX and RX phase noise, which can potentially swamp the return signal from a small moving object. This places a requirement on close in phase noise for the close in phase noise of the radar chirp.

Radars are also sensitive to spurious signals, and for this example, assume 90dBFS is required for the inband SFDR.

#### 8.2.3 Detailed Design Procedure

A summary of the design parameters are listed in [Table 8-2](#). A input sample rate of 250MSPS complex covers the 200MHz signal bandwidth, and interpolation by 32x is used to increase the TX sample rate to 8GSPS. The device's numerically controlled oscillator (NCO) is used to place the signal at the TX output at 3.2GHz. An addition 2x interpolation is applied in DES2XL mode, increasing the sample rate to 16GSPS.

The suppression of the image at 4.7 - 4.9GHz in DES2XL mode would be limited by the 2x DES interpolator to 40dB.

To optimize the low offset frequency phase noise, DEM and dither are disabled.

The JESD204C interface is configured in JMODE 5 with 4 streams (2 IQ pairs) and 1 Serdes lane per IQ pair. With 64/66 bit encoding, the Serdes baud rate is 8.25Gbps.

**Table 8-2. Design Parameters for an S-band Transmitter**

| Parameter               | Value                  |
|-------------------------|------------------------|
| Input Clock             | 8GHz                   |
| DAC Sample Rate         | 16GSPS                 |
| Output Mode             | DES2XL                 |
| DEM and Dither Settings | Off                    |
| TX Interpolation Factor | 32x                    |
| TX Input Rate           | 250MSPS Complex        |
| NCO frequency           | 3.2GHz                 |
| JMODE                   | 5                      |
| # Streams               | 4 (2x IQ pairs, 1/DAC) |
| # Serdes Lanes          | 2                      |
| Encoding                | 64/66                  |
| Serdes Baud Rate        | 8.25Gbps               |

## 8.2.4 Detailed Clocking Subsystem Design Procedure

One of the major advantages of the DDS39RF12 and 'RFS12 in applications like Doppler radar, Quantum Computing and Wireless Test is the ability to directly synthesize very low phase noise signals all the way through X-band (12GHz). To take full advantage of the exceptionally low additive phase noise of the DAC, a high-performance clock is required.

Equally important in most systems is the impact of Size, Weight, Area, Power and Cost (SWAP-C). This means each system architect must weight tradeoffs in performance vs. overall system SWAP-C based on system requirements. This section presents three clocking examples based on SWAP-C vs. performance tradeoffs.

Figure 8-6 shows a plot of phase noise for an 8GHz sample clock produced by an integrated PLL+VCO, integrated PLL with external high performance VCO and a fully discrete high performance analog PLL. All examples assume a reference clock is provided as an input to the synthesizer, which can range from low cost surface mount crystal oscillators all the way to expense reference subsystems. The DDS39RF12 and 'RFS12 additive phase noise at 8GHz is also provided for comparison, even for the analog PLL, the clock phase noise degrades the DDS39RF12 and 'RFS12 output phase noise for offset frequencies below 5MHz.

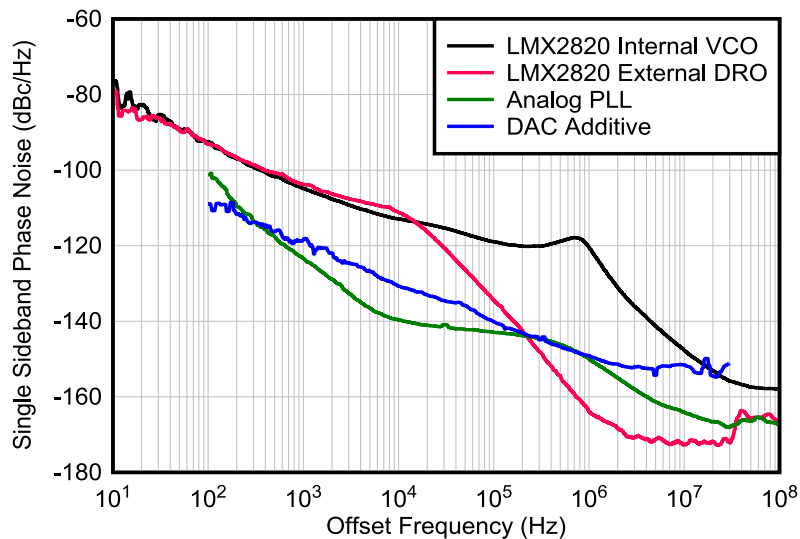


Figure 8-6. Phase Noise of DAC Clock Examples with the Device Additive Phase Noise

### 8.2.4.1 Example 1: SWAP-C Optimized

The best SWAP-C sub-system leverages the high levels of integration offered by modern PLL+VCO devices, such as the LMX2820. Figure 8-7 shows a block diagram of the clocking sub-system. An external reference clock feeds the LMX2820 input, which is then used to lock the internal PLL+VCO before being fed to the output buffers. Only external passives are required to construct the loop filter and complete the sub-system system.

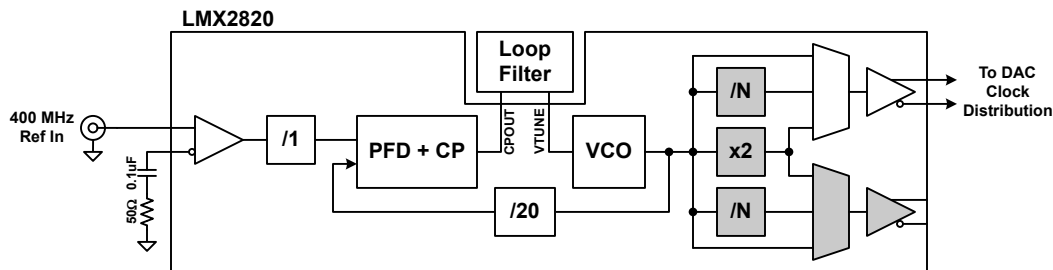


Figure 8-7. LMX2820 with Internal VCO

The LMX2820 is a flexible device and configuration can be overwhelming. For example, deciding how to decipher configure dividers, set loop filter components, and so on. A few high-level guidelines can be taken into consideration to optimize phase noise.

First, always operate the LMX2820 in integer mode when possible, as opposed to fractional mode. This implies that relationship between reference clock and output clock follows the general form:

$$F_{OUT} = (F_{REF}/N_{REF}) \times N_{DIV}/N_{OUT} \quad (5)$$

where  $N_{REF}$ ,  $N_{DIV}$  and  $N_{OUT}$  are the reference, feedback and output dividers respectively.  $F_{REF}$  is the input reference frequency and  $F_{OUT}$  is the output frequency used as the DAC clock. If this ratio cannot be found, then fractional mode must be used at the expense of degraded overall phase noise.

Second, the best in-band phase noise is achieved when the phase detector frequency is maximized and the feedback divider is minimized. The LMX2820 has a maximum phase detector frequency of 400MHz and an optional reference doubler is available for reference inputs up to 200MHz. For the same output frequency, each doubling of phase detector frequency (while halving the feedback divider) results in 3dB of in band phase noise reduction.

For an 8GHz output, use the maximum phase detector frequency of 400MHz. Set  $N_{REF} = 1$ ,  $N_{DIV} = 20$ , and  $N_{OUT} = 1$  (divider bypass). For a slight degradation in in-band noise, the input can be set to 200MHz and the reference doubler is used.

Third, note that any noise on the reference input impacts close in phase noise before the in-band noise begins to dominate. In-band noise is a combination of PLL noise (phase detector, charge pump and dividers) and VCO noise, while wideband noise is limited by the noise floor of the output buffers. Close in noise is limited by the device flicker, which is independent of phase detector frequency and scales  $20 \times \text{LOG}_{\text{base}10}$  with output frequency.

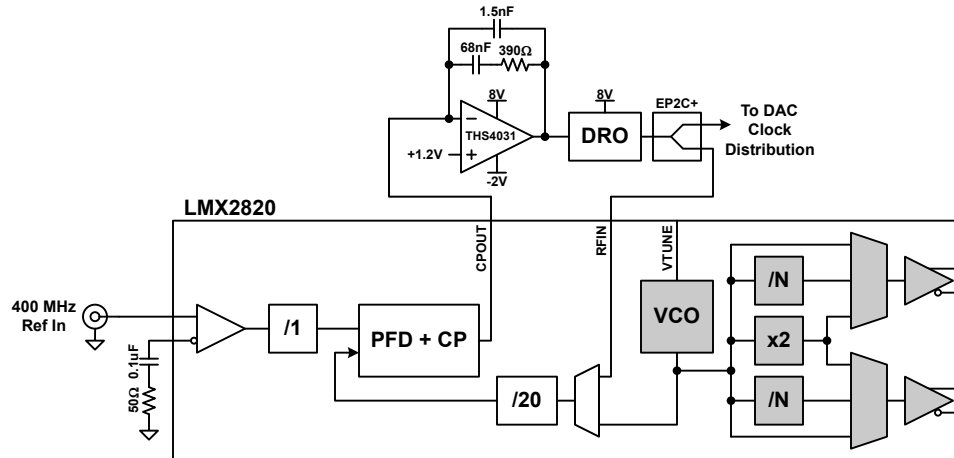
Finally, when operating the LMX2820 above 11GHz, the integrated output doubler must be used and this results in a sub-harmonic (that is, output frequency divided by 2) that possibly requires external filtering using either a high-pass or bandpass filter (depending on system requirements). Following the LMX2820 output with a narrow bandpass filter can also be used to suppress wideband noise.

The [PLLatinumSim](#) software is available from TI to design the external loop filter passive values.

#### 8.2.4.2 Example 2: Improved Phase Noise LMX2820 with External VCO

An external VCO can significantly improve in-band and wideband noise, with best phase noise typically achieved with narrow band VCOs such as Voltage Controlled Crystal Oscillators (VCXO), Voltage Controlled Surface Acoustic Wave Oscillators (VCSO) and Dielectric Resonance Oscillators (DRO). For this design, a Synergy Microwave 8GHz DRO (SDRO800-8), is used for the wideband noise (-170dBc/Hz) and low flicker noise corner (-160dBc/Hz at 1MHz). DROs are typically available from about 5 to over 25GHz.

[Figure 8-8](#) shows a block diagram of the synthesizer. An external active loop filter is used to improve noise performance and extend the tuning voltage range required for the DRO (0 to 10V). The DROs output is split, with one output feeding back into the LMX2820 and the other being sent to the DAC clock distribution network.



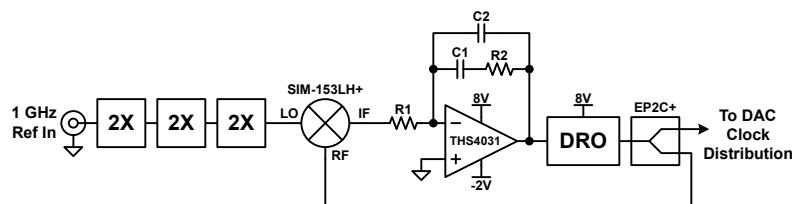
**Figure 8-8. External LMX2820 with an External VCO**

In this implementation, the loop bandwidth was set to around 24kHz, where the flicker noise of the PLL intersects the open loop noise of the DRO. This offers the best overall integrated phase noise. The noise floor is improved by about 10dB from the fully integrated example since the output buffers were not used and the DRO has exceptional broadband noise of around -170dBc/Hz.

As with the integrated VCO, the loop filter components can be designed using [PLLatinumSim](#) software.

#### 8.2.4.3 Example 3: Discrete Analog PLL for Best DAC Performance

When phase noise performance is paramount, a discrete analog PLL (APLL) offers substantially lower phase noise than the integrated examples. The trade off is increased SWAP-C. [Figure 8-9](#) shows the block diagram of such an implementation that uses the same Synergy Microwave 8GHz DRO as the LMX2820 external VCO example discussed previously.

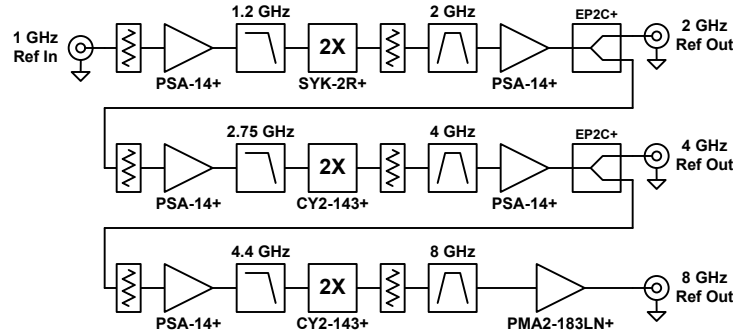


**Figure 8-9. Discrete Analog PLL**

The APLL outperforms the previous examples by avoiding use of digital dividers and phase detectors, which significantly degrade phase noise. Instead passive diode-based frequency multipliers and mixers are used, which contribute little additive phase noise. Like all synthesizers, a frequency reference with very good close in phase noise, below the loop bandwidth of the APLL, is required for best performance.

In this case, a 1GHz reference was chosen as the reference is a convenient division of the sample rate and is available either as an output of an R&S SMA100B RF signal generator or as a standalone unit from Wenzel Associates.

As mentioned previously, the APLL does not use digital dividers or phase detectors, which significantly degrade phase noise. Instead the reference is multiplied up to the output frequency using passive multiplier stages (see [Figure 8-10](#)). A passive mixer is used as a phase detector that feeds a low noise operational amplifier loop filter. The DRO output is split with one output going to the DAC clock distribution network and the other feeding back into the RF port of the mixer.



**Figure 8-10. Reference Multiplier Chain**

The multiplier chain uses low noise amplifiers, passive diode multipliers and bandpass filters. For this part of the circuit, what is most critical is the close in phase noise below the loop bandwidth of the PLL. Not all amplifiers demonstrate good close in noise, especially when driven near or into compression. Generally, heterojunction bipolar transistor (HBT) amplifiers, have low flicker noise and operate well when driven into compression.

Bandpass filters were selected to remove the  $F_{IN}$  and  $3 \times F_{IN}/2$  harmonics that are only partially suppressed by the multipliers. In some implementations the driving amplifier can be filtered to prevent degradation of the harmonic suppression performance. This chain was experimentally optimized, but additional attenuation between stages can be added to manage reflections and amplifier operating conditions.

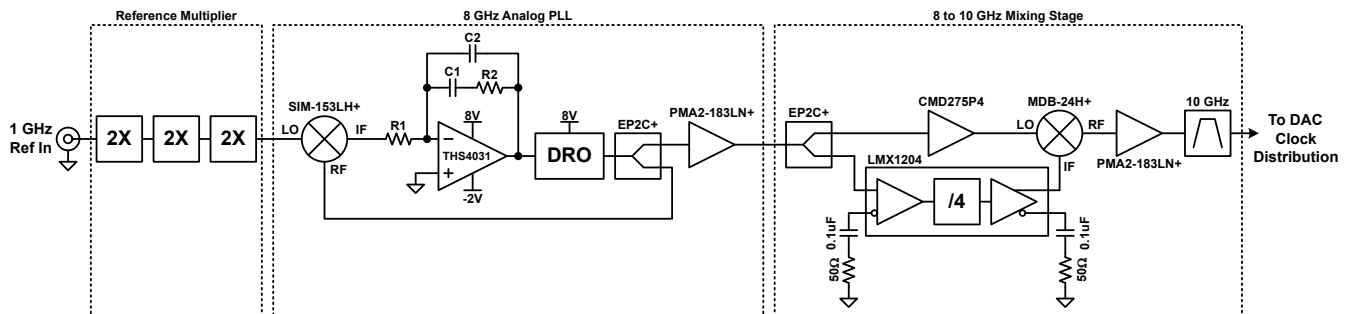
The loop filter bandwidth is set near where the open loop DRO phase noise crosses the multiplied reference noise with a damping factor set to give a smooth roll off that minimizes integrated phase noise. An optional additional feedback cap can be used to speed up the roll off if desired (C2 is set roughly to  $1/10^{\text{th}}$  to  $1/100^{\text{th}}$  of C1). The loop filter component values were determined experimentally for this design.

In some implementations a start-up circuit is needed to help the loop acquire lock. In practice, the initial power up was all that is needed for the loop to pull in and lock.

#### 8.2.4.4 10GHz Clock Generation

For higher sample rates several options are available. First, a DRO can be selected that operates directly at the desired frequency and the multiplier chain and or reference frequency can be modified accordingly.

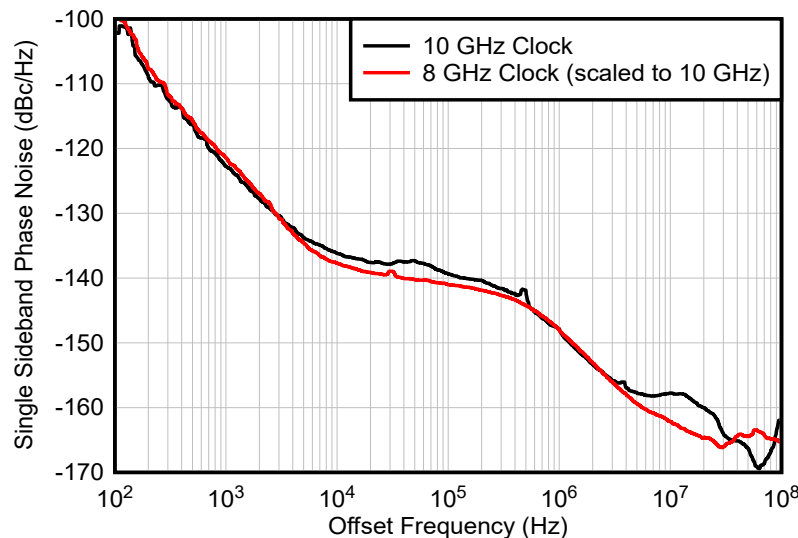
An alternative is to use dividers and mixers to translate the APLL output to a new higher frequency. Figure 8-11 shows an example for a 10GHz clock synthesizer. This uses the same reference multiplier chain and APLL as described above and adds a mixing stage to translate the DAC clock from 8 to 10GHz.



**Figure 8-11. 10GHz Clock Synthesizer**

The LMX1204 can operate as a buffer, multiplier or divider. In this case the LMX1204 is used to divide the 8GHz APLL output by 4, which is then mixed with the input to translate the clock to 10GHz. A bandpass filter is required after mixing to remove the LO feedthrough and undesirable mixing products. Figure 8-12 shows the input 8GHz scaled to 10GHz and resulting 10GHz after mixing.

As with the reference multiplier chain, special care must be taken selecting the components and operating points for best phase noise. A slight improvement in noise floor was found by power combining two the of the LMX1204 outputs before feeding the IF input of the mixer.



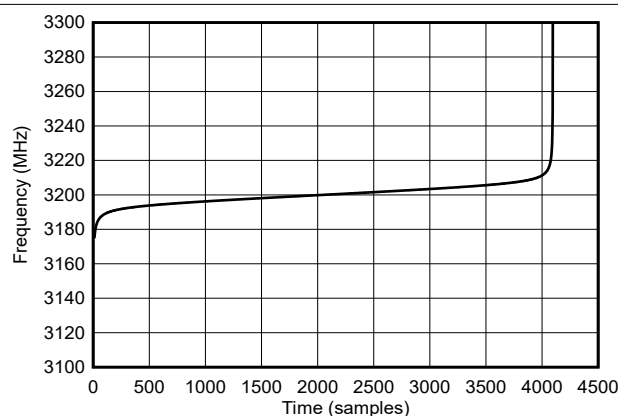
**Figure 8-12. 8GHz and 10GHz Clock Phase Noise**

### 8.2.5 Application Curves

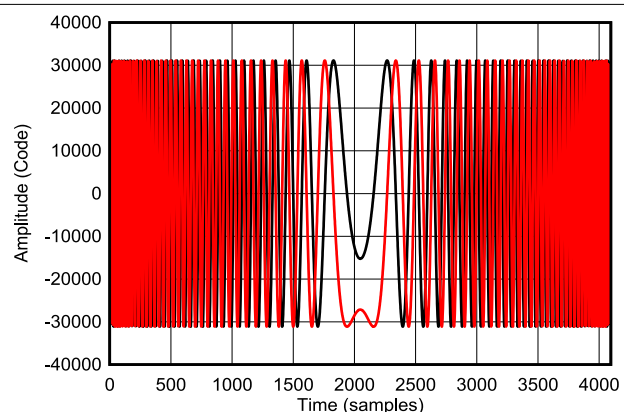
The radar chip waveform used for testing is a non-linear frequency modulated (NLFM) pulse, lasting 4096 samples at the 250MSPS complex input rate. At baseband, the frequency ramps from -100MHz to + 100MHz, following a frequency ramp curve developed by Price and shown in Equation 6 [Price R. *Chebyshev Low Pulse Compression Sidelobes via a Nonlinear FM*. National Radio Science Meeting of URSI; PortSaid, Egypt: 1979.] with  $T = 4096$  samples,  $B = 0.8$ ,  $B_l = 0.5611$  and  $B_c = 0.238$ .

$$f(f, B_l, B_c) = B \times \frac{t - T/2}{T} \times \left( B_l + \frac{B_c}{\sqrt{1 - 4(t - T/2)^2 / T^2}} \right) \quad (6)$$

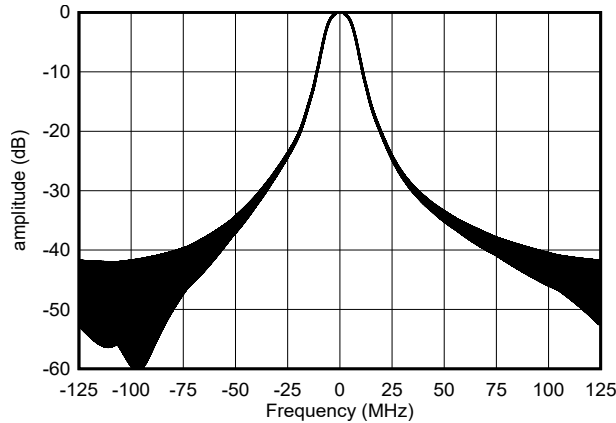
The NLFM Chirp frequency ramp is shown in Figure 8-13, complex time domain baseband waveform in Figure 8-14, baseband frequency spectrum in Figure 8-15 and auto-correlation in Figure 8-16.



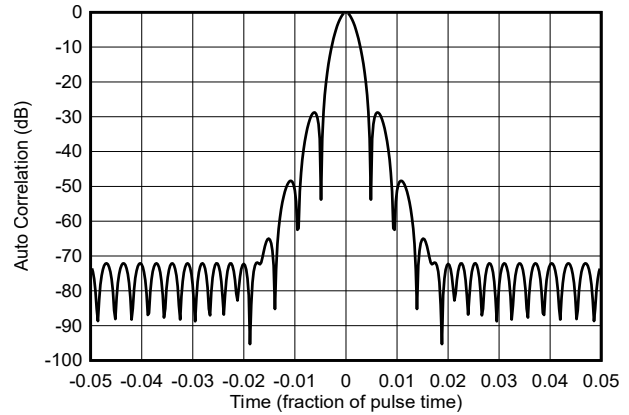
**Figure 8-13. NLFM Frequency Ramp**



**Figure 8-14. Complex Time Domain of NLFM Chirp (Red = real, Black = imag)**

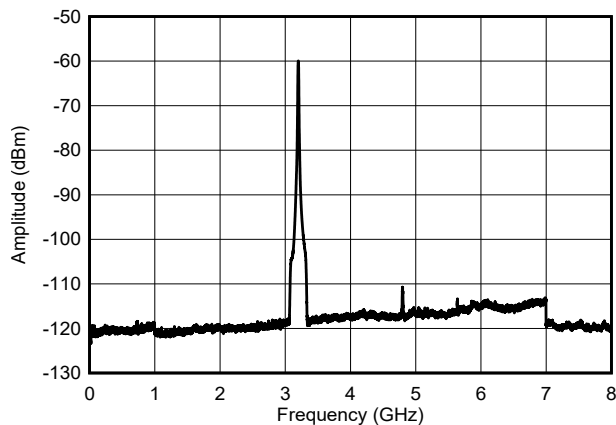


**Figure 8-15. Digital Spectrum for NLFM Chirp**

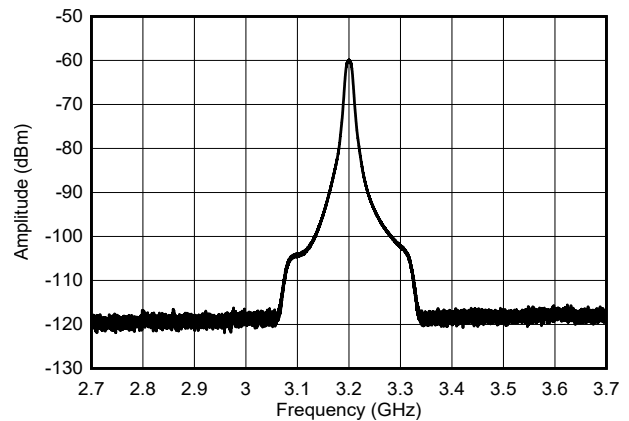


**Figure 8-16. Auto-correlation of NLFM Chirp**

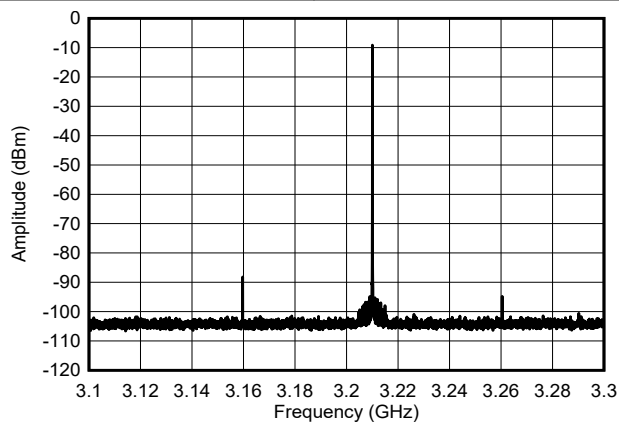
The output spectra for the NLFM Chirp at 3.2GHz is shown in [Figure 8-17](#). The largest spur is the duty-cycle image at 4.8GHz, which is suppressed 50dB. [Figure 8-18](#) shows a 1 GHz span centered at 3.2GHz. the interpolation filters confine the output spectrum to a 250MHz wide band at 3.2GHz. The spectra purity of the 200MHz is shown with a fullscale tone in [Figure 8-19](#). The largest spurs are ~ 80dBc at 3.16GHz, which is the 4<sup>th</sup> harmonic (aliased back into 1<sup>st</sup> Nyquist zone), and the 6<sup>th</sup> harmonic at ~ 86dBc.



**Figure 8-17. NLFM Chirp Output Spectra across 0 - 8GHz**



**Figure 8-18. NLFM Chirp Output Spectra across 1GHz**



**Figure 8-19. In Band Single Tone Frequency Spectra with  $f_{OUT} = 3.211\text{GHz}$**

The output phase noise for a tone at 3.2GHz using the recommended clocking circuit is shown in [Figure 8-20](#). The additive phase noise for the DAC by itself is shown in [Figure 8-21](#).

**Figure 8-20. Output Phase Noise at 3.2GHz using Recommended Clock Circuit**

**Figure 8-21. DAC Additive Phase Noise at 3.2GHz**

### 8.3 Power Supply Recommendations

The device has three supply voltages and requires seven supply domains to achieve data sheet performance as shown in [Table 8-3](#):

**Table 8-3. Recommended Power Supply Domains**

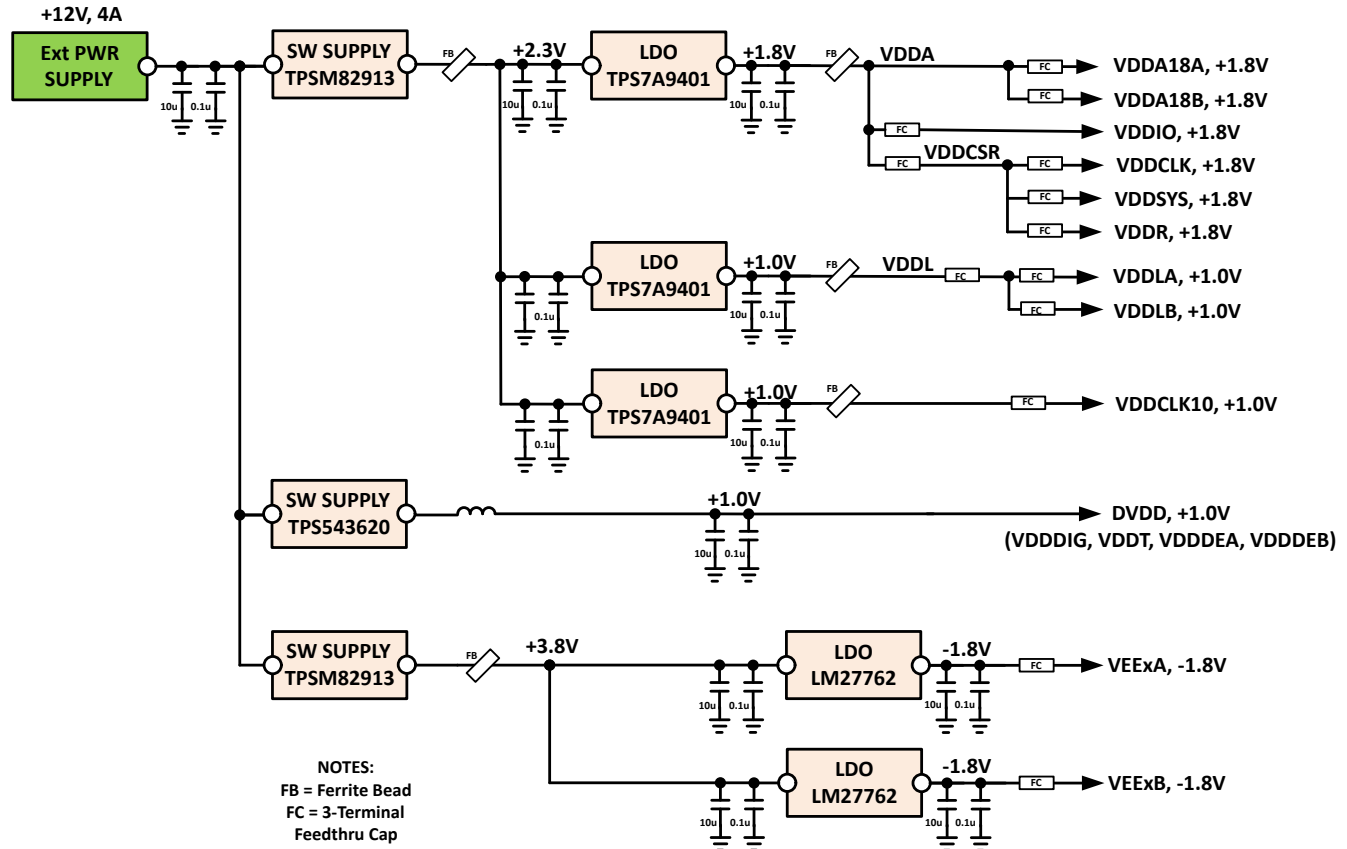
| Voltage | Supply Domain | Device Supplies                 |
|---------|---------------|---------------------------------|
| +1.8V   | VDDA          | VDDA18A, VDDA18B                |
|         | VDDIO         | VDDIO                           |
|         | VDDCSR        | VDDCLK, VDDSYS, VDDR            |
| +1V     | VDDL          | VDDLA, VDDLb                    |
|         | VDCCCLK       | VDDCLK10                        |
|         | DVDD          | VDDDIG, VDDT, VDDDEA and VDDDEB |
| -1.8V   | VEEx          | VEEAM18, VEEBM18                |

The recommended power supply is shown in [Figure 8-22](#). The power-supply voltages must be low in noise and provide the needed current to achieve rated device performance. A step down high-efficiency switching converter is used first, followed by a second stage of regulation using LDOs to provide switching noise reduction and improved voltage accuracy. The user can also refer to the TI WEBENCH® Power Designer which can be used to select and design the individual power supply elements as needed. The recommended switching regulators are:

- TPSM82913 = +2.3V for the VDDA, VDDIO, VDDCSR, VDDL and VDCCCLK domains
- TPS543620 = +1V for DVDD
- TPSM82913 = +3.8V for VEEEx domain

and recommended LDOs include:

- TPS7A9401 for +1.8V and +1V
- LM27762 for -1.8V



**Figure 8-22. Recommended Power Supply Block Diagram**

The VDDA supply is regulated by an LDO, or low-noise drop-out linear regulator, with a +1.8V output and is further broken down into the following subgroup power domains:

- VDDA: VDDA18A, VDDA18B
- VDDIO
- VDDCSR: VDDCLK, VDDSYS, VDDR

Each device supply can be tied to a single LDO but are isolated with a ferrite bead and/or three-terminal capacitor or similar.

The VDDL supply is +1V and is further broken down into VDDL A and VDDL B. Each device supply can be tied to a single LDO but are isolated with a ferrite bead and/or three-terminal capacitor or similar.

The VDDCLK10 supply is +1V and is the most sensitive for achieving the best phase noise performance. VDDCLK10 should be isolated to a LDO by itself to prevent noise from other 1.0V supplies coupling into the clock path.

The DVDD supply is +1V and can be directly connected to a switching power supply. The DVDD encompasses the following device supplies, VDDDIG, VDDT, VDDDEA and VDDDEB, which can all be connected together. No further isolation with a ferrite bead and/or three-terminal capacitor or similar is required.

The VEEx supply is -1.8V derived from a single LDO and is further broken down into VEEAM18 and VEEBM18, which are isolated with a ferrite bead and/or three-terminal capacitor or similar.

It is also highly recommended to follow these important power supply design considerations:

1. Decouple all power supply rails and bus voltages as they come onto the system board. Further place additional decoupling at or near the DAC itself for each power domain. Typically, one decoupling capacitor per power supply pin is suffice unless specified in the data sheet or EVM assembly.
2. Remember that approximately 20dB/decade noise suppression is gained for each additional filtering stage.

3. Decouple for both high and low frequencies, which might require multiple capacitor values.
4. Series ferrite beads and feed through capacitors are commonly used at the power plain entry point and can be used for addition power domain isolation. This should be done for each individual supply voltage on the system board whether it comes from an LDO or a switching regulator.
5. For added capacitance, use tightly stacked power and ground plane pairs ( $\leq 4$  mil spacing) this adds inherent high-frequency ( $>500\text{MHz}$ ) decoupling to the PCB design.
6. Keep supplies away from sensitive analog circuitry such as the front-end RF stage of the DAC and high-speed clocking and digital circuits if possible.
7. Keep power domains that demand higher currents, near the top of the stack-up or layer that has power plain entry point. This minimizes the overall loop inductance.
8. Any open or voided areas on power plane, fill with ground to provide additional isolation and shielding.
9. Keep a 20 to 25 mil gap between all adjacent power and/or ground plane fills. This helps eliminate all gap coupling between adjacent power domains and/or grounds within the same layer.
10. Some switcher regulator circuitry/components could be located on the opposite side of the PCB for added isolation.
11. Follow the IC manufacture recommendations; if they are not directly stated in an application note or data sheet, then study the evaluation board. These are great vehicles to learn from. Applying these points above can help provide a solid power supply design yielding data sheet performance in many applications.

Each application has different tolerances for noise on the supply voltage, so understanding these trades is best described in the following two application notes for more details:

- [Clutter-free power supplies for RF converters in radar applications \(Part 1\)](#)
- [Clutter-free power supplies for RF converters in radar applications \(Part 2\)](#)

Also refer to [Figure 8-30](#) through [Figure 8-33](#) to illustrate the one power supply layout and stack-up approach.

### 8.3.1 Power Up and Down Sequence

At power up, ramp up the power supplies in the following order:

1. Ramp 1.8V supplies, including the bias voltage for DACOUTA+/- and DACOUTB+/-
2. Ramp -1.8V supplies
3. Ramp 1V supplies

Use the reverse order for ramp down.

1. Ramp down 1V supplies
2. Ramp down -1.8V supplies
3. Ramp down 1.8V supplies, including the bias voltage for DACOUTA+/- and DACOUTB+/-

## 8.4 Layout

### 8.4.1 Layout Guidelines and Example

There are many critical signal connections that require specific care and attention during PC board design:

1. DAC analog output signals
2. Sampling clock
3. Serdes (JESD204x) data inputs
4. Power supplies
5. Power and grounding strategy

There are many considerations to take note of when developing a high-speed PCB design. Here are a few recommendations and example figures to follow for any high-speed PCB design:

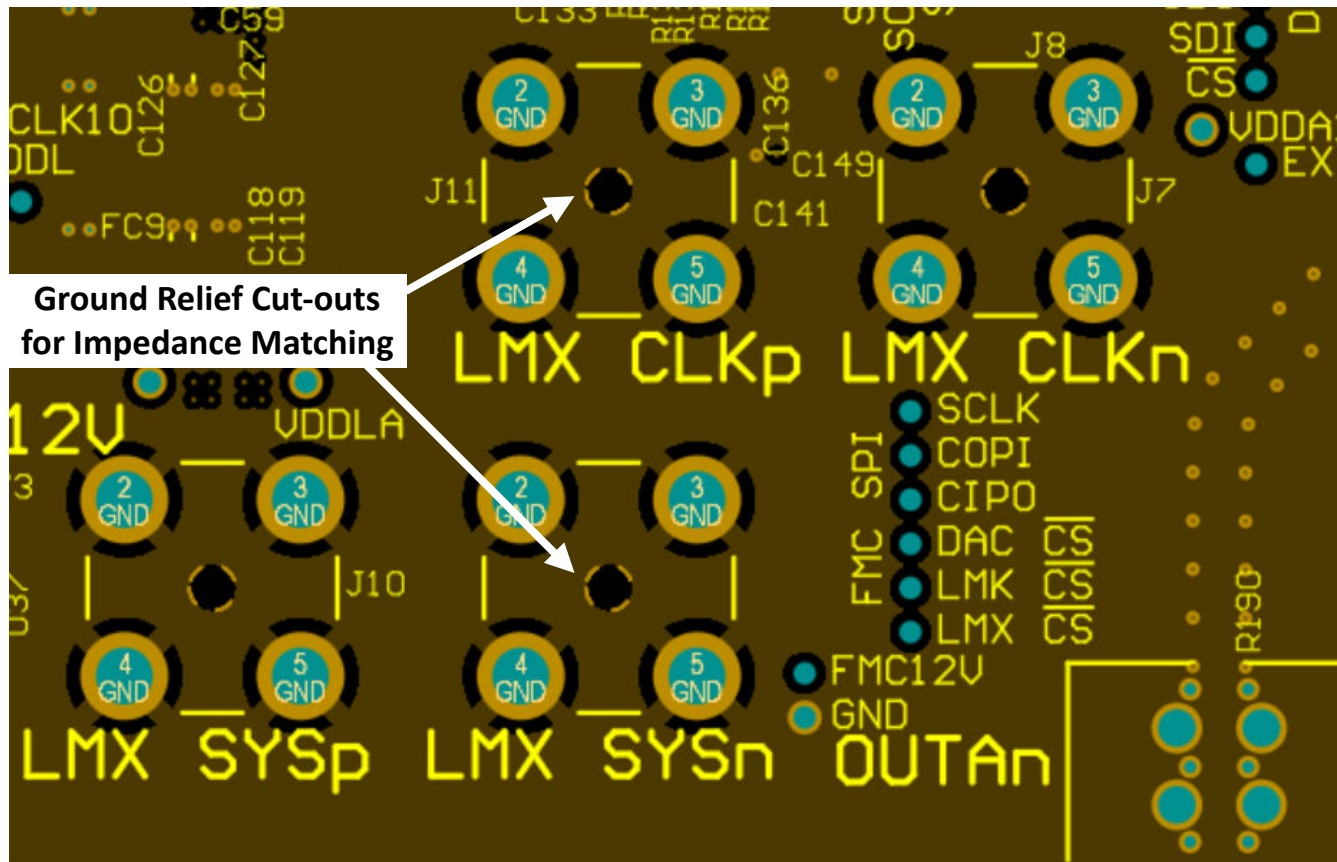
1. Route using loosely coupled 100Ω differential traces when possible on the Serdes inputs. This routing minimizes impact of corners and length-matching serpentine on pair impedance.
2. Provide adequate pair-to-pair spacing to minimize crosstalk, especially with loosely coupled differential traces. Tightly coupled differential traces can be used to reduce self-radiated noise or to improve neighboring trace noise immunity when adequate spacing cannot be provided.
3. Provide adequate ground plane pour spacing to minimize coupling with the high-speed traces. Any ground plane pour must have sufficient via connections to the main ground plane of the board. Do not use floating or poorly connected ground pours.
4. Use smoothly radiused corners and avoid 45- or 90-degree bends to reduce impedance mismatches on all high-speed inputs/outputs for both analog and digital signal traces. See [Figure 8-23](#) as an example.



5. Incorporate any ground plane cutouts necessary at component landing pads, ie – SMA connectors, baluns, and so on, to avoid impedance discontinuities at these locations. Cut-outs below these landing pads on one or multiple ground planes to achieve a pad size or stackup height that achieves the needed  $50\Omega$ , single-ended impedance. See [Figure 8-24](#) and [Figure 8-25](#) as an examples.



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**Figure 8-25. Ground Cut-out Below SMA Connector Center Pin**

6. Avoid routing traces near irregularities in the reference ground planes. Irregularities include cuts in the ground plane or ground plane clearances associated with power and signal vias and through-hole component leads.
7. Provide symmetrically located ground tie stitching vias adjacent to any high-speed signal at an appropriate spacing as determined by the maximum frequency the trace transports ( $\lambda/4$ ). See [Figure 8-23](#) as an example.
8. When high-speed signals must transition to another layer using vias, transition as far through the board as possible (top to bottom is best case) to minimize via stubs on top or bottom of the vias. If layer selection is not flexible, use back-drilled or buried, blind vias to eliminate stubs. Always place two ground vias (“return vias”) close to critical high-speed signal trace via when transitioning between layers to provide a nearby ground return path. See [Figure 8-26](#) and [Figure 8-27](#) as examples.

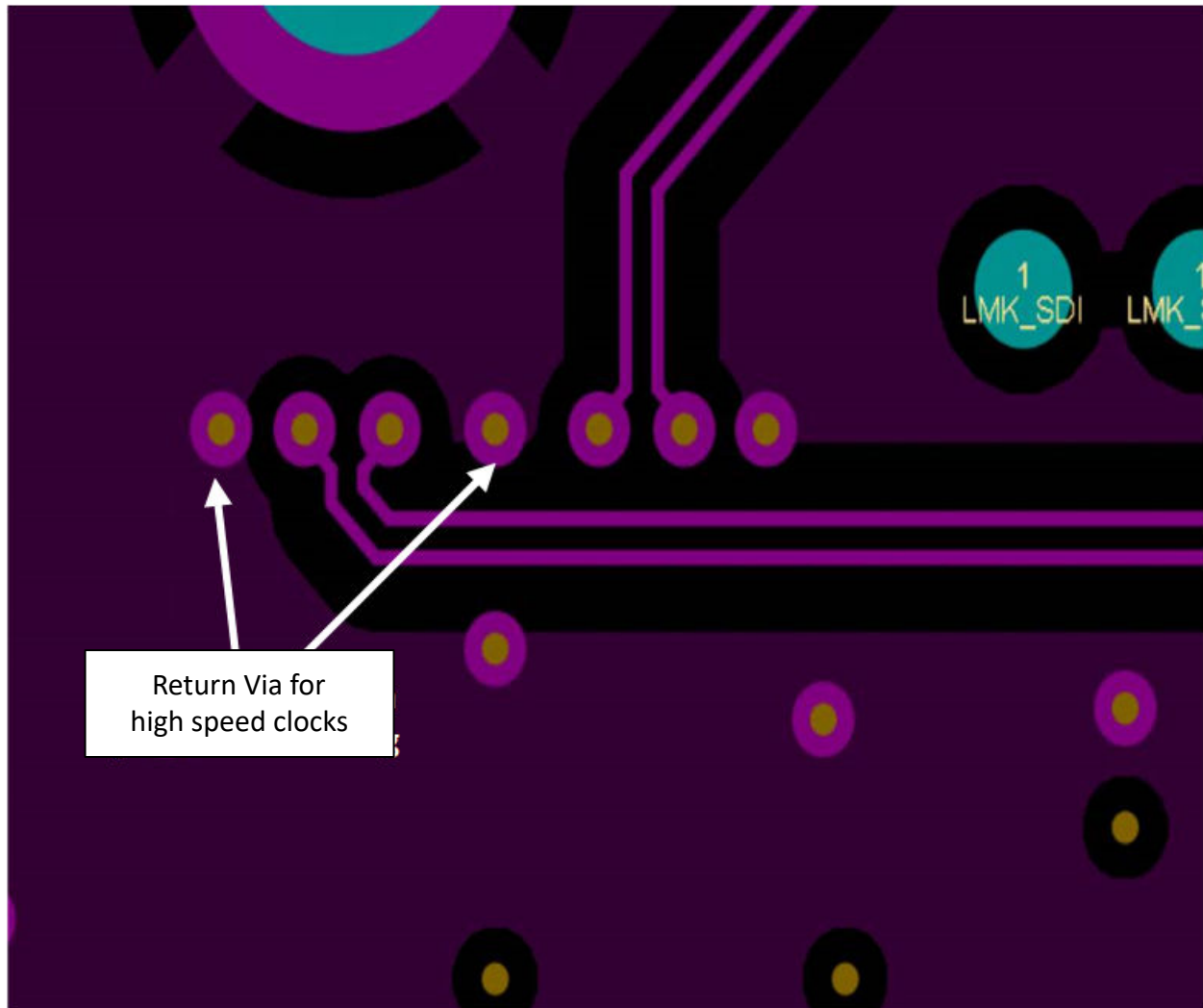
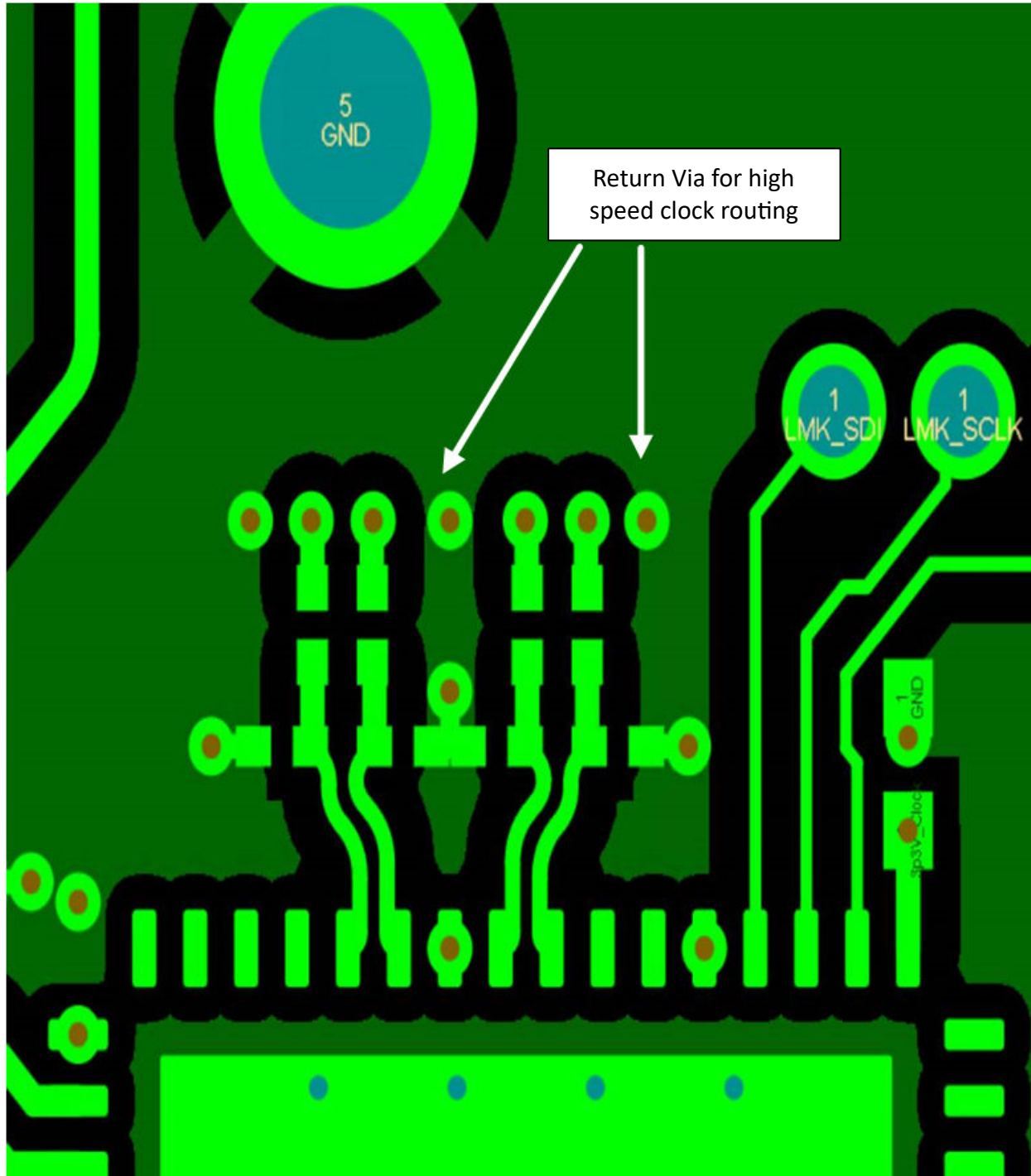


Figure 8-26. Return Vias for High Speed Clock



**Figure 8-27. Return Vias for High Speed Clock Near Clock Generator**

9. Pay particular attention to potential coupling between JESD204x data input routing and the analog output routing. Switching noise from the JESD204x inputs can couple into the analog output traces and show up as wideband noise due to the high bandwidth of the DAC. Route the Serdes JESD204x data inputs on a separate layer, if possible, from the DAC output traces to avoid noise coupling, see [Figure 8-28](#) and [Figure 8-29](#) as examples.

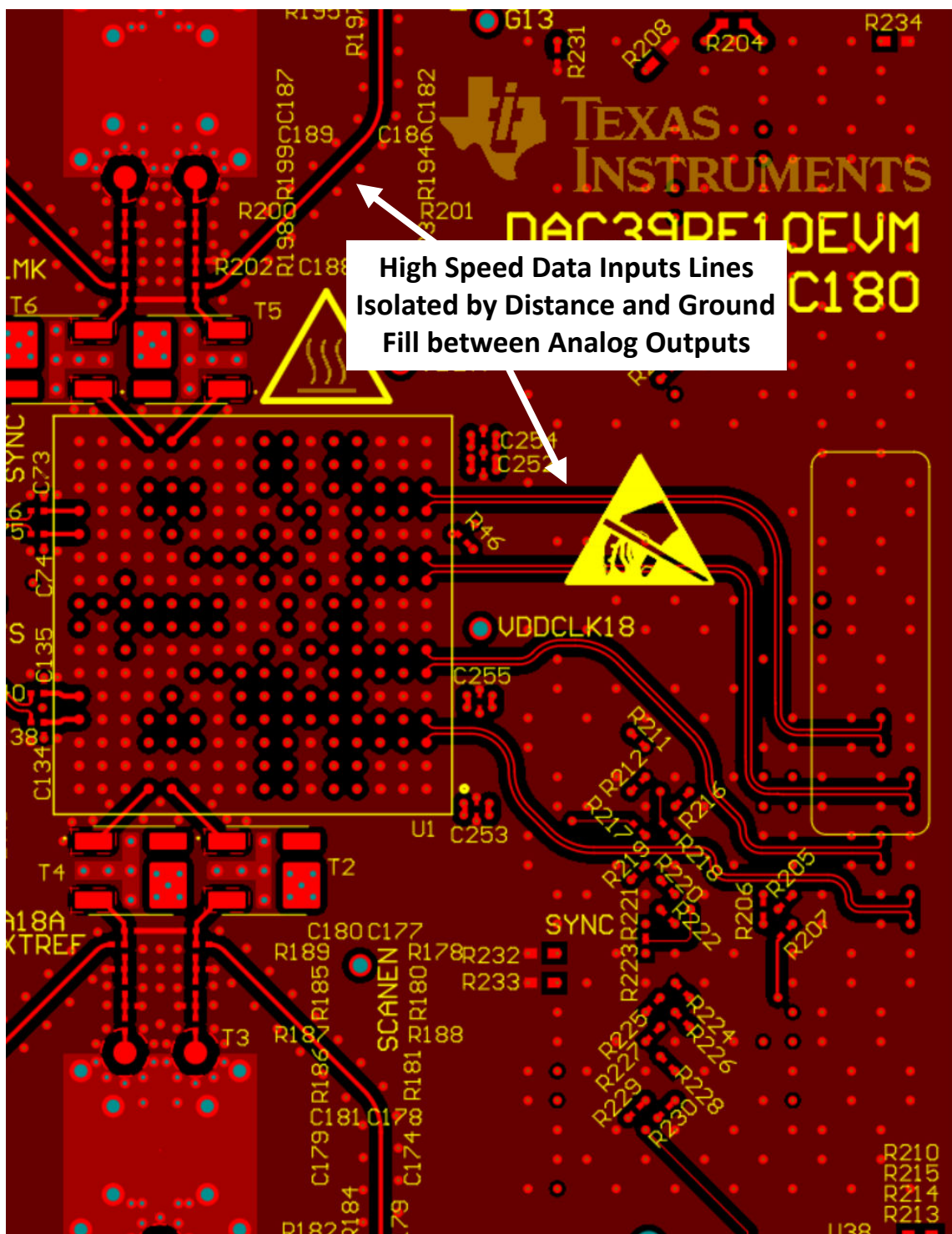
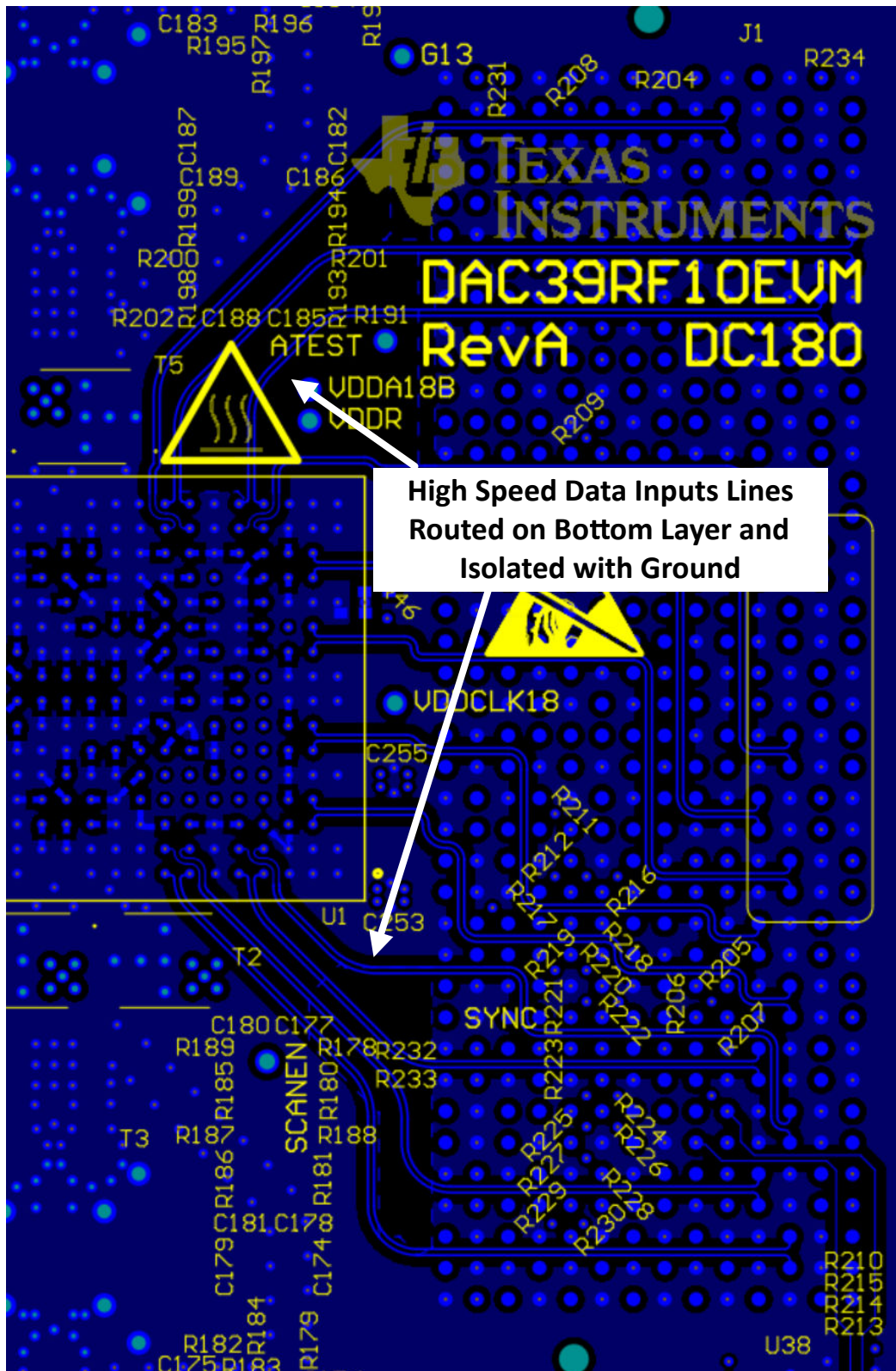


Figure 8-28. Serdes Top Layer Routing with Ground Fill Isolation

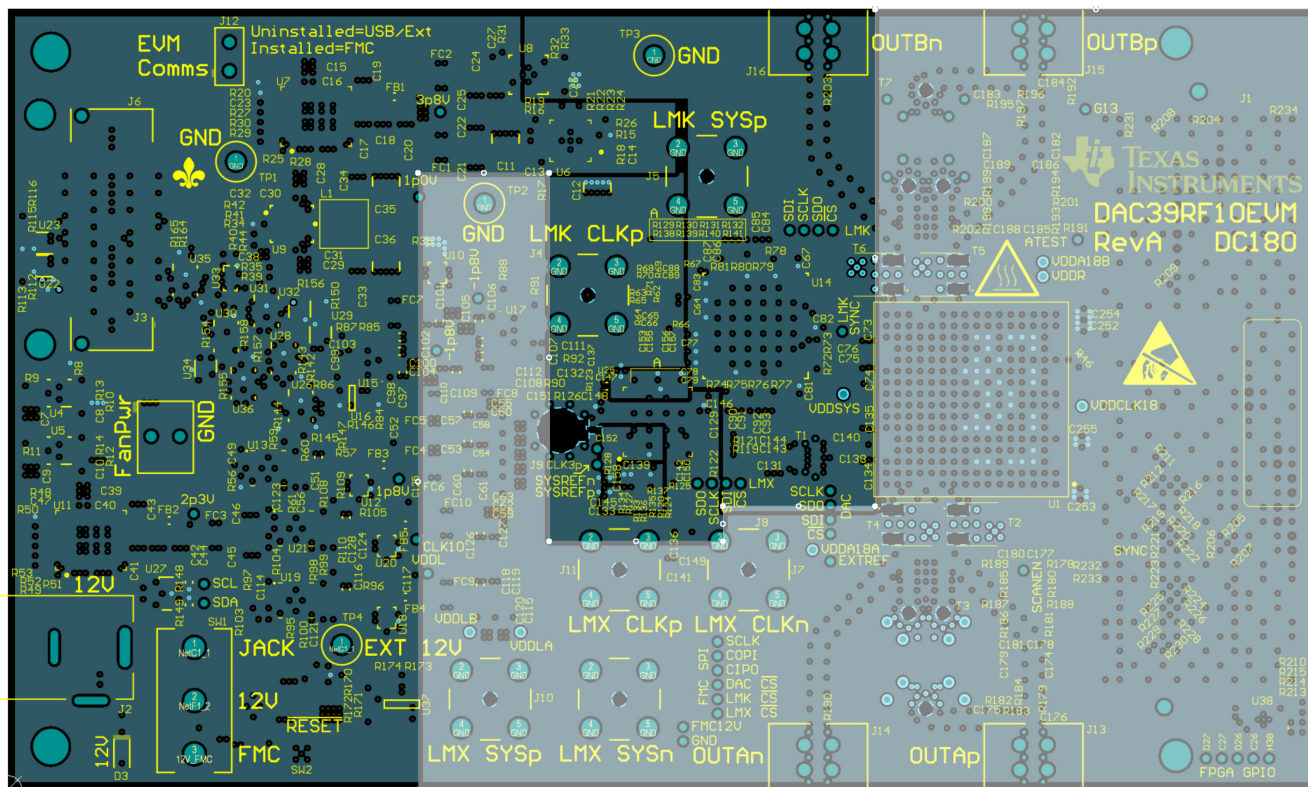


**Figure 8-29. Serdes Bottom Layer Routing with Ground Isolation**

10. A reduction in the clock amplitude can degrade the DAC noise performance, so make sure the clock signal has adequate drive strength, especially for high frequencies. To help avoid this, keep the clock source close to the DAC if using a passive balun to drive or interface with the sampling clock pins of the converter. If trace

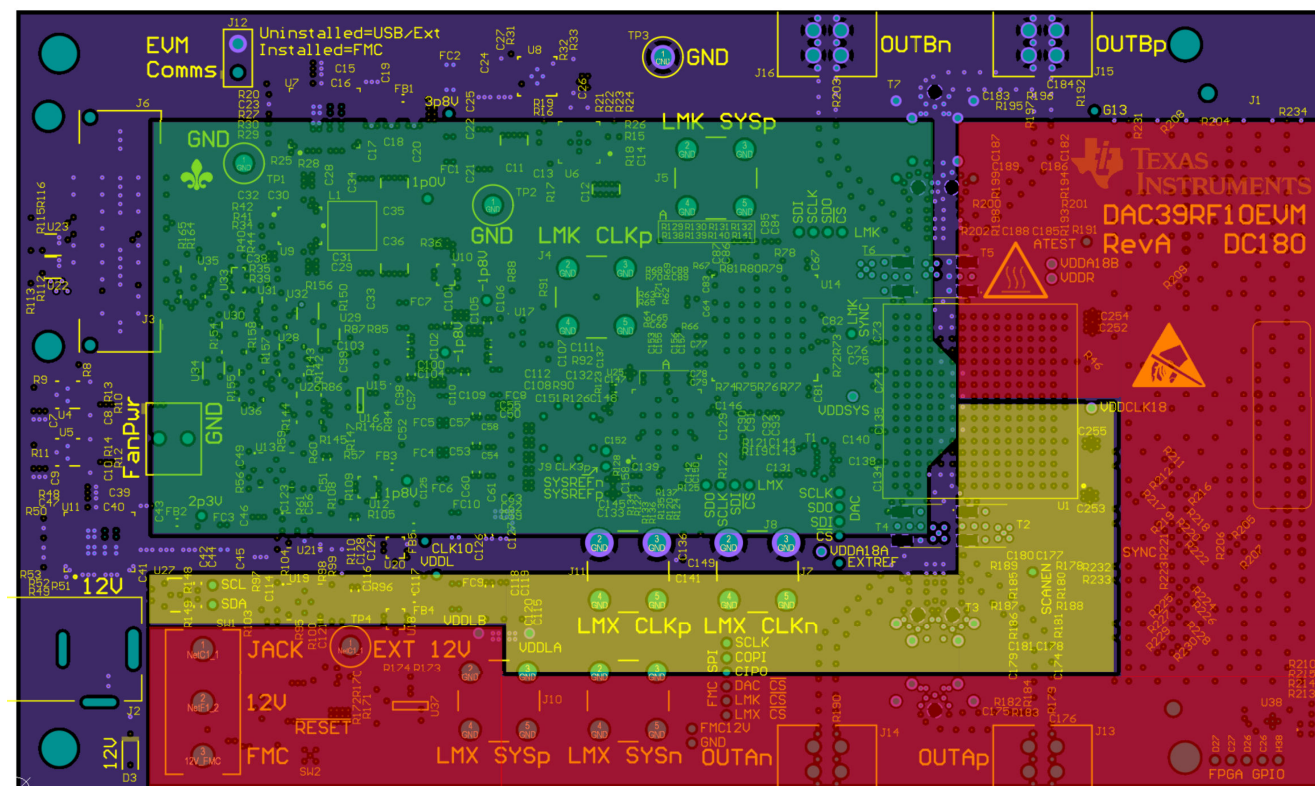
routes are longer than a few inches, impedance matching at the DACs sampling clock input pins can be necessary.

Examples of the power plane design is show in [Figure 8-30](#) through [Figure 8-33](#).



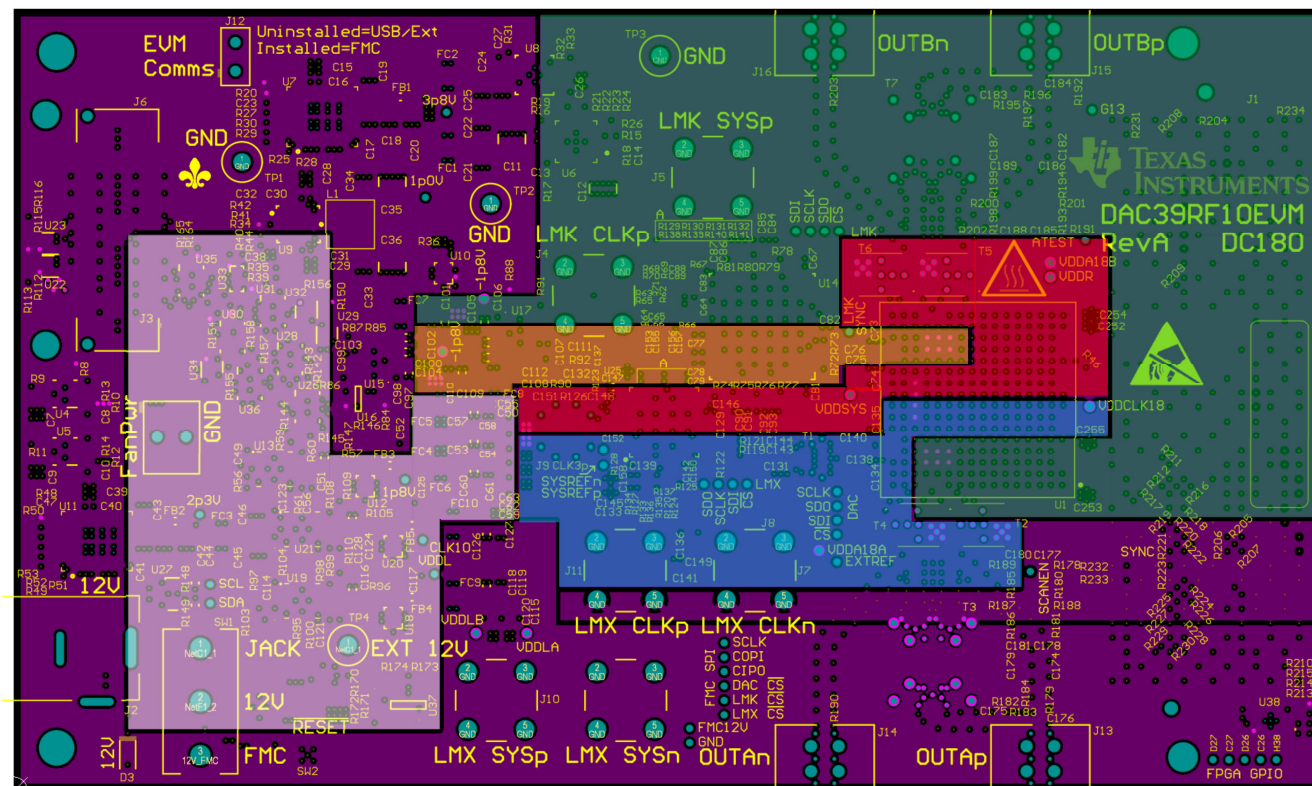
**Layer3 / PWR1**  
**DAC DVDD = WHITE**  
**Other PWR Planes = AUX Supplies**

**Figure 8-30. Power Plane Layout for Layer 3**

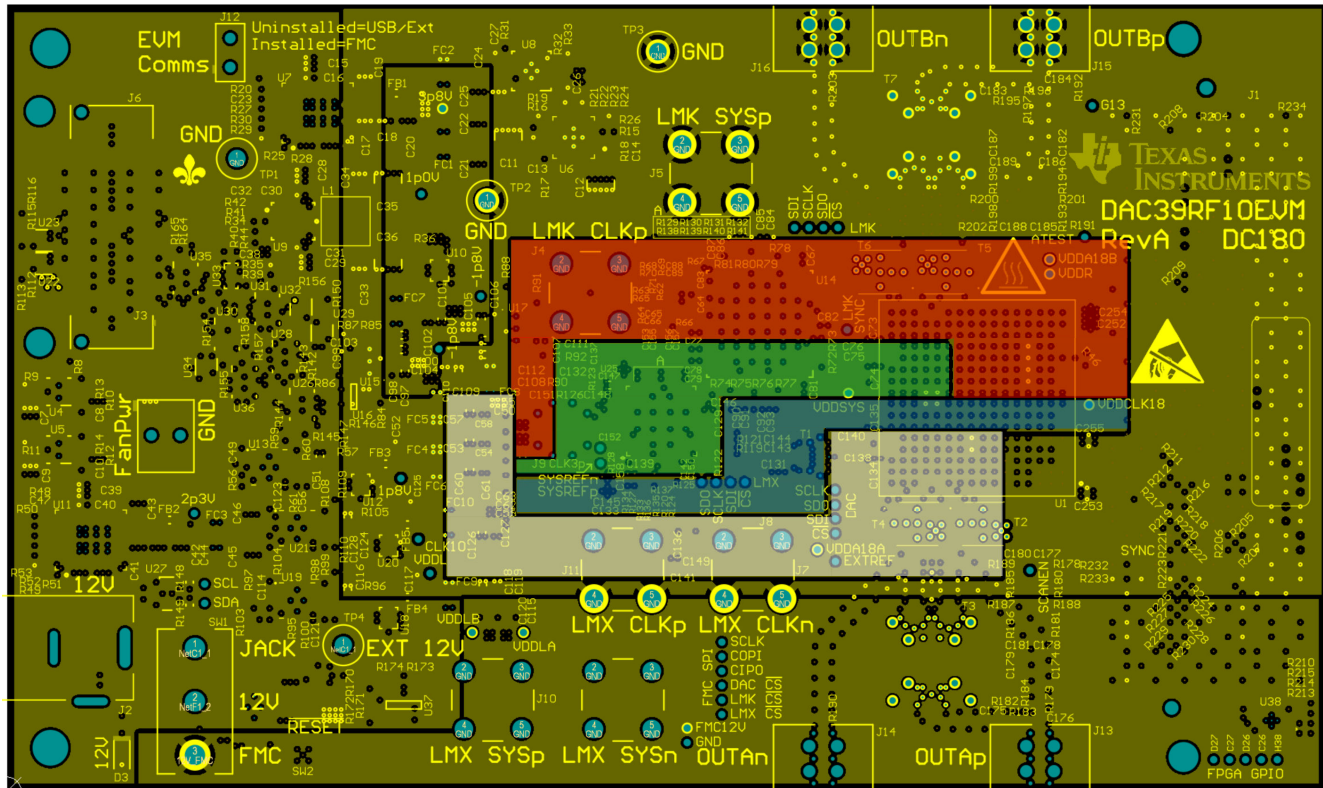


**Layer5 / PWR2**  
**DAC VDDL A = RED**  
**DAC VDDL B = YELLOW**  
**DAC VDDL CLK1P0V = GREEN**

**Figure 8-31. Power Plane Layout for Layer 5**



**Layer12 / PWR3**  
**DAC VDDA18A = RED**  
**DAC VDDA18B = ORANGE**  
**DAC VDDB = YELLOW**  
**DAC VEExA = GREEN**  
**DAC VEExB = BLUE**  
**VDDIO = WHITE**  
**Figure 8-32. Power Plane Layout for Layer 12**



**Layer14 / PWR4**  
**DAC VDDR = RED**  
**DAC VDDSYS18 = GREEN**  
**DAC VDDCLK18 = BLUE**  
**VDDIO = WHITE**

**Figure 8-33. Power Plane Layout for Layer 14**

In addition, TI recommends the following general PCB fabrication considerations for all high-speed PCB designs:

1. Use high quality dielectric materials for any critical signal layers within the PCB stack-up. Typically, the top and bottom layers are the most critical and more board houses can implement a mix of high and standard quality dielectrics, also known as a hybrid stack-up.
2. Use multiple power layers if necessary to provide a robust power delivery system to the converter.
3. Use multiple ground, power, ground layer stacks within the PCB to develop high frequency decoupling within the PCB, the recommendation for these layers is 4 mils or less.
4. Use a solid ground plane, do not split or “slot” the ground plane to create an analog vs. digital grounding barrier or divider to avoid harm.

## 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE           | REVISION | NOTES           |
|----------------|----------|-----------------|
| September 2024 | *        | Initial Release |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number         | Status<br>(1) | Material type<br>(2) | Package   Pins    | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-------------------------------|---------------|----------------------|-------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">DDS39RF12ACK</a>  | Active        | Production           | FCBGA (ACK)   256 | 90   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 85    | DDS39RF<br>12       |
| <a href="#">DDS39RF12ACL</a>  | Active        | Production           | FCBGA (ACL)   256 | 90   JEDEC TRAY (5+1) | No          | Call TI                              | Call TI                           | -40 to 85    | DDS39RF<br>12       |
| <a href="#">DDS39RFS12ACK</a> | Active        | Production           | FCBGA (ACK)   256 | 90   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 85    | DDS39RF<br>S12      |
| <a href="#">DDS39RFS12ACL</a> | Active        | Production           | FCBGA (ACL)   256 | 90   JEDEC TRAY (5+1) | No          | Call TI                              | Level-3-220C-168 HR               | -40 to 85    | DDS39RF<br>S12      |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

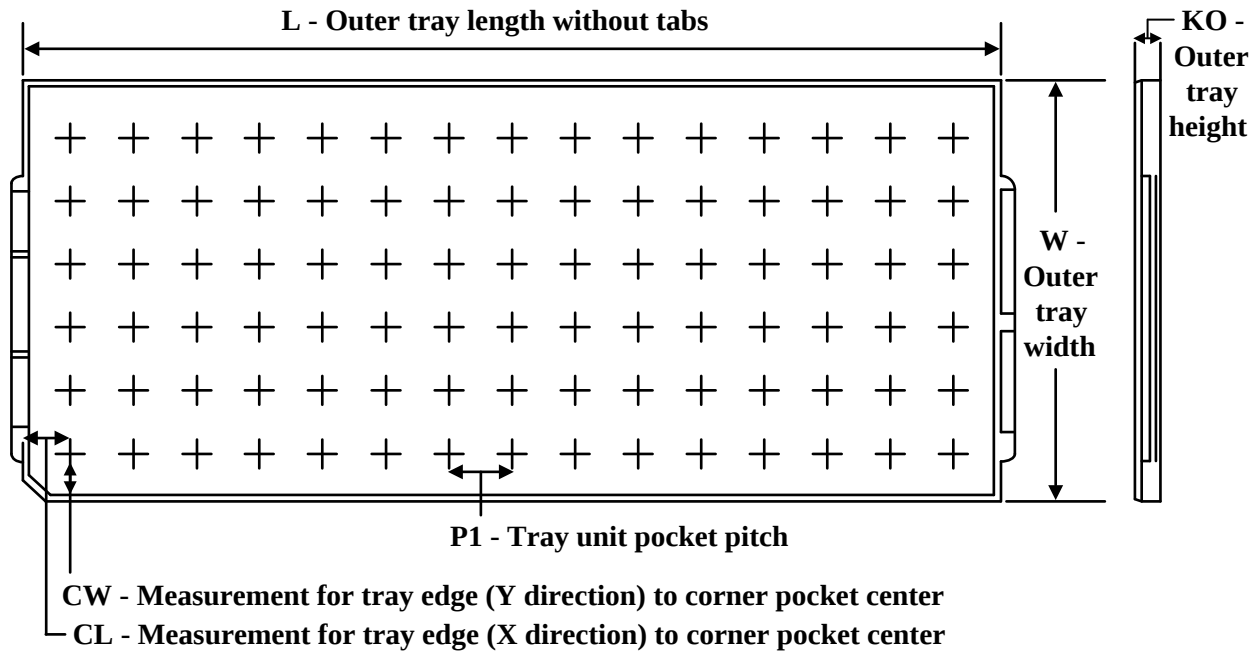
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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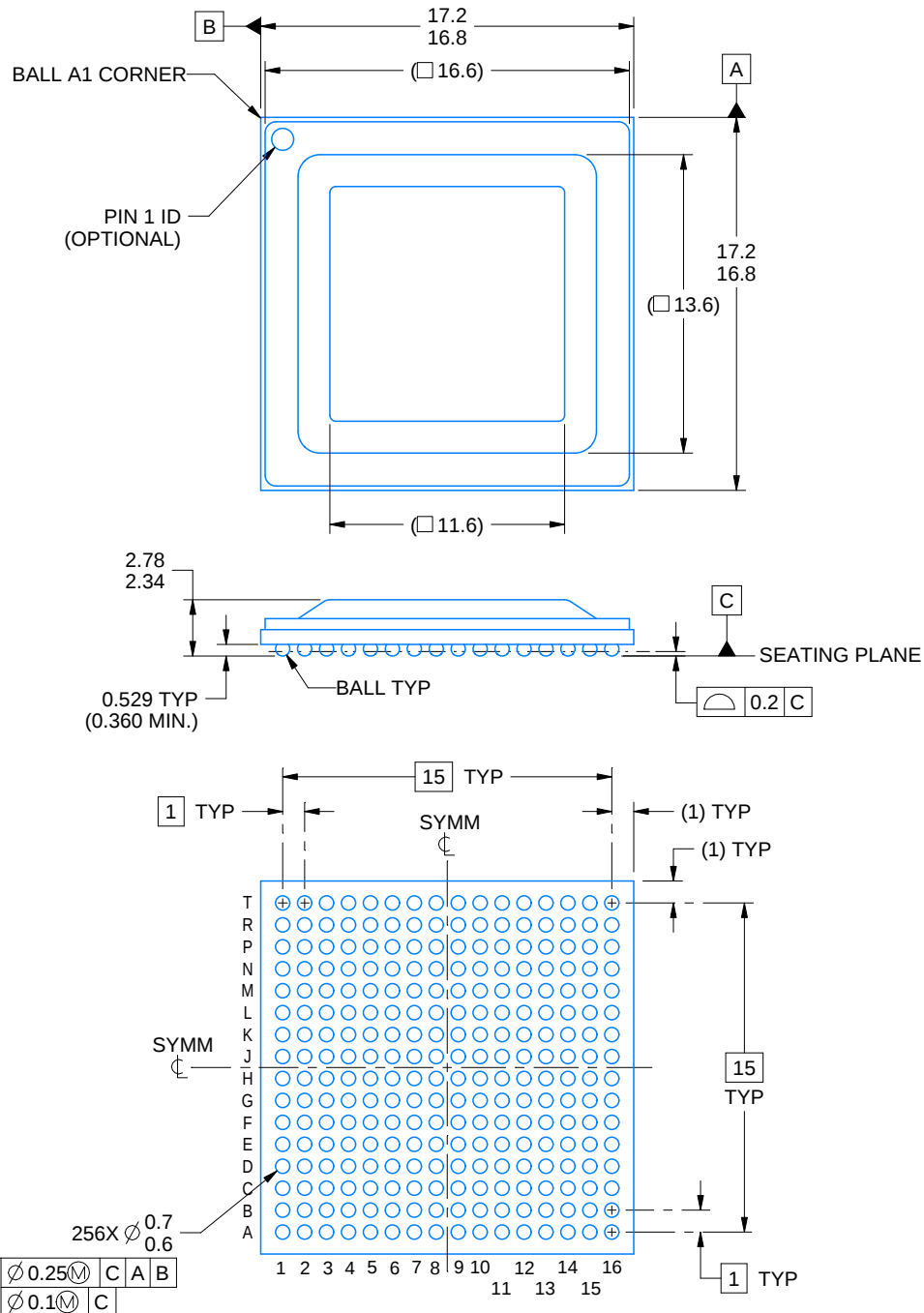
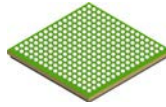
## TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

\*All dimensions are nominal

| Device        | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (μm) | P1 (mm) | CL (mm) | CW (mm) |
|---------------|--------------|--------------|------|-----|-------------------|----------------------|--------|--------|---------|---------|---------|---------|
| DDS39RF12ACK  | ACK          | FCBGA        | 256  | 90  | 6 x 15            | 150                  | 315    | 135.9  | 7620    | 19.5    | 21      | 19.2    |
| DDS39RF12ACL  | ACL          | FCBGA        | 256  | 90  | 6 x 15            | 150                  | 315    | 135.9  | 7620    | 19.5    | 21      | 19.2    |
| DDS39RFS12ACK | ACK          | FCBGA        | 256  | 90  | 6 x 15            | 150                  | 315    | 135.9  | 7620    | 19.5    | 21      | 19.2    |
| DDS39RFS12ACL | ACL          | FCBGA        | 256  | 90  | 6 x 15            | 150                  | 315    | 135.9  | 7620    | 19.5    | 21      | 19.2    |



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NOTES:

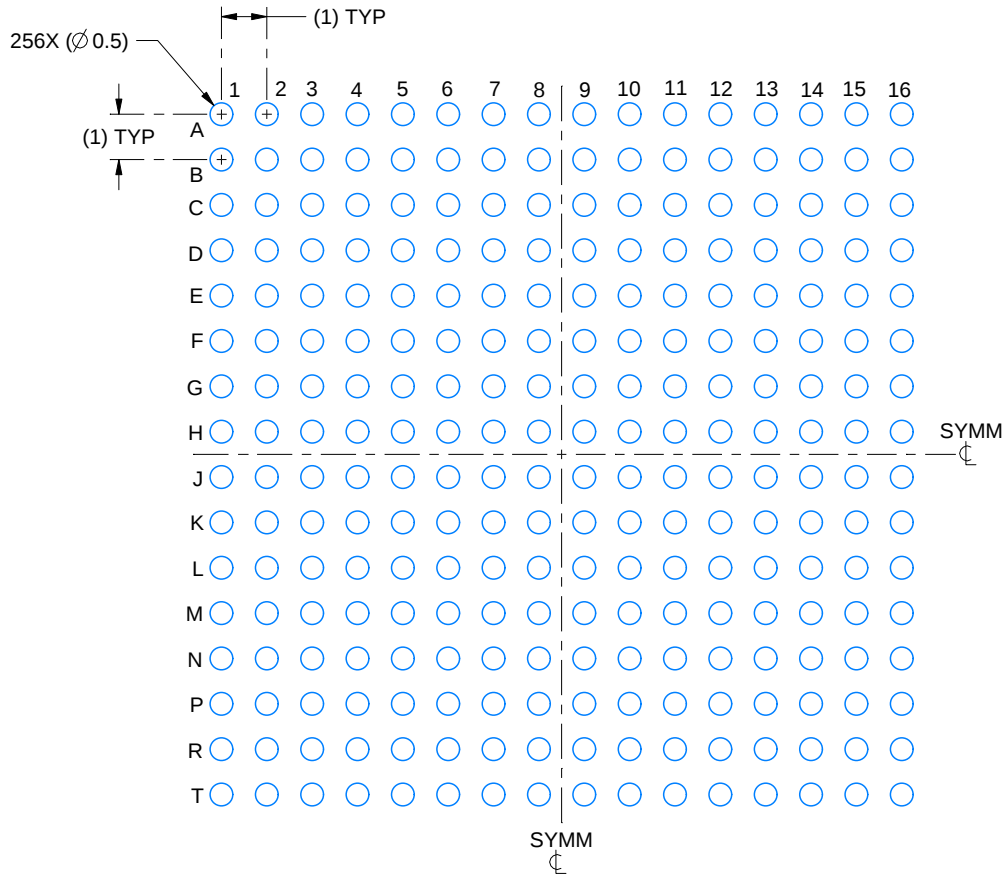
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

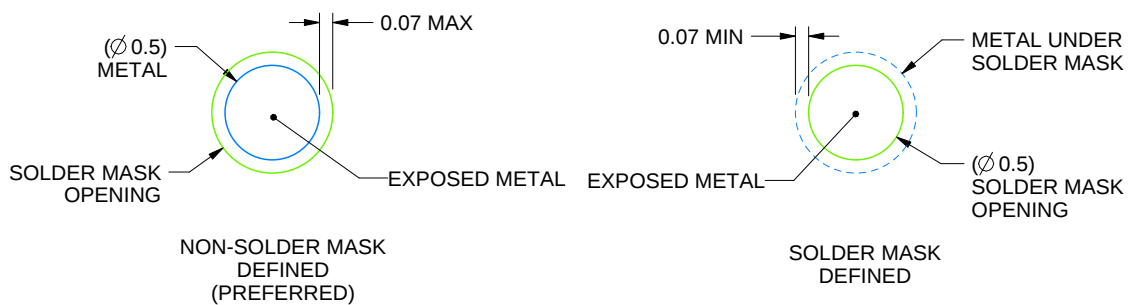
ACL0256A

FCBGA - 2.78 mm max height

BALL GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:6X



SOLDER MASK DETAILS  
NOT TO SCALE

4229409/A 02/2023

NOTES: (continued)

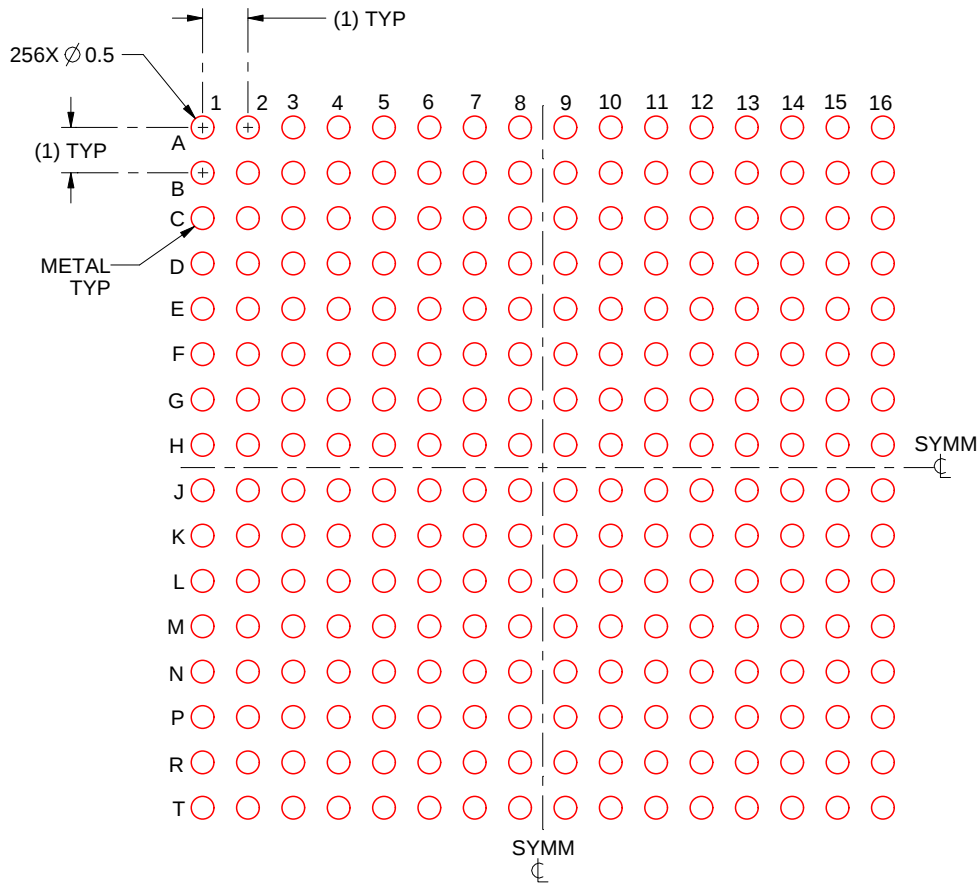
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 ([www.ti.com/lit/spru811](http://www.ti.com/lit/spru811)).

# EXAMPLE STENCIL DESIGN

ACL0256A

FCBGA - 2.78 mm max height

BALL GRID ARRAY

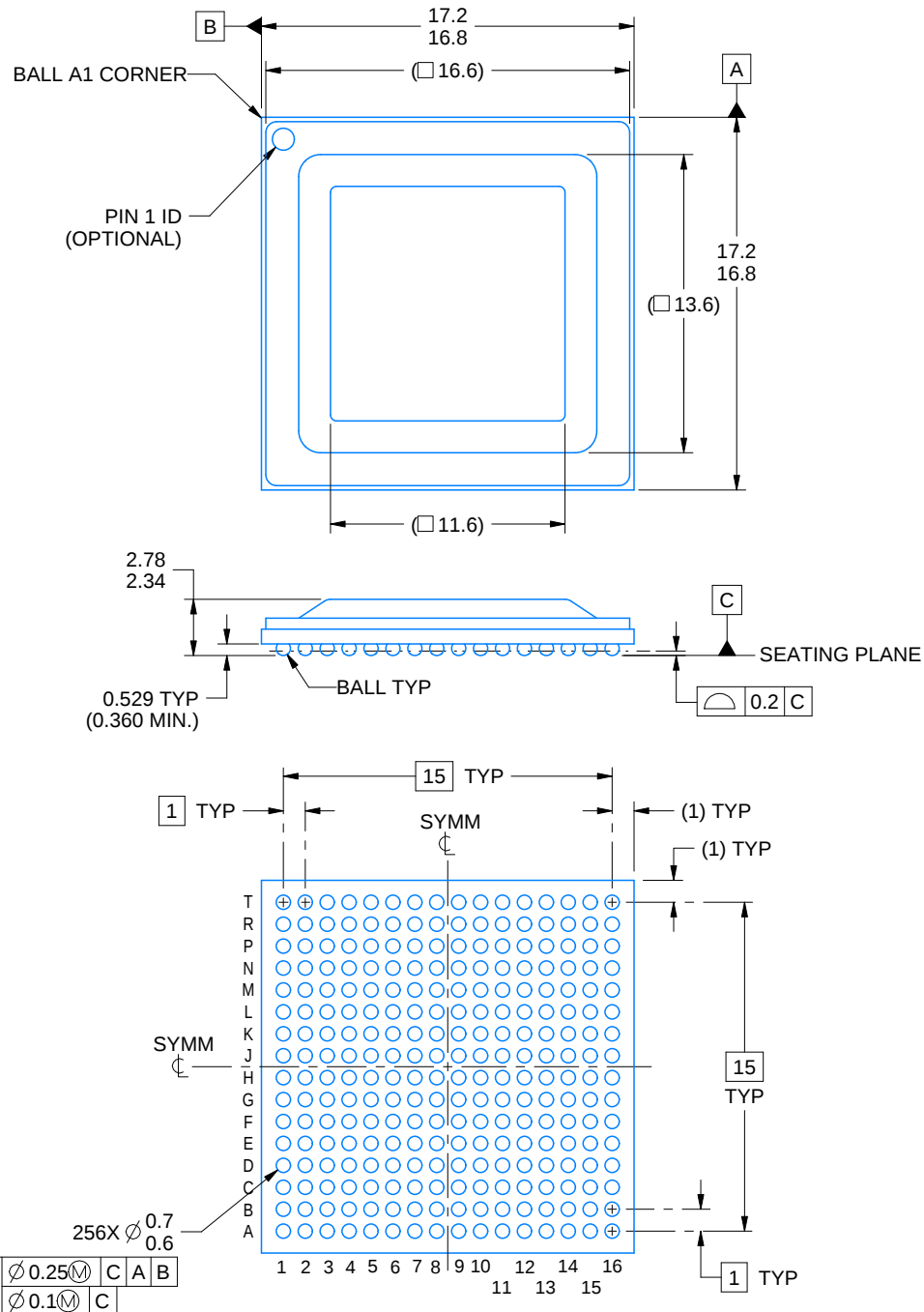
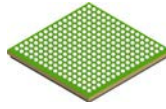


SOLDER PASTE EXAMPLE  
 BASED ON 0.15 mm THICK STENCIL  
 SCALE: 6X

4229409/A 02/2023

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



4226903/C 03/2023

## NOTES:

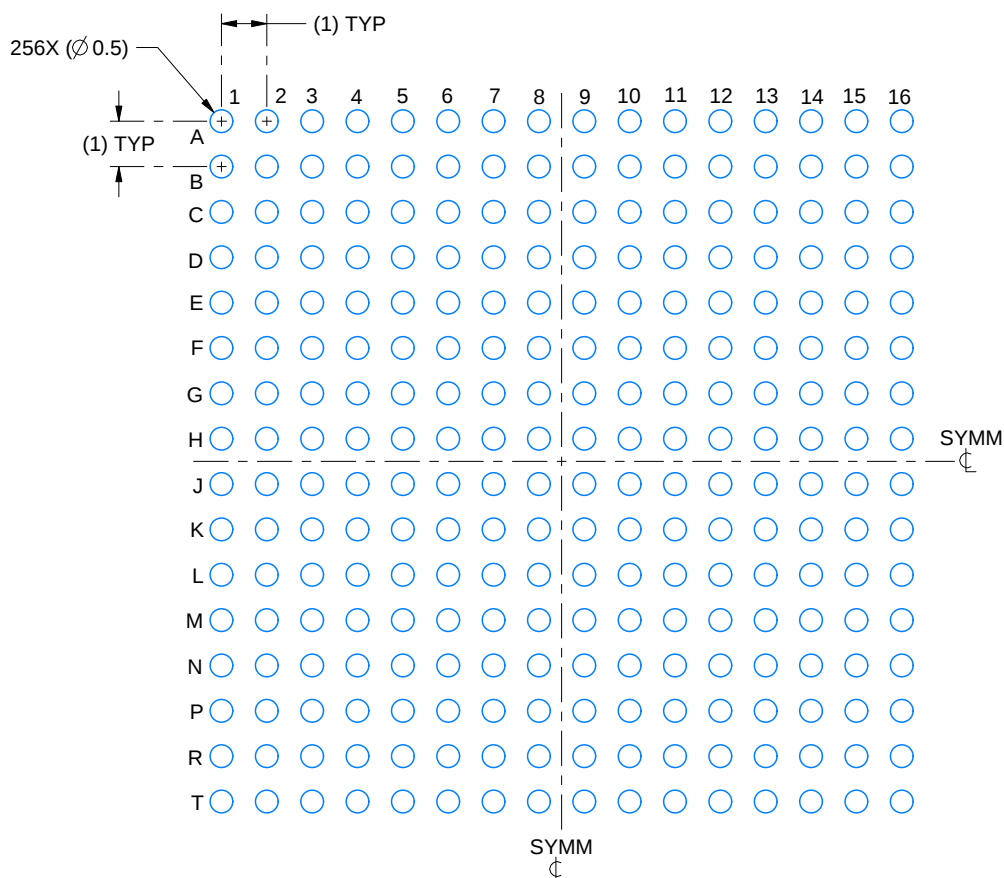
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The lids are electrically floating (e.g. not tied to GND).

# EXAMPLE BOARD LAYOUT

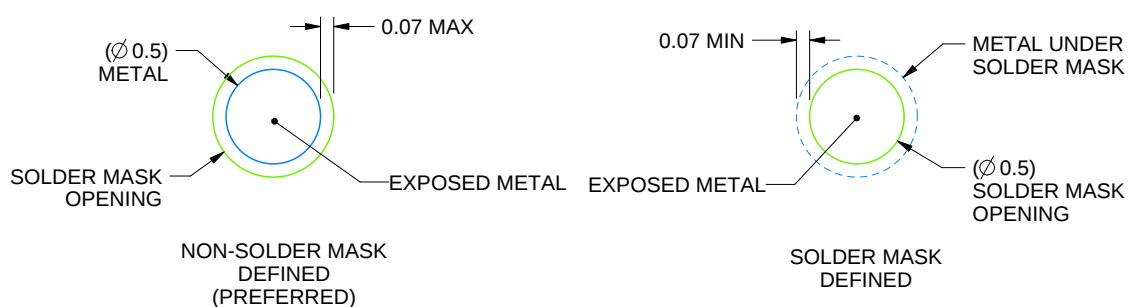
ACK0256A

FCBGA - 2.78 mm max height

BALL GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:6X



SOLDER MASK DETAILS  
NOT TO SCALE

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NOTES: (continued)

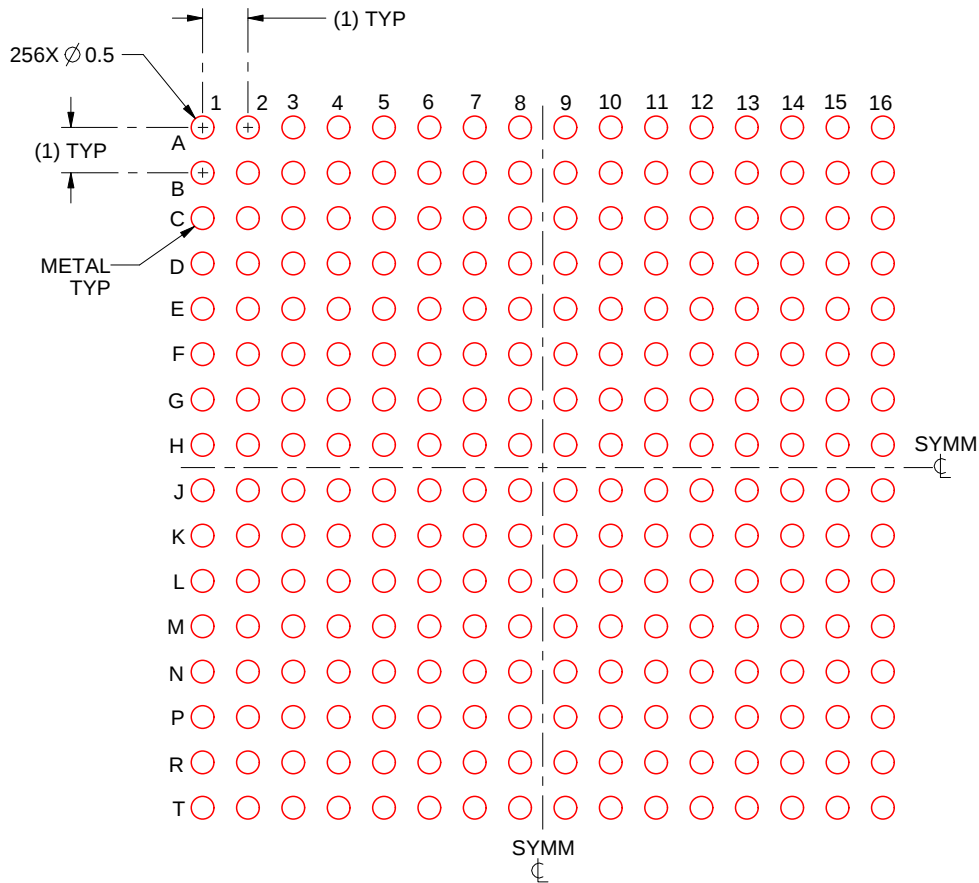
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 ([www.ti.com/lit/spru811](http://www.ti.com/lit/spru811)).

# EXAMPLE STENCIL DESIGN

ACK0256A

FCBGA - 2.78 mm max height

BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
 BASED ON 0.15 mm THICK STENCIL  
 SCALE: 6X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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