TEXAS INSTRUMENTS

DLP471TP .47 4K UHD DMD

1 Features

- 0.47-Inch diagonal micromirror array
  - 4K UHD (3840 × 2160) display resolution
  - 5.4-µm micromirror pitch
  - ±17° micromirror tilt (relative to flat surface)
  - Bottom illumination
- High-speed serial interface (HSSI) input data bus
- Supports 4K UHD at 60 Hz
- Supports 1080p up to 240 Hz
- LED operation supported by DLPC6540 display controller, DLPA3005 power management IC (PMIC) and LED driver

2 Applications

- Mobile smart TV
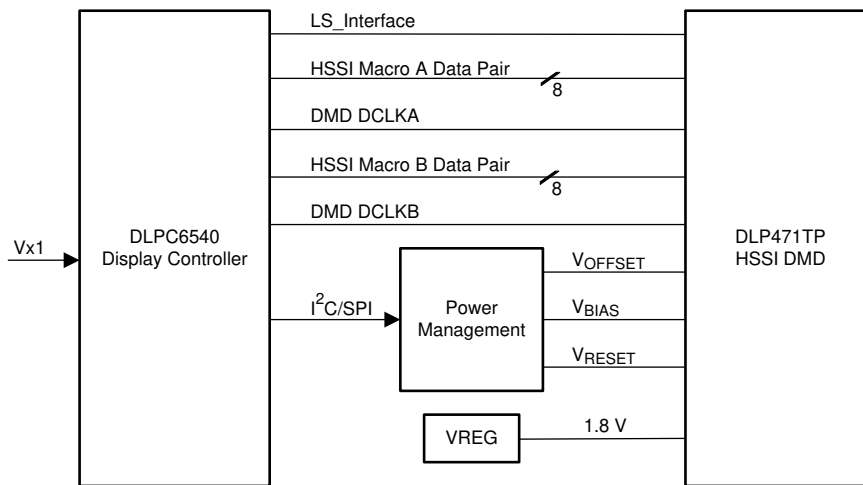- Mobile projector
- Digital signage

3 Description

The DLP471TP digital micromirror device (DMD) is a digitally controlled micro-electro-mechanical system (MEMS) spatial light modulator (SLM) that enables bright 4K UHD display systems. The TI DLP® products 0.47" 4K UHD chipset is composed of the DMD, DLPC6540 display controller, and DLPA3005 PMIC and LED driver. The compact physical size of the chipset provides a complete system solution that enables small form factor 4K UHD displays.

Device Information[(1)]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DLP471TP	FQQ (270)	25.65 mm × 16.9 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2022) to Revision B (July 2023)   **Page**
- Added section "ILLUMINATION" to *Recommended Operating Conditions* 9
- Updated *Micromirror Array Temperature Calculation* 24
- Added *Micromirror Power DensityCalculation* 25

Changes from Revision * (August 2020) to Revision A (June 2022)   **Page**
- This document is updated per the latest Texas Instruments and industry standards...........1
- Updated |T_{DELTA}| MAX from 14°C to 15°C...........9
- Updated *Micromirror Array Optical Characteristics* 19
- Updated Figure 9-1 33
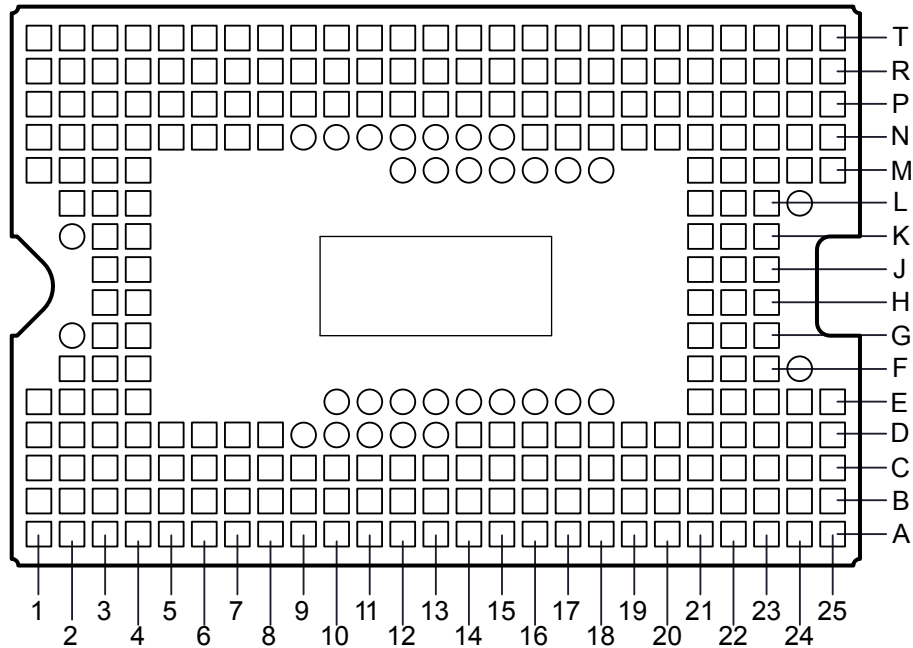
5 Pin Configuration and Functions

Figure 5-1. FQQ Package 270-Pin CLGA (Bottom View)

Table 5-1. Pin Functions

PIN[2]		TYPE[1]	DESCRIPTION	TERMINATION	TRACE LENGTH (mm)
NAME	PAD ID				
D_AP(0)	A8	I	High-speed Differential Data Pair lane A0	Differential 100 Ω	2.15873
D_AN(0)	A7	I	High-speed Differential Data Pair lane A0	Differential 100 Ω	2.16135
D_AP(1)	B2	I	High-speed Differential Data Pair lane A1	Differential 100 Ω	8.33946
D_AN(1)	C2	I	High-speed Differential Data Pair lane A1	Differential 100 Ω	8.34121
D_AP(2)	A6	I	High-speed Differential Data Pair lane A2	Differential 100 Ω	6.41271
D_AN(2)	A5	I	High-speed Differential Data Pair lane A2	Differential 100 Ω	6.41305
D_AP(3)	A10	I	High-speed Differential Data Pair lane A3	Differential 100 Ω	1.8959
D_AN(3)	A9	I	High-speed Differential Data Pair lane A3	Differential 100 Ω	1.8959
D_AP(4)	D1	I	High-speed Differential Data Pair lane A4	Differential 100 Ω	12.11543
D_AN(4)	E1	I	High-speed Differential Data Pair lane A4	Differential 100 Ω	12.11539
D_AP(5)	D3	I	High-speed Differential Data Pair lane A5	Differential 100 Ω	12.01561
D_AN(5)	E3	I	High-speed Differential Data Pair lane A5	Differential 100 Ω	12.0164
D_AP(6)	F3	I	High-speed Differential Data Pair lane A6	Differential 100 Ω	12.98403
D_AN(6)	G3	I	High-speed Differential Data Pair lane A6	Differential 100 Ω	12.98177
D_AP(7)	A12	I	High-speed Differential Data Pair lane A7	Differential 100 Ω	2.29773
D_AN(7)	A11	I	High-speed Differential Data Pair lane A7	Differential 100 Ω	2.29773
DCLK_AP	A3	I	High-speed Differential Clock A	Differential 100 Ω	11.75367
DCLK_AN	A4	I	High-speed Differential Clock A	Differential 100 Ω	11.57432
D_BP(0)	A14	I	High-speed Differential Data Pair lane B0	Differential 100 Ω	2.10786
D_BN(0)	A15	I	High-speed Differential Data Pair lane B0	Differential 100 Ω	2.10711
D_BP(1)	F23	I	High-speed Differential Data Pair lane B1	Differential 100 Ω	12.79448

Product Folder Links: *DLP471TP*

Table 5-1. Pin Functions (continued)

PIN[2]		TYPE[1]	DESCRIPTION	TERMINATION	TRACE LENGTH (mm)
NAME	PAD ID				
D_BN(1)	G23	I	High-speed Differential Data Pair lane B1	Differential 100 Ω	12.79438
D_BP(2)	E24	I	High-speed Differential Data Pair lane B2	Differential 100 Ω	13.00876
D_BN(2)	E23	I	High-speed Differential Data Pair lane B2	Differential 100 Ω	13.00932
D_BP(3)	A22	I	High-speed Differential Data Pair lane B3	Differential 100 Ω	11.21886
D_BN(3)	A23	I	High-speed Differential Data Pair lane B3	Differential 100 Ω	11.21881
D_BP(4)	D25	I	High-speed Differential Data Pair lane B4	Differential 100 Ω	10.79038
D_BN(4)	D24	I	High-speed Differential Data Pair lane B4	Differential 100 Ω	10.78946
D_BP(5)	A20	I	High-speed Differential Data Pair lane B5	Differential 100 Ω	5.75986
D_BN(5)	A21	I	High-speed Differential Data Pair lane B5	Differential 100 Ω	5.75928
D_BP(6)	B24	I	High-speed Differential Data Pair lane B6	Differential 100 Ω	9.01461
D_BN(6)	B25	I	High-speed Differential Data Pair lane B6	Differential 100 Ω	9.01416
D_BP(7)	A18	I	High-speed Differential Data Pair lane B7	Differential 100 Ω	2.08767
D_BN(7)	A19	I	High-speed Differential Data Pair lane B7	Differential 100 Ω	2.08767
DCLK_BP	A17	I	High-speed Differential Clock B	Differential 100 Ω	2.12928
DCLK_BN	A16	I	High-speed Differential Clock B	Differential 100 Ω	2.30933
LS_WDATA_P	T16	I	LVDS Data	Differential 100 Ω	0
LS_WDATA_N	R16	I	LVDS Data	Differential 100 Ω	0.27407
LS_CLK_P	T14	I	LVDS CLK	Differential 100 Ω	2.43086
LS_CLK_N	R14	I	LVDS CLK	Differential 100 Ω	2.40852
LS_RDATA_A_BISTA	R18	O	LVCMOS Output		2.00263
BIST_B	T20	O	LVCMOS Output		4.61261
AMUX_OUT	C21	O	Analog Test Mux		3.03604
DMUX_OUT	R20	O	Digital Test Mux		2.88361
DMD_DEN_ARSTZ	T18	I	ARSTZ	17.5-kΩ pulldown	1.89945
TEMP_N	R12	I	Temp Diode N		4.02546
TEMP_P	T12	I	Temp Diode P		3.62598

Product Folder Links: *DLP471TP*

Table 5-1. Pin Functions (continued)

PIN[2]		TYPE[1]	DESCRIPTION	TERMINATION	TRACE LENGTH (mm)
NAME	PAD ID				
VDD	B13, C5, C9, C12, C15, C18, C22, D6, D7, D14, D16, D19, D20, E21, G21, J4, J21, J23, K3, K22, L2, L4, L22, M1, M3, M21, M23, M25, N2, N4, N6, N8, N16, N18, N20, N22, N24, P3, P5, P7, P9, P11, P13, P15, P17, P19, P21, P23, P25, R2, R4, R6, R8, R10, T3, T5, T7, T9, T11, T13, T15, T17, T19, T21, T23	P	Digital core supply voltage		Plane
VDDA	A24, B3, B5, B7, B9, B11, B14, B16, B18, B20, B22, C1, C24, D4, D23, E2, F4, F22, H3, H22	P	HSSI supply voltage		Plane
VRESET	A2, R1	P	Supply voltage for negative bias of micromirror reset signal		Plane
VBIAS	B1, P1	P	Supply voltage for positive bias of micromirror reset signal		Plane
VOFFSET	A1, A25, T1, T25	P	Supply voltage for HVCMOS logic, stepped up logic level		Plane

Product Folder Links: DLP471TP

Table 5-1. Pin Functions (continued)

PIN[2]		TYPE[1]	DESCRIPTION	TERMINATION	TRACE LENGTH (mm)
NAME	PAD ID				
VSS	C4, C6, C8, C10, C13, C14, C17, C19, C23, D5, D8, D15, D17, D18, D21, D22, F21, H4, H21, J3, J22, K4, K21, K23, L3, L21, L23, M2, M4, M22, M24, N1, N3, N5, N7, N17, N19, N21, N23, N25, P2, P4, P6, P8, P10, P12, P14, P16, P18, P20, P22, P24, R3, R5, R7, R9, R11, R13, R15, R17, R19, R21, R23, R25, T2, T4, T8, T10	G	Ground		Plane
VSSA	A13, B4, B6, B8, B10, B12, B15, B17, B19, B21, B23, C3, C7, C11, C16, C20, C25, D2, E4, E22, E25, F2, G4, G22, H23	G	Ground		Plane
DMD_Detect	T6	NC	DMD detection		None

Product Folder Links: *DLP471TP*

Table 5-1. Pin Functions (continued)

PIN[2]		TYPE[1]	DESCRIPTION	TERMINATION	TRACE LENGTH (mm)
NAME	PAD ID				
N/C	D9, D10, D11, D12, D13, E10, E11, E12, E13, E14, E15, E16, E17, E18, F24, G2, K2, L24, M12, M13, M14, M15, M16, M17, M18, N9, N10, N11, N12, N13, N14, N15, R22, R24 ,T22, T24	NC	No connect pin		None

(1)   I=Input, O=Output, P=Power, G=Ground, NC = No Connect
(2)   Only 238 pins are electrically connected for functional use.

6 Specifications

6.1 Absolute Maximum Ratings

Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

		MIN	MAX	UNIT
SUPPLY VOLTAGE				
V_{DD}	Supply voltage for LVCMOS core logic and LVCMOS low speed interface (LSIF)[1]	–0.5	2.3	V
V_{DDA}	Supply voltage for high speed serial interface (HSSI) receivers[1]	–0.3	2.2	V
V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrode[1] [2]	–0.5	11	V
V_{BIAS}	Supply voltage for micromirror electrode[1]	–0.5	19	V
V_{RESET}	Supply voltage for micromirror electrode[1]	–15	0.5	V
$\| V_{DDA} - V_{DD} \|$	Supply voltage delta (absolute value)[3]		0.3	V
$\| V_{BIAS} - V_{OFFSET} \|$	Supply voltage delta (absolute value)[4]		11	V
$\| V_{BIAS} - V_{RESET} \|$	Supply voltage delta (absolute value)[5]		34	V
INPUT VOLTAGE				
	Input voltage for other inputs – LSIF and LVCMOS[1]	–0.5	2.45	V
	Input voltage for other inputs – HSSI[1] [6]	–0.2	V_{DDA}	V
LOW SPEED INTERFACE (LSIF)				
f_{CLOCK}	LSIF clock frequency (LS_CLK)		130	MHz
$\| V_{ID} \|$	LSIF differential input voltage magnitude[6]		810	mV
I_{ID}	LSIF differential input current		10	mA
HIGH SPEED SERIAL INTERFACE (HSSI)				
f_{CLOCK}	HSSI clock frequency (DCLK)		1.65	GHz
$\| V_{ID} \|$	HSSI differential input voltage magnitude Data Lane[6]		700	mV
$\| V_{ID} \|$	HSSI differential input voltage magnitude Clock Lane[6]		700	mV
ENVIRONMENTAL				
T_{WINDOW} and T_{ARRAY}	Temperature, operating[7]	0	90	°C
	Temperature, non-operating[7]	–40	90	°C
$\|T_{DELTA}\|$	Absolute temperature delta between any point on the window edge and the ceramic test point TP1[8]		30	°C
T_{DP}	Dew point temperature, operating and non–operating (noncondensing)		81	°C

(1) All voltage values are with respect to the ground terminals (V_{SS}). The following required power supplies must be connected for proper DMD operation: V_{DD}, V_{DDA}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. All V_{SS} connections are also required.
(2) V_{OFFSET} supply transients must fall within specified voltages.
(3) Exceeding the recommended allowable absolute voltage difference between V_{DDA} and V_{DD} may result in excessive current draw.
(4) Exceeding the recommended allowable absolute voltage difference between V_{BIAS} and V_{OFFSET} may result in excessive current draw.
(5) Exceeding the recommended allowable absolute voltage difference between V_{BIAS} and V_{RESET} may result in excessive current draw.
(6) This maximum input voltage rating applies when each input of a differential pair is at the same voltage potential. LVDS and HSSI differential inputs must not exceed the specified limit or damage may result to the internal termination resistors.
(7) The highest temperature of the active array (as calculated using Micromirror Array Temperature Calculation) or of any point along the window edge as defined in Figure 7-1. The locations of thermal test points TP2, TP3, TP4 and TP5 in Figure 7-1 are intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, that point should be used.
(8) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in Figure 7-1. The window test points TP2, TP3, TP4, and TP5 shown in Figure 7-1 are intended to result in the worst case delta. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used.

Product Folder Links: *DLP471TP*

6.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system.

		MIN	MAX	UNIT
T_{DMD}	DMD temperature	–40	85	°C
T_{DP-AVG}	Average dew point temperature, non-condensing[1]		24	°C
T_{DP-ELR}	Elevated dew point temperature range, non-condensing[2]	28	36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range		6	months

(1) The average temperature over time (including storage and operating temperatures) that the device is not in the elevated dew point temperature range.
(2) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR}.

6.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged device model (CDM), per JEDEC specification ANSI/ESDA/JEDEC JS-002[2]	±500	V

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions

Over operating free-air temperature range and supply voltages (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by the Recommended Operating Conditions. No level of performance is implied when operating the device above or below the Recommended Operating Conditions limits.

		MIN	TYP	MAX	UNIT
SUPPLY VOLTAGES [1] [2]					
V_{DD}	Supply voltage for LVCMOS core logic and low speed interface (LSIF)	1.71	1.8	1.95	V
V_{DDA}	Supply voltage for high speed serial interface (HSSI) receivers	1.71	1.8	1.95	V
V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrode[3]	9.5	10	10.5	V
V_{BIAS}	Supply voltage for micromirror electrode	17.5	18	18.5	V
V_{RESET}	Supply voltage for micromirror electrode	–14.5	–14	–13.5	V
$\mid V_{DDA} - V_{DD} \mid$	Supply voltage delta, absolute value[4]			0.3	V
$\mid V_{BIAS} - V_{OFFSET} \mid$	Supply voltage delta, absolute value[5]			10.5	V
$\mid V_{BIAS} - V_{RESET} \mid$	Supply voltage delta, absolute value			33	V
LVCMOS INPUT					
V_{IH}	High level input voltage[6]	$0.7 \times V_{DD}$			V
V_{IL}	Low level input voltage[6]			$0.3 \times V_{DD}$	V
LOW SPEED SERIAL INTERFACE (LSIF)					
f_{CLOCK}	LSIF clock frequency (LS_CLK)[7]	108	120	130	MHz
DCD_{IN}	LSIF duty cycle distortion (LS_CLK)	44%		56%	
$\mid V_{ID} \mid$	LSIF differential input voltage magnitude[7]	150	350	440	mV
V_{LVDS}	LSIF voltage[7]	575		1520	mV
V_{CM}	Common mode voltage[7]	700	900	1300	mV
Z_{LINE}	Line differential impedance (PWB/trace)	90	100	110	Ω
Z_{IN}	Internal differential termination resistance	80	100	120	Ω

Product Folder Links: *DLP471TP*

6.4 Recommended Operating Conditions (continued)

Over operating free-air temperature range and supply voltages (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by the Recommended Operating Conditions. No level of performance is implied when operating the device above or below the Recommended Operating Conditions limits.

		MIN	TYP	MAX	UNIT
HIGH SPEED SERIAL INTERFACE (HSSI)					
f_{CLOCK}	HSSI clock frequency (DCLK)[8]	1.2		1.6	GHz
DCD_{IN}	HSSI duty cycle distortion (DCLK)	44	50	56	%
$\mid V_{ID} \mid$ Data	HSSI differential input voltage magnitude Data Lane[8]	100		600	mV
$\mid V_{ID} \mid$ CLK	HSSI differential input voltage magnitude Clock Lane[8]	295		600	mV
VCM_{DC} Data	Input common mode voltage (DC) Data Lane[8]	200	600	800	mV
VCM_{DC} CLK	Input common mode voltage (DC) Clk Lane[8]	200	600	800	mV
VCM_{ACp-p}	AC peak to peak (ripple) on common mode voltage of Data Lane and Clock Lane[8]			100	mV
Z_{LINE}	Line differential impedance (PWB/trace)		100		Ω
Z_{IN}	Internal differential termination resistance. (R_{Xterm})	80	100	120	Ω
ENVIRONMENTAL					
T_{ARRAY}	Array temperature, long–term operational[9] [10] [11] [12]	10		40 to 70 [11]	°C
	Array temperature, short-term operational, 500 hr max[10] [13]	0		10	°C
T_{WINDOW}	Window temperature, operational[14]			85	°C
$\mid T_{DELTA} \mid$	Absolute temperature delta between any point on the window edge and the ceramic test point TP1[15]			15	°C
T_{DP-AVG}	Average dew point temperature (non–condensing)[16]			24	°C
T_{DP-ELR}	Elevated dew point temperature range (non-condensing)[17]	28		36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range			6	months
ILLUMINATION					
ILL_{UV}	Illumination power at wavelengths < 410 nm[9]			10	mW/cm^2
ILL_{VIS}	Illumination power at wavelengths ≥ 410 nm and ≤ 800 nm[19]			20.5	W/cm^2
ILL_{IR}	Illumination power at wavelengths > 800 nm			10	mW/cm^2
ILL_{BLU}	Illumination power at wavelengths ≥ 410 nm and ≤ 475 nm[19]			6.5	W/cm^2
ILL_{BLU1}	Illumination power at wavelengths ≥ 410 nm and ≤ 445 nm[19]			1.2	W/cm^2
ILL_{θ}	Illumination marginal ray angle[18]			55	deg

(1) All power supply connections are required to operate the DMD: V_{DD}, V_{DDA}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. All V_{SS} connections are required to operate the DMD.
(2) All voltage values are with respect to the V_{SS} ground pins.
(3) V_{OFFSET} supply transients must fall within specified max voltages.
(4) To prevent excess current, the supply voltage delta $\mid V_{DDA} - V_{DD} \mid$ must be less than specified limit.
(5) To prevent excess current, the supply voltage delta $\mid V_{BIAS} - V_{OFFSET} \mid$ must be less than specified limit.
(6) LVCMOS input pin is DMD_DEN_ARSTZ.
(7) See the low speed interface (LSIF) timing requirements in Timing Requirements.
(8) See the high speed serial interface (HSSI) timing requirements in Timing Requirements.
(9) Simultaneous exposure of the DMD to the maximum *Recommended Operating Conditions* for temperature and UV illumination will reduce device lifetime.
(10) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point (TP1) shown in Figure 7-1 and the package thermal resistance using the Micromirror Array Temperature Calculation.
(11) Per Figure 6-1, the maximum operational array temperature should be derated based on the micromirror landed duty cycle that the DMD experiences in the end application. Refer to Micromirror Landed-On/Landed-Off Duty Cycle for a definition of micromirror landed duty cycle.
(12) Long-term is defined as the usable life of the device.
(13) Short-term is the total cumulative time over the useful life of the device.
(14) The locations of thermal test points TP2, TP3, TP4, and TP5 shown in Figure 7-1 are intended to measure the highest window edge temperature. For most applications, the locations shown are representative of the highest window edge temperature. If a particular application causes additional points on the window edge to be at a higher temperature, test points should be added to those locations.
(15) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in

Figure 7-1. The window test points TP2, TP3, TP4, and TP5 shown in Figure 7-1 are intended to result in the worst case delta temperature. If a particular application causes another point on the window edge to result in a larger delta in temperature, that point should be used.

(16) The average over time (including storage and operating) that the device is not in the 'elevated dew point temperature range'.

(17) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR}.

(18) The maximum marginal ray angle of the incoming illumination light at any point in the micromirror array, including Pond of Micromirrors (POM), should not exceed 55 degrees from the normal to the device array plane. The device window aperture has not necessarily been designed to allow incoming light at higher maximum angles to pass to the micromirrors, and the device performance has not been tested nor qualified at angles exceeding this. Illumination light exceeding this angle outside the micromirror array (including POM) will contribute to thermal limitations described in this document, and may negatively affect lifetime.

(19) The maximum allowable optical power incident on the DMD is limited by the maximum optical power density for each wavelength range specified and the micromirror array temperature (T_{ARRAY}).
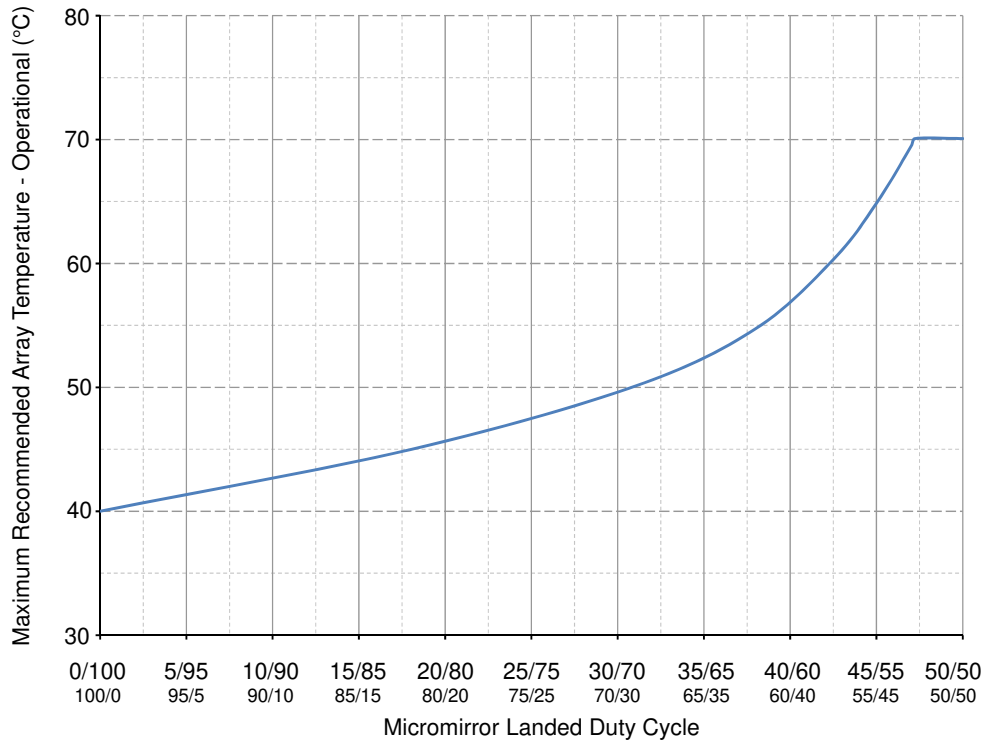

Figure 6-1. Maximum Recommended Array Temperature—Derating Curve

6.5 Thermal Information

THERMAL METRIC	DLP471TP FQQ PACKAGE 270 PIN	Unit
Thermal Resistance, active area to test point 1 (TP1)[1]	1.0	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in the Section 6.4. The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

6.6 Electrical Characteristics

Over operating free-air temperature range and supply voltages (unless otherwise noted)

PARAMETER [1] [2]	TEST CONDITIONS [1]	MIN	TYP	MAX	UNIT
CURRENT – TYPICAL					
I_{DD}	Supply current V_{DD} [3]			800	1200	mA

Product Folder Links: *DLP471TP*

6.6 Electrical Characteristics (continued)

Over operating free-air temperature range and supply voltages (unless otherwise noted)

PARAMETER [1] [2]		TEST CONDITIONS [1]	MIN	TYP	MAX	UNIT
I_{DDA}	Supply current V_{DDA} [3]			1000	1200	mA
I_{OFFSET}	Supply current V_{OFFSET} [4] [5]			20	25	mA
I_{BIAS}	Supply current V_{BIAS} [4] [5]			2.5	4.0	mA
I_{RESET}	Supply current V_{RESET} [5]		-9.3	-6.9		mA
POWER – TYPICAL						
P_{DD}	Supply power dissipation V_{DD} [3]			1440	2437.5	mW
P_{DDA}	Supply power dissipation V_{DDA} [3]			1620	2340	mW
P_{OFFSET}	Supply power dissipation V_{OFFSET} [4] [5]			230	367.5	mW
P_{BIAS}	Supply power dissipation V_{BIAS} [4] [5]			43.2	70.3	mW
P_{RESET}	Supply power dissipation V_{RESET} [5]			107.8	152.25	mW
P_{TOTAL}	Supply power dissipation Total			3441	5367.55	mW
LVCMOS INPUT						
I_{IL}	Low level input current [6]	$V_{DD} = 1.95\ V,\ V_I = 0\ V$	−100			nA
I_{IH}	High level input current [6]	$V_{DD} = 1.95\ V,\ V_I = 1.95\ V$			135	uA
LVCMOS OUTPUT						
V_{OH}	DC output high voltage [7]	$I_{OH} = -2\ mA$	$0.8 \times V_{DD}$			V
V_{OL}	DC output low voltage [7]	$I_{OL} = 2\ mA$			$0.2 \times V_{DD}$	V
RECEIVER EYE CHARACTERISTICS						
A1	Minimum data eye opening [8] [9]		100	400	600	mV
A2	Maximum data signal swing [8] [9]				600	mV
X1	Maximum data eye closure [8]				0.275	UI
X2	Maximum data eye closure [8]				0.4	UI
| t_{DRIFT} |	Drift between Clock and Data between Training Patterns				20	ps
CAPACITANCE						
C_{IN}	Input capacitance LVCMOS	f = 1 MHz			10	pF
C_{IN}	Input capacitance LSIF (low speed interface)	f = 1 MHz			20	pF
C_{IN}	Input capacitance HSSI (high speed serial interface)	f = 1 MHz			20	pF
C_{OUT}	Output capacitance	f = 1 MHz			10	pF

(1) All power supply connections are required to operate the DMD: V_{DD}, V_{DDA}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. All V_{SS} connections are required to operate the DMD.
(2) All voltage values are with respect to the ground pins (V_{SS}).
(3) To prevent excess current, the supply voltage delta \| $V_{DDA} - V_{DD}$ \| must be less than specified limit.
(4) To prevent excess current, the supply voltage delta \| $V_{BIAS} - V_{OFFSET}$ \| must be less than specified limit.
(5) Supply power dissipation based on 3 global resets in 200 µs.
(6) LVCMOS input specifications are for pin DMD_DEN_ARSTZ.
(7) LVCMOS output specification is for pins LS_RDATA_A and LS_RDATA_B.
(8) Refer to Figure 6-11, Receiver Eye Mask (1e-12 BER).
(9) Defined in Recommended Operating Conditions.

6.7 Switching Characteristics

Over operating free-air temperature range and supply voltages (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	Output propagation, Clock to Q (C2Q), rising edge of LS_CLK (differential clock signal) input to LS_RDATA output. [(1)]	C_L = 5 pF			11.1	ns
		C_L = 10 pF			11.3	ns
	Slew rate, LS_RDATA	20%–80%, C_L <10pF	0.5			V/ns
	Output duty cycle distortion, LS_RDATA_A and LS_RDATA_B	50-(C2Q rise – C2Q fall) ×130e6×100	40%		60%	

(1) See Figure 6-2.
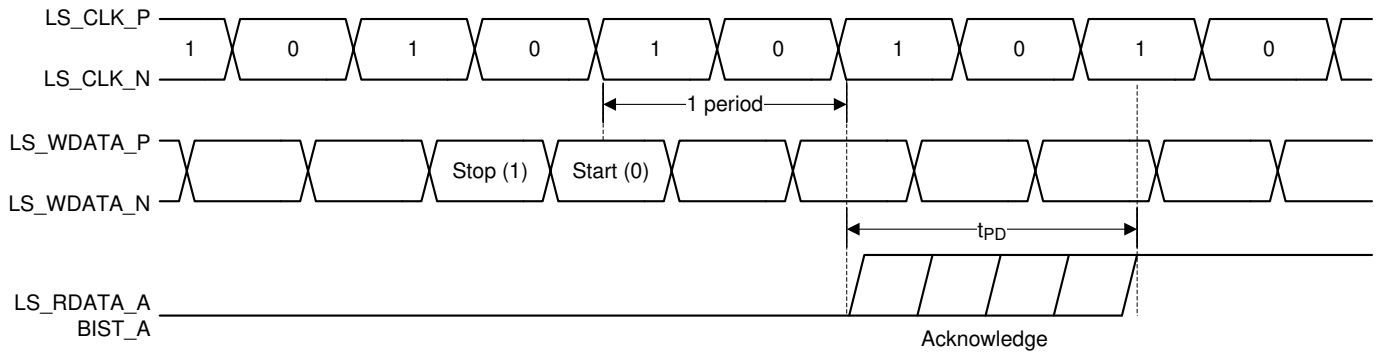
Figure 6-2. Switching Characteristics

Product Folder Links: *DLP471TP*

6.8 Timing Requirements

Over operating free-air temperature range and supply voltages (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVCMOS						
t_r	Rise time[1]	20% to 80% reference points			25	ns
t_f	Fall time[1]	80% to 20% reference points			25	ns
LOW SPEED INTERFACE (LSIF)						
t_r	Rise time[2]	20% to 80% reference points			450	ps
t_f	Fall time[2]	80% to 20% reference points			450	ps
$t_{W(H)}$	Pulse duration high[3]	LS_CLK. 50% to 50% reference points	3.1			ns
$t_{W(L)}$	Pulse duration low[3]	LS_CLK. 50% to 50% reference points	3.1			ns
t_{su}	Setup time[4]	LS_WDATA valid before rising edge of LS_CLK (differential)			1.5	ns
t_h	Hold time[4]	LS_WDATA valid after rising edge of LS_CLK (differential)			1.5	ns
HIGH SPEED SERIAL INTERFACE (HSSI)						
t_r	Rise time - data[5] [6]	From –A1 to A1 minimum eye height specification	50		115	ps
	Rise time - clock[5] [6]	From –A1 to A1 minimum eye height specification	50		135	ps
t_f	Fall time — data[5] [6]	From A1 to –A1 minimum eye height specification	50		115	ps
	Fall time — clock[5] [6]	From A1 to –A1 minimum eye height specification	50		135	ps
$t_{W(H)}$	Pulse duration high[7]	DCLK. 50% to 50% reference points	0.275			ns
$t_{W(L)}$	Pulse duration low[7]	DCLK. 50% to 50% reference points	0.275			ns

(1)   See Figure 6-9 for rise time and fall time for LVCMOS.
(2)   See Figure 6-4 for rise time and fall time for LSIF.
(3)   See Figure 6-4 for pulse duration high and low time for LSIF.
(4)   See Figure 6-4 for setup and hold time for LSIF.
(5)   See Figure 6-11 for rise time and fall time for HSSI Eye Characteristics.
(6)   See Figure 6-12 for rise time and fall time for HSSI.
(7)   See Figure 6-12 for pulse duration high and low for HSSI.
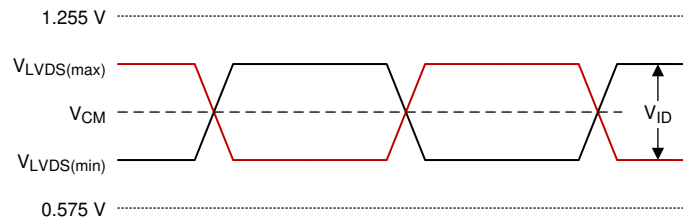
A.   See Equation 1 and Equation 2

Figure 6-3. LSIF Waveform Requirements

$$V_{LVDS\,(max)} = V_{CM\,(max)} + \left| \frac{1}{2} \times V_{ID\,(max)} \right|$$

(1)

$$V_{LVDS\,(min)} = V_{CM\,(min)} - \left| \frac{1}{2} \times V_{ID\,(max)} \right|$$

(2)

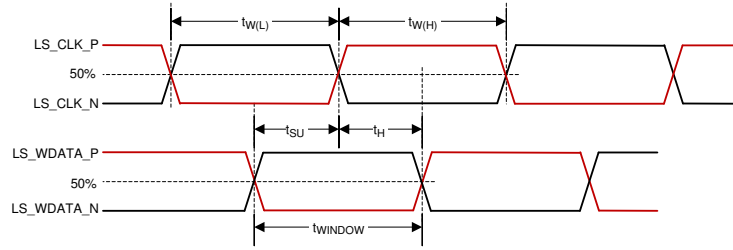Product Folder Links: *DLP471TP*

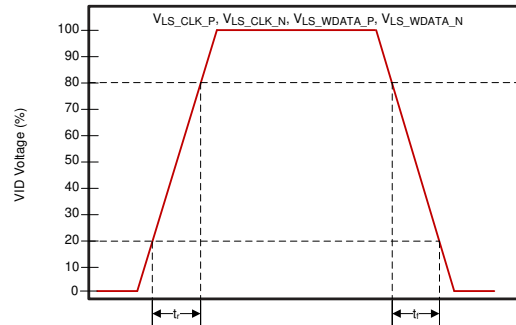**Figure 6-4. LSIF Timing Requirements**

Figure 6-5. LSIF Rise, Fall Time Slew
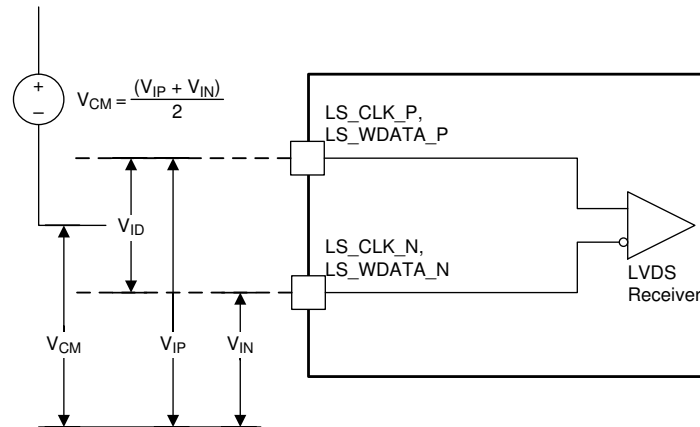
Figure 6-6. LSIF Voltage Requirements
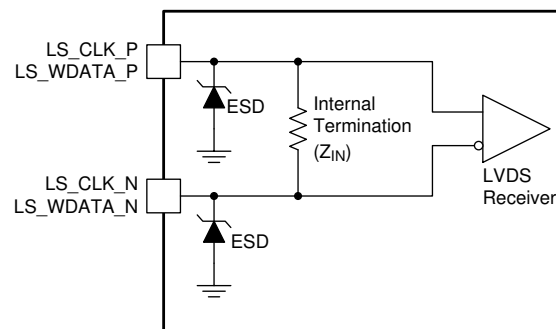
Figure 6-7. LSIF Equivalent Input
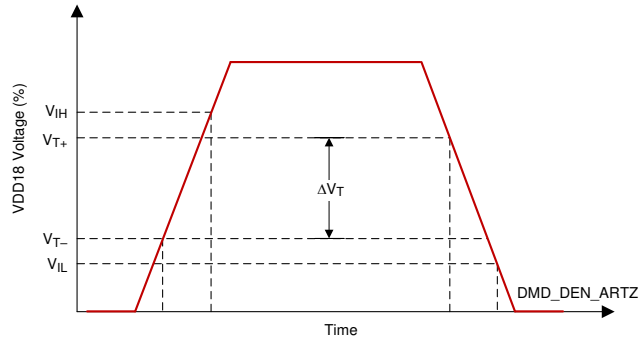
Product Folder Links: *DLP471TP*

Figure 6-8. LVCMOS Input Hysteresis

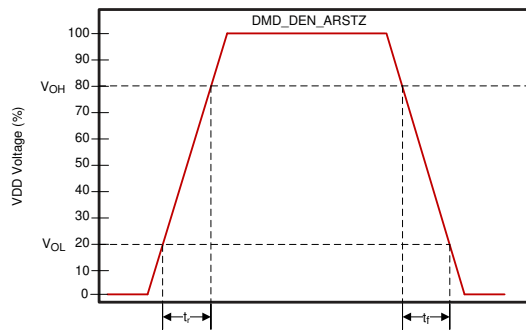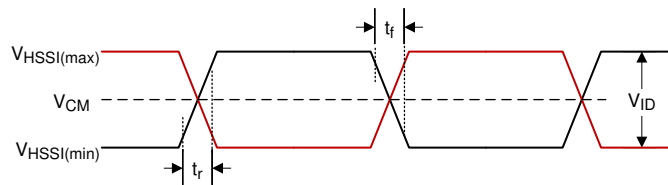**Figure 6-9. LVCMOS Rise, Fall Time Slew Rate**

A.   See Equation 3 and Equation 4

Figure 6-10. HSSI Waveform Requirements

$$V_{HSSI(max)} = V_{CM(max)} + \left| \frac{1}{2} \times V_{ID(max)} \right|$$

(3)

$$V_{HSSI(min)} = V_{CM(min)} - \left| \frac{1}{2} \times V_{ID(max)} \right|$$
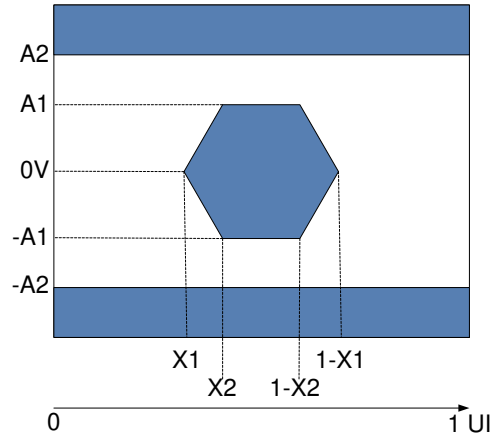
(4)

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Figure 6-11. HSSI Eye Characteristics
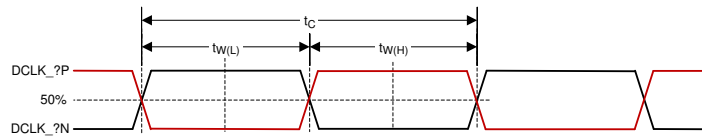
Figure 6-12. HSSI CLK Characteristics

6.9 System Mounting Interface Loads

PARAMETER	MIN	TYP	MAX	UNIT
Thermal interface area[1]			100	N
Electrical interface area[1]			245	N

(1)   The load should be uniformly applied within the area shown in Figure 6-13.

Electrical Interface Area

Thermal Interface Area
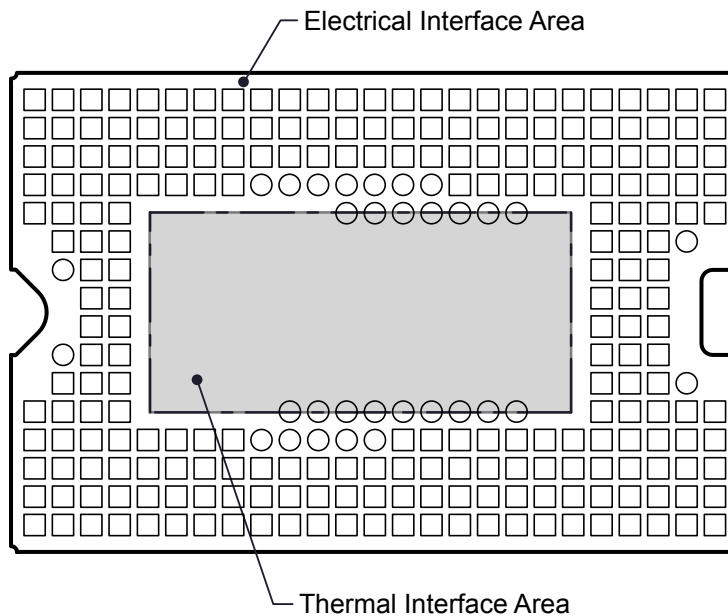
Figure 6-13. System Mounting Interface Loads

Product Folder Links: DLP471TP

6.10 Micromirror Array Physical Characteristics

PARAMETER DESCRIPTION		VALUE	UNIT
Number of active columns[1] [2]	M	1920	micromirrors
Number of active rows[1] [2]	N	1080	micromirrors
Micromirror (pixel) pitch [1]	P	5.4	µm
Micromirror active array width[1]	Micromirror pitch × number of active columns	10.368	mm
Micromirror active array height[1]	Micromirror pitch × number of active rows	5.832	mm
Micromirror active border[3]	Pond of micromirror (POM)	20	micromirrors/side

(1) See Figure 6-14.
(2) The fast switching speed of the DMD micromirrors combined with advanced DLP image processing algorithms enables each micromirror
to display four distinct pixels on the screen during every frame, resulting in a full 3840 × 2160 pixel image being displayed.
(3) The structure and qualities of the border around the active array includes a band of partially functional micromirrors referred to as the
Pond Of Micromirrors (POM). These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state
but still require an electrical bias to tilt toward the OFF state.
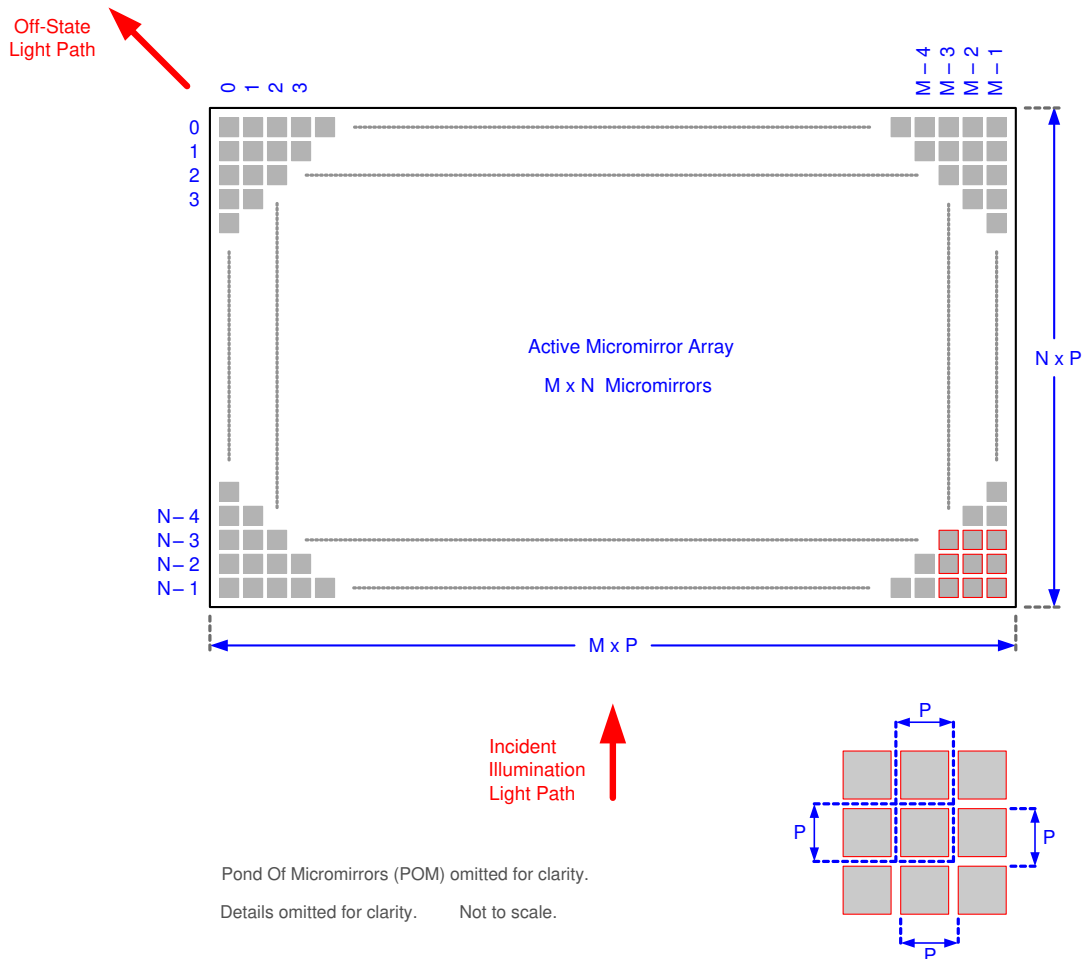

Figure 6-14. Micromirror Array Physical Characteristics

Product Folder Links: *DLP471TP*

6.11 Micromirror Array Optical Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Micromirror tilt angle		Landed state [1]		17		°
Micromirror tilt angle tolerance[2] [3] [4] [5]			−1.4		1.4	°
Micromirror tilt direction [6] [7]		Landed ON state		270		°
Micromirror tilt direction [6] [7]		Landed OFF state		180		°
Micromirror crossover time [8]		Typical performance		1	3	µs
Micromirror switching time [9]		Typical performance	6			µs
Image performance[10]	Bright pixel(s) in active area [11]	Gray 10 Screen [12]			0	micromirrors
	Bright pixel(s) in the POM [13]	Gray 10 Screen [12]			1	micromirrors
	Dark pixel(s) in the active area [14]	White Screen			4	micromirrors
	Adjacent pixel(s) [15]	Any Screen			0	micromirrors
	Unstable pixel(s) in active area [16]	Any Screen			0	micromirrors

(1) Measured relative to the plane formed by the overall micromirror array.
(2) Additional variation exists between the micromirror array and the package datums.
(3) Represents the landed tilt angle variation relative to the nominal landed tilt angle.
(4) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
(5) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations or system contrast variations.
(6) When the micromirror array is landed (not parked), the tilt direction of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of 1 results in a micromirror landing in the ON State direction. A binary value of 0 results in a micromirror landing in the OFF State direction. See Figure 6-15.
(7) Micromirror tilt direction is measured as in a typical polar coordinate system: Measuring counter-clockwise from a 0° degree reference which is aligned with the +X Cartesian axis.
(8) The time required for a micromirror to nominally transition from one landed state to the opposite landed state.
(9) The minimum time between successive transitions of a micromirror.
(10) Conditions of Acceptance: All DMD image quality returns will be evaluated using the following projected image test conditions:
   Test set degamma shall be linear
   Test set brightness and contrast shall be set to nominal
   The diagonal size of the projected image shall be a minimum of 20 inches
   The projections screen shall be 1X gain
   The projected image shall be inspected from a 38 inch minimum viewing distance
   The image shall be in focus during all image quality tests
(11) Bright pixel definition: A single pixel or mirror that is stuck in the ON position and is visibly brighter than the surrounding pixels
(12) Gray 10 screen definition: All areas of the screen are colored with the following settings:
   Red = 10/255
   Green = 10/255
   Blue = 10/255
(13) POM definition: Rectangular border of off-state mirrors surrounding the active area
(14) Dark pixel definition: A single pixel or mirror that is stuck in the OFF position and is visibly darker than the surrounding pixels
(15) Adjacent pixel definition: Two or more stuck pixels sharing a common border or common point, also referred to as a cluster
(16) Unstable pixel definition: A single pixel or mirror that does not operate in sequence with parameters loaded into memory. The unstable pixel appears to be flickering asynchronously with the image
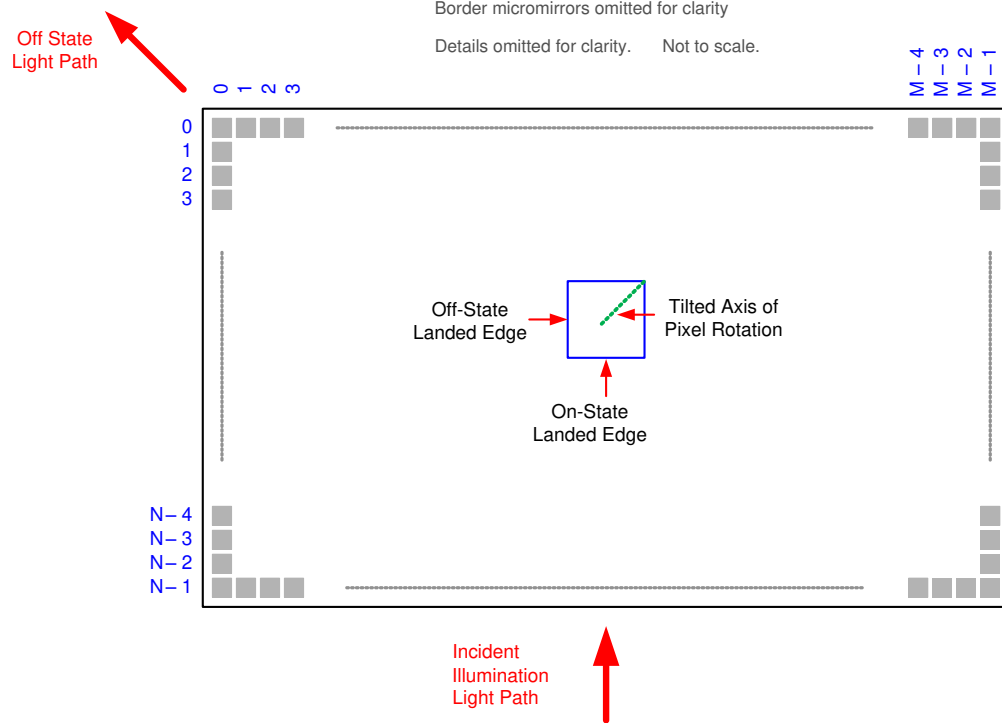
Figure 6-15. Micromirror Landed Orientation and Tilt

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6.12 Window Characteristics

DESCRIPTION[1]		MIN	TYP	MAX
Window material			Corning Eagle XG	
Window refractive index	At wavelength 546.1 nm		1.5119	
Window aperture [2]			See [2].	
Illumination overfill [3]			See [3].	
Window transmittance, single-pass through both surfaces and glass	Minimum within the wavelength range 420 nm to 680 nm. Applies to all angles 0° to 30° AOI[4]	97%		
	Average over the wavelength range 420 nm to 680 nm. Applies to all angles 30° to 45° AOI[4]	97%		

(1) See Section 7.5 for more information.
(2) See the package mechanical characteristics for details regarding the size and location of the window aperture.
(3) The active area of the DLP471TP device is surrounded by an aperture on the inside of the DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical conditions. Overfill light illuminating the area outside the active array can scatter and create adverse effects to the performance of an end application using the DMD. The illumination optical system should be designed to limit light flux incident outside the active array to less than 10% of the average flux level in the active area. Depending on the particular system's optical architecture and assembly tolerances, the amount of overfill light on the outside of the active array may cause system performance degradation.
(4) Angle of incidence (AOI) is the angle between an incident ray and the normal to a reflecting or refracting surface.

6.13 Chipset Component Usage Specification

Reliable function and operation of the DLP471TP DMD requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology consists of the TI technology and devices used for operating or controlling a DLP DMD.

Note

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

7 Detailed Description

7.1 Overview

The DMD is a 0.47-inch diagonal spatial light modulator which consists of an array of highly reflective aluminum micromirrors. The DMD is an electrical input, optical output micro-optical-electrical-mechanical system (MOEMS). The fast switching speed of the DMD micromirrors combined with advanced DLP image processing algorithms enables each micromirror to display four distinct pixels on the screen during every frame, resulting in a full 3840 × 2160 pixel image being displayed. The electrical interface is low voltage differential signaling (LVDS). The DMD consists of a two-dimensional array of 1-bit CMOS memory cells. The array is organized in a grid of M memory cell columns by N memory cell rows. Refer to the Functional Block Diagram. The positive or negative deflection angle of the micromirrors can be individually controlled by changing the address voltage of underlying CMOS addressing circuitry and micromirror reset signals (MBRST).

The DLP 0.47" 4K UHD chipset is comprised of the DLP471TP DMD, DLPC6540 display controller, and the DLPA3005 PMIC and the LED driver. To ensure reliable operation, the DLP471TP DMD must always be used with the DLP display controller and the PMIC specified in the chipset.

7.2 Functional Block Diagram

Product Folder Links: *DLP471TP*
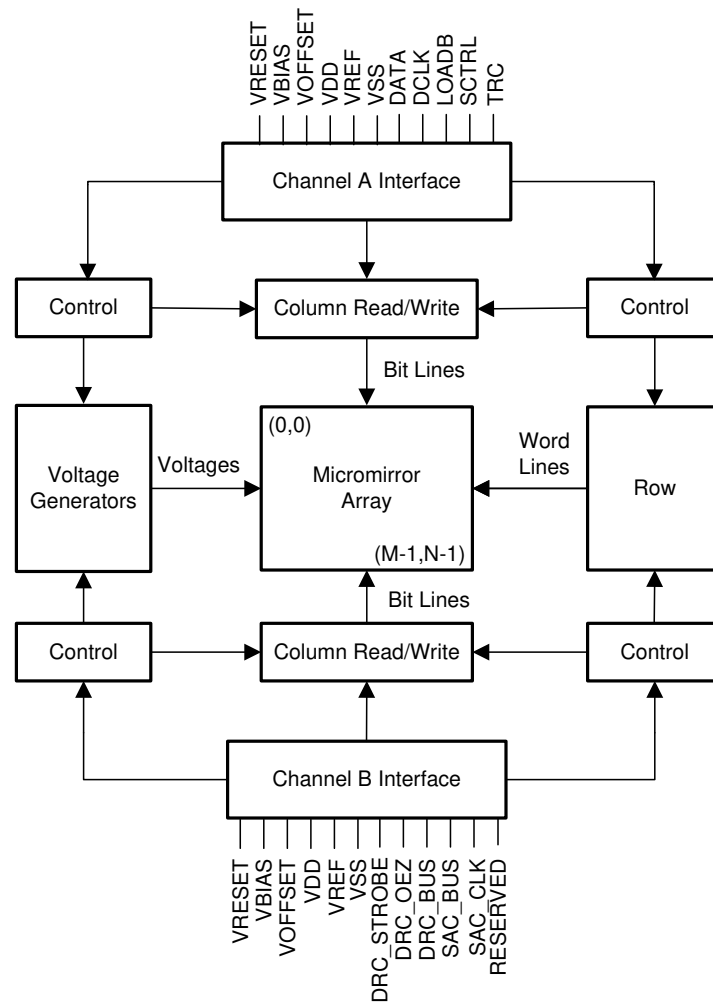
7.3 Feature Description

7.3.1 Power Interface

The DMD requires 4 DC voltages: 1.8 V source, V_{OFFSET}, V_{RESET}, and V_{BIAS}. In a typical LED-based system, 1.8 V is provided by a TPS54320 and the V_{OFFSET}, V_{RESET}, and V_{BIAS} is managed by the DLPA3005 PMIC and LED driver.

7.3.2 Timing

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be considered. Timing reference loads are not intended to be precise representations of any particular system environment or depiction of the actual load presented by a production test. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

7.4 Device Functional Modes

DMD functional modes are controlled by the DLPC6540 display controller. See the DLPC6540 display controller data sheet or contact a TI applications engineer.

7.5 Optical Interface and System Image Quality Considerations

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

7.5.1 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This angle should not exceed the nominal device micromirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The micromirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the micromirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle (and vice versa), contrast degradation and objectionable artifacts in the display border and/or active area could occur.

7.5.2 Pupil Match

TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

7.5.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view, and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. The illumination optical system should be designed to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system optical architecture, overfill light may have to be further reduced below the suggested 10% level in order to be acceptable.
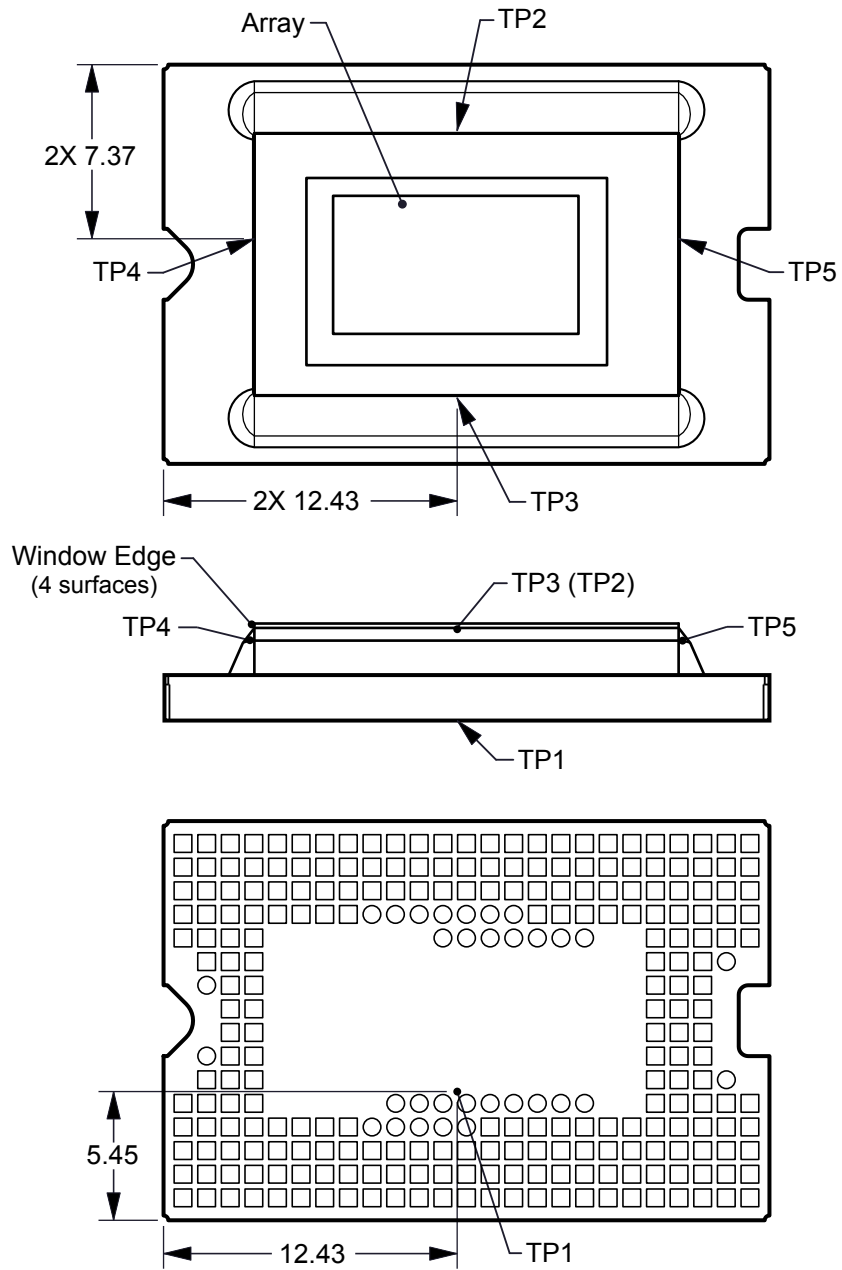
7.6 Micromirror Array Temperature Calculation

Figure 7-1. DMD Thermal Test Points

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Micromirror array temperature cannot be measured directly, therefore it must be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The relationship between array temperature and the reference ceramic temperature (thermal test TP1 in Figure 7-1) is provided by the following equations:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY\text{-}TO\text{-}CERAMIC})$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION}$$

where

- T_{ARRAY} = Computed array temperature (°C)

- $T_{CERAMIC}$ = Measured ceramic temperature (°C) (TP1 location)

- $R_{ARRAY\text{-}TO\text{-}CERAMIC}$ = Thermal resistance of package specified in *Section 6.5* from array to ceramic TP1 (°C/Watt)

- Q_{ARRAY} = Total DMD power on the array (W) (electrical + absorbed)

- $Q_{ELECTRICAL}$ = Nominal electrical power (W)

- $Q_{INCIDENT}$ = Incident illumination optical power (W)

- $Q_{ILLUMINATION}$ = (DMD average thermal absorptivity × $Q_{INCIDENT}$) (W)

- DMD average thermal absorptivity = 0.4

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates and operating frequencies. A nominal electrical power dissipation to use when calculating array temperature is 2.5 Watts. The absorbed power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. The equations shown above are valid for a single chip or multichip DMD system. It assumes an illumination distribution of 83.7% on the active array, and 16.3% on the array border.

The sample calculation for a typical projection application is as follows:

$Q_{INCIDENT}$ = 9.4 W (measured)

$T_{CERAMIC}$ = 55.0°C (measured)

$Q_{ELECTRICAL}$ = 2.5 W

Q_{ARRAY} = 2.5 W + (0.40 × 9.4 W) = 6.26 W

T_{ARRAY} = 55.0°C + (6.26 W × 1.0°C/W) = 61.3°C

7.7 Micromirror Power Density Calculation

The calculation of the optical power density of the illumination on the DMD in the different wavelength bands uses the total measured optical power on the DMD, percent illumination overfill, area of the active array, and ratio of the spectrum in the wavelength band of interest to the total spectral optical power.

- $ILL_{UV} = [OP_{UV\text{-}RATIO} \times Q_{INCIDENT}] \times 1000 \div A_{ILL}$ (mW/cm^2)
- $ILL_{VIS} = [OP_{VIS\text{-}RATIO} \times Q_{INCIDENT}] \div A_{ILL}$ (W/cm^2)
- $ILL_{IR} = [OP_{IR\text{-}RATIO} \times Q_{INCIDENT}] \times 1000 \div A_{ILL}$ (mW/cm^2)
- $ILL_{BLU} = [OP_{BLU\text{-}RATIO} \times Q_{INCIDENT}] \div A_{ILL}$ (W/cm^2)
- $ILL_{BLU1} = [OP_{BLU1\text{-}RATIO} \times Q_{INCIDENT}] \div A_{ILL}$ (W/cm^2)
- $A_{ILL} = A_{ARRAY} \div (1 - OV_{ILL})$ (cm^2)

where:

- ILL_{UV} = UV illumination power density on the DMD (mW/cm^2)

- ILL_{VIS} = VIS illumination power density on the DMD (W/cm^2)

- ILL_{IR} = IR illumination power density on the DMD (mW/cm^2)

- ILL_{BLU} = BLU illumination power density on the DMD (W/cm^2)

- ILL_{BLU1} = BLU1 illumination power density on the DMD (W/cm^2)

- A_{ILL} = illumination area on the DMD (cm^2)

- $Q_{INCIDENT}$ = total incident optical power on DMD (W) (measured)

- A_{ARRAY} = area of the array (cm^2) (data sheet)

- OV_{ILL} = percent of total illumination on the DMD outside the array (%) (optical model)

- $OP_{UV-RATIO}$ = ratio of the optical power for wavelengths <410 nm to the total optical power in the illumination spectrum (spectral measurement)

- $OP_{VIS-RATIO}$ = ratio of the optical power for wavelengths ≥410 and ≤800 nm to the total optical power in the illumination spectrum (spectral measurement)

- $OP_{IR-RATIO}$ = ratio of the optical power for wavelengths >800 nm to the total optical power in the illumination spectrum (spectral measurement)

- $OP_{BLU-RATIO}$ = ratio of the optical power for wavelengths ≥410 and ≤475 nm to the total optical power in the illumination spectrum (spectral measurement)

- $OP_{BLU1-RATIO}$ = ratio of the optical power for wavelengths ≥410 and ≤445 nm to the total optical power in the illumination spectrum (spectral measurement)

The illumination area varies and depends on the illumination overfill. The total illumination area on the DMD is the array area and overfill area around the array. The optical model is used to determine the percent of the total illumination on the DMD that is outside the array (OV_{ILL}) and the percent of the total illumination that is on the active array. From these values the illumination area (A_{ILL}) is calculated. The illumination is assumed to be uniform across the entire array.

From the measured illumination spectrum, the ratio of the optical power in the wavelength bands of interest to the total optical power is calculated.

Sample calculation:

$Q_{INCIDENT}$ = 9.40 W (measured)

A_{ARRAY} = (1.0368 × 0.5832) = 0.6047 cm^2 (data sheet)

OV_{ILL} = 16.3% (optical model)

$OP_{UV-RATIO}$ = 0.00021 (spectral measurement)

$OP_{VIS-RATIO}$ = 0.99977 (spectral measurement)

$OP_{IR-RATIO}$ = 0.00002 (spectral measurement)

$OP_{BLU-RATIO}$ = 0.28100 (spectral measurement)

$OP_{BLU1-RATIO}$ = 0.03200 (spectral measurement)

A_{ILL} = 0.6047 ÷ (1 - 0.163) = 0.7224 cm^2

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$ILL_{UV} = [0.00021 \times 9.40W] \times 1000 \div 0.7224\ cm^2 = 2.732\ mW/cm^2$

$ILL_{VIS} = [0.99977 \times 9.40W] \div 0.7224\ cm^2 = 13.01\ W/cm^2$

$ILL_{IR} = [0.00002 \times 9.40W] \times 1000 \div 0.7224\ cm^2 = 0.260\ mW/cm^2$

$ILL_{BLU} = [0.28100 \times 9.40W] \div 0.7224\ cm^2 = 3.66\ W/cm^2$

$ILL_{BLU1} = [0.03200 \times 9.40W] \div 0.7224\ cm^2 = 0.42\ W/cm^2$

7.8 Micromirror Landed-On/Landed-Off Duty Cycle

7.8.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the percentage of time that an individual micromirror is landed in the ON state versus the amount of time the same micromirror is landed in the OFF state.

For example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the ON state 100% of the time (and in the OFF state 0% of the time); whereas 0/100 would indicate that the pixel is in the OFF state 100% of the time. Likewise, 50/50 indicates that the pixel is ON for 50% of the time (and OFF for 50% of the time).

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) always add to 100.

7.8.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD useful life.

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

7.8.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD temperature and landed duty cycle interact to affect DMD useful life, and this interaction can be exploited to reduce the impact that an asymmetrical landed duty cycle has on the DMD useful life. This is quantified in the de-rating curve shown in Figure 6-1. The importance of this curve is that:

- All points along this curve represent the same useful life.
- All points above this curve represent lower useful life (and the further away from the curve, the lower the useful life).
- All points below this curve represent higher useful life (and the further away from the curve, the higher the useful life).

In practice, this curve specifies the maximum operating DMD temperature that the DMD should be operated at for a given long-term average landed duty cycle.

7.8.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the landed duty cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel operates under a 100/0 landed duty cycle during that time period. Likewise, when displaying pure-black, the pixel operates under a 0/100 landed duty cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the landed duty cycle tracks one-to-one with the gray scale value, as shown in Table 7-1.

Table 7-1. Grayscale Value and Landed Duty Cycle

GRAYSCALE VALUE	LANDED DUTY CYCLE
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and/or blue) for the given pixel as well as the color cycle time for each primary color, where "color cycle time" is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

Use Equation 5 to calculate the landed duty cycle of a given pixel during a given time period

$$\text{Landed Duty Cycle} = (\text{Red\_Cycle\_\%} \times \text{Red\_Scale\_Value}) + (\text{Green\_Cycle\_\%} \times \text{Green\_Scale\_Value}) + (\text{Blue\_Cycle\_\%} \times \text{Blue\_Scale\_Value}) \quad (5)$$

where

- Red_Cycle_%, represents the percentage of the frame time that red is displayed to achieve the desired white point
- Green_Cycle_% represents the percentage of the frame time that green is displayed to achieve the desired white point
- Blue_Cycle_%, represents the percentage of the frame time that blue is displayed to achieve the desired white point

For example, assume that the red, green, and blue color cycle times are 30%, 50%, and 20% respectively (in order to achieve the desired white point), then the landed duty cycle for various combinations of red, green, blue color intensities would be as shown in Table 7-2 and Table 7-3.

Table 7-2. Example Landed Duty Cycle for Full-Color, Color Percentage

CYCLE PERCENTAGE		
RED	**GREEN**	**BLUE**
30%	50%	20%

Product Folder Links: *DLP471TP*

Texas Instruments
www.ti.com

Table 7-3. Example Landed Duty Cycle for Full-Color

SCALE VALUE			LANDED DUTY CYCLE
RED	GREEN	BLUE	
0%	0%	0%	0/100
100%	0%	0%	50/50
0%	100%	0%	20/80
0%	0%	100%	30/70
12%	0%	0%	6/94
0%	35%	0%	7/93
0%	0%	60%	18/82
100%	100%	0%	70/30
0%	100%	100%	50/50
100%	0%	100%	80/20
12%	35%	0%	13/87
0%	35%	60%	25/75
12%	0%	60%	24/76
100%	100%	100%	100/0

The last factor to account for in estimating the landed duty cycle is any applied image processing. Within the DLPC6540 controller, the gamma function affects the landed duty cycle.

Gamma is a power function of the form Output_Level = A × Input_Level^{Gamma}, where A is a scaling factor that is typically set to 1.

In the DLPC6540 controller, gamma is applied to the incoming image data on a pixel-by-pixel basis. A typical gamma factor is 2.2, which transforms the incoming data as shown in Figure 7-2.
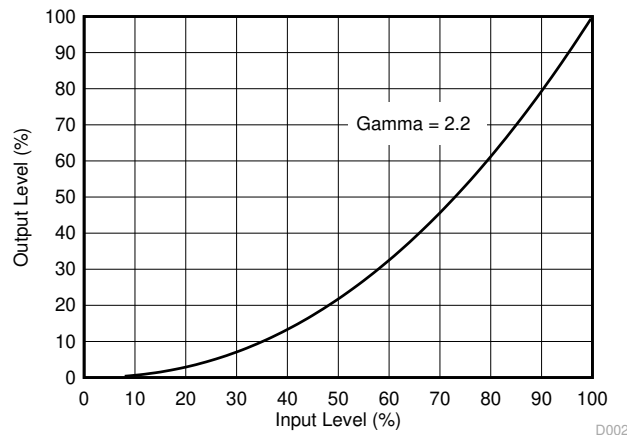
Figure 7-2. Example of Gamma = 2.2

From Figure 7-2, if the gray scale value of a given input pixel is 40% (before gamma is applied), then gray scale value will be 13% after gamma is applied. Therefore, it can be seen that since gamma has a direct impact displayed gray scale level of a pixel, it also has a direct impact on the landed duty cycle of a pixel.

Consideration must also be given to any image processing which occurs before the DLPC6540 controller.

Product Folder Links: *DLP471TP*

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the DLPC6540 controller. The high tilt pixel in the bottom-illuminated DMD increases brightness performance and enables a smaller system footprint for thickness constrained applications. Typical applications using the DLP471TP include mobile smart TV and digital signage.

DMD power-up and power-down sequencing is strictly controlled by the DLPA3005. Refer to Section 9 for power-up and power-down specifications. To ensure reliable operation, the DLP471TP DMD must always be used with DLPC6540 controller and a DLPA3005 PMIC/LED driver.

8.2 Typical Application

The DLP471TP DMD combined with DLPC6540 digital controller and a power management device provides full 4K UHD resolution for bright, colorful display applications. See Typical 4K UHD LED Application Diagram , which shows the system components needed along with the LED configuration of the DLP 0.47" 4K UHD chipset. The components include the DLP471TP DMD, DLPC6540 display controller and the DLPA3005 PMIC and LED driver.
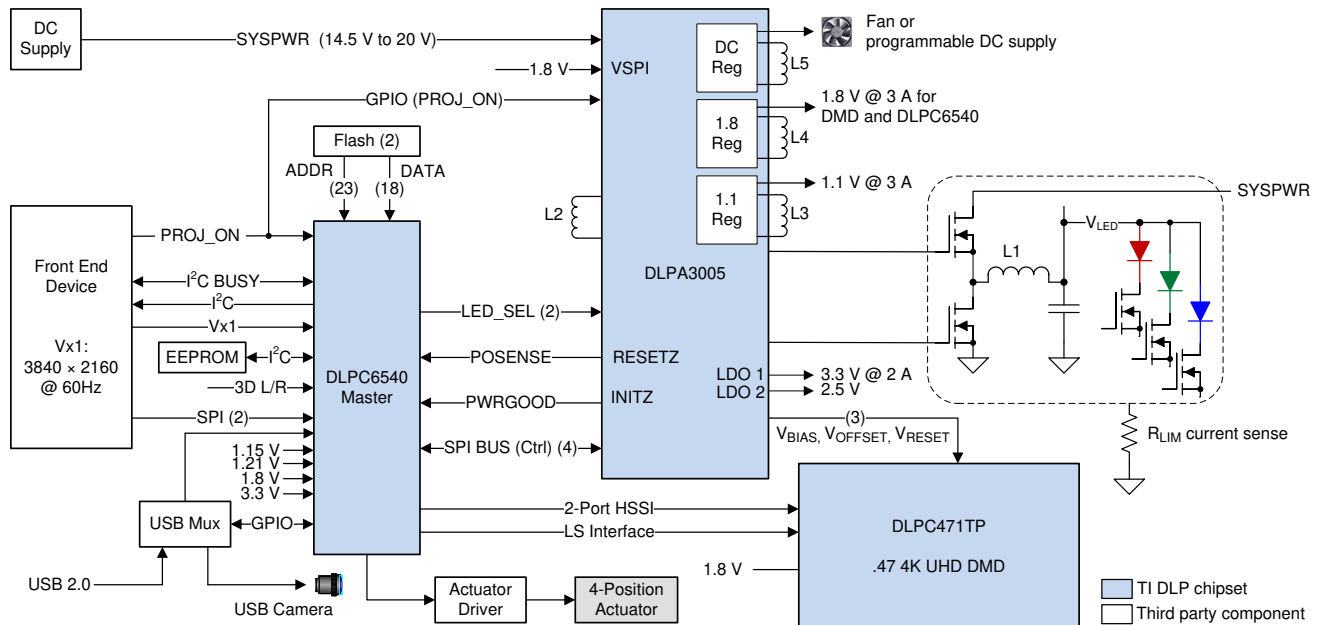

Figure 8-1. Typical 4K UHD LED Application Diagram

8.2.1 Design Requirements

Other core components of the display system include an illumination source, an optical engine for the illumination and projection optics, other electrical and mechanical components, and software. The type of illumination used and desired brightness will have a major effect on the overall system design and size.

The display system uses the DLP471TP as the core imaging device and contains a 0.47-inch array of micromirrors. The DLPC6540 controller is the digital interface between the DMD and the rest of the system, taking digital input from front end receiver and driving the DMD over a high-speed interface. The DLPA3005 PMIC serves as a voltage regulator for the DMD, controller, and LED illumination functionality.

8.2.2 Detailed Design Procedure

For a complete DLP system, an optical module or light engine is required that contains the DLP471TP DMD, associated illumination sources, optical elements, and necessary mechanical components.

To ensure reliable operation, the DMD must always be used with DLPC6540 display controller and the DLPA3005 PMIC and LED driver . Refer to PCB Design Requirements for TI DLP Pico TRP Digital Micromirror Devices for the DMD board design and manufacturing handling of the DMD sub assemblies.

8.2.3 Application Curves

The typical LED-current-to-luminance relationship when LED illumination is utilized is shown in Figure 8-2.
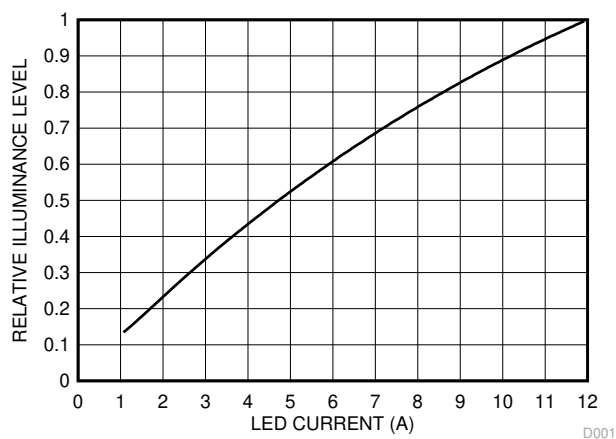
Figure 8-2. Luminance vs. Current

8.3 Temperature Sensor Diode

The software application provides functions to configure the TMP411 to read the DLP471TP DMD temperature sensor diode. Customers can use this data to incorporate additional functionality in the overall system design, such as adjusting illumination, fan speeds, and so on. All communication between the TMP411 and the DLPC6540 controller is completed using the I^{2}C interface. The TMP411 connects to the DMD through the pins outlined in Section 5.

9 Power Supply Recommendations

The following power supplies are all required to operate the DMD:

- V_{SS}
- V_{BIAS}
- V_{DD}
- V_{DDA}
- V_{OFFSET}
- V_{RESET}

DMD power-up and power-down sequencing is strictly controlled by the DLP display controller.

CAUTION

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to any of the prescribed power-up and power-down requirements may affect device reliability. See the DMD power supply sequencing requirements in Figure 9-1.

V_{BIAS}, V_{DD}, V_{DDA}, V_{OFFSET}, and V_{RESET} power supplies must be coordinated during power-up and power-down operations. Failure to meet any of the below requirements will result in a significant reduction in the DMD reliability and lifetime. Common ground V_{SS} must also be connected.

Table 9-1. Power Supply Sequence Requirements

| SYMBOL	PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{DELAY}	Delay requirement	from V_{OFFSET} power up to V_{BIAS} power up	2			ms
V_{OFFSET}	Supply voltage level	at beginning of power-up sequence delay[1]			6	V
V_{BIAS}	Supply voltage level	at end of power-up sequence delay[1]			6	V

(1) See Figure 9-1, Power-Up Sequence Delay Requirement.

9.1 DMD Power Supply Power-Up Procedure

- During power-up, V_{DD} and V_{DDA} must always start and settle before V_{OFFSET} plus Delay1 specified in Table 9-2, V_{BIAS}, and V_{RESET} voltages are applied to the DMD.
- During power-up, it is a strict requirement that the voltage difference between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in Section 6.4.
- During power-up, there is no requirement for the relative timing of V_{RESET} with respect to V_{BIAS}.
- Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements specified in Section 6.1, in Section 6.4, and in Figure 9-1.
- During power-up, LVCMOS input pins must not be driven high until after V_{DD} have settled at operating voltages listed in Section 6.4.

9.2 DMD Power Supply Power-Down Procedure

- During power-down, V_{DD} and V_{DDA} must be supplied until after V_{BIAS}, V_{RESET}, and V_{OFFSET} are discharged to within the specified limit of ground. See Table 9-2.
- During power-down, it is a strict requirement that the voltage difference between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in Section 6.4.
- During power-down, there is no requirement for the relative timing of V_{RESET} with respect to V_{BIAS}.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements specified in Section 6.1, in Section 6.4, and in Figure 9-1.
- During power-down, LVCMOS input pins must be less than specified in Section 6.4.
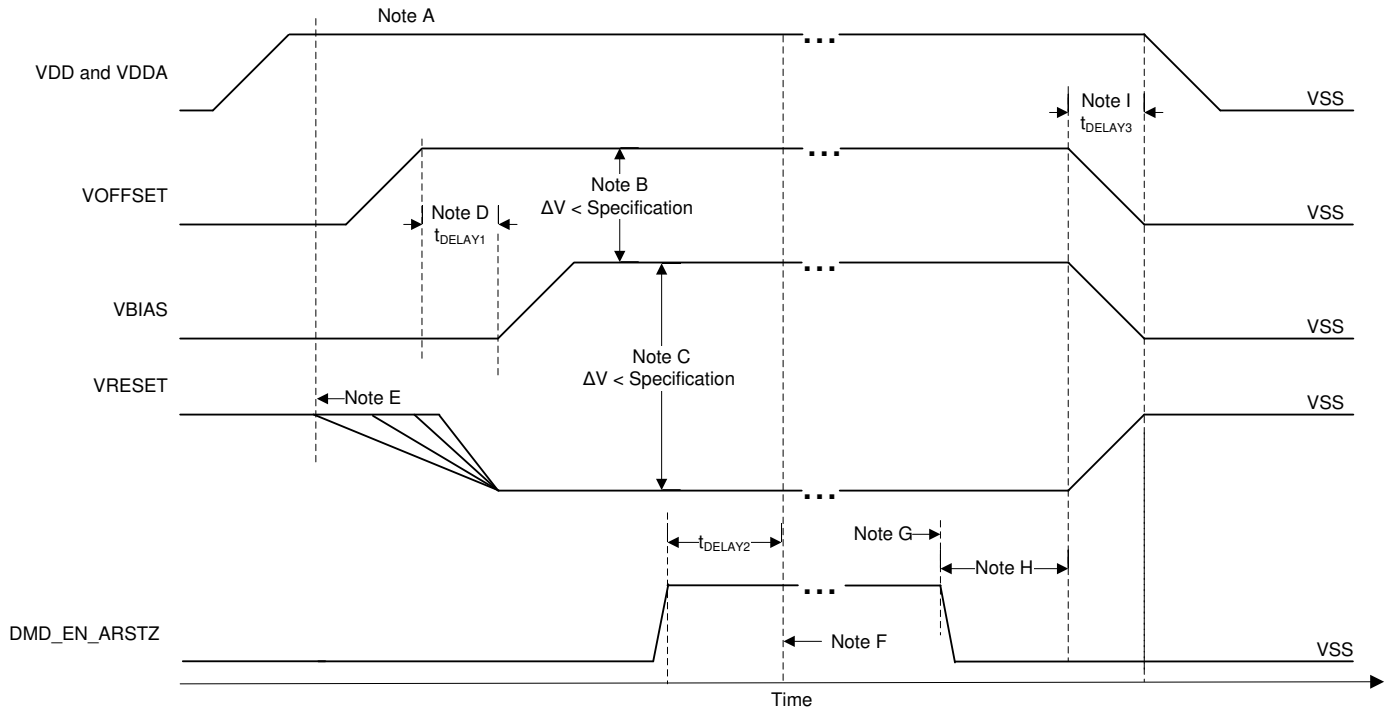
A. See Section 5 for the *Pin Functions Table*.

B. To prevent excess current, the supply voltage difference $|V_{OFFSET} - V_{BIAS}|$ must be less than the specified limit in Section 6.4.

C. To prevent excess current, the supply difference $|V_{BIAS} - V_{RESET}|$ must be less than the specified limit in Section 6.4.

D. V_{BIAS} should power up after V_{OFFSET} has powered up, per the Delay1 specification in Table 9-2.

E. DLP controller software initiates the global V_{BIAS} command.

F. After the DMD micromirror park sequence is complete, the DLP controller software initiates a hardware power-down that activates DMD_EN_ARSTZ and disables V_{BIAS}, V_{RESET}, and V_{OFFSET}.

G. Under power-loss conditions where emergency DMD micromirror park procedures are being enacted by the DLP controller hardware DMD_EN_ARSTZ will go low.

H. V_{DD} must remain high until after V_{OFFSET}, V_{BIAS}, V_{RESET} go low, per Delay2 specification in Table 9-2.

I. To prevent excess current, the supply voltage delta $|V_{DDA} - V_{DD}|$ must be less than specified limit in Section 6.4.

Figure 9-1. DMD Power Supply Requirements

Table 9-2. DMD Power-Supply Requirements

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNIT
Delay1[(1)]	Delay from V_{OFFSET} settled at recommended operating voltage to V_{BIAS} and V_{RESET} power up	1	2		ms
Delay2[(1)]	Delay V_{DD} must be held high from V_{OFFSET}, V_{BIAS} and V_{RESET} powering down.	50			us

(1) See Figure 9-1.

10 Layout

10.1 Layout Guidelines

The DLP471TP DMD is part of a chipset that is controlled by DLPC6540 display controller in conjunction with the DLPA3005 PMIC and LED driver. These guidelines are targeted at designing a PCB board with the DLP471TP DMD. The DMD board is a high-speed multi-layer PCB, with primarily high-speed digital logic including double data rate 3.2 Gbps and 250 Mbps differential data buses run to the DMD. TI recommends that full or mini power planes are used for V_{OFFSET}, V_{RESET}, and V_{BIAS}. Solid planes are required for ground (V_{SS}). The target impedance for the PCB is 50 Ω ±10% with exceptions listed in Table 10-1. TI recommends a 10 layer stack-up as described in Table 10-2. TI recommends manufacturing the PCB with a high quality FR-4 material.

10.2 Impedance Requirements

TI recommends a target impedance for the PCB of 50 Ω ±10% for all signals. The exceptions are listed in Table 10-1.

Table 10-1. Special Impedance Requirements

Signal Type	Signal Name	Impedance (ohms)
DMD High Speed Data Signals	DMD_HSSI0_N_(0…7), DMD_HSSI0_P_(0…7), DMD_HSSI1_N_(0…7), DMD_HSSI1_P_(0…7), DMD_HSSI0_CLK_N, DMD_HSSI0_CLK_P, DMD_HSSI1_CLK_N, DMD_HSSI1_CLK_P	100-Ω differential (50-Ω single ended)
DMD Low Speed Interface Signals	DMD_LS0_WDATA_N, DMD_LS0_WDATA_P, DMD_LS0_CLK_N, DMD_LS0_CLK_P	100-Ω differential (50-Ω single ended)

10.3 Layers

The layer stack-up and copper weight for each layer is shown in Table 10-2.

Table 10-2. Layer Stack-Up

LAYER NO.	LAYER NAME	COPPER WT. (oz.)	COMMENTS
1	Side A – DMD, primary components, power mini-planes	0.5 oz. (before plating)	DMD and escapes. Two data input connectors. Top components including power generation and two-data input connectors. Low frequency signals routing. Should have copper fill (GND) plated up to 1 oz.
2	Ground	0.5	Solid ground plane (net GND) reference for signal layers #1, 3
3	Signal (high frequency)	0.5	High-speed signal layer. High-speed differential data buses from input connector to DMD.
4	Ground	0.5	Solid ground plane (net GND) reference for signal layers #3, #5
5	Power	0.5	Primary split power planes for 1.8 V, 10 V, –14 V, 18 V
6	Power	0.5	Primary split power planes for 1.8 V, 10 V, –14 V, 18 V
7	Ground	0.5	Solid ground plane (net GND) reference for signal layer #8
8	Signal (high frequency)	0.5	High-speed signal layer. High-speed differential data buses from input connector to DMD
9	Ground	0.5	Solid ground plane (net GND) reference for signal layers #8, 10
10	Side B –secondary components, power mini-planes	0.5 oz. (before plating)	Discrete components if necessary. Low-frequency signals routing. Should have copper fill plated up to 1 oz.

10.4 Trace Width, Spacing

Unless otherwise specified, TI recommends that all signals follow the 0.005"/0.015" (Trace-Width/Spacing) design rule. Actual trace widths and clearances should be determined and calculated based on an analysis of impedance and stack-up requirements.

The width of all voltage signals shall be maximized as space permits. In particular, the following width and spacing requirements shall be observed for the specific signals listed in Table 10-3.

Table 10-3. Special Trace Widths, Spacing Requirements

SIGNAL NAME	MINIMUM TRACE WIDTH (MIL)	MINIMUM TRACE SPACING (MIL)	LAYOUT REQUIREMENT
GND	MAXIMIZE	5	Maximize trace width to connecting pin as a minimum.
P1P8V	100	15	Create mini planes on layers 1 and 10 as needed. Connect to devices on layers 1 and 10 as necessary with multiple vias.
V_{OFFSET}	40	15	Create mini planes on layers 1 and 10 as needed. Connect to devices on layers 1 and 10 as necessary.
V_{RESET}	40	15	Create mini planes on layers 1 and 10 as needed. Connect to devices on layers 1 and 10 as necessary.
V_{BIAS}	40	15	Create mini planes on layers 1 and 10 as needed. Connect to devices on layers 1 and 10 as necessary.

10.5 Power

TI strongly discourages signal routing on power planes or on planes adjacent to power planes. If signals must be routed on layers adjacent to power planes, they must not cross splits in power planes to prevent EMI and preserve signal integrity.

Have all internal digital ground (GND) planes connected together in as many places as possible. If possible, all internal ground planes should be connected together with a minimum distance between connections of 0.5". Extra vias may not be required if there are sufficient ground vias due to normal ground connections of devices.

The power and ground pins of each component should be connected to the power and ground planes with at least one via for each pin. Trace lengths for component power and ground pins should be minimized (ideally, less than 0.100").

Ground plane slots are strongly discouraged.

10.6 Trace Length Matching Recommendations

Recommended signal trace length matching requirements can be found in Table 10-4 and Table 10-5. When length matching traces, the longer signals should be routed in a serpentine fashion, keeping the number of turns to a minimum and the turn angles no sharper than 45 degrees as opposed to running long traces over large areas of the PCB.

Signals in Table 10-4 should be routed for data rate operation at up to 3.2 Gbps. Layer changes for these signals should be minimized, the number of vias should be minimized. Avoid sharp turns and layer switching while keeping lengths to a minimum. When layer changes are necessary, GND vias should be placed around the signal vias to provide a signal return path. The distance from one pair of differential signals to another shall be at least 2 times the distance within the pair.

Table 10-4. HSSI High Speed DMD Data Signals

SIGNAL NAME	REFERENCE SIGNAL	Routing Spec	Unit
DMD_HSSI0_N(0...7), DMD_HSSI0_P(0...7)	DMD_HSSI0_CLK_N, DMD_HSSI_CLK_P	+/- 0.25	inch
DMD_HSSI1_N(0...7), DMD_HSSI1_P(0...7)	DMD_HSSI0_CLK_N, DMD_HSSI_CLK_P	+/- 0.25	inch
DMD_HSSI0_CLK_P	DMD_HSSI1_CLK_P	+/- 0.05	inch
Intra-pair P	Intra-pair N	+/- 0.01	inch

Table 10-5. Other Timing Critical Signals

SIGNAL NAME	Constraints	Routing Layers
LS_CLK_P, LS_CLK_N LS_WDATA_P, LS_WDATA_N LS_RDATA_A	Intra-pair (P to N) Matched to 0.01 inches Signal-to-signal Matched to +/- 0.25 inches	Layers 3, 8

Product Folder Links: DLP471TP

11 Device and Documentation Support

11.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Device Support

11.2.1 Device Nomenclature
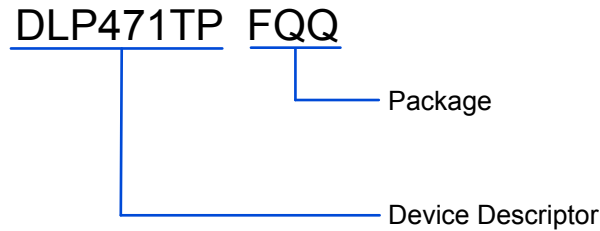
DLP471TP FQQ

— Package

— Device Descriptor

Figure 11-1. Part Number Description

11.2.2 Device Markings

The device marking includes both human-readable information and a 2-dimensional matrix code. The human-readable information is described in Figure 11-2 and includes the legible character string GHJJJJK DLP471TPFQQ. GHJJJJK is the lot trace code and DLP471TPFQQ is the device marking.
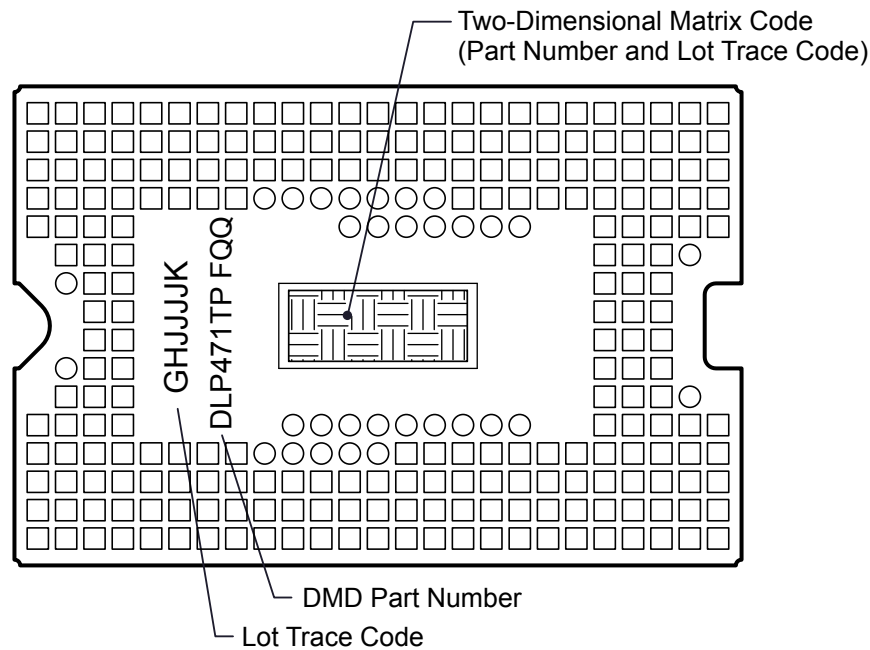
Example: GHJJJJK DLP471TPFQQ

Two-Dimensional Matrix Code
(Part Number and Lot Trace Code)

GHJJJJK

DLP471TP FQQ

DMD Part Number

Lot Trace Code

Figure 11-2. DMD Marking Locations

Product Folder Links: *DLP471TP*

11.3 Documentation Support

11.3.1 Related Documentation

The following documents contain additional information related to the chipset components used with the DMD.

- *DLPC6540 Display Controller Data Sheet*
- *DLPA3005 PMIC/LED Driver Data Sheet*

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 Trademarks

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DLP® is a registered trademark of Texas Instruments.

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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Product Folder Links: *DLP471TP*

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DLP471TPFQQ	Active	Production	CLGA (FQQ) | 270	54 | JEDEC TRAY (5+1)	Yes	NIAU	N/A for Pkg Type	0 to 70	
DLP471TPFQQ.B	Active	Production	CLGA (FQQ) | 270	54 | JEDEC TRAY (5+1)	Yes	NIAU	N/A for Pkg Type	0 to 70	

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TRAY

L - Outer tray length without tabs

KO - Outer tray height

W - Outer tray width

P1 - Tray unit pocket pitch

CW - Measurement for tray edge (Y direction) to corner pocket center

CL - Measurement for tray edge (X direction) to corner pocket center

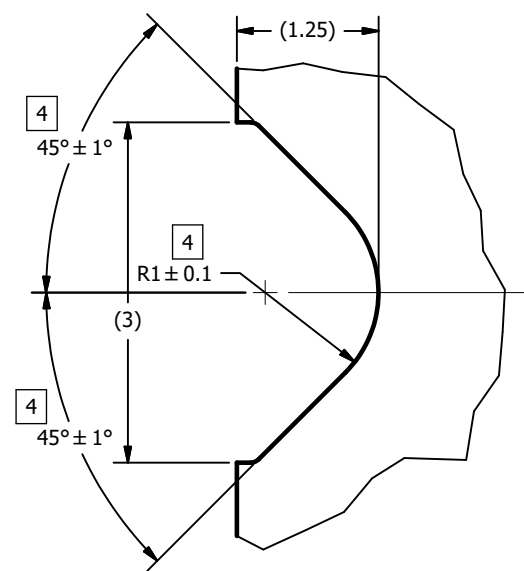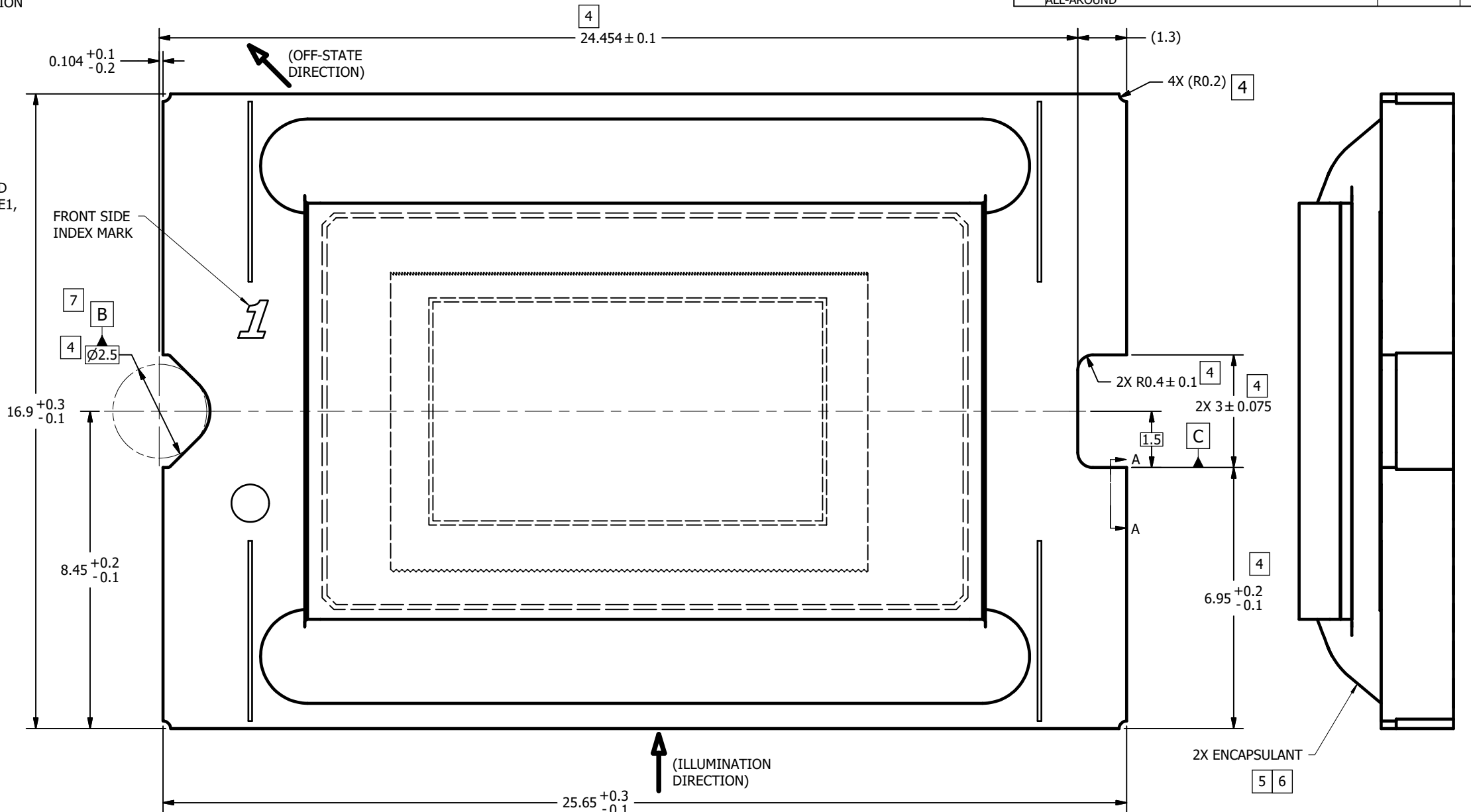Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DLP471TPFQQ	FQQ	CLGA	270	54	6 x 9	150	315	135.9	12190	31.5	31.5	16.2
DLP471TPFQQ.B	FQQ	CLGA	270	54	6 x 9	150	315	135.9	12190	31.5	31.5	16.2

NOTES UNLESS OTHERWISE SPECIFIED:

1. DIE PARALLELISM TOLERANCES APPLY TO DMD ACTIVE ARRAY ONLY.

2. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.6 DEGREES.

3. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE ARRAY.

4. NOTCH DIMENSIONS ARE DEFINED BY UPPERMOST LAYERS OF CERAMIC, AS SHOWN IN SECTION A-A.

5. ENCAPSULANT TO BE CONTAINED WITHIN DIMENSIONS SHOWN IN VIEW D (SHEET 3). NO ENCAPSULANT IS ALLOWED ON TOP OF THE WINDOW.

6. ENCAPSULANT NOT TO EXCEED THE HEIGHT OF THE WINDOW.

7. SEE DETAIL B FOR "V-NOTCH" DIMENSIONS.

8. WHILE ONLY THE THREE DATUM A TARGET AREAS A1, A2, AND A3 ARE USED FOR MEASUREMENT, ALL 4 CORNERS SHOULD BE CONTACTED, INCLUDING E1, TO SUPPORT MECHANICAL LOADS.

REVISIONS

REV	DESCRIPTION	DATE	BY
A	ECO 2178176: INITIAL RELEASE	12/11/2018	BMH
B	ECO: 2187413: CHANGE SHORT APERTURE SLOTS TO ALL-AROUND	4/29/2020	PPC

24.454 ± 0.1

(1.3)

0.104 +0.1 / -0.2

(OFF-STATE DIRECTION)

4X (R0.2)

FRONT SIDE INDEX MARK

Ø2.5

16.9 +0.3 / -0.1

8.45 +0.2 / -0.1

2X R0.4 ± 0.1

2X 3 ± 0.075

1.5

6.95 +0.2 / -0.1

(ILLUMINATION DIRECTION)

25.65 +0.3 / -0.1

2X ENCAPSULANT

DETAIL B
V-NOTCH
SCALE 30 : 1

(1.25)

45° ± 1°

R1 ± 1

(3)

45° ± 1°

SECTION A-A
(ROTATED 90°)

(3)

0.35 MIN TYP

0 MIN TYP

1.403 ± 0.077

1.1 ± 0.05

0.042 A
0.02 D

ACTIVE ARRAY

0.78 ± 0.063

(2.183)

3 SURFACES INDICATED IN VIEW B (SHEET 2)

1.925 ± 0.1

H (SHEET 3)

H (SHEET 3)

UNLESS OTHERWISE SPECIFIED
● DIMENSIONS ARE IN MILLIMETERS
● TOLERANCES:
  ANGLES ± 1°
  2 PLACE DECIMALS ± 0.25
  1 PLACE DECIMALS ± 0.50
  DIMENSIONAL LIMITS APPLY BEFORE PROCESSED
● INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5M-1994
● REMOVE ALL BURRS AND SHARP EDGES
● PARENTHETICAL INFORMATION FOR REFERENCE ONLY

DRAWN	B. HASKETT	12/11/2018
ENGINEER	B. HASKETT	12/11/2018
QA/CE	K. DICKERSON	12/12/2018
CM	B. HASKETT	12/19/2018
	J. MCKINLEY	12/18/2018
APPROVED	HERMOSILLO	12/18/2018

TEXAS INSTRUMENTS
Dallas Texas

TITLE
ICD, MECHANICAL, DMD,
.47 4K HSSI SERIES 317
(FQQ PACKAGE)

SIZE D

DWG NO 2516402

REV B

SCALE 15:1

SHEET 1 OF 5

THIRD ANGLE PROJECTION

NEXT ASSY   USED ON
0314DA
APPLICATION

INV11-2006a

D

C

B

A

2X � 1.604 ⌝   2X ⌜ 22.65 ⌝   4X (1.5)

A3

4X (5)

A2

1

2X ⌜ 3.45 ⌝

⌀2.5

B

2X ⌜ 3.45 ⌝

1.5 C

8

E1

A1
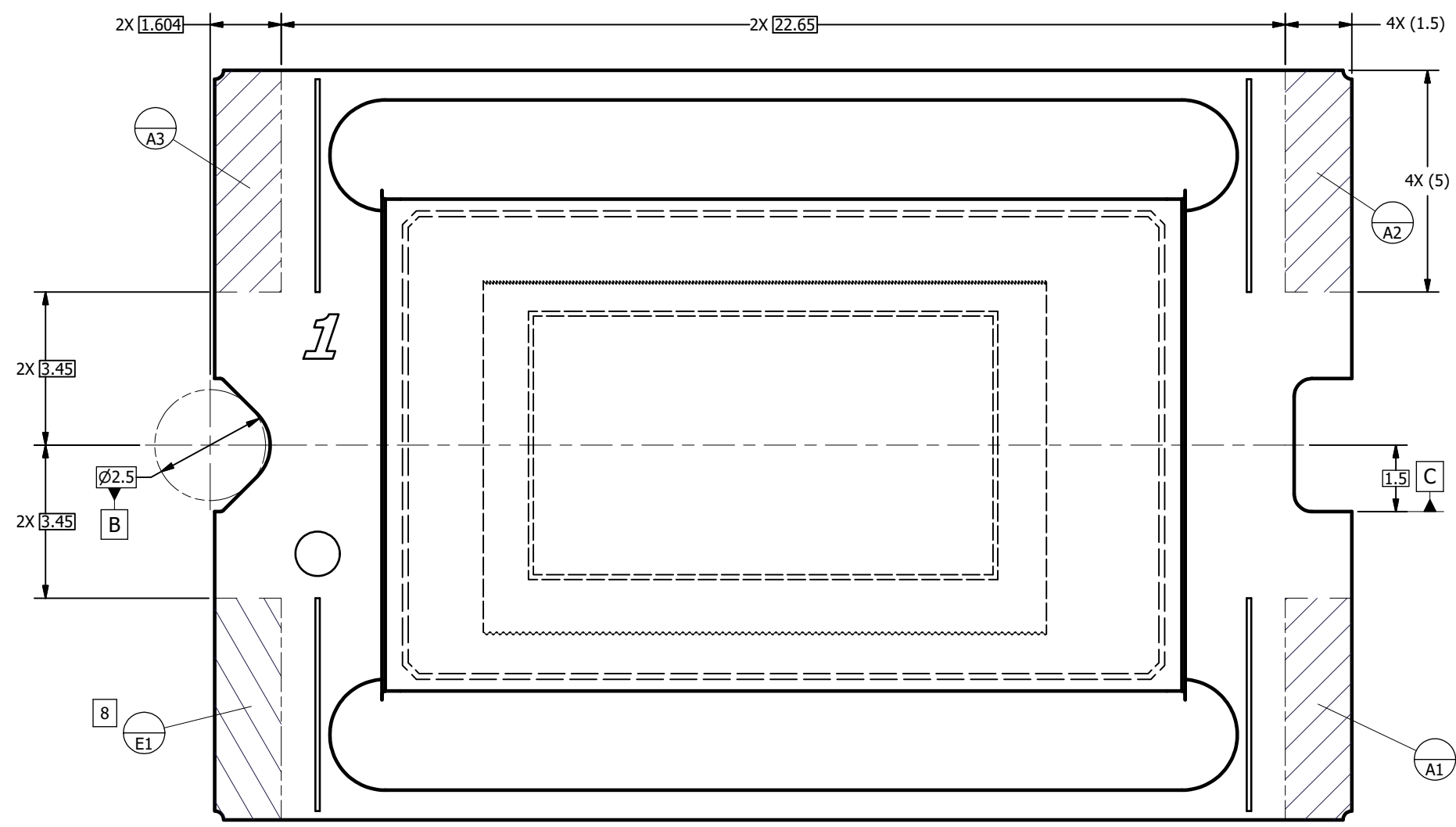
VIEW C
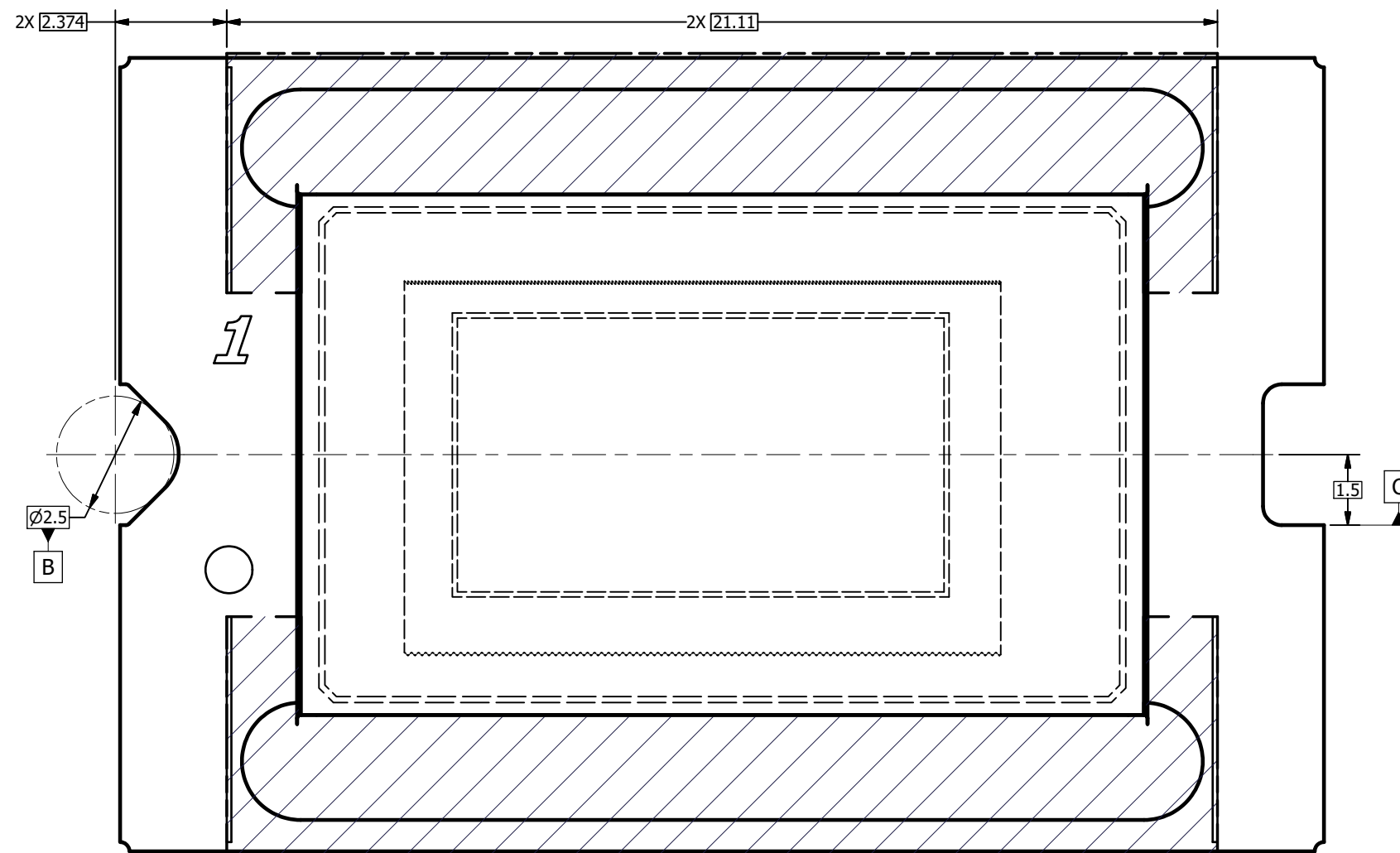**DATUMS A AND E**
(FROM SHEET 1)

2X 2.374

2X 21.11

1

Ø2.5

B

1.5   C

VIEW D
ENCAPSULANT MAXIMUM X/Y DIMENSIONS 5
(FROM SHEET 1)

6
2X 0 MIN
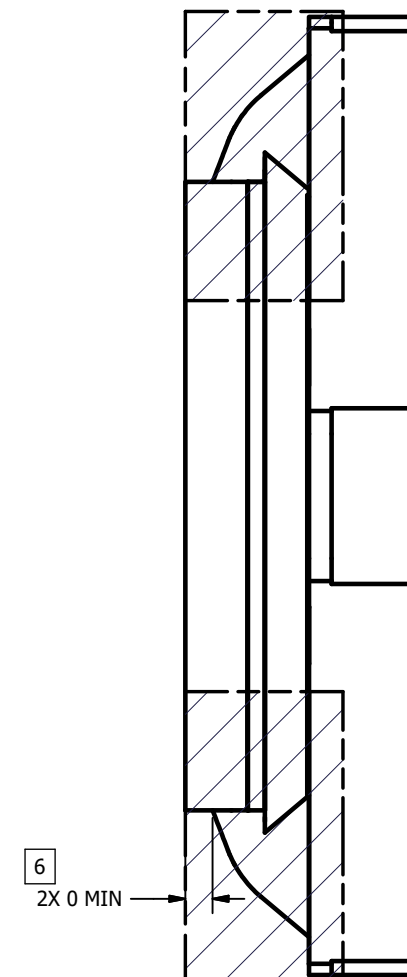
VIEW E
MAXIMUM ENCAPSULANT HEIGHT

6

INV11-2006a

(OFF-STATE DIRECTION)

2 7.29 ± 0.075

(10.368) ACTIVE ARRAY

4X (0.108) 3

(0.075) TYP.

(42°) TYP.

(0.068) TYP.

DETAIL F
APERTURE TOP EDGE
(GLASS OMITTED FOR CLARITY)
SCALE 60 : 1

2.633 ± 0.05

2 2.91 ± 0.075

(11.085) WINDOW

(5.832) ACTIVE ARRAY

Ø2.5 B

8.452 ± 0.05

F

G

0.754 ± 0.0635

7.155 ± 0.0635

1.5 C

(7.909) APERTURE

(0.15) TYP.

(42°) TYP.

(42°) TYP.

(0.068) TYP.
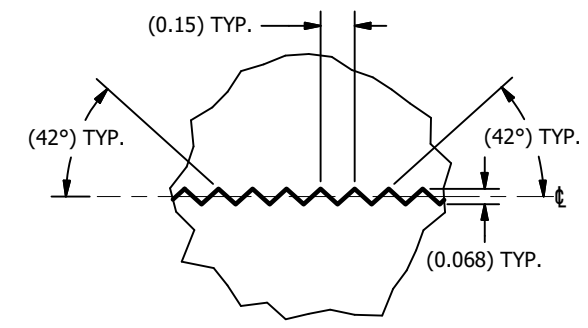
DETAIL G
APERTURE BOTTOM EDGE
(GLASS OMITTED FOR CLARITY)
SCALE 60 : 1

(ILLUMINATION DIRECTION)

1.127 ±0.0635

11.574 ± 0.0635

(12.701) APERTURE

3.34 ± 0.05

14.63 ± 0.05

(17.97) WINDOW

VIEW E
WINDOW AND ACTIVE ARRAY
(FROM SHEET 1)

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0.929

24 X 1 = 24

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25

T R P N M L K J H G F E D C B A

7.5

15 X 1 = 15

Ø2.5

B

BACK SIDE
INDEX MARK

CR

700-0

1.5 C

32X CIRCULAR TEST PADS
(Ø0.75)

SYMBOLIZATION PAD
(7 X 3)
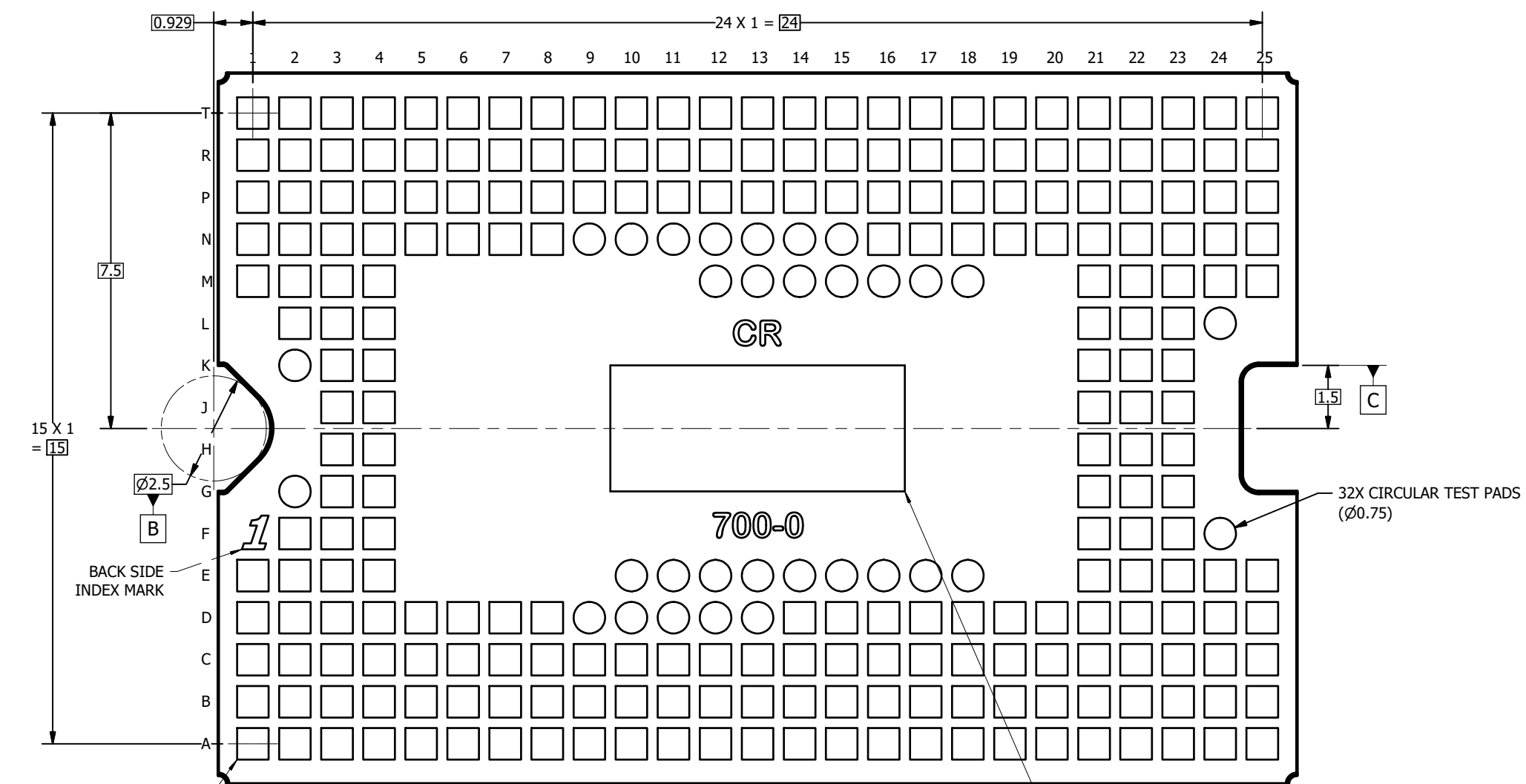
238X SQUARE LGA PADS
0.75±0.05 X 0.75±0.05
⌖ 0.2 A B C
⌖ 0.1 A

VIEW H-H
BACK SIDE METALIZATION
(FROM SHEET 1)

INV11-2006a

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