

# DLP473NE 0.47-Inch 1080p Digital Micromirror Device

## 1 Features

- 0.47-inch diagonal micromirror array
  - 1080p (1920 × 1080) display resolution
  - 5.4µm micromirror pitch
  - ±14.5° micromirror tilt (relative to flat surface)
  - Corner illumination
- SubLVDS input data bus
- Supports 1080p up to 240Hz
- RGB laser, LED and Laser Phosphor operation supported by DLPC8454 display controller

## 2 Applications

- [Smart projector](#)
- [Enterprise projector](#)
- [Laser TV](#)
- [Gaming projectors](#)
- [Home theaters](#)
- [Golf simulators](#)

## 3 Description

The DLP473NE digital micromirror device (DMD) is a digitally controlled micro-electromechanical system (MEMS) spatial light modulator (SLM) that enables bright 1080p display systems. The TI DLP® Products 0.47-inch 1080p chipset is composed of the DMD and DLPC8454 display controller, the [DLPA3082](#) PMIC, and the [DLPA100](#) color wheel driver. The compact physical size of the chipset provides a complete system solution that enables small form factor 1080p displays.

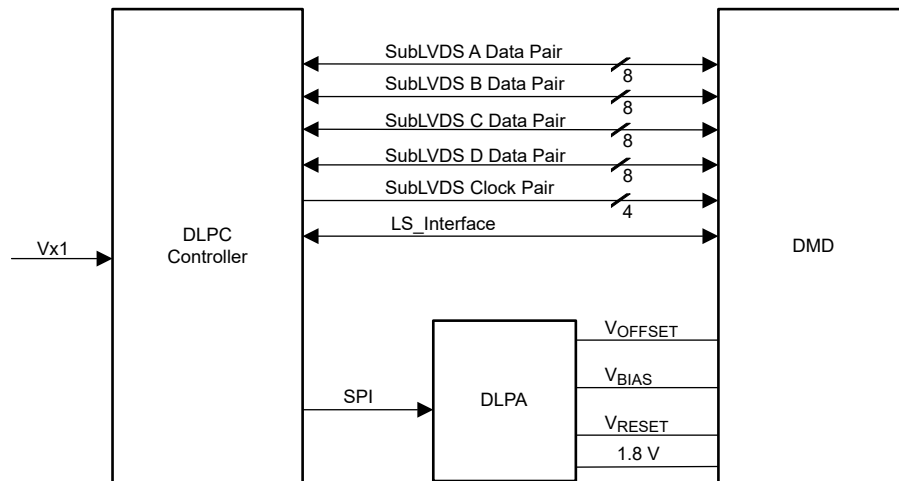
The DMD ecosystem includes established resources to help the user accelerate the design cycle, visit the [DLP® Products third-party search tools](#) to find approved optical module manufacturers and third-party providers.

Visit the [Getting Started with TI DLP display technology](#) page to learn more about how to start designing with the DMD.

### Device Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE
DLP473NE	FXL (173)	32.2mm × 22.3mm

(1) For more information, see the *Mechanical, Packaging, and Orderable* addendum.



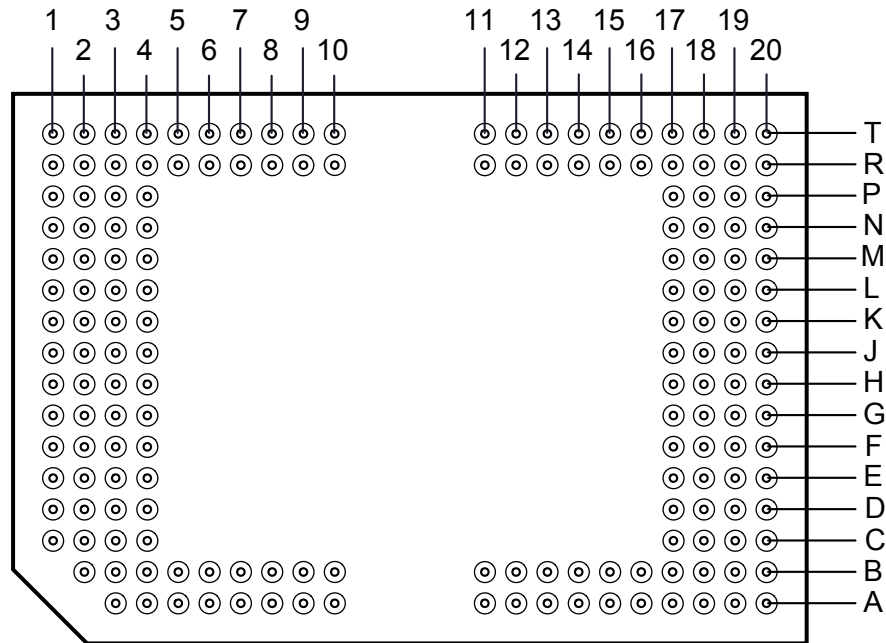
Simplified Application



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## 4 Pin Configuration and Functions



**Figure 4-1. FXL Package 173-Pin PGA Bottom View**

**CAUTION**

Properly manage the layout and the operation of signals identified in the Pin Functions table to make sure there is reliable, long-term operation of the 0.47" 1080p S460 DMD. Refer to the [PCB Design Requirements for TI DLP Digital Micromirror Devices](#) application report for specific details and guidelines before designing the board.

**Table 4-1. Pin Functions**

PIN		INPUT- OUTPUT <sup>(1)</sup>	DESCRIPTION	TERMINATION	TRACE LENGTH (mm)
NAME	ID				
D_AP(0)	R2	I	High-speed Differential Data Pair lane A0	Differential 100Ω	8.204
D_AN(0)	P2	I	High-speed Differential Data Pair lane A0	Differential 100Ω	8.201
D_AP(1)	T4	I	High-speed Differential Data Pair lane A1	Differential 100Ω	9.95
D_AN(1)	T3	I	High-speed Differential Data Pair lane A1	Differential 100Ω	9.95
D_AP(2)	P1	I	High-speed Differential Data Pair lane A2	Differential 100Ω	8.439
D_AN(2)	N1	I	High-speed Differential Data Pair lane A2	Differential 100Ω	8.44
D_AP(3)	R5	I	High-speed Differential Data Pair lane A3	Differential 100Ω	10.166
D_AN(3)	R6	I	High-speed Differential Data Pair lane A3	Differential 100Ω	10.167
D_AP(4)	T5	I	High-speed Differential Data Pair lane A4	Differential 100Ω	12.672
D_AN(4)	T6	I	High-speed Differential Data Pair lane A4	Differential 100Ω	12.673
D_AP(5)	K2	I	High-speed Differential Data Pair lane A5	Differential 100Ω	5.097
D_AN(5)	L2	I	High-speed Differential Data Pair lane A5	Differential 100Ω	5.094
D_AP(6)	T7	I	High-speed Differential Data Pair lane A6	Differential 100Ω	13.416
D_AN(6)	T8	I	High-speed Differential Data Pair lane A6	Differential 100Ω	13.416
D_AP(7)	J1	I	High-speed Differential Data Pair lane A7	Differential 100Ω	6.356

**Table 4-1. Pin Functions (continued)**

PIN		INPUT- OUTPUT <sup>(1)</sup>	DESCRIPTION	TERMINATION	TRACE LENGTH (mm)
NAME	ID				
D_AN(7)	K1	I	High-speed Differential Data Pair lane A7	Differential 100Ω	6.356
DCLK_AP	L1	I	High-speed Differential Clock A	Differential 100Ω	7.247
DCLK_AN	M1	I	High-speed Differential Clock A	Differential 100Ω	7.247
D_BP(0)	T13	I	High-speed Differential Data Pair lane B0	Differential 100Ω	9.167
D_BN(0)	T14	I	High-speed Differential Data Pair lane B0	Differential 100Ω	9.168
D_BP(1)	T17	I	High-speed Differential Data Pair lane B1	Differential 100Ω	10.163
D_BN(1)	T18	I	High-speed Differential Data Pair lane B1	Differential 100Ω	10.163
D_BP(2)	T12	I	High-speed Differential Data Pair lane B2	Differential 100Ω	12.753
D_BN(2)	T11	I	High-speed Differential Data Pair lane B2	Differential 100Ω	12.756
D_BP(3)	T15	I	High-speed Differential Data Pair lane B3	Differential 100Ω	14.679
D_BN(3)	T16	I	High-speed Differential Data Pair lane B3	Differential 100Ω	14.684
D_BP(4)	P20	I	High-speed Differential Data Pair lane B4	Differential 100Ω	10.903
D_BN(4)	N20	I	High-speed Differential Data Pair lane B4	Differential 100Ω	10.901
D_BP(5)	M20	I	High-speed Differential Data Pair lane B5	Differential 100Ω	10.043
D_BN(5)	L20	I	High-speed Differential Data Pair lane B5	Differential 100Ω	10.042
D_BP(6)	L19	I	High-speed Differential Data Pair lane B6	Differential 100Ω	8.167
D_BN(6)	K19	I	High-speed Differential Data Pair lane B6	Differential 100Ω	8.167
D_BP(7)	K20	I	High-speed Differential Data Pair lane B7	Differential 100Ω	7.373
D_BN(7)	J20	I	High-speed Differential Data Pair lane B7	Differential 100Ω	7.373
DCLK_BP	R19	I	High-speed Differential Clock B	Differential 100Ω	10.517
DCLK_BN	P19	I	High-speed Differential Clock B	Differential 100Ω	10.516
D_CP(0)	H1	I	High-speed Differential Data Pair lane C0	Differential 100Ω	6.308
D_CN(0)	G1	I	High-speed Differential Data Pair lane C0	Differential 100Ω	6.308
D_CP(1)	H2	I	High-speed Differential Data Pair lane C1	Differential 100Ω	4.941
D_CN(1)	G2	I	High-speed Differential Data Pair lane C1	Differential 100Ω	4.939
D_CP(2)	F1	I	High-speed Differential Data Pair lane C2	Differential 100Ω	7.011
D_CN(2)	E1	I	High-speed Differential Data Pair lane C2	Differential 100Ω	7.009
D_CP(3)	E2	I	High-speed Differential Data Pair lane C3	Differential 100Ω	6.959
D_CN(3)	D2	I	High-speed Differential Data Pair lane C3	Differential 100Ω	6.959
D_CP(4)	A4	I	High-speed Differential Data Pair lane C4	Differential 100Ω	10.185
D_CN(4)	A5	I	High-speed Differential Data Pair lane C4	Differential 100Ω	10.185
D_CP(5)	A7	I	High-speed Differential Data Pair lane C5	Differential 100Ω	9.34
D_CN(5)	A6	I	High-speed Differential Data Pair lane C5	Differential 100Ω	9.34
D_CP(6)	B7	I	High-speed Differential Data Pair lane C6	Differential 100Ω	9.109
D_CN(6)	B8	I	High-speed Differential Data Pair lane C6	Differential 100Ω	9.11
D_CP(7)	B5	I	High-speed Differential Data Pair lane C7	Differential 100Ω	7.548
D_CN(7)	B4	I	High-speed Differential Data Pair lane C7	Differential 100Ω	7.551
DCLK_CP	A9	I	High-speed Differential Clock C	Differential 100Ω	11.431
DCLK_CN	A8	I	High-speed Differential Clock C	Differential 100Ω	11.429
D_DP(0)	H19	I	High-speed Differential Data Pair lane D0	Differential 100Ω	5.531
D_DN(0)	G19	I	High-speed Differential Data Pair lane D0	Differential 100Ω	5.53
D_DP(1)	H20	I	High-speed Differential Data Pair lane D1	Differential 100Ω	7.153
D_DN(1)	G20	I	High-speed Differential Data Pair lane D1	Differential 100Ω	7.152
D_DP(2)	F20	I	High-speed Differential Data Pair lane D2	Differential 100Ω	7.449

**Table 4-1. Pin Functions (continued)**

PIN		INPUT- OUTPUT <sup>(1)</sup>	DESCRIPTION	TERMINATION	TRACE LENGTH (mm)
NAME	ID				
D_DN(2)	E20	I	High-speed Differential Data Pair lane D2	Differential 100Ω	7.449
D_DP(3)	E19	I	High-speed Differential Data Pair lane D3	Differential 100Ω	7.592
D_DN(3)	D19	I	High-speed Differential Data Pair lane D3	Differential 100Ω	7.592
D_DP(4)	B19	I	High-speed Differential Data Pair lane D4	Differential 100Ω	9.968
D_DN(4)	B18	I	High-speed Differential Data Pair lane D4	Differential 100Ω	9.967
D_DP(5)	A18	I	High-speed Differential Data Pair lane D5	Differential 100Ω	10.435
D_DN(5)	A17	I	High-speed Differential Data Pair lane D5	Differential 100Ω	10.435
D_DP(6)	B16	I	High-speed Differential Data Pair lane D6	Differential 100Ω	9.291
D_DN(6)	B15	I	High-speed Differential Data Pair lane D6	Differential 100Ω	9.293
D_DP(7)	A16	I	High-speed Differential Data Pair lane D7	Differential 100Ω	9.269
D_DN(7)	A15	I	High-speed Differential Data Pair lane D7	Differential 100Ω	9.274
DCCLK_DP	D20	I	High-speed Differential Clock D	Differential 100Ω	9.019
DCCLK_DN	C20	I	High-speed Differential Clock D	Differential 100Ω	9.02
LS_WDATA	L3	I	Low speed interface (LSIF) write data		3.907
LS_CLK	P4	I	Low speed interface (LSIF) clock		4.52
LS_RDATA_A	N4	O	LPSDR Output		2.812
LS_RDATA_B	M3	O	LPSDR Output		2.925
LS_RDATA_C	J4	O	LPSDR Output		3.54
LS_RDATA_D	K3	O	LPSDR Output		3.094
DMD_DEN_A RSTZ	H4	I	ARSTZ		5.06
TP0	D18	I			4.175
TP1	C17	I			4.334
TP2	C18	I			0.34971
TEMP_N	E17	I	Temp Diode N		2.676
TEMP_P	F17	I	Temp Diode P		2.146
VDD	A10, A12, A13, A20, B2, B10, B11, B14, C4, D1, D4, E3, E18, F3, F4, G17, J3, J18, M18, N3, N18, R3, R8, R10, R12, R13, R18, T9	P	Digital Core Supply Voltage		
VDDI	D3, F18, G4, H18, K4, K18, L18, M4	P			
VRESET	T2, T19	P			
VBIAS	R1, R20	P			
VOFFSET	D17, E4, T1, T20	P			

**Table 4-1. Pin Functions (continued)**

PIN		INPUT- OUTPUT <sup>(1)</sup>	DESCRIPTION	TERMINATION	TRACE LENGTH (mm)
NAME	ID				
VSS	A3, A11, A14, A19, B3, B6, B9, B12, B13, B17, B20, C1, C2, C3, C19, F2, F19, G3, G18, H3, J2, J19, L4, M2, M19, N2, N19, P3, P18, R4, R7, R9, R11, R14, R17, T10	G	Ground		
N/C	H17, R16, R15, P17, N17, M17, L17, K17, J17,	NC	No Connect Pin		None

(1) I=Input, O=Output, P=Power, G=Ground, NC = No Connect

## 5 Specifications

### 5.1 Absolute Maximum Ratings

Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, which may affect device reliability, functionality, and performance, and shorten the device's lifetime.

		MIN	MAX	UNIT
<b>SUPPLY VOLTAGE</b>				
$V_{DD}$	Supply voltage for LVCMOS core logic and LPSDR low-speed interface (LSIF) <sup>(1)</sup>	-0.5	2.3	V
$V_{DDI}$	Supply voltage for SubLVDS receivers <sup>(1)</sup>	-0.5	2.3	V
$V_{OFFSET}$	Supply voltage for HVCMOS and micromirror electrode <sup>(1) (2)</sup>	-0.5	11	V
$V_{BIAS}$	Supply voltage for micromirror electrode <sup>(1)</sup>	-0.5	19	V
$V_{RESET}$	Supply voltage for micromirror electrode <sup>(1)</sup>	-15	0.5	V
$ V_{DDI} - V_{DD} $	Supply voltage delta (absolute value) <sup>(3)</sup>		0.3	V
$ V_{BIAS} - V_{OFFSET} $	Supply voltage delta (absolute value) <sup>(4)</sup>		11	V
$ V_{BIAS} - V_{RESET} $	Supply voltage delta (absolute value) <sup>(5)</sup>		34	V
<b>INPUT VOLTAGE</b>				
	Input voltage for other inputs – LSIF and LVCMOS <sup>(1)</sup>	-0.5	$V_{DD}+0.5$	V
	Input voltage for other inputs – SubLVDS <sup>(1) (6)</sup>	-0.5	$V_{DDI}+0.5$	V
<b>SUBLVDS INTERFACE (HSIF)</b>				
$ V_{ID} $	SubLVDS differential input voltage (absolute value) <sup>(6)</sup>		810	mV
$ I_{ID} $	SubLVDS input differential current <sup>(6)</sup>		10	mA
<b>CLOCK FREQUENCY</b>				
$f_{CLOCK}$	LSIF clock frequency (LS_CLK)	100	130	MHz
<b>TEMPERATURE DIODE</b>				
$I_{TEMP\_DIODE}$	Max current source into temperature diode		120	$\mu$ A
<b>ENVIRONMENTAL</b>				
$T_{ARRAY}$	Temperature, operating <sup>(7)</sup>	0	90	$^{\circ}$ C
	Temperature, non-operating <sup>(7)</sup>	-40	90	$^{\circ}$ C
$T_{DP}$	Dew point temperature, operating and non-operating (noncondensing)		81	$^{\circ}$ C

- (1) All voltage values are concerning the ground terminals ( $V_{SS}$ ). The following required power supplies must be connected for proper DMD operation:  $V_{DD}$ ,  $V_{DDI}$ ,  $V_{OFFSET}$ ,  $V_{BIAS}$ , and  $V_{RESET}$ . All  $V_{SS}$  connections are also required.
- (2)  $V_{OFFSET}$  supply transients must fall within specified voltages.
- (3) Exceeding the recommended allowable absolute voltage difference between  $V_{DDI}$  and  $V_{DD}$  may result in excessive current draw.
- (4) Exceeding the recommended allowable absolute voltage difference between  $V_{BIAS}$  and  $V_{OFFSET}$  may result in excessive current draw.
- (5) Exceeding the recommended allowable absolute voltage difference between  $V_{BIAS}$  and  $V_{RESET}$  may result in excessive current draw.
- (6) This maximum input voltage rating applies when each input of a differential pair is at the same voltage potential. SubLVDS differential inputs must not exceed the specified limit or damage may result to the internal termination resistors.
- (7) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1), as shown in [Figure 6-1](#) and [Section 6.6](#).

### 5.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system.

		MIN	MAX	UNIT
$T_{DMD}$	DMD temperature	-40	80	$^{\circ}$ C
$T_{DP-AVG}$	Average dew point temperature, non-condensing <sup>(1)</sup>		28	$^{\circ}$ C
$T_{DP-ELR}$	Elevated dew point temperature range, non-condensing <sup>(2)</sup>	28	36	$^{\circ}$ C

## 5.2 Storage Conditions (continued)

Applicable for the DMD as a component or non-operating in a system.

		MIN	MAX	UNIT
CT <sub>ELR</sub>	Cumulative time in elevated dew point temperature range		24	months

- (1) The average temperature over time (including storage and operating temperatures) that the device is not in the elevated dew point temperature range.
- (2) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT<sub>ELR</sub>.

## 5.3 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±250	V

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

## 5.4 Recommended Operating Conditions

Over operating free-air temperature range and supply voltages (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by the Recommended Operating Conditions. No level of performance is implied when operating the device above or below the Recommended Operating Conditions limits.

		MIN	TYP	MAX	UNIT
<b>SUPPLY VOLTAGE RANGE</b>					
V <sub>DD</sub>	Supply voltage for LVCMOS core logic <sup>(1) (2)</sup> Supply voltage for LPSDR low-speed interface	1.71	1.8	1.95	V
V <sub>DDI</sub>	Supply voltage for SubLVDS receivers <sup>(1) (2)</sup>	1.71	1.8	1.95	V
V <sub>OFFSET</sub>	Supply voltage for HVCMOS and micromirror electrode <sup>(1) (2) (3)</sup>	9.5	10	10.5	V
V <sub>BIAS</sub>	Supply voltage for mirror electrode <sup>(1) (2)</sup>	17.5	18	18.5	V
V <sub>RESET</sub>	Supply voltage for micromirror electrode <sup>(1) (2)</sup>	-14.5	-14	-13.5	V
V <sub>DDI</sub> - V <sub>DD</sub>	Supply voltage delta (absolute value) <sup>(1) (2) (4)</sup>			0.3	V
V <sub>BIAS</sub> - V <sub>OFFSET</sub>	Supply voltage delta (absolute value) <sup>(1) (2) (5)</sup>			10.5	V
V <sub>BIAS</sub> - V <sub>RESET</sub>	Supply voltage delta (absolute value) <sup>(1) (2) (6)</sup>			33	V
<b>CLOCK FREQUENCY</b>					
f <sub>clock</sub>	Clock frequency for low speed interface LS_CLK <sup>(7)</sup>	108		120	MHz
	Clock frequency for high-speed interface DCLK <sup>(8)</sup>			720	MHz
DCD <sub>IN</sub>	Duty cycle distortion	48%		52%	
DCD <sub>OUT</sub>	Duty cycle distortion	44%	50%	56%	
<b>SUBLVDS INTERFACE</b>					
V <sub>ID</sub>	LVDS differential input voltage magnitude <sup>(8)</sup>	150	250	350	mV
V <sub>CM</sub>	Common mode voltage <sup>(8)</sup>	700	900	1100	mV
V <sub>SUBLVDS</sub>	SubLVDS voltage <sup>(8)</sup>	525		1275	mV
Z <sub>LINE</sub>	Line differential impedance (PWB/trace)	90	100	110	Ω
Z <sub>IN</sub>	Internal differential termination resistance <sup>(10)</sup>	80	100	120	Ω
	100Ω differential PCB trace	6.35		152.4	mm
<b>ENVIRONMENTAL</b>					
T <sub>ARRAY</sub>	Array temperature, long-term operation <sup>(9) (10) (11) (12)</sup>	10		40 to 70	°C
	Array temperature, short-term operation, 500 hr max <sup>(10) (13)</sup>	0		10	°C
T <sub>DP-AVG</sub>	Average dew point temperature, (non-condensing) <sup>(14)</sup>			28	°C

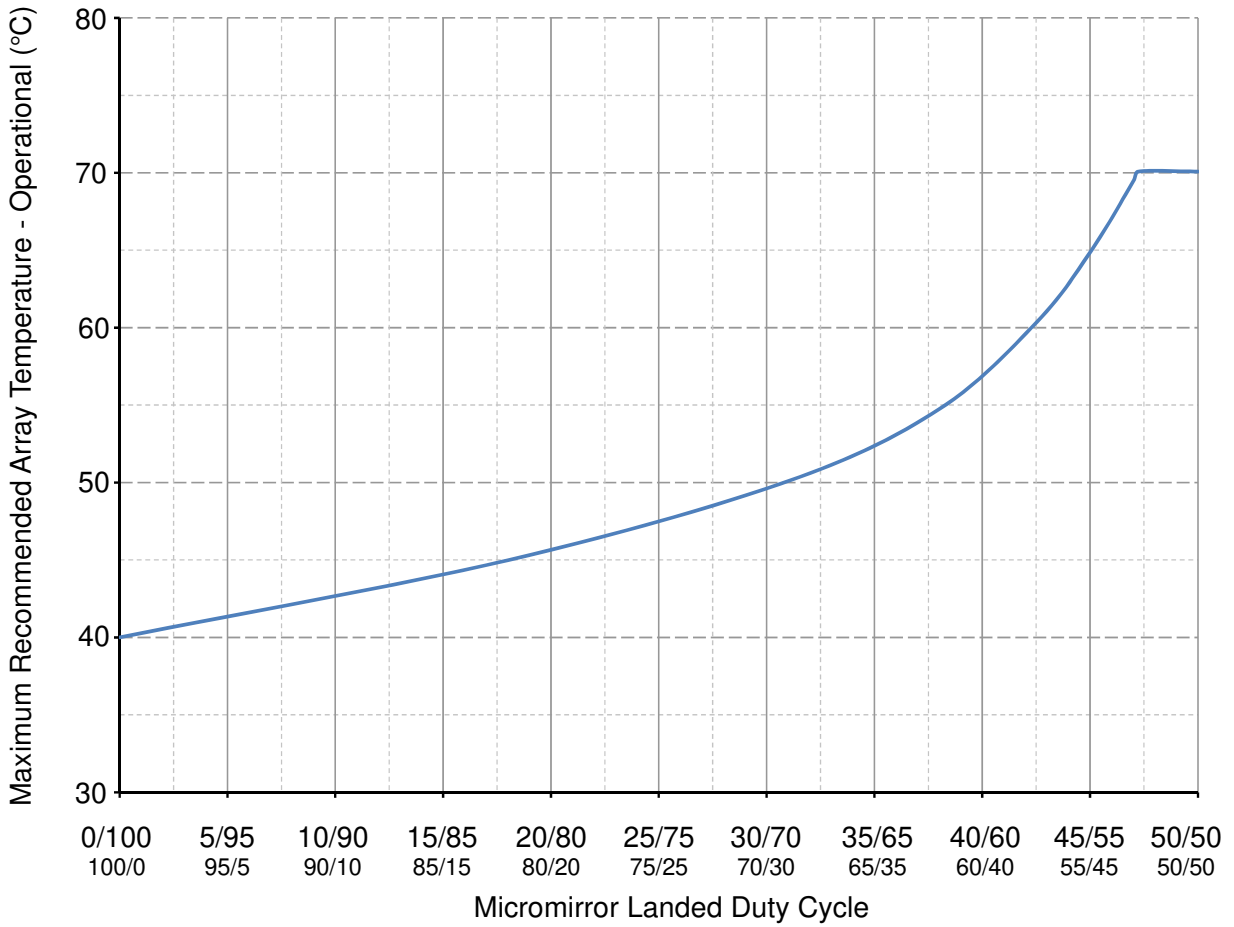


## 5.4 Recommended Operating Conditions (continued)

Over operating free-air temperature range and supply voltages (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by the Recommended Operating Conditions. No level of performance is implied when operating the device above or below the Recommended Operating Conditions limits.

		MIN	TYP	MAX	UNIT
T <sub>DP-ELR</sub>	Elevated dew point temperature range, (non-condensing) <sup>(15)</sup>		28	36	°C
CT <sub>ELR</sub>	Cumulative time in elevated dew point temperature range			28	Months
Q <sub>AP-LL</sub>	Window Aperture illumination overfill <sup>(16)</sup> <sup>(17)</sup> <sup>(18)</sup>			17	W/cm <sup>2</sup>
<b>ILLUMINATION LPCW, RGB Laser and LED</b>					
ILL <sub>UV</sub>	Illumination, wavelength < 410nm <sup>(9)</sup> <sup>(20)</sup>			10	mW/cm <sup>2</sup>
ILL <sub>VIS</sub>	Illumination power at wavelengths ≥ 410nm and ≤ 800nm <sup>(19)</sup> <sup>(20)</sup>			60	W/cm <sup>2</sup>
ILL <sub>IR</sub>	Illumination, wavelength between > 800nm <sup>(20)</sup>			10	mW/cm <sup>2</sup>
ILL <sub>BLU</sub>	Illumination power at wavelengths ≥ 410nm and ≤ 475nm <sup>(19)</sup> <sup>(20)</sup>			19.5	W/cm <sup>2</sup>
ILL <sub>BLU1</sub>	Illumination power at wavelengths ≥ 410nm and ≤ 440nm <sup>(19)</sup> <sup>(20)</sup>			3.06	W/cm <sup>2</sup>

- (1) The following power supplies are required to operate the DMD: V<sub>DD</sub>, V<sub>DDI</sub>, V<sub>OFFSET</sub>, V<sub>BIAS</sub>, and V<sub>RESET</sub>. All V<sub>SS</sub> connections are required to operate the DMD.
- (2) All voltage values are with respect to the V<sub>SS</sub> ground pins.
- (3) V<sub>OFFSET</sub> supply transients must fall within the specified max voltages.
- (4) To prevent excess current, the supply voltage delta |V<sub>DDI</sub> – V<sub>DD</sub>| must be less than the specified limit.
- (5) To prevent excess current, the supply voltage delta |V<sub>BIAS</sub> – V<sub>OFFSET</sub>| must be less than the specified limit.
- (6) To prevent excess current, the supply voltage delta |V<sub>BIAS</sub> – V<sub>RESET</sub>| must be less than the specified limit.
- (7) LS\_CLK must run as specified to ensure internal DMD timing for reset waveform commands.
- (8) Refer to the SubLVDS timing requirements in *Timing Requirements*.
- (9) Simultaneous exposure of the DMD to the maximum Recommended Operating Conditions for temperature and UV illumination will reduce device lifetime.
- (10) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point (TP1) and the package thermal resistance using the Micromirror Array Temperature Calculation.
- (11) The maximum operational array temperature is derated based on the micromirror landed duty cycle that the DMD experiences in the end application. See the [Section 6.9.1](#) section for a definition of micromirror landed duty cycle.
- (12) Long-term is defined as the usable life of the device.
- (13) Short-term is the total cumulative time over the useful life of the device.
- (14) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
- (15) Exposure to dew point temperatures in the elevated range during storage and operation is limited to less than a total cumulative time of CT<sub>ELR</sub>.
- (16) Applies to the region defined in the [Figure 5-2](#).
- (17) The active area of the DMD is surrounded by an aperture on the inside of the DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical conditions. Overfill light illuminating the area outside the active array can scatter and create adverse effects to the performance of an end application using the DMD. Minimizing the light flux incident outside the active array is a design requirement of the illumination optical system. Depending on the particular optical architecture and assembly tolerances of the optical system, the amount of overfill light on the outside of the active array may cause system performance degradation.
- (18) To calculate, see the [Section 6.8](#).
- (19) The maximum allowable optical power incident on the DMD is limited by the maximum optical power density for each wavelength range specified and the micromirror array temperature (T<sub>ARRAY</sub>).
- (20) To calculate, see the [Section 6.7](#).



**Figure 5-1. Maximum Recommended Array Temperature—Derating Curve**

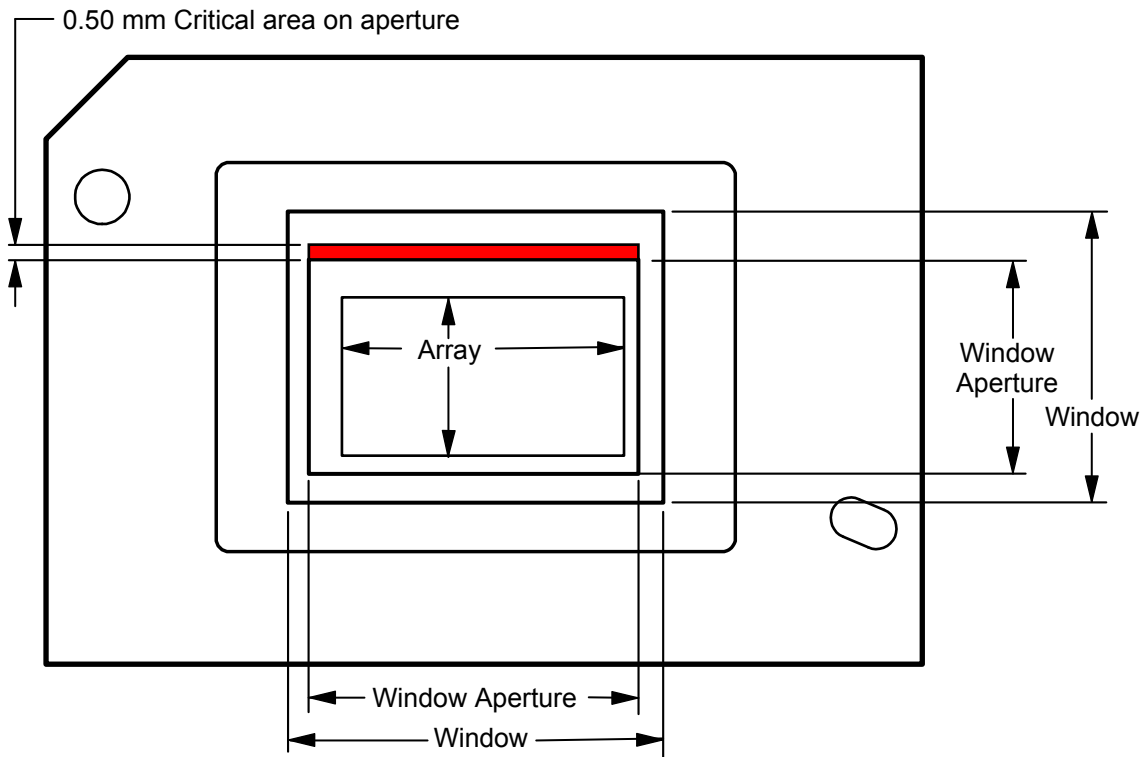


Figure 5-2. Illumination Overfill Diagram—Critical Area

## 5.5 Thermal Information

THERMAL METRIC	DLP473NE	UNIT
	FXL PACKAGE	
	173 PINS	
Thermal Resistance, active area to test point 1 (TP1) <sup>(1)</sup>	1.0	°C/W

- (1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the DMD within the temperature range specified in the [Recommended Operating Conditions](#). The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems must be designed to minimize the light energy falling outside the window's clear aperture, since any additional thermal load in this area can significantly degrade the reliability of the device.

## 5.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

PARAMETER <sup>(7)</sup>		TEST CONDITIONS <sup>(2)</sup>	MIN	TYP	MAX	UNIT
<b>CURRENT</b>						
$I_{DD}$	Supply current: $V_{DD}$ <sup>(3) (4)</sup>	Typical		70		mA
$I_{DDI}$	Supply current: $V_{DDI}$ <sup>(3) (4)</sup>	Typical		28		mA
$I_{OFFSET}$	Supply current: $V_{OFFSET}$ <sup>(5) (6)</sup>	Typical		7		mA
$I_{BIAS}$	Supply current: $V_{BIAS}$ <sup>(5) (6)</sup>	Typical		1.5		mA
$I_{RESET}$	Supply current: $V_{RESET}$ <sup>(6)</sup>	Typical		3		mA
<b>POWER</b>						
$P_{DD}$	Supply power dissipation: $V_{DD}$ <sup>(3) (4)</sup>	Typical		126		mW
$P_{DDI}$	Supply power dissipation: $V_{DDI}$ <sup>(3) (4)</sup>	Typical		51		mW

## 5.6 Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

PARAMETER <sup>(7)</sup>		TEST CONDITIONS <sup>(2)</sup>	MIN	TYP	MAX	UNIT
P <sub>OFFSET</sub>	Supply power dissipation: V <sub>OFFSET</sub> <sup>(5) (6)</sup>	Typical		70		mW
P <sub>BIAS</sub>	Supply power dissipation: V <sub>BIAS</sub> <sup>(5) (6)</sup>	Typical		27		mW
P <sub>RESET</sub>	Supply power dissipation: V <sub>RESET</sub> <sup>(6)</sup>	Typical		42		mW
P <sub>TOTAL</sub>	Supply power dissipation Total	Typical		316		mW
<b>LPSDR INPUT</b>						
V <sub>IH</sub>	High-level input voltage <sup>(8) (9)</sup>		0.7 × V <sub>DD</sub>	V <sub>DD</sub> + 0.3	x V <sub>DD</sub>	
V <sub>IL</sub>	Low-level input voltage <sup>(8) (9)</sup>		-0.3	0.3 × V <sub>DD</sub>	x V <sub>DD</sub>	
V <sub>IH(AC)</sub>	AC input high voltage <sup>(8) (9)</sup>		0.8 × V <sub>DD</sub>	V <sub>DD</sub> + 0.3	x V <sub>DD</sub>	
V <sub>IL(AC)</sub>	AC input low voltage <sup>(8) (9)</sup>		-0.3	0.2 × V <sub>DD</sub>	x V <sub>DD</sub>	
V <sub>Hyst</sub>	Input Hysteresis ( V <sub>T+</sub> – V <sub>T-</sub> )		0.1 × V <sub>DD</sub>	0.4 × V <sub>DD</sub>		V
I <sub>IL</sub>	Low level input current	V <sub>DD</sub> = 1.95V, V <sub>I</sub> = 0V	-100			nA
I <sub>IH</sub>	High level input current	V <sub>DD</sub> = 1.95V, V <sub>I</sub> = 1.95V			135	uA
<b>LPSDR OUTPUT</b>						
V <sub>OH</sub>	DC output high voltage <sup>(10)</sup>	I <sub>OH</sub> = -2mA	0.8 × V <sub>DD</sub>			X V <sub>DD</sub>
V <sub>OL</sub>	DC output low voltage <sup>(10)</sup>	I <sub>OL</sub> = 2mA		0.2 × V <sub>DD</sub>		X V <sub>DD</sub>
<b>CAPACITANCE</b>						
C <sub>IN</sub>	Input capacitance LVCMOS	F = 1MHz			10	pF
C <sub>IN</sub>	Input capacitance SubLVDS	F = 1MHz			20	pF
C <sub>OUT</sub>	Output capacitance	F = 1MHz			10	pF

(1) Device electrical characteristics are over [Section 5.4](#) unless otherwise noted.

(2) All voltage values are with respect to the ground pins (V<sub>SS</sub>).

(3) To prevent excess current, the supply voltage delta |V<sub>DDI</sub> – V<sub>DD</sub>| must be less than the specified limit.

(4) Supply power dissipation based on non-compressed commands and data.

(5) To prevent excess current, the supply voltage delta |V<sub>BIAS</sub> – V<sub>OFFSET</sub>| must be less than the specified limit.

(6) Supply power dissipation based on three global resets in 200μs.

(7) All power supply connections are required to operate the DMD: V<sub>DD</sub>, V<sub>DDI</sub>, V<sub>OFFSET</sub>, V<sub>BIAS</sub>, V<sub>RESET</sub>. All V<sub>SS</sub> connections are also required.

(8) LPSDR specifications are for pins LS\_CLK and LS\_WDATA.

(9) Low-speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, Low-Power Double Data Rate (LPDDR) [JESD209B](#).

(10) LPSDR output specification is for pins LS\_RDATA\_A, LS\_RDATA\_B, LS\_RDATA\_C, LS\_RDATA\_D.

## 5.7 Switching Characteristics

Over operating free-air temperature range and supply voltages (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PD</sub>	Output propagation, clock to Q, rising edge of LS_CLK input to LS_RDATA output	C <sub>L</sub> = 45pF			15	ns
	Slew rate, LS_RDATA		0.3			V/ns
	Output duty cycle distortion, LS_RDATA_A and LS_RDATA_B		40%		60%	

## 5.8 Timing Requirements

Over operating free-air temperature range and supply voltages (unless otherwise noted)

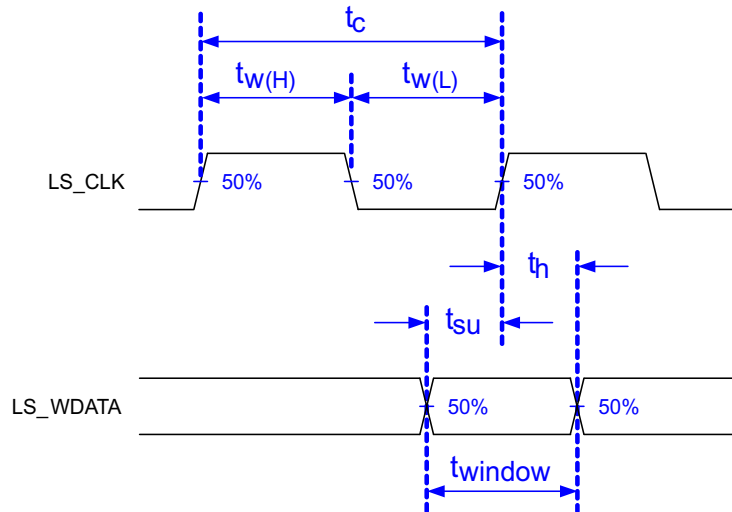
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>LPSDR</b>						
t <sub>f</sub>	Fall slew rate <sup>(2)</sup>	(80% to 20%) × V <sub>DD</sub> <sup>(5)</sup>	0.25			V/ns

## 5.8 Timing Requirements (continued)

Over operating free-air temperature range and supply voltages (unless otherwise noted)

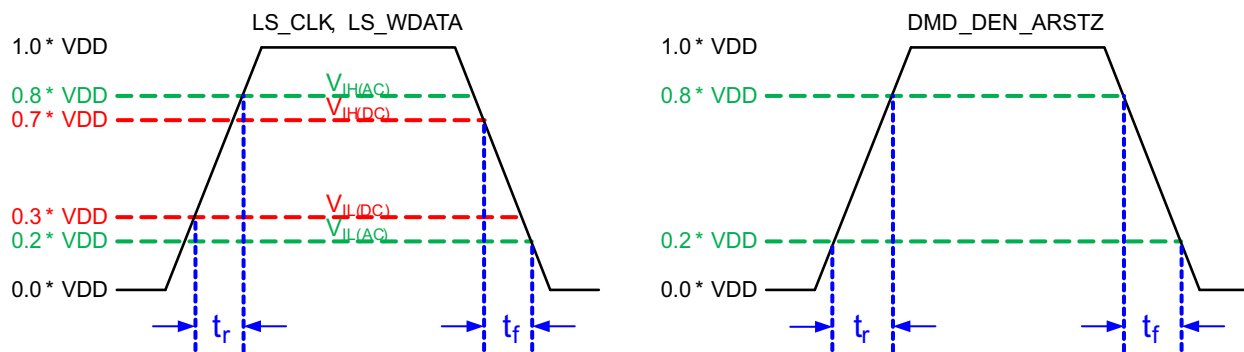
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_c$	Cycle time LS_CLK <sup>(5)</sup>	50% to 50% reference points <sup>(5)</sup>	7.7	8.3		ns
$t_r$	Rise slew rate <sup>(1)</sup>	$(30\% \text{ to } 80\%) \times V_{DD}$ <sup>(6)</sup>	1		3	V/ns
$t_f$	Fall slew rate <sup>(1)</sup>	$(70\% \text{ to } 20\%) \times V_{DD}$ <sup>(6)</sup>	1		3	V/ns
$t_r$	Rise slew rate <sup>(2)</sup>	$(20\% \text{ to } 80\%) \times V_{DD}$ <sup>(6)</sup>	0.25			V/ns
$t_{W(H)}$	Pulse duration LS_CLK high	50% to 50% reference points <sup>(5)</sup>	3.1			ns
$t_{W(L)}$	Pulse duration LS_CLK low	50% to 50% reference points <sup>(5)</sup>	3.1			ns
$t_{WINDOW}$	Window time <sup>(1) (3)</sup>	Setup time + Hold time <sup>(5)</sup>	3			ns
$t_{DERATING}$	Window time derating <sup>(1) (3)</sup>	For each 0.25V/ns reduction in slew rate below 1 V/ns <sup>(8)</sup>		0.35		ns
$t_{su}$	Setup time	LS_WDATA valid before LS_CLK <sup>(5)</sup>			1.5	ns
$t_h$	Hold time	LS_WDATA valid after LS_CLK <sup>(5)</sup>			1.5	ns
<b>SubLVDS</b>						
$t_r$	Rise slew rate	20% to 80% reference points <sup>(7)</sup>	0.7	1		V/ns
$t_f$	Fall slew rate	80% to 20% reference points <sup>(7)</sup>	0.7	1		V/ns
$t_c$	Cycle time D_CLK <sup>(9)</sup>	50% to 50% reference points <sup>(9)</sup>	1.35	1.39		ns
$t_{W(H)}$	Pulse duration DCLK high	50% to 50% reference points <sup>(9)</sup>	0.7			ns
$t_{W(L)}$	Pulse duration DCLK low	50% to 50% reference points <sup>(9)</sup>	0.7			ns
$t_{su}$	Setup time	DATA valid before D_CLK <sup>(9)</sup>			0.17	ns
$t_h$	Hold time	DATA valid after D_CLK <sup>(9)</sup>			0.17	ns
$t_{WINDOW}$	Window time	Setup time + Hold time <sup>(9) (10)</sup>			0.25	ns
$t_{POWER}$	Power-up receiver <sup>(4)</sup>				200	ns

- (1) The specification is for the LS\_CLK and LS\_WDATA pins. Refer to the LPSDR input rise and fall slew rate in [Figure 5-4](#).
- (2) The specification is for the DMD\_DEN\_ARSTZ pin. Refer to the LPSDR input rise and fall slew rate in [Figure 5-4](#).
- (3) Window time derating example: 0.5V/ns slew rate increases the window time by 0.7ns, from 3 to 3.7ns.
- (4) The specification is for SubLVDS receiver time only and does not take into account commanding and latency after commanding.
- (5) See [Figure 5-3](#).
- (6) See [Figure 5-4](#).
- (7) See [Figure 5-5](#).
- (8) See [Figure 5-6](#).
- (9) See [Figure 5-7](#).
- (10) See [Figure 5-8](#).



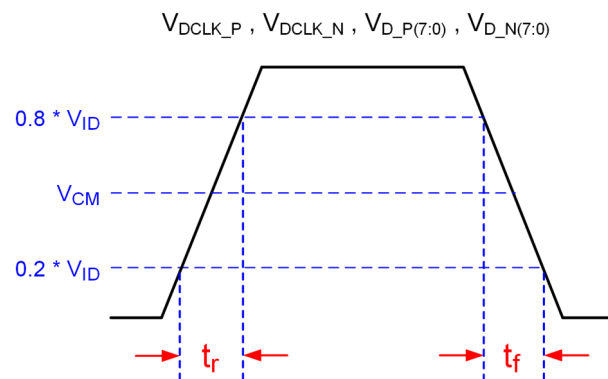
The low-speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low Power Double Data Rate (LPDDR)* [JESD209B](#).

**Figure 5-3. LPSDR Switching Parameters**

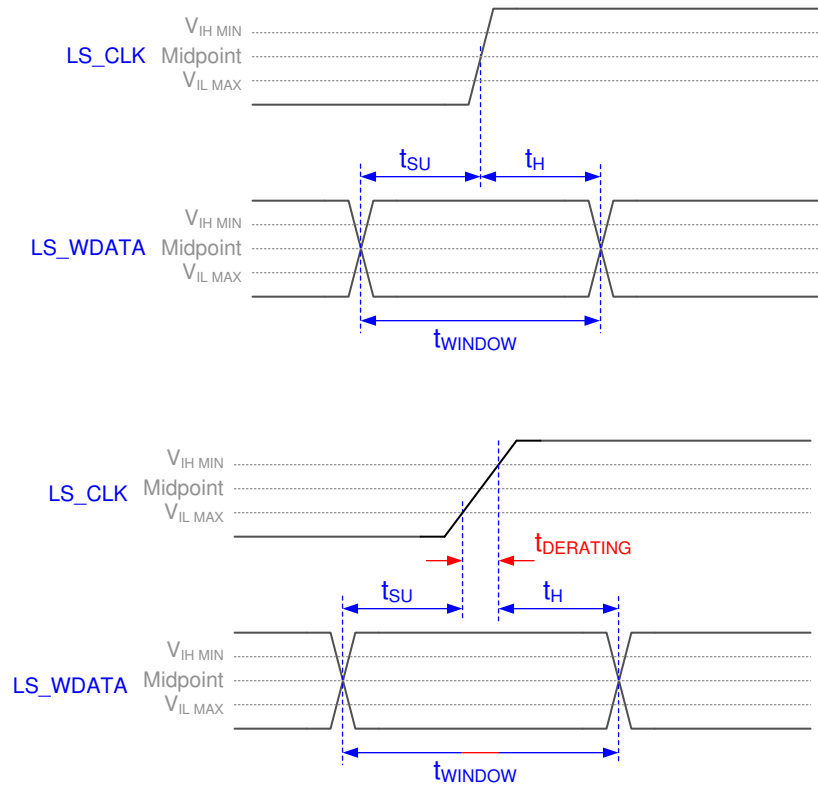


**Figure 5-4. LPSDR Input Rise and Fall Slew Rate**

Not to Scale

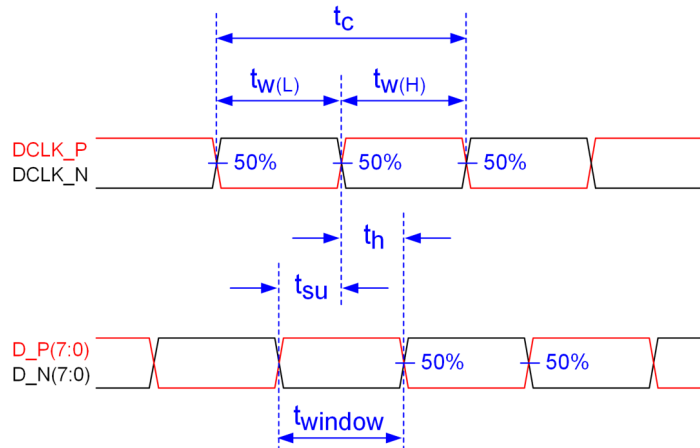


**Figure 5-5. SubLVDS Input Rise and Fall Slew Rate**

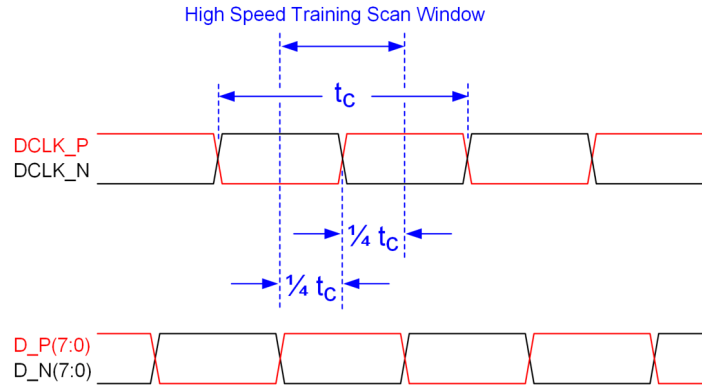


**Figure 5-6. Window Time Derating Concept**

Not to Scale

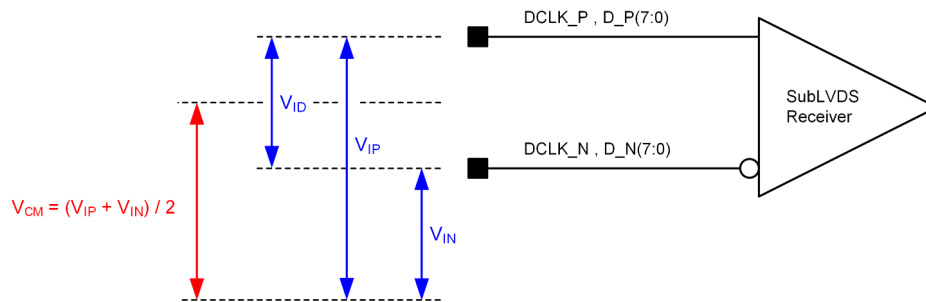


**Figure 5-7. SubLVDS Switching Parameters**

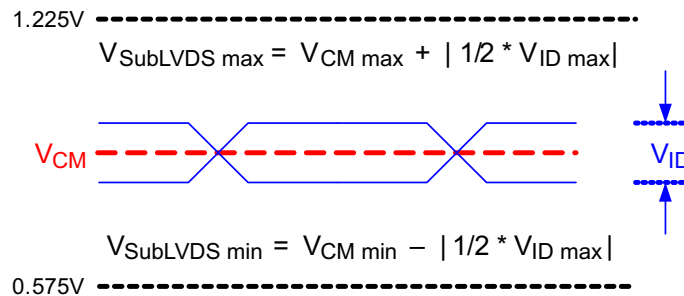


Note: Refer to the timing requirements for details.

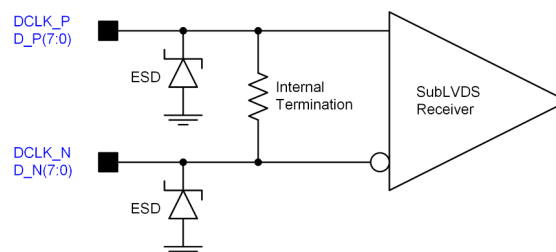
**Figure 5-8. High-Speed Training Scan Window**



**Figure 5-9. SubLVDS Voltage Parameters**

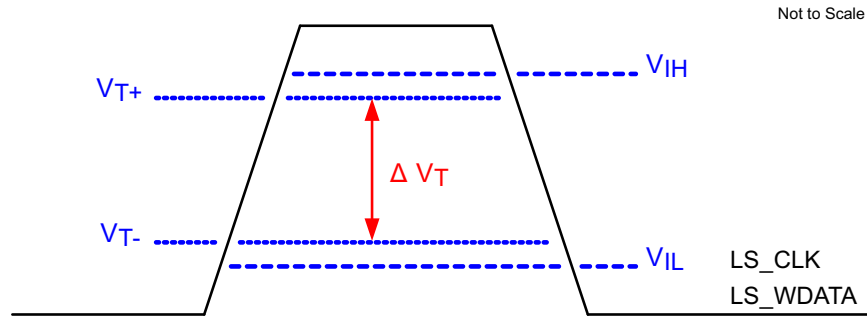


**Figure 5-10. SubLVDS Waveform Parameters**

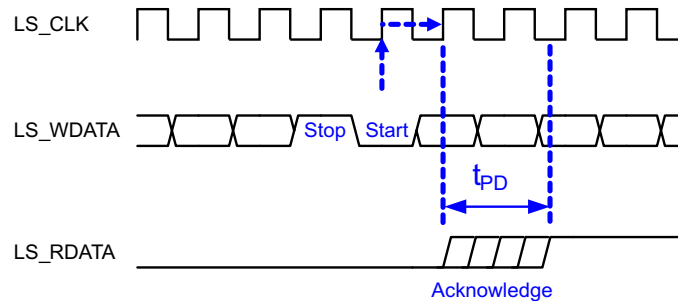


**Figure 5-11. SubLVDS Equivalent Input Circuit**



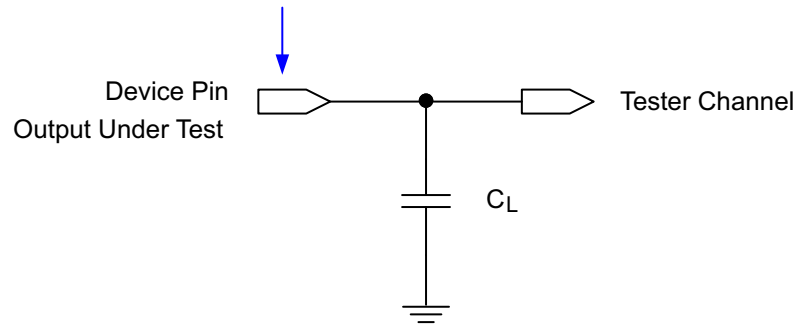


**Figure 5-12. LPSDR Input Hysteresis**



**Figure 5-13. LPSDR Read Out**

Data Sheet Timing Reference Point



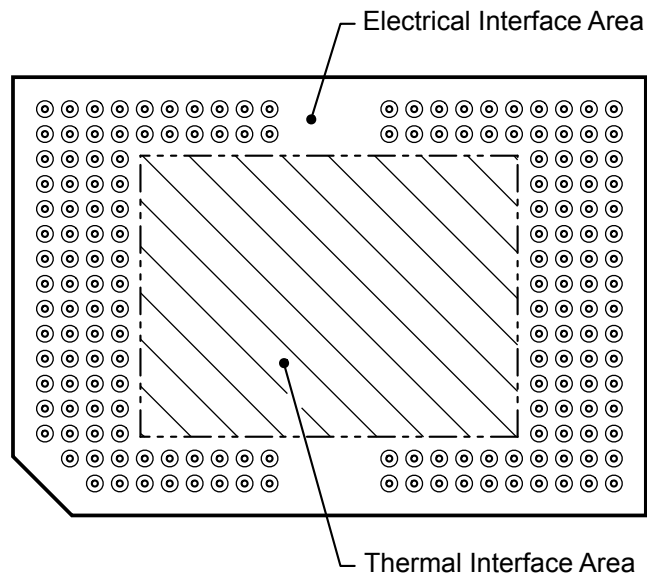
See the timing section for more information.

**Figure 5-14. Test Load Circuit for Output Propagation Measurement**

### 5.9 System Mounting Interface Loads

PARAMETER	MIN	TYP	MAX	UNIT
<b>When loads are applied to the electrical and thermal interface areas</b>				
Maximum load to be applied to the electrical interface area <sup>(1)</sup>			111	N
Maximum load to be applied to the thermal interface area <sup>(1)</sup>			111	N
<b>When a load is applied to only the electrical interface area</b>				
Maximum load to be applied to the electrical interface area <sup>(1)</sup>			222	N
Maximum load to be applied to the thermal interface area <sup>(1)</sup>			0	N

(1) The load should be uniformly applied in the corresponding areas shown in [Figure 5-15](#).



**Figure 5-15. System Mounting Interface Loads**

### 5.10 Micromirror Array Physical Characteristics

PARAMETER DESCRIPTION		VALUE	UNIT
Number of active columns <sup>(1) (2)</sup>	M	1920	micromirrors
Number of active rows <sup>(1) (2)</sup>	N	1080	micromirrors
Micromirror (pixel) pitch <sup>(1)</sup>	P	5.4	μm
Micromirror active array width <sup>(1)</sup>	Micromirror pitch × number of active columns	10.368	mm
Micromirror active array height <sup>(1)</sup>	Micromirror pitch × number of active rows	5.832	mm
Micromirror active border <sup>(3)</sup>	Pond of micromirror (POM)	20	micromirrors/side

- (1) See Figure 5-16.
- (2) The fast switching speed of the DMD micromirrors combined with advanced DLP image processing algorithms enables each micromirror to display four distinct pixels on the screen during every frame, resulting in a full 3840 × 2160 pixel image being displayed.
- (3) The structure and qualities of the border around the active array include a band of partially functional micromirrors referred to as the pond of micromirrors (POM). These micromirrors are structurally and electrically prevented from tilting toward the bright or ON state but still require an electrical bias to tilt toward the OFF state.

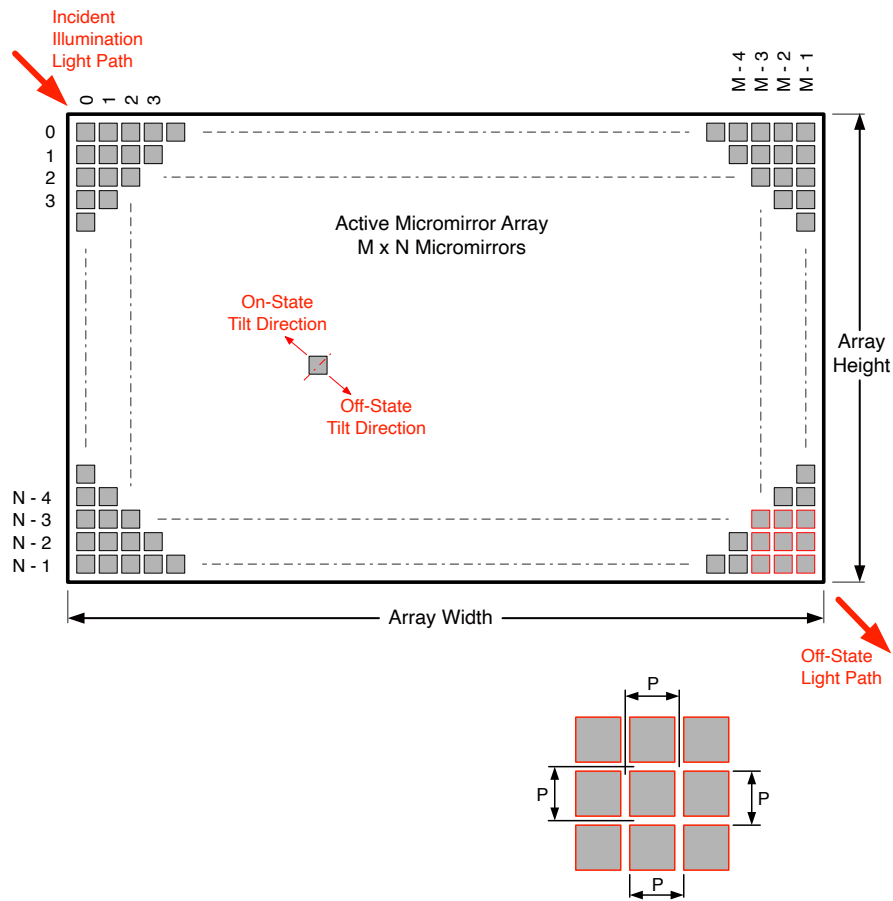


Figure 5-16. Micromirror Array Physical Characteristics

## 5.11 Micromirror Array Optical Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Micromirror tilt angle <sup>(1) (2) (3) (4)</sup>			13.5	14.5	15.5	degrees
Micromirror crossover time <sup>(5)</sup>		Typical Performance		3		µs
Micromirror switching time <sup>(6)</sup>		Typical Performance	6			
Image Performance <sup>(7)</sup>	Bright pixel(s) in active area <sup>(8)</sup>	Gray 10 Screen <sup>(9)</sup>			0	micromirrors
	Bright pixel(s) in the POM <sup>(10)</sup>	Gray 10 Screen <sup>(9)</sup>			1	
	Dark pixel(s) in the active area <sup>(11)</sup>	White Screen			4	
	Adjacent pixel(s) <sup>(12)</sup>	Any Screen			0	
	Unstable pixel(s) in active area <sup>(13)</sup>	Any Screen			0	

- (1) Measured relative to the plane formed by the overall micromirror array.
- (2) Represents the variation that can occur between any two individual micromirrors, located on the same device or on different devices.
- (3) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations, or system contrast variations.
- (4) When the micromirror array is landed (not parked), the tilt direction of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of 1 results in a micromirror landing in the ON State direction. A binary value of 0 results in a micromirror landing in the OFF State direction.
- (5) The time required for a micromirror to nominally transition from one landed state to the opposite landed state.
- (6) The minimum time between successive transitions of a micromirror.
- (7) Conditions of Acceptance: All DMD image quality returns will be evaluated using the following projected image test conditions:  
 Test set degamma shall be linear  
 Test set brightness and contrast shall be set to nominal  
 The diagonal size of the projected image shall be a minimum of 20 inches  
 The projections screen shall be 1X gain  
 The projected image shall be inspected from a 38 inch minimum viewing distance  
 The image shall be in focus during all image quality tests
- (8) Bright pixel definition: A single pixel or mirror that is stuck in the ON position and is visibly brighter than the surrounding pixels
- (9) Gray 10 screen definition: All areas of the screen are colored with the following settings:  
 Red = 10/255  
 Green = 10/255  
 Blue = 10/255
- (10) POM definition: Rectangular border of off-state mirrors surrounding the active area
- (11) Dark pixel definition: A single pixel or mirror that is stuck in the OFF position and is visibly darker than the surrounding pixels
- (12) Adjacent pixel definition: Two or more stuck pixels sharing a common border or common point, also referred to as a cluster
- (13) Unstable pixel definition: A single pixel or mirror that does not operate in sequence with parameters loaded into memory. The unstable pixel appears to be flickering asynchronously with the image.

## 5.12 Window Characteristics

DESCRIPTION <sup>(1)</sup>		MIN	TYP	MAX
Window material			Corning Eagle XG	
Window refractive index	At wavelength 546.1nm		1.5119	

(1) See [Section 6.5](#) for more information.

## 5.13 Chipset Component Usage Specification

Reliable function and operation of the DLP473NE DMD requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology consists of the TI technology and devices used for operating or controlling a DLP DMD.

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### Note

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding the limits described previously.

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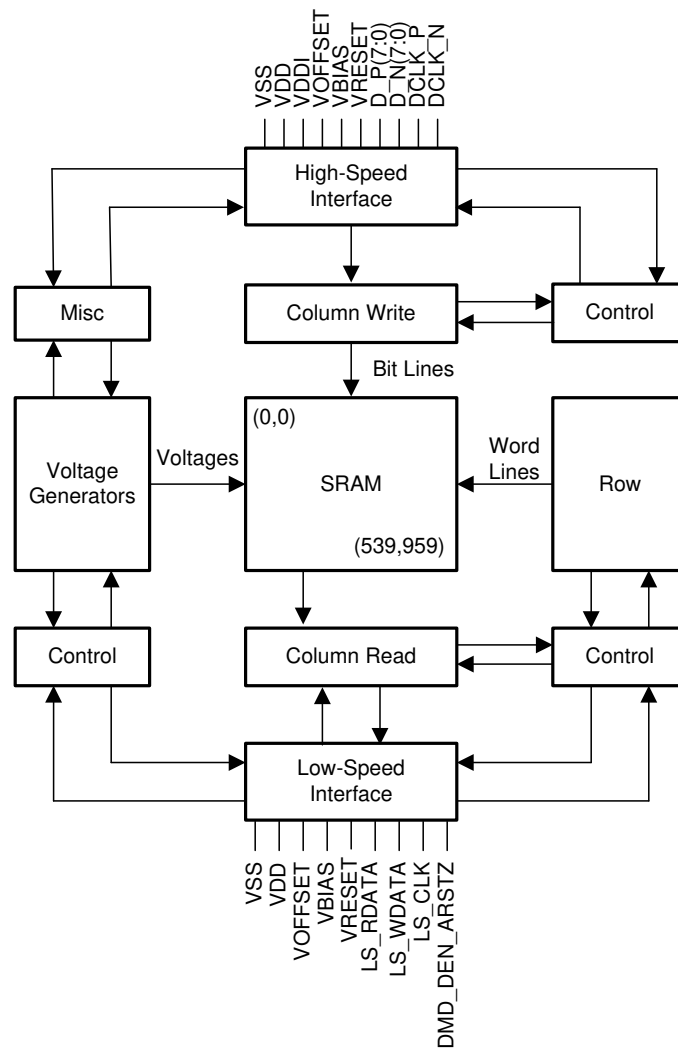
## 6 Detailed Description

### 6.1 Overview

The DLP473NE digital micromirror device (DMD) is a 0.47-inch diagonal spatial light modulator, which consists of an array of highly reflective aluminum micromirrors. The DMD is an electrical input, optical output micro-optical-electrical-mechanical system (MOEMS). The fast switching speed of the DMD micromirrors combined with advanced DLP image processing algorithms enables each micromirror to display four distinct pixels on the screen during every frame, resulting in a full 1920 × 1080 pixel image being displayed. The electrical interface is low-voltage differential signaling (LVDS). The DMD consists of a two-dimensional array of 1-bit CMOS memory cells. The array is organized in a grid of M memory cell columns by N memory cell rows. Refer to the [Functional Block Diagram](#). The positive or negative deflection angle of the micromirrors can be individually controlled by changing the address voltage of the underlying CMOS addressing circuitry and micromirror reset signals (MBRST).

The DLP 0.47" 1080p chipset is comprised of the DLP473NE DMD, the DLPC8454 display controller, and the DLPA3082 PMIC. For reliable operation, always use the DLP473NE DMD with the DLP display controller and the PMIC specified in the chipset.

### 6.2 Functional Block Diagram



## 6.3 Feature Description

### 6.3.1 Power Interface

The DMD requires four DC voltages: 1.8V source,  $V_{\text{OFFSET}}$ ,  $V_{\text{RESET}}$ , and  $V_{\text{BIAS}}$ . In a typical configuration, all required voltages are generated by DLPA3082 PMIC.

### 6.3.2 Timing

The data sheet specifies the timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be considered. Timing reference loads are not intended to be precise representations of any particular system environment or depiction of the actual load presented by a production test. TI recommends that system designers use IBIS or other simulation tools to correlate the timing reference load to a system environment. Use the specified load capacitance value for characterization and measurement of AC timing signals only. This load capacitance value does not indicate the maximum load the device is capable of driving.

## 6.4 Device Functional Modes

DMD functional modes are controlled by the DLPC8454 display controller. See the DLPC8454 display controller data sheet or contact a TI applications engineer.

## 6.5 Optical Interface and System Image Quality Considerations

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance are contingent on compliance with the optical system operating conditions described in the following sections.

### 6.5.1 Numerical Aperture and Stray Light Control

TI recommends that the light cone angle defined by the numerical aperture of the illumination optics is the same as the light cone angle defined by the numerical aperture of the projection optics. This angle must not exceed the nominal device micromirror tilt angle unless appropriate apertures are added in the illumination and projection pupils to block out flat-state and stray light from the projection lens. The micromirror tilt angle defines the DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD, such as prism or lens surfaces. If the numerical aperture exceeds the micromirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle (and vice versa), contrast degradation and objectionable artifacts in the display border and or active area could occur.

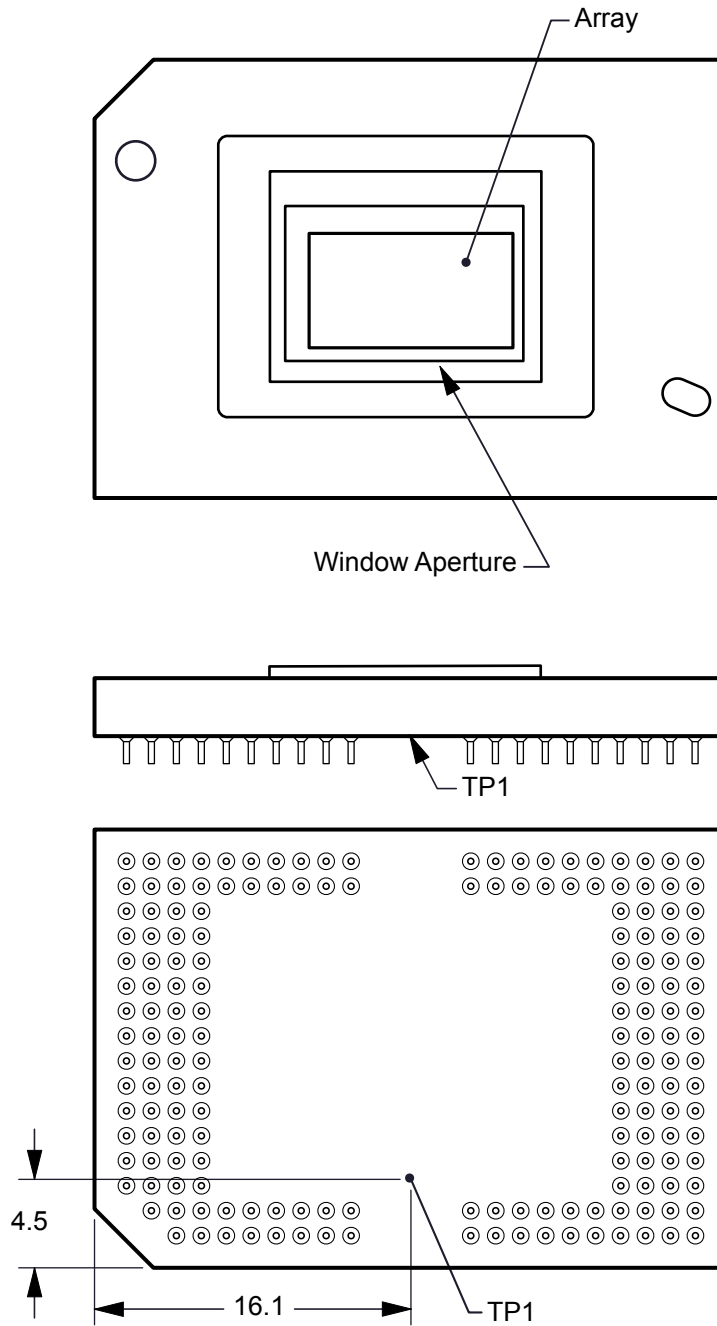
### 6.5.2 Pupil Match

TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

### 6.5.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. Design the illumination optical system to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system's optical architecture, overfill light on the window aperture may have to be further reduced below the suggested 10% maximum level in order to be acceptable.

## 6.6 Micromirror Array Temperature Calculation



**Figure 6-1. DMD Thermal Test Points**



Micromirror array temperature cannot be measured directly; therefore, it must be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The following equations show the relationship between array temperature and the reference ceramic temperature, thermal test TP1, shown above.

$$T_{\text{ARRAY}} = T_{\text{CERAMIC}} + (Q_{\text{ARRAY}} \times R_{\text{ARRAY-TO-CERAMIC}}) \quad (1)$$

$$Q_{\text{ARRAY}} = Q_{\text{ELECTRICAL}} + Q_{\text{ILLUMINATION}} \quad (2)$$

where

- $T_{\text{ARRAY}}$  = Computed array temperature (°C)
- $T_{\text{CERAMIC}}$  = Measured ceramic temperature (°C) (TP1 location)
- $R_{\text{ARRAY-TO-CERAMIC}}$  = Thermal resistance of the package specified in [Section 5.5](#) from array to ceramic TP1 (°C/Watt)
- $Q_{\text{ARRAY}}$  = Total DMD power on the array (W) (electrical + absorbed)
- $Q_{\text{ELECTRICAL}}$  = Nominal electrical power (W)
- $Q_{\text{INCIDENT}}$  = Incident illumination optical power (W)
- $Q_{\text{ILLUMINATION}}$  = (DMD average thermal absorptivity  $\times$   $Q_{\text{INCIDENT}}$ ) (W)
- DMD average thermal absorptivity = 0.54

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies. A nominal electrical power dissipation to use when calculating array temperature is 0.6W. The absorbed power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. The equations shown above are valid for a single-chip or multichip DMD system. It assumes an illumination distribution of 83.7% on the active array and 16.3% on the array border.

The sample calculation for a typical projection application is as follows:

$$Q_{\text{INCIDENT}} = 35\text{W (measured)} \quad (3)$$

$$T_{\text{CERAMIC}} = 50.0^{\circ}\text{C (measured)} \quad (4)$$

$$Q_{\text{ELECTRICAL}} = 0.6\text{W} \quad (5)$$

$$Q_{\text{ARRAY}} = 0.6\text{W} + (0.54 \times 35\text{ W}) = 19.5\text{W} \quad (6)$$

$$T_{\text{ARRAY}} = 50.0^{\circ}\text{C} + (19.5\text{W} \times 1.0^{\circ}\text{C/W}) = 69.5^{\circ}\text{C} \quad (7)$$

## 6.7 Micromirror Power Density Calculation

The calculation of the optical power density of the illumination on the DMD in the different wavelength bands uses the total measured optical power on the DMD, the percent illumination overfill, the area of the active array, and the ratio of the spectrum in the wavelength band of interest to the total spectral optical power.

- $ILL_{\text{UV}} = [OP_{\text{UV-RATIO}} \times Q_{\text{INCIDENT}}] \times 1000\text{mW/W} \div A_{\text{ILL}}$  (mW/cm<sup>2</sup>)
- $ILL_{\text{VIS}} = [OP_{\text{VIS-RATIO}} \times Q_{\text{INCIDENT}}] \div A_{\text{ILL}}$  (W/cm<sup>2</sup>)
- $ILL_{\text{IR}} = [OP_{\text{IR-RATIO}} \times Q_{\text{INCIDENT}}] \times 1000\text{mW/W} \div A_{\text{ILL}}$  (mW/cm<sup>2</sup>)
- $ILL_{\text{BLU}} = [OP_{\text{BLU-RATIO}} \times Q_{\text{INCIDENT}}] \div A_{\text{ILL}}$  (W/cm<sup>2</sup>)
- $ILL_{\text{BLU1}} = [OP_{\text{BLU1-RATIO}} \times Q_{\text{INCIDENT}}] \div A_{\text{ILL}}$  (W/cm<sup>2</sup>)
- $A_{\text{ILL}} = A_{\text{ARRAY}} \div (1 - OV_{\text{ILL}})$  (cm<sup>2</sup>)

where:

- $ILL_{UV}$  = UV illumination power density on the DMD ( $mW/cm^2$ )
- $ILL_{VIS}$  = VIS illumination power density on the DMD ( $W/cm^2$ )
- $ILL_{IR}$  = IR illumination power density on the DMD ( $mW/cm^2$ )
- $ILL_{BLU}$  = BLU illumination power density on the DMD ( $W/cm^2$ )
- $ILL_{BLU1}$  = BLU1 illumination power density on the DMD ( $W/cm^2$ )
- $A_{ILL}$  = illumination area on the DMD ( $cm^2$ )
- $Q_{INCIDENT}$  = total incident optical power on DMD (W) (measured)
- $A_{ARRAY}$  = area of the array ( $cm^2$ ) (data sheet)
- $OV_{ILL}$  = percent of total illumination on the DMD outside the array (%) (optical model)
- $OP_{UV-RATIO}$  = ratio of the optical power for wavelengths  $<410nm$  to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{VIS-RATIO}$  = ratio of the optical power for wavelengths  $\geq 410nm$  and  $\leq 800nm$  to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{IR-RATIO}$  = ratio of the optical power for wavelengths  $>800nm$  to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{BLU-RATIO}$  = ratio of the optical power for wavelengths  $\geq 410nm$  and  $\leq 475nm$  to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{BLU1-RATIO}$  = ratio of the optical power for wavelengths  $\geq 410nm$  and  $\leq 440nm$  to the total optical power in the illumination spectrum (spectral measurement)

The illumination area varies and depends on the illumination overfill. The total illumination area on the DMD is the array area and the overfill area around the array. The optical model is used to determine the percent of the total illumination on the DMD that is outside the array ( $OV_{ILL}$ ) and the percent of the total illumination that is on the active array. From these values, the illumination area ( $A_{ILL}$ ) is calculated. The illumination is assumed to be uniform across the entire array.

From the measured illumination spectrum, the ratio of the optical power in the wavelength bands of interest to the total optical power is calculated.

Sample calculation:

$$Q_{INCIDENT} = 35W \text{ (measured)} \quad (8)$$

$$A_{ARRAY} = (10.368mm \times 5.832mm) \div 100mm^2/cm^2 = 0.6047cm^2 \text{ (data sheet)} \quad (9)$$

$$OV_{ILL} = 16.3\% \text{ (optical model)} \quad (10)$$

$$OP_{UV-RATIO} = 0.00017 \text{ (spectral measurement)} \quad (11)$$

$$OP_{VIS-RATIO} = 0.99977 \text{ (spectral measurement)} \quad (12)$$

$$OP_{IR-RATIO} = 0.00006 \text{ (spectral measurement)} \quad (13)$$

$$OP_{BLU-RATIO} = 0.28100 \text{ (spectral measurement)} \quad (14)$$

$$OP_{BLU1-RATIO} = 0.03200 \text{ (spectral measurement)} \quad (15)$$

$$A_{ILL} = 0.6047cm^2 \div (1 - 0.163) = 0.7224cm^2 \quad (16)$$

$$ILL_{UV} = [0.00017 \times 35W] \times 1000 \text{ mW/W} \div 0.7224\text{cm}^2 = 8.236\text{mW/cm}^2 \quad (17)$$

$$ILL_{VIS} = [0.99977 \times 35W] \div 0.7224\text{cm}^2 = 48.44\text{W/cm}^2 \quad (18)$$

$$ILL_{IR} = [0.00006 \times 35W] \times 1000\text{mW/W} \div 0.7224\text{cm}^2 = 2.907\text{mW/cm}^2 \quad (19)$$

$$ILL_{BLU} = [0.28100 \times 35W] \div 0.7224\text{cm}^2 = 13.61\text{W/cm}^2 \quad (20)$$

$$ILL_{BLU1} = [0.03200 \times 35W] \div 0.7224\text{cm}^2 = 1.55\text{W/cm}^2 \quad (21)$$

## 6.8 Window Aperture Illumination Overfill Calculation

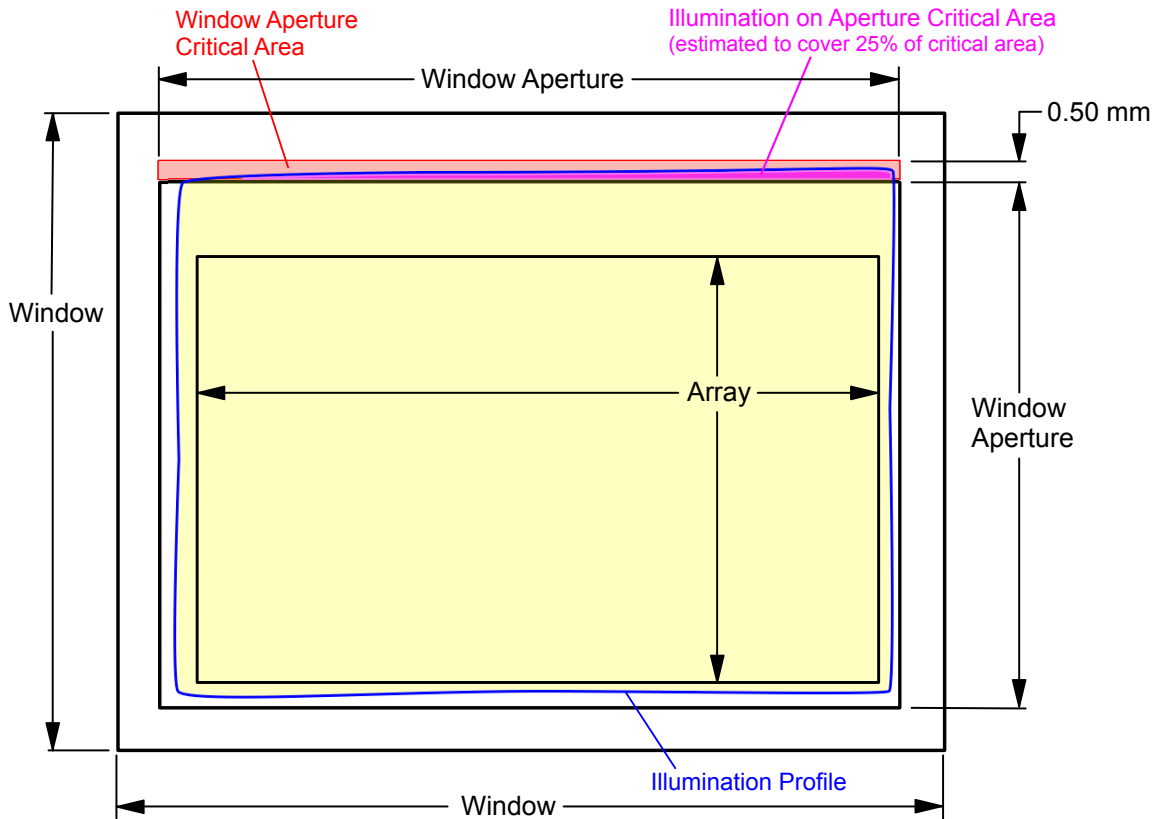
The amount of optical overfill on the critical area of the window aperture cannot be measured directly. For systems with uniform illumination on the array, the amount is determined using the total measured incident optical power on the DMD and the ratio of the total optical power on the DMD that is on the defined critical area. The optical model is used to determine the percent of optical power on the window aperture critical area and estimate the size of the area.

- $Q_{AP-ILL} = [Q_{INCIDENT} \times OP_{AP\_ILL\_RATIO}] \div A_{AP\_ILL} \text{ (W/cm}^2\text{)}$

where:

- $Q_{AP-ILL}$  = window aperture illumination overfill (W/cm<sup>2</sup>)
- $Q_{INCIDENT}$  = total incident optical power on the DMD (Watts) (measured)
- $OP_{AP\_ILL\_RATIO}$  = ratio of the optical power on the critical area of the window aperture to the total optical power on the DMD (optical model)
- $A_{AP-ILL}$  = size of the window aperture critical area (cm<sup>2</sup>) (data sheet)
- $OP_{CA\_RATIO}$  = percent of the window aperture critical area with incident optical power (%) (optical model)

Sample calculation:



**Figure 6-2. Window Aperture Overfill Example**

See the figure for the length of the critical aperture.

$$Q_{\text{INCIDENT}} = 35\text{W (measured)} \quad (22)$$

$$OP_{\text{AP\_ILL\_RATIO}} = 0.312\% \text{ (optical model)} \quad (23)$$

$$OV_{\text{CA\_RATIO}} = 25\% \text{ (optical model)} \quad (24)$$

$$\text{Length of the window aperture for critical area} = 1.2496\text{cm (data sheet)} \quad (25)$$

$$\text{Width of critical area} = 0.050\text{cm (data sheet)} \quad (26)$$

$$A_{\text{AP-ILL}} = 1.2496\text{cm} \times 0.050\text{cm} = 0.06248 \text{ (cm}^2\text{)} \quad (27)$$

$$Q_{\text{AP-ILL}} = (35\text{W} \times 0.00312) \div (0.06248\text{cm}^2 \times 0.25) = 7.0\text{(W/cm}^2\text{)} \quad (28)$$

## 6.9 Micromirror Landed-On/Landed-Off Duty Cycle

### 6.9.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the percentage of time that an individual micromirror is landed in the ON state versus the amount of time the same micromirror is landed in the OFF state.

For example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the ON state 100% of the time (and in the OFF state 0% of the time); whereas 0/100 would indicate that the pixel is in the OFF state 100% of the time. Likewise, 50/50 indicates that the pixel is ON for 50% of the time (and OFF for 50% of the time).

Note that when assessing the landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) always add to 100.

### 6.9.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD useful life.

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

### 6.9.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD temperature and landed duty cycle interact to affect DMD useful life, and this interaction can be exploited to reduce the impact that an asymmetrical landed duty cycle has on the DMD useful life. This is quantified in the derating curve shown in [Figure 5-1](#). The importance of this curve is that:

- All points along this curve represent the same useful life.
- All points above this curve represent a lower useful life (and the further away from the curve, the lower the useful life).
- All points below this curve represent a higher useful life (and the further away from the curve, the higher the useful life).

In practice, this curve specifies the maximum operating DMD temperature for a given long-term average landed duty cycle.

### 6.9.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the landed duty cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel operates under a 100/0 landed duty cycle during that time period. Likewise, when displaying pure-black, the pixel operates under a 0/100 landed duty cycle.

Between the two extremes (ignoring, for the moment, color and any image processing that may be applied to an incoming image), the landed duty cycle tracks one-to-one with the gray scale value, as shown in [Table 6-1](#).

**Table 6-1. Grayscale Value and Landed Duty Cycle**

GRAYSCALE VALUE	LANDED DUTY CYCLE
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and/or blue) for the given pixel as well as the color cycle time for each primary color, where “color cycle time” is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

Use [Equation 29](#) to calculate the landed duty cycle of a given pixel during a given time period.

$$\text{Landed Duty Cycle} = (\text{Red\_Cycle\_}\% \times \text{Red\_Scale\_Value}) + (\text{Green\_Cycle\_}\% \times \text{Green\_Scale\_Value}) + (\text{Blue\_Cycle\_}\% \times \text{Blue\_Scale\_Value}) \quad (29)$$

where

- Red\_Cycle\_%, represents the percentage of the frame time that red is displayed to achieve the desired white point.
- Green\_Cycle\_% represents the percentage of the frame time that green is displayed to achieve the desired white point.
- Blue\_Cycle\_%, represents the percentage of the frame time that blue is displayed to achieve the desired white point.

For example, assume that the red, green, and blue color cycle times are 30%, 50%, and 20% respectively (in order to achieve the desired white point), then the landed duty cycle for various combinations of red, green, blue color intensities would be as shown in [Table 6-2](#) and [Table 6-3](#).

**Table 6-2. Example Landed Duty Cycle for Full-Color, Color Percentage**

CYCLE PERCENTAGE		
RED	GREEN	BLUE
30%	50%	20%

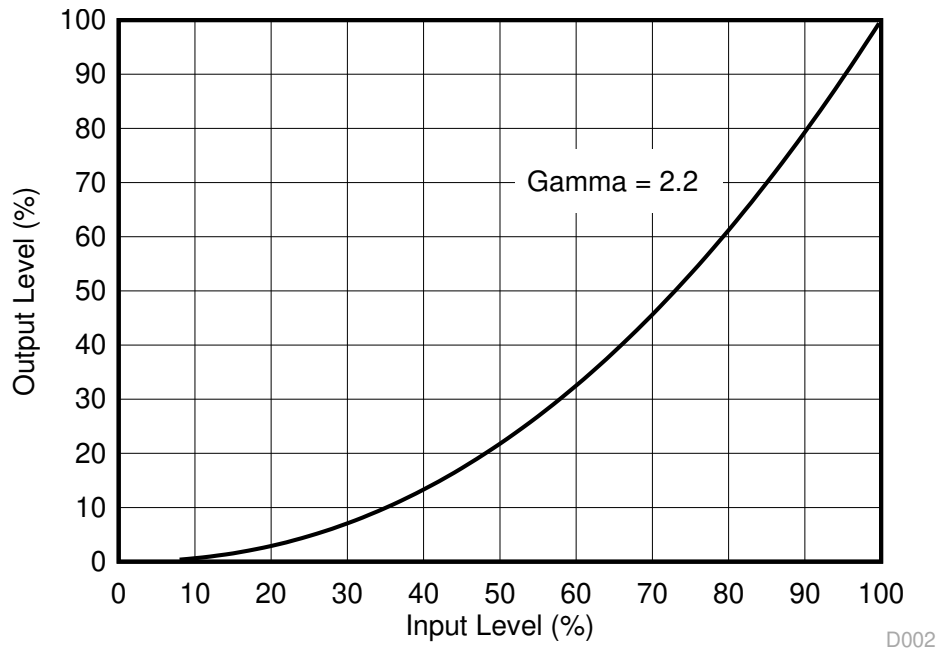
**Table 6-3. Example Landed Duty Cycle for Full-Color**

SCALE VALUE			LANDED DUTY CYCLE
RED	GREEN	BLUE	
0%	0%	0%	0/100
100%	0%	0%	30/70
0%	100%	0%	50/50
0%	0%	100%	20/80
0%	12%	0%	6/94
0%	0%	35%	7/93
60%	0%	0%	18/82
0%	100%	100%	70/30
100%	0%	100%	50/50
100%	100%	0%	80/20
0%	12%	35%	13/87
60%	0%	35%	25/75
60%	12%	0%	24/76
100%	100%	100%	100/0

The last factor to account for in estimating the landed duty cycle is any applied image processing. Within the DLPC8454 controller, the gamma function affects the landed duty cycle.

Gamma is a power function of the form  $Output\_Level = A \times Input\_Level^{Gamma}$ , where A is a scaling factor that is typically set to 1.

In the DLPC8454 controller, gamma is applied to the incoming image data on a pixel-by-pixel basis. A typical gamma factor is 2.2, which transforms the incoming data as shown in [Figure 6-3](#).



**Figure 6-3. Example of Gamma = 2.2**

From [Figure 6-3](#), if the gray scale value of a given input pixel is 40% (before gamma is applied), then grayscale value is 13% after gamma is applied. Therefore, it can be seen that since gamma has a direct impact on the displayed gray scale level of a pixel, it also has a direct impact on the landed duty cycle of a pixel.

Consideration must also be given to any image processing that occurs before the DLPC8454 controllers.

## 7 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

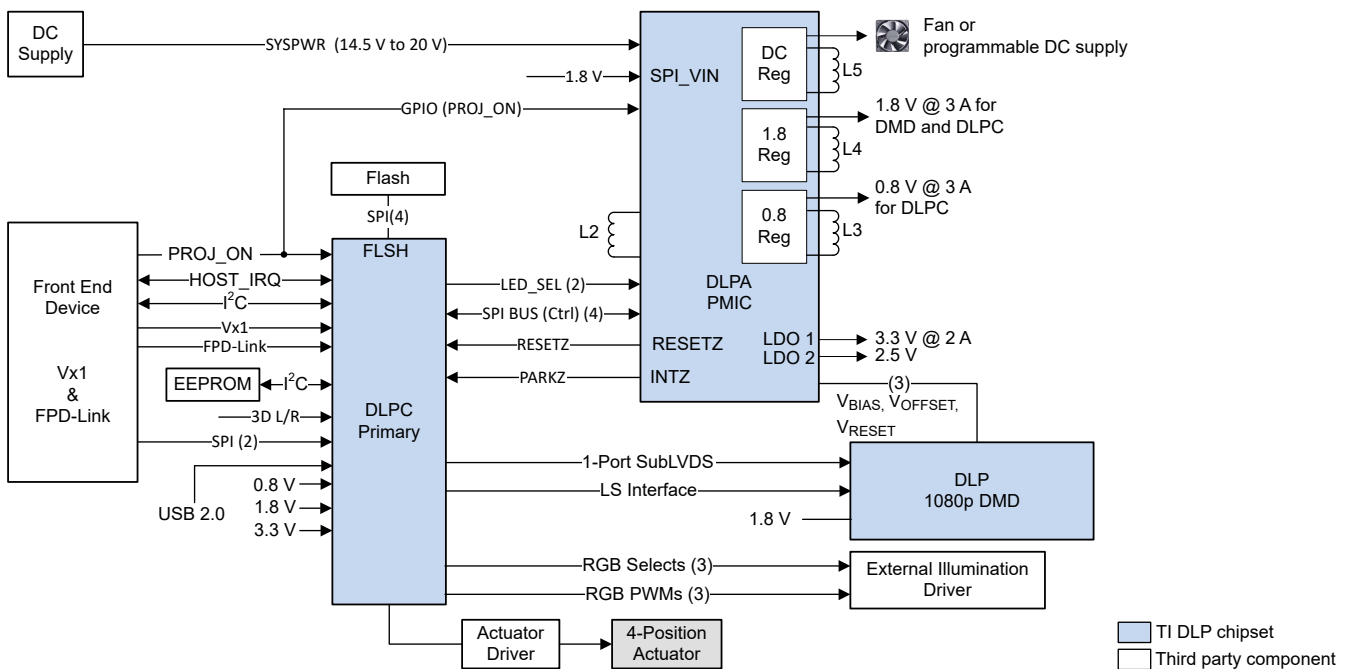
### 7.1 Application Information

DMDs are spatial light modulators that reflect incoming light from an illumination source in one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the DLPC8454 controller. The high-tilt pixel in the corner-illuminated DMD increases brightness performance and enables a smaller system footprint for thickness-constrained applications. Typical applications using the DLP473NE include Laser TVs, home cinemas, and business projectors.

DMD power-up and power-down sequencing are strictly controlled by the DLPC8454 through the DLPA3082 PMIC. Refer to [Section 8](#) for power-up and power-down specifications. To ensure reliable operation, the DLP473NE DMD must always be used with the DLPC8454 controller and the DLPA3082 PMIC.

### 7.2 Typical Application

The DLP473NE DMD combined with the DLPC8454 digital controller and a power management device provides full 1080p resolution for bright, colorful display applications. A typical RGB laser or LED system combines the DLP473NE DMD, DLPC8454 display controller, DLPA3082 voltage regulator, and the external illumination driver. In addition, the laser phosphor system includes the [DLPA100](#) motor driver. [Figure 7-1](#) shows a system block diagram for DLP 0.47" 1080p chipset.



**Figure 7-1. Typical 1080p System Diagram with External Illumination Driver**



### **7.2.1 Design Requirements**

Other core components of the display system include an illumination source, an optical engine for the illumination and projection optics, other electrical and mechanical components, and software. The type of illumination used and desired brightness have a major effect on the overall system design and size.

The display system uses the DLP473NE as the core imaging device and contains a 0.47-inch array of micromirrors. The DLPC8454 controller is the digital interface between the DMD and the rest of the system, taking digital input from the front-end receiver and driving the DMD over a high-speed interface. The DLPA3082 PMIC serves as a voltage regulator for the controller, and [DLPA100](#) is the color filter wheel and phosphor wheel motor control. The DLPA3082 PMIC also serves as a voltage regulator and provides the DMD reset, offset, and bias voltages.

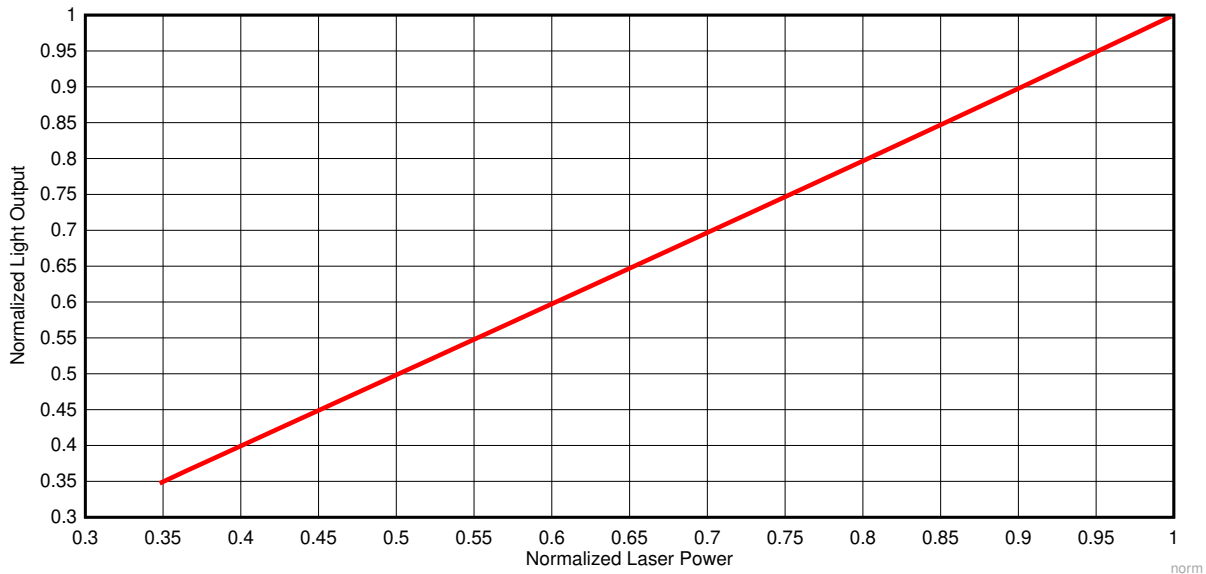
### **7.2.2 Detailed Design Procedure**

For a complete DLP system, an optical module or light engine is required that contains the DLP473NE DMD, associated illumination sources, optical elements, and necessary mechanical components.

To ensure reliable operation, the DMD must always be used with the DLPC8454 display controller and the [DLPA3082](#) PMIC. Refer to [PCB Design Requirements for TI DLP Digital Micromirror Devices](#) for the DMD board design and manufacturing handling of the DMD sub-assemblies.

### 7.2.3 Application Curve

In a typical projector application, the luminous flux on the screen from the DMD depends on the optical design of the projector. The efficiency and total power of the illumination optical system and the projection optical system determine the overall light output of the projector. The DMD is inherently a linear spatial light modulator, so its efficiency just scales the light output. [Figure 7-2](#) describes the relationship of laser input optical power to light output for a laser-phosphor illumination system, where the phosphor is not at its thermal quenching limit.

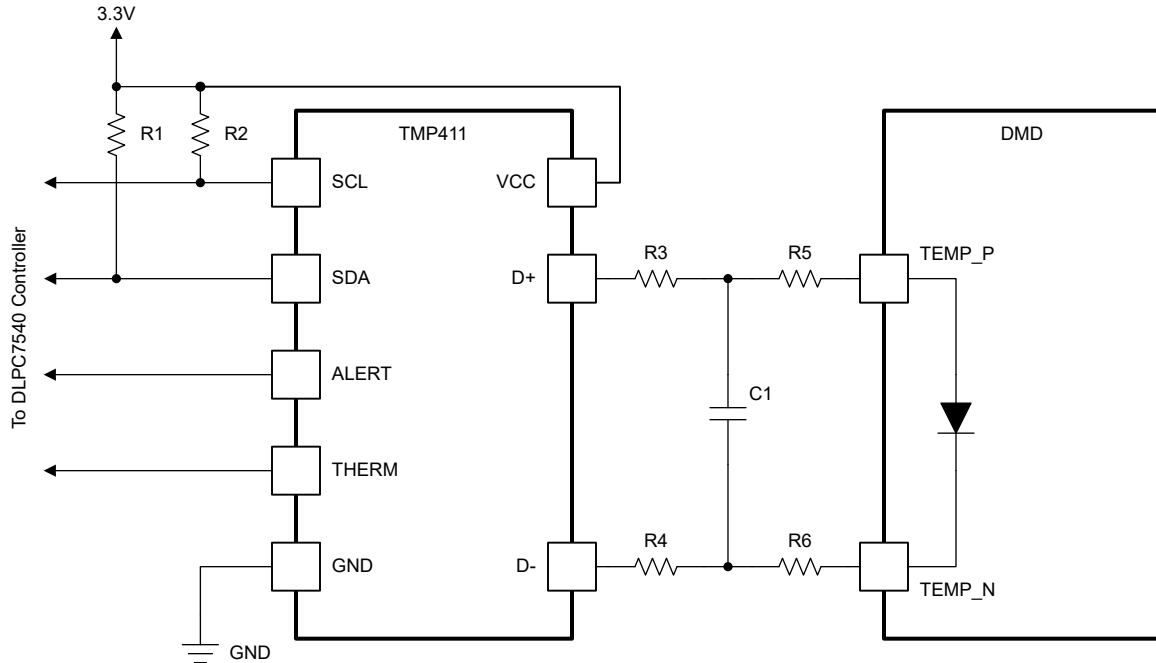


**Figure 7-2. Normalized Light Output vs Normalized Laser Power for Laser Phosphor Illumination**

### 7.3 Temperature Sensor Diode

The DMD features a built-in thermal diode that measures the temperature at one corner of the die outside the micromirror array. The thermal diode can be interfaced with the TMP411 temperature sensor, as shown in [Figure 7-3](#). The software application contains functions to configure the [TMP411](#) to read the DLP473NE DMD temperature sensor diode. This data can be leveraged by the customer to incorporate additional functionality in the overall system design such as adjusting illumination, fan speeds, etc. All communication between the [TMP411](#) and the DLPC8454 controller happens over the I<sup>2</sup>C interface. The [TMP411](#) connects to the DMD via pins outlined in [Table 4-1](#).

If the temp sensor is not used, TEMP\_N and TEMP\_P pins should be left unconnected (NC).



- A. Details omitted for clarity
- B. See the [TMP411](#) data sheet for the system board layout recommendation.
- C. See the [TMP411](#) data sheet and the T1 reference design for suggested component values for R1, R2, R3, R4, and C1.
- D. R5 = 0Ω. R6 = 0Ω. Place 0Ω resistors close to the DMD package pins.

**Figure 7-3. TMP411 Sample Schematic**

## 8 Power Supply Recommendations

The following power supplies are all required to operate the DMD:

- $V_{SS}$
- $V_{BIAS}$
- $V_{DD}$
- $V_{DDI}$
- $V_{OFFSET}$
- $V_{RESET}$

DMD power-up and power-down sequencing is strictly controlled by the DLP display controller.

### CAUTION

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to any of the prescribed power-up and power-down requirements may affect device reliability. See the DMD power supply sequencing requirements in [Figure 8-1](#).

$V_{BIAS}$ ,  $V_{DD}$ ,  $V_{DDI}$ ,  $V_{OFFSET}$ , and  $V_{RESET}$  power supplies must be coordinated during power-up and power-down operations. Failure to meet any of the below requirements will result in a significant reduction in the DMD reliability and lifetime. Common ground  $V_{SS}$  must also be connected.

**Table 8-1. Power Supply Sequence Requirements**

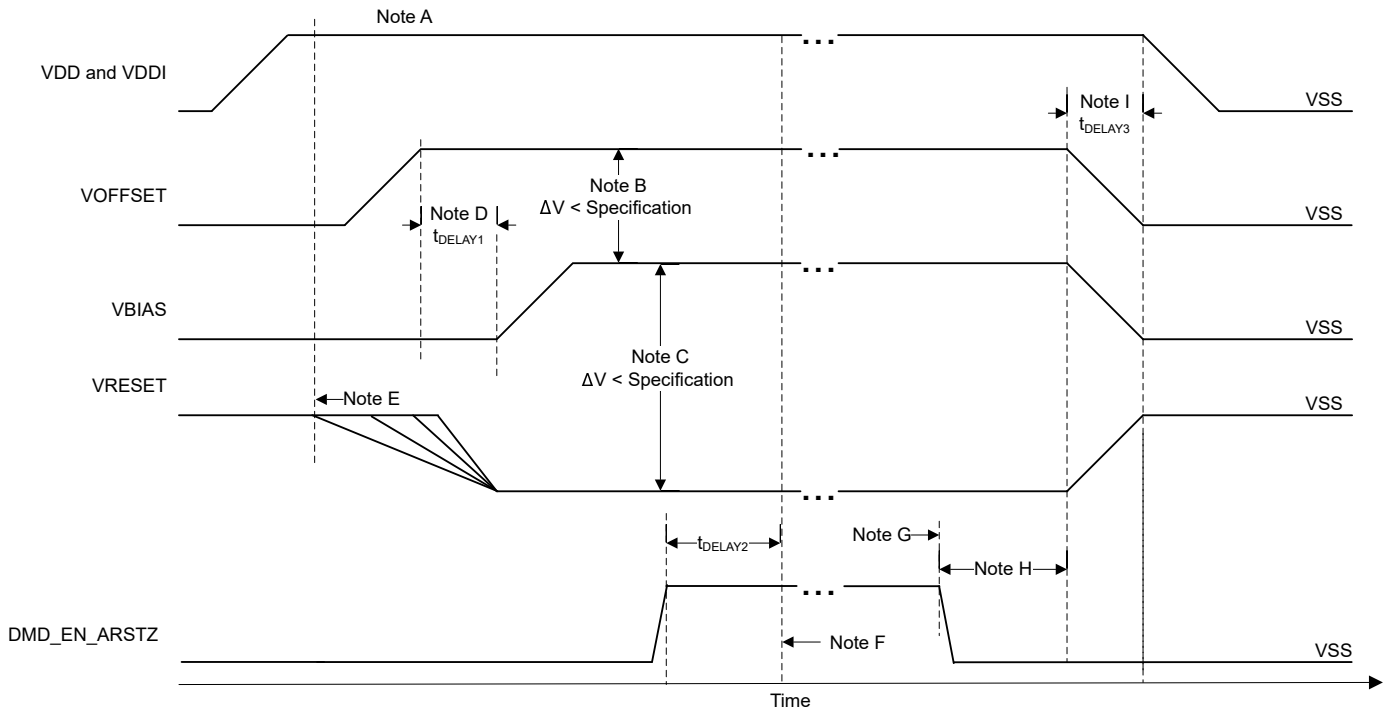
SYMBOL	PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
$t_{DELAY}$	Delay requirement	from $V_{OFFSET}$ power up to $V_{BIAS}$ power up	2			ms
$V_{OFFSET}$	Supply voltage level	at beginning of power-up sequence delay			6	V
$V_{BIAS}$	Supply voltage level	at end of power-up sequence delay			6	V

### 8.1 DMD Power Supply Power-Up Procedure

- During power-up,  $V_{DD}$  and  $V_{DDI}$  must always start and settle before  $V_{OFFSET}$  plus Delay1 specified in the *DMD power-supply requirements*,  $V_{BIAS}$ , and  $V_{RESET}$  voltages are applied to the DMD.
- During power-up, it is a strict requirement that the voltage difference between  $V_{BIAS}$  and  $V_{OFFSET}$  must be within the specified limit shown in the *recommended operating conditions*.
- During power-up, there is no requirement for the relative timing of  $V_{RESET}$  with respect to  $V_{BIAS}$ .
- Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements specified in the *absolute maximum ratings*, *recommended operating conditions*, and the *DMD power-supply requirements*.
- During power-up, LVCMOS input pins must not be driven high until after  $V_{DD}$  have settled at operating voltages listed in the *recommended operating conditions*.

### 8.2 DMD Power Supply Power-Down Procedure

- During power-down,  $V_{DD}$  and  $V_{DDI}$  must be supplied until after  $V_{BIAS}$ ,  $V_{RESET}$ , and  $V_{OFFSET}$  are discharged to within the specified limit of ground. See the *DMD power-supply requirements*.
- During power-down, it is a strict requirement that the voltage difference between  $V_{BIAS}$  and  $V_{OFFSET}$  must be within the specified limit shown in the *recommended operating conditions*.
- During power-down, there is no requirement for the relative timing of  $V_{RESET}$  with respect to  $V_{BIAS}$ .
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements specified in *absolute maximum ratings*, in the *recommended operating conditions*, and in the *DMD power-supply requirements*.
- During power-down, LVCMOS input pins must be less than specified in the *recommended operating conditions*.



- A. See the *pin configuration and functions* section for the *Pin Functions Table*.
- B. To prevent excess current, the supply voltage difference  $|V_{\text{OFFSET}} - V_{\text{BIAS}}|$  must be less than the specified limit in the *recommended operating conditions*.
- C. To prevent excess current, the supply difference  $|V_{\text{BIAS}} - V_{\text{RESET}}|$  must be less than the specified limit in the *recommended operating conditions*.
- D.  $V_{\text{BIAS}}$  should power up after  $V_{\text{OFFSET}}$  has powered up, per the Delay1 specification in *DMD power-supply requirements*.
- E. DLP controller software initiates the global  $V_{\text{BIAS}}$  command.
- F. After the DMD micromirror park sequence is complete, the DLP controller software initiates a hardware power-down that activates  $\text{DMD\_EN\_ARSTZ}$  and disables  $V_{\text{BIAS}}$ ,  $V_{\text{RESET}}$ , and  $V_{\text{OFFSET}}$ .
- G. Under power-loss conditions where emergency DMD micromirror park procedures are being enacted by the DLP controller hardware  $\text{DMD\_EN\_ARSTZ}$  will go low.
- H.  $V_{\text{DD}}$  must remain high until after  $V_{\text{OFFSET}}$ ,  $V_{\text{BIAS}}$ , and  $V_{\text{RESET}}$  go low, per Delay2 specification in *DMD power-supply requirements*.
- I. To prevent excess current, the supply voltage delta  $|V_{\text{DDI}} - V_{\text{DD}}|$  must be less than the specified limit in the *recommended operating conditions*.

**Figure 8-1. DMD Power-Supply Requirements**

**Table 8-2. DMD Power-Supply Requirements**

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNIT
Delay1 <sup>(1)</sup>	Delay from $V_{\text{OFFSET}}$ settled at recommended operating voltage to $V_{\text{BIAS}}$ and $V_{\text{RESET}}$ power up	1	2		ms
Delay2 <sup>(1)</sup>	Delay $V_{\text{DD}}$ must be held high from $V_{\text{OFFSET}}$ , $V_{\text{BIAS}}$ , and $V_{\text{RESET}}$ powering down.	50			$\mu\text{s}$

(1) See the *DMD power-supply requirements*.

## 9 Device and Documentation Support

### 9.1 Third-Party Products Disclaimer

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### 9.2 Device Support

#### 9.2.1 Device Nomenclature

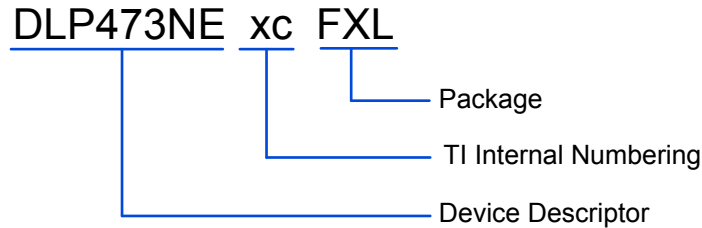


Figure 9-1. Part Number Description

#### 9.2.2 Device Markings

The device marking includes both human-readable information and a 2-dimensional matrix code. The human-readable information is described in Figure 9-2. The 2-dimensional matrix code is an alpha-numeric string that contains the DMD part number, Part 1 and Part 2 of the serial number.

Example:

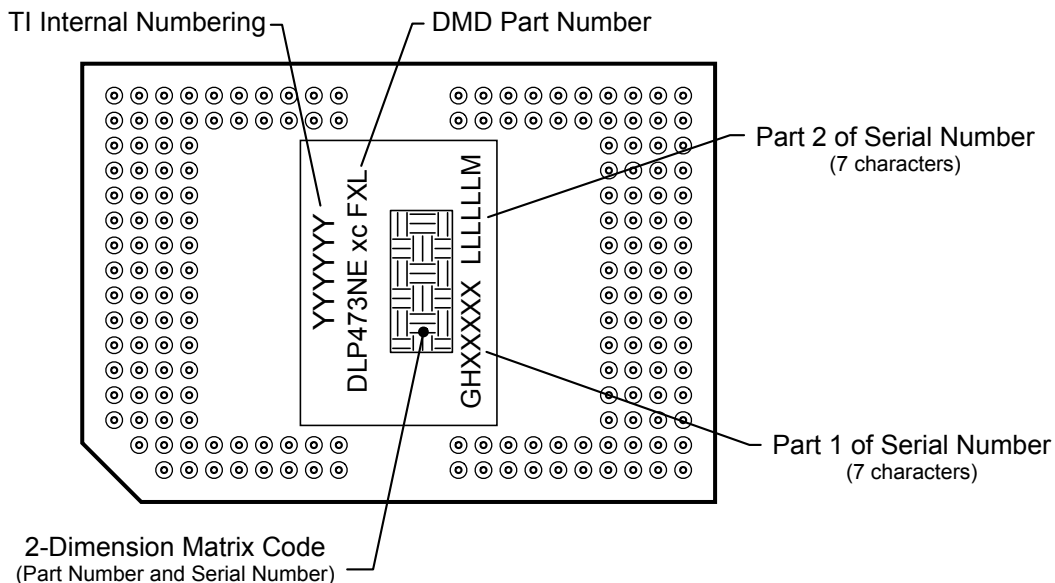


Figure 9-2. DMD Marking Locations

## 9.3 Documentation Support

### 9.3.1 Related Documentation

The following documents contain additional information related to the chipset components used with the DMD.

- Texas Instruments, [DLPC8454](#) controller data sheet
- Texas Instruments, [DLPA3082](#) PMIC data sheet
- Texas Instruments, [DLPA100](#) Motor Driver data sheet

## 9.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.5 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

## 9.6 Trademarks

TI E2E™ is a trademark of Texas Instruments.

DLP® is a registered trademark of Texas Instruments.

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## 9.7 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.8 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2025	*	Initial Release

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">DLP473NE0FXL</a>	Active	Production	CPGA (FXL)   173	33   JEDEC TRAY (5+1)	Yes	NIPDAU	N/A for Pkg Type	0 to 70	

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

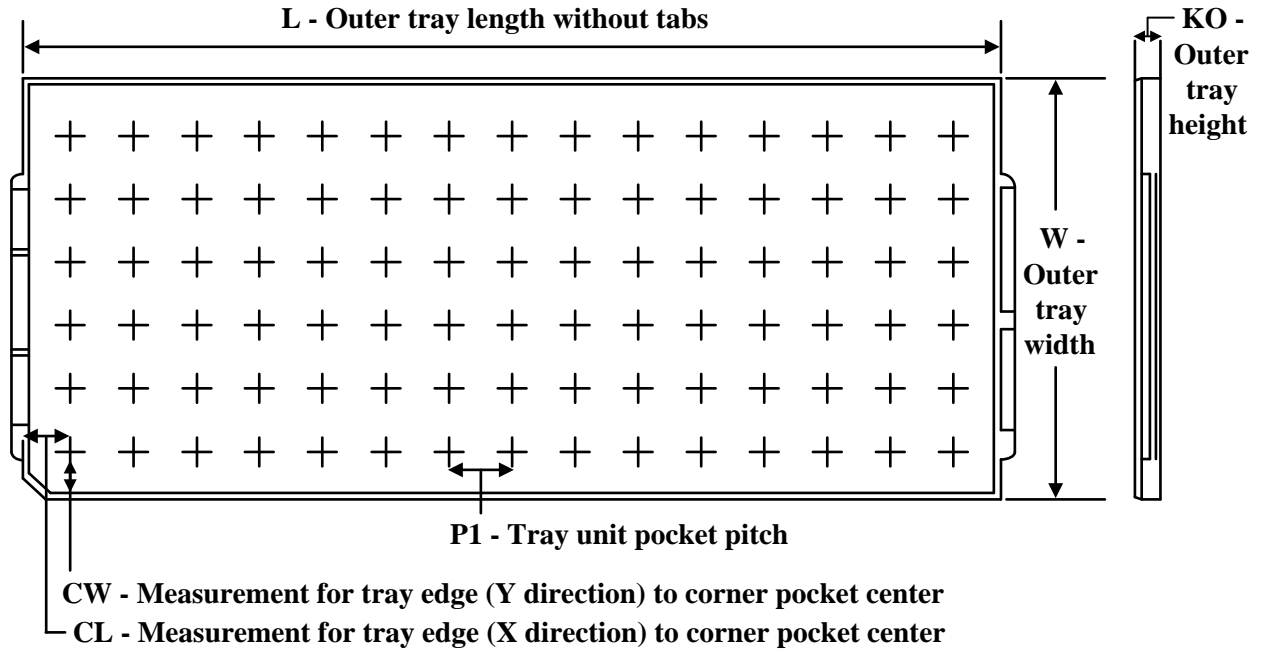
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TRAY**



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

\*All dimensions are nominal

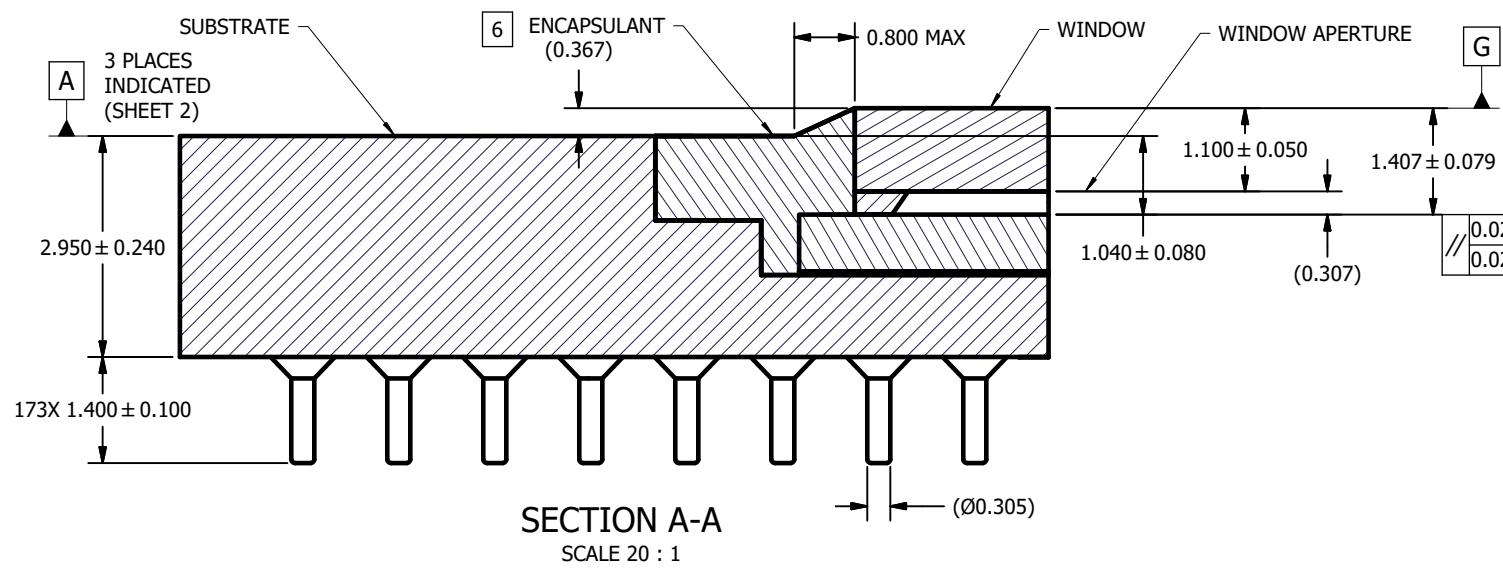
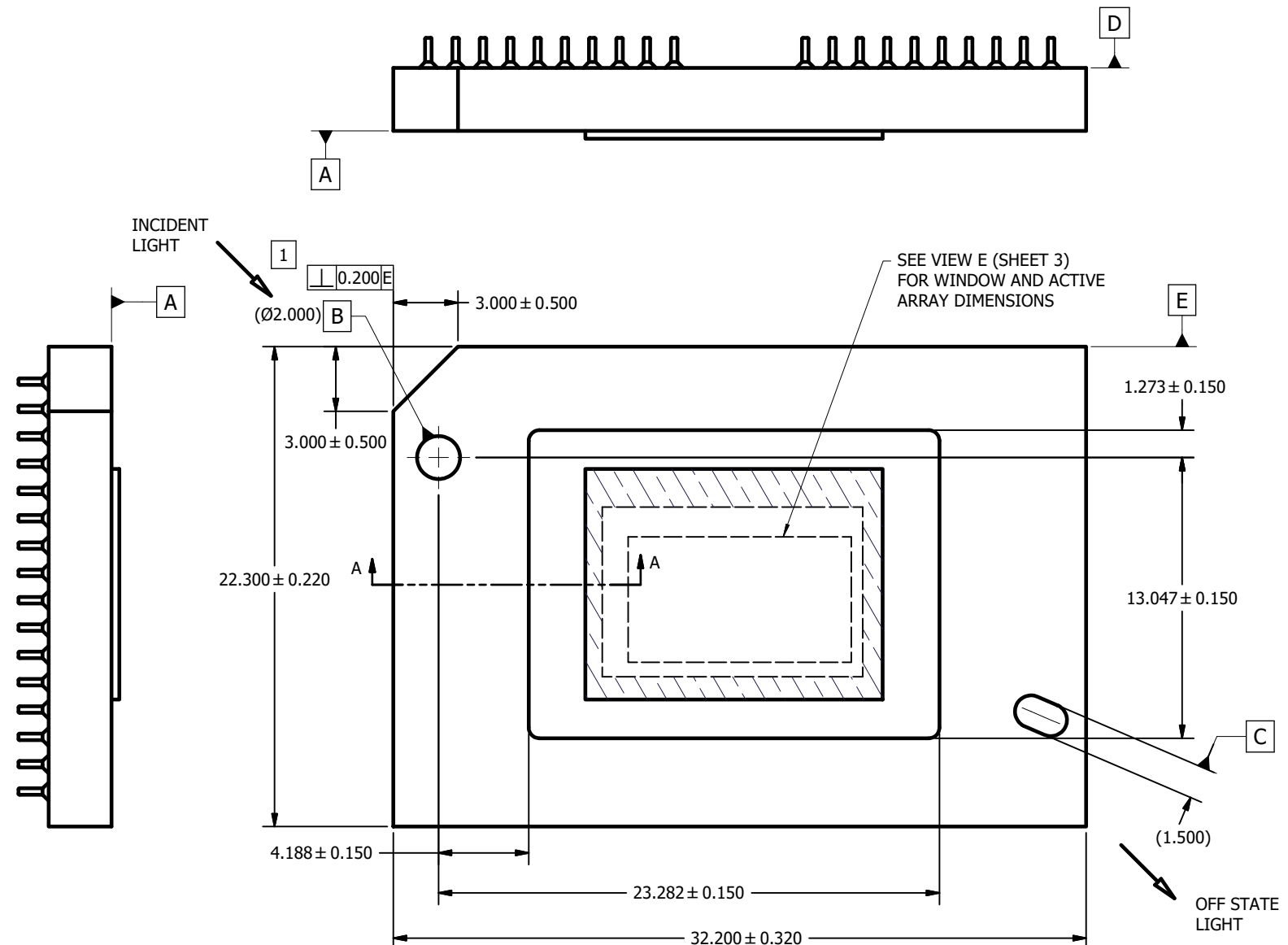
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DLP473NE0FXL	FXL	CPGA	173	33	3 x 11	150	315	135.9	12190	27.5	20	27.45

NOTES UNLESS OTHERWISE SPECIFIED:

- 1 SUBSTRATE EDGE PERPENDICULARITY TOLERANCE APPLIES TO ENTIRE SURFACE.
- 2 DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY.
- 3 ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM VALUE OF 0.8 DEGREES.
- 4 SUBSTRATE SYMBOLIZATION PAD AND PLATING AT BOTTOM OF DATUMS B AND C HOLES TO BE ELECTRICALLY CONNECTED TO VSS PLANE WITHIN THE SUBSTRATE.
- 5 BOUNDARY MIRRORS SURROUNDING THE ACTIVE ARRAY.
- 6 MAXIMUM ENCAPSULANT PROFILE SHOWN.
- 7 ENCAPSULANT ALLOWED ON THE SURFACE OF THE CERAMIC IN THE AREA SHOWN IN VIEW B (SHEET 2). ENCAPSULATION SHALL NOT EXCEED 0.2 THICKNESS MAXIMUM.
- 8 SUBSTRATES PLATED WITH Ni/Au SHALL HAVE THE THREE-DIGIT NUMERICAL MARKING IN THE AREA ABOVE THE SYMBOLIZATION PAD. SUBSTRATES PLATED WITH Ni/Pd/Au SHALL HAVE THE MARKING IN THE AREA BELOW THE SYMBOLIZATION PAD.

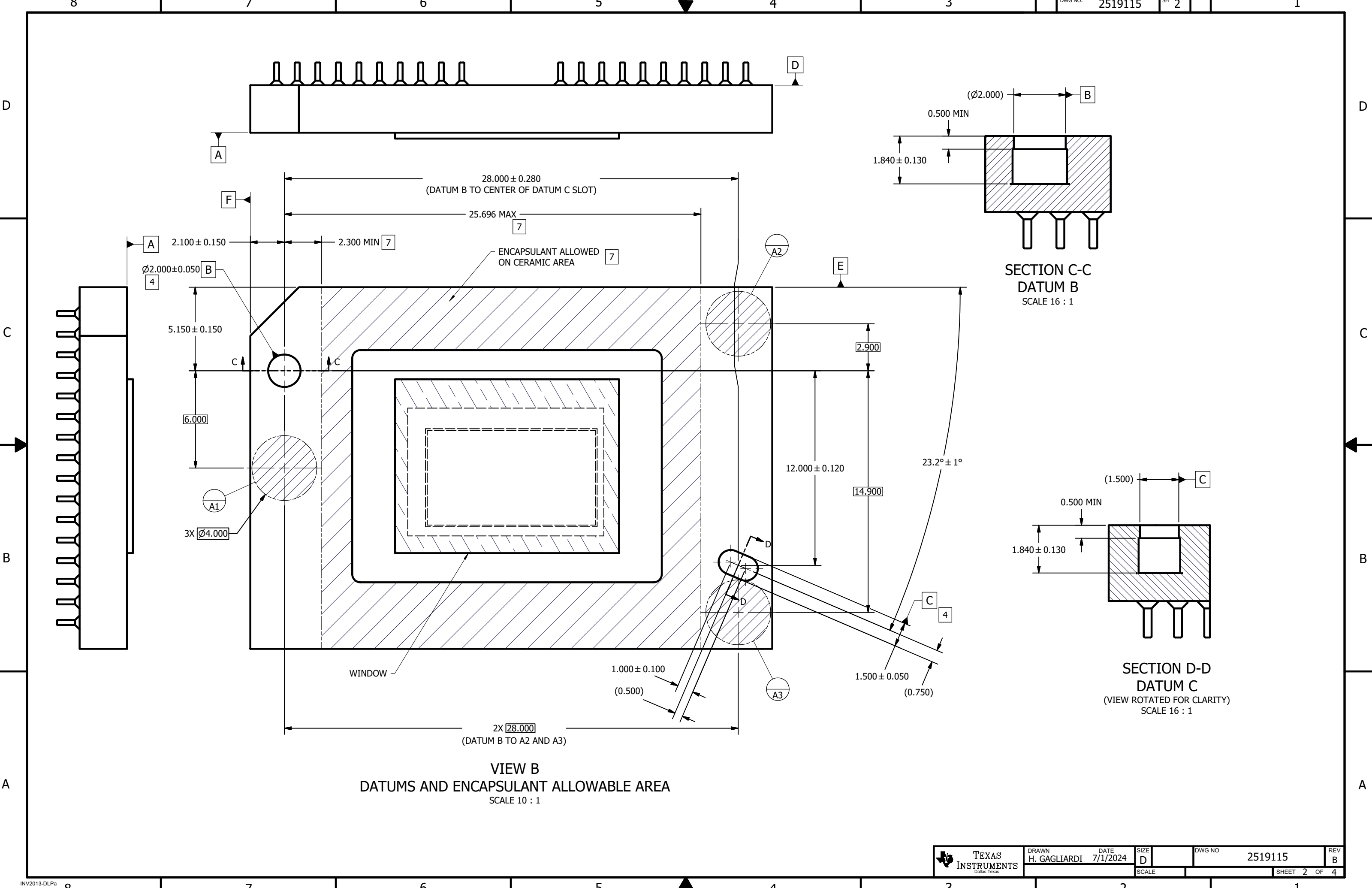
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REVISIONS		DATE	BY
A	ECO 2209145: INITIAL RELEASE	07/01/2024	HG
B	ECO 2211621: UPDATE PoM DIMENSIONS	01/22/2025	PPC



SECTION A-A  
SCALE 20 : 1

UNLESS OTHERWISE SPECIFIED		DRAWN H. GAGLIARDI 7/1/2024		DATE 7/1/2024	
● DIMENSIONS ARE IN MILLIMETERS		ENGINEER H. GAGLIARDI 7/8/2024		TITLE ICD, MECHANICAL, DMD .47" SST subLVDS SERIES 460 (FXL PACKAGE)	
● TOLERANCES:		QA/CE M. DORAK 7/2/2024		SIZE D	
ANGLES ± 1°		CM M. GARCIA 7/1/2024		DWG NO. 2519115	
2 PLACE DECIMALS ± 0.25		APPROVED J. MCKINLEY 7/3/2024		REV B	
1 PLACE DECIMALS ± 0.50		SCALE 4:1		SHEET 1 OF 4	
● DIMENSIONAL LIMITS APPLY BEFORE PROCEEDING					
● INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5M-1994					
● REMOVE ALL BURRS AND SHARP EDGES					
● PARENTHETICAL INFORMATION FOR REFERENCE ONLY					



28.000 ± 0.280  
(DATUM B TO CENTER OF DATUM C SLOT)

25.696 MAX

ENCAPSULANT ALLOWED ON CERAMIC AREA

SECTION C-C  
DATUM B  
SCALE 16 : 1

SECTION D-D  
DATUM C  
(VIEW ROTATED FOR CLARITY)  
SCALE 16 : 1

VIEW B  
DATUMS AND ENCAPSULANT ALLOWABLE AREA  
SCALE 10 : 1

8

7

6

5

4

3

DWG NO. 2519115 SH 3

1

D

D

C

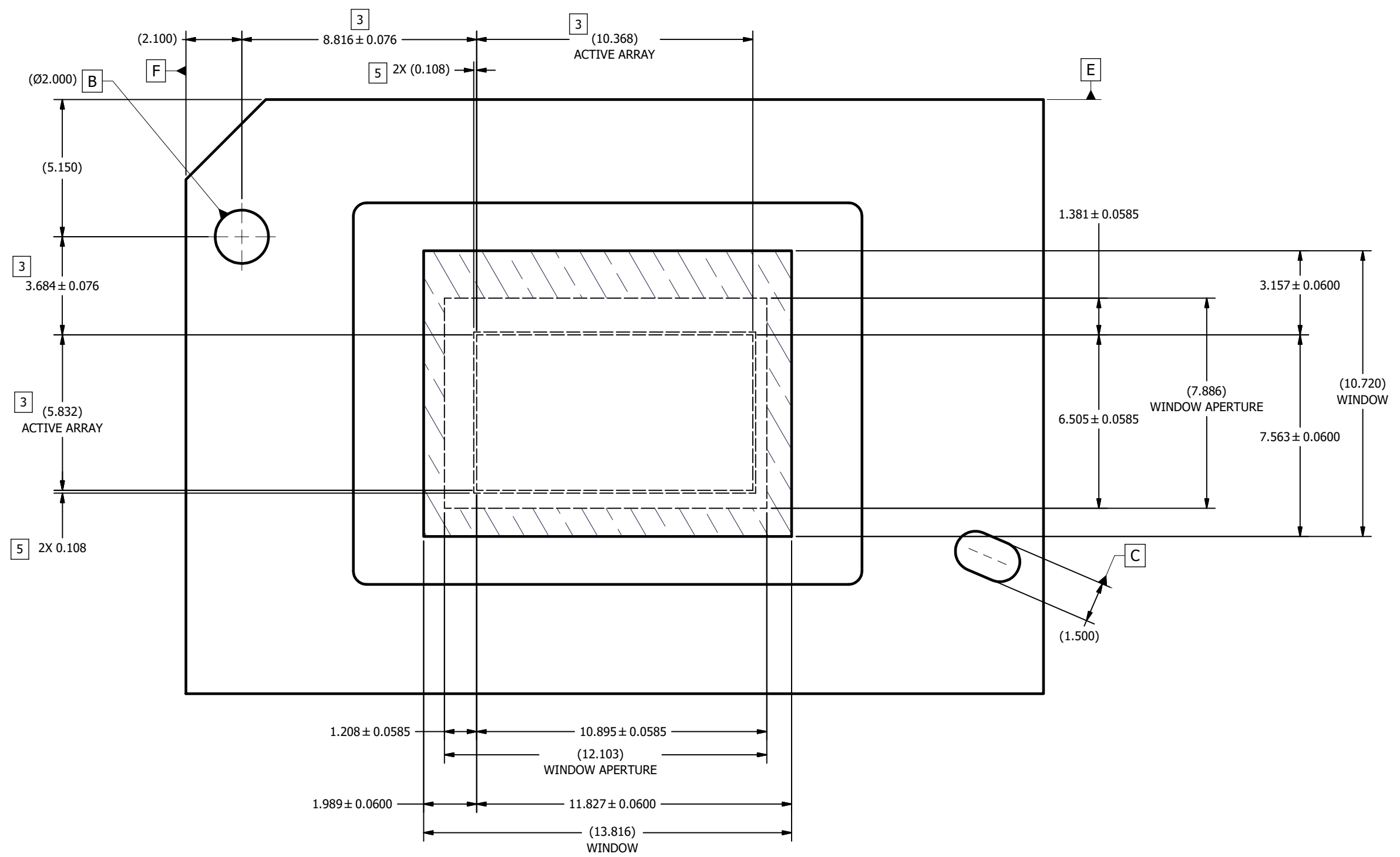
C

B

B

A

A



VIEW E  
ACTIVE ARRAY AND WINDOW  
SCALE 12 : 1



DRAWN H. GAGLIARDI DATE 7/1/2024

SIZE D

DWG NO. 2519115

REV B

SCALE

SHEET 3 OF 4

8

7

6

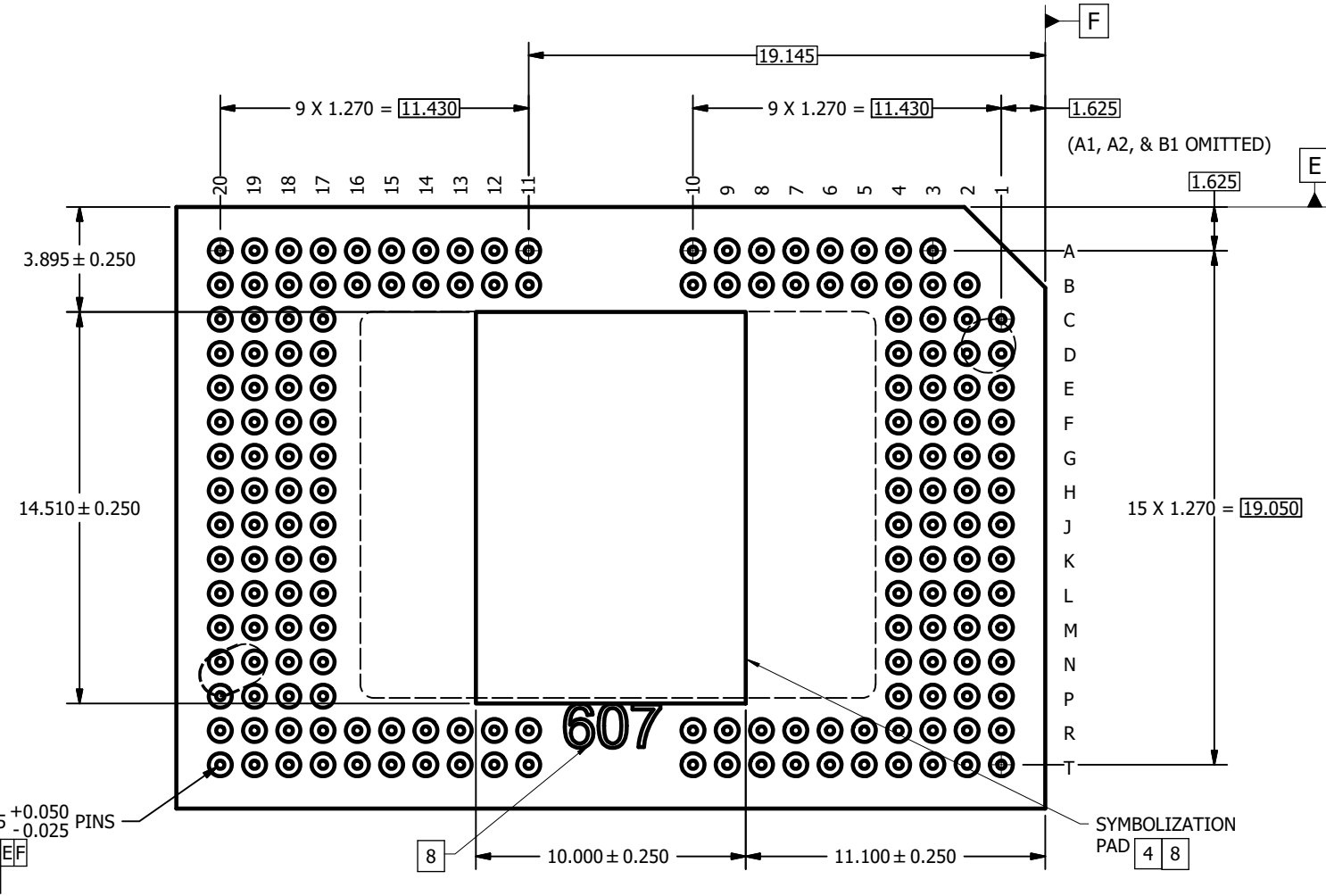
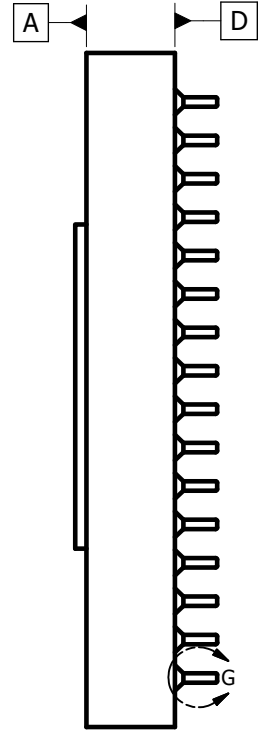
5

4

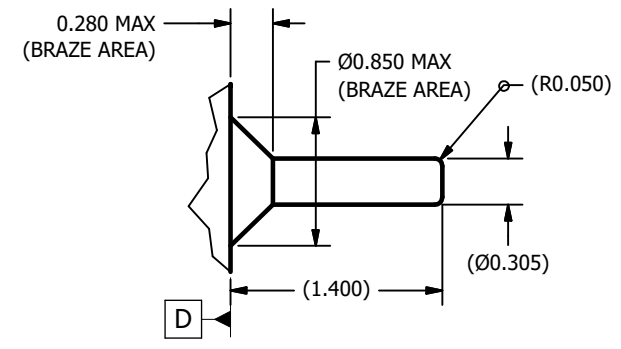
3

2

1



VIEW F  
PINS AND SYMBOLIZATION PAD  
SCALE 8 : 1



DETAIL G  
PIN AND BRAZE DIMENSIONS  
173 PLACES  
SCALE 40 : 1

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