



## DIRECTPATH™ STEREO LINE DRIVER, ADJUSTABLE GAIN

Check for Samples: [DRV601](#)

### FEATURES

- External Gain Setting Resistors
- Space Saving Package
  - 20-Pin, 4 mm × 4 mm Thin QFN, Thermally Optimized PowerPAD™ Package
- Ground-Referenced Outputs Eliminate DC-Blocking Capacitor
  - Reduce Board Area
  - Reduce Component Cost
  - Improve THD+N Performance
  - No Degradation of Low-Frequency Response Due to Output Capacitors
- Wide Power Supply Range: 1.8 V to 4.5 V
- 2 Vrms/Ch Output Voltage into 600 Ω at 3.3 V supply

- Independent Right and Left Channel Shutdown Control
- Short-Circuit and Thermal Protection
- Pop Reduction Circuitry

### APPLICATIONS

- Set-Top Boxes
- CD / DVD Players
- DVD-Receivers
- HTIB
- PDP / LCD TV's

### DESCRIPTION

The DRV601 is a stereo line driver designed to allow the removal of the output dc-blocking capacitors for reduced component count and cost. The device is ideal for single supply electronics where size and cost are critical design parameters.

The DRV601 is capable of driving 2 Vrms into a 600-Ω load at 3.3 V. The device has external gain setting resistors, that support a gain range of -1V/V to -10V/V, and line outputs that has ±8-kV IEC ESD protection. The device has independent shutdown control for the right and left audio channels.

The DRV601 is available in a 4 mm × 4 mm Thin QFN package.

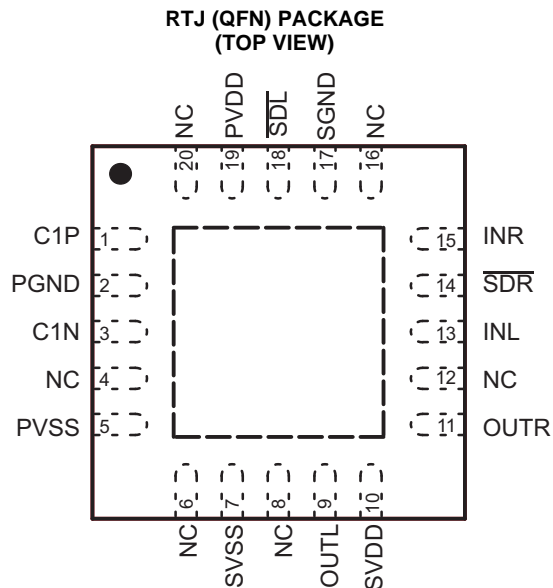


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



NC – No internal connection

**TERMINAL FUNCTIONS**

TERMINAL		I/O	DESCRIPTION
NAME	QFN		
C1P	1	I/O	Charge pump flying capacitor positive terminal
PGND	2	I	Power ground, connect to ground.
C1N	3	I/O	Charge pump flying capacitor negative terminal
NC	4, 6, 8, 12, 16, 20		No connection
PVSS	5	O	Output from charge pump.
SVSS	7	I	Amplifier negative supply, connect to PVSS via star connection.
OUTL	9	O	Left audio channel output signal
SVDD	10	I	Amplifier positive supply, connect to PVDD via star connection.
OUTR	11	O	Right audio channel output signal
INL	13	I	Left audio channel input signal
$\overline{\text{SDR}}$	14	I	Right channel shutdown, active low logic.
INR	15	I	Right audio channel input signal
SGND	17	I	Signal ground, connect to ground.
$\overline{\text{SDL}}$	18	I	Left channel shutdown, active low logic.
PVDD	19	I	Supply voltage, connect to positive supply.
Exposed Pad			Exposed pad must be soldered to a floating plane. Do NOT connect to power or ground.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

		VALUE / UNIT
	Supply voltage, AVDD, PVDD	-0.3 V to 5.5 V
$V_I$	Input voltage	$V_{SS} - 0.3 \text{ V}$ to $V_{DD} + 0.3 \text{ V}$
$R_{(\text{Load})}$	Minimum load impedance	$\geq 100 \Omega$
$T_A$	Operating free-air temperature range	$-40^\circ\text{C}$ to $85^\circ\text{C}$
$T_J$	Operating junction temperature range	$0^\circ\text{C}$ to $150^\circ\text{C}$
$T_{\text{stg}}$	Storage temperature range	$-65^\circ\text{C}$ to $85^\circ\text{C}$

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## AVAILABLE OPTIONS

$T_A$	PACKAGED DEVICES <sup>(1)</sup>	PART NUMBER	SYMBOL
$-40^\circ\text{C}$ to $85^\circ\text{C}$	20-pin, 4 mm x 4 mm QFN	DRV601RTJ <sup>(2)</sup>	AKQ

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).
- (2) The RTJ package is only available taped and reeled. To order, add the suffix "R" to the end of the part number for a reel of 3000, or add the suffix "T" to the end of the part number for a reel of 250 (e.g., DRV601RTJR).

## RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
$V_{SS}$	Supply voltage, AVDD, PVDD	1.8	4.5 <sup>(1)</sup>	V
$V_{IH}$	High-level input voltage	$\overline{\text{SDL}}, \overline{\text{SDR}}$	1.5	V
$V_{IL}$	Low-level input voltage	$\overline{\text{SDL}}, \overline{\text{SDR}}$	0.5	V
$T_A$	Operating free-air temperature	-40	85	$^\circ\text{C}$

- (1) Device can shut down for  $V_{DD} > 4.5 \text{ V}$  to prevent damage to the device.

## ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$  (unless otherwise noted)

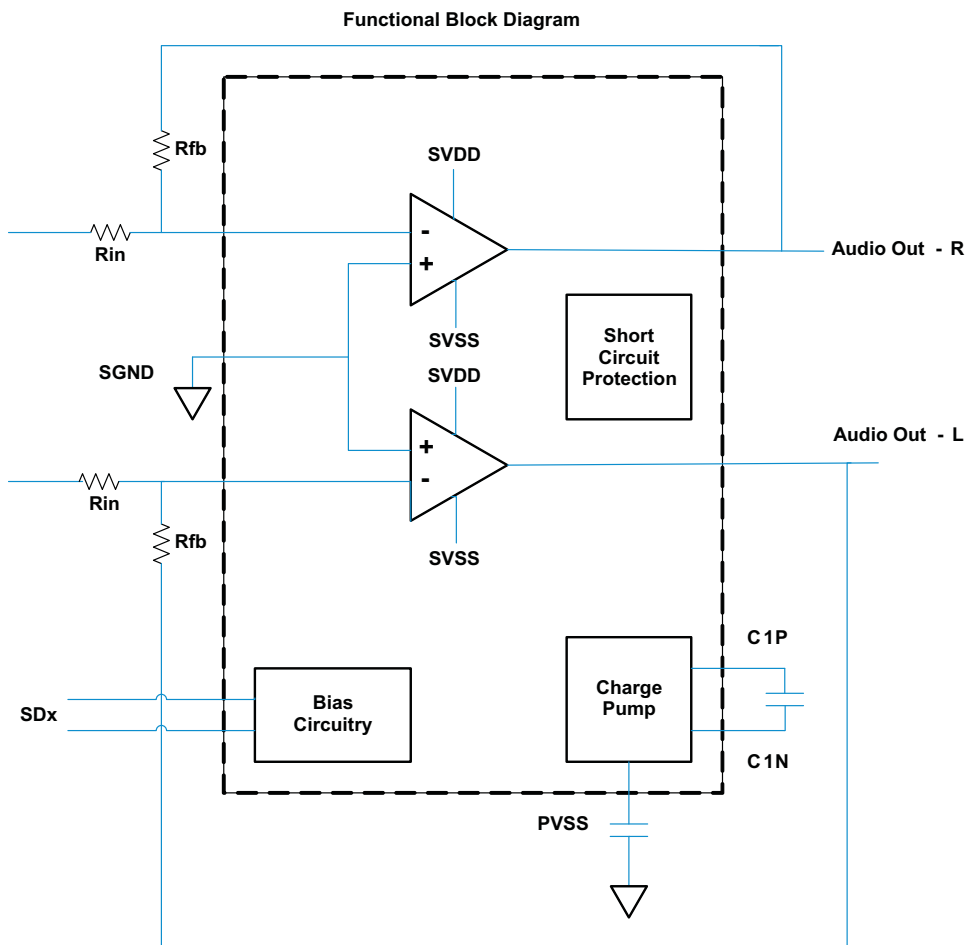
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$ V_{OS} $	Output offset voltage			8	mV
PSRR	Power Supply Rejection Ratio		88		dB
$V_{OH}$	High-level output voltage	3.10			V
$V_{OL}$	Low-level output voltage			-3.05	V
$ I_{IH} $	High-level input current ( $\overline{\text{SDL}}, \overline{\text{SDR}}$ )			1	$\mu\text{A}$
$ I_{IL} $	Low-level input current ( $\overline{\text{SDL}}, \overline{\text{SDR}}$ )			1	$\mu\text{A}$
$I_{DD}$	Supply Current	$V_{DD} = 1.8 \text{ V}$ , No load, $\overline{\text{SDL}} = \overline{\text{SDR}} = V_{DD}$	5.3		mA
		$V_{DD} = 3.3 \text{ V}$ , No load, $\overline{\text{SDL}} = \overline{\text{SDR}} = V_{DD}$	7.1		
		$V_{DD} = 4.5 \text{ V}$ , No load, $\overline{\text{SDL}} = \overline{\text{SDR}} = V_{DD}$	8.7		
		Shutdown mode, $V_{DD} = 1.8 \text{ V}$ to $4.5 \text{ V}$		1	$\mu\text{A}$

## OPERATING CHARACTERISTICS

$V_{DD} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $R_L = 600\ \Omega$ ,  $C_{(PUMP)} = C_{(PVSS)} = 1\ \mu\text{F}$ ,  $C_{IN} = 1\ \mu\text{F}$ ,  $R_{in} = 10\ \text{k}\Omega$ ,  $R_{fb} = 20\ \text{k}\Omega$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_O$	Output Voltage(Outputs In Phase)	THD = 1%, $V_{DD} = 3.3\text{ V}$ , $f = 1\ \text{kHz}$		2.1		$V_{RMS}$
		THD = 1%, $V_{DD} = 4.5\text{ V}$ , $f = 1\ \text{kHz}$		2.7		
		THD = 1%, $V_{DD} = 4.5\text{ V}$ , $f = 1\ \text{kHz}$ , $R_L = 100\ \text{k}\Omega$		2.8		
THD+N	Total harmonic distortion plus noise	$V_O = 2\text{ V}_{rms}$ , $f = 1\ \text{kHz}$		0.008%		
		$V_O = 2\text{ V}_{rms}$ , $f = 6.67\ \text{kHz}$		0.030%		
	Crosstalk	$V_O = 2\text{ V}_{rms}$ , $f = 1\ \text{kHz}$		-80		dB
$A_{vo}$	Open-loop voltage gain			155		dB
$R_{in}$	Input resistor range		1	10	47	k $\Omega$
$R_{fb}$	Feedback resistor range		4.7	20	100	k $\Omega$
	Slew rate			2.2		V/ $\mu\text{s}$
	Maximum capacitive load			300		pF
$V_n$	Noise output voltage	22-kHz filter, A-weighted		10		$\mu\text{V}_{rms}$
ESD	Electrostatic discharge	OUTR, OUTL		$\pm 8$		kV
$f_{osc}$	Charge pump switching frequency		225	450	690	kHz
	Start-up time from shutdown			450		$\mu\text{s}$
	Input impedance		1			M $\Omega$
SNR	Signal-to-noise ratio	$V_O = 2\text{ V}_{rms}$ (THD+N = 0.1%), 22-kHz BW, A-weighted		105		dB
$G_{(bw)}$	Unity Gain Bandwidth			3.5		MHz
	Thermal shutdown	Threshold	150		170	$^\circ\text{C}$
		Hysteresis		15		$^\circ\text{C}$

### Functional Block Diagram



**TYPICAL CHARACTERISTICS**

$C_{(PUMP)} = C_{(PVSS)} = 1 \mu F$ ,  $C_{IN} = 1 \mu F$ ,  $R_{in} = 10 \text{ k}\Omega$ ,  $R_{fb} = 20 \text{ k}\Omega$  (unless otherwise noted)

**Table of Graphs**

		FIGURE
Total harmonic distortion + noise	vs Output Voltage	1-6
Total harmonic distortion + noise	vs Frequency	7-8
Quiescent supply current	vs Supply voltage	9
Output spectrum		10
Gain and phase	vs Frequency	11-12

**TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE**

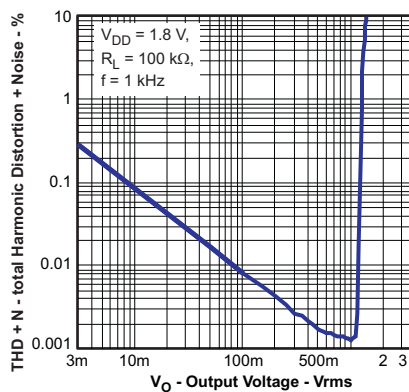


Figure 1.

**TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE**

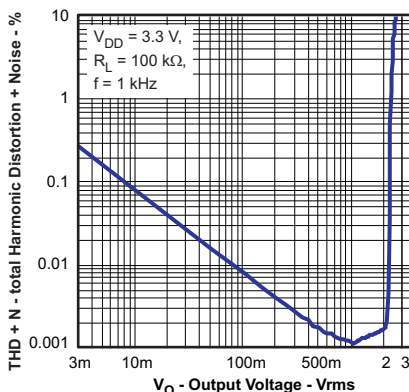


Figure 2.

**TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE**

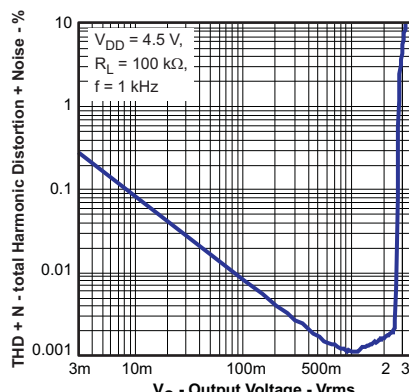


Figure 3.

**TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE**

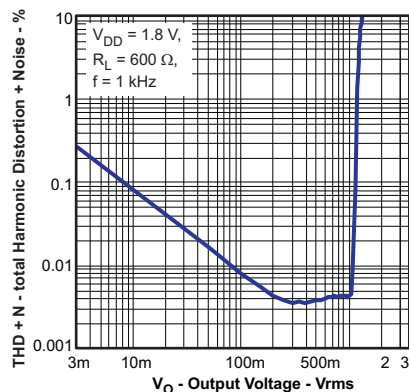


Figure 4.

**TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE**

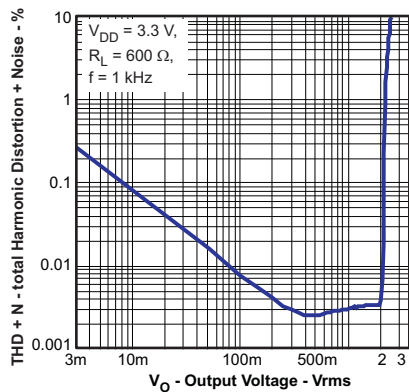


Figure 5.

**TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE**

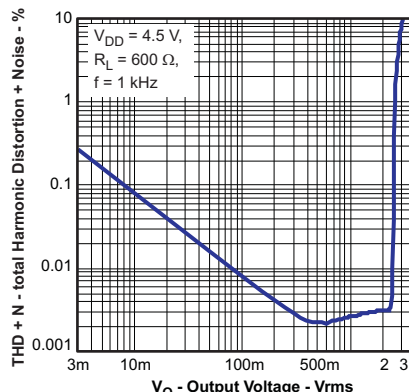


Figure 6.

**TOTAL HARMONIC DISTORTION + NOISE  
VS  
FREQUENCY**

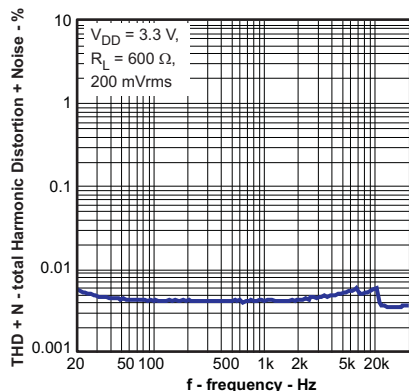


Figure 7.

**TOTAL HARMONIC DISTORTION + NOISE  
VS  
FREQUENCY**

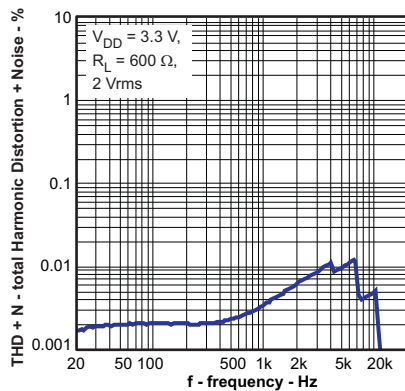


Figure 8.

**QUIESCENT SUPPLY CURRENT  
VS  
SUPPLY VOLTAGE**

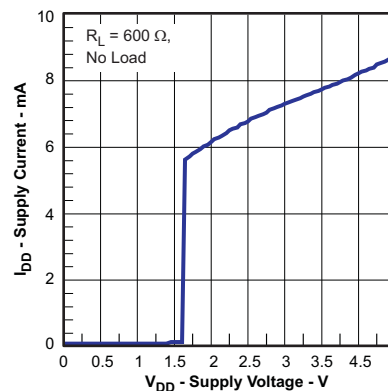


Figure 9.

**FFT  
VS  
FREQUENCY**

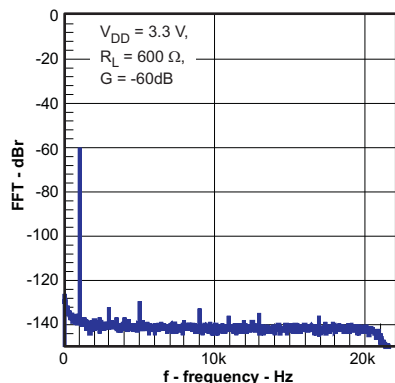


Figure 10.

**GAIN  
VS  
FREQUENCY**

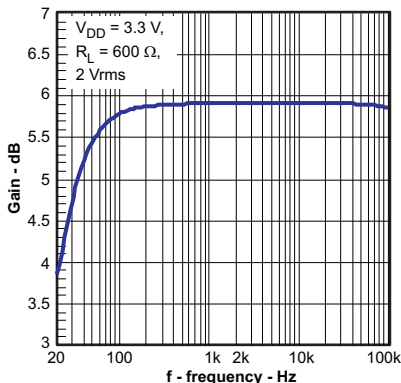


Figure 11.

**PHASE  
VS  
FREQUENCY**

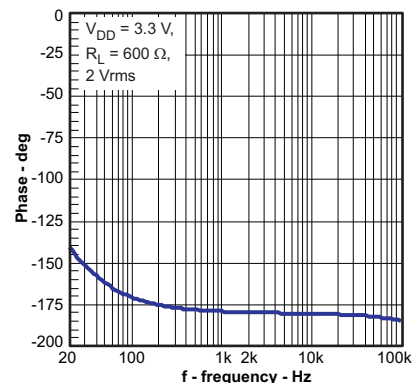


Figure 12.

## APPLICATION INFORMATION

### Line Driver Amplifiers

Single-supply Line Driver amplifiers typically require dc-blocking capacitors. The top drawing in [Figure 13](#) illustrates the conventional Line Driver amplifier connection to the load and output signal.

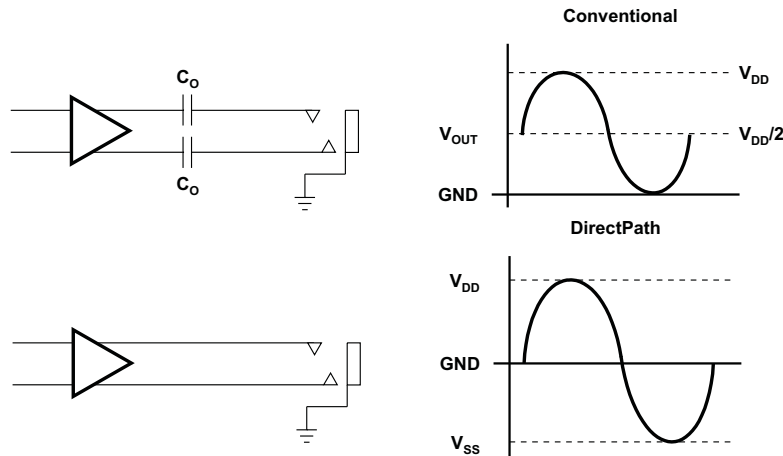
DC blocking capacitors are often large in value. The line load (typical resistive values of 600  $\Omega$  to 10 k $\Omega$ ) combine with the dc blocking capacitors to form a high-pass filter. [Equation 1](#) shows the relationship between the load impedance ( $R_L$ ), the capacitor ( $C_O$ ), and the cutoff frequency ( $f_c$ ).

$$f_c = \frac{1}{2\pi R_L C_O} \quad (1)$$

$C_O$  can be determined using [Equation 2](#), where the load impedance and the cutoff frequency are known.

$$C_O = \frac{1}{2\pi R_L f_c} \quad (2)$$

If  $f_c$  is low, the capacitor must then have a large value because the load resistance is small. Large capacitance values require large package sizes. Large package sizes consume PCB area, stand high above the PCB, increase cost of assembly, and can reduce the fidelity of the audio output signal.



**Figure 13. Amplifier Applications**

The DirectPath™ amplifier architecture operates from a single supply but makes use of an internal charge pump to provide a negative voltage rail. Combining the user provided positive rail and the negative rail generated by the IC, the device operates in what is effectively a split supply mode. The output voltages are now centered at zero volts with the capability to swing to the positive rail or negative rail. The DirectPath™ amplifier requires no output dc blocking capacitors. The bottom block diagram and waveform of [Figure 13](#) illustrate the ground-referenced Line Driver architecture. This is the architecture of the DRV601.



## Charge Pump Flying Capacitor and PVSS Capacitor

The charge pump flying capacitor serves to transfer charge during the generation of the negative supply voltage. The PVSS capacitor must be at least equal to the charge pump capacitor in order to allow maximum charge transfer. Low ESR capacitors are an ideal selection, and a value of 1 $\mu$ F is typical. Capacitor values that are smaller than 1 $\mu$ F can be used, but the maximum output voltage may be reduced and the device may not operate to specifications.

## Decoupling Capacitors

The DRV601 is a DirectPath™ Line Driver amplifier that require adequate power supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. A good low equivalent-series-resistance (ESR) ceramic capacitor, typically 2.2 $\mu$ F, placed as close as possible to the device  $V_{DD}$  lead works best. Placing this decoupling capacitor close to the DRV601 is important for the performance of the amplifier. For filtering lower frequency noise signals, a 10- $\mu$ F or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

## Gain setting resistors ranges

The gain setting resistors,  $R_{in}$  and  $R_{fb}$ , must be chosen so that noise, stability and input capacitor size of the DRV601 is kept within acceptable limits. Voltage gain is defined as  $R_{fb}$  divided by  $R_{in}$ .

Selecting values that are too low demands a large input ac-coupling capacitor,  $C_{IN}$ . Selecting values that are too high increases the noise of the amplifier. [Table 1](#) lists the recommended resistor values for different gain settings.

**Table 1. Recommended Resistor Values**

Gain	Input Resistor Value, $R_{in}$	Feedback Resistor Value, $R_{fb}$
-1 V/V	10 k $\Omega$	10 k $\Omega$
-1.5 V/V	10 k $\Omega$	15 k $\Omega$
-2 V/V	10 k $\Omega$	20 k $\Omega$
-10 V/V	4,7 k $\Omega$	47 k $\Omega$

## Input-Blocking Capacitors

DC input-blocking capacitors are required to be added in series with the audio signal into the input pins of the DRV601. These capacitors block the DC portion of the audio source and allow the DRV601 inputs to be properly biased to provide maximum performance.

These capacitors form a high-pass filter with the input resistor,  $R_{in}$ . The cutoff frequency is calculated using [Equation 3](#). For this calculation, the capacitance used is the input-blocking capacitor and the resistance is the input resistor chosen from the gain table above, then the frequency and/or capacitance can be determined when one of the two values are given.

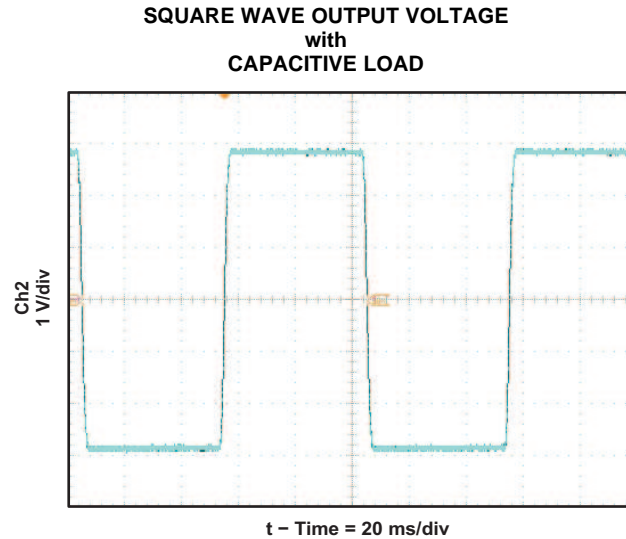
$$f_{C_{IN}} = \frac{1}{2\pi R_{IN} C_{IN}} \quad \text{or} \quad C_{IN} = \frac{1}{2\pi f_{C_{IN}} R_{IN}} \quad (3)$$

## Supply Voltage Limiting At 4.5 V

The DRV601 have a built-in charge pump which serves to generate a negative rail for the line driver. Because the line driver operates from a positive voltage and negative voltage supply, circuitry has been implemented to protect the devices in the amplifier from an overvoltage condition. Once the supply is above 4.5 V, the DRV601 can shut down in an overvoltage protection mode to prevent damage to the device. The DRV601 resume normal operation once the supply is reduced to 4.5 V or lower.

## Capacitive load

The DRV601 has the ability to drive a high capacitive load up to 330pF directly, higher capacitive loads can be accepted by adding a series resistor of 10 $\Omega$  or larger. The figure below shows a 10kHz signal into a 470pF capacitor using the 10R series resistor.

**Figure 14.**

### Layout Recommendations

A proposed layout for the DRV601 can be seen in the DRV601EVM user's guide, [SLOU215](#), and the Gerber files can be downloaded on [www.ti.com](http://www.ti.com), open the DRV601 product folder and look in the Tools & Software folder.

### Exposed Pad On DRV601RTJ Package

The exposed metal pad on the DRV601RTJ package must be soldered down to a pad on the PCB in order to maintain reliability. *The pad on the PCB should be allowed to float and not be connected to ground or power.* Connecting this pad to power or ground prevents the device from working properly because it is connected internally to PVSS.

### SGND and PGND Connections

The SGND and PGND pins of the DRV601 must be routed back to the decoupling capacitor separately in order to provide proper device operation. If the SGND and PGND pins are connected directly to each other, the part functions without risk of failure, but the noise and THD performance do not meet the specifications.

### Gain setting resistors

The gain setting resistors,  $R_{in}$  and  $R_{fb}$ , must be placed close to pin 13 respectively pin 17 to minimize the capacitive loading on these input pins and to ensure maximum stability of the DRV601. For the recommended PCB layout, see the DRV601EVM user guide.

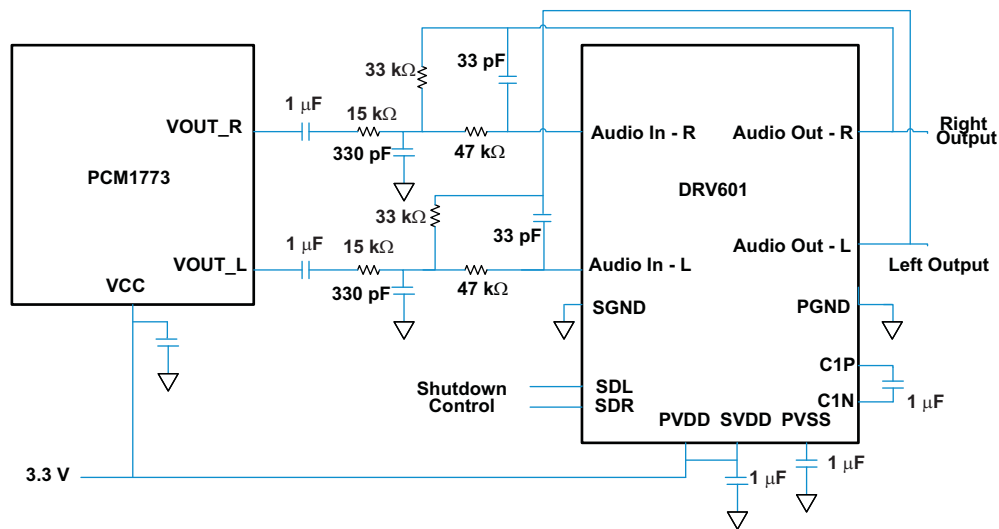


Figure 15. Application Circuit

REVISION HISTORY

Changes from Original (January 2008) to Revision A	Page
<ul style="list-style-type: none"> <li>Changed <math>T_A</math> From: -40°C to 85°C To: 0°C to 70°C (AVAILABLE OPTIONS table) .....</li> </ul>	3
Changes from Revision A (August 2008) to Revision B	Page
<ul style="list-style-type: none"> <li>Changed <math>T_A</math> From: 0°C to 70°C To: -40°C to 85°C (ABSOLUTE MAXIMUM RATING table) .....</li> <li>Changed <math>T_A</math> From: 0°C to 70°C To: -40°C to 85°C (AVAILABLE OPTIONS table) .....</li> <li>Changed <math>T_A</math> From: 0°C to 70°C To: -40°C to 85°C (RECOMMENDED OPERATING CONDITIONS table) .....</li> </ul>	3
Changes from Revision B (Novemembr 2008) to Revision C	Page
<ul style="list-style-type: none"> <li>Changed values - Charge pump switching frequency. From: Min = 280 Typ = 320 Max = 420 To: Min = 225 Typ = 450 Max = 690 .....</li> </ul>	4

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">DRV601RTJR</a>	Active	Production	QFN (RTJ)   20	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV601
DRV601RTJR.A	Active	Production	QFN (RTJ)   20	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV601
DRV601RTJRG4	Active	Production	QFN (RTJ)   20	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV601
<a href="#">DRV601RTJT</a>	Active	Production	QFN (RTJ)   20	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV601
DRV601RTJT.A	Active	Production	QFN (RTJ)   20	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV601

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV601RTJR	QFN	RTJ	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
DRV601RTJT	QFN	RTJ	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV601RTJR	QFN	RTJ	20	3000	353.0	353.0	32.0
DRV601RTJT	QFN	RTJ	20	250	213.0	191.0	35.0

## GENERIC PACKAGE VIEW

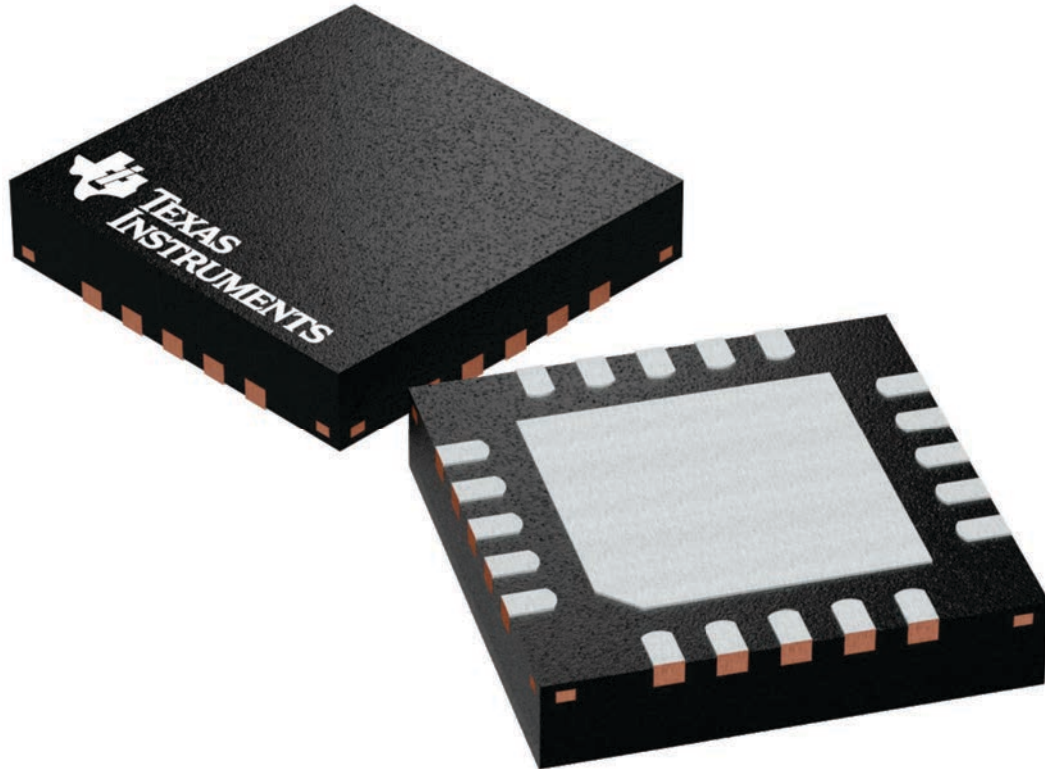
**RTJ 20**

**WQFN - 0.8 mm max height**

4 x 4, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD


This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224842/A

# DATA BOOK PACKAGE OUTLINE

LEADFRAME EXAMPLE
4222370

DRAFTSMAN: H. DENG	DATE: 09/12/2016		DIMENSIONS IN MILLIMETERS								
DESIGNER: H. DENG	DATE: 09/12/2016	 <b>TEXAS INSTRUMENTS</b> SEMICONDUCTOR OPERATIONS	CODE IDENTITY NUMBER 01295								
CHECKER: V. PAKU & T. LEQUANG	DATE: 09/12/2016		<b>ePOD, RTJ0020D / WQFN, 20 PIN, 0.5 MM PITCH</b>								
ENGINEER: T. TANG	DATE: 09/12/2016										
APPROVED: E. REY & D. CHIN	DATE: 10/06/2016										
RELEASED: WDM	DATE: 10/24/2016										
TEMPLATE INFO: EDGE# 4218519	DATE: 04/07/2016	<table border="1" style="display: inline-table; border-collapse: collapse;"> <tr> <td style="padding: 2px;">SCALE</td> <td style="padding: 2px;">SIZE</td> </tr> <tr> <td style="text-align: center;">15X</td> <td style="text-align: center;">A</td> </tr> </table>	SCALE	SIZE	15X	A	<table border="1" style="display: inline-table; border-collapse: collapse;"> <tr> <td style="padding: 2px;">REV</td> <td style="padding: 2px;">PAGE</td> </tr> <tr> <td style="text-align: center;">A</td> <td style="text-align: center;">1 OF 5</td> </tr> </table>	REV	PAGE	A	1 OF 5
SCALE	SIZE										
15X	A										
REV	PAGE										
A	1 OF 5										

4219125

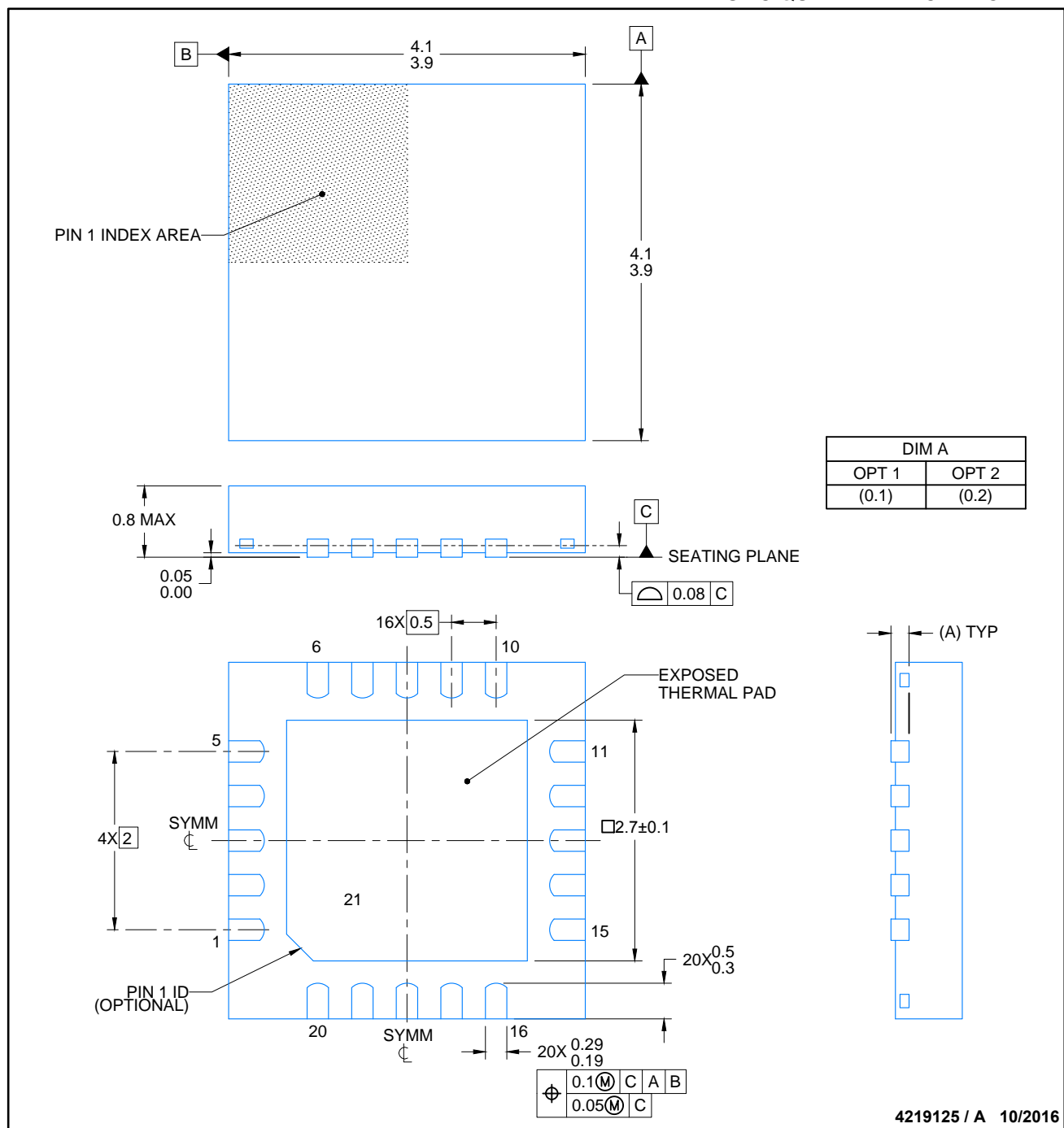


# RTJ0020D

# PACKAGE OUTLINE

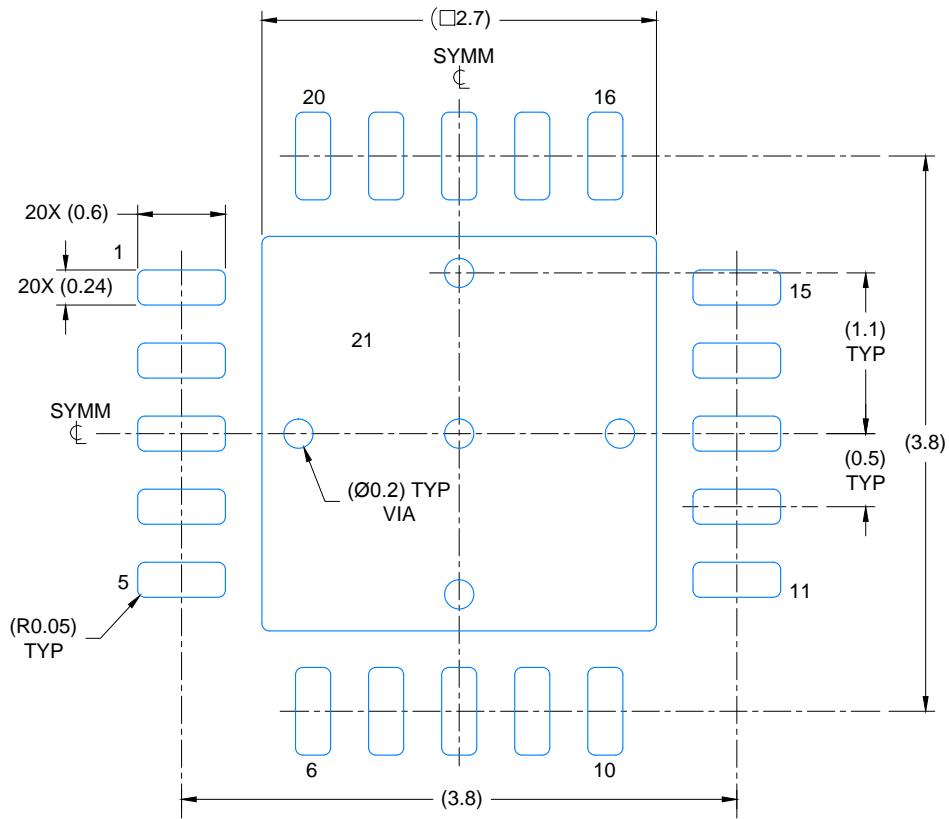
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

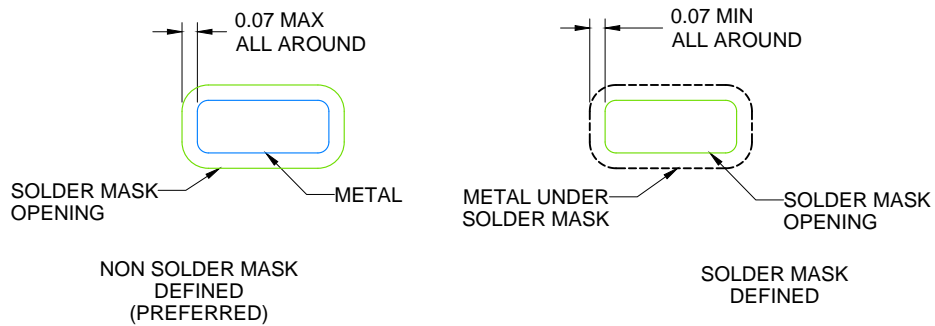


**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE  
SCALE: 20X

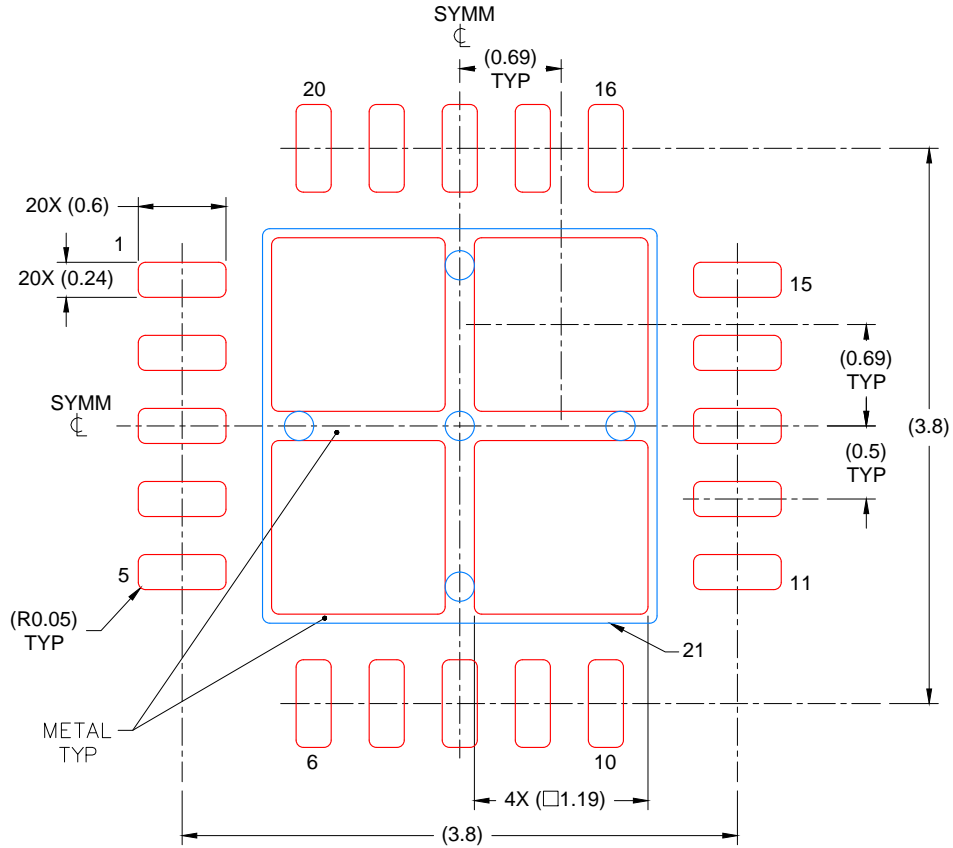


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
78% PRINTED COVERAGE BY AREA  
SCALE: 20X

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NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

# REVISIONS

REV	DESCRIPTION	ECR	DATE	ENGINEER / DRAFTSMAN
A	RELEASE NEW DRAWING	2160736	10/24/2016	T. TANG / H. DENG

Blank area for drawing content.

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