DRV81646: 65V Four-Channel Low-side Driver with Hardware, SPI, and Configurable Slew Rate and Cut-off Duration

1 Features

- Four-channel integrated low-side switches
  - **140mΩ $R_{DS(ON)}$** at 25°C
  - Operating supply voltage range: **4.5V** to **65V (70V absolute maximum)**
  - Selectable current limit from **0.5A** up to **4A** per channel
  - Fast PWM switching up to **500kHz**
- Flexible interface options:
  - **Hardware** interface with independent channel PWM input
  - **SPI** enables reduction in GPIO and isolation overhead for high channel count designs
- **Integrated catch diodes** for flexible decay modes with optional external TVS/Zener diode as alternate current path on switch turnoff
- **Slew rate** configurable (100ns – 1500ns) enables both slow/fast switching applications
- Diagnostic feedback
  - MCU fault interrupt signal **(nFAULT)**
  - **Per channel fault report** available through SPI
- Protection Features
  - User settable **current limit**
  - Independent **overtemperature** and **overcurrent** protection for each channel
  - Configurable overcurrent **cut-off delay** (COD) 0.5ms-2ms

2 Applications

- PLC
- Distributed I/O
- Field Devices
- General relay and solenoid drive
- Textile machines

3 Description

The DRV81646 is a four-channel low-side switch driver that operates from 4.5V to 65V and supports a wide range of load currents. The device integrates four low-side switches with a $R_{DS(ON)}$ of 140mΩ, each with a freewheeling diode to the VCLAMP pin. This feature allows the user to either recirculate current or connect an external TVS for inductive load turn-off.

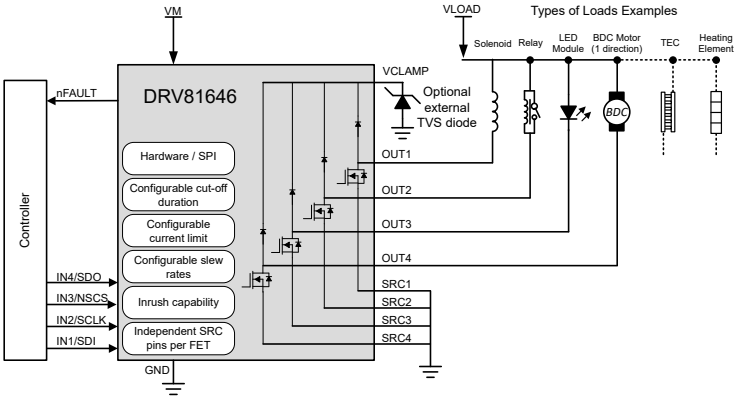
The device can be controlled through a hardware GPIO interface or standard 4-wire SPI. Each channel features individual overtemperature protection, and an analog current limit adjustable with an external resistor on the ILIM pin. There is an optional cut-off delay (COD) configuration which limits the duration of a current-limiting condition on the respective channel, helping to prevent damage to the device or the load. The output slew rates are configurable by setting a resistor on the RSLEW/CNTL pin, providing further flexibility in the control of the output switches. The device has an INRUSH mode boosting the current limit threshold for capacitive loads.

The DRV81646 provides a fault output pin (nFAULT) to indicate fault conditions, and per-channel fault status can be monitored in SPI mode. This feature allows the user to quickly identify and respond to any faults that occur.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
DRV81646PWPR	PWP (HTSSOP, 20)	6.50mm × 6.40mm
DRV81646DGQR	DGQ (HVSSOP, 24)	7.10mm × 4.90mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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4 Pin Configuration and Functions

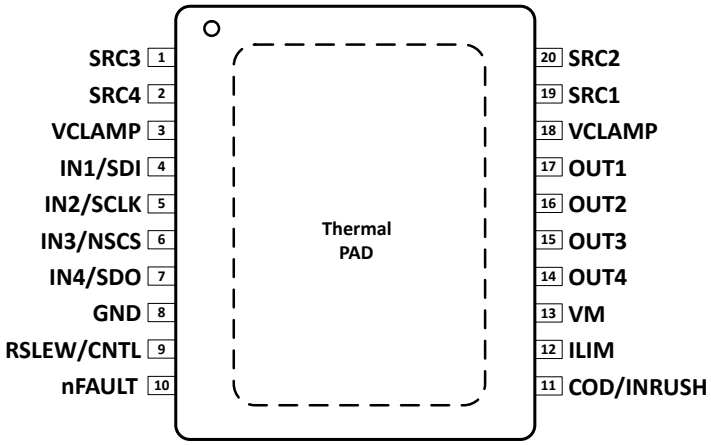


Figure 4-1. 20-Pin PWP Package, HTSSOP (Top View)

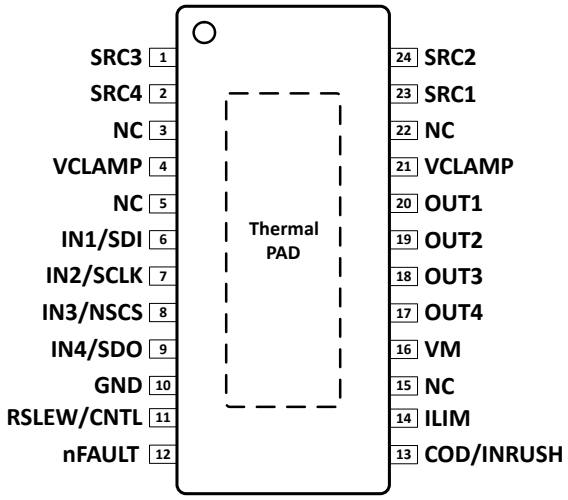


Figure 4-2. 24-Pin DGQ Package, HVSSOP (Top View)

Table 4-1. Pin Functions

PIN			TYPE[1]	DESCRIPTION
NAME	PWP (20)	DGQ (24)		
POWER AND GROUND				
VM	13	16	PWR	Power supply. Bypass this pin to the GND pin with a 0.1µF ceramic capacitor as well as sufficient bulk capacitance rated for VM.
VCLAMP	3, 18	4, 21	PWR	Connect to VM supply, or zener diode to VM supply or GND. Do not leave this pin unconnected.
GND	8	10	GND	Device ground. Connect to system ground.
SRC1	19	23	GND	Source terminal of channel 1 low side FET. Connect to system ground or optional sense resistor to system ground for external current sense
SRC2	20	24	GND	Source terminal of channel 2 low side FET. Connect to system ground or optional sense resistor to system ground for external current sense
SRC3	1	1	GND	Source terminal of channel 3 low side FET. Connect to system ground or optional sense resistor to system ground for external current sense
SRC4	2	2	GND	Source terminal of channel 4 low side FET. Connect to system ground or optional sense resistor to system ground for external current sense
THERMAL PAD	—	—	—	Thermal Pad. Connect to system ground. Connect to a continuous ground pour copper plane with direct-connect vias for the best thermal dissipation.
NC	—	3, 5, 15, 22	—	
CONTROL				
ILIM	12	14	I	Current limit input. Connect a resistor between ILIM and GND to set the current limit threshold. For details see Section 6.3.4.1. Do not leave this pin unconnected. Connect directly to GND for the maximum current limit setting.
RSLEW/CNTL	9	11	I	Slew Rate and Control Interface selection input. Connect a resistor to GND for desired combination of slew rate and control interface setting. For details, see Section 6.3.1.

Table 4-1. Pin Functions (continued)

PIN			TYPE[1]	DESCRIPTION
NAME	PWP (20)	DGQ (24)		
COD/INRUSH	11	13	I	Device configuration pin for Cutoff Delay or Inrush mode. Connect to an appropriate resistor to GND to set the corresponding cut off delay. Connect to GND to disable this feature. Leave unconnected (Hi-Z) for INRUSH mode
IN1/SDI	4	6	I	With **Hardware** mode, this pin controls the output of channel 1. If this channel is not used, tie the pin to GND directly or with a 10kΩ With **SPI** mode, this pin is serial data input. Pin has internal pull-down resistor.
IN2/SCLK	5	7	I	With **Hardware** mode, this pin controls the output of channel 2. If this channel is not used, tie the pin to GND directly or with a 10kΩ With **SPI** mode, this pin is serial clock input. Serial data is shifted out on the rising edge of this pin, and captured on the falling edge of this pin. Pin has internal pull-down resistor.
IN3/NSCS	6	8	I	With **Hardware** mode, this pin controls the output of channel 3. If this channel is not used, tie the pin to GND directly or with a 10kΩ With **SPI** mode, this pin is serial chip select. An active low on this pin enables the serial interface communications. Pin has internal pull-down resistor.
IN4/SDO	7	9	I/O	With **Hardware** mode, this pin controls the output of channel 4. If this channel is not used, tie the pin to GND directly or with a 10kΩ. In Hardware mode this pin has an internal pulldown resistor. With **SPI** mode, this pin is serial data output. Data is shifted out on the rising edge of the SCLK pin. In SPI mode this pin is an open drain output and requires an external pull-up resistor.
nFAULT	10	12	O	Open drain output. Connect pull-up resistor to external logic supply. Logic low when in fault condition.
OUTPUT				
OUT1	17	20	O	Connect to load 1
OUT2	16	19	O	Connect to load 2
OUT3	15	18	O	Connect to load 3
OUT4	14	17	O	Connect to load 4

(1) I = input, O = output, PWR = power, GND = ground

5 Specification

5.1 Absolute Maximum Ratings

Over operating temperature range (unless otherwise noted)(1)

	PIN	MIN	MAX	UNIT
Power supply voltage	VM	–0.3	70	V
Output voltage	OUTx	–0.3	VCLAMP+0.3	V
Peak output current	OUTx		Internally limited	A
Clamp voltage	VCLAMP	–0.3	70	V
FET source terminal voltage relative to GND (steady state)	SRCx	-0.6	0.6	V
Continuous RMS current on VCLAMP (pins 3, 18 tied together)	VCLAMP		8	A
Transient current < 1ms on VCLAMP (pin 3, 18 tied together)	VCLAMP		20	A
Sense resistor between SRCx and board GND	SRCx		300	mΩ
OUTx FET recirculation diode current RMS or continuous	OUTx FET body diode		5	A
Digital input pin voltage	ILIM, RSLEW/CNTL, COD/INRUSH, INx	–0.5	5.5	V
Digital output current	nFAULT, SDO		10	mA
Digital output pin voltage	nFAULT, SDO	–0.5	7	V
Operating virtual junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–60	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Over operating temperature range (unless otherwise noted)

				MIN	NOM	MAX	UNIT
V_M	Power supply voltage			4.5		65	V
V_{CLAMP}	Output clamp voltage					65	V
I_{OUT}	Continuous output current (each channel)	PWP package, T_A = 25°C(1)	1 channel on			3.7	A
			4 channels on			2.7	A
		DGQ package, T_A = 25°C(1)	1 channel on			3.4	A
			4 channels on			2.5	A
T_{AMB}	Operating Ambient temperature			-40		125	°C
T_J	Operating junction temperature			-40		150	°C

(1) See Continuous Current Capability for ratings across temperature

5.4 Thermal Information

THERMAL METRIC[1]		DRV81646		UNIT
		PWP (HTSSOP)	DGQ (HVSSOP)	
		20 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.6	32.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.5	33.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.6	8.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.8	1.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	10.5	8.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.7	1.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

4.5V ≤ V_{VM} ≤ 65V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted), Typical values at 24V, 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_{VM}	VM operating supply current	V_M = 24V, No Switching			3	mA
		V_M = 24V, Output switching at 200kHz			5	mA
V_{UVLO}	VM undervoltage lockout voltage	V_M rising	4.1	4.25	4.45	V
		V_M falling	4.0	4.15	4.35	V
V_{UVLO_HYS}	VM undervoltage lockout hysteresis			100		mV
t_{UVLO}	VM undervoltage deglitch			10		µs
LOGIC-LEVEL INPUTS (INx, nSCS, SCLK, SDI)						
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage		2			V
V_{HYS}	Input hysteresis			0.4		V
I_{IL}	Input low current	V_{IN} = 0	–5		5	µA
I_{IH}	Input high current	V_{IN} = 3.3V		50	100	µA
OPEN-DRAIN OUTPUT (nFAULT, SDO)						
V_{OL}	Output low voltage for nFAULT, SDO	I_O = 5mA			0.1	V
I_{OH}	Output high leakage current for nFAULT, SDO	Pull-up resistor to 5V			1	µA
t_{nFAULT_VALID}	Time after V_{VM} > V_{UVLO} (rising) that nFAULT signal is valid.				30	µs
SEVEN-LEVEL INPUT (RSLEW/CNTL)						
V_{LVL1}	Level 1 of 7	Tied to GND	0		0.1	V
V_{LVL2}	Level 2 of 7	14.7kΩ ±5% to GND	0.2		0.35	V
V_{LVL3}	Level 3 of 7	44.2kΩ ± 5% to GND	0.55		0.8	V
V_{LVL4}	Level 4 of 7	100kΩ ± 5% to GND	1		1.25	V
V_{LVL5}	Level 5 of 7	249kΩ ± 5% to GND	1.5		1.75	V
V_{LVL6}	Level 6 of 7	Hi-Z	2.1		2.4	V
V_{LVL7}	Level 7 of 7	Tied to DVDD (logic voltage)	3		5	V
$I_{RSLEW/CNTL}$	Input current			22.5		µA
SWITCHING						

5.5 Electrical Characteristics (continued)

4.5V ≤ V_{VM} ≤ 65V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted), Typical values at 24V, 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_R	Rise time OUTx rising from 10% to 90% V_M = 24V, R_L = 48Ω, C_L = 0.1nF	V_{LVL1} on RSLEW/CNTL		100	150	ns
		V_{LVL6} or V_{LVL7} on RSLEW/CNTL		300	450	ns
		V_{LVL4} or V_{LVL5} on RSLEW/CNTL		700	1000	ns
		V_{LVL2} or V_{LVL3} on RSLEW/CNTL		1500	2300	ns
t_F	Fall time OUTx falling from 90% to 10% V_M = 24V, R_L = 48Ω, C_L = 0.1nF	V_{LVL1} on RSLEW/CNTL		100	150	ns
		V_{LVL6} or V_{LVL7} on RSLEW/CNTL		300	450	ns
		V_{LVL4} or V_{LVL5} on RSLEW/CNTL		700	1000	ns
		V_{LVL2} or V_{LVL3} on RSLEW/CNTL		1500	2300	ns
t_{PD}	Input to output propagation delay INx rising above V_{IH} to OUTx falling to 90%, or INx falling below V_{IL} to OUTx rising to 10% V_M = 24V; R_L = 48Ω C_L = 0.1nF	V_{LVL1} on RSLEW/CNTL		100	150	ns
		V_{LVL6} or V_{LVL7} on RSLEW/CNTL		250	370	ns
		V_{LVL4} or V_{LVL5} on RSLEW/CNTL		400	600	ns
		V_{LVL2} or V_{LVL3} on RSLEW/CNTL		700	1000	ns
DRIVER OUTPUTS (OUTx)						
$R_{DS(ON)}$	FET on resistance	V_M = 24V, I_O = 500mA, T_J = 25°C		140		mΩ
		V_M = 24V, I_O = 500mA, T_J = 85°C			225	mΩ
I_{OFF}	Off-state leakage current	V_{OUT} = V_M = 24V		0.5		µA
I_{OFF}	Off-state leakage current	V_{OUT} = V_M = 65V			10	µA
V_F	Recirculation Diodes forward voltage	V_{OUT} = 24V, I_O = 500mA			1.2	V
I_{OFF}	Recirculation Diodes reverse leakage current	V_{OUT} = 0V, V_{CLAMP} = 65V			10	µA
PROTECTION CIRCUITS						
I_{LIM}	Current limitation value Follows 60/R_{ILIM}[kΩ] for 30kΩ ≤ R_{ILIM} ≤ 120kΩ	R_{ILIM} short to GND or R_{ILIM} < 20kΩ		3		A
		R_{ILIM} = 30kΩ	1.4	2	2.6	A
		R_{ILIM} = 60kΩ	0.7	1	1.3	A
		R_{ILIM} = 90kΩ	0.4	0.66	0.9	A
		R_{ILIM} = 120kΩ	0.3	0.5	0.7	A
$I_{LIM\_ACTIVATE}$	Current limit activation threshold Follows I_{LIM}+50%	R_{ILIM} = Short to GND		4.7		A
		R_{ILIM} = 30kΩ		3		A
		R_{ILIM} = 60kΩ		1.5		A
		R_{ILIM} = 90kΩ		1		A
		R_{ILIM} = 120kΩ		0.75		A
I_{INRUSH}	Current limitation value during t_{INRUSH} Follows 2*I_{LIM}[kΩ] for R_{ILIM}≥40kΩ	R_{ILIM} = Short to GND		4		A
		R_{ILIM} = 30kΩ		4		A
		R_{ILIM} = 60kΩ	1.4	2	2.6	A
		R_{ILIM} = 90kΩ	0.8	1.2	1.6	A
		R_{ILIM} = 120kΩ	0.6	1	1.4	A
$I_{INRUSH\_ACTIVATE}$	Current limit activation threshold during INRUSH Follows I_{INRUSH}+50%	R_{ILIM} = Short to GND		6.5		A
		R_{ILIM} = 30kΩ		6		A
		R_{ILIM} = 60kΩ		3		A
		R_{ILIM} = 90kΩ		2		A
		R_{ILIM} = 120kΩ		1.5		A
R_{HiZ}	Inrush mode selection.	Pull down resistor on COD/Inrush pin. Value of external resistor above which Inrush Mode is selected.	1			MΩ

5.5 Electrical Characteristics (continued)

4.5V ≤ V_{VM} ≤ 65V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted), Typical values at 24V, 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{COD_DIS}	Cut off Delay disable threshold	Value of external resistor below which Cut off function is disabled			20	kΩ
t_{COD}	Cut off Delay Adjust with external resistor R_{COD} to GND Follows R_{COD}[kΩ]/120 ±15% for 60kΩ ≤ R_{COD} ≤ 240kΩ	R_{COD} = 60kΩ	0.4	0.5	0.6	ms
		R_{COD} = 120kΩ	0.8	1	1.2	ms
		R_{COD} = 180kΩ	1.2	1.5	1.8	ms
		R_{COD} = 240kΩ	1.6	2	2.4	ms
t_{INRUSH}	Inrush Mode duration	COD/INRUSH pin unconnected		10		ms
t_{RETRY}	Overcurrent protection retry time Adjust with external resistor R_{COD} to GND Follows 32*t_{COD} ±15% for 60kΩ ≤ R_{COD} ≤ 240kΩ	R_{COD} = 60kΩ		15.5		ms
		R_{COD} = 120kΩ		31		ms
		R_{COD} = 180kΩ		46.5		ms
		R_{COD} = 240kΩ		62		ms
T_{TSD}	Thermal shutdown temperature	Die temperature	150	170	190	°C
T_{TSD_HYS}	Thermal shutdown temperature hysteresis			40		°C
t_{TSD_DG}	Thermal shutdown deglitch			20		µs

5.6 Timing Requirements

		MIN	NOM	MAX	UNIT
t_{SCLK}	SCLK cycle time	500			ns
t_{SCLKH}	SCLK high time	170			ns
t_{SCLKL}	SCLK low time	170			ns
t_{H_SCLK}	Hold time, nSCS falling to SCLK rising edge	1000			ns
$t_{SU(SDI)}$	Setup time, SDI valid to SCLK falling edge	30			ns
$t_{H(SDI)}$	Hold time, SCLK falling edge to SDI not valid	30			ns
$t_{D(SDO)}$	Delay time, SCLK rising edge to SDO valid (C_{LOAD} < 20pF)			100	ns
t_{SU_NSCS}	Delay between final SCLK falling edge to nSCS rising edge	200			ns
t_{SDOHIZ}	Delay between NSCS rising edge and SDO HiZ			100	ns
t_{NSCS_H}	Pulse width for nSCS	1000			ns
t_{D_LATCH}	nSCS rising edge to input data latched in device			2000	ns

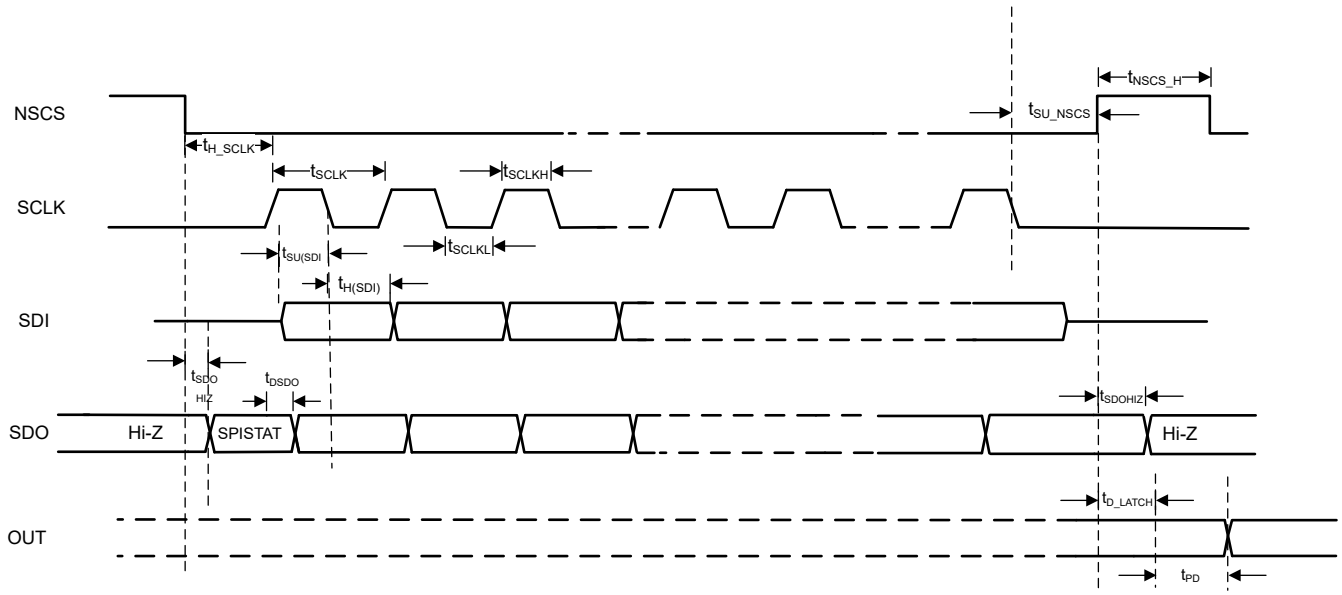


Figure 5-1. SPI Timing Parameters

5.7 Typical Characteristics

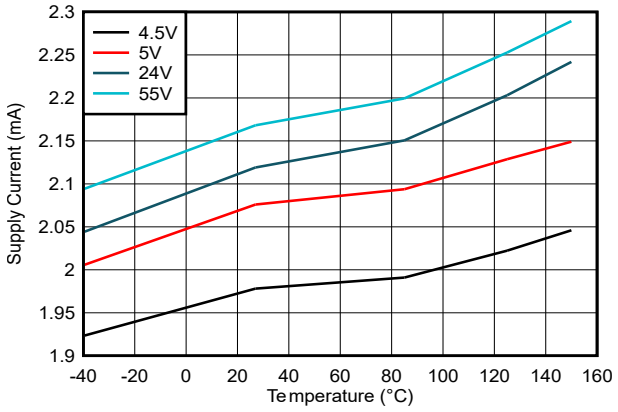


Figure 5-2. Supply Current Over Temperature

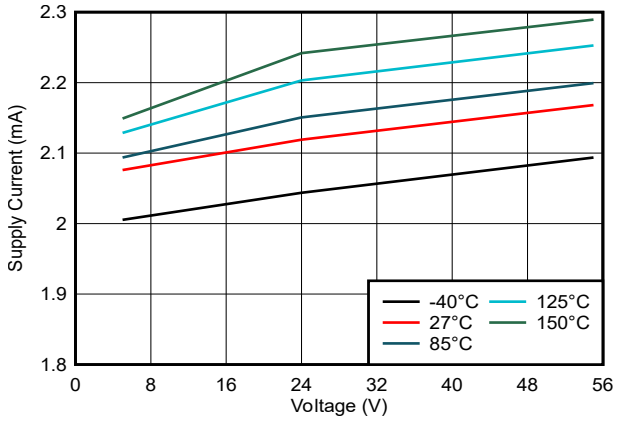


Figure 5-3. Supply Current Over V_M

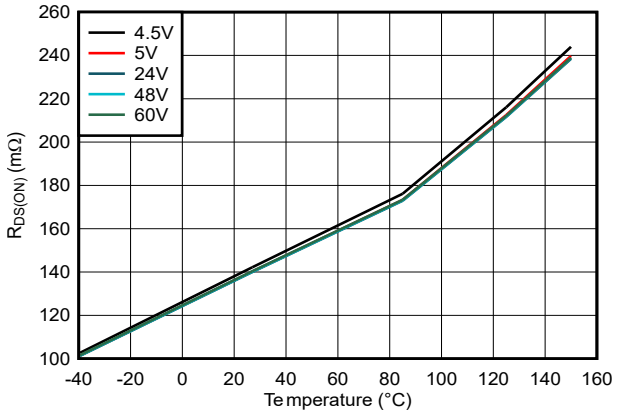


Figure 5-4. $R_{DS(on)}$ Over Temperature

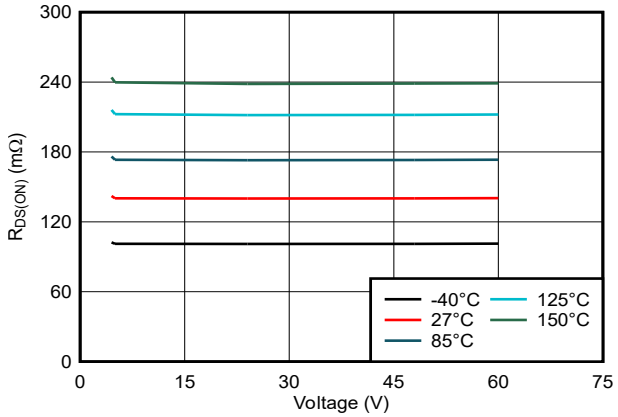


Figure 5-5. $R_{DS(on)}$ Over V_M

6 Detailed Description

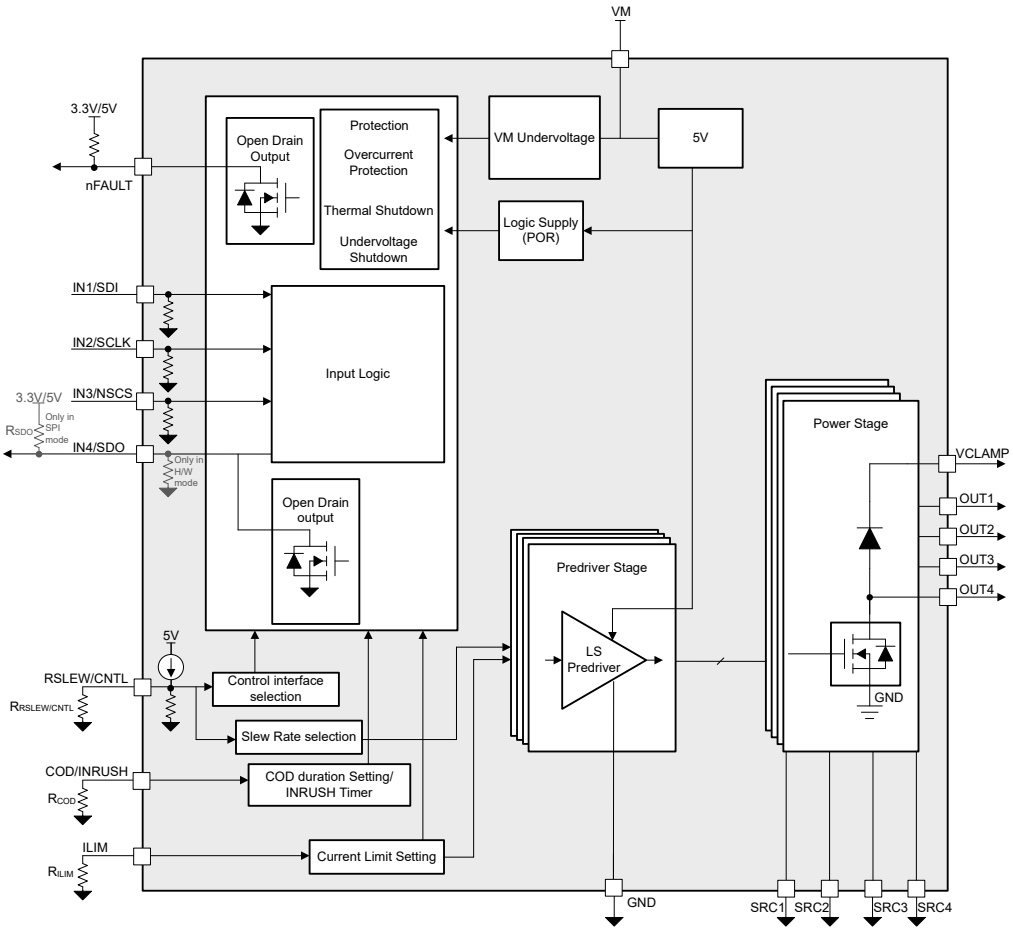
6.1 Overview

The DRV81646 is a versatile four-channel low-side switching driver that operates within a wide voltage range of 4.5V to 65V, supporting a broad spectrum of load current requirements. This device incorporates four integrated low-side switches, each featuring low on-resistance of 140mΩ and equipped with a freewheeling diode connected to the VCLAMP pin. This configuration enables users to either recirculate current flow or attach an external Transient Voltage Suppressor (TVS) for safe management of inductive load turn-off.

The device offers flexible control through multiple interface options, including hardware GPIO and standard 4-wire SPI communication. Each channel is equipped with dedicated overtemperature protection and adjustable current limiting capabilities, which can be configured using an external resistor on the ILIM pin. An optional cut-off delay (COD) feature is available to restrict the time duration of current-limiting events on individual channels, thereby preventing damage to both the device and connected loads. Output switching rates can be customized through resistor configuration on the RSLEW/CNTL pin, providing enhanced control flexibility over the output switches. Additionally, the device includes an INRUSH mode that temporarily elevates the current limit threshold to accommodate capacitive load applications.

The DRV81646 provides a dedicated fault output pin (nFAULT) for indicating error conditions, while individual channel fault status monitoring is available when operating in SPI mode. This capability enables rapid identification and response to any fault conditions that occur, supporting efficient and reliable system operation.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Control Interface and Slew Rate (RSLEW/CNTL)

The RSLEW/CNTL pin sets the output slew rate and control interface. This pin can be set by external resistors or directly controlled by a microcontroller DAC. The slew rate and control interface is latched on device start-up when VM rises above V_{UVLO} and cannot be changed during operation. Table 6-1 shows the rise/fall times available in Hardware mode. Table 6-2 shows the rise and fall times available in SPI mode.

The slew rate stays fairly consistent across VM and VLOAD voltages, but the rise time changes based on the voltage. For example, V_{VM}=12V has approximately half the rise time as V_{VM} = 24V for the same slew rate.

Table 6-1. Hardware Mode Slew Rate Selection

CONTROL INTERFACE	RISE TIME OR FALL TIME (TYPICAL, V_{VM} = 24V)	SLEW RATE FOR V_{VM} = 24V	RSLEW/CNTL PIN VOLTAGE
Hardware (GPIO)	100ns	192V/µs	V_{LVL1} (Tied to GND)
	300ns	64V/µs	V_{LVL6} (Hi-Z/floating)
	700ns	27.4V/µs	V_{LVL4} (100kΩ to GND)
	1500ns	12.8V/µs	V_{LVL3} (44.2kΩ to GND)

Table 6-2. SPI Mode Slew Rate Selection

CONTROL INTERFACE	RISE TIME OR FALL TIME (TYPICAL, V_{VM} = 24V)	SLEW RATE FOR V_{VM} = 24V	RSLEW/CNTL PIN VOLTAGE
SPI	300ns	64V/µs	V_{LVL7} (Tied to Logic Voltage)
	700ns	27.4V/µs	V_{LVL5} (249kΩ to GND)
	1500ns	12.8V/µs	V_{LVL2} (14.7kΩ to GND)

6.3.2 Current Sensing With FET Source Terminals

The source terminal of each MOSFET is exposed on the SRCx pins. An external sense resistor can be connected between a SRC pin and GND to measure the current on that channel as shown in Figure 6-1.

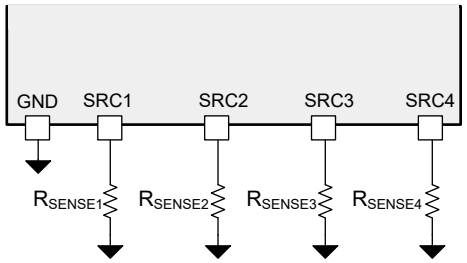


Figure 6-1. Sense Resistors on Each SRC Pin

The SRC pins must be connected directly to GND if external current sensing is not used.

The Absolute Maximum Ratings for the SRCx pins set the maximum voltage across the shunt resistor to 0.6V. The shunt resistor must be sized so that at the highest load current the voltage across the sense resistor doesn't exceed 0.6V.

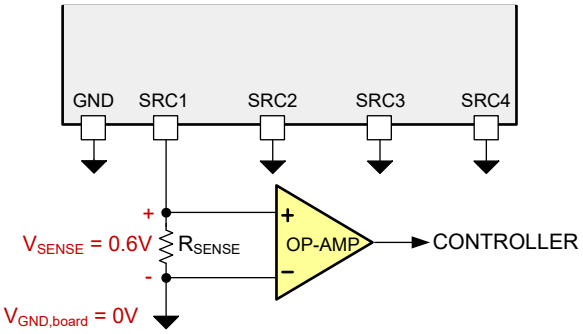


Figure 6-2. SRCx Voltage With Respect to Board Ground Using Current Sense Resistor

For example, let's use 250mV for the maximum V_{SENSE}, which is less than 0.6V and provides some margin for safety or error. Let's use a maximum current I_{PEAK} of 4A for an example load, as if ILIM is set to 30kΩ for a I_{LIM} = 2A and $I_{LIM\_ACTIVATE}$ = 3A.

$$R_{SENSE} = \frac{V_{SENSE}}{I_{PEAK}} = \frac{0.250V}{4A} = 0.0625\Omega = 62.5m\Omega \quad (1)$$

The current sense resistor must be less than or equal to 62.5mΩ for this example load of 4A peak current to maintain a V_{SENSE} less than 250mV. The sense resistor also needs to be sized appropriately for power dissipation. For this example of 4A across a 62.5mΩ resistor the power dissipation:

$$D = I2R = 4A^2 \times 0.0625\Omega = 1.0W \quad (2)$$

Thus, a 1W resistor or larger is recommended for this example.

6.3.3 Integrated Clamp Diode, VCLAMP

The DRV81646 contains four protected low-side drivers. Each output has an integrated clamp diode connected to a common pin, VCLAMP.

VCLAMP can connect to a Zener or TVS diode to VM or to GND, allowing the switch voltage to exceed the main supply voltage VM. This connection can be beneficial when driving loads that require very fast current decay. Because each output has a diode to the VCLAMP pin, the user can share a single external TVS diode for all 4 channels. Alternatively, VCLAMP can be connected directly to the main power supply voltage (VM).

In all cases, the voltage on the outputs must not be allowed to exceed the DRV81646 maximum output voltage specification. Below are some configurations which are supported by the DRV81646.

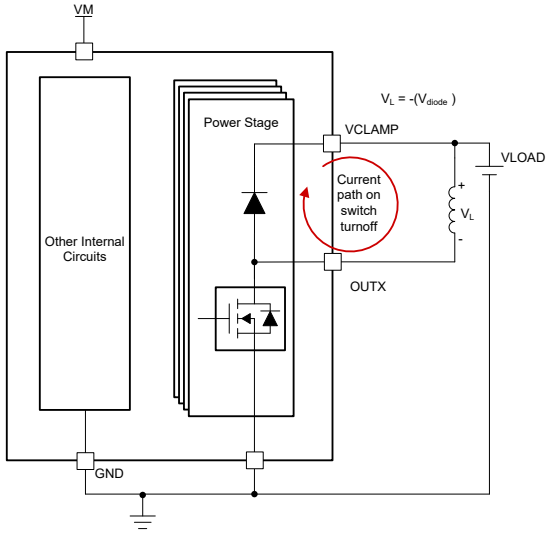


Figure 6-3. Slow Decay (VCLAMP Tied to VLOAD)

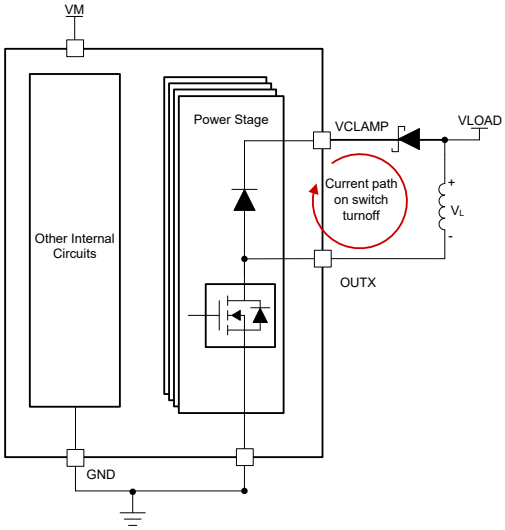


Figure 6-4. Fastest Decay (TVS/Zener VCLAMP to VLOAD)

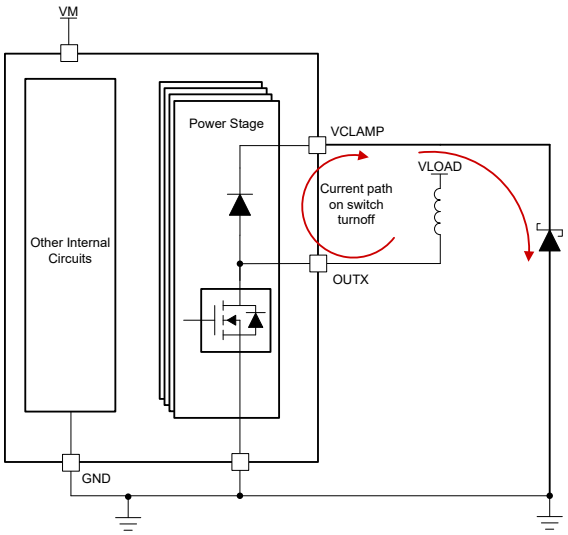


Figure 6-5. Fast Decay (TVS/Zener CLAMP to GND)

Table 6-3. VCLAMP Decay Modes

VCLAMP CONNECTION	DECAY MODE	WHEN TO USE	V_L VOLTAGE
Directly to VLOAD	Slow Decay	Loads that do not need fast decay. Safe for the full VM operating range.	$V_L = -V_{diode}$
TVS or Zener to VLOAD	Fast Decay	Fastest current decay. Not recommended when VM or VLOAD > 28V due to chance of exceeding OUTx maximum voltage.	$V_L = -[V_{diode} + V_{zener}]$
TVS or Zener to GND	Fast Decay	Lower clamping voltage than TVS to VLOAD, but slightly less fast current decay. TVS needs higher breakdown voltage than VLOAD to prevent leakage current.	$V_L = -[V_{diode} + V_{zener} - V_{LOAD}]$

6.3.4 Protection Circuits

The DRV81646 is protected from VM undervoltage, per-channel overtemperature, die overtemperature, and overcurrent events.

6.3.4.1 ILIM Analog Current Limit

The DRV81646 implements an analog current limit on each output as a protection against short circuits or capacitive loads with large inrush current. If the output stage sees a high-current condition I > $I_{LIM\_ACTIVATE}$, the FET gate drive voltage is reduced to regulate the output current at the I_{LIM} level. This gate drive adjustment operates the FET in the linear region, resulting in a much higher $R_{DS(ON)}$ and dissipating significant power. This current limiting feature (ILIM) is designed to be similar to overcurrent protection, but instead of completely shutting the FET off during an overcurrent event, the current is limited to a safe level until the device overheats.

Figures Figure 6-6 and Figure 6-7 show ILIM reducing the inrush current to a safe level before steady-state continuous current, such as in the case of a capacitive load. This feature provides system-level benefits of reducing PCB trace width and reducing the system power supply capability requirements.

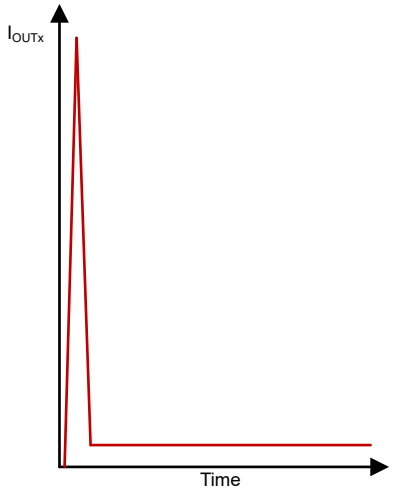


Figure 6-6. High Startup Current Without Current Limiting Protection

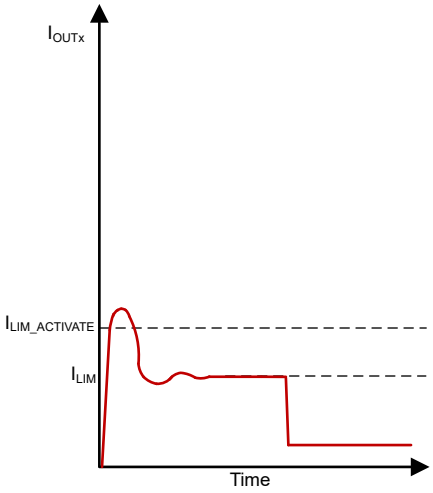


Figure 6-7. Controlled Startup Current With ILIM Current Limiting Protection

The analog current limit level, I_{LIM}, can be configured with a pull-down resistor on the ILIM pin to GND as shown in Table 6-4. The same value of I_{LIM} is set for all four channels based on R_{ILIM}. The current limit condition on one channel does not affect other channels, unless there is an event such as a chip-wide over-temperature.

Table 6-4. Analog Current Limit Level Depending on ILIM Resistor

R_{ILIM} RESISTOR BETWEEN ILIM PIN AND GND	CURRENT LIMIT LEVEL, I_{LIM}
$0 \le R_{LIM} < 20k\Omega$	3A
$30k\Omega \le R_{LIM} \le 120k\Omega$	$I_{LIM}[A] = 60/R_{LIM}[k\Omega]$
$R_{LIM} \ge 120k\Omega$	$I_{LIM}[A] = 60/R_{LIM}[k\Omega]$, can be non-linear

Figure 6-8 shows the active current limit during $t_{TIME\_TO\_TSD}$ during a short condition with cut-off delay disabled ($0k\Omega \le R_{COD} < 20k\Omega$). The cut-off delay feature is explained further in Section 6.3.4.2. After the channel shuts off, the channel retries only after the channel temperature returns to safe level ($t_{TSD} - t_{TSD\_HYS}$). If the channel INx state changes during a I_{LIM} condition the controller responds to the input state change, such as shutting off the output. If the device has shut off due to TSD and the temperature is still above a safe level, the device does not respond to the input state change, meaning the devices does not turn the output back on if the device is still too hot, even if INx is toggled.

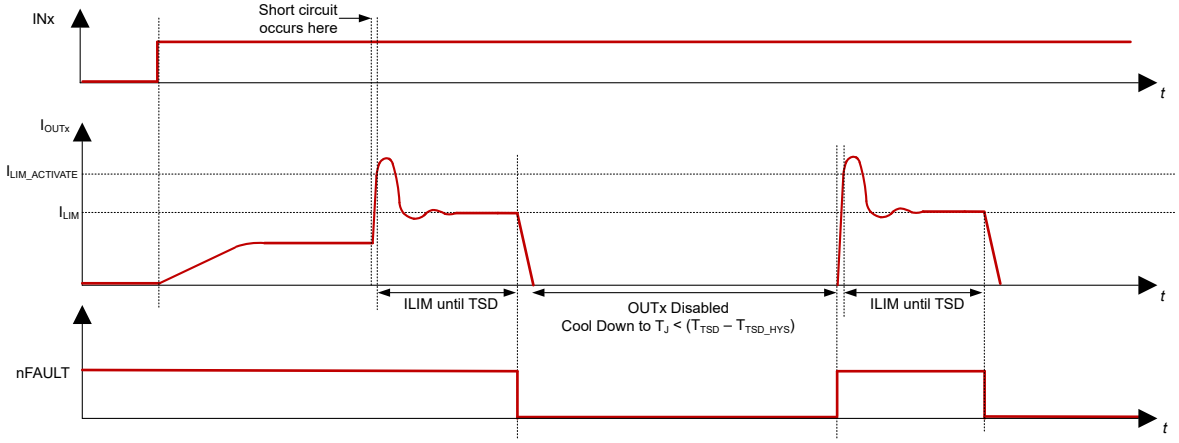


Figure 6-8. Current Limit Response to Short With Thermal Shutdown Based Retry (Cut-Off Delay Disabled)

Figure 6-9 shows a simplified schematic of the analog current limit circuit for each low-side FET.

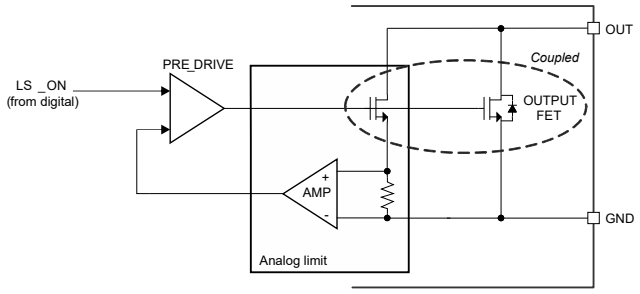


Figure 6-9. Analog Current Limit and Sensing Diagram

6.3.4.1.1 Effect of Load Resistance on Power Dissipation Before TSD

The resistance of the load affects how long the channel operates in the linear region before hitting thermal shutdown. The resistance functions similarly to a linear drop-out regulator (LDO), where a higher voltage drop requires the device to dissipate more power.

For example, take a 24V system with a 1A I_{LIM} setting for a 5Ω load versus an 11Ω load. Without current limiting these draw 4.8A and 2.2A respectively, but with the I_{LIM} feature, these regulate to 1A. Use Equation 3 to calculate the linear region resistance of the FET to achieve this 1A current limit:

$$I = \frac{V}{R} \quad (3)$$

$$I_{LIM} = \frac{V_{VM}}{\left[R_{LOAD} + R_{DS(ON)}\right]} \quad (4)$$

Rearrange Equation 4 to solve for $R_{DS(ON)}$, then plug in the system values for loads 5Ω and 11Ω:

$$R_{DS(ON)} = \left[\frac{V_{VM}}{I_{LIM}}\right] - R_{LOAD} \quad (5)$$

$$R_{DS(ON)\_5\Omega} = \left(\frac{24V}{1A}\right) - 5\Omega \rightarrow R_{DS(ON)\_5\Omega} = 19\Omega \quad (6)$$

$$R_{DS(ON)\_11\Omega} = \left(\frac{24V}{1A}\right) - 11\Omega \rightarrow R_{DS(ON)\_11\Omega} = 13\Omega \quad (7)$$

Use this resistance to calculate the power dissipated inside the DRV81646 FET:

$$P_{FET\_5\Omega} = I^2 \times R = 1A^2 \times 19\Omega = 19W \quad (8)$$

$$P_{FET\_11\Omega} = I^2 \times R = 1A^2 \times 13\Omega = 13W \quad (9)$$

As in Equation 8 and Equation 9, even though both loads are limited to 1A, the DRV81646 has to dissipate more power for a 5Ω load than an 11Ω load. This power dissipation directly correlates with the temperature rise of the FET over time. More power dissipated means the channel hits thermal shutdown faster.

6.3.4.2 Cut-Off Delay (COD)

Since the analog current limit condition results in very high power dissipation, the DRV81646 offers a cut-off delay feature that controls the maximum length of an I_{LIM} or overcurrent condition. t_{COD} can be adjusted with a pull-down resistor on the COD/INRUSH pin as shown in Table 6-5.

Table 6-5. Cut-Off Delay (COD) Settings

R_{COD} RESISTOR BETWEEN COD/INRUSH AND GND	FUNCTION BEHAVIOR	nFAULT PIN	FAULT BIT (SPI)
$0 \le R_{COD} < 20k\Omega$	Cut-off delay function is disabled, output stage and IC are protected by thermal shutdown only	Pulled low when a channel hits thermal shutdown. Released when channel temperature returns to safe level	The FAULT bit of the corresponding channel is set if the channel hits thermal shutdown. The bit is cleared automatically at the end of valid SPI transaction
$60k\Omega \le R_{COD} \le 240k\Omega$	Current limit allowed to persist for $t_{COD} = R_{COD}(k\Omega)/120ms$ typical, before power stage shuts off	Pulled low when t_{COD} elapses. Released when t_{RETRY} elapses.	The FAULT bit of the corresponding channel is set when t_{COD} elapses. The bit is cleared automatically at the end of valid SPI transaction
$240k\Omega \le R_{COD} \le 470k\Omega$	$t_{COD} = R_{COD}(k\Omega)/120ms$, but linearity is not specified.		
$R_{COD} \ge 1M\Omega$	INRUSH mode enabled. t_{INRUSH} = 10ms typical.	Masked during inrush period t_{INRUSH}, then pulled low if a power stage hits thermal shutdown.	The FAULT bit of the corresponding channel is masked during inrush period t_{INRUSH}, then pulled low if a power stage hits thermal shutdown.

For $60k\Omega \le R_{COD} \le 240k\Omega$, the device lasts in current limit condition for duration $t_{COD} = R_{COD}(k\Omega)/120ms$. After the channel shuts off, the channel retries only after an interval of $t_{RETRY} = (t_{COD} \times 32)$ ms typical. If the user changes channel state during a current limit condition, the controller responds to the input state change. During t_{RETRY}, however, the controller does not respond to an input state change.

For $R_{COD} \ge 240k\Omega$ the same equation holds true, t_{COD} (ms) = $R_{COD}(k\Omega)/120$, but linearity is not specified.

If a thermal shutdown occurs during the COD interval, the channel turns off and retries once the temperature reaches safe level. The COD timer is paused for the duration the output turns off due to thermal shutdown.

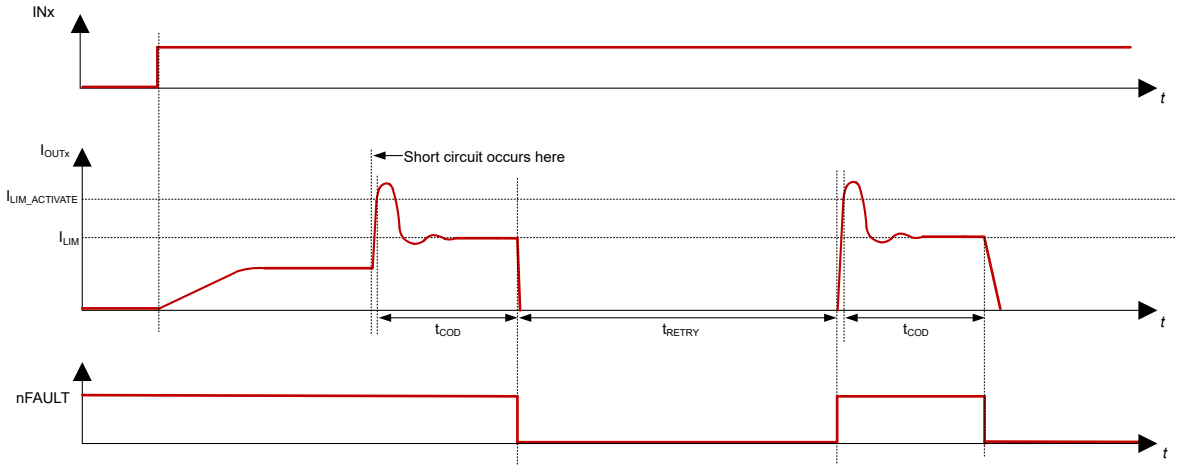


Figure 6-10. Current Limit Circuit Response to Short with COD Enabled

The cut-off delay-based timing of t_{COD} and t_{RETRY} feature reduces the average power dissipation compared to thermal-shutdown based retry. Without COD, the device recovers from thermal shutdown in 1-5ms at room temperature with one channel on. With COD, the device waits the full t_{RETRY} period before re-enabling the output. For example, let's calculate the average power dissipation per cycle with versus without COD for R_{ILIM}=100kΩ, V_{VM} = V_{LOAD} = 24V, R_{LOAD} = 1Ω

$$I_{LIM} = \frac{60}{R_{ILIM}} = \frac{60}{100} = 0.6A \quad (10)$$

$$P_{OUTx\_ILIM} = V_{OUTx} \times I_{LIM} = [V_{LOAD} - I_{LIM} \times R_{LOAD}] \times I_{LIM} = [24V - 1\Omega \times 0.6A] = 0.6A = 14.0W \quad (11)$$

With cut-off delay enabled (60kΩ ≤ R_{COD} ≤ 240kΩ) the average current depends on the t_{COD} and the t_{RETRY} = t_{COD} × 32ms. For R_{COD} = 120kΩ

$$t_{COD} = \frac{R_{COD}[k\Omega]}{120} = \frac{120}{120} = 1ms \quad (12)$$

$$t_{RETRY} = t_{COD} \times 32 = 1ms \times 32 = 32ms \quad (13)$$

$$P_{COD\_AVERAGE} = \frac{[P_{OUTx\_ILIM} \times t_{COD}]}{t_{COD} + t_{RETRY}} = \frac{[14.0W \times 1ms]}{1ms + 32ms} = 0.43W \quad (14)$$

Without cut-off delay (COD pin connected to GND, or R_{COD} < 20kΩ) the device automatically retries after thermal hysteresis (T_J < (t_{TSD} – t_{TSD_HYS}). Calculate the average power dissipation using a retry time of $t_{TSD\_HYS\_RETRY}$ = 2.5ms and the same 1ms on-time as if the device thermal shutdown after t_{TSD} = 1ms:

$$P_{ILIM\_AVERAGE} = \frac{[P_{OUTx\_ILIM} \times t_{TSD}]}{[t_{TSD} + t_{TSD\_HYS\_RETRY}]} = \frac{[14.0W \times 1ms]}{[1ms + 2.5ms]} = 4W \quad (15)$$

Cut-off delay results in a significantly lower average power dissipation (0.43W in this example) than thermal-shutdown based protection (4W in this example). This result leads to lower overall system heating and better performance on adjacent device channels.

6.3.4.3 INRUSH Mode

The DRV81646 offers an INRUSH mode which boosts the current limit for a 10ms interval (t_{INRUSH}) to support capacitive loads such as lamps which require a large current at turn on. To enable INRUSH mode, leave the COD/INRUSH pin unconnected or put a pulldown resistor larger than or equal to 1MΩ on the pin.

The current limit during t_{INRUSH} is I_{INRUSH} = 120 ÷ R_{ILIM}[kΩ] for R_{ILIM}≥ 40kΩ. This is also equal to 2 times the I_{LIM} current limitation value. $I_{INRUSH\_ACTIVATE}$ = I_{INRUSH} + 50%, or

$$I_{INRUSH}[A] = 120 \times R_{ILIM}[k\Omega] \quad (16)$$

$$I_{INRUSH\_ACTIVATE}[A] = I_{INRUSH} \times 1.50 \quad (17)$$

For example, a 60kΩ resistor on the ILIM pin results in I_{INRUSH} = 120 ÷ 60 = 2.0A. The inrush current regulation only activates after the current passes $I_{INRUSH\_ACTIVATE}$ = 2.0A × 1.5 = 3.0A. After 10ms the current is regulated at the I_{LIM} level. Figure 6-11 shows the inrush behavior followed by regular I_{LIM} current regulation until thermal shutdown or until the current drops below the I_{LIM} level.

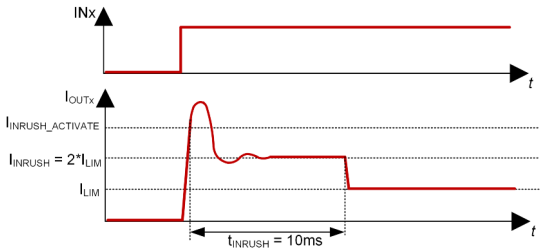


Figure 6-11. Current Limit Value During INRUSH

If a channel shuts off during t_{INRUSH} due to thermal shutdown, the inrush timer is paused until the channel temperature falls to a safe level, below T_{TSD}-T_{TSD_HYS}. Then the timer continues with the boosted current limit I_{INRUSH}. The inrush timer count is reset if the corresponding INx is pulled low. When INx is pulled high the inrush counter restarts. Figure 6-12 illustrates this timer functionality with a load that causes a thermal shutdown during t_{INRUSH}, and the current regulation dropping down to the I_{LIM} setting after t > t_{INRUSH} .

During t_{INRUSH}, the nFAULT pin and NFAULT SPI bit is masked for that channel to prevent unwanted fault trigger during the initial inrush period. The nFAULT pin and bit still reports a fault on a *different* channel. For example, if Channel 1 is within t_{INRUSH} and Channel 3 has a thermal shutdown, the nFAULT pin and bit report a fault.

Table 6-6. INRUSH Mode Fault Reporting

DEVICE STATE	CURRENT LIMIT	nFAULT PIN	FAULT BIT (SPI)
t < t_{INRUSH}	I_{INRUSH}	Masked during Inrush period t_{INRUSH}	The FAULT bit of the corresponding channel is masked during Inrush period t_{INRUSH} .
t > t_{INRUSH}	I_{LIM}	Pulled low if a power stage hits thermal shutdown. Released when channel temperature returns to a safe level.	The FAULT bit of the corresponding channel is set if channel hits thermal shutdown. The bit is cleared automatically at the end of valid SPI transaction

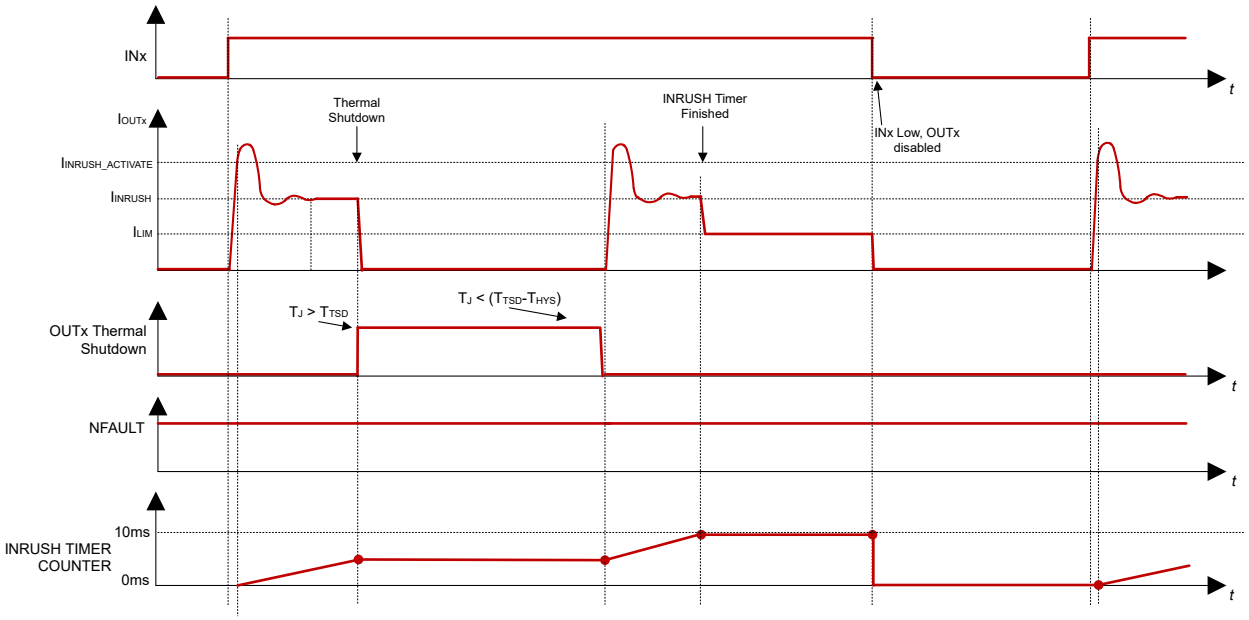


Figure 6-12. INRUSH Timer Example With Channel Thermal Shutdown During t_{INRUSH}

6.3.4.4 Thermal Shutdown (TSD)

A dedicated thermal sensor is placed close to each power FET. When a channel encounters an overtemperature condition, the corresponding power FET is disabled and the NFAULT pin is asserted low. The thermal protection of the four output power stages is independent.

In SPI mode, when a channel hits thermal shut-down the corresponding channel FAULT bit is set. The bit is automatically cleared when an input state change is detected.

If the die temperature exceeds safe limits, all output FETs are disabled and the nFAULT pin is driven low. After the die temperature has fallen to a safe level, operation automatically resumes. In SPI mode, the FAULT bits for all channels are set in case of a full die-level overtemperature event.

6.3.4.5 Undervoltage Lockout (UVLO)

Whenever the voltage on the VM pin falls below the UVLO falling threshold voltage, V_{UVLO}, all circuitry in the device is disabled, the output FETS are disabled, and all internal logic is reset. Operation continues when the V_{VM} voltage rises above the UVLO rising threshold, as shown in Figure 6-13

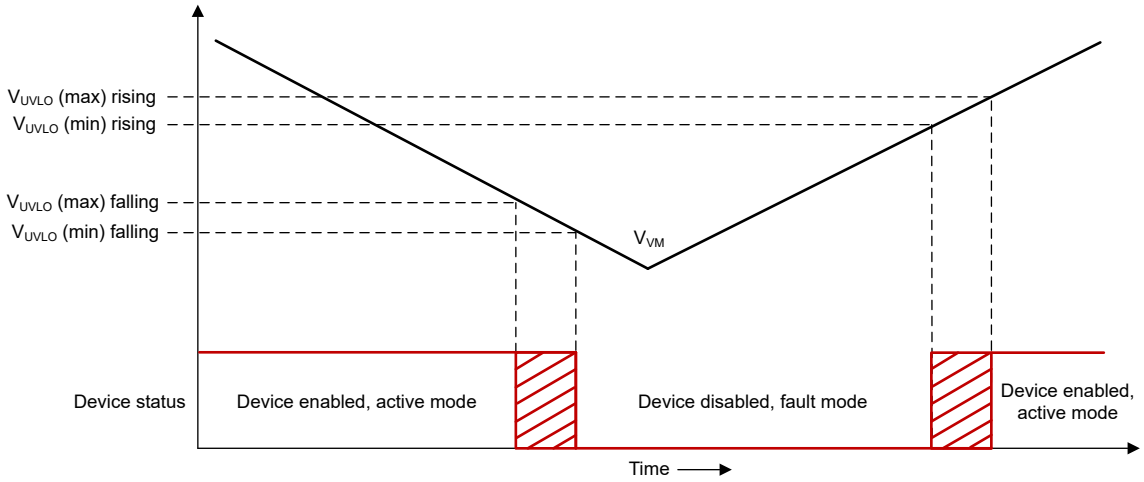


Figure 6-13. VM UVLO Operation

6.3.5 Fault Conditions Summary

Table 6-7 summarizes the fault conditions and how to recover from each condition. Additionally, the nFAULT pin is pulled low momentarily when the device first wakes up (VM > $V_{UVLO(rising)}$). After time t_{nFAULT_VALID} the nFAULT pin accurately reports any fault states, but during the t_{nFAULT_VALID} time the microcontroller can ignore any nFAULT low signals.

Table 6-7. Fault Conditions Summary

FAULT		SPI FAULT [X] – FAULT BIT OF CHANNEL X	INRUSH COUNTER	NFAULT PIN	SDO IN T_{H_SCLK} INTERVAL	RECOVERY
Channel Overtemperature, $T_{J\_CHx} > T_{TSD}$	$0 < t < t_{INRUSH}$	Not set	Paused	High	SDI	$T_J < (T_{TSD} – T_{TSD\_HYS})$
	$t > t_{INRUSH}$	Set only for affected channel	-	Pulled Low	SDI	
Global (Die) Overtemperature, $T_J > T_{TSD}$	$0 < t < t_{INRUSH}$	Set for all channels	Paused	Pulled Low	SDI	$T_J < (T_{TSD} – T_{TSD\_HYS})$
	$t > t_{INRUSH}$		—			
COD time expiry, when COD enabled		Set only for affected channel	-	Pulled Low	SDI	t_{RETRY} elapses
SPI Error		Not set	-	High	Low	Next valid SPI frame
VM Undervoltage (UVLO), $V_{VM} < V_{UVLO}$ VM falling		SPI unavailable	—	Internal circuits disabled	SPI unavailable	$V_{VM} > V_{UVLO}$ VM rising

6.4 Device Functional Modes

6.4.1 Hardware Interface Operation

The DRV81646 can be controlled through a simple hardware interface where IN_X decides state of OUT_X. When the INx pin is driven high, internal logic switches on the corresponding output FET. Setting INx low switches off the corresponding OUTx FET. Table 6-8 lists this control scheme.

Table 6-8. Hardware Control Mode for Channel x

INx	OUTx	DESCRIPTION
0	Hi-Z	OUTx disabled (Hi-Z)
1	L	OUTx FET on

6.4.2 Parallel Outputs

Two outputs can be connected together in parallel for higher current. Figure 6-14 shows the schematic of DRV81646 driving two solenoid loads. The device also supports paralleling all four channels together.

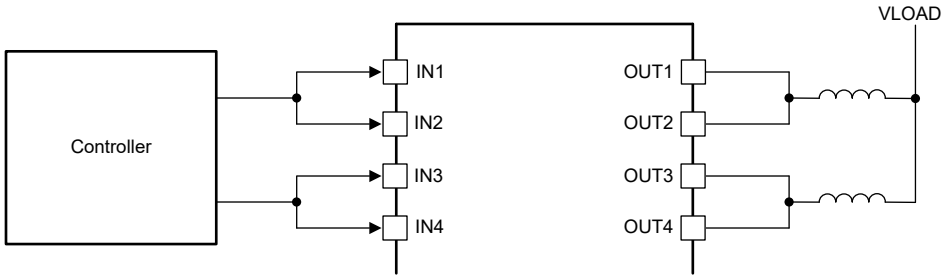


Figure 6-14. Drive Two Solenoids with Higher Current

Take care that the recirculation current on the VCLAMP pin does not exceed the absolute maximum ratings for continuous RMS current or transient current <1ms. PWM with a large inductive load can cause high current on VCLAMP.

6.4.3 SPI Mode

The DRV81646 offers a 4-wire serial peripheral interface (SPI) which allows the user to program channel states and read back fault information for each channel. The serial data must be in 8-bit format as shown in Figure 6-15.

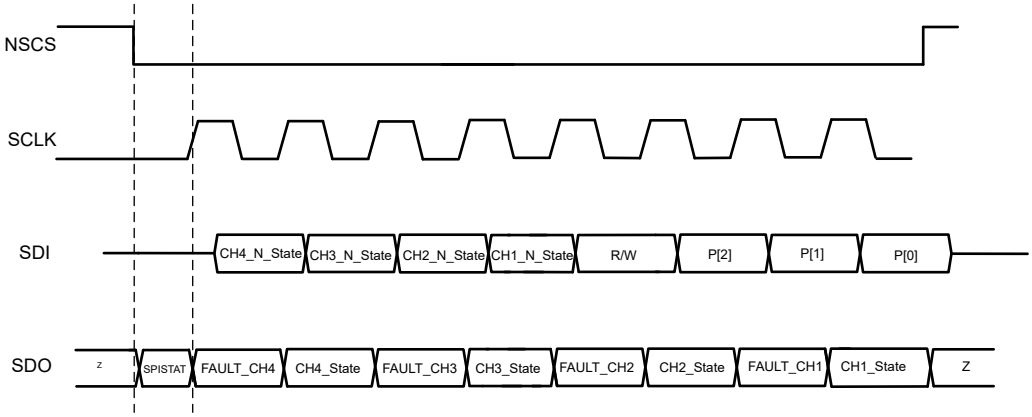


Figure 6-15. SPI Data - Standard *8-Bit* Frame With SPISTAT

6.4.3.1 Parity Bit Calculation

P[2:0] is a set of 3 parity bits which are used to check the correctness of received data word. If the parity check fails then the output states are not updated. The parity bits are calculated as follows, where ⊕ is XOR:

- P[2] : B7 ⊕ B6 ⊕ B5
- P[1] : B6 ⊕ B5 ⊕ B4
- P[0] : B5 ⊕ B4 ⊕ B3

For example to set (R/W=1) the channels to OUT4=1, OUT3=0, OUT2=0, and OUT1=1 the parity calculation and frame construction is below:

- P[2] = (1 ⊕ 0 ⊕ 0) = 1
- P[1] = (0 ⊕ 1 ⊕ 1) = 0
- P[0] = (0 ⊕ 1 ⊕ 1) = 0
- Thus, P[2:0] = 0b100
- Full frame = 0b1001 1100 = 0x9C

The following is pseudo-code from the EVM firmware implementing the parity bit calculation :

```
bool B7 = startOut4;
bool B6 = startOut3;
bool B5 = startOut2;
bool B4 = startOut1;
bool B3 = rw_bit;

bool P2 = B7 ^ B6 ^ B5;
bool P1 = B6 ^ B5 ^ B4;
bool P0 = B5 ^ B4 ^ B3;

uint8_t CMD = (B7 << 7)|(B6 << 6)|(B5 << 5)|(B4 << 4)|(B3 << 3)|(P2 << 2)|(P1 << 1)|(P0 << 0);
```

6.4.3.2 SPI Input Packet

Table 6-9. SPI Input Packet

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CH4_N_State	CH3_N_State	CH2_N_State	CH1_N_State	R/W	P[2:0]		

When CHx_N_State bit is set to 1, internal logic switches on the corresponding low side output channel N-FET. Setting CHx_N_State to 0 switches off the corresponding OUTx.

The R/W (Read/Write) bit determines if the CHx_N_state bit is propagated to outputs or not. Set R/W to 1 to perform write operation. Set R/W to 0 to read the existing channel state and fault information while leaving current output state unchanged. A fault on an output switches off the output and the state returns 0.

6.4.3.3 SPI Response Packet

Table 6-10. SPI Response Packet

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FAULT_CH4	CH4_State	FAULT_CH3	CH3_State	FAULT_CH2	CH2_State	FAULT_CH1	CH1_State

The current channel states of individual channels are latched on the falling edge of the nSCS pin (when SPI transaction is initiated). Latched faults are cleared on rising edge of the nSCS pin.

Table 6-11. FAULT_CHx Bit Description

FAULT_CHx	DESCRIPTION
0	Channel is working normally since last SPI transaction
1	Fault occurred on channel X. This bit is set if channel X encountered a fault since the last SPI transaction. The bit clears when NSCS is pulled back high at the end of valid SPI transaction (parity checks pass).

6.4.3.4 SPI Error Reporting

An SPI error occurs if:

- The parity check on received data bits does not match with received parity bits
- The number of SCLK pulses received when NSCS is low is not a multiple of 8

A SPI error on current transaction is reported in the **next** transaction by the DRV81646 pulling SDO low/high during the t_{H_SCLK} interval. The SDO state is set to SPISTAT = (SDI) and NOT(SPI_ERROR). The easiest way to read the SPISTAT value is to hold SDI=1 during the t_{H_SCLK} interval and read SPISTAT after t_{SDOHIZ}, so that if there is a SPI error then SPISTAT=0, else SPISTAT=1.

A SPI error is not reported on the nFAULT pin.

Table 6-12. SPISTAT SPI Error Reporting

SPI ERROR?	NOT(SPI_ERROR)	SDI	SPISTAT
No	1	0	0
No	1	1	1
Yes	0	0	0
Yes	0	1	0

6.4.3.5 SPI Daisy Chain

Multiple devices can be connected to the controller with and without the daisy chain. For connecting 'n' number of devices to a controller without using a daisy chain, 'n' number of GPIO resources from controller have to be used for the individual NSCS pins. Whereas, if the daisy chain configuration is used, a single NSCS line can be used for connecting multiple devices.

Figure 6-16 shows how two DRV81646 devices can be connected in daisy chain to leverage GPIO or isolation pin saving. SDO pin of one device is fed to the SDI pin of the following device in the chain. Note that a pullup resistor needs to be connected at each SDO pin because the pin is open-drain.

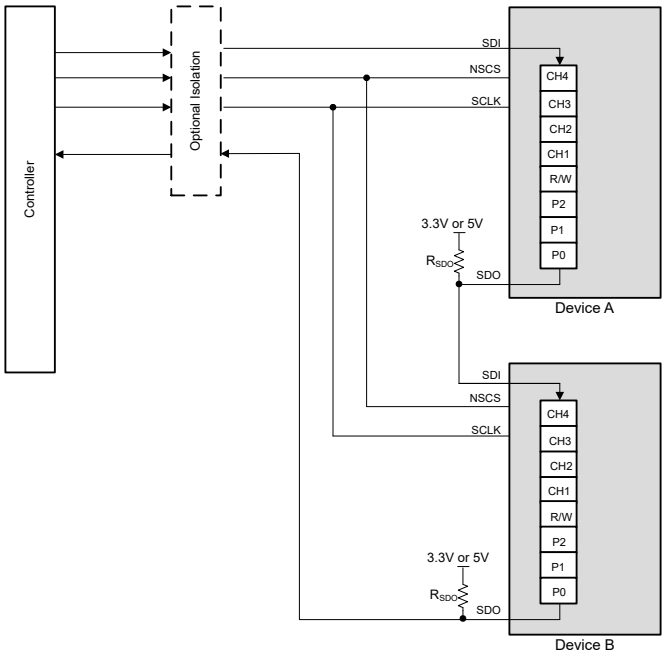


Figure 6-16. Two DRV81646 Devices Connected in Daisy Chain

To write to two devices, 16 bits of data need to be written as shown in Figure 6-17. Note SDO is sent out on the positive edge of SCLK. SDO is ready to be sampled on following negative edge of SCLK. The value on SDI pin is also sampled on negative edge of SCLK.

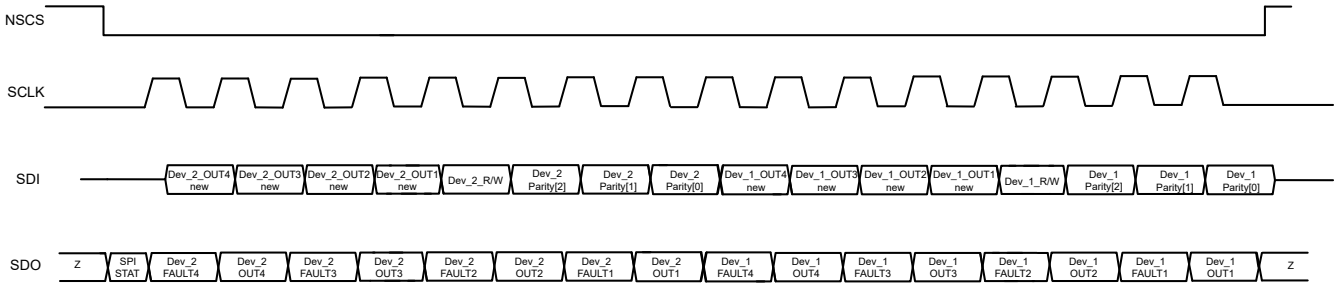


Figure 6-17. 16-bit Data Packet for Communication With Two Daisy Chained Devices

Command word decoding is only carried out at rising edge of NSCS if the number of SCLK cycles detected between NSCS falling and rising edges is a multiple of 8. An error detected in SPI communication is reported on the SPI_STAT bit (SDO state between NSCS falling edge and first SCLK rising edge), which can be read back in the subsequent SPI transaction. No report is made on the NFAULT pin.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

The DRV81646 is a quad channel low side that can be used to drive loads to ground such as bulbs, coils, unipolar BDC motors, capacitive loads like LED modules. Channels can be paralleled to drive higher current. For inductive loads that need PWM type control, the DRV81646 also integrates catch diodes from OUT to VCLAMP that can be used to recirculate current for a slow decay. For fast turn-off the user can connect a breakdown Zener at the VCLAMP pin for a fast decay of current in an Inductive load.

7.2 Typical Application

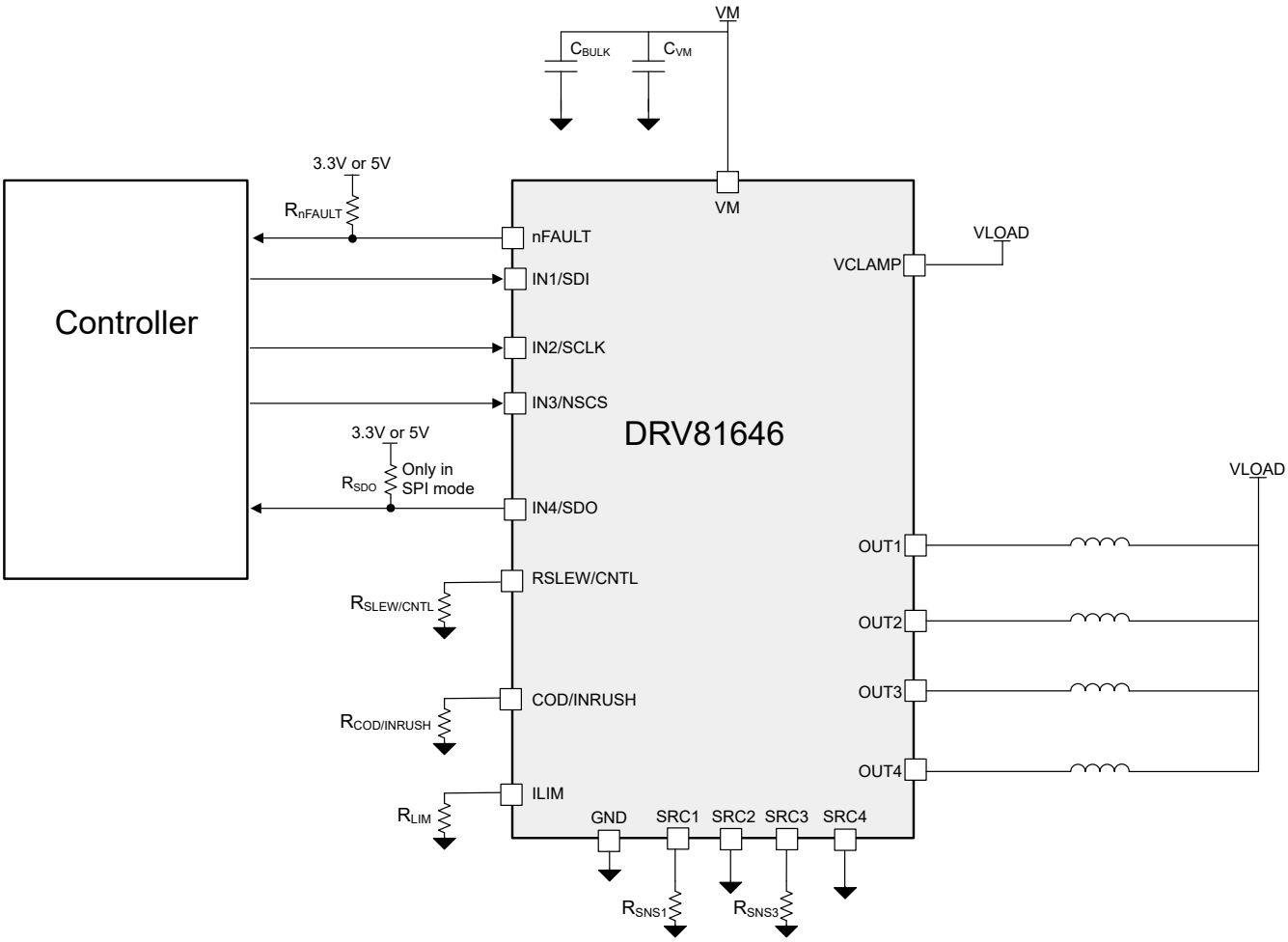


Figure 7-1. Typical Application Schematic

Figure 7-1 shows the application schematic of the DRV81646. The example figure shows optional sense resistors on SRC1 and SRC3 for external current sensing on those channels. VLOAD and VM can be tied together, or can be different voltages as long as the voltages do not exceed any pin absolute maximum ratings.

7.2.1 External Components

Table 7-1 lists the recommended external components for the DRV81646, and Table 7-2 lists additional components that can be used to improve performance or add electrical isolation.

Table 7-1. Required External Components

SYMBOL	DESCRIPTION	VALUE	PURPOSE
C_{VM}	Capacitor on VM	1uF	Supply voltage filtering
C_{BULK}	Bulk capacitor on VM	47uF – 100uF	Supply voltage inrush and ripple smoothing
R_{COD_INRUSH}	Pull-down resistor on COD_INRUSH pin	Set resistance based on desired cut-off delay and INRUSH mode	
R_{SLEW_CNTL}	Pull-down resistor on RSLEW/CNTL pin	Set a pulldown resistor based on slew rate setting and control interface desired	
R_{ILIM}	Pull-down resistor on ILIM pin	Set resistance based on current limit desired	
R_{SDO}	Pull-up resistor to logic voltage on open drain IN4/SDO pin if in SPI mode	10kΩ	Make the SDO voltage rises to logic high when the pin is not pulled low
R_{nFAULT}	Pull-up resistor to logic voltage on open-drain nFAULT pin	10kΩ	Bias the nFAULT voltage to high when the pin is not pulled low

Table 7-2. Optional External Components

SYMBOL	DESCRIPTION	VALUE	PURPOSE
C_{OUT}	Capacitor on each OUTx to GND	10nF	Filtering for system level ESD
TVS_{SURGE}	Surge diode on VCLAMP pin	SMAJ33CA or TVS3300	Protection against system level voltage surge and for inductive demagnetization
R_{SNS}	Current sense resistor on SRC pins to GND	< 200mΩ	Optional Resistor at SRC pin for sensing of load current
$U_{ISOLATION}$	Quad-channel digital isolator for INx or SPI signals	INx control: ISO6440 SPI: ISO6441	Provide electrical isolation between rest of the circuit and the DRV81646

7.2.2 Continuous Current Capability

Table 7-3 and Table 7-4 below show an estimation of the continuous current ability of each channel with different numbers of channels on for different ambient temperatures. Row *1 Channel on* illustrates the continuous current ability if 1 OUT is on, and the other 3 outputs are off. Row *2 Channels on* illustrates if 2 channels are on with an equal load and the other two outputs are off. Row *4 Channels on* illustrates if all 4 channels are on simultaneously with an equal load on each one. For example, with *4 Channels on* each channel can output 2.7A (PWP package) for a total of 10.8A running through the device.

This data is from bench tests on a large PCB with layout optimized for power dissipation, the continuous current capability is different for every system and PCB design.

Table 7-3. FET DC Current Capability per OUTx - PWP Package

Setup	25°C	55°C	85°C	125°C
1 Channel on	3.7A	3.4A	3.2A	2.5A
2 Channels on	3.5A	3.0A	2.7A	2.1A
4 Channels on	2.7A	2.4A	2.0A	1.5A

Table 7-4. FET DC Current Capability per OUTx - DGQ Package

Setup	25°C	55°C	85°C	125°C
1 Channel on	3.4A	3.1A	2.9A	2.4A
2 Channels on	3.1A	2.7A	2.4A	1.8A
4 Channels on	2.5A	2.2A	1.7A	1.3A

Note that this only applies for loads that are continuous ON, not PWM. Switching the outputs with PWM introduces switching losses which further heat the device and results in significantly less average current capability.

7.2.3 Power Dissipation

Power dissipation in the DRV81646 device is dominated by the power dissipated in the output FET resistance, or $R_{DS(on)}$. Average power dissipation of each FET when running a static load can be roughly estimated by Equation 18:

$$P = R_{DS(ON)} \times [I_{OUT}]^2 \quad (18)$$

where

- P is the power dissipation of one FET
- $R_{DS(ON)}$ is the resistance of each FET
- I_{OUT} is equal to the average current drawn by the load.

At start-up and fault conditions, this current is much higher than normal running current; consider these peak currents and duration. When driving more than one load simultaneously, the power in all active output stages must be summed.

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{DS(on)}$ increases with temperature, so as the device heats, the power dissipation increases. Take this action into consideration when sizing the heatsink.

7.2.4 Application Curves

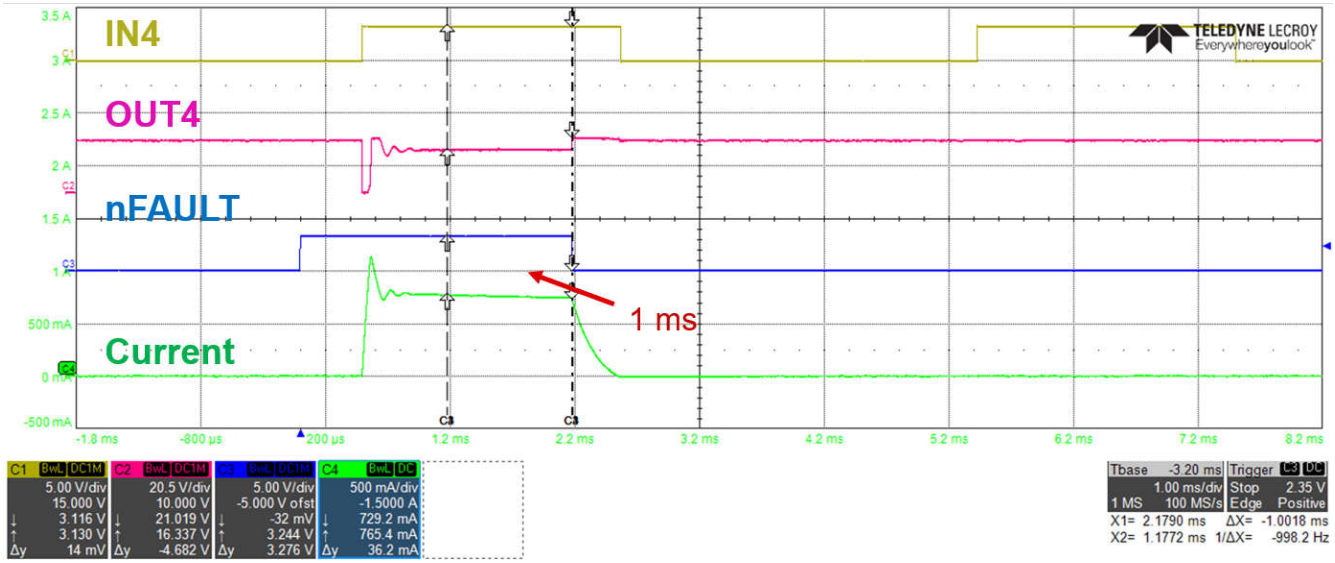


Figure 7-2. t_{COD} = 1ms with R_{COD} = 120kΩ, 12V, 12Ω Load, VCLAMP Shorted to VM

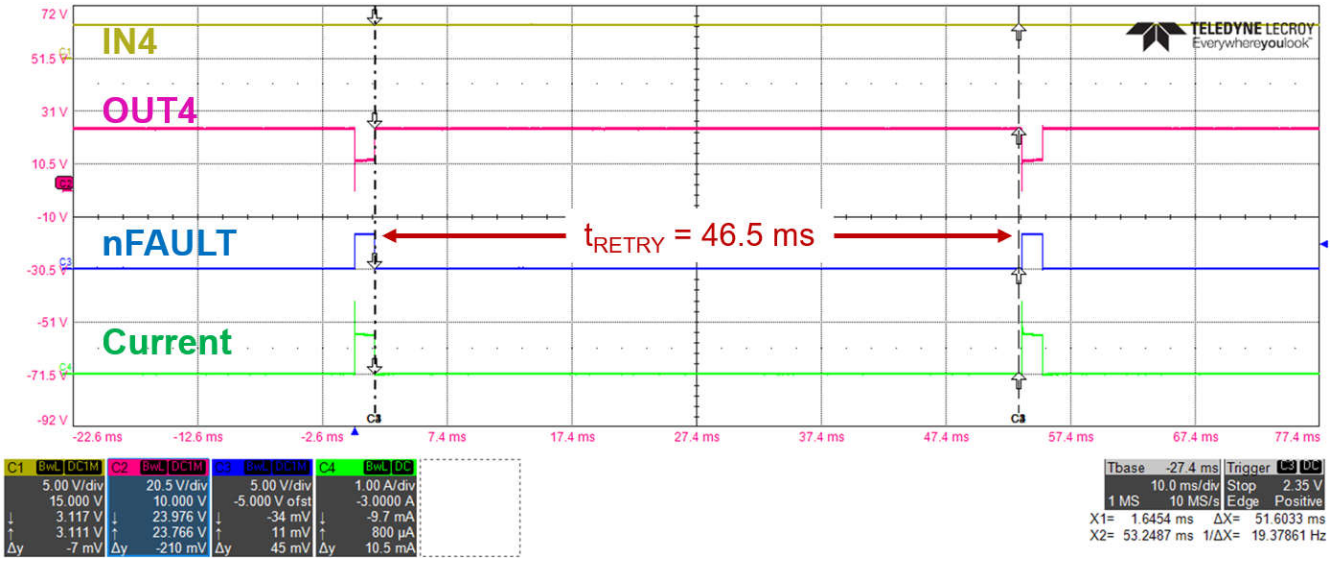


Figure 7-3. t_{RETRY} = 46.5ms with Cut-Off Delay (COD) Enabled, R_{COD} = 180kΩ, 12V, 12Ω 1mH Load, VCLAMP Shorted to VM

7.3 Power Supply Recommendations

7.3.1 Bulk Capacitance

Appropriate local bulk capacitance is an important factor in motor drive system design. Having more bulk capacitance is generally beneficial, although the disadvantages include increased cost and physical size. Bulk capacitors near the motor driver act as a local reservoir of electrical charge to smooth out the motor current variation.

Experienced engineers often use general guidelines about bulk capacitance to select the capacitor values. One such guideline says to use at least *1µF to 4µF of capacitance for each Watt of load power*. For example, a solenoid which draws 4 Amps from a 24V supply has a power of 96 Watts, leading to bulk capacitance of 96µF to 384µF, using this general guideline.

The voltage rating for bulk capacitors must be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

A large value of bulk capacitance is desired to provide a constant VM supply voltage during current transitions, such as solenoid start-up, changes in load torque, or PWM operation. A working estimate of the required capacitance for consistent supply is essential to reduce complexity, cost and size of board electronics. We can use a general guideline method to find an appropriate capacitor size based on the expected load current variation and allowable motor supply voltage variation:

$$C_{BULK} > k \times \Delta I_{MOTOR} \times T_{PWM} \div \Delta V_{SUPPLY} \quad (19)$$

Where:

C_{BULK} is the bulk capacitance

k is a scale factor to account for the ESR for typical capacitors in this type of application; k ≈ 3 is practical for these cases.

ΔI_{MOTOR} is the expected variation in motor current, $i_{max} - i_{min}$

T_{PWM} is the PWM period which is the reciprocal of the PWM frequency

ΔV_{SUPPLY} is the allowable variation in the motor supply voltage.

Figure 7-4 plots several data points and applies this general guideline, showing relatively good agreement.

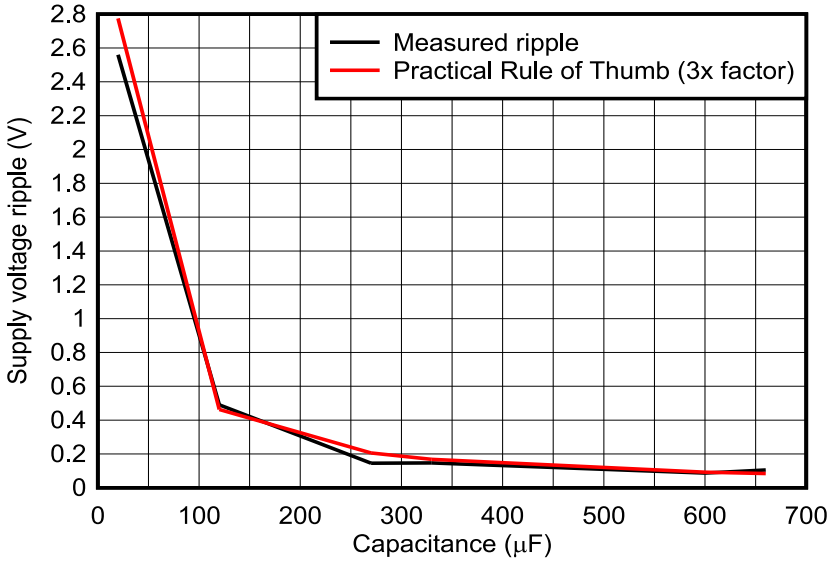


Figure 7-4. Measured Results and 3 × General Guideline, Accounting for Real-World Non-Zero ESR Values of Electrolytic Capacitors

See also the *Bulk Capacitor Sizing for DC Motor Drive Applications* application note.

7.4 Layout

7.4.1 Layout Guidelines

- Place the bulk capacitor to minimize the distance of the high-current path through the motor driver device. Make the connecting metal trace widths as wide as possible, and numerous vias must be used when connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.
- Use wide metal traces for the high-current device outputs.
- The VM pins are bypassed to GND pins using low-ESR ceramic bypass capacitors with a recommended value rated for VM. The capacitors are placed as close to the VM pins as possible with a thick trace or ground plane connection to the device VNEG pins.
- In general, inductance between the power supply pins and decoupling capacitors must be avoided.
- The thermal PAD of the package must be connected to system ground.
  - Try to use a big unbroken single ground plane for the whole system / board. The ground plane can be made at bottom PCB layer. Figure 7-5 shows an example of temperature rise from constricted versus continuous ground pours underneath the driver.
  - To minimize the impedance and inductance, the traces from ground pins are as short and wide as possible, before connecting to bottom layer ground plane through vias.
  - Use multiple vias to reduce the impedance.
  - Try to clear the space around the device as much as possible especially at bottom PCB layer to improve the heat spreading.
  - Single or multiple internal ground planes connected to the thermal PAD also help spread the heat and reduce the thermal resistance.
- For more layout guidelines and best practices see the *Best Practices for Board Layout of Motor Drivers* application note.

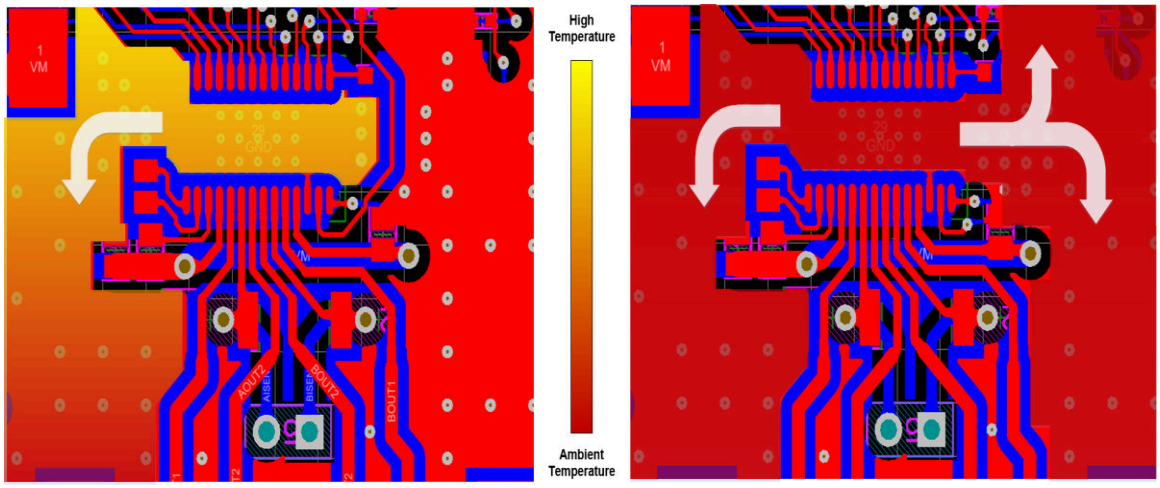


Figure 7-5. Broken Ground vs Continuous Ground Pour Heat Map

7.4.2 Layout Example

For the layout example, see the evaluation module (EVM). The Altium design files can be downloaded from the DRV81646EVM or DRV81646DGQEVM product folder.

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Best Practices for Board Layout of Motor Drivers* application note
- Texas Instruments, *Bulk Capacitor Sizing for DC Motor Drive Applications* application note
- Texas Instruments, *PowerPAD™ Made Easy* application note
- Texas Instruments, *PowerPAD™ Thermally Enhanced Package* application note

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

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All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2025) to Revision A (December 2025)	Page
• Changed the document status from Advance Information to Production Data	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV81646DGQR	Active	Production	HVSSOP (DGQ) | 24	3000 | LARGE T&R	-	NIPDAU	Level-3-260C-168 HR	-40 to 125	81646
DRV81646PWPR	Active	Production	HTSSOP (PWP) | 20	3000 | LARGE T&R	-	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV81646

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

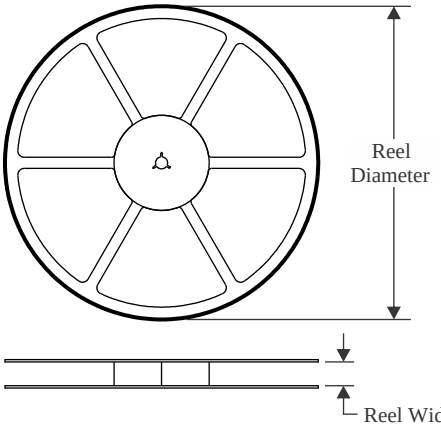
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

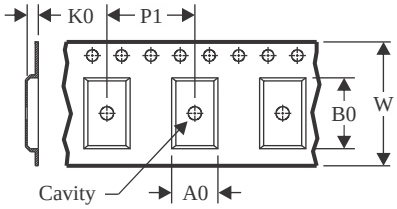
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

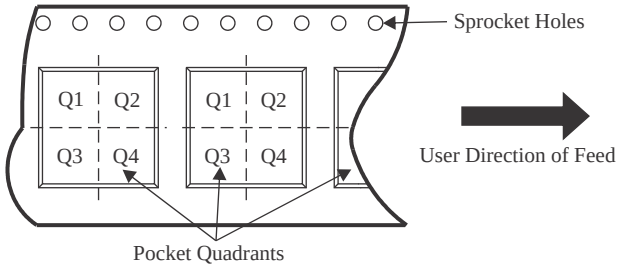


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

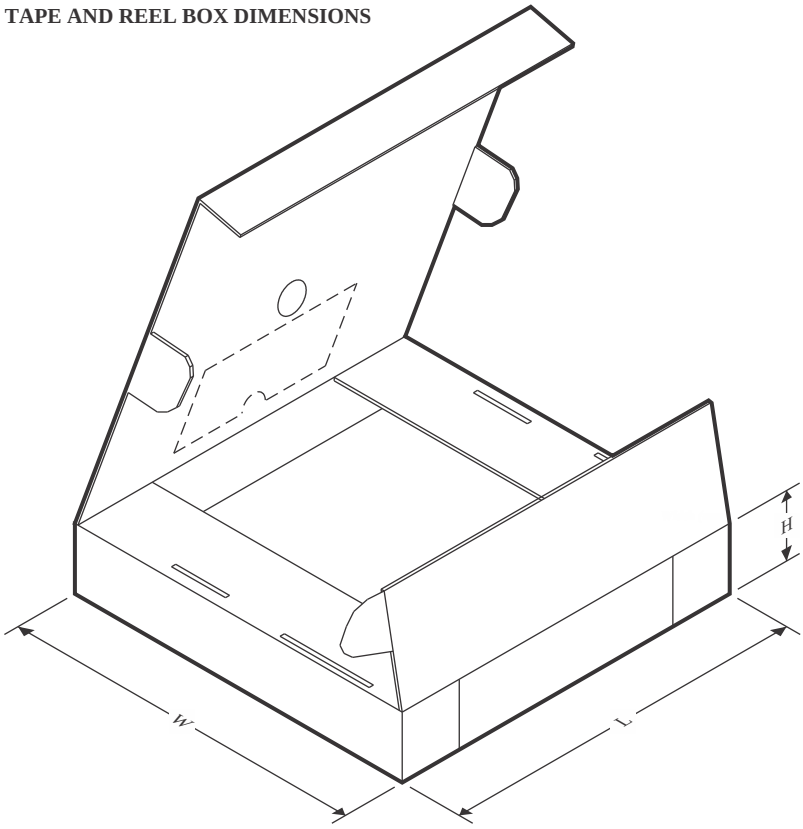
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV81646DGQR	HVSSOP	DGQ	24	3000	330.0	16.4	5.44	6.4	1.45	8.0	16.0	Q1
DRV81646PWPR	HTSSOP	PWP	20	3000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

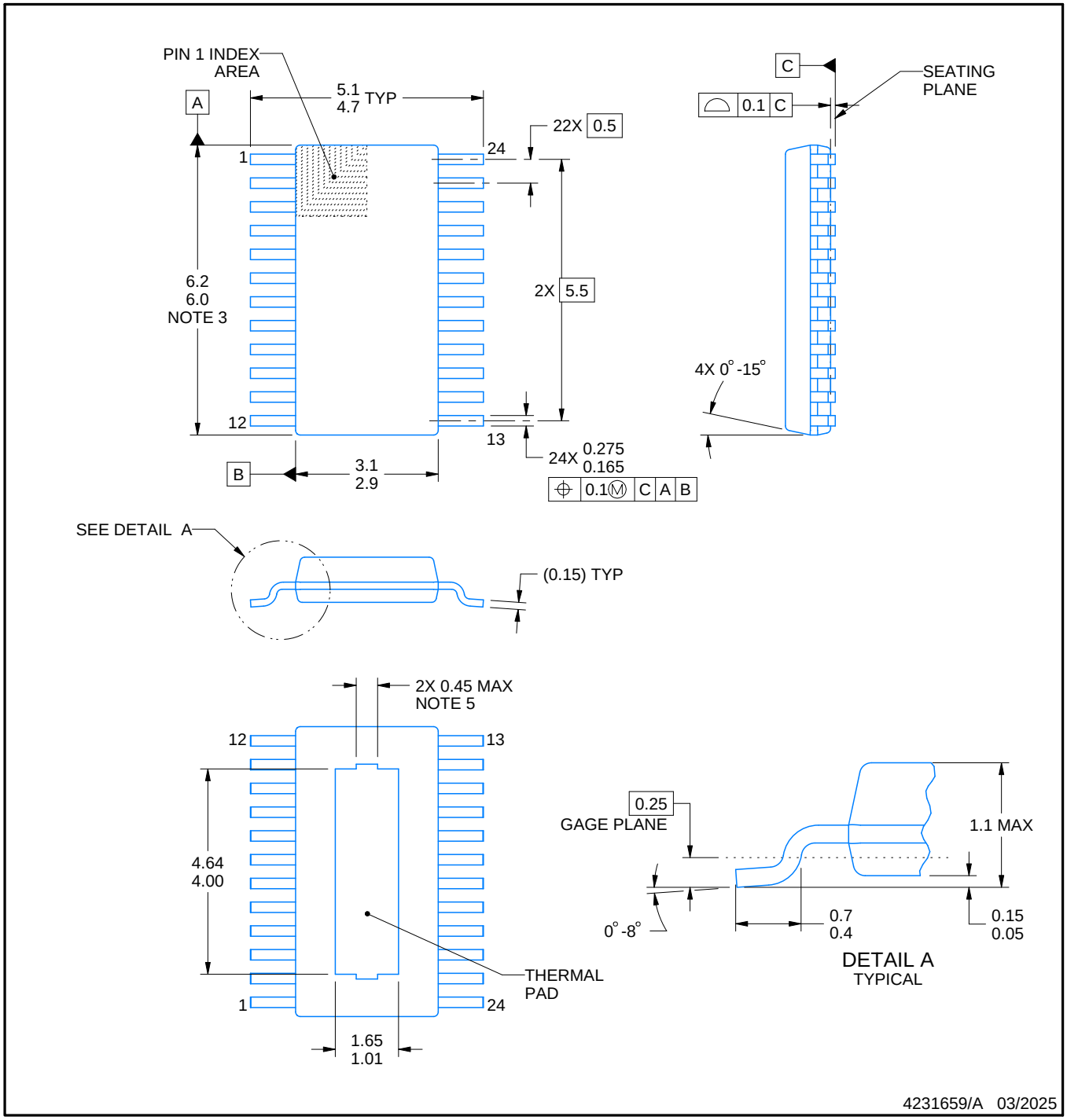
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV81646DGQR	HVSSOP	DGQ	24	3000	353.0	353.0	32.0
DRV81646PWPR	HTSSOP	PWP	20	3000	353.0	353.0	32.0

PACKAGE OUTLINE

DGQ0024A

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



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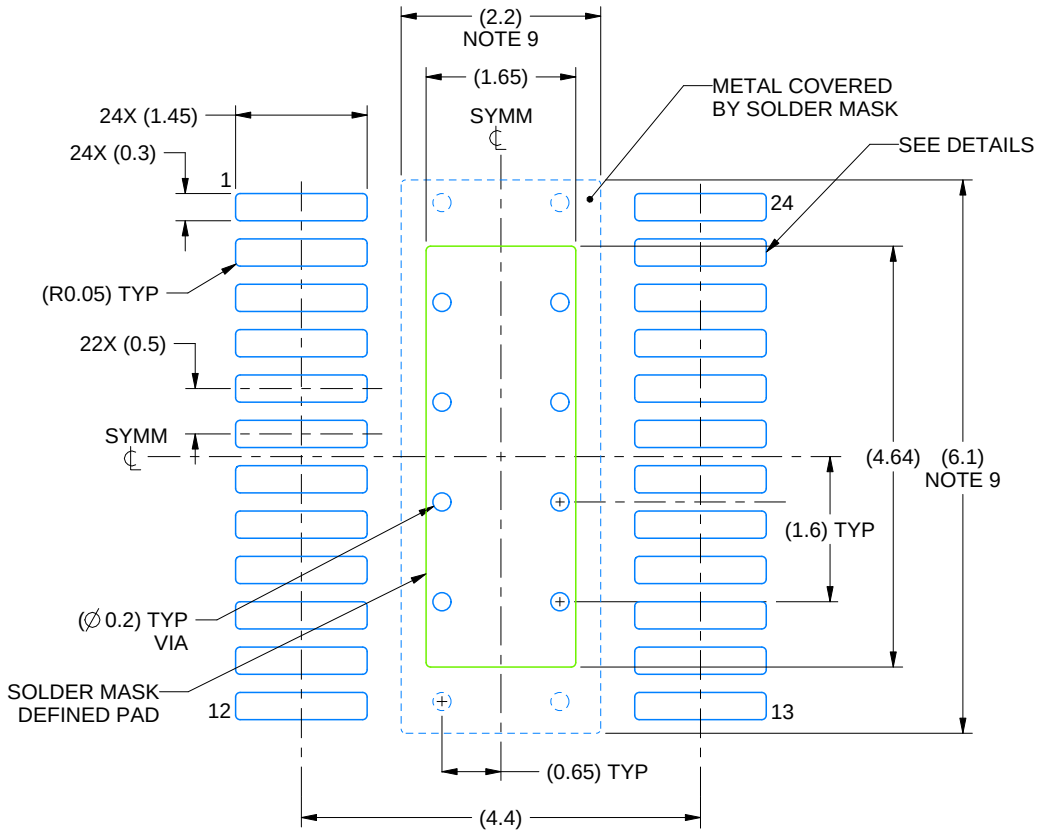
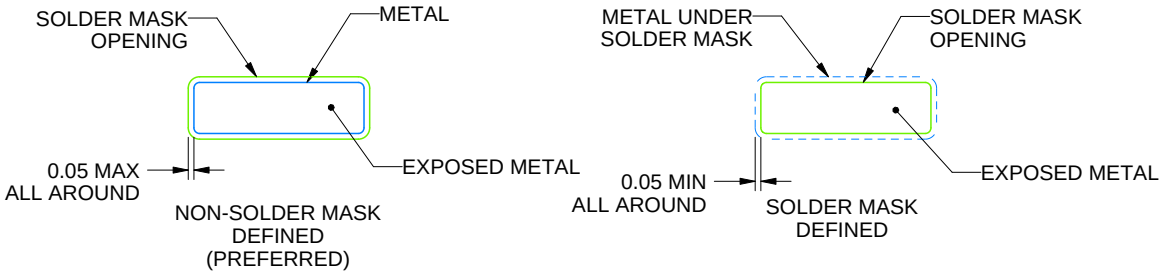
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

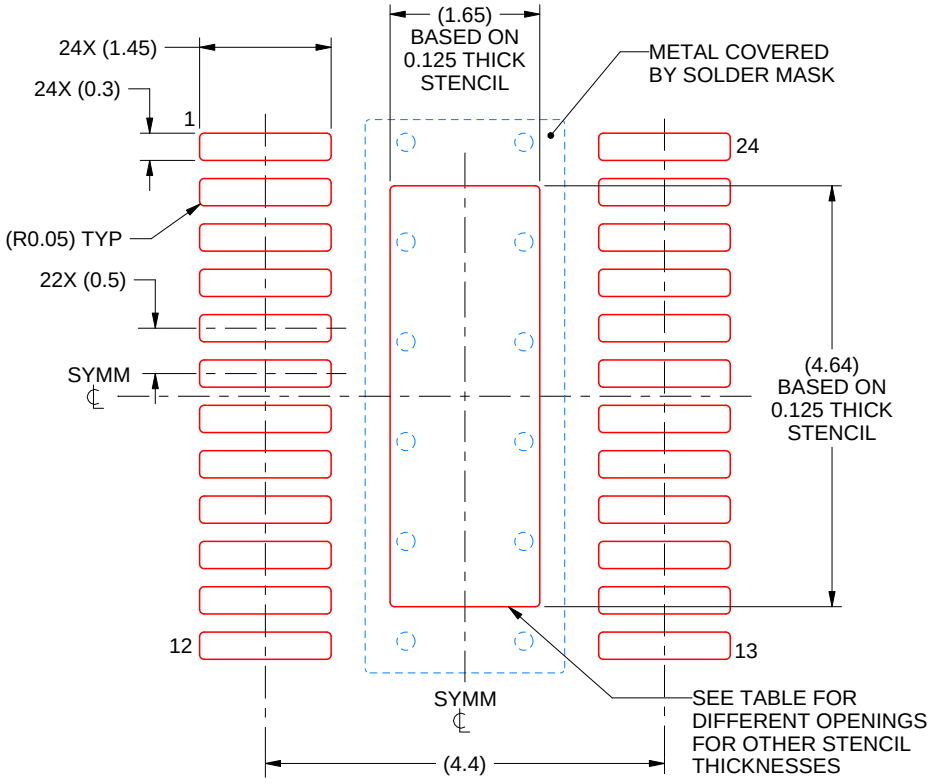


SOLDER MASK DETAILS

4231659/A 03/2025

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.84 X 5.19
0.125	1.65 X 4.64 (SHOWN)
0.15	1.51 X 4.24
0.175	1.39 X 3.92

4231659/A 03/2025

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

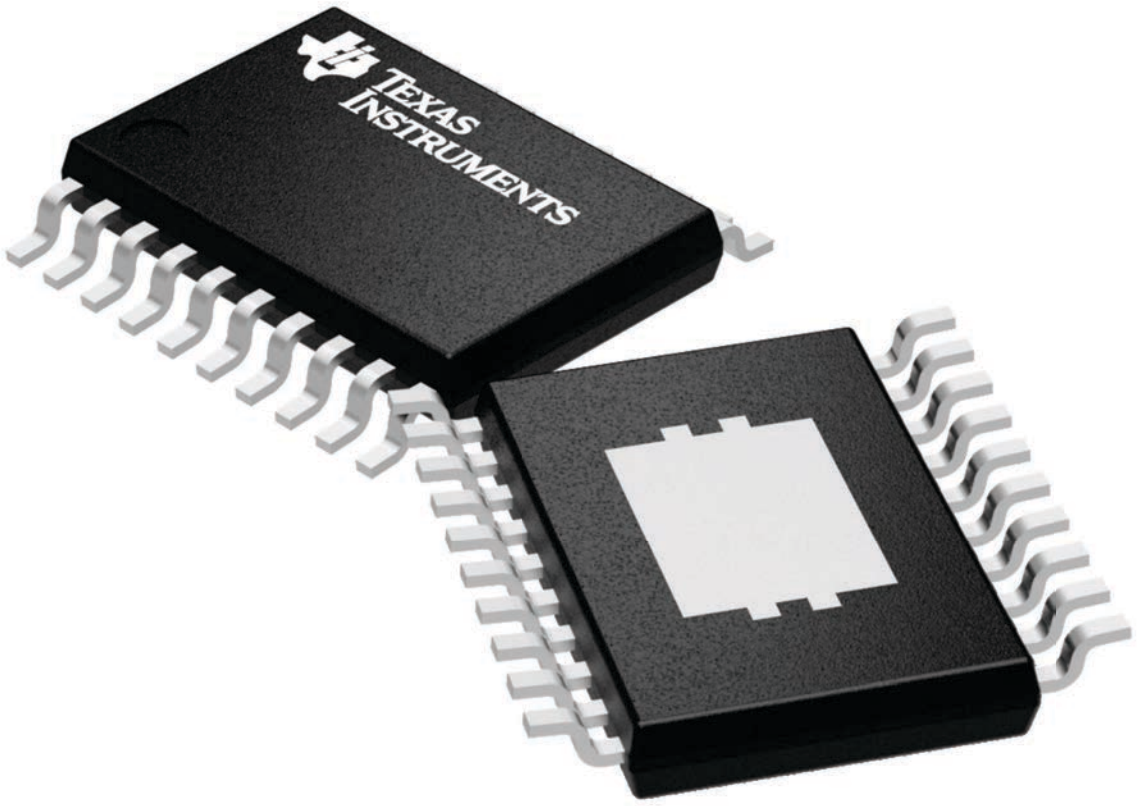
PWP 20

HTSSOP - 1.2 mm max height

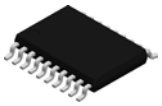
6.5 x 4.4, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224669/A

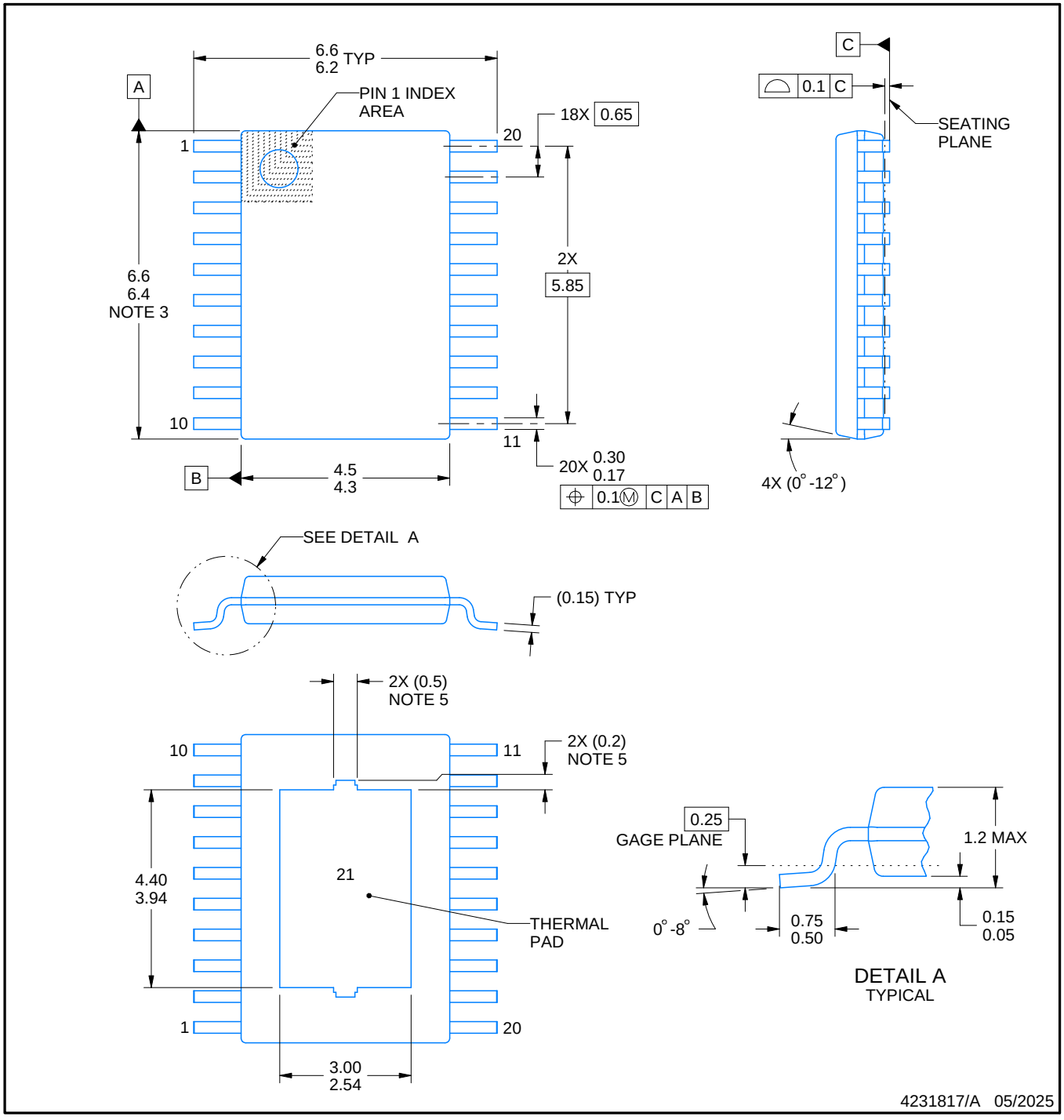


PACKAGE OUTLINE

PWP0020AC

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



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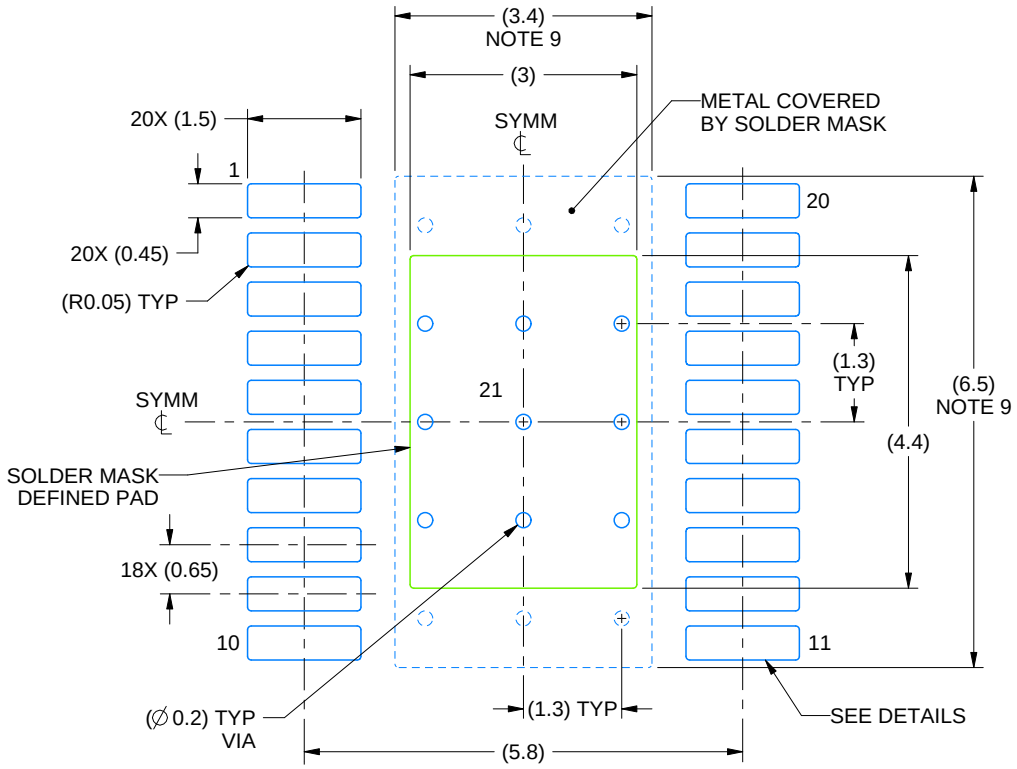
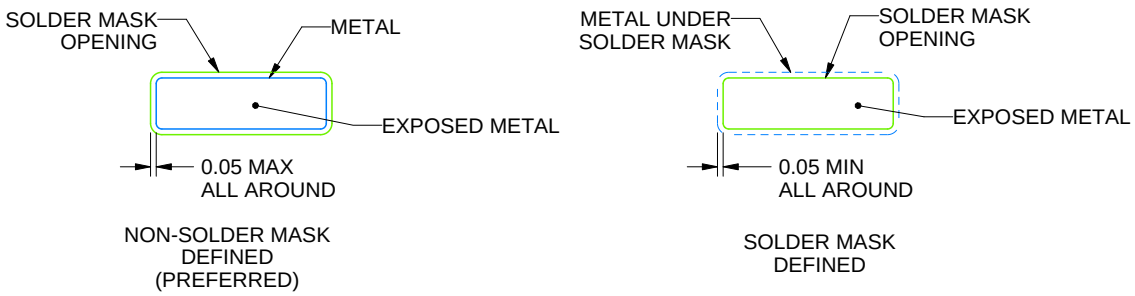
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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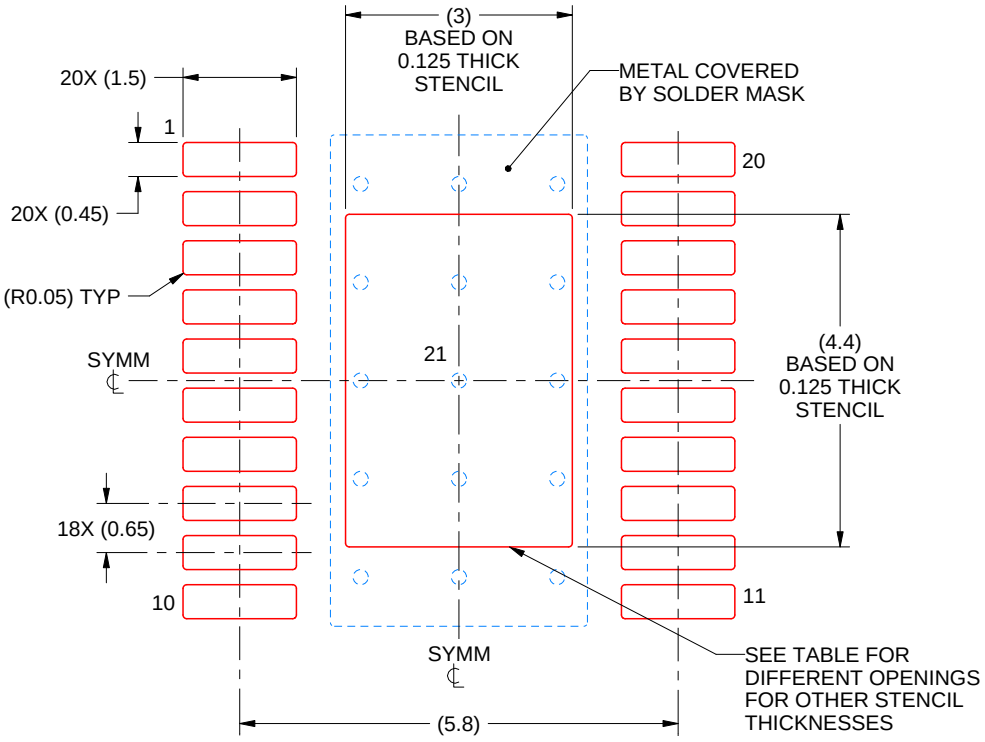
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.35 X 4.92
0.125	3.00 X 4.40 (SHOWN)
0.15	2.74 X 4.02
0.175	2.54 X 3.72

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025