

DRV8262: 60V, Single or Dual H-Bridge Motor Driver with Current Sense Output

1 Features

- – Single or dual H-bridge motor driver
- – Drives One or two brushed-DC motors
- – One stepper motor
- – One or two thermoelectric coolers (TEC)
- **4.5V to 60V** operating supply voltage range
- Low $R_{DS(ON)}$:
 - **100mΩ** HS + LS (**Dual** H-Bridge)
 - **50mΩ** HS + LS (**Single** H-Bridge)
- High output current capability:
 - Dual H-Bridge (24V, 25 °C):
 - **8A peak** with DDW package
 - **16A peak** with DDV package
 - Single H-Bridge (24V, 25 °C):
 - **16A peak** with DDW package
 - **32A peak** with DDV package
- Programmable interface of operation -
 - Phase/Enable (**PH/EN**)
 - PWM (**IN/IN**)
- Integrated current sense and regulation
 - Current sensing for high-side MOSFETs
 - Sense output (**I_{PROPI}**) for each H-bridge
 - **± 4 %** sense accuracy at maximum current
- Separate logic supply voltage (**VCC**)
- Configurable off-Time PWM chopping
 - 7, 16, 24 or 32μs
- Programmable fault recovery method
- Supports 1.8V, 3.3V, 5.0V logic inputs
- Low-current sleep mode (**3μA**)
- Protection features
 - VM undervoltage lockout (UVLO)
 - Charge pump undervoltage (CPUV)
 - Overcurrent protection (OCP)
 - Thermal shutdown (OTSD)
 - Fault condition output (nFAULT)

2 Applications

- [Brushed DC Motors](#)
- [Factory Automation, Stepper Drives and Robotics](#)
- [Medical Imaging, Diagnostics and Equipment](#)
- [ATMs, currency counters, and EPOS](#)
- [TEC Drivers](#)

3 Description

The DRV8262 is a wide-voltage, high-power, H-bridge motor driver for a wide variety of industrial applications. The device integrates two H-bridges to drive one or two DC motors or a bipolar stepper motor. The DRV8262 supports up to 16A peak current in the dual H-bridge mode and up to 32A in the single H-bridge mode. The device also integrates current sensing and regulation, current sense output and protection circuitry.

Integrated current sensing across the high-side MOSFETs allows the driver to regulate the motor current during startup and high load events. A current limit can be set with an adjustable external voltage reference. The device also provides output current proportional to the motor current for each H-bridge. Integrated sensing removes the need for shunt resistors, reducing board area and system cost.

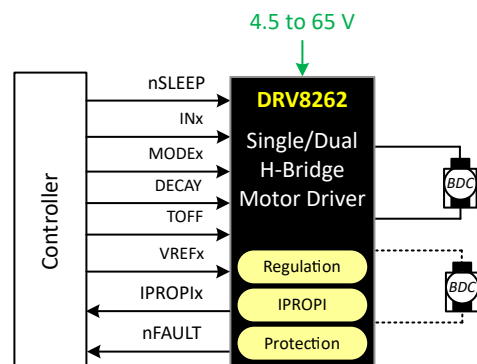
A low-power sleep mode is provided to achieve ultra-low quiescent current. Internal protection features are provided for supply undervoltage lockout (UVLO), charge pump undervoltage (CPUV), output over current (OCP), and device overtemperature (OTSD).

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE (NOM)
DRV8262DDWR	HTSSOP-44 (bottom thermal pad)	14mm × 8.1mm	14mm × 6.1mm
DRV8262DDVR	HTSSOP-44 (top thermal pad)	14mm × 8.1mm	14mm × 6.1mm

(1) See the orderable addendum at the end of the data sheet.

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



DRV8262 Simplified Schematic



Table of Contents

1 Features	1	6.10 Protection Circuits.....	28
2 Applications	1	6.11 Device Functional Modes.....	30
3 Description	1	7 Application and Implementation	32
4 Pin Configuration and Functions	3	7.1 Application Information.....	32
5 Specifications	7	7.2 Power Supply Recommendations.....	40
5.1 Absolute Maximum Ratings.....	7	7.3 Layout.....	42
5.2 ESD Ratings.....	7	8 Package Thermal Considerations	43
5.3 Recommended Operating Conditions.....	8	8.1 DDW Package.....	43
5.4 Thermal Information.....	8	8.2 DDV Package.....	46
5.5 Electrical Characteristics.....	9	8.3 PCB Material Recommendation.....	47
5.6 Typical Characteristics.....	12	9 Device and Documentation Support	48
6 Detailed Description	15	9.1 Documentation Support.....	48
6.1 Overview.....	15	9.2 Receiving Notification of Documentation Updates...	48
6.2 Functional Block Diagram.....	16	9.3 Support Resources.....	48
6.3 Feature Description.....	18	9.4 Trademarks.....	48
6.4 Device Operational Modes.....	19	9.5 Electrostatic Discharge Caution.....	48
6.5 Current Sensing and Regulation.....	21	9.6 Glossary.....	48
6.6 Charge Pump.....	26	10 Revision History	48
6.7 Linear Voltage Regulator.....	27	11 Mechanical, Packaging, and Orderable Information	49
6.8 VCC Voltage Supply.....	27		
6.9 Logic Level, Tri-Level and Quad-Level Pin Diagrams.....	27		

4 Pin Configuration and Functions

The DRV8262 is available in thermally-enhanced, 44-Pin HTSSOP packages.

- The DDW package contains a PowerPAD™ on the bottom side of the device.
- The DDV package contains a PowerPAD™ on the top side of the device for thermal coupling to a heatsink.

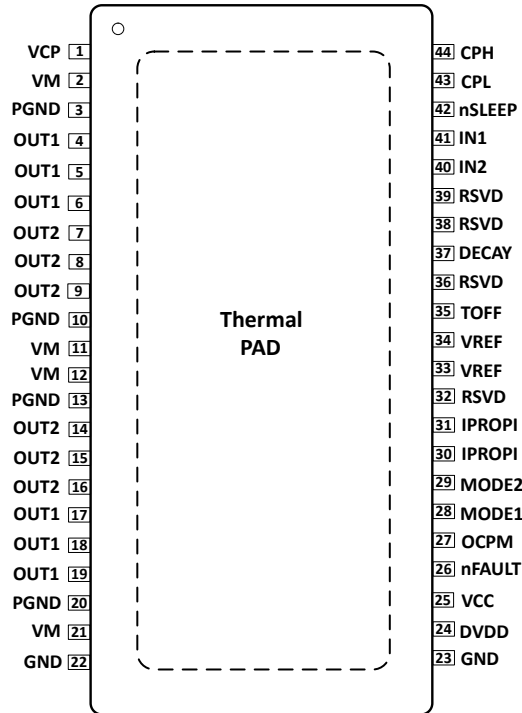


Figure 4-1. Single H-bridge Mode, DDW Package, Top View

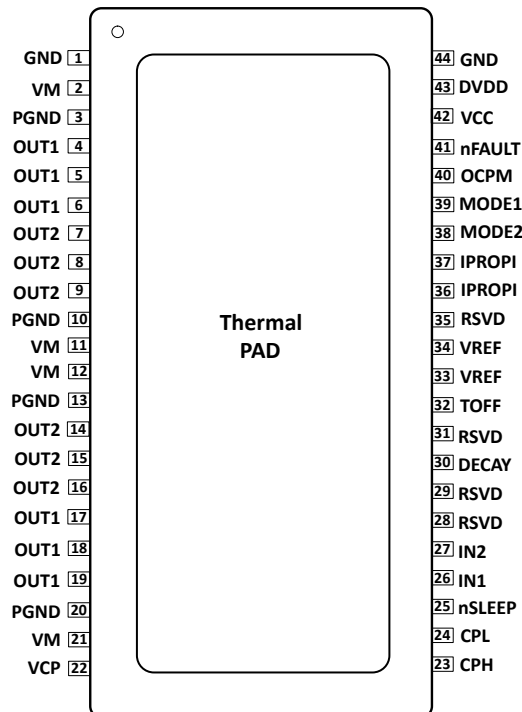


Figure 4-2. Single H-bridge Mode, DDV Package, Top View

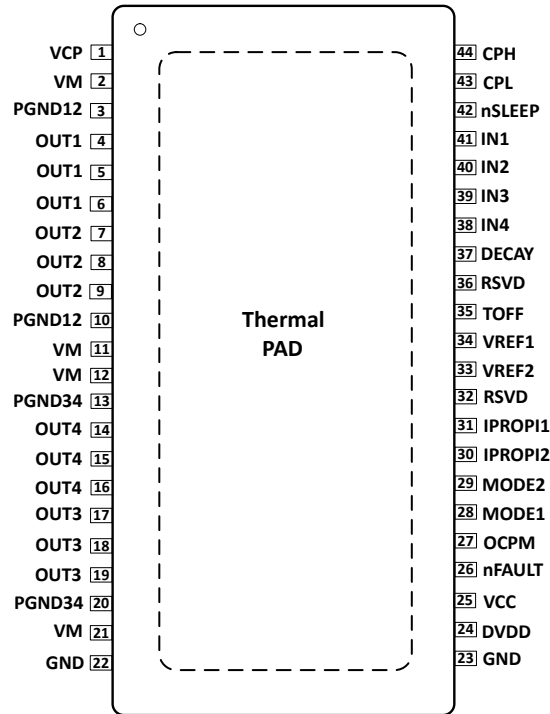


Figure 4-3. Dual H-bridge Mode, DDW Package, Top View

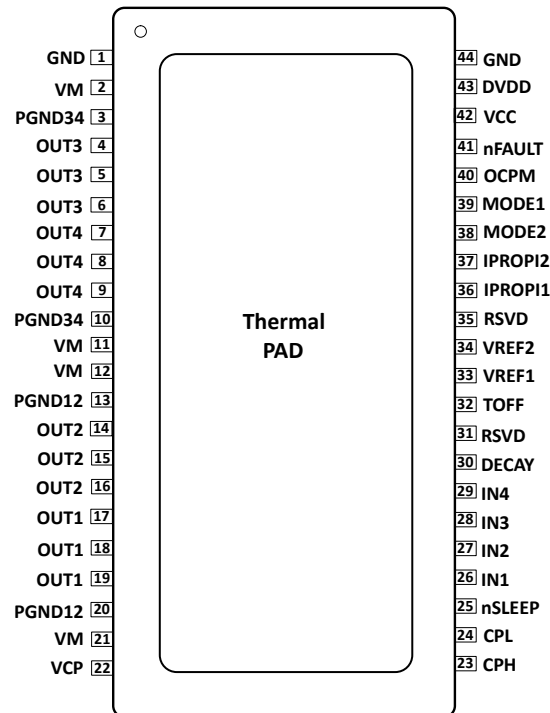


Figure 4-4. Dual H-bridge Mode, DDV Package, Top View

Table 4-1. Pin Configuration

PIN				TYPE	DESCRIPTION
NAME		DDW	DDV		
Single H-Bridge	Dual H-Bridge				
RSVD	IN4	38	29	Input	PWM input for H-bridge 2 in dual H-bridge mode. Leave this pin unconnected in single H-bridge mode.
RSVD	IN3	39	28	Input	PWM input for H-bridge 2 in dual H-bridge mode. Leave this pin unconnected in single H-bridge mode.
IPROPI	IPROPI2	30	37	Output	Analog current output for H-bridge 2 in dual H-bridge mode. Connect to the other IPROPI pin in single H-bridge mode.
IPROPI	IPROPI1	31	36	Output	Analog current output for H-bridge 1 in dual H-bridge mode. Connect to the other IPROPI pin in single H-bridge mode.
VREF	VREF2	33	34	Input	Reference input to set current for H-bridge 2 in dual H-bridge mode. Tie to the other VREF pin in single H-bridge mode. DVDD can be used to provide VREF through a resistor divider.
VREF	VREF1	34	33	Input	Reference input to set current for H-bridge 1 in dual H-bridge mode. Tie to the other VREF pin in single H-bridge mode. DVDD can be used to provide VREF through a resistor divider.
OUT1	OUT1	4, 5, 6	17, 18, 19	Output	Winding output. Connect to motor terminal.
OUT2	OUT2	7, 8, 9	14, 15, 16	Output	Winding output. Connect to motor terminal.
OUT1	OUT3	17, 18, 19	4, 5, 6	Output	Winding output. Connect to motor terminal.
OUT2	OUT4	14, 15, 16	7, 8, 9	Output	Winding output. Connect to motor terminal.
PGND	PGND12	3, 10	13, 20	Power	Power ground for H-bridge. Connect to system ground.
PGND	PGND34	13, 20	3, 10	Power	Power ground for H-bridge. Connect to system ground.
IN2		40	27	Input	PWM input for H-bridge 1.
IN1		41	26	Input	PWM input for H-bridge 1.
RSVD		36	31	-	Reserved. Leave Unconnected.
DECAY		37	30	Input	Decay setting pin.
TOFF		35	32	Input	PWM OFF time setting pin.
OCPM		27	40	Input	Determines the fault recovery method. Depending on the OCPM voltage, fault recovery can be either latch-off or auto-retry.
VCP		1	22	Power	Charge pump output. Connect a X7R, 1 μ F, 16V ceramic capacitor to VM.
VM		2, 11, 12, 21	2, 11, 12, 21	Power	Power supply. Connect to supply voltage and bypass to PGND with two 0.01 μ F ceramic capacitors plus a bulk capacitor rated for VM.
GND		22, 23	1, 44	Power	Device ground. Connect to system ground.
CPH		44	23	Power	Charge pump switching node. Connect a X7R, 0.1 μ F, VM rated ceramic capacitor from CPH to CPL.
CPL		43	24		
DVDD		24	43	Power	Internal LDO output. Connect a X7R, 0.47 μ F to 1 μ F, 6.3V or 10V rated ceramic capacitor to GND.
VCC		25	42	Power	Supply voltage for internal logic blocks. When no separate supply voltage is available, tie the VCC pin to the DVDD output.
nFAULT		26	41	Open Drain	Fault indication. Pulled logic low with fault condition; open drain output requires an external pullup resistor.
MODE1		28	39	Input	This pin selects between dual H-bridge and single H-bridge modes of operation.

Table 4-1. Pin Configuration (continued)

PIN				TYPE	DESCRIPTION
NAME		DDW	DDV		
Single H-Bridge	Dual H-Bridge				
MODE2		29	38	Input	This pin selects the interface - between Phase/Enable (PH/EN) and PWM (IN/IN). When this pin is grounded, the device operates with PH/EN interface. To configure PWM interface, see Section 6.4 for details.
nSLEEP		42	25	Input	Sleep mode input. Logic high to enable device; logic low to enter low-power sleep mode. An nSLEEP low pulse clears latched faults.
RSVD		32	35	-	Reserved. Leave Unconnected.
PAD		-	-	-	Thermal pad.

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted). ^{1 2}

	MIN	MAX	UNIT
Power supply voltage (VM)	-0.3	70	V
Charge pump voltage (VCP, CPH)	-0.3	$V_{VM} + 5.75$	V
Charge pump negative switching pin (CPL)	-0.3	V_{VM}	V
nSLEEP pin voltage (nSLEEP)	-0.3	V_{VM}	V
Internal regulator voltage (DVDD)	-0.3	5.75	V
External logic supply (VCC)	-0.3	5.75	V
IPROPI pin voltage (IPROPI)	-0.3	$DVDD + 0.3$	V
Control pin voltage	-0.3	5.75	V
Open drain output current (nFAULT)	0	10	mA
Reference input pin voltage (VREF)	-0.3	5.75	V
PGNDx to GND voltage	-0.5	0.5	V
PGNDx to GND voltage, < 1 μ s	-2.5	2.5	V
Continuous OUTx pin voltage	-1	$V_{VM} + 1$	V
Transient 100ns OUTx pin voltage	-3	$V_{VM} + 3$	V
Peak drive current	Internally Limited		A
Operating ambient temperature, T_A	-40	125	$^{\circ}$ C
Operating junction temperature, T_J	-40	150	$^{\circ}$ C
Storage temperature, T_{stg}	-65	150	$^{\circ}$ C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values are with respect to network ground terminal GND.

5.2 ESD Ratings

			VALUE	UNIT	
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ¹	± 2000	V	
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ²	Corner pins		± 750
			Other pins		± 500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{VM}	Supply voltage range for normal (DC) operation	4.5	60	V
V_I	Logic level input voltage	0	5.5	V
V_{VCC}	VCC pin voltage	3.05	5.5	V
V_{REF}	Reference voltage (VREF)	0.05	3.3	V
$I_{RMS,DUAL,DDW}$	RMS current, dual H-bridge mode, DDW Package	0	5	A
$I_{RMS,DUAL,DDV}$	RMS current, dual H-bridge mode, DDV Package	0	10	A
$I_{RMS,SINGLE,DDW}$	RMS current, single H-bridge mode, DDW Package	0	10	A
$I_{RMS,SINGLE,DDV}$	RMS current, single H-bridge mode, DDV Package	0	20	A
T_A	Operating ambient temperature	-40	125	°C
T_J	Operating junction temperature	-40	150	°C

5.4 Thermal Information

THERMAL METRIC		DDW	DDV	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	22.2	44.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	9.1	0.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.3	18.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.1	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	5.3	18.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.7	N/A	°C/W

For the DDV package, as the exposed pad is on top of the package, $R_{\theta JC(top)}$ is the most important thermal resistance parameter.

5.4.1 Transient Thermal Impedance & Current Capability

Information based on thermal simulations

Table 5-1. Transient Thermal Impedance ($R_{\theta JA}$) and Current Capability

$R_{\theta JA}$ [°C/W] ⁽¹⁾				Configuration	Current (A) ⁽²⁾					
					without PWM ⁽³⁾				with PWM ⁽⁴⁾	
0.1 sec	1 sec	10 sec	DC		0.1 sec	1 sec	10 sec	DC	10 sec	DC
1.8	4.7	8.4	23.3	Dual H-Bridge (both outputs loaded with same current)	8	5.7	4.2	2.5	4	2.2
				Dual H-Bridge (only one output loaded)	8	8	6	3.5	5.4	3
				Single H-Bridge	16	11.3	8.4	4.9	7.9	4.4

(1) Simulated using 114.3mm x 76.2mm x 1.6mm 4 layer PCB – 2oz Cu on top and bottom layers, 1oz Cu on internal planes, 16cm² top and bottom layer Cu area, with 13 x 5 thermal via array below thermal pad, 1.1mm pitch, 0.2mm diameter, 0.025mm Cu plating.

(2) Estimated transient current capability at 85 °C ambient temperature for junction temperature rise up to 150°C.

(3) Only conduction losses (I^2R) and quiescent current loss at 48V supply voltage are considered. Maximum ON resistance values at 150°C as per Electrical Characteristics table are considered to calculate conduction losses.

(4) Switching loss estimated by the equation: $P_{SW} = V_{VM} \times I_{Load} \times f_{PWM} \times t_{RF}$, where $V_{VM} = 48V$, $f_{PWM} = 20KHz$, $t_{RF} = 110ns$

5.5 Electrical Characteristics

Typical values are at $T_A = 25^\circ\text{C}$. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, DVDD)						
I_{VM}	VM operating supply current	nSLEEP = 1, No load, VCC = External 5V		5	8	mA
		nSLEEP = 1, No motor load, VCC = DVDD		8.5	13	
I_{VMQ}	VM sleep mode supply current	nSLEEP = 0		3	8	μA
t_{SLEEP}	Sleep time	nSLEEP = 0 to sleep-mode	120			μs
t_{RESET}	nSLEEP reset pulse	nSLEEP low to clear fault	20		40	μs
t_{WAKE}	Wake-up time	nSLEEP = 1 to output transition		0.75	1	ms
t_{ON}	Turn-on time	VM > UVLO to output transition		0.8	1.3	ms
V_{DVDD}	Internal regulator voltage	No external load, $6\text{V} < V_{VM} < 60\text{V}$	4.75	5	5.25	V
		No external load, $V_{VM} = 4.5\text{V}$	4.3	4.45		V
CHARGE PUMP (VCP, CPH, CPL)						
V_{VCP}	VCP operating voltage	$6\text{V} < V_{VM} < 60\text{V}$		$V_{VM} + 5$		V
$f_{(VCP)}$	Charge pump switching frequency	$V_{VM} > UVLO$; nSLEEP = 1		360		kHz
LOGIC-LEVEL INPUTS (IN1, IN2, IN3, IN4, OCPM, MODE1, MODE2, nSLEEP)						
V_{IL}	Input logic-low voltage		0		0.6	V
V_{IH}	Input logic-high voltage		1.5		5.5	V
V_{HYS}	Input logic hysteresis			100		mV
V_{HYS_nSLEEP}	nSLEEP logic hysteresis			300		mV
I_{IL}	Input logic-low current (except MODE2)	$V_{IN} = 0\text{V}$	-1		1	μA
I_{IH}	Input logic-high current (except MODE2)	$V_{IN} = 5\text{V}$			50	μA
R_{PU}	MODE2 internal pull-up resistor			220		k Ω
t_{PDH}^1	INx high to OUTx high propagation delay			600		ns
t_{PDL}^1	INx low to OUTx low propagation delay			600		ns
TRI-LEVEL INPUTS (DECAY)						
V_{I1}	Input logic-low voltage	Tied to GND	0		0.6	V
V_{I2}	Input Hi-Z voltage	Hi-Z (>500k Ω to GND)	1.8	2	2.2	V
V_{I3}	Input logic-high voltage	Tied to DVDD	2.7		5.5	V
I_O	Output pull-up current			10.5		μA
QUAD-LEVEL INPUTS (TOFF)						
V_{I1}	Input logic-low voltage	Tied to GND	0		0.6	V
V_{I2}		330k $\Omega \pm 5\%$ to GND	1	1.25	1.4	V
V_{I3}	Input Hi-Z voltage	Hi-Z (>500k Ω to GND)	1.8	2	2.2	V
V_{I4}	Input logic-high voltage	Tied to DVDD	2.7		5.5	V
I_O	Output pull-up current			10.5		μA
CONTROL OUTPUTS (nFAULT)						
V_{OL}	Output logic-low voltage	$I_O = 5\text{mA}$			0.3	V

Typical values are at $T_A = 25^\circ\text{C}$. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OH}	Output logic-high leakage		-1		1	μA
MOTOR DRIVER OUTPUTS (OUT1, OUT2, OUT3, OUT4)						
$R_{DS(OH_DUAL)}$	Dual H-bridge, High-side FET on resistance	$T_J = 25^\circ\text{C}, I_O = -5\text{A}$		50	60	$\text{m}\Omega$
		$T_J = 125^\circ\text{C}, I_O = -5\text{A}$		75	94	$\text{m}\Omega$
		$T_J = 150^\circ\text{C}, I_O = -5\text{A}$		85	107	$\text{m}\Omega$
$R_{DS(ONL_DUAL)}$	Dual H-bridge, Low-side FET on resistance	$T_J = 25^\circ\text{C}, I_O = 5\text{A}$		50	60	$\text{m}\Omega$
		$T_J = 125^\circ\text{C}, I_O = 5\text{A}$		72	90	$\text{m}\Omega$
		$T_J = 150^\circ\text{C}, I_O = 5\text{A}$		80	100	$\text{m}\Omega$
$R_{DS(OH_SINGLE)}$	Single H-bridge, High-side FET on resistance	$T_J = 25^\circ\text{C}, I_O = -5\text{A}$		25	30	$\text{m}\Omega$
		$T_J = 125^\circ\text{C}, I_O = -5\text{A}$		38	47	$\text{m}\Omega$
		$T_J = 150^\circ\text{C}, I_O = -5\text{A}$		43	54	$\text{m}\Omega$
$R_{DS(ONL_SINGLE)}$	Single H-bridge, Low-side FET on resistance	$T_J = 25^\circ\text{C}, I_O = 5\text{A}$		25	30	$\text{m}\Omega$
		$T_J = 125^\circ\text{C}, I_O = 5\text{A}$		36	45	$\text{m}\Omega$
		$T_J = 150^\circ\text{C}, I_O = 5\text{A}$		40	50	$\text{m}\Omega$
I_{LEAK}	Output leakage current to GND	Sleep-mode, H-bridges are Hi-Z, $V_{VM} = 60\text{V}$			300	μA
t_{RF}	Output rise/fall time	$I_O = 5\text{A}$, between 10% and 90%		110		ns
t_D	Output dead time	$V_M = 24\text{V}, I_O = 5\text{A}$		300		ns
CURRENT SENSE AND REGULATION (IPROPI, VREF)						
A_{IPROPI}	Current mirror gain			212		$\mu\text{A}/\text{A}$
A_{ERR}	Current mirror scaling error	10% to 20% rated current	-12		12	%
		20% to 40% rated current	-7		7	
		40% to 100% rated current	-4		4	
I_{VREF}	VREF Leakage Current	$V_{REF} = 3.3\text{V}$			30	nA
t_{OFF}	PWM off-time	$TOFF = 0$		7		μs
		$TOFF = 1$		16		
		$TOFF = \text{Hi-Z}$		24		
		$TOFF = 330\text{k}\Omega$ to GND		32		
t_{DEG}	Current regulation deglitch time			0.5		μs
t_{BLK}	Current Regulation Blanking time			1.5		μs
PROTECTION CIRCUITS						
V_{UVLO}	VM UVLO lockout	VM falling	4.1	4.25	4.35	V
		VM rising	4.2	4.35	4.45	
V_{CCUVLO}	VCC UVLO lockout	VCC falling	2.7	2.8	2.9	V
		VCC rising	2.8	2.9	3.05	
$V_{UVLO,HYS}$	Undervoltage hysteresis	Rising to falling threshold		100		mV
V_{CPOV}	Charge pump undervoltage	VCP falling		$V_{VM} + 2$		V
I_{OCP}	Overcurrent protection, DDW Package	Dual H-bridge, Current through any FET, DDW Package	8			A
		Single H-bridge, Current through any FET, DDW Package	16			A

Typical values are at $T_A = 25^\circ\text{C}$. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
I_{OCP}	Overcurrent protection, DDV Package	16			A	
	Single H-bridge, Current through any FET, DDV Package	32			A	
t_{OCP}	Overcurrent detection delay		2.1		μs	
t_{RETRY}	Overcurrent retry time		4.1		ms	
T_{OTSD}	Thermal shutdown	Die temperature T_J	150	165	180	$^\circ\text{C}$
$T_{\text{HYS_OTSD}}$	Thermal shutdown hysteresis	Die temperature T_J		20		$^\circ\text{C}$

(1) Verified by design.

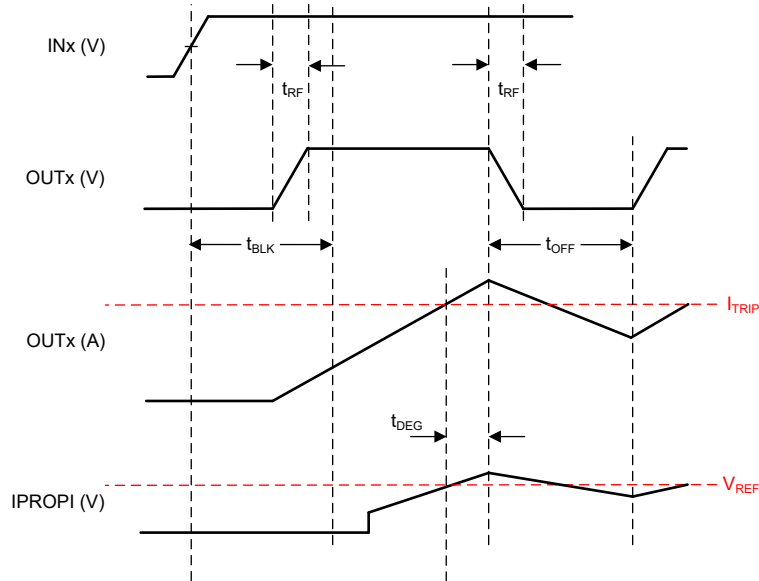


Figure 5-1. IPROPI Timing Diagram

5.6 Typical Characteristics

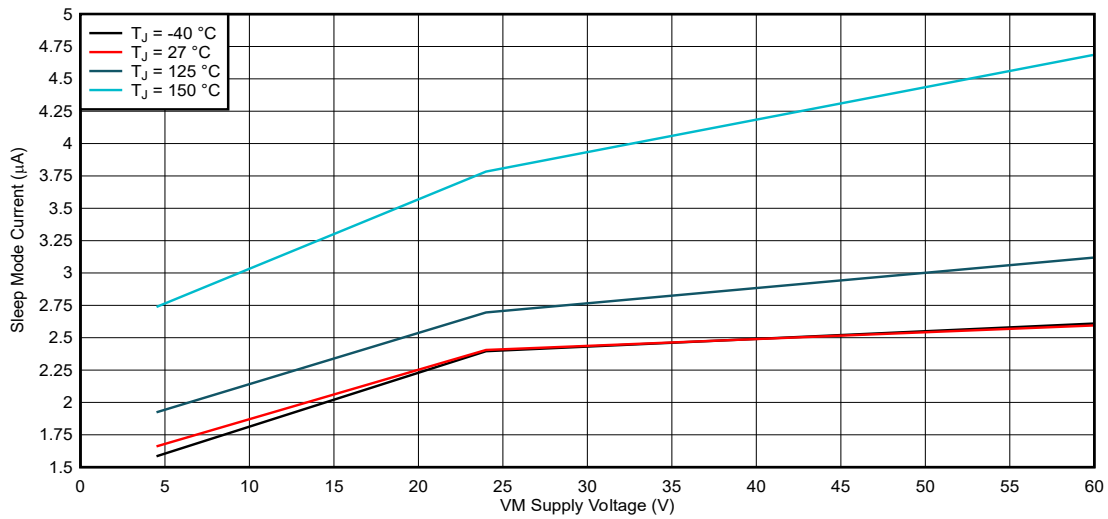


Figure 5-2. Sleep Mode Supply Current

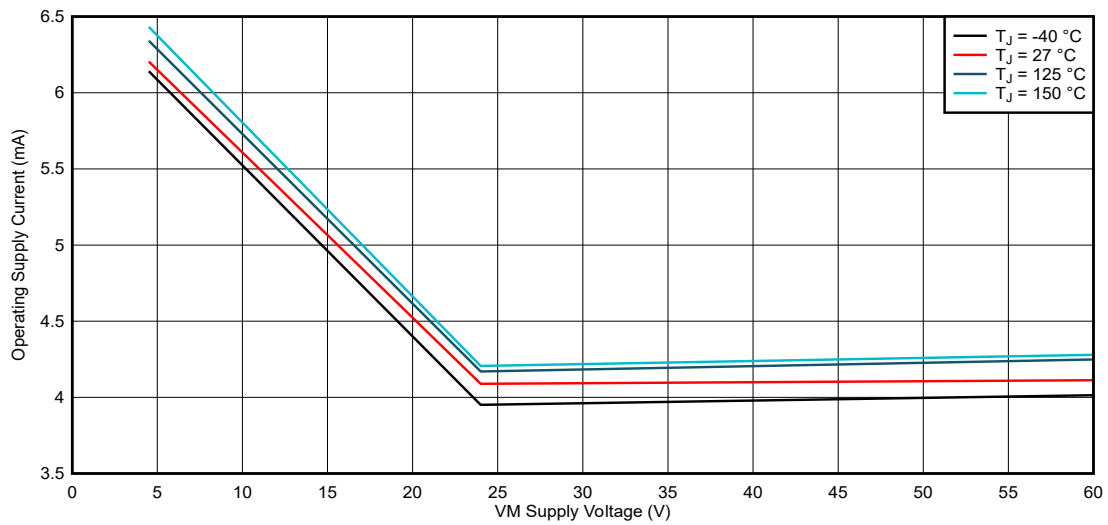


Figure 5-3. Operating Supply Current, VCC = External 5V

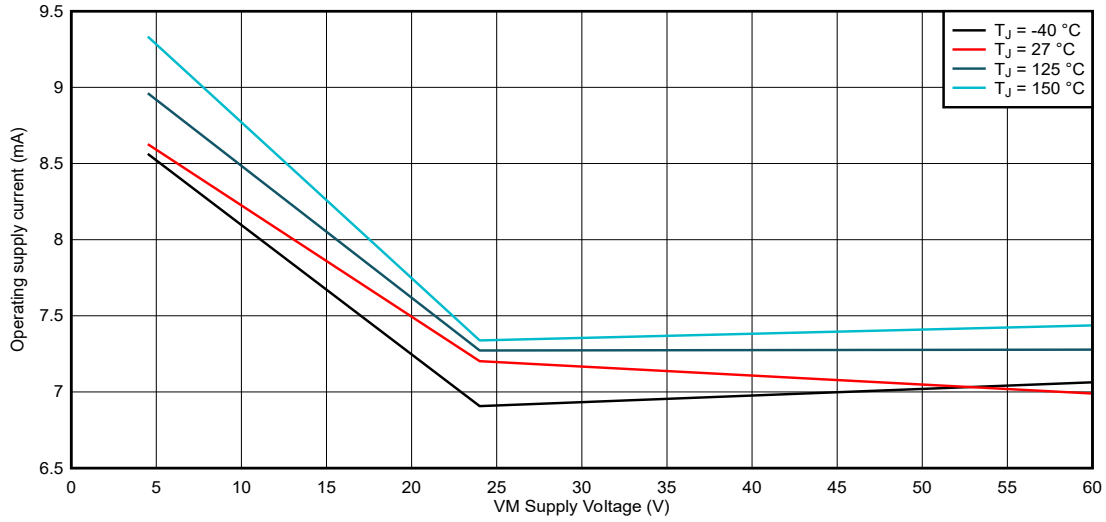


Figure 5-4. Operating Supply Current, VCC = DVDD

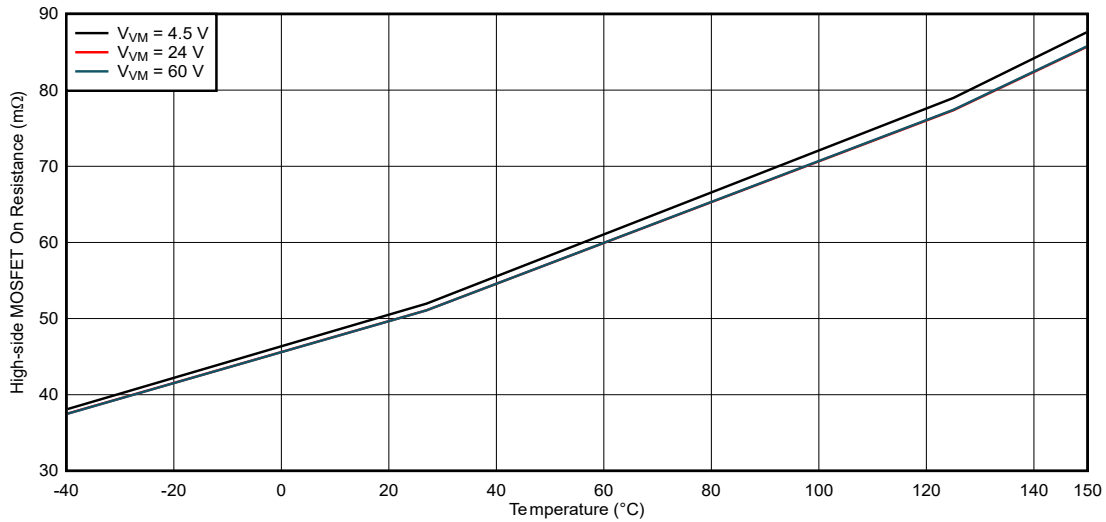


Figure 5-5. High-side FET on Resistance, Dual H-bridge Mode

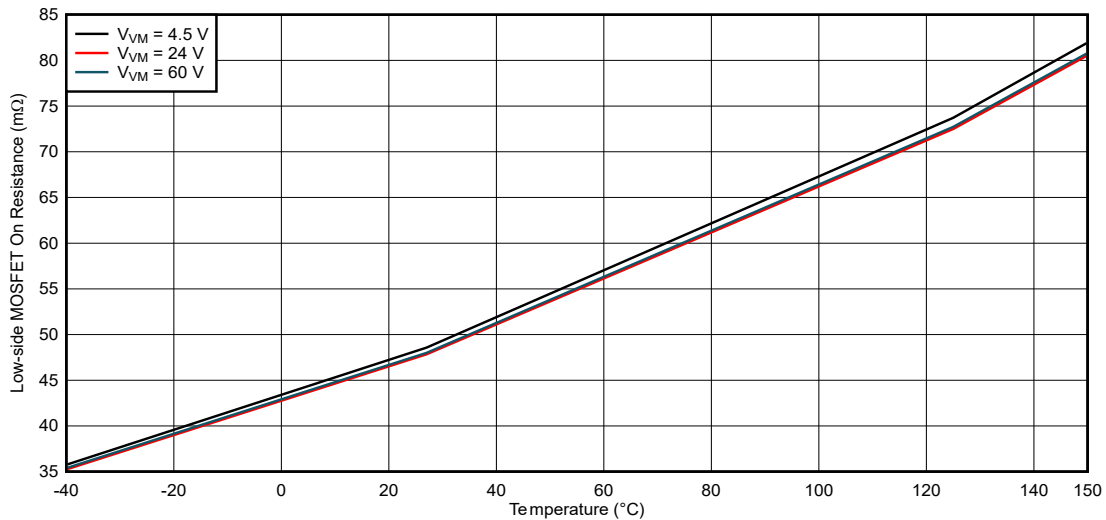


Figure 5-6. Low-side FET on Resistance, Dual H-bridge Mode

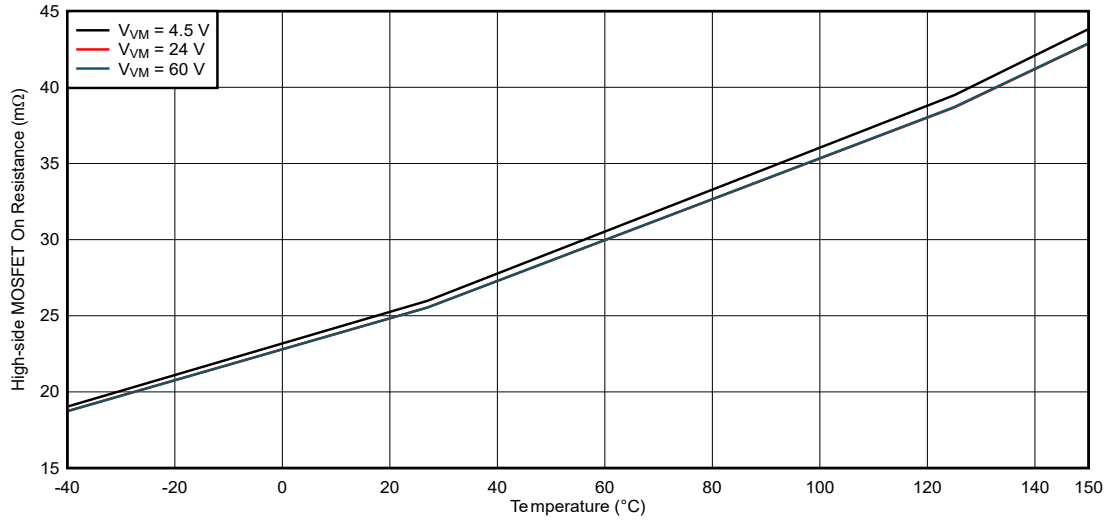


Figure 5-7. High-side FET on Resistance, Single H-bridge Mode

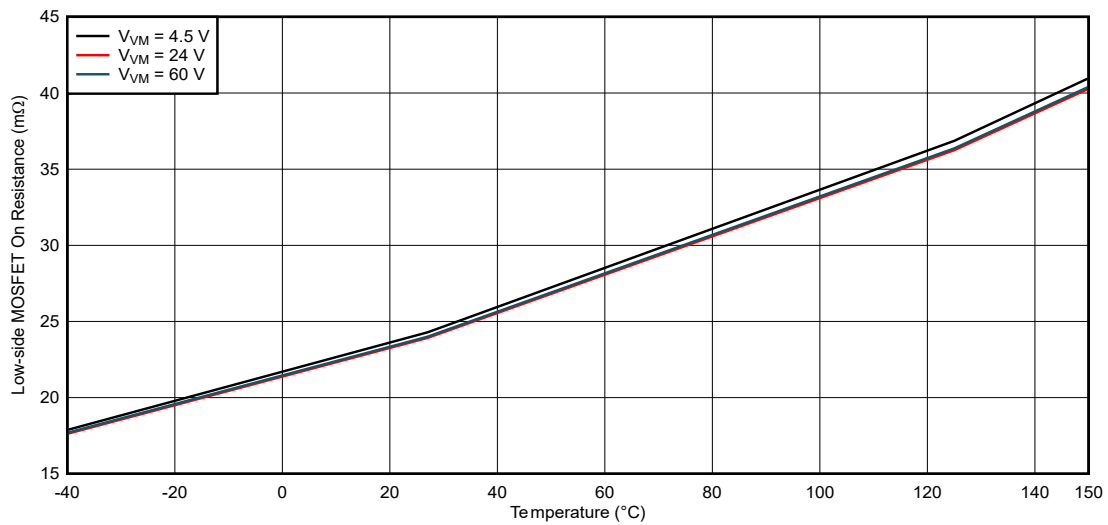


Figure 5-8. Low-side FET on Resistance, Single H-bridge Mode

6 Detailed Description

6.1 Overview

The DRV8262 is a H-Bridge motor driver that operates from 4.5V to 60V and supports up to 32A peak motor currents for various types of motors and loads. The device integrates two H-bridge output power stages to drive two brushed-DC motors. The H-bridges can be paralleled to provide a higher current to a single brushed-DC motor. The number of H-bridges and the interface of operation are selected by the MODE1 and MODE2 pin settings.

The device integrates a charge pump to efficiently drive high-side N-channel MOSFETs with 100% duty cycle. The device can operate from a single power supply input (VM). Alternatively, the VCC pin can be connected to a second power supply to provide power to the internal logic blocks. The nSLEEP pin provides an ultra-low power mode to minimize current drawn during system inactivity.

The device is available in two packages - a 44-pin HTSSOP (DDW) package with an exposed pad at the bottom of the package; and another 44-pin HTSSOP (DDV) package with an exposed pad on the top of the package. In the dual H-bridge mode, the DDW package delivers up to 8A peak current per output; and the DDV package delivers up to 16A peak current per output. In single H-bridge mode, the DDW and DDV packages deliver up to 16A and 32A peak current respectively. The actual current that can be delivered depends on the ambient temperature, supply voltage, and PCB thermal design.

The device integrates current sense outputs. The IPROPI pins source a small current that is proportional to the current in the high-side MOSFETs. The current from the IPROPI pins can be converted to a proportional voltage using an external resistor (R_{IPROPI}). The integrated current sensing allows the DRV8262 to limit the output current with a fixed off-time PWM chopping scheme and provide load information to the external controller to detect changes in load or stall conditions. The sensing accuracy of the IPROPI output is $\pm 4\%$ for 40% to 100% of the rated current. External power sense resistors can also be connected if higher accuracy sensing is required. The current regulation level can be configured during operation through the VREF pin to limit the load current according to the system's demands.

A variety of integrated protection features protect the device in the case of a system fault. These include undervoltage lockout (UVLO), charge pump undervoltage (CPUV), over current protection (OCP), and over temperature shutdown (OTSD). Fault conditions are indicated on the nFAULT pin.

6.2 Functional Block Diagram

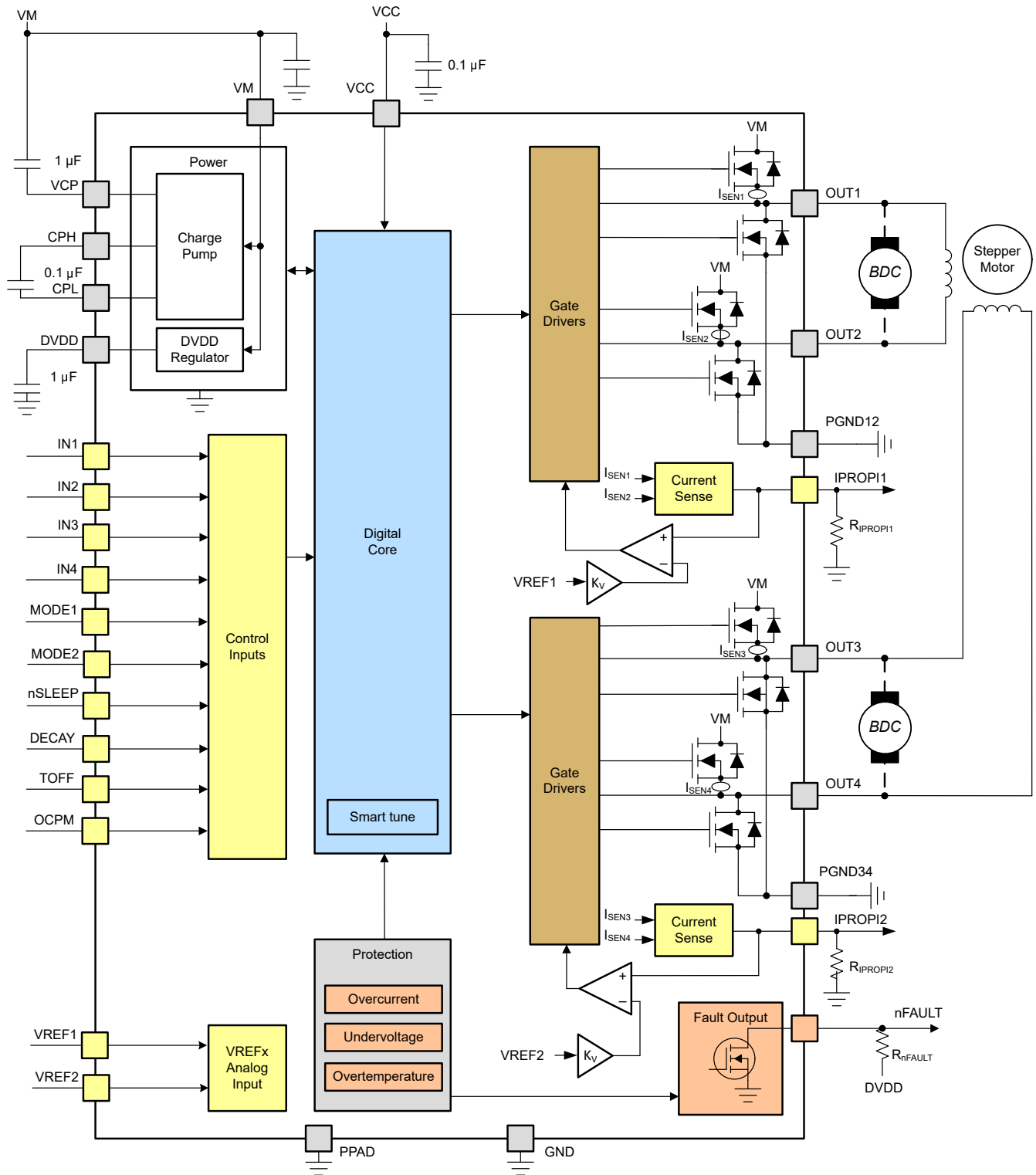


Figure 6-1. Dual H-Bridge Block Diagram

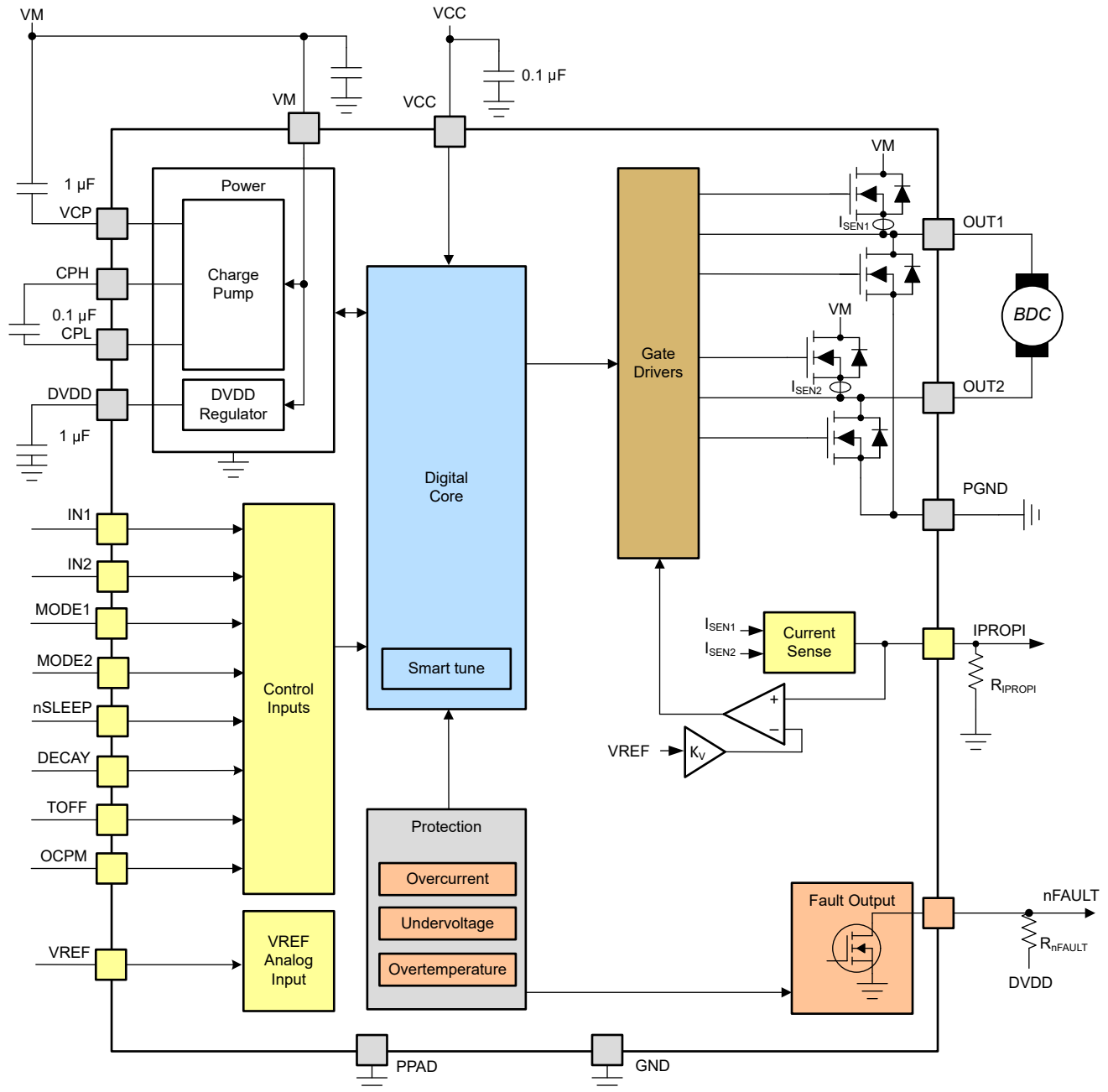


Figure 6-2. Single H-Bridge Block Diagram

6.3 Feature Description

The following table shows the recommended values of the external components for the driver.

Table 6-1. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	PGND12	X7R, 0.01 μ F, VM-rated ceramic capacitor
C_{VM2}	VM	PGND34	X7R, 0.01 μ F, VM-rated ceramic capacitor
C_{VM3}	VM	PGND12	Bulk, VM-rated capacitor
C_{VCP}	VCP	VM	X7R, 1 μ F, 16V ceramic capacitor
C_{SW}	CPH	CPL	X7R, 0.1 μ F, VM-rated ceramic capacitor
C_{DVDD}	DVDD	GND	X7R, 1 μ F, 10V rated ceramic capacitor
C_{VCC}	VCC	GND	X7R, 0.1 μ F, 6.3V or 10V rated ceramic capacitor
R_{nFAULT}	DVDD or VCC	nFAULT	10k Ω resistor
R_{REF1}	VREFx	DVDD	Resistor to set current regulation threshold.
R_{REF2}	VREFx	GND	
$R_{IPROPIx}$	IPROPIx	GND	For details, see Section 6.5.2

6.3.1 Spread Spectrum

Spread spectrum or frequency dithering is used to reduce the effect of EMI by converting a narrowband signal into a wideband signal, which spreads the energy across multiple frequencies. [Figure 6-3](#) illustrates how manipulating the clock frequency over time has the effect of spreading the energy.

In the context of the DRV8262, the frequencies of the internal clock for digital circuits (10MHz typical) and the clock for charge pump (357kHz typical) are manipulated to reduce the peak energy and is distributed to other frequencies and harmonics. Spread spectrum combined with output slew rate control minimize the radiated emissions from the device and help pass strict EMI standards.

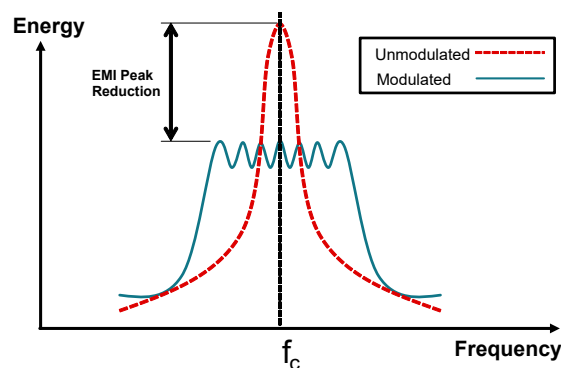


Figure 6-3. EMI Reduction by Spread Spectrum, Frequency Modulation

When the DRV8262 is powered up, spread spectrum is enabled. There are many ways to implement spread spectrum. The DRV8262 uses the triangular analog modulation profile. [Figure 6-4](#) and [Figure 6-5](#) shows the spread spectrum profiles of the internal digital clock and the charge pump clock around the respective center frequencies. The digital clock varies by equal amounts over 14 steps between 9MHz and 11MHz.

Note

The center frequencies themselves vary with process and temperature changes, and the variations due to spread spectrum are in addition to those.

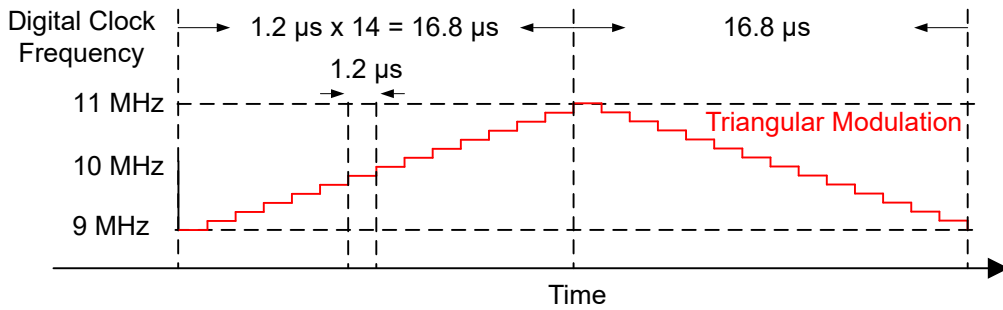


Figure 6-4. Triangular Spread Spectrum of Internal Digital Clock

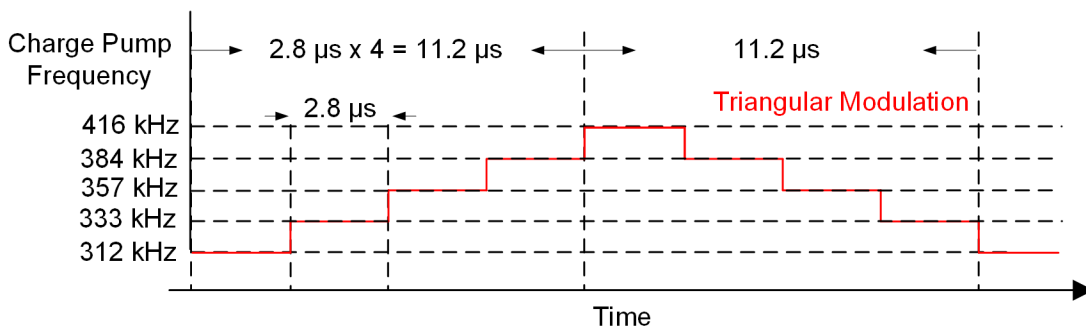


Figure 6-5. Triangular Spread Spectrum of Charge Pump Clock

6.4 Device Operational Modes

The DRV8262 supports dual or single H-bridge with PH/EN or PWM interface. The mode of operation is selected by the MODE1 and MODE2 pins as shown in [Table 6-2](#).

- The MODE1 and MODE2 pin states are latched when the device is enabled through the nSLEEP pin or at power-up.
- The MODE2 pin has to be grounded to select PH/EN interface.
- To select PWM interface, keep MODE2 pin floating or connect the MODE2 pin to DVDD.

Table 6-2. Modes of Operation

MODE1	MODE2	Dual or Single H-bridge	Interface
0	0	Dual	PH/EN
	Floating or DVDD	Dual	PWM
1	0	Single	PH/EN
	Floating or DVDD	Single	PWM

The INx inputs can be set to static voltages for 100% duty cycle drive, or the INx inputs can be pulse-width modulated for variable motor speed. The input pins can be powered before VM supply is applied.

[Section 6.4.1](#) and [Section 6.4.2](#) show the truth tables for each interface. Note that the tables do not take into account the internal current regulation feature. Additionally, the DRV8262 automatically handles the dead time generation when switching between the high-side and low-side MOSFETs of a H-bridge.

6.4.1 Dual H-Bridge Mode (MODE1 = 0)

- If the MODE1 pin is logic low at power up, the device is latched into dual H-bridge mode.

- Two brushed-DC motors or a stepper motor can be driven in this mode.
- The MODE2 pin configures the interface of operation between PH/EN and PWM.
 - PH/EN mode allows the H-bridge to be controlled with a speed and direction type of interface.
 - PWM interface allows the H-bridge outputs to become Hi-Z without making the nSLEEP pin logic low.

The truth tables for dual H-bridge mode are shown in [Table 6-3](#) and [Table 6-4](#).

Table 6-3. Dual H-Bridge with PH/EN Interface

nSLEEP	IN1/IN3	IN2/IN4	OUT1/OUT3	OUT2/OUT4	DESCRIPTION
0	X	X	Hi-Z	Hi-Z	Sleep
1	0	X	H	H	Brake (High-Side Slow Decay)
1	1	0	L	H	Reverse (OUT2/4 -> OUT1/3)
1	1	1	H	L	Forward (OUT1/3 -> OUT2/4)

Table 6-4. Dual H-Bridge with PWM Interface

nSLEEP	IN1/IN3	IN2/IN4	OUT1/OUT3	OUT2/OUT4	DESCRIPTION
0	X	X	Hi-Z	Hi-Z	Sleep
1	0	0	Hi-Z	Hi-Z	Coast (H-Bridge outputs Hi-Z)
1	0	1	L	H	Reverse (OUT2/4 -> OUT1/3)
1	1	0	H	L	Forward (OUT1/3 -> OUT2/4)
1	1	1	H	H	Brake (High-Side Slow Decay)

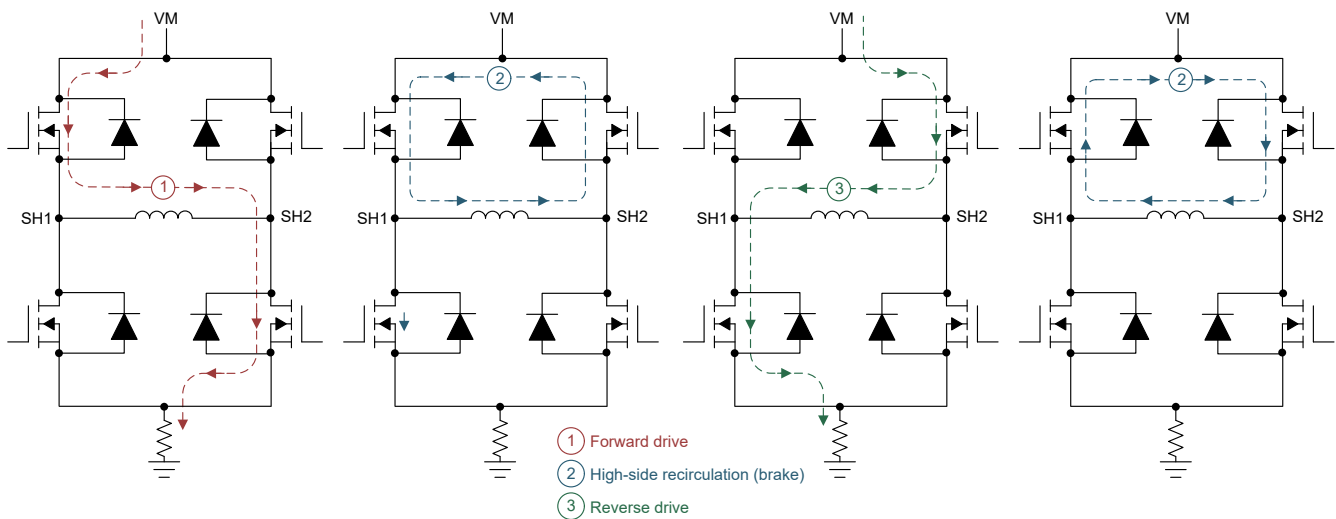


Figure 6-6. Current Paths

6.4.2 Single H-Bridge Mode (MODE1 = 1)

When the MODE1 pin is logic High on power up, the device is latched into single H-bridge mode. The device drives one brushed-DC motor in this mode. The truth table for single H-bridge mode is shown in [Table 6-5](#) and [Table 6-6](#).

Table 6-5. Single H-Bridge with PH/EN Interface

nSLEEP	IN1	IN2	OUT1/3	OUT2/4	DESCRIPTION
0	X	X	Hi-Z	Hi-Z	Sleep
1	0	X	H	H	Brake (High-Side Slow Decay)

Table 6-5. Single H-Bridge with PH/EN Interface (continued)

nSLEEP	IN1	IN2	OUT1/3	OUT2/4	DESCRIPTION
1	1	0	L	H	Reverse (OUT2/4 -> OUT1/3)
1	1	1	H	L	Forward (OUT1/3 -> OUT2/4)

Table 6-6. Single H-Bridge with PWM Interface

nSLEEP	IN1	IN2	OUT1/OUT3	OUT2/OUT4	DESCRIPTION
0	X	X	Hi-Z	Hi-Z	Sleep
1	0	0	Hi-Z	Hi-Z	Coast (H-bridge outputs Hi-Z)
1	0	1	L	H	Reverse (OUT2/4 -> OUT1/3)
1	1	0	H	L	Forward (OUT1/3 -> OUT2/4)
1	1	1	H	H	Brake (High-Side Slow Decay)

6.5 Current Sensing and Regulation

The device integrates current sensing across high-side MOSFETs, current regulation, and current sense feedback. These features allow the device to sense the motor current without an external sense resistor or current sense circuitry; reducing system size, cost, and complexity. This also allows the device to limit the motor current in the case of motor stall or high torque events and give detailed feedback to the controller about the load current through IPROPI outputs.

6.5.1 Current Sensing and Feedback

The device supports one IPROPI output when operating in the single H-bridge mode, and two IPROPI outputs when operating in the dual H-bridge mode.

The IPROPI pins output a current that is proportional to the current flowing in the high-side FETs of the H-bridge, scaled by the current mirror gain A_{IPROPI} . The IPROPI output current can be calculated by [Equation 1](#). The I_{HS1} and I_{HS2} in [Equation 1](#) are only valid when the current flows from drain to source in the high-side MOSFET. If current flows from source to drain, the value of I_{HS1} and I_{HS2} for that channel is zero. Because of this, the IPROPI pin does not represent the current when operating in a fast decay mode (coast mode) or low-side slow decay mode. The IPROPI pin represents the H-bridge current under forward drive, reverse drive, and high-side slow decay, thereby allowing for continuous current monitoring in typical brushed DC motor applications.

Even in coast mode, the current can be sampled by briefly re-enabling the driver in either drive or slow-decay modes and measuring the current before switching back to coast mode again.

$$I_{PROPI} = (I_{HS1} + I_{HS2}) \times A_{IPROPI} \quad (1)$$

Each IPROPI pin is connected to an external resistor (R_{IPROPI}) to ground to generate a proportional voltage (V_{IPROPI}) on the IPROPI pin with the I_{IPROPI} analog current output. This allows for the load current to be measured as the voltage drop across the R_{IPROPI} resistor with a standard analog to digital converter (ADC). The R_{IPROPI} resistor can be sized based on the expected load current in the application so that the full range of the controller ADC is utilized. The device implements an internal clamp circuit to limit V_{IPROPI} with respect to V_{VREF} on the VREF pin and protect the external ADC in case of output overcurrent or unexpected high current events.

The corresponding IPROPI voltage to the output current can be calculated by [Equation 2](#).

$$V_{IPROPI} (V) = I_{IPROPI} (A) \times R_{IPROPI} (\Omega) \quad (2)$$

The IPROPI voltage is less than the maximum recommended value of VREF, which is 3.3V. For the R_{IPROPI} resistor, 10%, 5%, 1% and 0.1% are all valid tolerance values. The typical recommendation is 1% for best trade off between performance and cost.

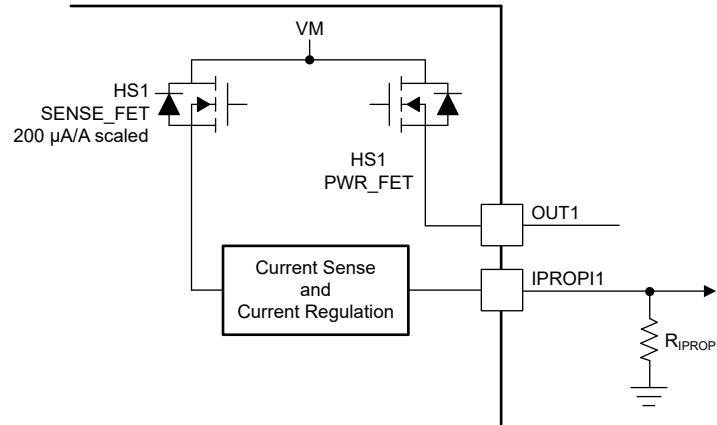


Figure 6-7. Integrated Current Sensing

The A_{ERR} parameter in the Electrical Characteristics table is the error of the A_{IPROPI} gain. The parameter indicates the combined effect of offset error added to the I_{OUT} current and gain error.

6.5.2 Current Regulation

The current chopping threshold (I_{TRIP}) is set through a combination of the V_{VREF} voltage (V_{VREF}) and IPROPI output resistor (R_{IPROPI}). This is done by comparing the voltage drop across the external R_{IPROPI} resistor to V_{VREF} with an internal comparator.

$$I_{TRIP} \times A_{IPROPI} = V_{VREF} (V) / R_{IPROPI} (\Omega) \tag{3}$$

For example, in the dual H-bridge mode, to set I_{TRIP} at 5A with V_{VREF} at 3.3V, R_{IPROPI} has to be -

$$R_{IPROPI} = V_{VREF} / (I_{TRIP} \times A_{IPROPI}) = 3.3 / (5 \times 212 \times 10^{-6}) = 3.09k\Omega$$

In the single H-bridge mode, connect the two IPROPI pins. In the dual H-bridge mode, there are two V_{VREF} pins, which allows setting separate current chopping thresholds for each brushed-DC motor.

The internal current regulation can be disabled by tying IPROPI to GND and setting the V_{VREF} pin voltage greater than GND (if current feedback is not required). If current feedback is required and current regulation is not required, set V_{VREF} and R_{IPROPI} such that V_{IPROPI} never reaches the V_{VREF} threshold.

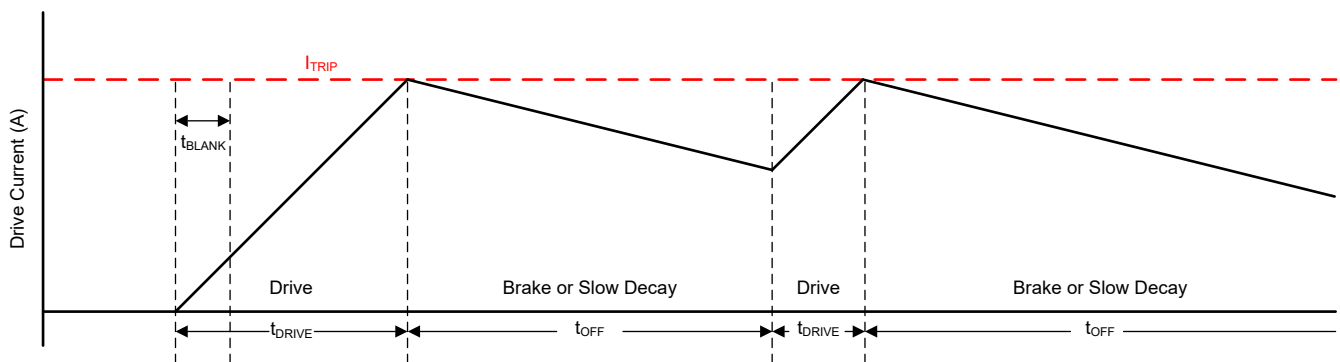


Figure 6-8. Current Regulation

The current through the motor windings is regulated by an adjustable off-time PWM current regulation circuit. During PWM current chopping, the H-bridge is enabled to drive through the motor winding until the PWM current chopping threshold is reached.

When the I_{TRIP} current has been reached, for single BDC or dual BDC applications, with the DECAY pin grounded, the device enforces slow current decay by enabling both the high-side FETs for a time of t_{OFF} , programmed by the TOFF pin.

When the t_{OFF} time has elapsed and the current level falls below the current regulation (I_{TRIP}) level, the output is re-enabled according to the inputs. If, after the t_{OFF} time has elapsed, the current is still higher than the I_{TRIP} level, the device enforces another t_{OFF} time period of the same duration. This "double t_{OFF} " time continues until the current is less than I_{TRIP} at the end of t_{OFF} time.

In current regulation, the inputs can be toggled to drive the load in the opposite direction to decay the current faster. For example, if the load is in forward drive before entering the current regulation the load can only go into reverse drive when the driver enforces current regulation.

For single or dual-BDC applications, the DECAY pin is kept grounded for high-side slow decay during t_{OFF} . For stepper applications, DECAY pin voltage is according to the desired decay mode. The decay mode is selected by the DECAY pin as shown in [Table 6-7](#).

Table 6-7. Decay Mode Settings

DECAY	DECAY MODE
0	Slow decay (brake or high-side re-circulation)
1	Smart tune dynamic decay
Hi-Z	Mixed decay: 30% fast

If the state of the INx control pin inputs changes during the t_{OFF} time, the remainder of the t_{OFF} time is ignored, and the outputs again follows the inputs. This is shown in [Figure 6-9](#).

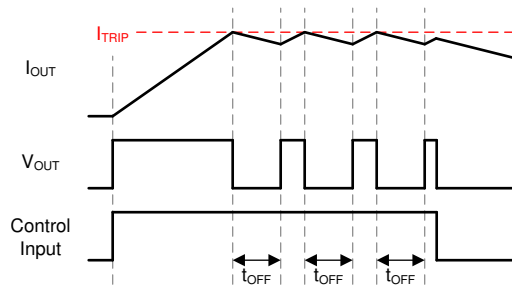


Figure 6-9. Current Regulation

As shown in [Table 6-8](#), the TOFF pin configures the PWM OFF time. The OFF time settings can be changed on the fly.

Table 6-8. Off-Time Settings

TOFF	OFF-TIME (t_{OFF})
0	7 μ s
1	16 μ s
Hi-Z	24 μ s
330k Ω to GND	32 μ s

6.5.2.1 Mixed Decay

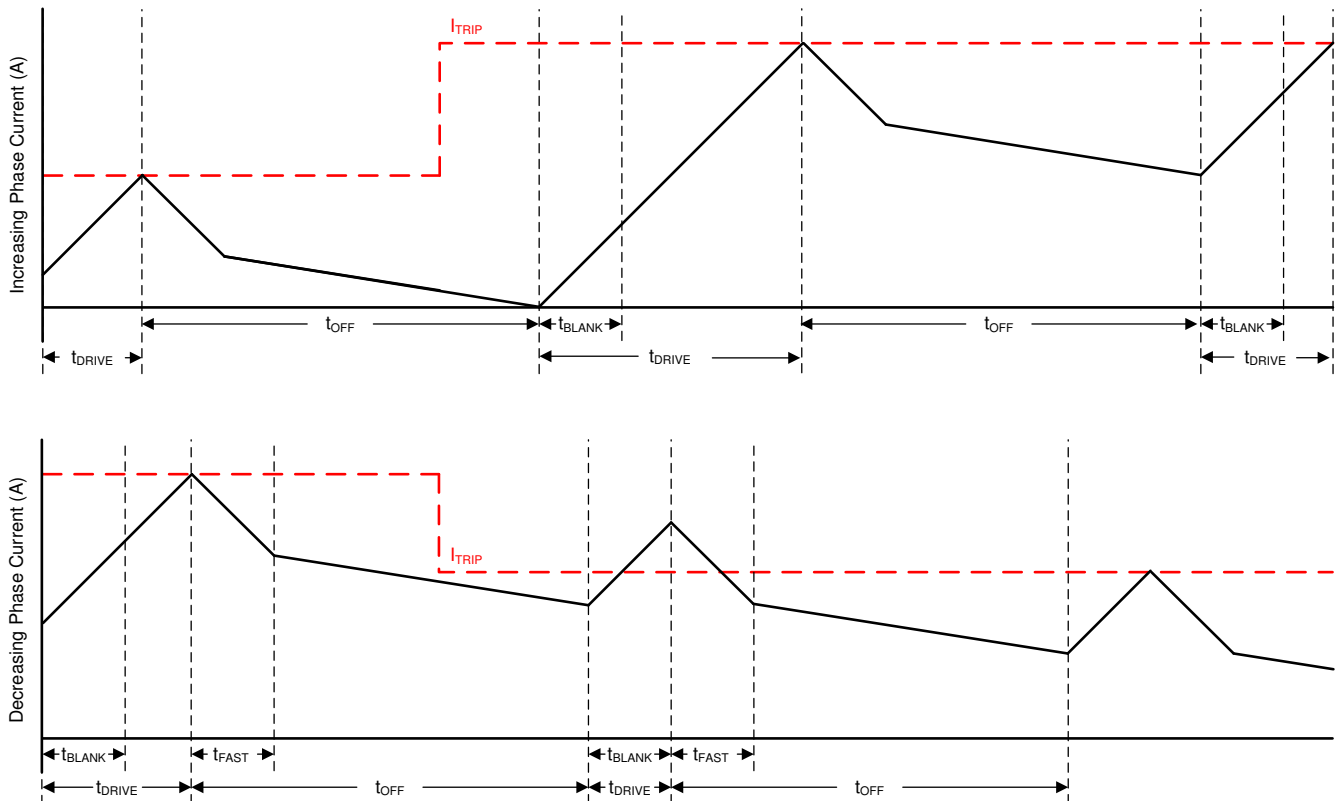


Figure 6-10. Mixed Decay Mode

Mixed decay begins as fast decay for 30% of t_{OFF} , followed by slow decay for the remainder of t_{OFF} .

6.5.2.2 Smart tune Dynamic Decay

The smart tune current regulation scheme is an advanced current-regulation control method compared to traditional fixed off-time current regulation schemes. Smart tune current regulation scheme helps the stepper motor driver adjust the decay scheme based on operating factors such as the ones listed as follows:

- Motor winding resistance and inductance
- Motor aging effects
- Motor dynamic speed and load
- Motor supply voltage variation
- Low-current versus high-current di/dt

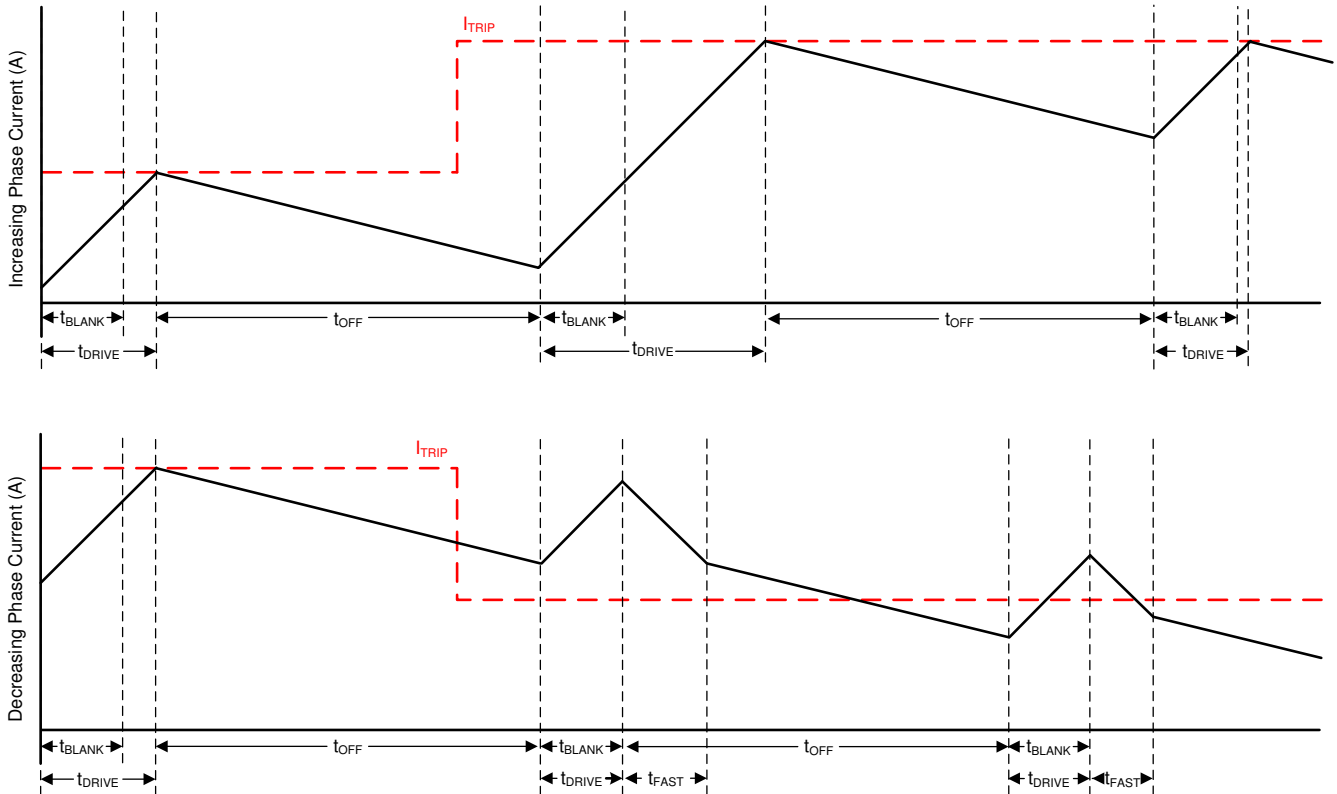


Figure 6-11. Smart tune Dynamic Decay Mode

Smart tune Dynamic Decay dynamically adjusts the fast decay percentage of the total mixed decay time. This feature eliminates motor tuning by automatically determining the best decay setting that results in the lowest ripple for the motor.

The decay mode setting is optimized iteratively each PWM cycle. If the motor current overshoots the target trip level, then the decay mode becomes more aggressive (add fast decay percentage) on the next cycle to prevent regulation loss. If a long drive time must occur to reach the target trip level, the decay mode becomes less aggressive (remove fast decay percentage) on the next cycle to operate with less ripple and more efficiently. On falling steps, smart tune Dynamic Decay automatically switches to fast decay to reach the next step quickly.

Smart tune Dynamic Decay is designed for applications that require minimal current ripple but want to maintain a fixed frequency in the current regulation scheme.

6.5.3 Current Sensing with External Resistor

The IPROPI output accuracy is $\pm 4\%$ for 40% to 100% of rated current. If more accurate current sensing is desired, external sense resistors can also be used between the PGND pins and the system ground to sense the load currents, as shown below.

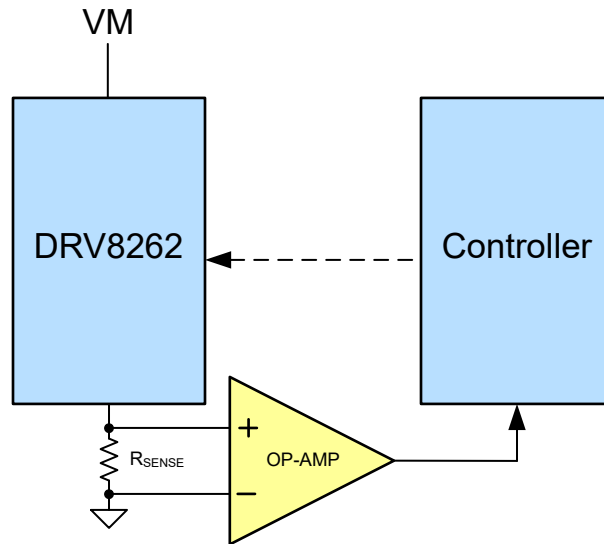


Figure 6-12. Current Sensing with External Resistor

The voltage drop across the external sense resistor does not exceed 300mV.

Place the sense resistors as close as possible to the corresponding IC pins. Use a symmetrical sense resistor layout to maintain good matching. Low-inductance sense resistors is used to prevent voltage spikes and ringing. For desired performance, the sense resistor is a surface-mount resistor rated for high enough power. Because power resistors are larger and more expensive than standard resistors, using multiple standard resistors in parallel is common practice. This distributes the current and heat dissipation.

6.6 Charge Pump

A charge pump is integrated to supply the high-side N-channel MOSFET gate-drive voltage. The charge pump requires a capacitor between the VM and VCP pins to act as the storage capacitor. Additionally a ceramic capacitor is required between the CPH and CPL pins to act as the flying capacitor.

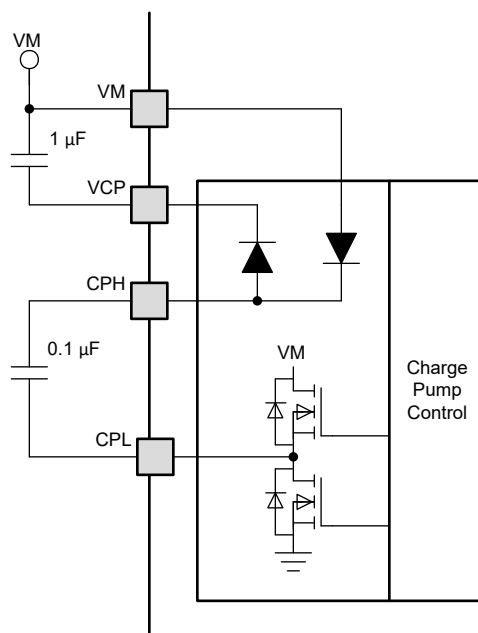


Figure 6-13. Charge Pump Block Diagram

6.7 Linear Voltage Regulator

A linear voltage regulator is integrated in the device. When the VCC pin is connected to DVDD, the DVDD regulator provides power to the low-side gate driver and all the internal circuits. For proper operation, bypass the DVDD pin to GND using a 1µF ceramic capacitor. The DVDD output is nominally 5V.

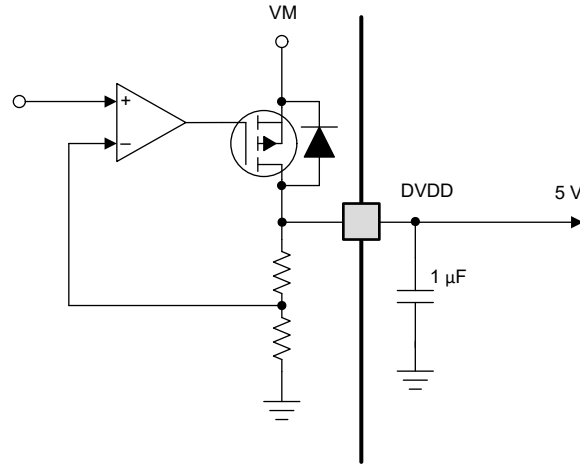


Figure 6-14. Linear Voltage Regulator Block Diagram

If a digital input must be tied permanently high, tying the input to the DVDD pin instead of an external regulator is preferred. This method saves power when the VM pin is not applied or in sleep mode: the DVDD regulator is disabled and current does not flow through the input pulldown resistors. For reference, logic level inputs have a typical pulldown of 200kΩ.

6.8 VCC Voltage Supply

An external voltage can be applied to the VCC pin to power the internal logic circuitry. Maintain the voltage on the VCC pin between 3.05V and 5.5V. When an external supply is not available, VCC must be connected to the DVDD pin of the device.

When powered by the VCC, the internal logic blocks do not consume power from the VM supply rail - thereby reducing the power loss in the DRV8262. This is beneficial in high voltage applications, and when ambient temperature is high. Bypass the VCC pin to ground using a 0.1µF ceramic capacitor.

6.9 Logic Level, Tri-Level and Quad-Level Pin Diagrams

Figure 6-15 shows the input structure for DECAY pin.

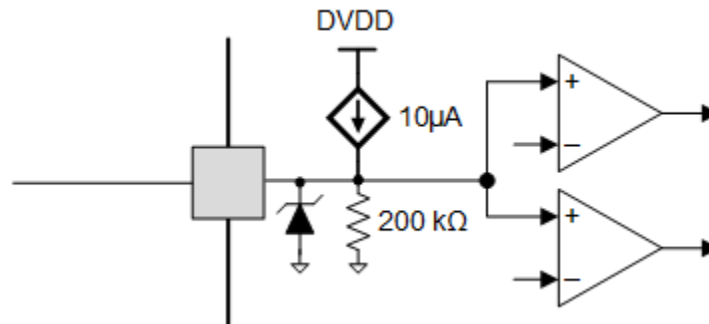


Figure 6-15. Tri-Level Input Pin Diagram

Figure 6-16 shows the input structure for TOFF pin.

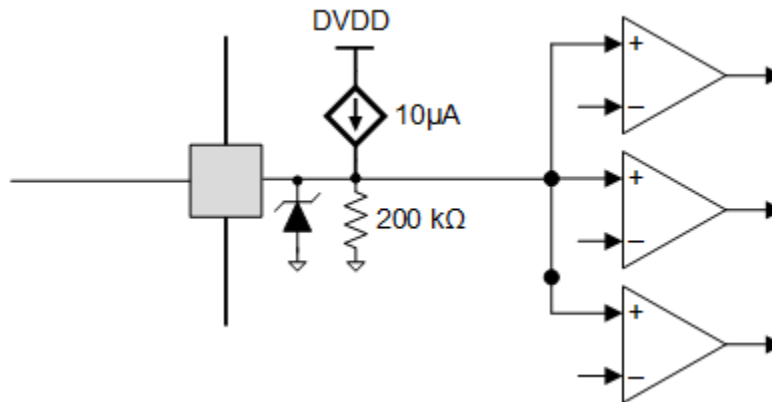


Figure 6-16. Quad-Level Input Pin Diagram

Figure 6-17 shows the input structure for IN1, IN2, IN3, IN4, MODE1, MODE2, OCPM and nSLEEP pins.

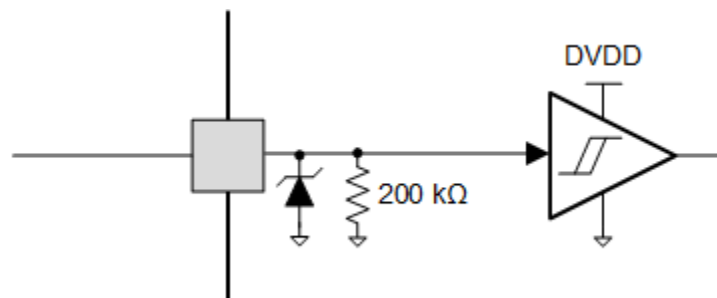


Figure 6-17. Logic-Level Input Pin Diagram

6.10 Protection Circuits

The devices are fully protected against supply undervoltage, charge pump undervoltage, output overcurrent, and device overtemperature events.

6.10.1 VM Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the UVLO threshold voltage:

- All the outputs are disabled (High-Z)
- nFAULT pin is driven low
- The charge pump is disabled

Normal operation resumes (driver operation and nFAULT released) when the VM voltage recovers above the UVLO rising threshold voltage.

If the VM voltage falls below the internal digital reset voltage (3.9V maximum), then the internal logic circuits are disabled and the pull-down on nFAULT is also disabled. So, when VM drops below about 3.9V, nFAULT is pulled high again.

6.10.2 VCP Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin falls below the CPUV voltage:

- All the outputs are disabled (High-Z)
- nFAULT pin is driven low
- The charge pump remains active

Normal operation resumes (driver operation and nFAULT released) when the VCP undervoltage condition is removed.

6.10.3 Logic Supply Power on Reset (POR)

If at any time the voltage on the VCC pin falls below the VCC_{UVLO} threshold:

- All the outputs are disabled (High-Z)
- Charge pump is disabled

VCC UVLO is not reported on the nFAULT pin. Normal motor-driver operation resumes when the VCC undervoltage condition is removed.

6.10.4 Overcurrent Protection (OCP)

Analog current-limit circuit on each MOSFET limits the current through that MOSFET by removing the gate drive. If this current limit persists for longer than the t_{OCP} time, an overcurrent fault is detected.

- The H-bridge is disabled. For Dual H-bridge mode, only the H-bridge experiencing the overcurrent is disabled.
- nFAULT is driven low
- Charge pump remains active

Overcurrent conditions on both high and low side MOSFETs; meaning a short to ground or short to supply results in an overcurrent fault detection.

Once the overcurrent condition is removed, the recovery mechanism depends on the OCPM pin setting. OCPM pin programs either latch-off or automatic retry type recovery.

- When the OCPM pin is logic low, the device has latch-off type recovery - which means once the OCP condition is removed, normal operation resumes after applying an nSLEEP reset pulse or a power cycling.
- When the OCPM pin is logic high, normal operation resumes automatically (driver operation and nFAULT released) after the t_{RETRY} time has elapsed and the fault condition is removed.

6.10.5 Thermal Shutdown (OTSD)

Thermal shutdown is detected if the die temperature exceeds the thermal shutdown limit (T_{OTSD}). When thermal shutdown is detected -

- All MOSFETs are disabled
- nFAULT is driven low
- Charge pump is disabled

Once the thermal shutdown condition is removed, the recovery mechanism depends on the OCPM pin setting. OCPM pin programs either latch-off or automatic retry type recovery.

- When the OCPM pin is logic low, the device has latch-off type recovery - which means after the junction temperature falls below the overtemperature threshold limit minus the hysteresis ($T_{OTSD} - T_{HYS_OTSD}$), normal operation resumes after applying an nSLEEP reset pulse or a power cycling.
- When the OCPM pin is logic high, normal operation resumes automatically after the junction temperature falls below the overtemperature threshold limit minus the hysteresis ($T_{OTSD} - T_{HYS_OTSD}$).

6.10.6 nFAULT Output

The nFAULT pin has an open-drain output and pulled up to a 5V, 3.3V, or 1.8V supply. When a fault is detected, the nFAULT pin is logic low. The nFAULT pin is high after power-up. For a 5V pullup, the nFAULT pin can be tied to the DVDD pin with a resistor. For a 3.3V or 1.8V pullup, an external supply must be used.

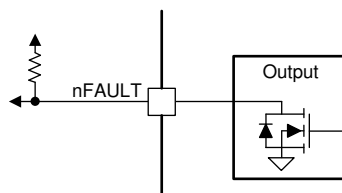


Figure 6-18. nFAULT Pin

6.10.7 Fault Condition Summary

Table 6-9. Fault Condition Summary

FAULT	CONDITION	ERROR REPORT	H-BRIDGE	CHARGE PUMP	LOGIC	RECOVERY
VM undervoltage (UVLO)	$VM < V_{UVLO}$	nFAULT	Disabled	Disabled	Reset	$VM > V_{UVLO}$
VCP undervoltage (CPUV)	$VCP < V_{CPUV}$	nFAULT	Disabled	Operating	Operating	$VCP > V_{CPUV}$
Logic Supply POR	$VCC < VCC_{UVLO}$	-	Disabled	Disabled	Reset	$VCC > VCC_{UVLO}$
Overcurrent (OCP)	$I_{OUT} > I_{OCP}, OCPM = 0$	nFAULT	Disabled	Operating	Operating	Latched: nSLEEP reset pulse
	$I_{OUT} > I_{OCP}, OCPM = 1$	nFAULT	Disabled	Operating	Operating	Automatic retry: t_{RETRY}
Thermal Shutdown (OTSD)	$T_J > T_{TSD}, OCPM = 0$	nFAULT	Disabled	Disabled	Operating	Latched: nSLEEP reset pulse
	$T_J > T_{TSD}, OCPM = 1$	nFAULT	Disabled	Disabled	Operating	Automatic: $T_J < T_{OTSD} - T_{HYS_OTSD}$

6.11 Device Functional Modes

6.11.1 Sleep Mode

When the nSLEEP pin is low, the device enters a low-power sleep mode. In sleep mode, all the internal MOSFETs, the DVDD regulator, SPI and the charge pump is disabled. The t_{SLEEP} time must elapse after a falling edge on the nSLEEP pin before the device enters sleep mode. The device is brought out of sleep automatically if the nSLEEP pin is brought high. The t_{WAKE} time must elapse before the device is ready for inputs.

6.11.2 Operating Mode

This mode is enabled when -

- nSLEEP is high
- $VM > UVLO$

The t_{WAKE} time must elapse before the device is ready for inputs.

6.11.3 nSLEEP Reset Pulse

A latched fault can be cleared by an nSLEEP reset pulse. This pulse width must be greater than 20µs and smaller than 40µs. If nSLEEP is low for longer than 40µs, but less than 120µs, the faults are cleared and the device can shutdown, as shown in the timing diagram below. This reset pulse does not affect the status of the charge pump or other functional blocks.

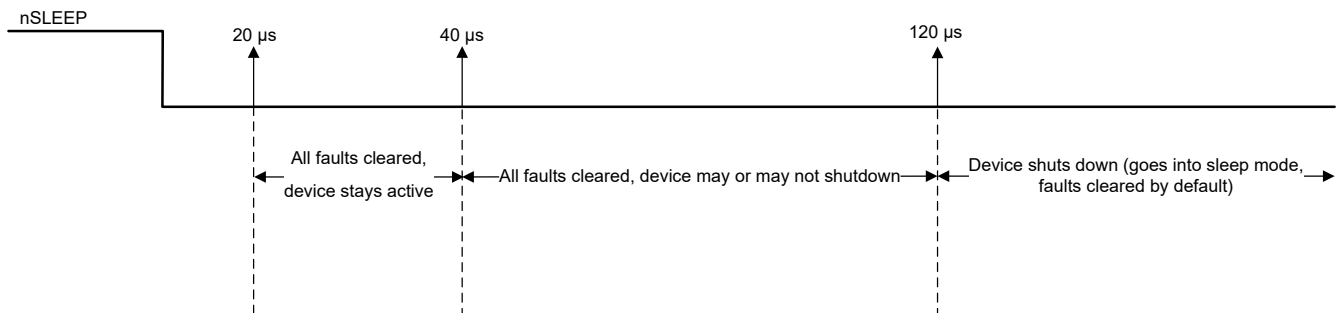


Figure 6-19. nSLEEP Reset Pulse

6.11.4 Functional Modes Summary

The table below lists a summary of the functional modes.

Table 6-10. Functional Modes Summary

CONDITION		CONFIGURATION	H-BRIDGE	DVDD Regulator	CHARGE PUMP	Logic
Sleep mode	4.5V < VM < 60V	nSLEEP pin = 0	Disabled	Disabled	Disabled	Disabled
Operating	4.5V < VM < 60V	nSLEEP pin = 1	Operating	Operating	Operating	Operating

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The DRV8262 can be used to drive the following types of loads -

- One or two brushed-DC motors
- One stepper motor
- One or two thermoelectric coolers (TEC)

7.1.1 Driving Brushed-DC Motors

In this application example, the device is configured to drive a bidirectional current through one or two brushed-DC motors. The H-bridge configuration, polarity, interface and duty cycle are controlled with PWM and IO resources from the external controller to the INx and MODEx pins. The current limit threshold (I_{TRIP}) is generated with a resistor divider from the VREF pin. The device is configured for the slow decay by tying the DECAY pin to ground.

7.1.1.1 Brushed-DC Motor Driver Typical Application

The following schematics show the DRV8262 driving one and two brushed-DC motors respectively.

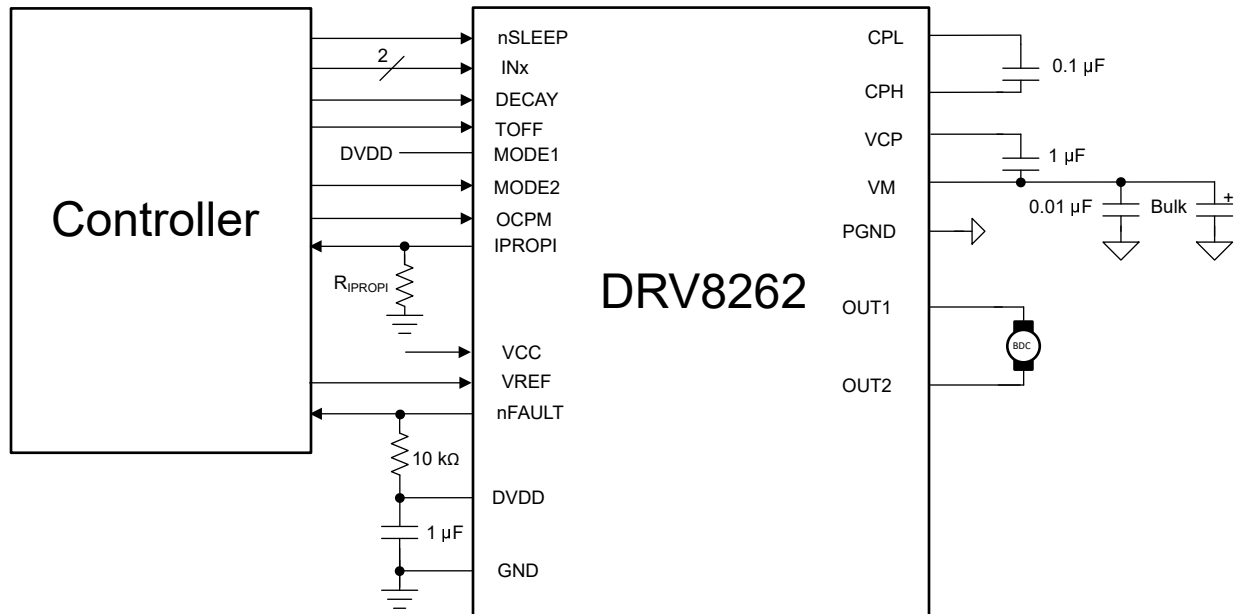


Figure 7-1. Driving One Brushed-DC Motor

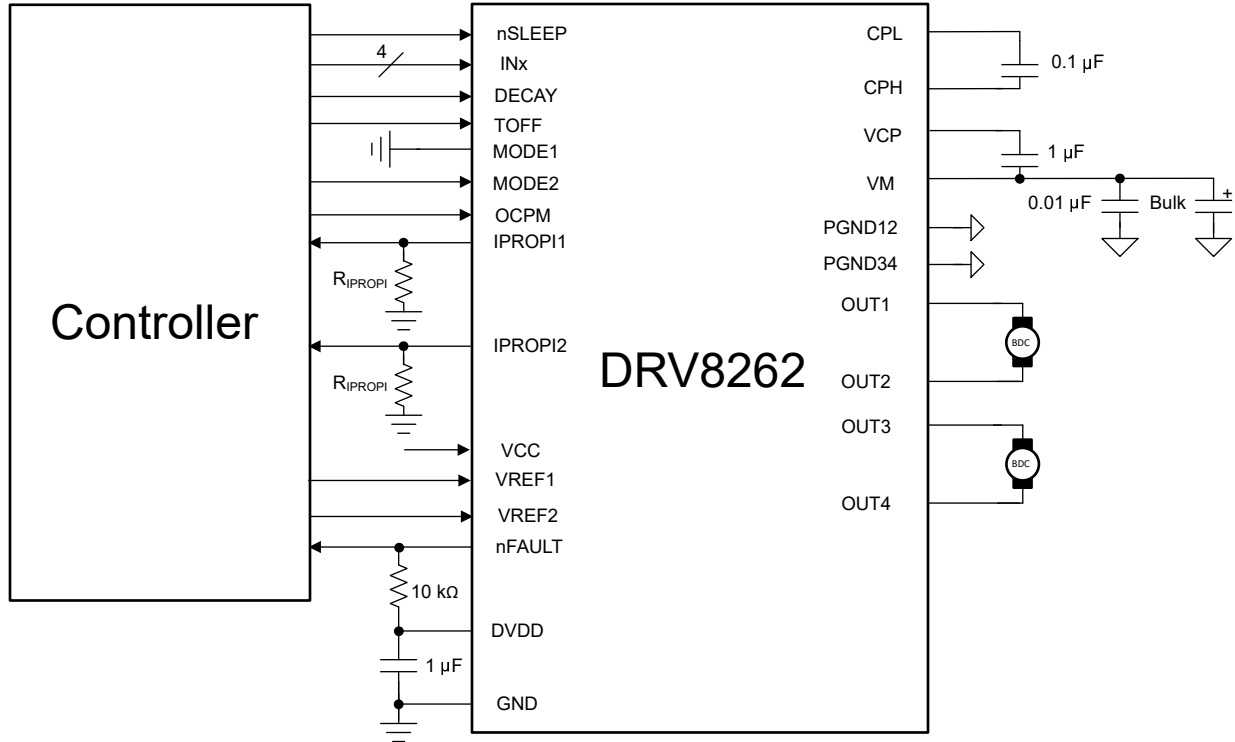


Figure 7-2. Driving Two Brushed-DC Motors

7.1.1.2 Power Loss Calculations - Dual H-bridge

For a H-bridge with high-side recirculation, power dissipation for each FET can be approximated as follows:

- $P_{HS1} = R_{DS(ON)} \times I_L^2$
- $P_{LS1} = 0$
- $P_{HS2} = [R_{DS(ON)} \times I_L^2 \times (1-D)] + [2 \times V_D \times I_L \times t_D \times f_{PWM}]$
- $P_{LS2} = [R_{DS(ON)} \times I_L^2 \times D] + [VM \times I_L \times t_{RF} \times f_{PWM}]$

Where,

- $R_{DS(ON)}$ = ON resistance of each FET
 - For DRV8262 in dual H-bridge mode, $R_{DS(ON)}$ is typically 50mΩ at 25 °C, and 85mΩ at 150 °C.
- f_{PWM} = PWM switching frequency
- VM = Supply voltage to the driver
- I_L = Motor RMS current
- D = PWM duty cycle (between 0 and 1)
- t_{RF} = Output voltage rise/ fall time
 - For DRV8262, the rise/fall time is 110ns
- V_D = FET body diode forward bias voltage
 - For DRV8262, the voltage is 1V
- t_D = dead time
 - For DRV8262, the voltage 300ns

For estimating power dissipation for load current flow in the reverse direction, identical equations apply, with only swapping of HS1 with HS2 and LS1 with LS2.

Substituting the following values in the equations above -

- VM = 24V
- I_L = 4A
- $R_{DS(ON)}$ = 50mΩ

- $D = 0.5$
- $V_D = 1V$
- $t_D = 300ns$
- $t_{RF} = 110ns$
- $f_{PWM} = 20kHz$

The losses in each FET can be calculated as follows -

$$P_{HS1} = 50m\Omega \times 4^2 = 0.8 \text{ W}$$

$$P_{LS1} = 0$$

$$P_{HS2} = [50m\Omega \times 4^2 \times (1-0.5)] + [2 \times 1V \times 4A \times 300ns \times 20kHz] = 0.448W$$

$$P_{LS2} = [50m\Omega \times 4^2 \times 0.5] + [24 \times 4A \times 110ns \times 20kHz] = 0.611W$$

$$\text{Quiescent Current Loss } P_Q = 24V \times 5mA = 0.12W$$

$$P_{TOT} = 2 \times (P_{HS1} + P_{LS1} + P_{HS2} + P_{LS2}) + P_Q = 2 \times (0.8 + 0 + 0.448 + 0.611) + 0.12 = 3.84 \text{ W}$$

7.1.1.3 Power Loss Calculations - Single H-bridge

In single H-bridge mode, on-resistance of each FET is typically 25mΩ at 25 °C, and 43mΩ at 150 °C.

Substituting the following values in the power loss equations -

- $V_M = 24V$
- $I_L = 8A$
- $R_{DS(ON)} = 25m\Omega$
- $D = 0.5$
- $V_D = 1V$
- $t_D = 300ns$
- $t_{RF} = 110ns$
- $f_{PWM} = 20kHz$

The losses in each FET can be calculated as follows -

$$P_{HS1} = 25m\Omega \times 8^2 = 1.6W$$

$$P_{LS1} = 0$$

$$P_{HS2} = [25m\Omega \times 8^2 \times (1-0.5)] + [2 \times 1V \times 8A \times 300ns \times 20kHz] = 0.896W$$

$$P_{LS2} = [25m\Omega \times 8^2 \times 0.5] + [24 \times 8A \times 110ns \times 20kHz] = 1.223W$$

$$\text{Quiescent Current Loss } P_Q = 24V \times 5mA = 0.12W$$

$$P_{TOT} = P_{HS1} + P_{LS1} + P_{HS2} + P_{LS2} + P_Q = 1.6 + 0 + 0.896 + 1.223 + 0.12 = 3.84W$$

7.1.1.4 Junction Temperature Estimation

For an ambient temperature of T_A and total power dissipation (P_{TOT}), the junction temperature (T_J) is calculated as -

$$T_J = T_A + (P_{TOT} \times R_{\theta JA})$$

Considering a JEDEC standard 4-layer PCB, the junction-to-ambient thermal resistance ($R_{\theta JA}$) is 22.2 °C/W for the DDW package.

Assuming 25°C ambient temperature, the junction temperature is calculated as shown below -

$$T_J = 25^\circ\text{C} + (3.84W \times 22.2^\circ\text{C/W}) = 110.2^\circ\text{C} \quad (4)$$

For more accurate calculation, consider the dependency of on-resistance of FETs with device junction temperature shown in the Typical Operating Characteristics section.

For example,

- At 110.2 °C junction temperature, the on-resistance likely increases by a factor of 1.4 compared to the on-resistance at 25 °C.
- The initial estimate of conduction loss is 3.2W.
- New estimate of conduction loss is 3.2W x 1.4 = 4.48W.
- New estimate of the total power loss accordingly be 5.12W.
- New estimate of junction temperature for the DDW package is 138.7 °C.
- Further iterations are unlikely to increase the junction temperature estimate by significant amount.

When using the DDV package, if a heat sink with less than 4 °C/W thermal resistance is chosen, the junction to ambient thermal resistance can be lower than 5 °C/W. The initial estimate of the junction temperature with the DDV package in this application will therefore be -

$$T_J = 25^{\circ}\text{C} + (3.84\text{-W} \times 5^{\circ}\text{C/W}) = 44.2^{\circ}\text{C} \quad (5)$$

The DDV package is able to deliver up to 10A RMS current to both brushed-DC motors in dual H-bridge mode and up to 20A RMS current to a brushed-DC motor in single H-bridge mode.

7.1.1.5 Application Performance Plots

Traces from top to bottom: I_{OUT2}, V_{I_{PROPI2}}, I_{OUT1}, V_{I_{PROPI1}}, OUT2, OUT3, OUT1, OUT4

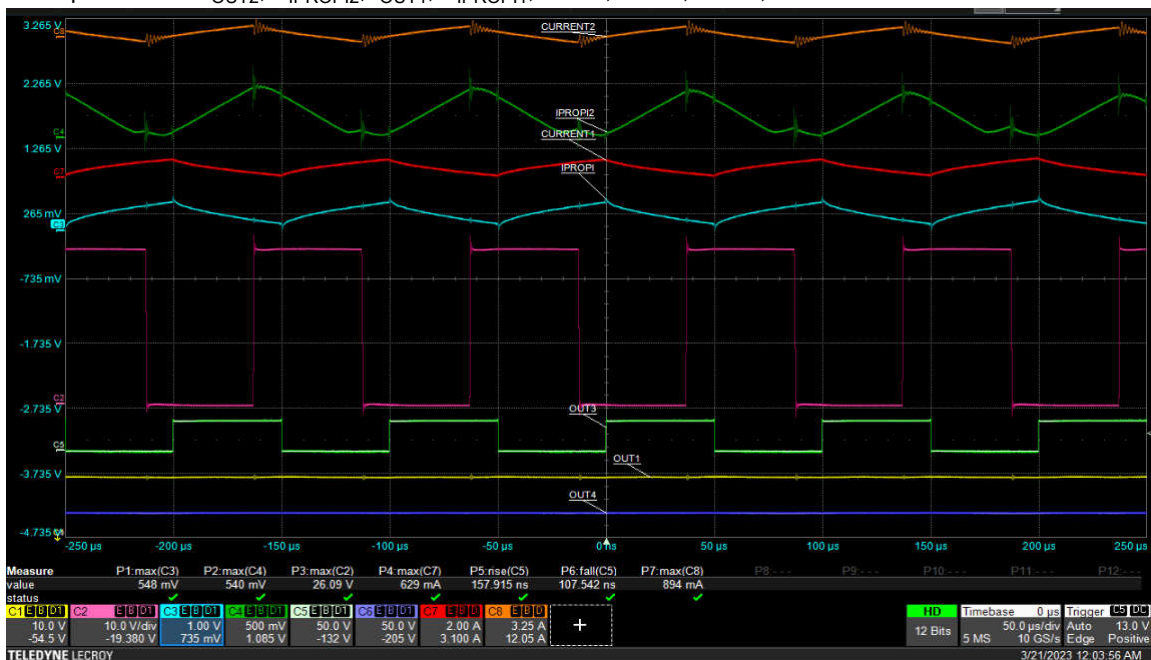


Figure 7-3. Dual H-bridge Operation, VM = 24 V

7.1.2 Driving Stepper Motors

When configured in the dual H-bridge mode, the device can drive one stepper motor.

7.1.2.1 Stepper Driver Typical Application

The following schematic shows the DRV8262 driving a stepper motor.

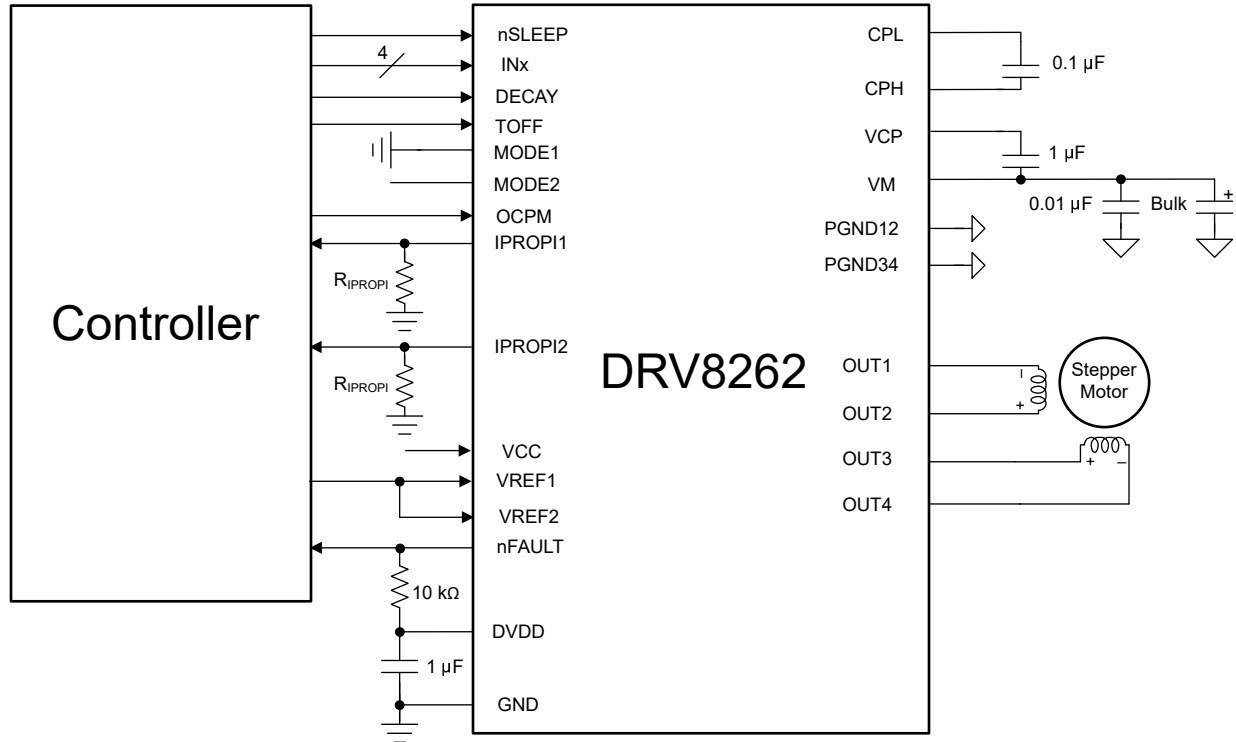


Figure 7-4. Driving One Stepper Motor

The full-scale current (I_{FS}) is the maximum current driven through either winding. This quantity depends on the VREF voltage and the resistor connected from IPROPI pin to ground.

$$I_{FS} \times A_{IPROPI} = V_{VREF} / R_{IPROPI}$$

The maximum allowable voltage on the VREF pins is 3.3V. DVDD can be used to provide VREF through a resistor divider.

Note

The I_{FS} current must also follow Equation 6 to avoid saturating the motor. VM is the motor supply voltage, and R_L is the motor winding resistance.

$$I_{FS} \text{ (A)} < \frac{VM \text{ (V)}}{R_L \text{ (}\Omega\text{)} + 2 \times R_{DS(ON)} \text{ (}\Omega\text{)}} \tag{6}$$

If the target motor speed is too high, the motor does not spin. Make sure that the motor can support the target speed.

For a desired motor speed (v), microstepping level (n_m), and motor full step angle (θ_{step}), determine the frequency of the input waveform as follows -

$$f_{\text{step}} \text{ (steps / s)} = \frac{v \text{ (rpm)} \times 360 \text{ (}^\circ \text{ / rot)}}{\theta_{\text{step}} \text{ (}^\circ \text{ / step)} \times n_m \text{ (steps / microstep)} \times 60 \text{ (s / min)}} \quad (7)$$

θ_{step} can be found in the stepper motor data sheet or written on the motor.

The frequency f_{step} gives the frequency of input change on the DRV8262. $1/f_{\text{step}} = t_{\text{STEP}}$ on the diagram below. Equation 8 shows an example calculation for a 120 rpm target speed and 1/2 step.

$$f_{\text{step}} \text{ (steps / s)} = \frac{120 \text{ rpm} \times 360^\circ \text{ / rot}}{1.8^\circ \text{ / step} \times 1/2 \text{ steps / microstep} \times 60 \text{ s / min}} = 800\text{Hz} \quad (8)$$

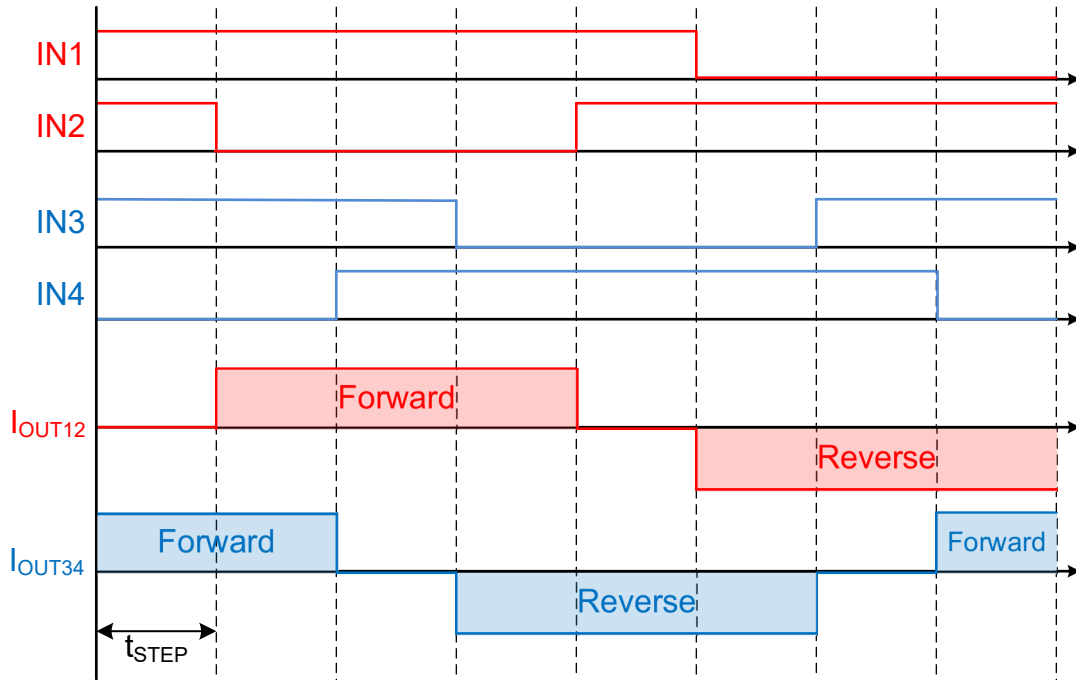


Figure 7-5. Example 1/2 Stepping Operation

The IPROPI pins output the current of each H-bridge, corresponding to current of coil A and coil B of the stepper motor during drive and slow-decay (high-side recirculation) modes.

7.1.2.2 Power Loss Calculations

The following calculations assume a use case where the supply voltage is 24V, full-scale current is 5A, and input PWM frequency is 30kHz.

The total power dissipation constitutes of three main components - conduction loss (P_{COND}), switching loss (P_{SW}) and power loss due to quiescent current consumption (P_{Q}).

The conduction loss (P_{COND}) depends on the motor rms current (I_{RMS}) and high-side ($R_{\text{DS(ONH)}}$) and low-side ($R_{\text{DS(ONL)}}$) on-state resistances as shown in Equation 9.

$$P_{\text{COND}} = 2 \times (I_{\text{RMS}})^2 \times (R_{\text{DS(ONH)}} + R_{\text{DS(ONL)}}) \quad (9)$$

The conduction loss for the typical application shown in Section 7.1.2.1 is calculated in Equation 10.

$$P_{\text{COND}} = 2 \times (I_{\text{RMS}})^2 \times (R_{\text{DS(ONH)}} + R_{\text{DS(ONL)}}) = 2 \times (5\text{A} / \sqrt{2})^2 \times (0.1\Omega) = 2.5\text{W} \quad (10)$$

The power loss due to the PWM switching frequency depends on the output voltage rise/fall time (t_{RF}), supply voltage, motor RMS current and the PWM switching frequency. The switching losses in each H-bridge during rise-time and fall-time are calculated as shown in [Equation 11](#) and [Equation 12](#).

$$P_{SW_RISE} = 0.5 \times V_{VM} \times I_{RMS} \times t_{RF} \times f_{PWM} \quad (11)$$

$$P_{SW_FALL} = 0.5 \times V_{VM} \times I_{RMS} \times t_{RF} \times f_{PWM} \quad (12)$$

After substituting the values of various parameters, the switching losses in each H-bridge are calculated as shown below -

$$P_{SW_RISE} = 0.5 \times 24V \times (5A / \sqrt{2}) \times (110ns) \times 30kHz = 0.14W \quad (13)$$

$$P_{SW_FALL} = 0.5 \times 24V \times (5A / \sqrt{2}) \times (110ns) \times 30kHz = 0.14W \quad (14)$$

The total switching loss for the stepper motor driver (P_{SW}) is calculated as twice the sum of rise-time (P_{SW_RISE}) switching loss and fall-time (P_{SW_FALL}) switching loss as shown below -

$$P_{SW} = 2 \times (P_{SW_RISE} + P_{SW_FALL}) = 2 \times (0.14W + 0.14W) = 0.56W \quad (15)$$

Note

The output rise/fall time (t_{RF}) is expected to change based on the supply-voltage, temperature and device to device variation.

When the VCC pin is connected to an external voltage, the quiescent current is typically 5mA. The power dissipation due to the quiescent current consumed by the power supply is calculated as shown below -

$$P_Q = V_{VM} \times I_{VM} \quad (16)$$

Substituting the values, quiescent power loss can be calculated as shown below -

$$P_Q = 24V \times 5mA = 0.12W \quad (17)$$

Note

The quiescent power loss is calculated using the typical operating supply current (I_{VM}) which is dependent on supply-voltage, temperature and device to device variations.

The total power dissipation (P_{TOT}) is calculated as the sum of conduction loss, switching loss and the quiescent power loss as shown in [Equation 18](#).

$$P_{TOT} = P_{COND} + P_{SW} + P_Q = 2.5W + 0.56W + 0.12W = 3.18W \quad (18)$$

7.1.2.3 Junction Temperature Estimation

Assuming 25°C ambient temperature, the junction temperature for the DDW package is calculated as shown below -

$$T_J = 25^\circ C + (3.18-W \times 22.2^\circ C/W) = 95.6^\circ C \quad (19)$$

For more accurate calculation, consider the dependency of on-resistance of FETs with device junction temperature, as explained in [Section 7.1.1.4](#).

7.1.3 Driving Thermoelectric Coolers (TEC)

Thermoelectric coolers (TEC) work according to the Peltier effect. When a voltage is applied across the TEC, a DC current flows through the junction of the semiconductors, causing a temperature difference. Heat is transferred from one side of the TEC to the other. This creates a “hot” and a “cold” side of the TEC element. If the DC current is reversed, the hot and cold sides reverse as well.

A common way of modulating the current through the TEC is to use PWM driving and make the average current change by varying the ON and OFF duty cycles. To allow both heating and cooling from a single supply, a H-bridge topology is required. In the dual H-bridge mode, the device can drive two H-bridges to drive two TECs bi-directionally with up to 10A current. In the single H-bridge mode, the device can drive a single TEC with up to 20A current.

The DRV8262 also features integrated current sensing and current sense output (IPROPI) with $\pm 4\%$ accuracy to eliminate the need for two external shunt resistors in a closed-loop control topology, saving bill-of-materials cost and space. The following schematic shows the DRV8262 driving two TECs.

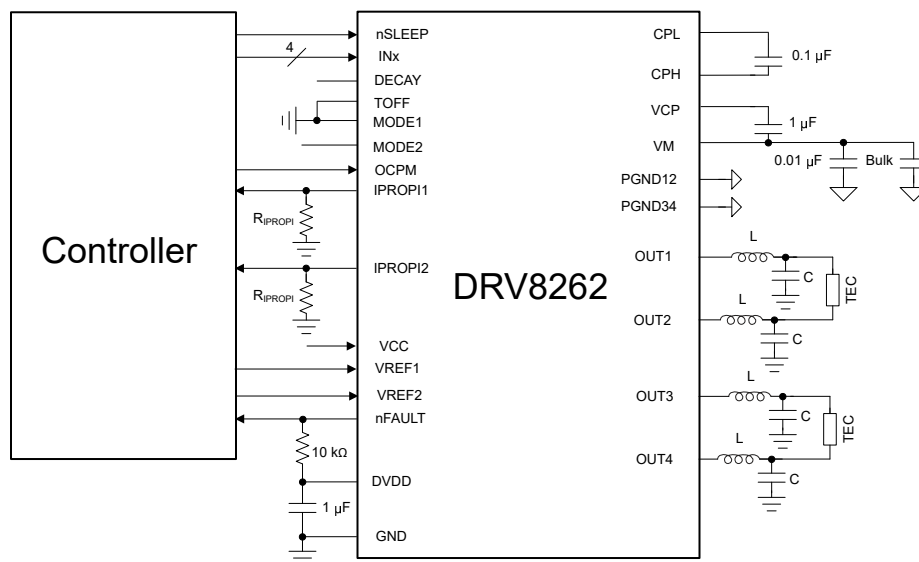


Figure 7-6. Driving two TECs

The following schematic shows the DRV8262 driving one TEC with higher current.

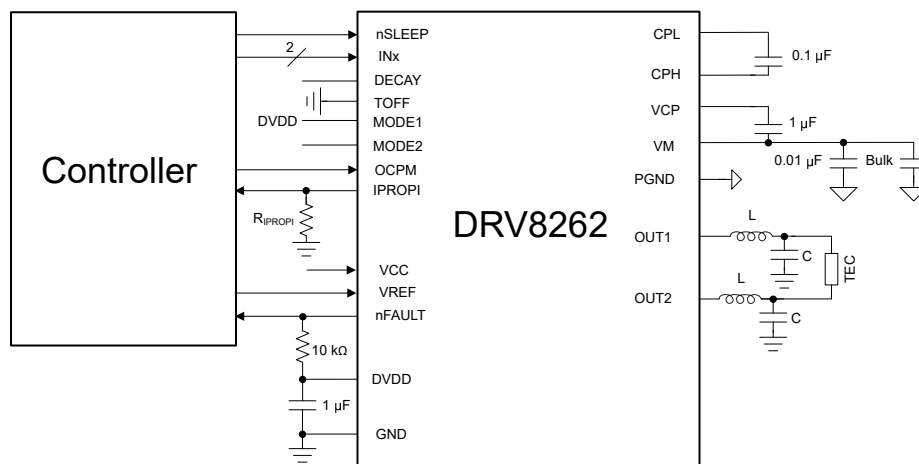


Figure 7-7. Driving one TEC with higher current

The LC filters connected to the output nodes convert the PWM output from the DRV8262 into a low-ripple DC voltage across the TEC. The filters are required to minimize the ripple current, because fast transients (for example, square wave power) can shorten the life of the TEC. The maximum ripple current is recommended to be less than 10% of maximum current. The maximum temperature differential across the TEC, which decreases as ripple current increases, is calculated with the following equation:

$$\Delta T = \Delta T_{MAX} / (1 + N^2) \quad (20)$$

Where ΔT is actual temperature differential, ΔT_{MAX} is maximum possible temperature differential specified in the TEC data sheet, N is the ratio between ripple and maximum current. N can not be greater than 0.1.

The choice of the input PWM frequency is a trade-off between switching loss and use of smaller inductors and capacitors. High PWM frequency also means that the voltage across the TEC can be tightly controlled, and the LC components can potentially be cheaper.

The transfer function of a second order low-pass filter is shown below:

$$H(j\omega) = 1 / (1 - (\omega / \omega_0)^2 + j\omega / Q\omega_0) \quad (21)$$

Where,

$\omega_0 = 1 / \sqrt{LC}$, resonant frequency of the filter

Q = quality factor

ω = DRV8262 input PWM frequency

The resonant frequency for the filter is typically chosen to be at least one order of magnitude lower than the PWM frequency. With this assumption, [Equation 20](#) can be simplified to -

H in dB = $-40 \log (f_S/f_0)$

Where $f_0 = 1/2\pi\sqrt{LC}$ and f_S is the input PWM switching frequency.

- If $L = 10\mu\text{H}$ and $C = 22\mu\text{F}$, the resonant frequency is 10.7kHz.
- This resonant frequency corresponds to 39dB of attenuation at 100kHz switching frequency.
- For $V_M = 48\text{V}$, 39dB attenuation means that the amount of ripple voltage across the TEC element is approximately 550mV.
- For a TEC element with a resistance of 1.5Ω , the ripple current through the TEC is therefore at 366mA.
- At 5A current, 366mA corresponds to 7.32% ripple current.
- This causes about 0.5% reduction of the maximum temperature differential of the TEC element, as per [Equation 20](#).

Adjust the LC values according to the supply voltage and DC current through the TEC element. The DRV8262 supports up to 200kHz input PWM frequency. The power loss in the device at any given ambient temperature must be carefully considered before selecting the input PWM frequency.

Closing the loop on current is important in some TEC based heating and cooling systems. The DRV8262 can achieve this without the need for external current shunt resistors. Internal current mirrors are used to monitor the currents in each half-bridge and this information is available on IPROPI pins. A microcontroller can monitor and adjust the PWM duty based on the IPROPI pin voltage.

Additionally, the DRV8262 can regulate the current internally by providing an external voltage reference (V_{REF}) to the device to adjust the current regulation trip point. The current loop is then closed within the H-bridge.

7.2 Power Supply Recommendations

The device is designed to operate from an input voltage supply (V_M) range from 4.5V to 60V. A $0.01\mu\text{F}$ ceramic capacitor rated for V_M must be placed close to the V_M pins of the device. In addition, a bulk capacitor must be included on V_M .

7.2.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. Having more bulk capacitance is generally beneficial, while the disadvantages are increased cost and physical size.

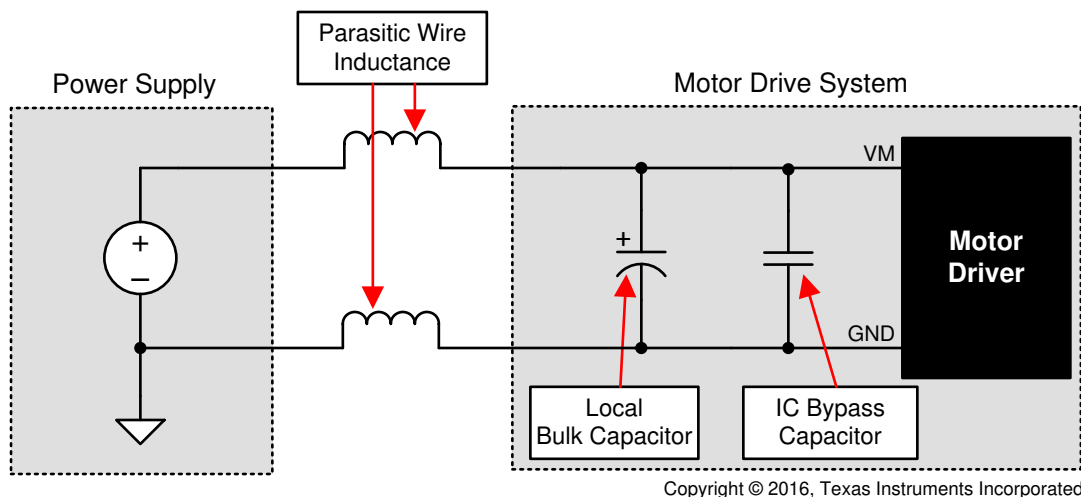
The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power supply's capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system limits the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

The voltage rating for bulk capacitors is higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.



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Figure 7-8. Example Setup of Motor Drive System With External Power Supply

7.2.2 Power Supplies

The device needs only a single supply voltage connected to the VM pins.

- The VM pin provides the power supply to the H-Bridges.
- An internal voltage regulator provides a 5V supply (DVDD) for the digital and low-voltage analog circuitry. The DVDD pin is not recommended to be used as a voltage source for external circuitry.
- An external low-voltage supply can be connected to the VCC pin to power the internal circuitry. A 0.1µF decoupling capacitor is placed close to the VCC pin to provide a constant voltage during transient.
- Additionally, the high-side gate drive requires a higher voltage supply, which is generated by built-in charge pump requiring external capacitors.

7.3 Layout

7.3.1 Layout Guidelines

- The VM pins is bypassed to PGND pins using low-ESR ceramic bypass capacitors with a recommended value of 0.01 μ F rated for VM. The capacitors is placed as close to the VM pins as possible with a thick trace or ground plane connection to the device PGND pins.
- The VM pins must be bypassed to PGND using a bulk capacitor rated for VM. This component can be an electrolytic capacitor.
- A low-ESR ceramic capacitor must be placed in between the CPL and CPH pins. A value of 0.1 μ F rated for VM is recommended. Place this component as close to the pins as possible.
- A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. A value of 1 μ F rated for 16V is recommended. Place this component as close to the pins as possible.
- Bypass the DVDD pin to ground with a low-ESR ceramic capacitor. A value of 1 μ F rated for 6.3V is recommended. Place this bypassing capacitor as close to the pin as possible.
- Bypass the VCC pin to ground with a low-ESR ceramic capacitor. A value of 0.1 μ F rated for 6.3V is recommended. Place this bypassing capacitor as close to the pin as possible.
- In general, inductance between the power supply pins and decoupling capacitors must be avoided.
- The thermal PAD of the DDW package must be connected to system ground.
 - TI recommends to use a big unbroken single ground plane for the whole system / board. The ground plane can be made at bottom PCB layer.
 - To minimize the impedance and inductance, the traces from ground pins are as short and wide as possible, before connecting to bottom layer ground plane through vias.
 - Multiple vias are suggested to reduce the impedance.
 - Try to clear the space around the device as much as possible especially at bottom PCB layer to improve the heat spreading.
 - Single or multiple internal ground planes connected to the thermal PAD also helps spreading the heat and reduce the thermal resistance.

7.3.2 Layout Example

Follow the layout example of the DRV8262 EVM. The design files can be downloaded from the [DRV8262EVM](#) product folder.

8 Package Thermal Considerations

8.1 DDW Package

Thermal pad of the DDW package is attached at bottom of device to improve the thermal capability of the device. The thermal pad has to be soldered with a very good coverage on PCB to deliver the power specified in the data sheet. Refer to the [Section 7.3.1](#) section for more details.

8.1.1 Thermal Performance

The data sheet-specified junction-to-ambient thermal resistance, $R_{\theta JA}$, is primarily useful for comparing various drivers or approximating thermal performance. However, the actual system performance is better or worse than this value depending on PCB stack-up, routing, number of vias, and copper area around the thermal pad. The length of time the driver drives a particular current also impacts power dissipation and thermal performance. This section considers how to design for steady-state and transient thermal conditions.

The data in this section is simulated using the following criteria:

HTSSOP (DDW package)

- 2-layer PCB (size 114.3 x 76.2 x 1.6mm), standard FR4, 1oz (35mm copper thickness) or 2oz copper thickness. Thermal vias are only present under the thermal pad (13 x 5 thermal via array, 1.1mm pitch, 0.2mm diameter, 0.025mm Cu plating).
 - Top layer: HTSSOP package footprint and copper plane heat sink. Top layer copper area is varied in simulation.
 - Bottom layer: ground plane thermally connected through vias under the thermal pad for the driver. Bottom layer copper area varies with top copper area.
- 4-layer PCB (size 114.3 x 76.2 x 1.6mm), standard FR4. Outer planes are 1oz (35mm copper thickness) or 2oz copper thickness. Inner planes are kept at 1oz. Thermal vias are only present under the thermal pad (13 x 5 thermal via array, 1.1mm pitch, 0.2mm diameter, 0.025mm Cu plating).
 - Top layer: HTSSOP package footprint and copper plane heat sink. Top layer copper area is varied in simulation.
 - Mid layer 1: GND plane thermally connected to thermal pad through vias. The area of the ground plane varies with top copper area.
 - Mid layer 2: power plane, no thermal connection. The area of the power plane varies with top copper area.
 - Bottom layer: signal layer thermally connected through via stitching from the TOP and internal GND plane. Bottom layer thermal pad is the same size as the top layer copper area.

[Figure 8-1](#) shows an example of the simulated board for the DDW package. [Table 8-1](#) shows the dimensions of the board that are varied for each simulation.

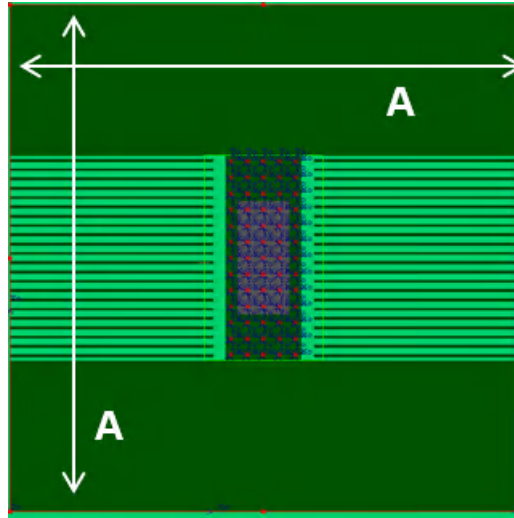


Figure 8-1. DDW PCB model top layer

Table 8-1. Dimension A for DDW package

Cu area (cm ²)	Dimension A (mm)
2	19.79
4	26.07
8	34.63
16	46.54
32	63.25

8.1.1.1 Steady-State Thermal Performance

"Steady-state" conditions assume that the driver operates with a constant RMS current over a long period of time. The figures in this section show how $R_{\theta JA}$ and Ψ_{JB} (junction-to-board characterization parameter) change depending on copper area, copper thickness, and number of layers of the PCB. More copper area, more layers, and thicker copper planes decrease $R_{\theta JA}$ and Ψ_{JB} , which indicate better thermal performance from the PCB layout.

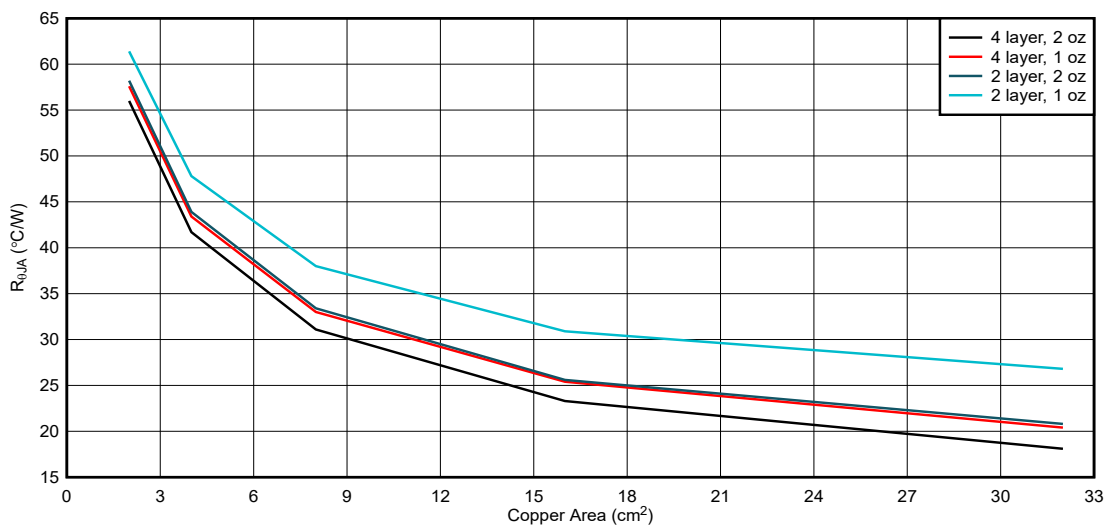


Figure 8-2. DDW Package, PCB junction-to-ambient thermal resistance vs copper area

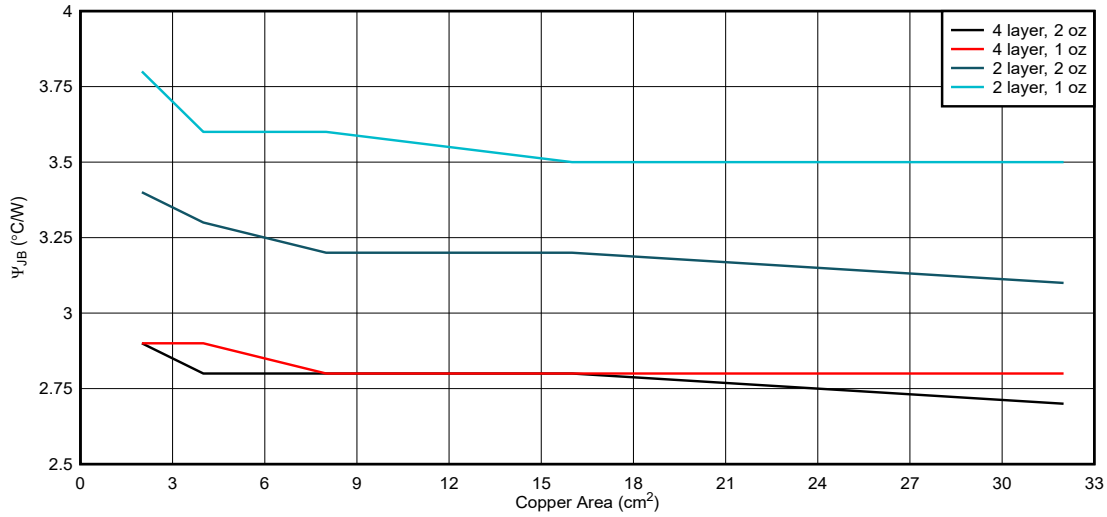


Figure 8-3. DDW Package, junction-to-board characterization parameter vs copper area

8.1.1.2 Transient Thermal Performance

The driver can experience different transient driving conditions that cause large currents to flow for a short duration of time. These include -

- Motor start-up when the rotor is initially stationary.
- Fault conditions when there is a supply or ground short to one of the motor outputs, and the overcurrent protection triggers.
- Briefly energizing a motor or solenoid for a limited time, then de-energizing.

For these transient cases, the duration of drive time is another factor that impacts thermal performance in addition to copper area and thickness. In transient cases, the thermal impedance parameter $Z_{\theta JA}$ denotes the junction-to-ambient thermal performance. The figures in this section show the simulated thermal impedances for 1oz and 2oz copper layouts for the DDW package. These graphs indicate better thermal performance with short current pulses. For short periods of drive time, the device die size and package dominates the thermal performance. For longer drive pulses, board layout has a more significant impact on thermal performance. Both graphs show the curves for thermal impedance split due to number of layers and copper area as the duration of the drive pulse duration increases. Long pulses can be considered steady-state performance.

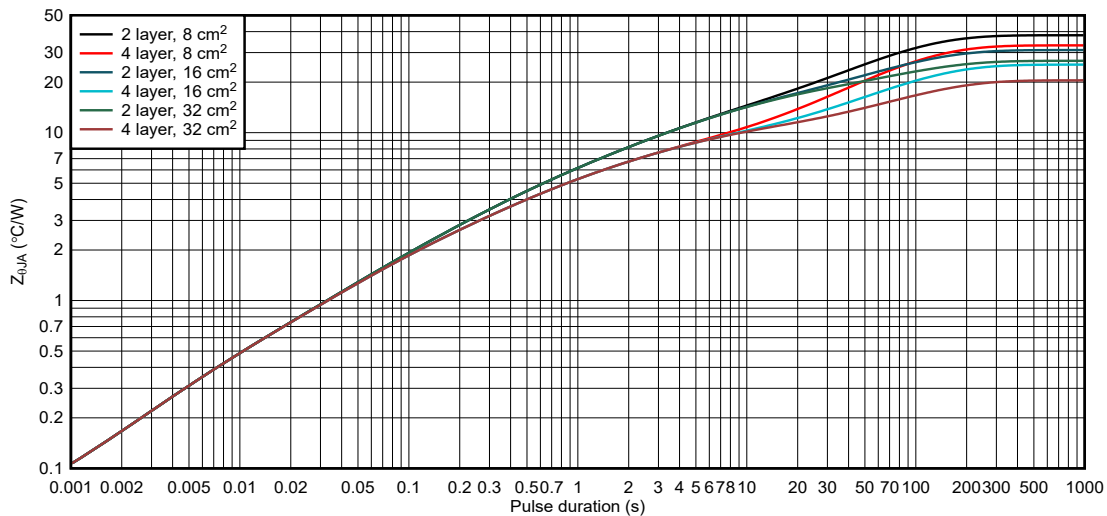


Figure 8-4. DDW package junction-to-ambient thermal impedance for 1oz copper layouts

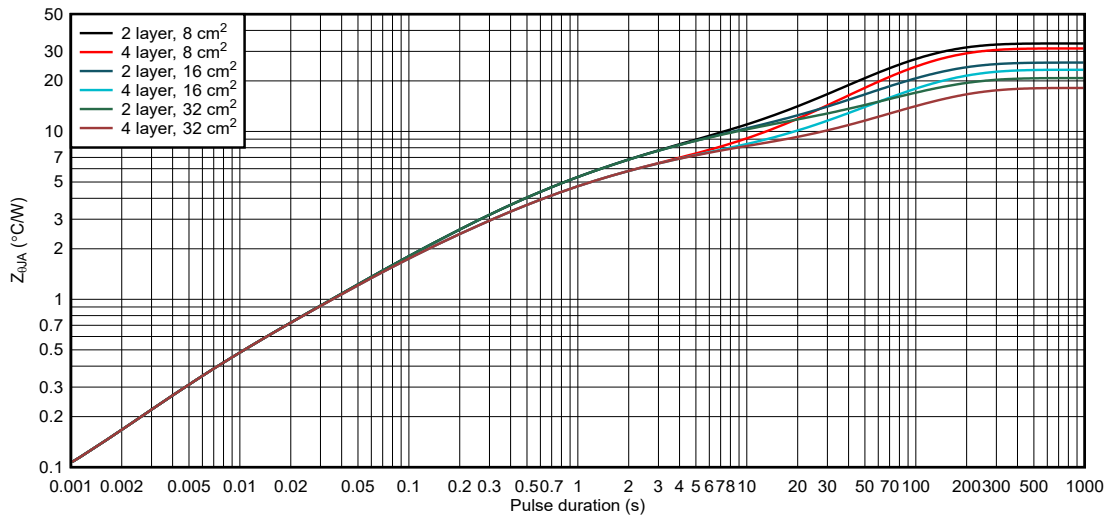


Figure 8-5. DDW package junction-to-ambient thermal impedance for 2oz copper layouts

8.2 DDV Package

The DDV package is designed to interface directly to a heat sink using a thermal interface compound in between, (for example, Ceramique from Arctic Silver, TIMTronics 413, and so forth). The heat sink absorbs heat from the DRV8262 and transfers the heat to the air. With proper thermal management this process can reach equilibrium and heat can be continually transferred from the device. A concept diagram of the heat sink on top of the DDV package is shown in [Figure 8-6](#).

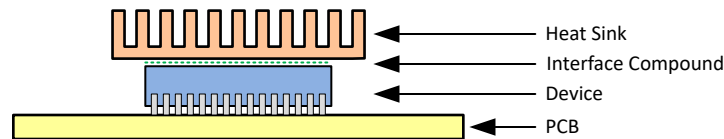


Figure 8-6. Heat sink on DDV Package

Care must be taken when mounting the heat sinks, maintaining good contact with thermal pads and not exceeding the mechanical stress capability of the parts to avoid breakage. The DDV package is capable of tolerating up to 90 Newton load. In production, TI recommend to apply less than 45 Newton load torque.

$R_{\theta JA}$ is a system thermal resistance from junction to ambient air. As such, $R_{\theta JA}$ is a system parameter with the following components:

- $R_{\theta JC}$ of the DDV Package (thermal resistance from junction to exposed pad)
- Thermal resistance of the thermal interface material
- Thermal resistance of the heat sink

$$R_{\theta JA} = R_{\theta JC} + \text{thermal interface resistance} + \text{heat sink resistance}$$

The thermal resistance of the thermal interface material can be determined from the area of the exposed metal package and manufacturer’s value for the area thermal resistance (expressed in $^{\circ}\text{Cmm}^2/\text{W}$). For example, a typical white thermal grease with a 0.0254mm (0.001 inch) thick layer has 4.52 $^{\circ}\text{Cmm}^2/\text{W}$ thermal resistance. The DDV package has an exposed area of 28.7mm². By dividing the area thermal resistance by the exposed metal area determines the thermal resistance for the interface material as 0.157 $^{\circ}\text{C}/\text{W}$.

Heat sink thermal resistance is predicted by the heat sink vendor, modeled using a continuous flow dynamics (CFD) model, or measured. The following are the various important parameters in selecting a heat sink.

1. Thermal resistance
2. Airflow
3. Volumetric resistance

4. Fin density
5. Fin spacing
6. Width
7. Length

The thermal resistance is one parameter that changes dynamically depending on the airflow available.

Airflow is typically measured in LFM (linear feet per minute) or CFM (cubic feet per minute). LFM is a measure of velocity, whereas CFM is a measure of volume. Typically, fan manufacturers use CFM because fans are rated according to the quantity of air 2 can move. Velocity is more meaningful for heat removal at the board level, which is why the derating curves provided by most power converter manufacturers use this.

Typically, airflow is either classified as natural or forced convection.

- Natural convection is a condition with no external induced flow and heat transfer depends on the air surrounding the heat sink. The effect of radiation heat transfer is very important in natural convection, as the effect of radiation heat transfer can be responsible for approximately 25% of the total heat dissipation. Unless the component is facing a hotter surface nearby, having the heat sink surfaces painted to enhance radiation is imperative.
- Forced convection occurs when the flow of air is induced by mechanical means, typically a fan or blower.

Limited thermal budget and space make the choice of a particular type of heat sink very important. This is where the volume of the heat sink becomes relevant. The volume of a heat sink for a given flow condition can be obtained by using the following equation:

$$\text{Volume}_{(\text{heat sink})} = \text{volumetric resistance (Cm}^3 \text{ }^\circ\text{C/W)} / \text{thermal resistance } \theta_{SA} \text{ (}^\circ\text{C/W)}$$

An approximate range of volumetric resistance is given in the following table:

Available Airflow (LFM)	Volumetric Resistance (Cm ³ °C/W)
NC	500 – 800
200	150 - 250
500	80 - 150
1000	50 - 80

The next important criterion for the performance of a heat sink is the width. The width is linearly proportional to the performance of the heat sink in the direction perpendicular to the airflow. An increase in the width of a heat sink by a factor of two, three, or four increase the heat dissipation capability by a factor of two, three, or four. Similarly, the square root of the fin length used is approximately proportional to the performance of the heat sink in the direction parallel to the airflow. In case of an increase in the length of the heat sink by a factor of two, three, or four only increases the heat dissipation capability by a factor of 1.4, 1.7, or 2.

Increasing the width of a heat sink rather than the length is always beneficial if the board has sufficient space. This is only the beginning of an iterative process before the correct and the actual heat sink design is achieved.

The heat sink must be supported mechanically at each end of the IC. This mounting maintains the correct pressure to provide good mechanical, thermal and electrical contact. The heat sink is connected to GND or left floating.

8.3 PCB Material Recommendation

FR-4 Glass Epoxy material with 2 oz. (70 μm) copper on both top and bottom layer is recommended for improved thermal performance and better EMI margin (due to lower PCB trace inductance).

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop designs are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

- Texas Instruments, [Calculating Motor Driver Power Dissipation](#) application report
- Texas Instruments, [Current Recirculation and Decay Modes](#) application report
- Texas Instruments, [Understanding Motor Driver Current Ratings](#) application report
- Texas Instruments, [Motor Drives Layout Guide](#) application report
- Texas Instruments, [Semiconductor and IC Package Thermal Metrics](#) application report
- Texas Instruments, [What Motor Drivers should be considered for driving TEC](#)

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (October 2024) to Revision C (July 2025) Page

- | | |
|------------------------------------|---|
| • Updated CPL/CPH description..... | 3 |
|------------------------------------|---|

Changes from Revision A (July 2023) to Revision B (October 2024) Page

- | | |
|--|---|
| • Removed incomplete device references. | 1 |
|--|---|

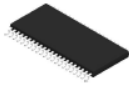
Changes from Revision * (July 2023) to Revision A (July 2023)

Page

- Updated [Table 5-1](#) table..... **8**
-

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

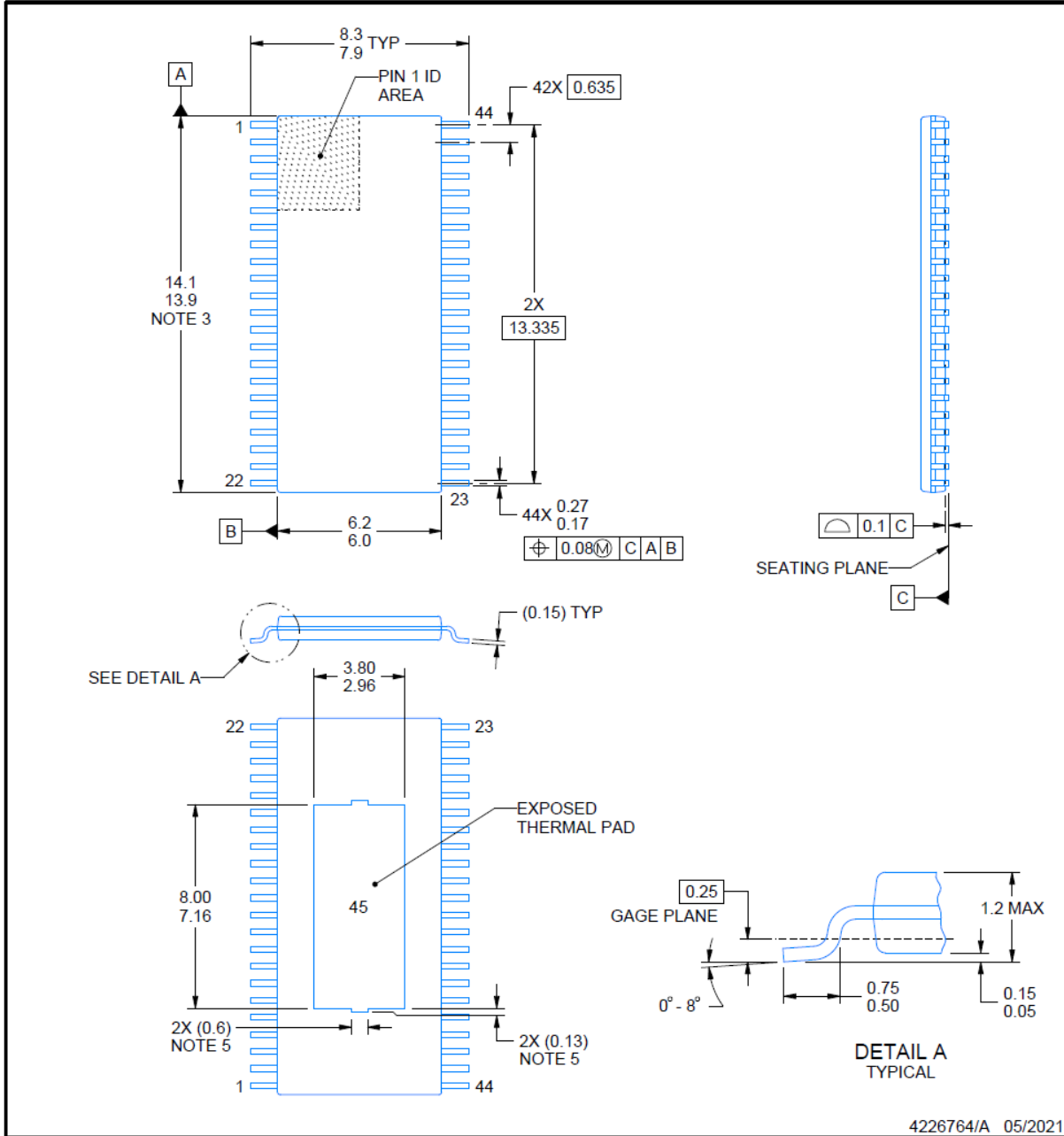


PACKAGE OUTLINE

DDW0044E

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



4226764/A 05/2021

NOTES:

PowerPAD is a trademark of Texas Instruments.

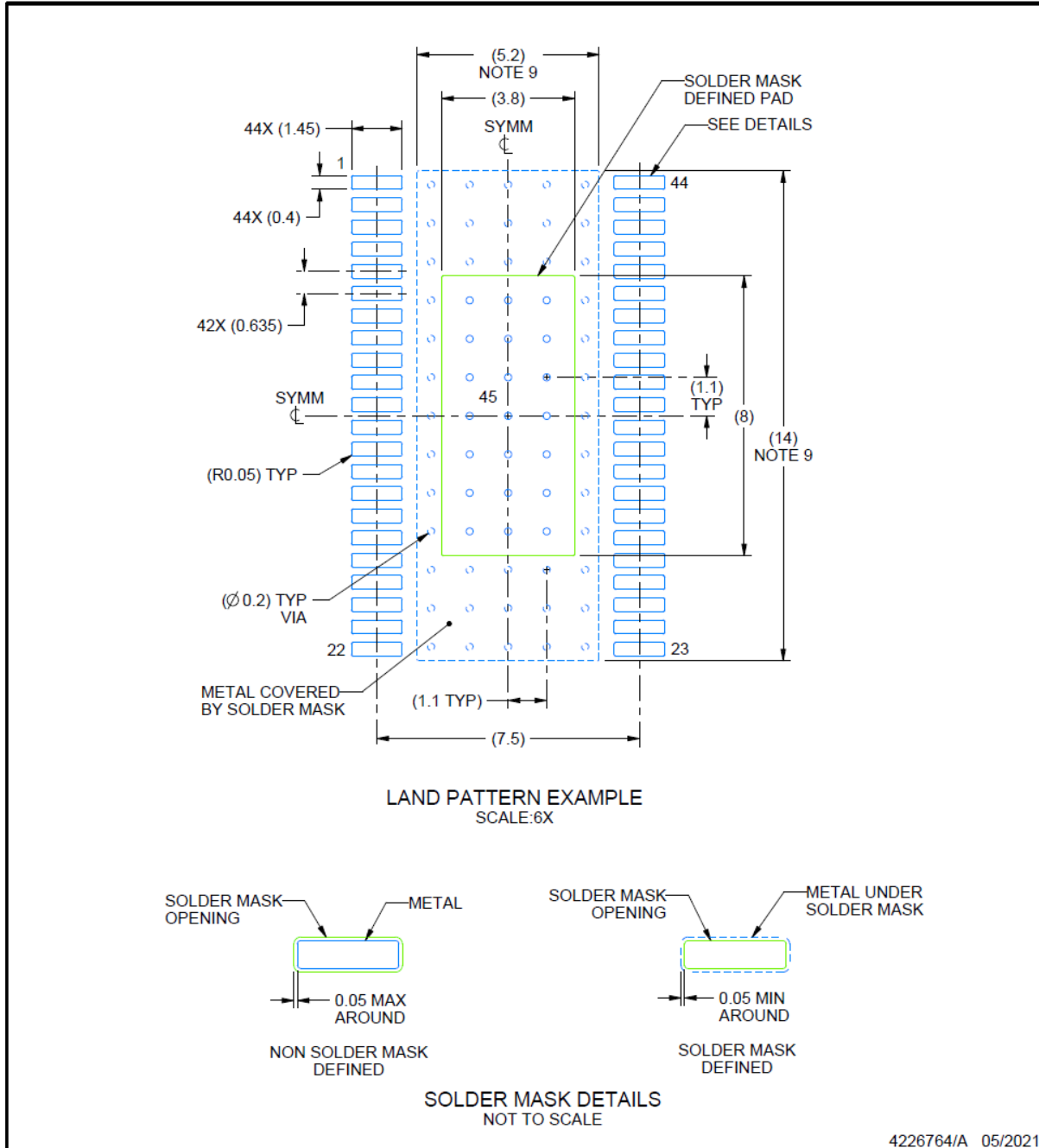
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

DDW0044E

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



NOTES: (continued)

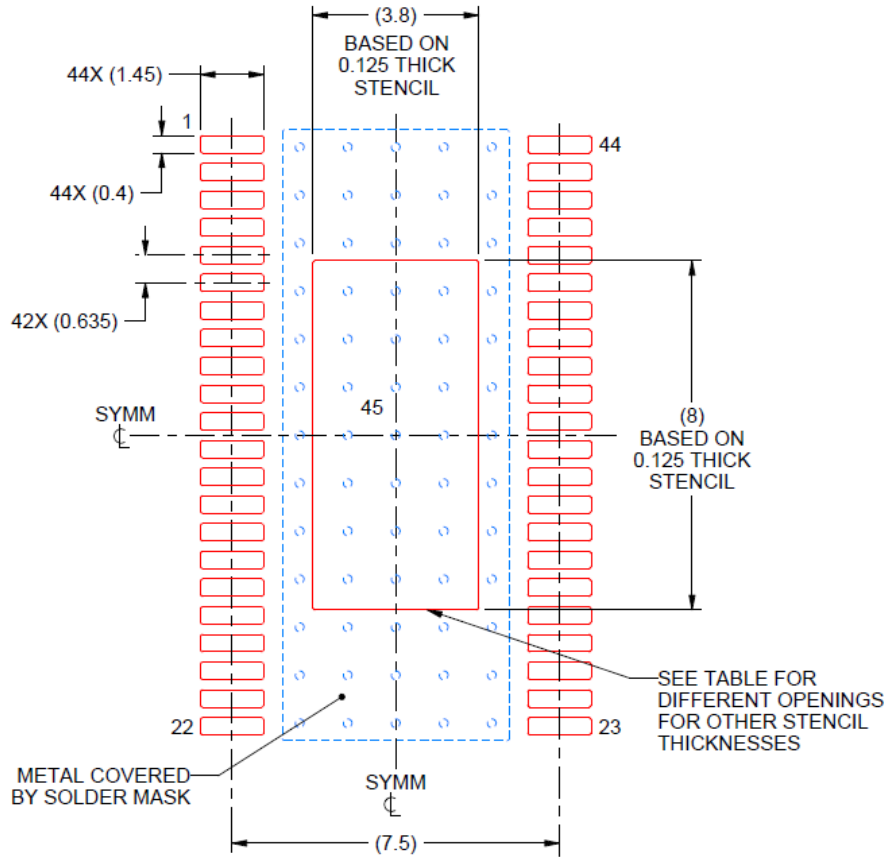
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DDW0044E

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE

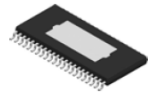
PAD 45:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	4.25 X 8.94
0.125	3.80 X 8.00 (SHOWN)
0.15	3.47 X 7.30
0.175	3.21 X 6.76

4226764/A 05/2021

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

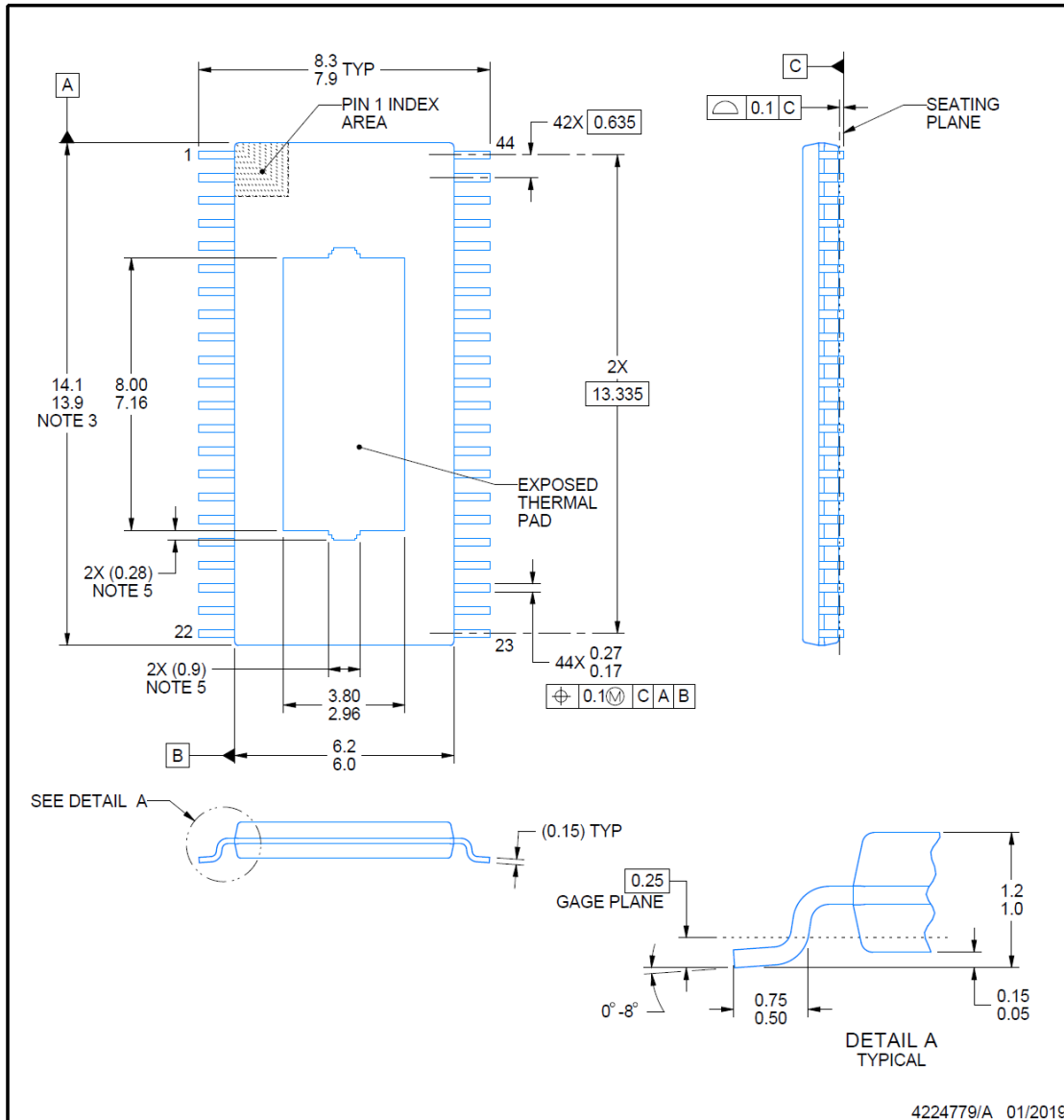


PACKAGE OUTLINE

DDV0044E

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



NOTES:

PowerPAD is a trademark of Texas Instruments.

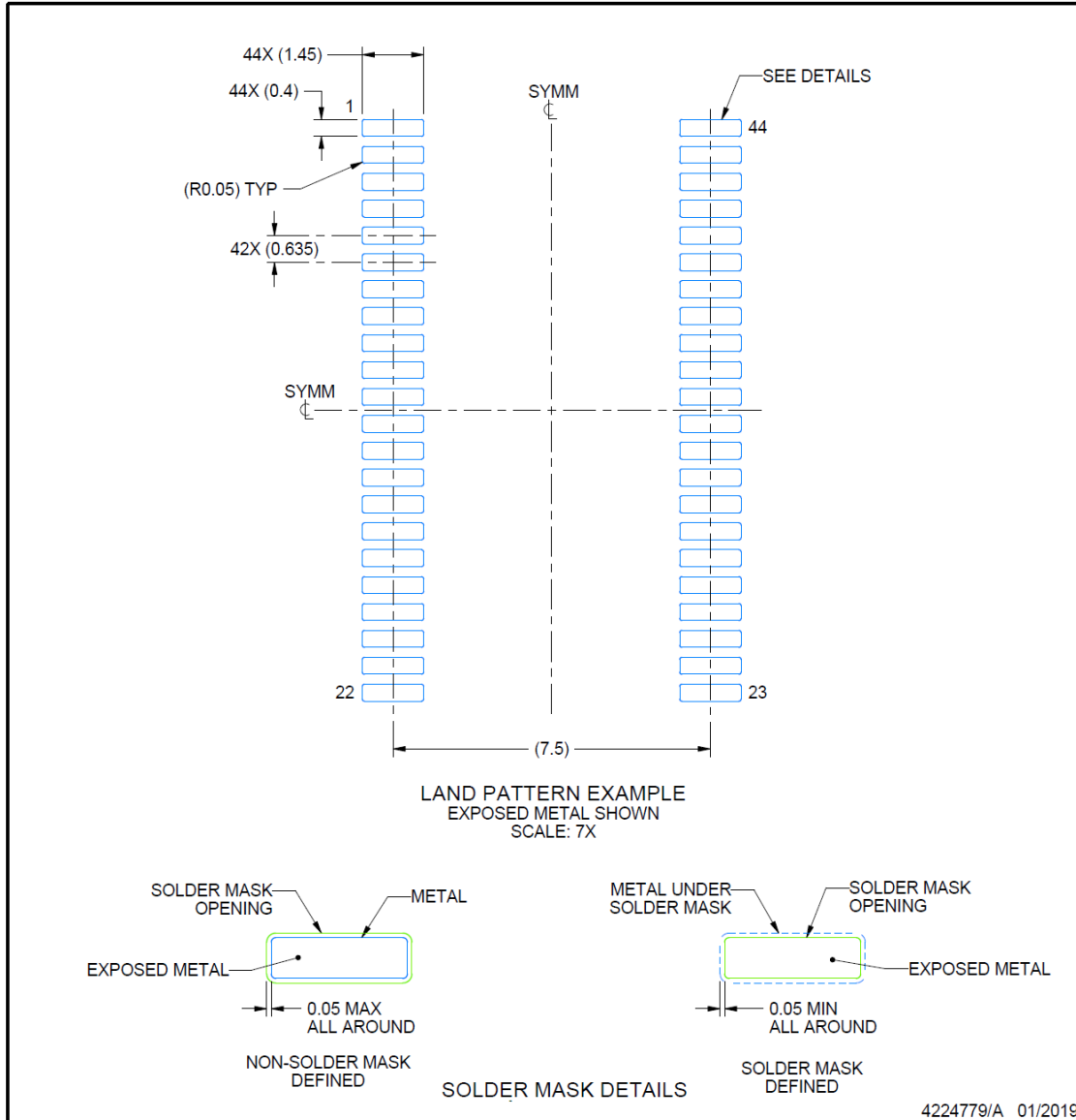
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. The exposed thermal pad is designed to be attached to an external heatsink.
6. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

DDV0044E

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



NOTES: (continued)

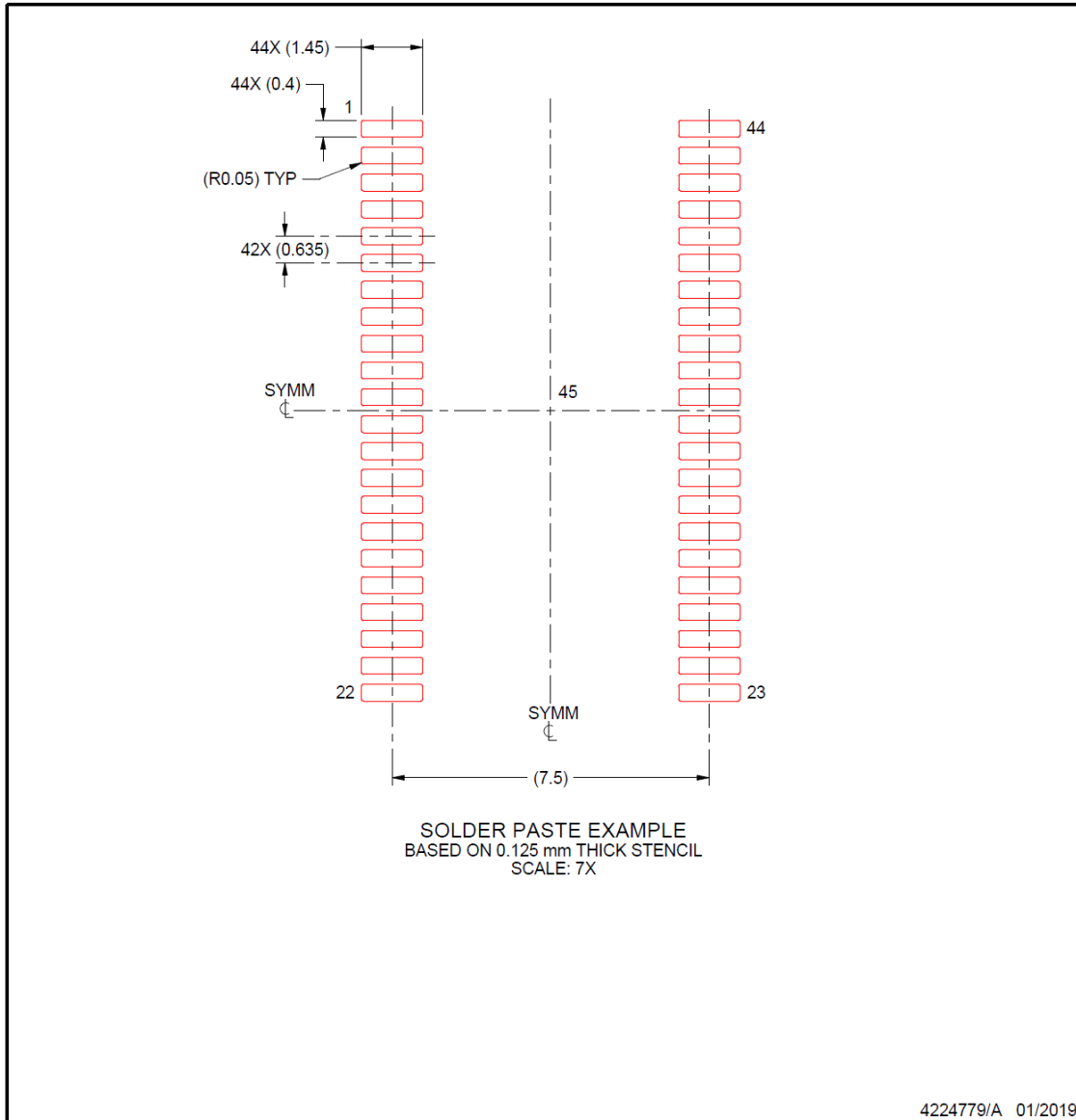
- 7. Publication IPC-7351 may have alternate designs.
- 8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDV0044E

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8262DDVR	Active	Production	HTSSOP (DDV) 44	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8262
DRV8262DDVR.A	Active	Production	HTSSOP (DDV) 44	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8262
DRV8262DDWR	Active	Production	HTSSOP (DDW) 44	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8262
DRV8262DDWR.A	Active	Production	HTSSOP (DDW) 44	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8262

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF DRV8262 :

- Automotive : [DRV8262-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

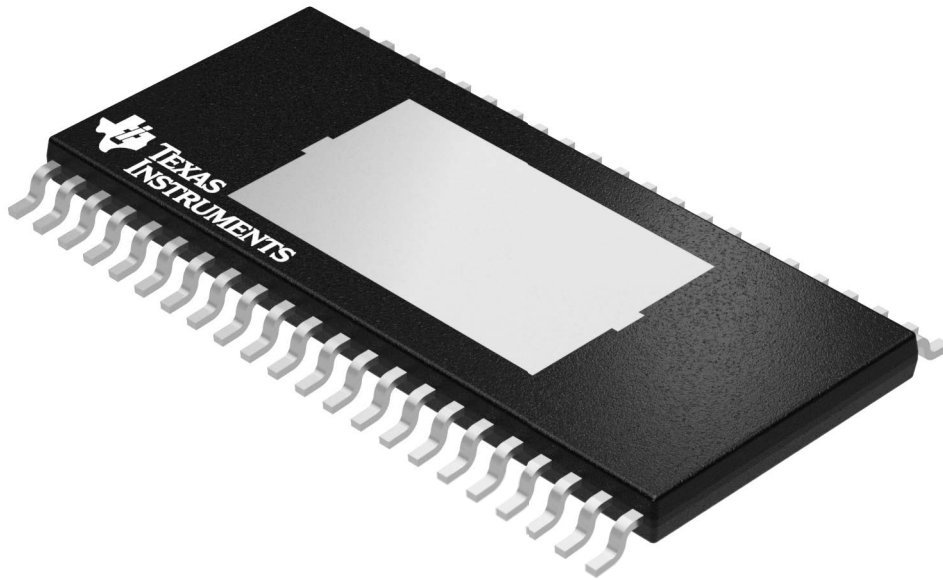

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8262DDVR	HTSSOP	DDV	44	2500	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1
DRV8262DDWR	HTSSOP	DDW	44	2500	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8262DDVR	HTSSOP	DDV	44	2500	356.0	356.0	45.0
DRV8262DDWR	HTSSOP	DDW	44	2500	356.0	356.0	45.0



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

GENERIC PACKAGE VIEW

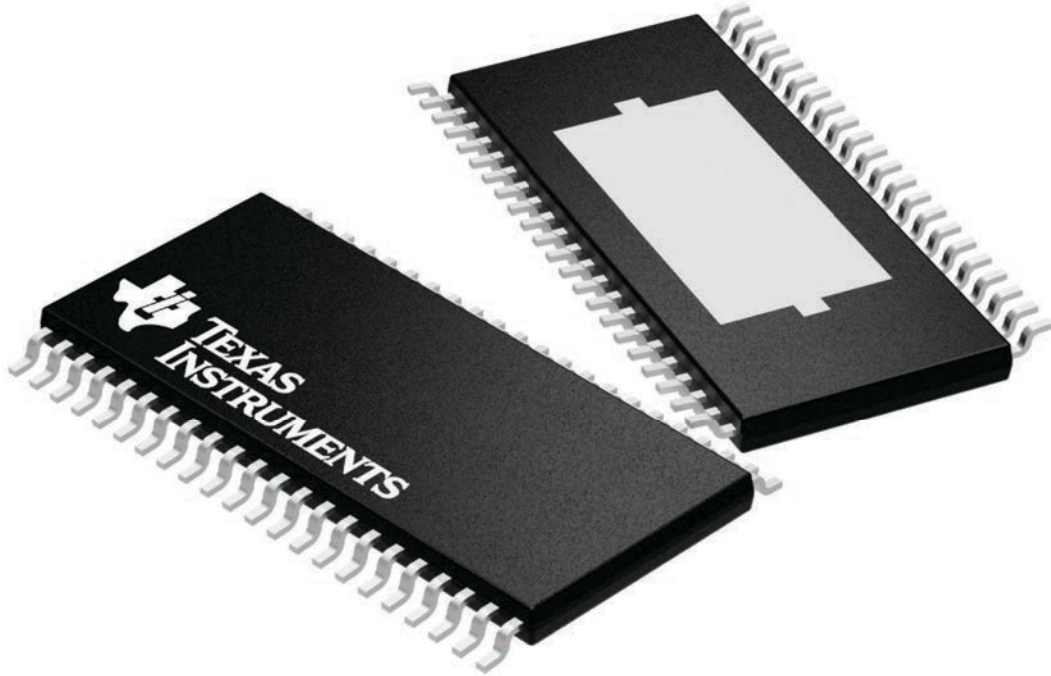
DDW 44

PowerPAD TSSOP - 1.2 mm max height

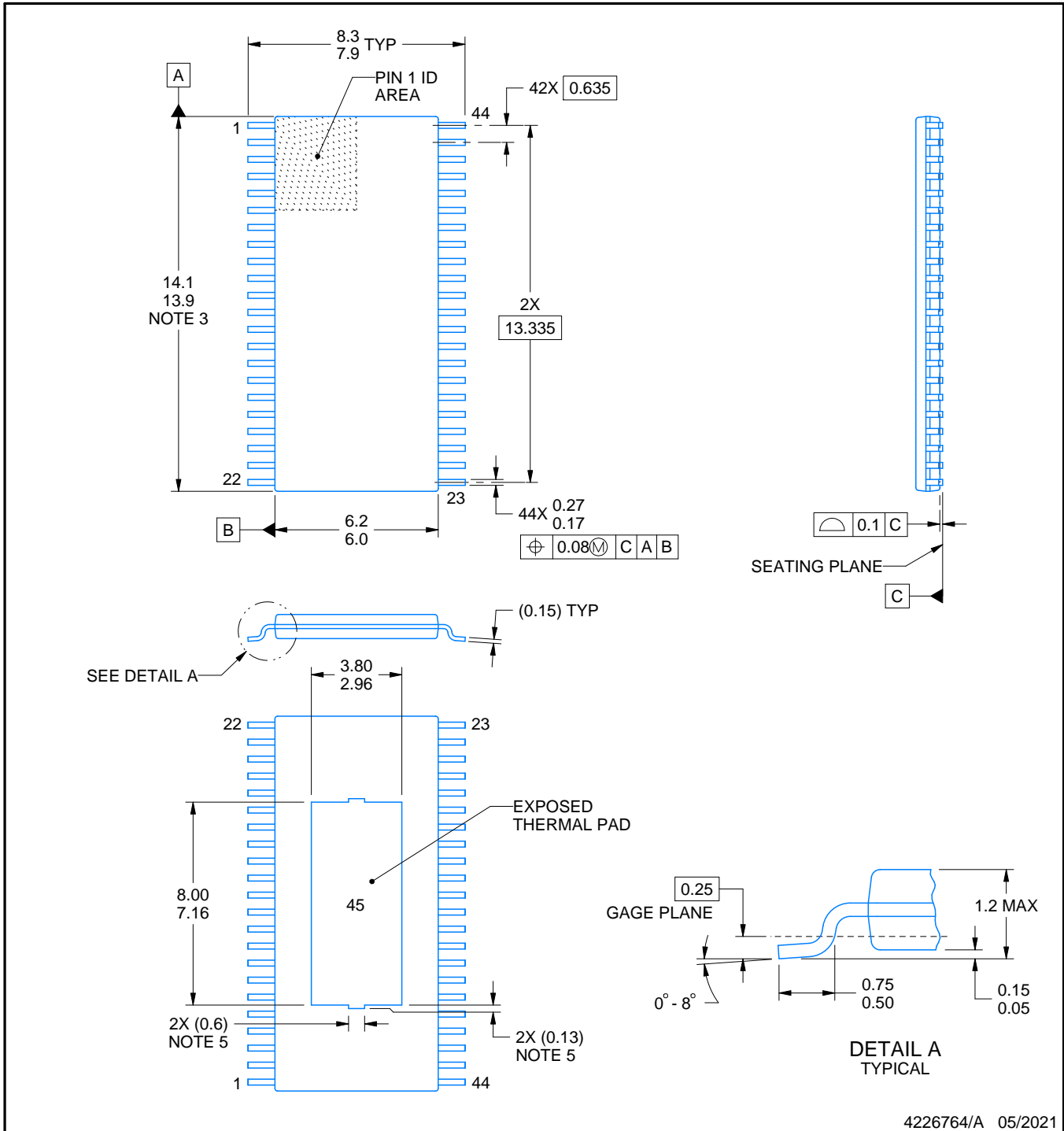
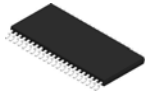
6.1 x 14, 0.635 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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NOTES:

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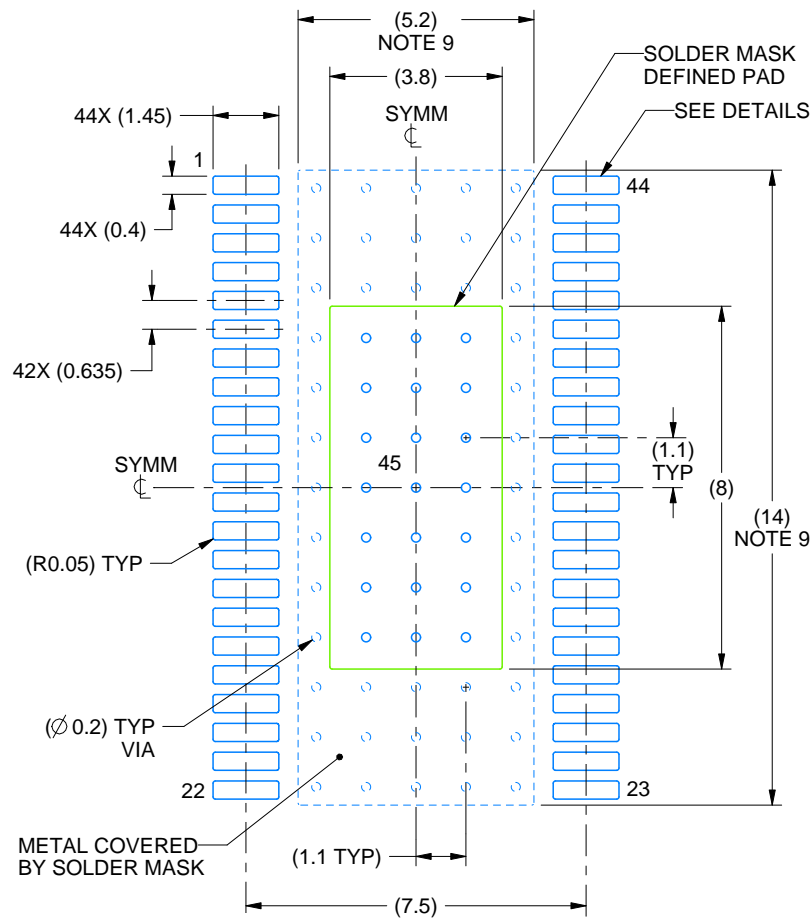
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

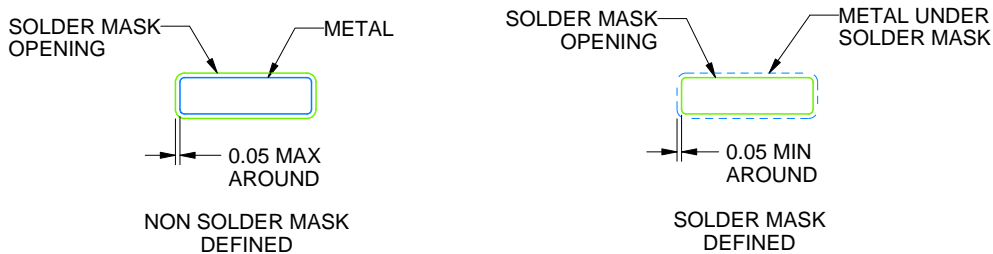
DDW0044E

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS
NOT TO SCALE

4226764/A 05/2021

NOTES: (continued)

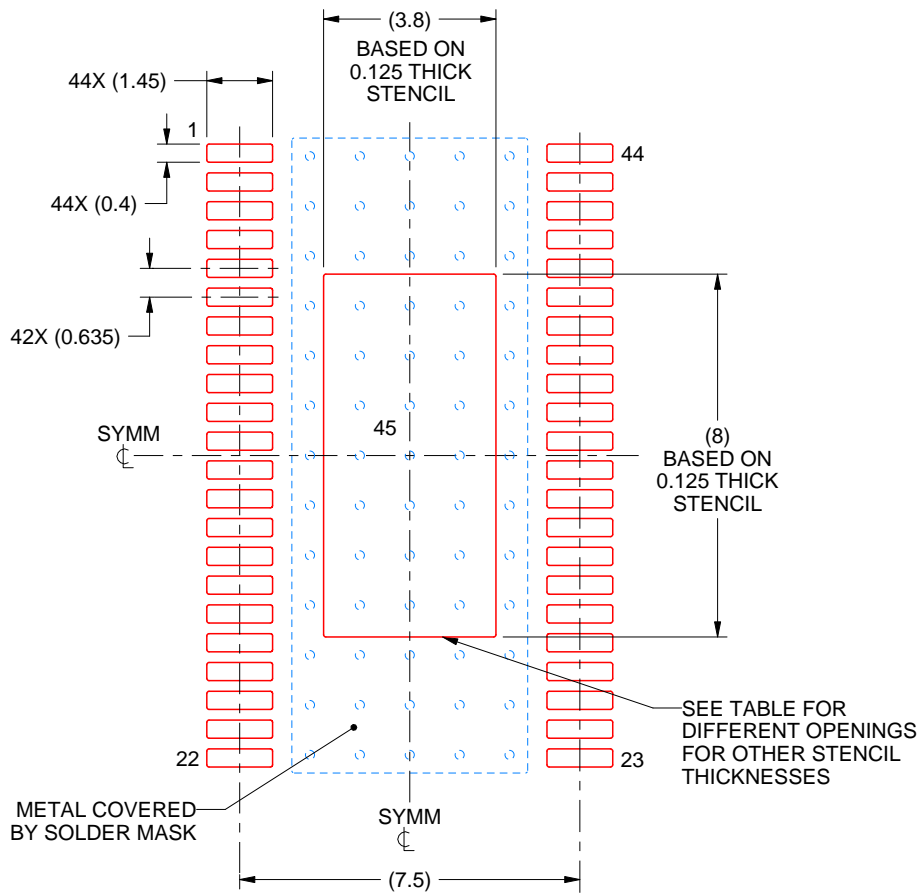
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DDW0044E

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
 PAD 45:
 100% PRINTED SOLDER COVERAGE BY AREA
 SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	4.25 X 8.94
0.125	3.80 X 8.00 (SHOWN)
0.15	3.47 X 7.30
0.175	3.21 X 6.76

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025