DRV8839 Low-Voltage Dual ½-H-Bridge Driver IC

1 Features

- Dual ½-H-Bridge Motor Driver
  - Drives a DC Motor or One Winding of a Stepper Motor, or Other Loads
  - Low MOSFET ON-Resistance: HS + LS 280 mΩ
- 1.8-A Maximum Drive Current
- Separate Motor and Logic Supply Pins:
  - 0-V to 11-V Motor-Operating Supply-Voltage
  - 1.8-V to 7-V Logic Supply-Voltage
- Individual ½-H-Bridge Control Input Interface
- Low-Power Sleep Mode With 120-nA Maximum Combined Supply Current
- 2.00-mm × 3.00-mm 12-Pin WSON Package

2 Applications

- Battery-Powered:
  - DSLR Lenses
  - Consumer Products
  - Toys
  - Robotics
  - Cameras
  - Medical Devices

3 Description

The DRV8839 provides a versatile power driver solution for cameras, consumer products, toys, and other low-voltage or battery-powered applications. The device has two independent ½-H-bridge drivers and can drive one DC motor or one winding of a stepper motor, as well as other devices like solenoids. The output stages use N-channel power MOSFETs configured as ½-H-bridges. An internal charge pump generates needed gate-drive voltages.

The DRV8839 can supply up to 1.8-A of output current. It operates on a motor power supply voltage from 0 V to 11 V and a device power supply voltage of 1.8 V to 7 V.

The DRV8839 has independent input and enable pins for each ½-H-bridge which allow independent control of each output.

Internal shutdown functions are provided for overcurrent protection, short-circuit protection, undervoltage lockout, and overtemperature.

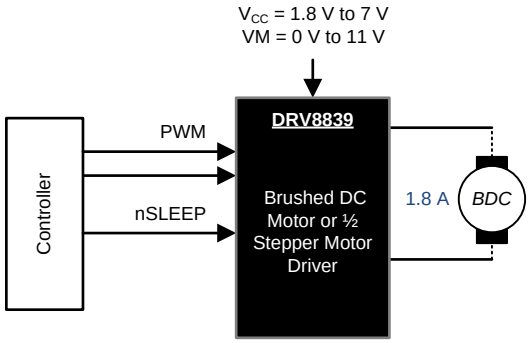
The DRV8839 is packaged in a 12-pin, 2.00-mm × 3.00-mm WSON package (Eco-friendly: RoHS and no Sb/Br).

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8839	WSON (12)	2.00 mm × 3.00 mm

(1) For all available packages, see the Orderable Addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (December 2015) to Revision C — **Page**

- Deleted nFAULT from the *Simplified Schematic* ... 1
- Deleted the NC pins from the *Pin Functions* table ... 3
- Changed the value of the capacitor on the VM pin from 10 µF to 0.1 µF in the *Typical Application Schematic* ... 12
- Changed the *Layout Guidelines* to clarify the guidelines for the VM pin ... 15
- Deleted references to TI's PowerPAD package and updated it with thermal pad where applicable ... 16
- Added the *Receiving Notification of Documentation Updates* section ... 17

Changes from Revision A (January 2014) to Revision B — **Page**

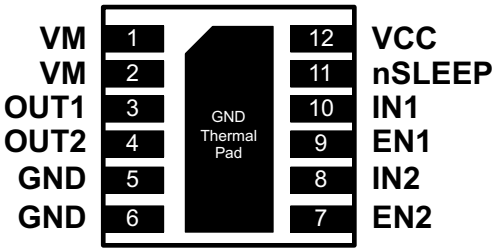
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Original (January 2013) to Revision A — **Page**

- Changed *Features* bullet ... 1
- Changed motor supply voltage range in *Description* section ... 1
- Changed Motor power supply voltage range in *Recommended Operating Conditions* ... 4
- Added t_{OCR} and t_{DEAD} parameters to *Electrical Characteristics* ... 5
- Added paragraph to *Power Supplies* and *Input Pins* section ... 14

5 Pin Configuration and Functions

DSS Package
12-Pin WSON With Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O (1)	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NO.			
POWER AND GROUND				
GND, Thermal pad	5, 6	—	Device ground	
VCC	12	—	Device supply	Bypass to GND with a 0.1-μF, 6.3-V ceramic capacitor
VM	1, 2	—	Motor supply	Bypass to GND with a 0.1-μF, 16-V ceramic capacitor
CONTROL				
EN1	9	I	Enable 1	Logic high enables OUT1 Internal pulldown resistor
EN2	7	I	Enable 2	Logic high enables OUT2 Internal pulldown resistor
IN1	10	I	Input 1	Logic input controls OUT1 Internal pulldown resistor
IN2	8	I	Input 2	Logic input controls OUT2 Internal pulldown resistor
nSLEEP	11	I	Sleep mode input	Logic low puts device in low-power sleep mode Logic high for normal operation Internal pulldown resistor
OUTPUT				
OUT1	3	O	Output 1	Connect to motor winding
OUT2	4	O	Output 2	

(1) Directions: I = input, O = output, OZ = tri-state output, OD = open-drain output, IO = input/output.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
	Power supply voltage, VM	–0.3	12	V
	Power supply voltage, VCC	–0.3	7	V
	Digital input pin voltage	–0.5	7	V
	Peak motor drive output current	Internally limited		A
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

T_A = 25°C (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Device power supply voltage	1.8		7	V
V_M	Motor power supply voltage	0		11	V
V_{IN}	Logic level input voltage	0		5.5	V
I_{OUT}	H-bridge output current (1)	0		1.8	A
f_{PWM}	Externally applied PWM frequency	0		250	kHz

(1) Power dissipation and thermal limits must be observed.

6.4 Thermal Information

THERMAL METRIC(1)		DRV8839 DSS (WSON) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	50.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	20	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_A = 25°C, V_M = 5 V, V_{CC} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_{VM}	VM operating supply current	No PWM		40	100	µA
		50 kHz PWM		0.8	1.5	mA
I_{VMQ}	VM sleep mode supply current	nSLEEP = 0 V		30	95	nA
I_{VCC}	VCC operating supply current	No PWM		300	500	µA
		50 kHz PWM		0.7	1.5	mA
I_{VCCQ}	VCC sleep mode supply current	nSLEEP = 0 V		5	25	nA
V_{UVLO}	VCC undervoltage lockout voltage	V_{CC} rising			1.8	V
		V_{CC} falling			1.7	
LOGIC-LEVEL INPUTS						
V_{IL}	Input low voltage		0.31 × V_{CC}	0.34 × V_{CC}		V
V_{IH}	Input high voltage			0.39 × V_{CC}	0.43 × V_{CC}	V
V_{HYS}	Input hysteresis			0.08 × V_{CC}		V
I_{IL}	Input low current	V_{IN} = 0	–5		5	µA
I_{IH}	Input high current	V_{IN} = 3.3 V			50	µA
R_{PD}	Pulldown resistance			100		kΩ
H-BRIDGE FETS						
$R_{DS(ON)}$	HS + LS FET on resistance	I_O = 800 mA, T_J = 25°C		280	330	mΩ
I_{OFF}	OFF-state leakage current				±200	nA
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level		1.9		3.5	A
t_{OCR}	Overcurrent protection retry time			1		ms
t_{DEAD}	Output dead time			100		ns
t_{TSD}	Thermal shutdown temperature	Die temperature	150	160	180	°C

6.6 Timing Requirements (1)

T_A = 25°C, V_M = 5 V, V_{CC} = 3 V, R_L = 20 Ω

			MIN	MAX	UNIT
1	t_1	Output enable time		120	ns
2	t_2	Output disable time		120	ns
3	t_3	Delay time, INx high to OUTx high		120	ns
4	t_4	Delay time, INx low to OUTx low		120	ns
5	t_5	Output rise time	50	150	ns
6	t_6	Output fall time	50	150	ns

(1) Not production tested – ensured by design

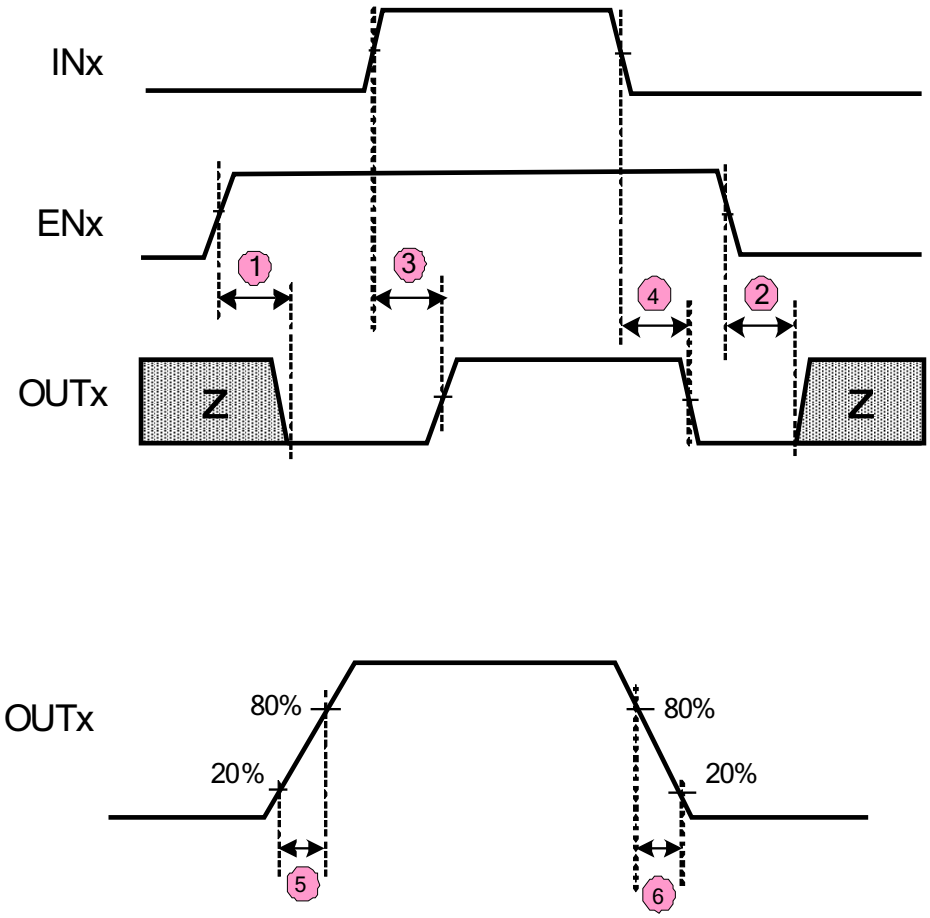


Figure 1. Timing Requirements

6.7 Typical Characteristics

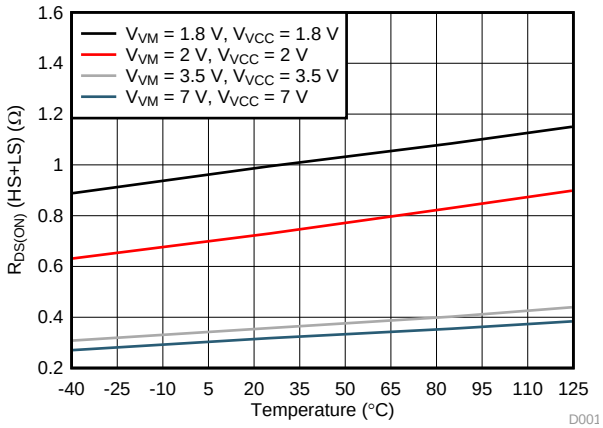


Figure 2. $R_{DS(ON)}$ HS + LS vs Temperature

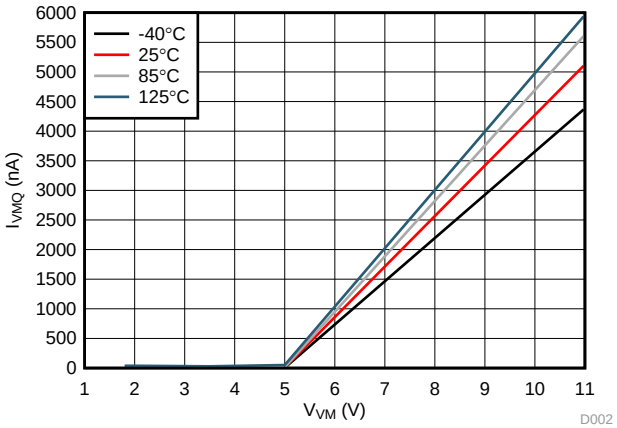


Figure 3. I_{VMQ} vs V_{VM}

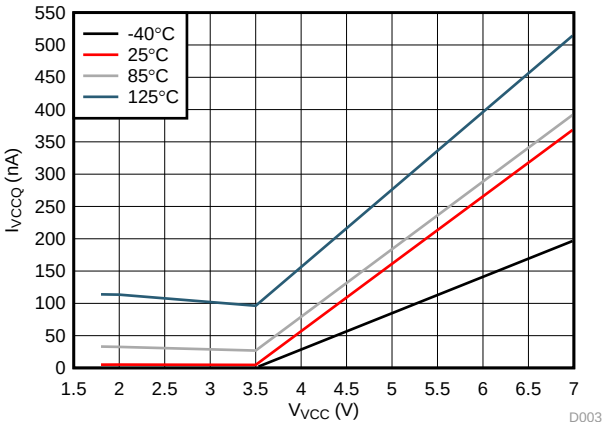


Figure 4. I_{VCCQ} vs V_{VCC}

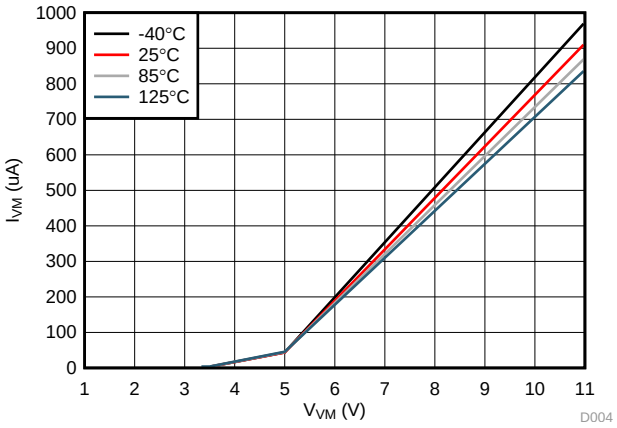


Figure 5. I_{VM} vs V_{VM} (No PWM)

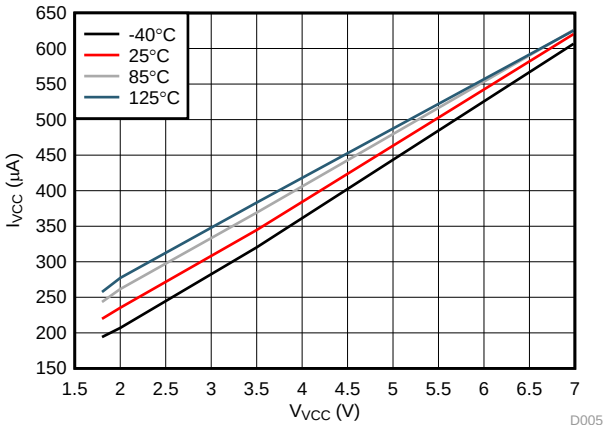


Figure 6. I_{VCC} vs V_{VCC} (No PWM)

7 Detailed Description

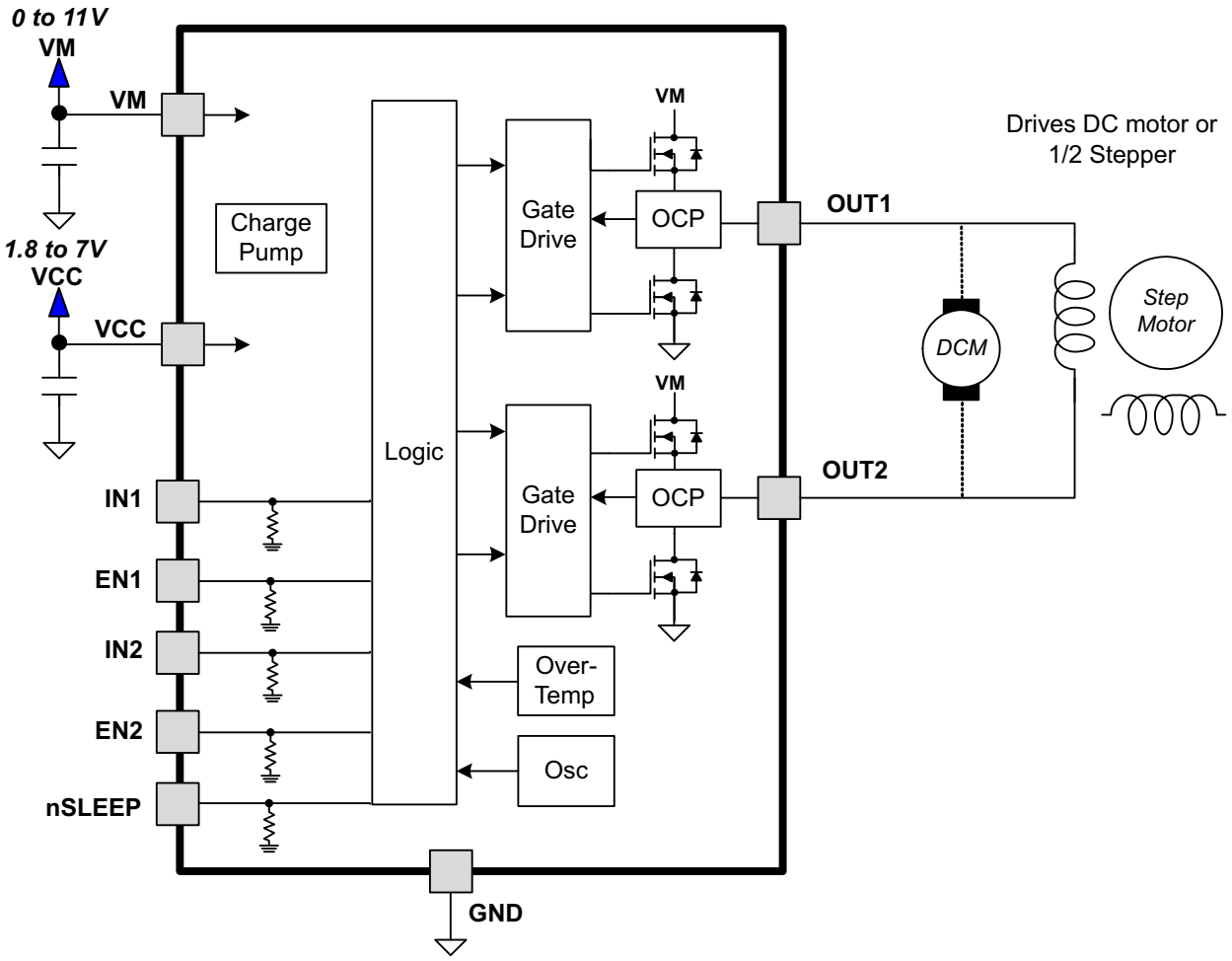
7.1 Overview

The DRV8839 is an integrated motor driver solution used for brushed motor control. The device integrates two independent ½ H-bridge, and can drive one motor in both directions or two motors in one direction. The output driver block for each ½ H-bridge consists of N-channel power MOSFETs. An internal charge pump generates the gate drive voltages. Protection features include overcurrent protection, short-circuit protection, undervoltage lockout, and overtemperature protection.

The DRV8839 allows separation of the motor voltage and logic voltage if desired. If VM and VCC are less than 7 V, the two voltages may be connected.

The control interface of the DRV8839 uses INx and ENx to control each ½ H-bridge separately.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Protection Circuits

The DRV8839 is fully protected against undervoltage, overcurrent, and overtemperature events.

7.3.1.1 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the OCP time, all FETs in the H-bridge disables. After approximately 1 ms, the bridge will be re-enabled automatically.

Overcurrent conditions on both high-side and low-side devices; a short to ground, supply, or across the motor winding result in an overcurrent shutdown.

7.3.1.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge disables. Operation automatically resumes once the die temperature has fallen to a safe level.

7.3.1.3 Undervoltage Lockout (UVLO)

If at any time the voltage on the VCC pin falls below the undervoltage lockout threshold voltage, all circuitry in the device disables and internal logic resets. Operation resumes when VCC rises above the UVLO threshold.

Table 1. Device Protection

FAULT	CONDITION	ERROR REPORT	H-BRIDGE	INTERNAL CIRCUITS	RECOVERY
VCC undervoltage (UVLO)	VCC < VUVLO	None	Disabled	Disabled	VCC > VUVLO
Overcurrent (OCP)	IOUT > IOCP	None	Disabled	Operating	tOCR
Thermal shutdown (TSD)	TJ > TTSD	None	Disabled	Operating	TJ < TTSD – THYS

7.4 Device Functional Modes

The DRV8839 is active when the nSLEEP pin is set to a logic high. When in sleep mode, the ½ H-bridge FETs are disabled (High-Z).

Table 2. Device Operating Modes

OPERATING MODE	CONDITION	H-BRIDGE	INTERNAL CIRCUITS
Operating	nSLEEP high	Operating	Operating
Sleep mode	nSLEEP low	Disabled	Disabled
Fault encountered	Any fault condition met	Disabled	See Table 1

7.4.1 Bridge Control

The DRV8839 is controlled using separate enable and input pins for each ½-H-bridge.

The following table shows the logic for the DRV8839:

Table 3. Bridge Control

ENx	INx	OUTx
0	X	Z
1	0	L
1	1	H

7.4.2 Sleep Mode

If the nSLEEP pin reaches a logic-low state, the DRV8839 enters a low-power sleep mode. In this state all unnecessary internal circuitry powers down.

7.4.3 Motor Connections

If a single DC motor connects to the DRV8839, it is connected between the OUT1 and OUT2 pins as shown in Figure 7:

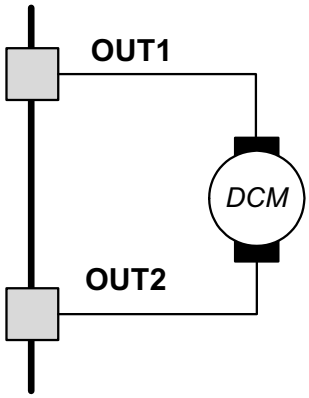


Figure 7. Single DC Motor Connection

Motor operation is controlled as show in Table 4.

Table 4. Single DC Motor Operation

EN1	EN2	IN1	IN2	OUT1	OUT2	MOTOR OPERATION
0	X	X	X	Z	See (1)	Off (coast)
X	0	X	X	See (2)	Z	Off (coast)
1	1	0	0	L	L	Brake
1	1	0	1	L	H	Reverse
1	1	1	0	H	L	Forward
1	1	1	1	H	H	Brake

(1) State depends on EN2 and IN2, but does not affect motor operation because OUT1 is tri-stated.
(2) State depends on EN1 and IN1, but does not affect motor operation because OUT2 is tri-stated.

Two DC motors can be connected to the DRV8839. In this mode, it is not possible to reverse the direction of the motors; they turn only in one direction. The connections are shown in Figure 8:

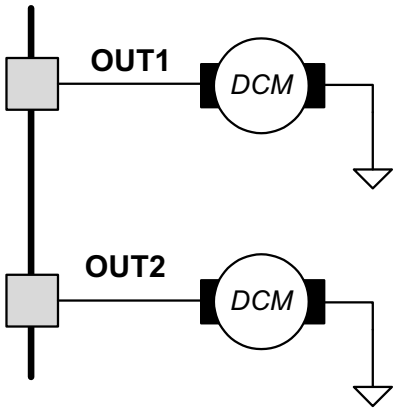


Figure 8. Dual DC Motor Connection

Motor operation is controlled shown in Table 5.

Table 5. Dual DC Motor Operation

ENx	INx	OUTx	MOTOR OPERATION
0	X	Z	Off (coast)
1	0	L	Brake
1	1	H	Forward

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8839 is used in one control applications.

8.2 Typical Application

The following design is a common application of the DRV8839.

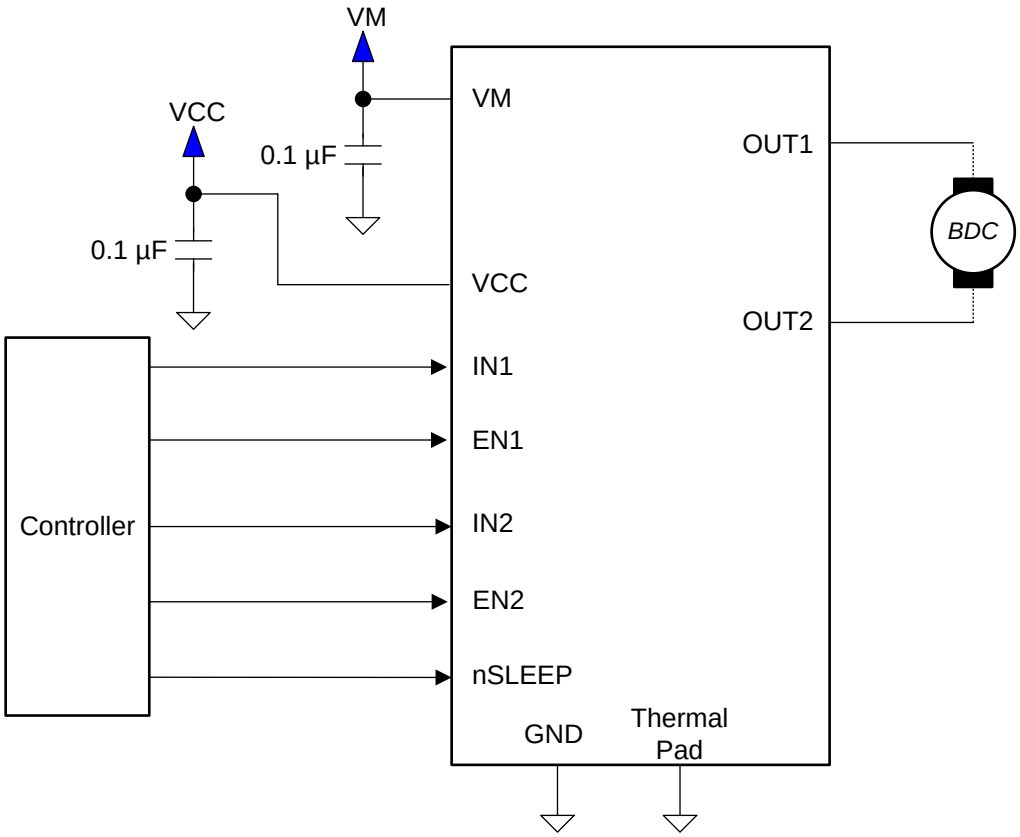


Figure 9. Typical Application Schematic

8.2.1 Design Requirements

The design requirements are shown in Table 6.

Table 6. Design Requirements

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor voltage	VM	5 V
Motor RMS current	IRMS	0.3 A
Motor startup current	ISTART	0.6 A

8.2.2 Detailed Design Procedure

The following design procedure can be used to configure the DRV8839 in a brushed motor application.

8.2.2.1 Motor Voltage

The appropriate motor voltage depends on the ratings of the motor selected and the desired RPM. A higher voltage spins a brushed DC motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

8.2.2.2 Low-Power Operation

When entering sleep mode, TI recommends setting all inputs as a logic low to minimize system power.

8.2.2.3 Application Curves

The following scope captures show a typical motor startup and running. Channel 1 is VM, Channel 2 is IN1, Channel 3 is IN2, and Channel 4 is motor current. the motor used is a NMB Technologies, PPN7PA12C1.

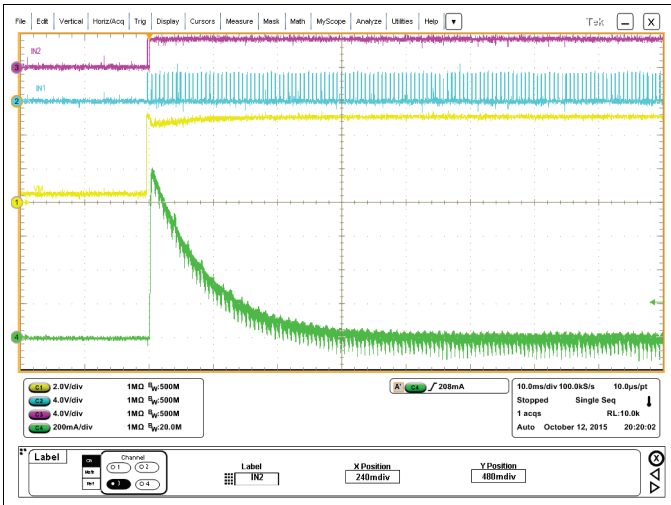


Figure 10. Motor Startup With VCC = 3.3 V, VM = 5 V

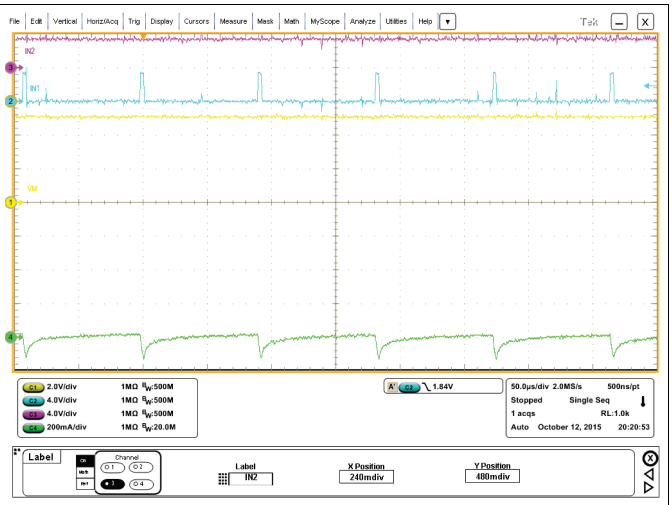


Figure 11. Motor Running With VCC = 3.3 V, VM = 5 V

9 Power Supply Recommendations

The input pins can drive within their recommended operating conditions with or without the VCC and VM power supplies present. No leakage current path exists to the supply. There is a weak pulldown resistor (approximately 100 kΩ) to ground on each input pin.

VCC and VM can be applied and removed in any order. When VCC is removed, the device enters a low-power state and draws very little current from VM. If the supply voltage is between 1.8 V and 7 V, VCC and VM can connect together.

The VM voltage supply does not have any undervoltage lockout protection (UVLO), so as long as VCC > 1.8 V, the internal device logic remains active. This means that the VM pin voltage may drop to 0 V, however, the load may not be sufficiently driven at low VM voltages.

9.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The required amount of local capacitance depends on a variety of factors, including:

- The highest current required by the motor system
- The power supply's capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

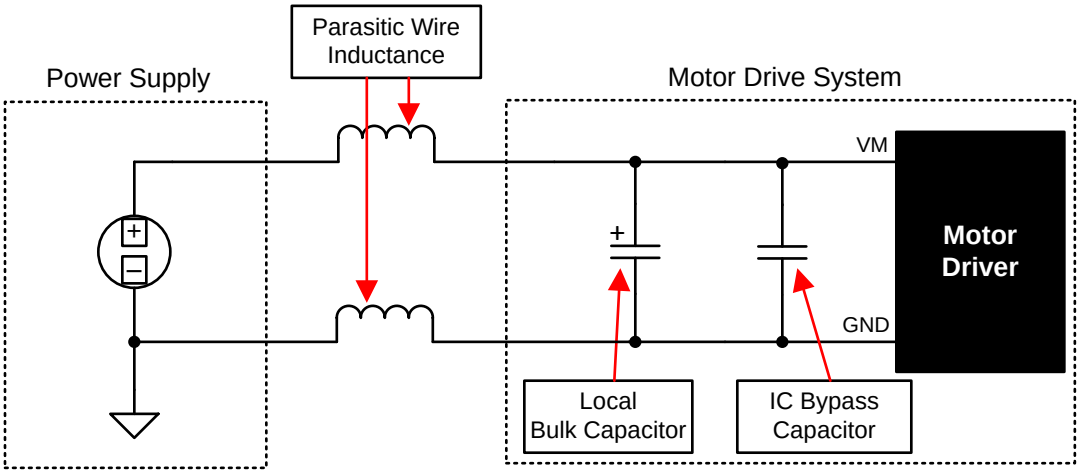


Figure 12. Bulk Capacitance

10 Layout

10.1 Layout Guidelines

The VCC pin should be bypassed to GND using low-ESR ceramic bypass capacitors with a recommended value of 0.1-µF rated for VCC. This capacitor should be placed as close to the VCC pin as possible with a thick trace.

The VM pin should be bypassed to GND using low-ESR ceramic bypass capacitors with a recommended value of 0.1 µF rated for VM. This capacitor should be placed as close to the VM pin as possible with a thick trace. The VM pin must bypass to ground using an appropriate bulk capacitor. This component can be an electrolytic and should be located close to the DRV8839 device.

10.2 Layout Example

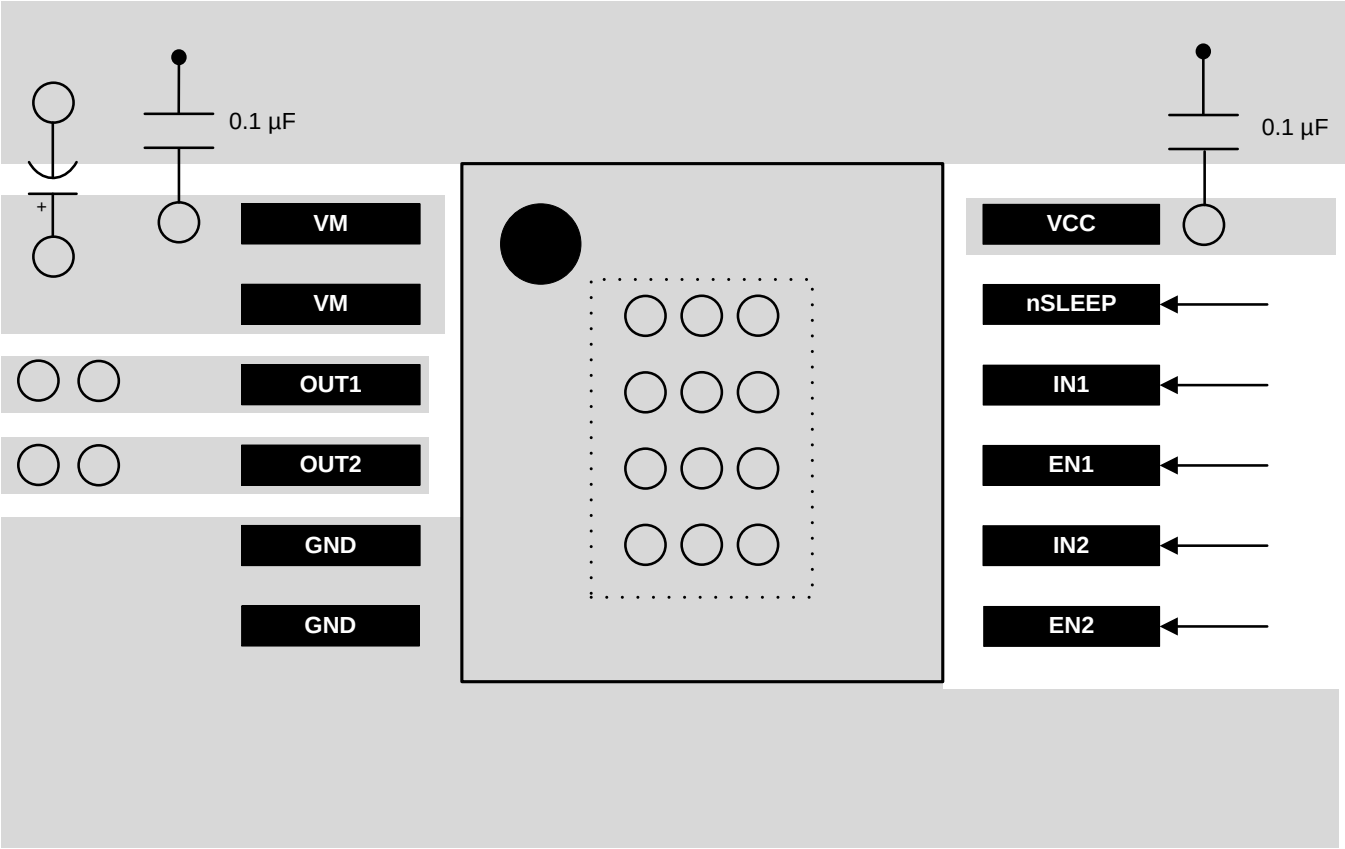


Figure 13. Layout Recommendation

10.3 Thermal Considerations

The DRV8839 has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 150°C, the device disables until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

10.3.1 Power Dissipation

The power dissipation of the DRV8839 is a function of RMS motor current and the each output's FET resistance ($R_{DS(ON)}$) as seen in Equation 1:

$$\text{Power} \approx I_{RMS}^2 \times (\text{High-Side } R_{DS(ON)} + \text{Low-Side } R_{DS(ON)} \quad (1)$$

Thermal Considerations (continued)

For this example, V_{VM} = 1.8 V, V_{VCC} = 1.8 V, the ambient temperature is 35°C, and the junction temperature reaches 65°C. At 65°C, the sum of $R_{DS(ON)}$ is about 1 Ω. With an example motor current of 0.8 A, the dissipated power in the form of heat will be 0.8 A² × 1 Ω = 0.64 W.

The temperature that the DRV8839 reaches will depend on the thermal resistance to the air and PCB. It is important to solder the device thermal pad to the PCB ground plane, with vias to the top and bottom board layers, in order dissipate heat into the PCB and reduce the device temperature. In the example used here, the DRV8839 had an effective thermal resistance $R_{\theta JA}$ of 47°C/W, and as shown in Equation 2:

$$T_J = T_A + (P_D \times R_{\theta JA}) = 35°C + (0.64\ W \times 47°C/W) = 65°C \quad (2)$$

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *AN-1187 Leadless Leadframe Package (LLP)* (SNOA401)
- *DRV8839 Evaluation Module* (SLVU879)
- *QFN/SON PCB Attachment* (SLUA271)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8839DSSR	Active	Production	WSON (DSS) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	8839
DRV8839DSSR.B	Active	Production	WSON (DSS) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	8839
DRV8839DSSRG4	Active	Production	WSON (DSS) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	8839
DRV8839DSSRG4.B	Active	Production	WSON (DSS) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	8839

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

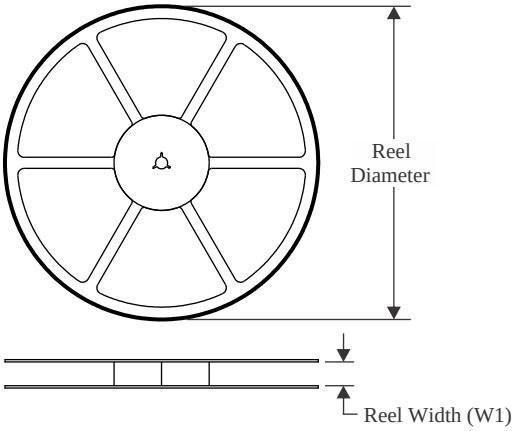
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

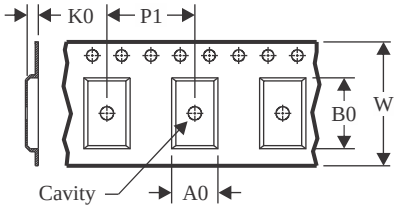
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

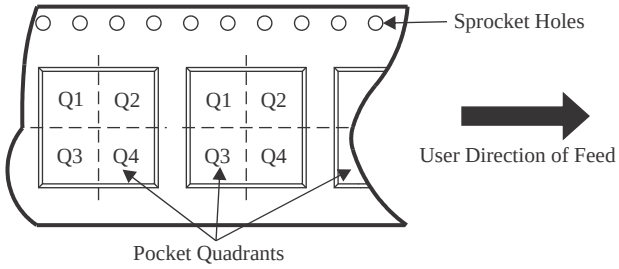


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

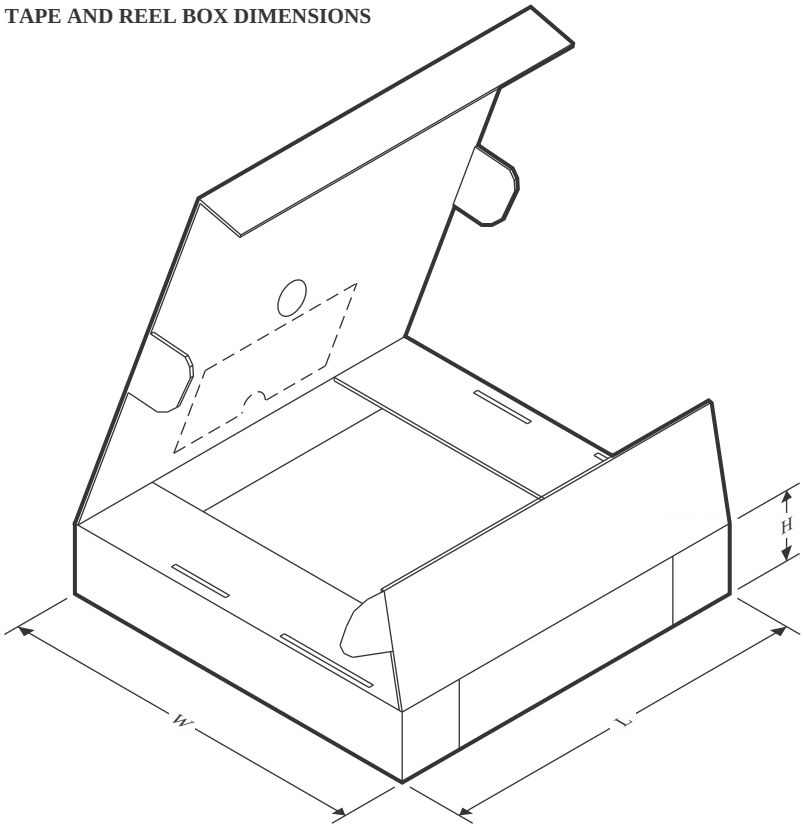
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8839DSSR	WSON	DSS	12	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
DRV8839DSSRG4	WSON	DSS	12	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



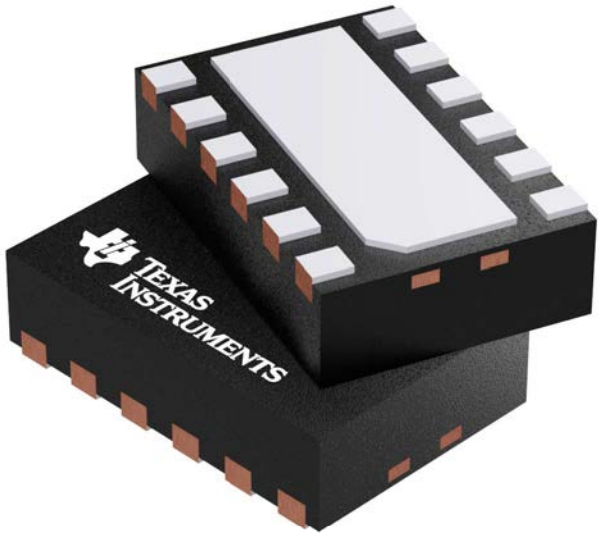
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8839DSSR	WSON	DSS	12	3000	182.0	182.0	20.0
DRV8839DSSRG4	WSON	DSS	12	3000	182.0	182.0	20.0

GENERIC PACKAGE VIEW

DSS 12 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



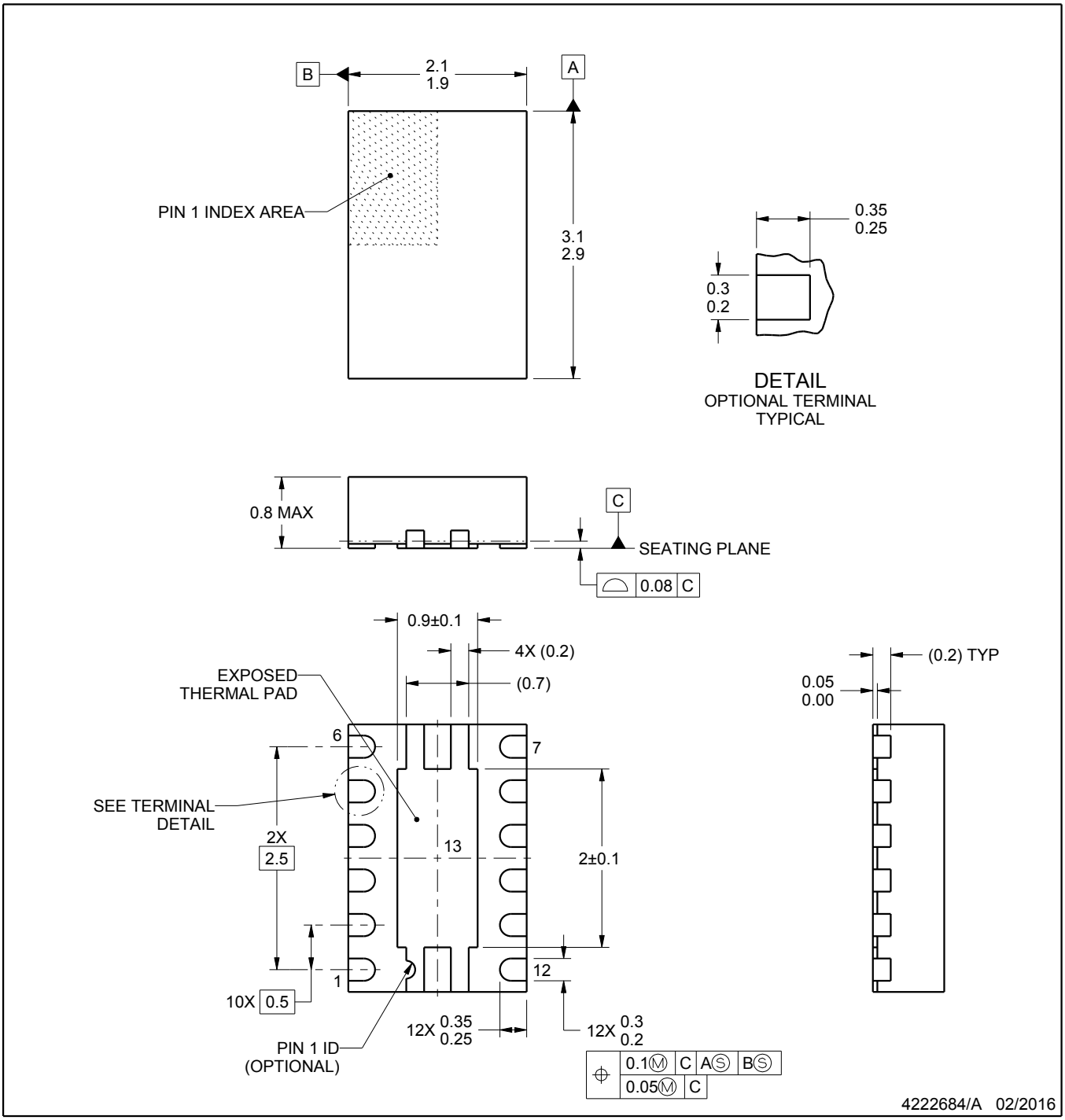
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DSS0012A

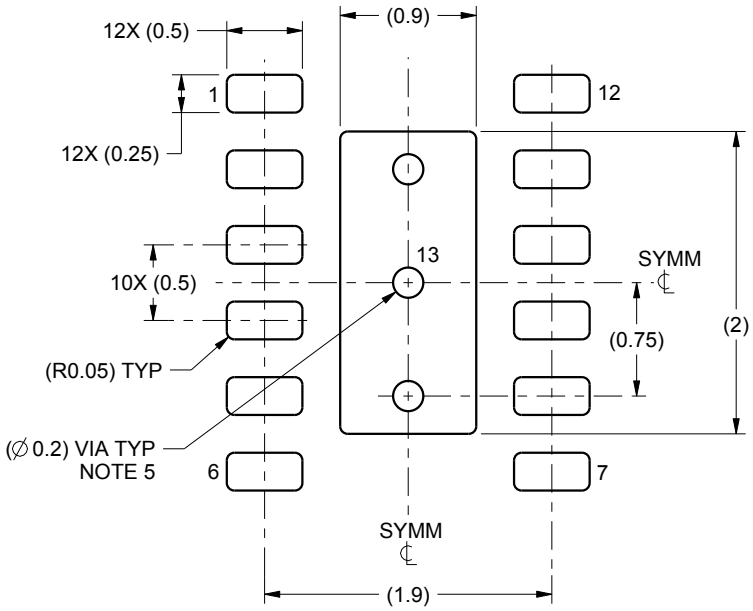
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

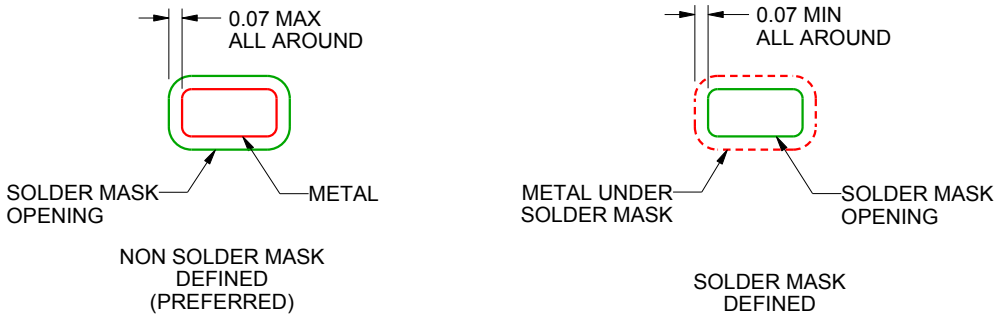


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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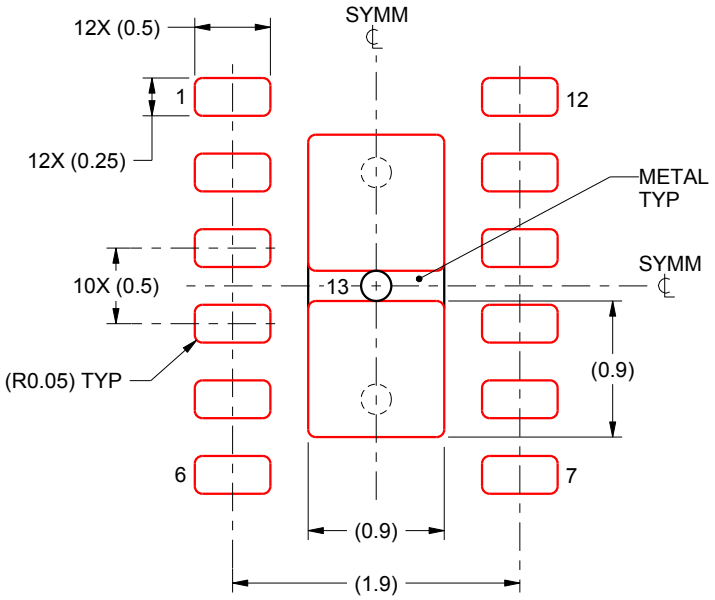
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown. It is recommended that vias located under solder paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 13:
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025