# DRV8847 Dual H-Bridge Motor Driver

## 1 Features

- Dual H-bridge motor driver
  - Single or dual-brushed DC motors
  - One bipolar stepper motor
  - Solenoid loads
- 2.7-V to 18-V operating voltage range
- High output current per H-bridge
  - 1-A RMS driver current at $T_A$ = 25°C
  - 2-A RMS driver current in parallel mode at $T_A$ = 25°C
- Low on-state resistance at VM > 5-V
  - 1000 mΩ $R_{DS(ON)}$ (HS + LS) at $T_A$ = 25°C
- Multiple control interface options
  - 4-Pin interface
  - 2-Pin interface
  - Parallel bridge interface
  - Independent bridge interface
- Current regulation with 20-µs fixed off-time
- Torque scalar for scaling output current to 50%
- Supports 1.8-V, 3.3-V, 5-V logic inputs
- Low-power sleep mode
  - 1.7-µA Sleep mode supply current at $V_{VM}$ = 12-V, $T_A$ = 25°C
- $I^2C$ Device Variant Available (DRV8847S)
  - Detailed diagnostics on $I^2C$ registers
  - Multi-slave operation support
  - Supports standard and fast $I^2C$ mode
- Small packages and footprints
  - 16 Pin TSSOP (no thermal pad)
  - 16 Pin HTSSOP PowerPAD™ package
  - 16 Pin WQFN thermal package
- Built-in protection features
  - VM undervoltage lockout
  - Overcurrent protection
  - Open load detection
  - Thermal shutdown
  - Fault condition indication pin (nFAULT)

## 2 Applications

- Refrigerator damper and ice maker
- Washers, dryers and dishwashers
- Electronic point-of-sale (ePOS) printers
- Stage lighting equipment
- Miniature circuit breakers and smart meters

## 3 Description

The DRV8847 device is a dual H-bridge motor driver for industrial applications, home appliances, ePOS printers, and other mechatronic applications. This device can be used for driving two DC motors, a bipolar stepper motor, or other loads such as relays. A simple PWM interface allows an easy interface with the controller. The DRV8847 device operates off a single power supply and supports a wide input supply range from 2.7 to 18 V.

The output stage of the driver consists of N-channel power MOSFETs configured as two full H-bridges to drive motor windings or four independent half bridges (in an independent bridge interface). A fixed off time controls the peak current in the bridge which can drive a 1-A load (2-A in parallel mode with proper heat sinking, at 25°C $T_A$).

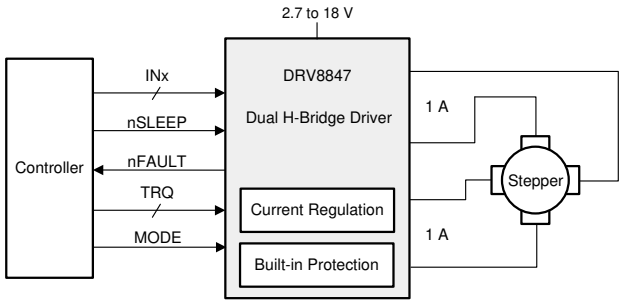
A low-power sleep mode is provided to achieve a low quiescent current draw by shutting down much of the internal circuitry. Additionally, a torque scalar is provided which dynamically scales the output current through a digital input pin. This feature lets the controller decrease the current required for lower power consumption.

Internal protection functions are provided for undervoltage-lockout, overcurrent protection on each FET, short circuit protection, open-load detection, and overtemperature. Fault conditions are indicated by the nFAULT pin. The $I^2C$ device variant (DRV8847S) has detailed diagnostics.

**Device Information**(1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| DRV8847 | HTSSOP (16) | 5.00 mm × 4.40 mm |
| | TSSOP (16) | 5.00 mm × 4.40 mm |
| | WQFN (16) | 3.00 mm × 3.00 mm |
| DRV8847S | TSSOP (16) | 5.00 mm × 4.40 mm |
| DRV88471 | WQFN (16) | 3.00 mm × 3.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.




**Simplified Schematic**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

# Table of Contents

**1 Features**....1
**2 Applications**....1
**3 Description**....1
**4 Revision History**....3
**5 Pin Configuration and Functions**....4
**6 Specifications**....7
6.1 Absolute Maximum Ratings....7
6.2 ESD Ratings....7
6.3 Recommended Operating Conditions....7
6.4 Thermal Information....7
6.5 Electrical Characteristics....8
6.6 I2C Timing Requirements....10
6.7 Typical Characteristics....12
**7 Detailed Description**....14
7.1 Overview....14
7.2 Functional Block Diagram....15
7.3 Feature Description....17
7.4 Device Functional Modes....42
7.5 Programming....44
7.6 Register Map....46
**8 Application and Implementation**....51
8.1 Application Information....51
8.2 Typical Application....51
**9 Layout**....70
9.1 Layout Guidelines....70
9.2 Layout Example....70
9.3 Thermal Considerations....72
9.4 Power Dissipation....72
**10 Device and Documentation Support**....73
10.1 Device Support (Optional)....73
10.2 Documentation Support....73
10.3 Receiving Notification of Documentation Updates....73
10.4 Community Resources....73
10.5 Trademarks....73
**11 Mechanical, Packaging, and Orderable Information**....73


Copyright © 2023 Texas Instruments Incorporated

# 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision B (April 2019) to Revision C (December 2023)** **Page**

- Added DRV88471 variant pinout and pin functions table....4
- Added DRV88471 bridge control MODE behavior description....21
- Added DRV88471 torque scaler TRQ behavior description....29

**Changes from Revision A (July 2018) to Revision B (April 2019)** **Page**

- Changed the Low On-State Resistance to be the indicated value when VM > 5 V....1
- Changed nFAULT pin type to OD/I....4
- Changed VM description to indicate 0.1-uF capacitor should be ceramic....4
- Changed digital pin voltage (IN1, IN2, IN3, IN4, TRQ, nSLEEP, nFAULT, SCL, SDA) maximum voltage from 5.5 V to 5.75 V....7
- Changed the Phase node pin voltage specification's name to Continuous phase node pin voltage....7
- Added for ISEN12, ISEN34 specification a footnote stating transients of +- 1V for less than 25 ns are acceptable....7
- Added for both Peak drive current (OUT1, OUT2, OUT3, OUT4) specifications a footnote stating Power dissipation and thermal limits must be observed....7
- Changed V(ESD) specification's value to 4000 V....7
- Changed the $V_{IL}$ specification to be two specifications based on test conditions VM < 7 V and VM >= 7 V....8
- Changed the $I_{IH}$ specification's minimum value to 18 uA for test condition IN1, IN2, IN3, IN4, TRQ, VIN = 5 V and to 10 uA for test condition nSLEEP, $V_{IN}$ = minimum (VM, 5 V)....8
- Added to $I_{OCP}$ specification a minimum value....8
- Changed pin naming of Block Diagram for DRV8847S figure....15
- Deleted ceramic from $C_{VM1}$....17
- Changed the relay or solenoid coils load bullet item for more clarity....25
- Added sentence to clarify nFAULT pin behavior when open load is detected....38
- Added sentence to clarify nFAULT pin behavior during power-up....42
- Added an Open Load Implementation section....60
- Added a Layout Recommendation of 16-Pin QFN Package for Double Layer Board figure....70

**Changes from Revision * (July 2018) to Revision A (August 2018)** **Page**

- Changed the data sheet status from *Advance Information* to *Production Data*....1
- Changed pin naming on Layout Recommendation of 16-Pin HTSSOP Package for Double Layer Board figure....70

Copyright © 2023 Texas Instruments Incorporated

## 5 Pin Configuration and Functions

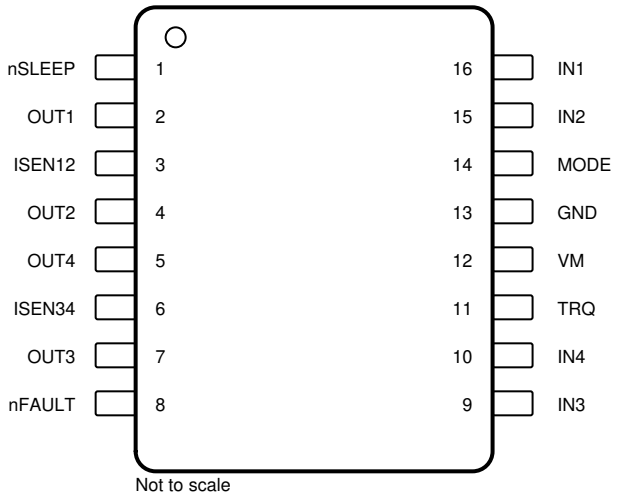



**Figure 5-1. DRV8847 PW Package 16-Pin TSSOP Top View**

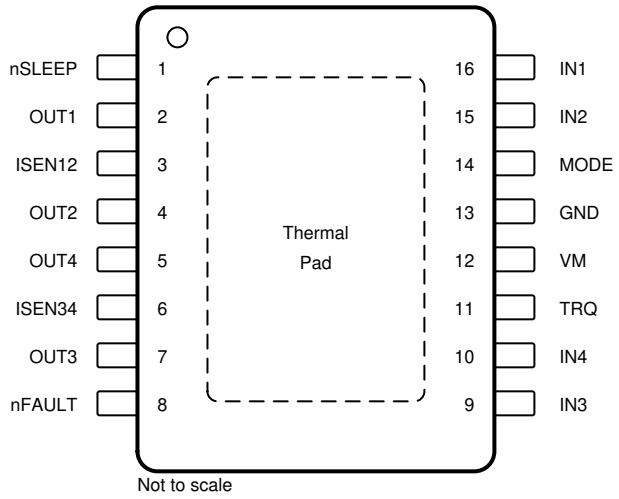



**Figure 5-2. DRV8847 PWP PowerPAD™ Package 16-Pin HTSSOP Top View**

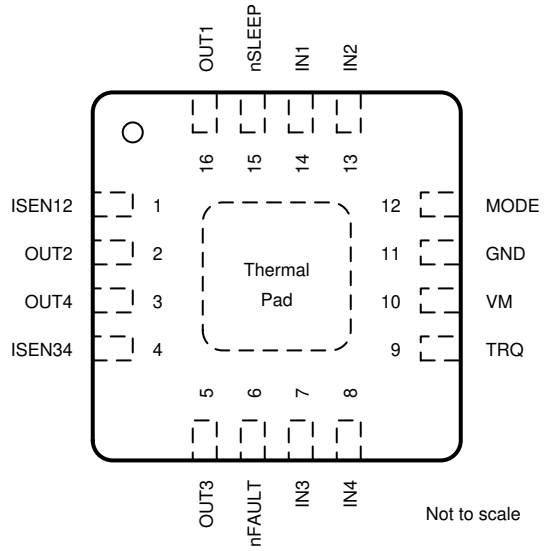



**Figure 5-3. DRV8847 RTE Package 16-Pin WQFN With Exposed Thermal Pad Top View**

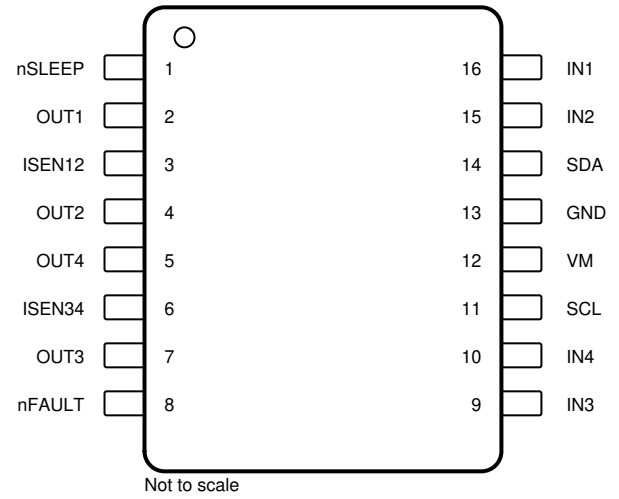



**Figure 5-4. DRV8847S PW Package 16-Pin TSSOP Top View**


Copyright © 2023 Texas Instruments Incorporated

**Table 5-1. Pin Functions**

| PIN | | | | TYPE[1] | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | DRV8847 | | DRV8847S | | |
| | TSSOP HTSSOP | WQFN | TSSOP | | |
| GND | 13 | 11 | 13 | PWR | Device ground. Recommended to connect the GND pin and device thermal pad (HTSSOP and WQFN packages) to ground |
| IN1 | 16 | 14 | 16 | I | Half-bridge input 1 |
| IN2 | 15 | 13 | 15 | I | Half-bridge input 2 |
| IN3 | 9 | 7 | 9 | I | Half-bridge input 3 |
| IN4 | 10 | 8 | 10 | I | Half-bridge input 4 |
| ISEN12 | 3 | 1 | 3 | O | Full-bridge-12 sense. Connect this pin to the current sense resistor for full-bridge-12. Connect this pin to the GND pin if current regulation is not required. |
| ISEN34 | 6 | 4 | 6 | O | Full-bridge-34 sense. Connect this pin to the to current sense resistor for full-bridge-34. Connect this pin to the GND pin if current regulation is not required. |
| MODE | 14 | 12 | — | I | Tri-state pin for selection of driver operating mode |
| nFAULT | 8 | 6 | 8 | OD / I | Fault indication pin. This pin is pulled logic low with a fault condition. This open-drain output requires an external pullup resistor. This pin is also used as an input pin for the DRV8847S device for releasing the $I^2C$ bus. |
| nSLEEP | 1 | 15 | 1 | I | Sleep mode input. Set this pin to logic high to enable the device. Set this pin to logic low to go to low-power sleep mode |
| OUT1 | 2 | 16 | 2 | O | Half-bridge output 1 |
| OUT2 | 4 | 2 | 4 | O | Half-bridge output 2 |
| OUT3 | 7 | 5 | 7 | O | Half-bridge output 3 |
| OUT4 | 5 | 3 | 5 | O | Half-bridge output 4 |
| SCL | — | — | 11 | I | $I^2C$ clock signal. |
| SDA | — | — | 14 | OD | $I^2C$ data signal. The SDA pin requires a pullup resistor. |
| TRQ | 11 | 9 | — | I | Torque current scalar |
| VM | 12 | 10 | 12 | PWR | Power supply. Connect the VM pin to the motor power supply. Bypass this pin to ground with a VM-rated 0.1-µF (ceramic) and 10-µF (minimum) capacitor. |

(1) I = input, O = output, OD = open-drain output, PWR = power

Copyright © 2023 Texas Instruments Incorporated

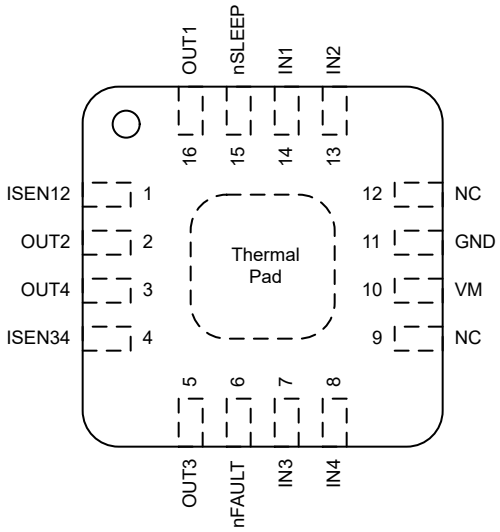



**Figure 5-5. DRV88471 RTE Package 16-Pin WQFN With Exposed Thermal Pad Top View**

**Table 5-2. New Pin Functions**

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| DRV8471 WQFN | NO. | | |
| GND | 11 | PWR | Device ground. Recommended to connect the GND pin and device thermal pad to ground |
| IN1 | 14 | I | Half-bridge input 1 |
| IN2 | 13 | I | Half-bridge input 2 |
| IN3 | 7 | I | Half-bridge input 3 |
| IN4 | 8 | I | Half-bridge input 4 |
| ISEN12 | 1 | O | Full-bridge-12 sense. Connect this pin to the current sense resistor for full-bridge-12. Connect this pin to the GND pin if current regulation is not required. |
| ISEN34 | 4 | O | Full-bridge-34 sense. Connect this pin to the to current sense resistor for full-bridge-34. Connect this pin to the GND pin if current regulation is not required. |
| NC | 9 | - | No connect |
| NC | 12 | - | No connect |
| nFAULT | 6 | OD | Fault indication pin. This pin is pulled logic low with a fault condition. This open-drain output requires an external pullup resistor. |
| nSLEEP | 15 | I | Sleep mode input. Set this pin to logic high to enable the device. Set this pin to logic low to go to low-power sleep mode. |
| OUT1 | 16 | O | Half-bridge output 1 |
| OUT2 | 2 | O | Half-bridge output 2 |
| OUT3 | 5 | O | Half-bridge output 3 |
| OUT4 | 3 | O | Half-bridge output 4 |
| VM | 10 | PWR | Power supply. Connect the VM pin to the motor power supply. Bypass this pin to ground with a VM-rated 0.1-µF (ceramic) and 10-µF (minimum) capacitor. |

(1) I = input, O = output, OD = open-drain output, PWR = power


Copyright © 2023 Texas Instruments Incorporated

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

| | MIN | MAX | UNIT |
|---|---|---|---|
| Power supply pin voltage (VM) | -0.3 | 20 | V |
| Power supply voltage ramp rate (VM) | 0 | 2 | V/µs |
| Digital pin voltage (IN1, IN2, IN3, IN4, TRQ, nSLEEP, nFAULT, SCL, SDA) | -0.3 | 5.75 | V |
| Continuous phase node pin voltage (OUT1, OUT2, OUT3, OUT4) | -0.7 | VM + 0.6 | V |
| Shunt amplifier input pin voltage (ISEN12, ISEN34)(2) | -0.6 | 0.6 | V |
| Peak drive current (OUT1, OUT2, OUT3, OUT4), $V_{VM}$ <= 16.5 V(3) | Internally Limited | | A |
| Peak drive current (OUT1, OUT2, OUT3, OUT4), $V_{VM}$ > 16.5 V(3) | 0 | 4 | A |
| Ambient temperature, $T_A$ | -40 | 125 | °C |
| Junction temperature, $T_J$ | -40 | 150 | °C |
| Storage temperature, $T_{stg}$ | -65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Transients of ±1 V for less than 25 ns are acceptable.
(3) Power dissipation and thermal limits must be observed.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±4000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

Over operating ambient temperature range (unless otherwise noted). Typical limits apply for TA = 25°C and $V_{VM}$ = 12 V.

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{VM}$ | Power supply voltage (VM) | 2.7 | | 18 | V |
| $V_{IN}$ | Logic input voltage (IN1, IN2, IN3, IN4, TRQ, nSLEEP, SCL, SDA) | 0 | | 5 | V |
| $I_{RMS}$ | Motor RMS current per bridge (OUT1, OUT2, OUT3, OUT4) | 0 | | 1(1) | A |
| $f_{PWM}$ | PWM frequency (IN1, IN2, IN3, IN4) | 0 | | 250(1) | kHz |
| $V_{OD}$ | Open drain pullup voltage (nFAULT) | 0 | | 5 | V |
| $I_{OD}$ | Open drain output current (nFAULT) | 0 | | 5 | mA |
| $T_A$ | Operating Ambient Temperature | -40 | | 85 | °C |
| $T_J$ | Operating Junction Temperature | -40 | | 150 | °C |

(1) Power dissipation and thermal limits must be observed. Dependent on the package thermal performance.

## 6.4 Thermal Information

| THERMAL METRIC(1) | | DRV8847, DRV8847S | DRV8847 | DRV8847 | UNIT |
|---|---|---|---|---|---|
| | | PW (TSSOP) | PWP (HTSSOP) | RTE (QFN) | |
| | | 16 PINS | 16 PINS | 16 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 107.9 | 46.5 | 46.4 | °C/W |

Copyright © 2023 Texas Instruments Incorporated

| THERMAL METRIC(1) | | DRV8847, DRV8847S | DRV8847 | DRV8847 | UNIT |
|---|---|---|---|---|---|
| | | PW (TSSOP) | PWP (HTSSOP) | RTE (QFN) | |
| | | 16 PINS | 16 PINS | 16 PINS | |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 38.5 | 40.1 | 47.5 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 54.2 | 18.8 | 21.2 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 3.1 | 1.3 | 0.9 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 53.6 | 19.0 | 21.3 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | 5.9 | 6.1 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6.5 Electrical Characteristics

Over recommended operating conditions unless otherwise noted. Typical limits apply for $T_A$ = 25°C and $V_{VM}$ = 12 V.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLIES (VM)** | | | | | | |
| $I_{VM}$ | VM operating supply current | VM = 2.7 V; nSLEEP = 1; INX = 0 | | 2 | 2.5 | mA |
| | | VM = 5 V; nSLEEP = 1; INX = 0 | | 3 | 3.5 | mA |
| | | VM = 12 V; nSLEEP = 1; INX = 0 | | 3 | 3.5 | mA |
| $I_{VMQ}$ | VM sleep mode current | VM = 2.7 V; nSLEEP = 0; TA = 25°C | | 0.1 | | µA |
| | | VM = 2.7 V; nSLEEP = 0; TA = 85°C | | | 0.5 | µA |
| | | VM = 5 V; nSLEEP = 0; TA = 25°C | | 0.2 | | µA |
| | | VM = 5 V; nSLEEP = 0; TA = 85°C | | | 1 | µA |
| | | VM = 12 V; nSLEEP = 0; TA = 25°C | | 1.7 | | µA |
| | | VM = 12 V; nSLEEP = 0; TA = 85°C | | | 2.5 | µA |
| $t_{SLEEP}$ | Sleep time | nSLEEP = 0 to sleep mode | | 2 | | µs |
| $t_{WAKE}$ | Wake-up time | nSLEEP = 1 to output transition | | | 1.5 | ms |
| $t_{ON}$ | Turnon-time | VM > UVLO to output transition (nSLEEP = 1) | | | 1.5 | ms |
| **LOGIC-LEVEL INPUTS (IN1, IN2, IN3, IN4, NSLEEP, TRQ, SCL, SDA)** | | | | | | |
| $V_{IL}$ | Input logic low voltage | VM < 7 V | 0 | | 0.6 | V |
| | | VM >= 7 V (1) | 0 | | 1.0 | V |
| $V_{IH}$ | Input logic high voltage | | 1.6 | | 5.5 | V |
| $V_{HYS}$ | Input logic hysteresis | nSLEEP pin | 40 | | | mV |
| $V_{HYS}$ | Input logic hysteresis | IN1, IN2, IN3, IN4, TRQ, SCL pins | 100 | | | mV |
| VIL | nSLEEP | | 0 | | 0.6 | V |
| VIH | nSLEEP | | 1.6 | | 5.5 | V |
| VHYS | nSLEEP | | 40 | | | mV |
| $I_{IL}$ | Input logic low current | $V_{IN}$ = 0 V | -1 | | 1 | µA |
| $I_{IH}$ | Input logic high current | IN1, IN2, IN3, IN4, TRQ, $V_{IN}$ = 5 V | 18 | | 35 | µA |
| | | nSLEEP, $V_{IN}$ = minimum (VM, 5 V) | 10 | | 25 | µA |
| $t_{PD}$ | Propagation Delay | INx edge to output | 100 | 400 | 600 | ns |
| $t_{DEGLITCH}$ | Input logic deglitch | | | 50 | | ns |
| **TRI-LEVEL INPUTS (MODE)** | | | | | | |
| $V_{IL}$ | Tri-level input logic low voltage | | 0 | | 0.6 | V |
| $V_{IZ}$ | Tri-level input hi-Z voltage | | | 1.2 | | V |
| $V_{IH}$ | Tri-level input logic high voltage | | 1.6 | | 5.5 | V |
| $I_{IL}$ | Tri-level input logic low current | $V_{IN}$ = 0 V | -9 | | -4 | µA |


Copyright © 2023 Texas Instruments Incorporated

Over recommended operating conditions unless otherwise noted. Typical limits apply for $T_A$ = 25°C and $V_{VM}$ = 12 V.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{IH}$ | Tri-level input logic high current | $V_{IN}$ = 5 V | 8 | | 25 | µA |
| **OPEN-DRAIN OUTPUTS (nFAULT)** | | | | | | |
| $V_{OL}$ | Output logic low voltage | $I_{OD}$ = 5 mA | | | 0.5 | V |
| $I_{OH}$ | Output logic high current | $V_{OD}$ = 3.3 V | -1 | | 1 | µA |
| **OPEN-DRAIN OUTPUTS (SDA)** | | | | | | |
| $V_{OL}$ | Output logic low voltage | $I_{OD}$ = 5 mA | | | 0.5 | V |
| $I_{OH}$ | Output logic high current | $V_{OD}$ = 3.3 V | -1 | | 1 | µA |
| $C_B$ | Capacitive load for each bus line | | | | 400 | pF |
| **DRIVER OUTPUTS (OUT1, OUT2, OUT3, OUT4)** | | | | | | |
| $R_{DS(ON)_HS}$ | High-side MOSFET on resistance | $V_{VM}$ = 2.7 V; $I_{OUT}$ = 0.5 A; $T_A$ = 25°C | | 690 | | mΩ |
| | | $V_{VM}$ = 2.7 V; $I_{OUT}$ = 0.5 A; $T_A$ = 85°C | | | 950 | mΩ |
| | | $V_{VM}$ = 5 V; $I_{OUT}$ = 0.5 A; $T_A$ = 25°C | | 530 | | mΩ |
| | | $V_{VM}$ = 5 V; $I_{OUT}$ = 0.5 A; $T_A$ = 85°C | | | 740 | mΩ |
| | | $V_{VM}$ = 12 V; $I_{OUT}$ = 0.5 A; $T_A$ = 25°C | | 520 | | mΩ |
| | | $V_{VM}$ = 12 V; $I_{OUT}$ = 0.5 A; $T_A$ = 85°C | | | 700 | mΩ |
| $R_{DS(ON)_LS}$ | Low-side MOSFET on resistance | $V_{VM}$ = 2.7 V; $I_{OUT}$ = 0.5 A; $T_A$ = 25°C | | 570 | | mΩ |
| | | $V_{VM}$ = 2.7 V; $I_{OUT}$ = 0.5 A; $T_A$ = 85°C | | | 900 | mΩ |
| | | $V_{VM}$ = 5 V; $I_{OUT}$ = 0.5 A; $T_A$ = 25°C | | 460 | | mΩ |
| | | $V_{VM}$ = 5 V; $I_{OUT}$ = 0.5 A; $T_A$ = 85°C | | | 690 | mΩ |
| | | $V_{VM}$ = 12 V; $I_{OUT}$ = 0.5 A; $T_A$ = 25°C | | 450 | | mΩ |
| | | $V_{VM}$ = 12 V; $I_{OUT}$ = 0.5 A; $T_A$ = 85°C | | | 680 | mΩ |
| $I_{OFF}$ | Off-state leakage current | $V_{VM}$ = 5 V; $T_J$ = 25 °C; $V_{OUT}$ = 0 V | -1 | | 1 | µA |
| $t_{RISE}$ | Output rise time | $V_{VM}$ = 12 V; $I_{OUT}$ = 0.5 A | | 150 | | ns |
| $t_{FALL}$ | Output fall time | $V_{VM}$ = 12 V, $I_{OUT}$ = 0.5 A | | 150 | | ns |
| $t_{DEAD}$ | Output dead time | Internal dead time | | 200 | | ns |
| $V_{SD}$ | Body diode forward voltage | $I_{OUT}$ = 0.5 A | | 1.1 | | V |
| **PWM CURRENT CONTROL (ISEN12, SEN34)** | | | | | | |
| $V_{TRIP}$ | ISENxx trip voltage | Torque at 100% (TRQ = 0) | 140 | 150 | 160 | mV |
| | | Torque at 50% (TRQ = 1) | 63.75 | 75 | 86.25 | mV |
| $t_{BLANK}$ | Current sense blanking time | | | 1.8 | | µs |
| $t_{OFF}$ | Current control constant off time | | | 20 | | µs |
| **PROTECTION CIRCUITS** | | | | | | |
| $V_{UVLO}$ | Supply undervoltage lockout | Supply rising | | | 2.7 | V |
| | | Supply falling | 2.4 | | | V |
| $V_{UVLO_HYS}$ | Supply undervoltage hysteresis | Rising to falling theshold | | 50 | | mV |
| $t_{UVLO}$ | Supply undervoltage deglitch time | VM falling; UVLO report | | 10 | | µs |
| $I_{OCP}$ | Overcurrent protection trip point (2) | | 1.6 | 2 | | A |
| $t_{OCP}$ | Overcurrent protection deglitch time | $V_{VM}$ < 15 V | | 3 | | µs |
| | | $V_{VM}$ >= 15 V | | 1 | | µs |
| $t_{RETRY}$ | Overcurrent protection retry time | | | 1 | | ms |
| $I_{OL_PU}$ | Open load pull up current | < 15 nF on OUTx Pin, $V_{VM}$ = 2.7 V | | 100 | | µA |
| $I_{OL_PU}$ | Open load pull-up current | < 15 nF on OUTx Pin | | 200 | | µA |
| $I_{OL_PD}$ | Open load pull down current | < 15 nF on OUTx Pin, $V_{VM}$ = 2.7 V | | 130 | | µA |
| $I_{OL_PD}$ | Open load pull-down current | < 15 nF on OUTx Pin | | 230 | | µA |
| $I_{OL}$ | Open load pull up and pull down current | | | 230 | | µA |

Copyright © 2023 Texas Instruments Incorporated

Over recommended operating conditions unless otherwise noted. Typical limits apply for $T_A$ = 25°C and $V_{VM}$ = 12 V.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OL_HS}$ | Open load detect threshold (high side) | $V_{VM}$ = 2.7 V | | 1.3 | | V |
| $V_{OL_HS}$ | Open load detect threshold (high side) | | | 2.3 | | V |
| $V_{OL_LS}$ | Open load detect threshold (low side) | $V_{VM}$ = 2.7 V | | 0.67 | | V |
| $V_{OL_LS}$ | Open load detect threshold (low side) | | | 1.2 | | V |
| $V_{OL}$ | Open load detect threshold voltage | | | 1.1 | | V |
| $T_{TSD}$ | Thermal shutdown temperature | | 150 | 160 | 180 | °C |
| $T_{HYS}$ | Thermal shutdown hysteresis | | | 40 | | °C |
| $V_{b_BJT_27C}$ | Base voltage of BJT in OTS (Testpad out at 12V supply) | | | | | |

(1) Specified by design and characterization
(2) For $V_M$ > 16.5 V, the output current on OUTx must be limited to 4 A

## 6.6 I2C Timing Requirements

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| **STANDARD MODE** | | | | | |
| $f_{SCL}$ | SCL Clock frequency | 0 | | 100 | kHz |
| $t_{HD,STA}$ | Hold time (repeated) START condition. After this period, the first clock pulse is generated | 4 | | | µs |
| $t_{LOW}$ | LOW period of the SCL clock | 4.7 | | | µs |
| $t_{HIGH}$ | HIGH period of the SCL clock | 4 | | | µs |
| $t_{SU,STA}$ | Setup time for a repeated START condition | 4.7 | | | µs |
| $t_{HD,DAT}$ | Data hold time: For I2C bus devices | 0 | | 3.45 | µs |
| $t_{SU,DAT}$ | Data set-up time | 250 | | | ns |
| $t_R$ | SDA and SCL rise time | | | 1000 | ns |
| $t_F$ | SDA and SCL fall time | | | 300 | ns |
| $t_{SU,STO}$ | Set-up time for STOP condition | 4 | | | µs |
| $t_{BUF}$ | Bus free time between a STOP and START condition | 4.7 | | | µs |
| **FAST MODE** | | | | | |
| $f_{SCL}$ | SCL Clock frequency | 0 | | 400 | kHz |
| $t_{HD,STA}$ | Hold time (repeated) START condition. After this period, the first clock pulse is generated | 0.6 | | | µs |
| $t_{LOW}$ | LOW period of the SCL clock | 1.3 | | | µs |
| $t_{HIGH}$ | HIGH period of the SCL clock | 0.6 | | | µs |
| $t_{SU,STA}$ | Setup time for a repeated START condition | 0.6 | | | µs |
| $t_{HD,DAT}$ | Data hold time: For I2C bus devices | 0 | | 0.9 | µs |
| $t_{SU,DAT}$ | Data set-up time | 250 | | | ns |
| $t_R$ | SDA and SCL rise time | | | 300 | ns |
| $t_F$ | SDA and SCL fall time | | | 300 | ns |
| $t_{SU,STO}$ | Set-up time for STOP condition | 0.6 | | | µs |
| $t_{BUF}$ | Bus free time between a STOP and START condition | 1.3 | | | µs |
| $t_{SP}$ | Pulse width of spikes to be supressed by input noise filter | | 50 | | ns |


Copyright © 2023 Texas Instruments Incorporated

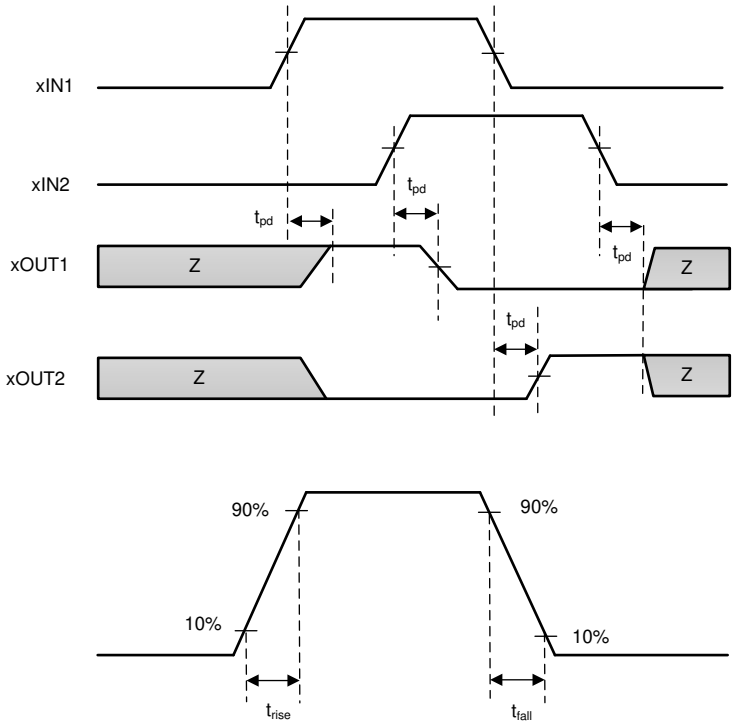



**Figure 6-1. Timing Diagram**

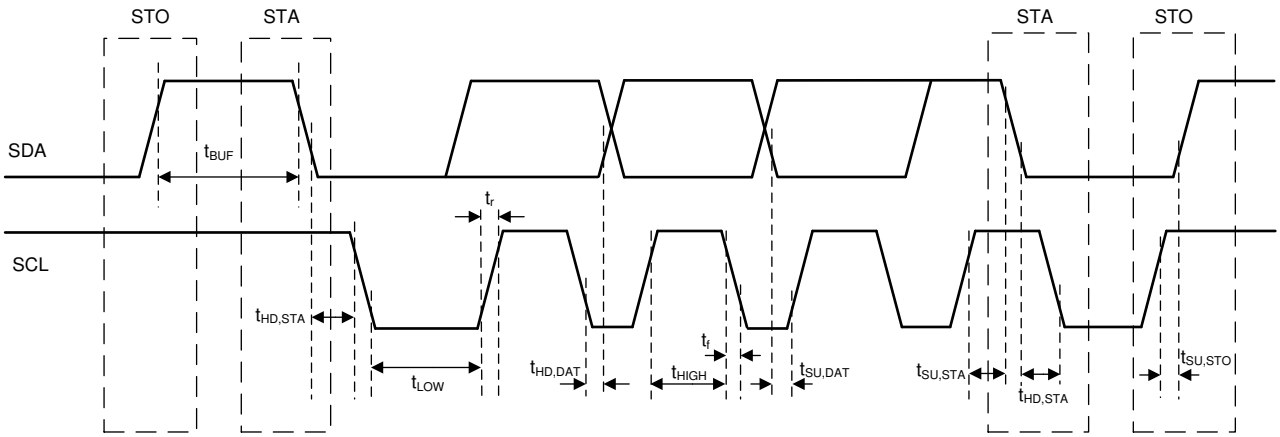



**Figure 6-2. I²C Timing Diagram**

## 6.7 Typical Characteristics

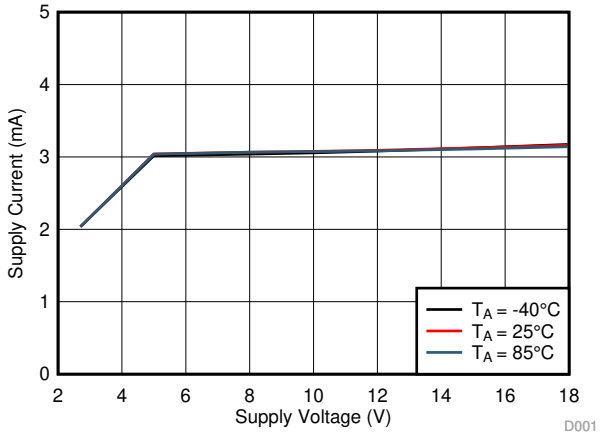



**Figure 6-3. Operating Supply Current ($I_{VM}$) vs Supply Voltage ($V_{VM}$)**

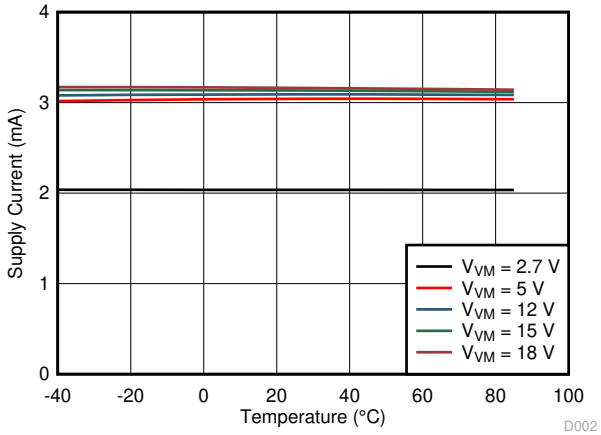



**Figure 6-4. Operating Supply Current ($I_{VM}$) vs Ambient Temperature ($T_A$)**

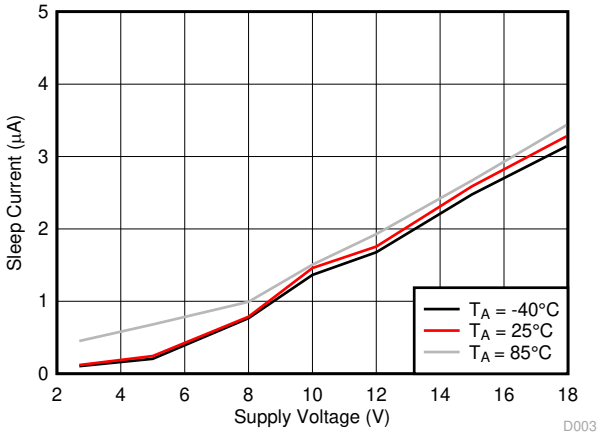



**Figure 6-5. Sleep Mode Supply Current ($I_{VMQ}$) vs Supply Voltage ($V_{VM}$)**

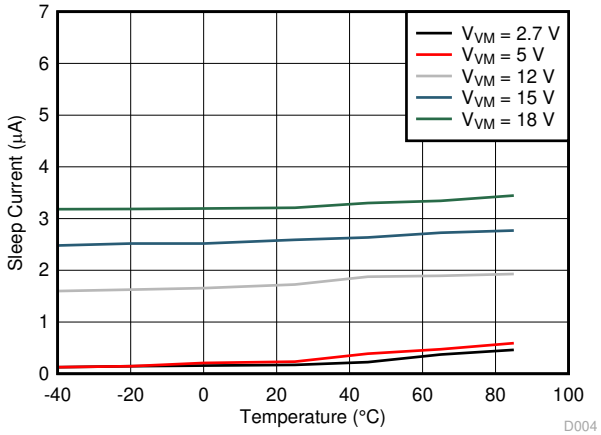



**Figure 6-6. Sleep Mode Supply Current ($I_{VMQ}$) vs Ambient Temperature ($T_A$)**

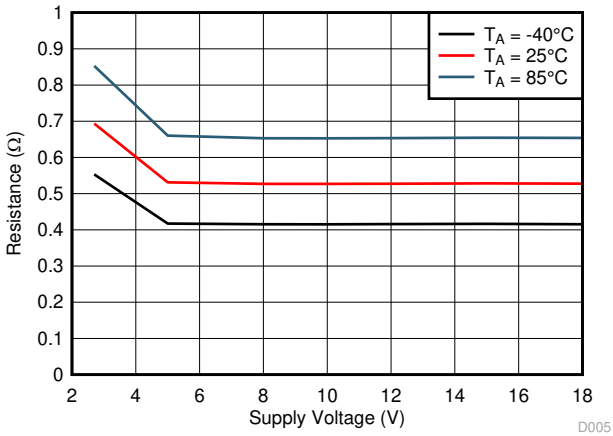



**Figure 6-7. High Side On-State Resistance ($R_{DS(ON)_HS}$) vs Supply Voltage ($V_{VM}$)**

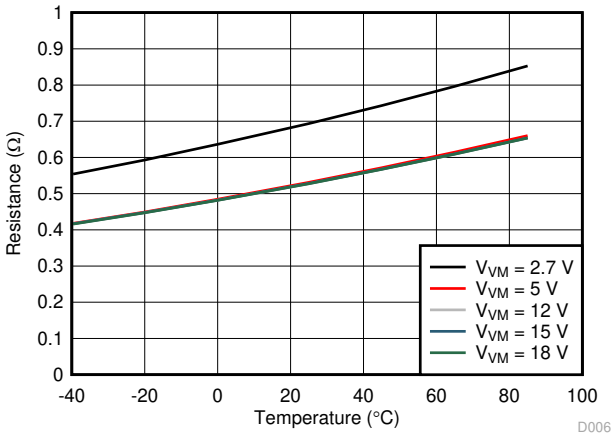



**Figure 6-8. High Side On-State Resistance ($R_{DS(ON)_HS}$) vs Ambient Temperature ($T_A$)**


Copyright © 2023 Texas Instruments Incorporated

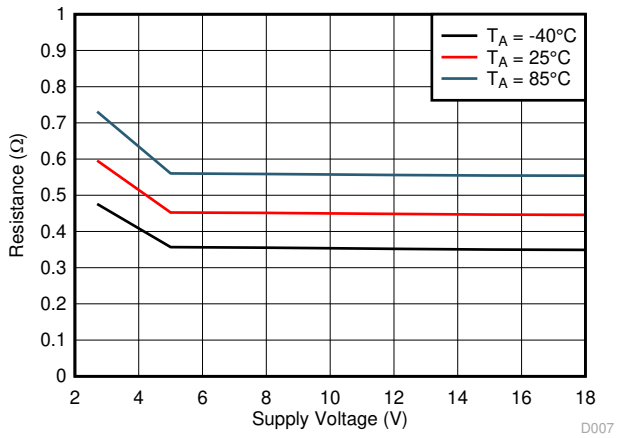



**Figure 6-9. Low Side On-State Resistance ($R_{DS(ON)_LS}$) vs Supply Voltage ($V_{VM}$)**

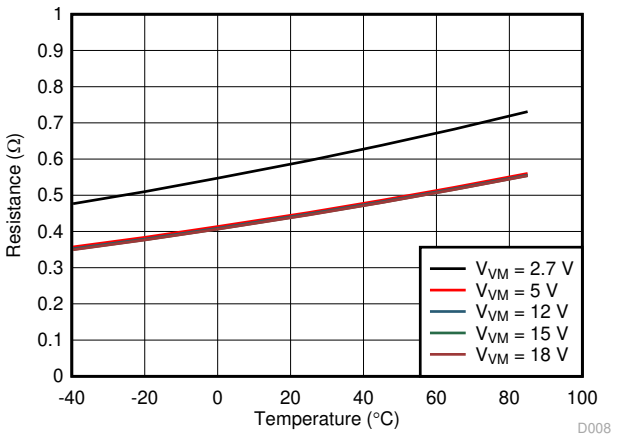



**Figure 6-10. Low Side On-State Resistance ($R_{DS(ON)_LS}$) vs Ambient Temperature ($T_A$)**

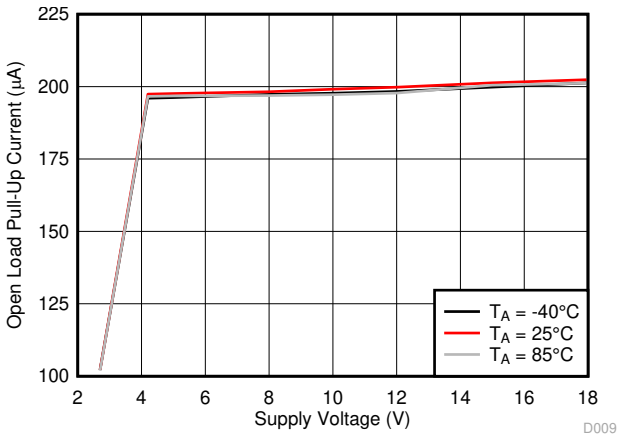



**Figure 6-11. Open Load Pull-Up Current ($I_{OL_PU}$) vs Supply Voltage ($V_{VM}$)**

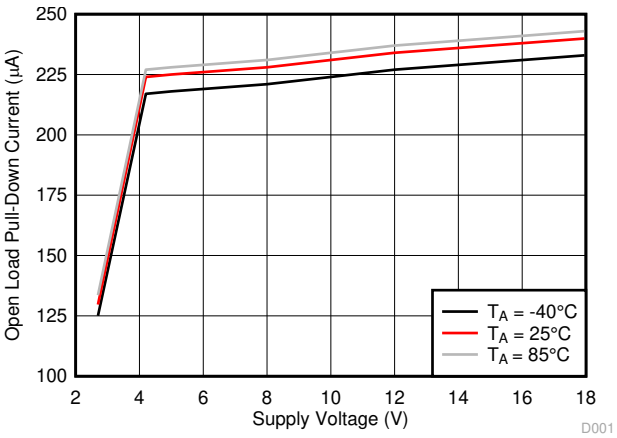



**Figure 6-12. Open Load Pull-Down Current ($I_{OL_PD}$) vs Supply Voltage ($V_{VM}$)**

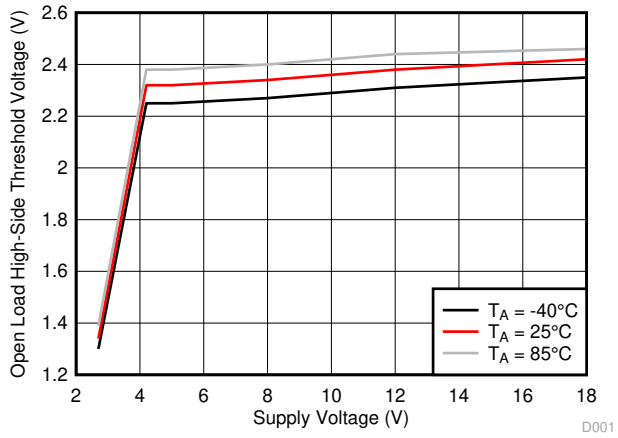



**Figure 6-13. Open Load High-Side Threshold Voltage ($V_{OL_HS}$) vs Supply Voltage ($V_{VM}$)**

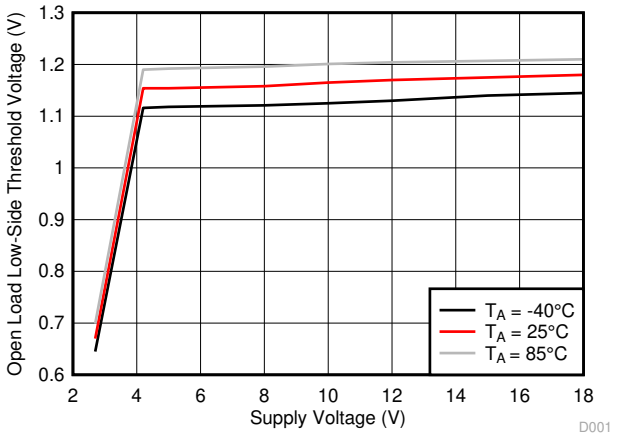



**Figure 6-14. Open Load Low-Side Threshold Voltage ($V_{OL_LS}$) vs Supply Voltage ($V_{VM}$)**

Copyright © 2023 Texas Instruments Incorporated

# 7 Detailed Description

## 7.1 Overview

The DRV8847 device is an integrated 2.7-V to 18-V dual motor driver for industrial brushed and stepper motor applications. This driver can drive two DC motors, a bipolar stepper motor, or the solenoid loads. The device integrates two H-bridges that use NMOS low-side and high-side drivers and current-sense regulation circuitry. The DRV8847 device supports a high output current of 1-A RMS per H-bridge using low-$R_{DS(ON)}$ integrated MOSFETs.

A simple PWM interface option allows easy interfacing with the H-bridge outputs. The interface options can be configured using the MODE and IN3 pins in the DRV8847 device. The interface options can be configured through an $I^2C$ interface in the $I^2C$ device variant (DRV8847S).

The current regulation uses a fixed off-time ($t_{OFF}$) PWM scheme. The trip point for current regulation is controlled by the value of the sense resistor and fixed internal $V_{TRIP}$ value.

A low-power sleep mode is included which lets the system save power when not driving the motor.

The DRV8847 device is available in three different packages:

- 16-pin TSSOP (no thermal pad)
- 16 pin HTSSOP (PowerPAD)
- 16 pin WQFN (thermal pad)

The $I^2C$ variant of the DRV8847 device is also available for a detailed diagnostics requirement and multi-slave operation with multi-slave operation control over the $I^2C$ bus.

The DRV8847S device variant is available in one package which is the 16-pin TSSOP (no thermal pad).

The DRV8847 device has a broad range of integrated protection features. These features include power supply undervoltage lockout, open-load detection, overcurrent faults, and thermal shutdown.


Copyright © 2023 Texas Instruments Incorporated

## 7.2 Functional Block Diagram

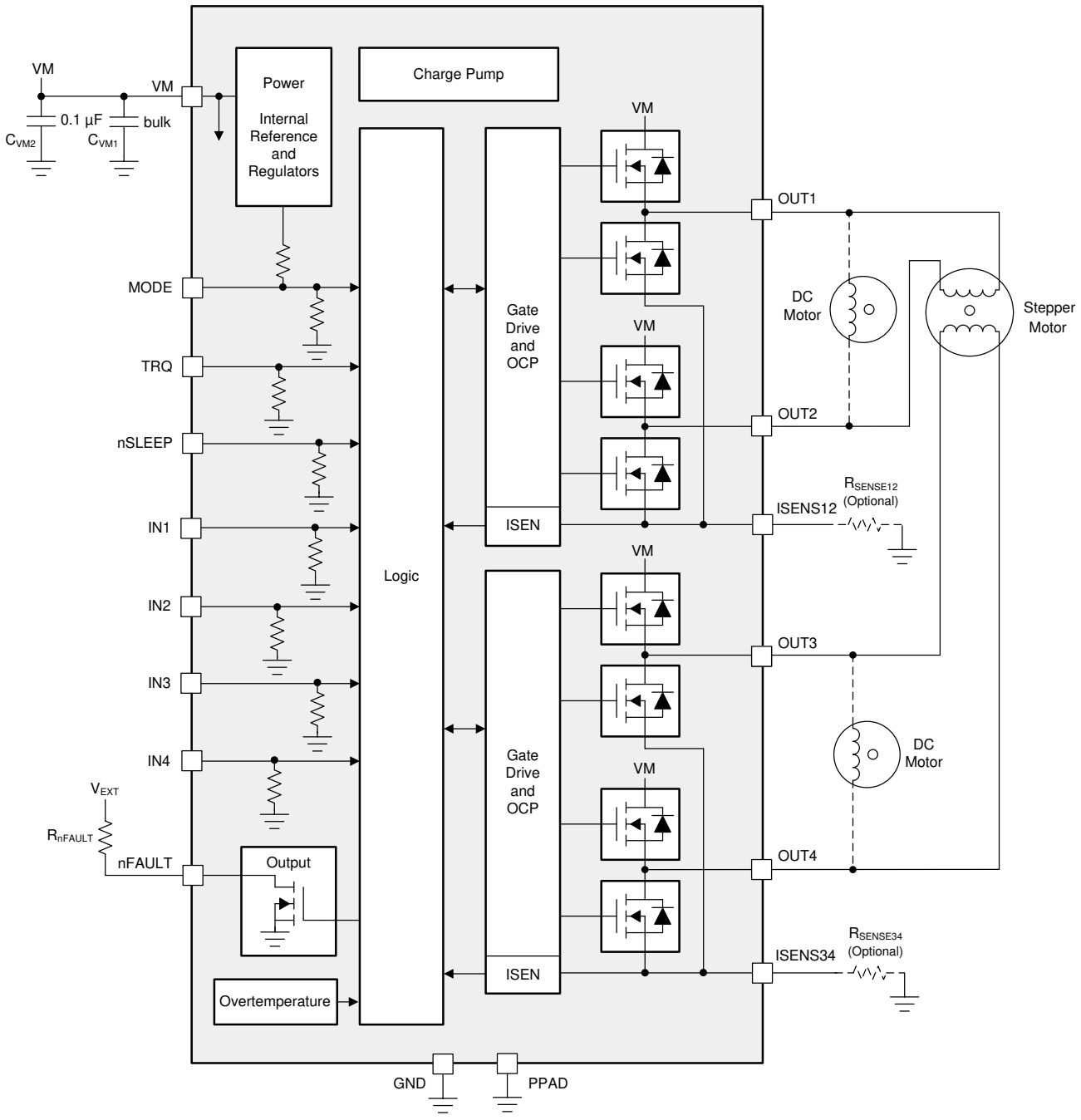



**Figure 7-1. Block Diagram for DRV8847**

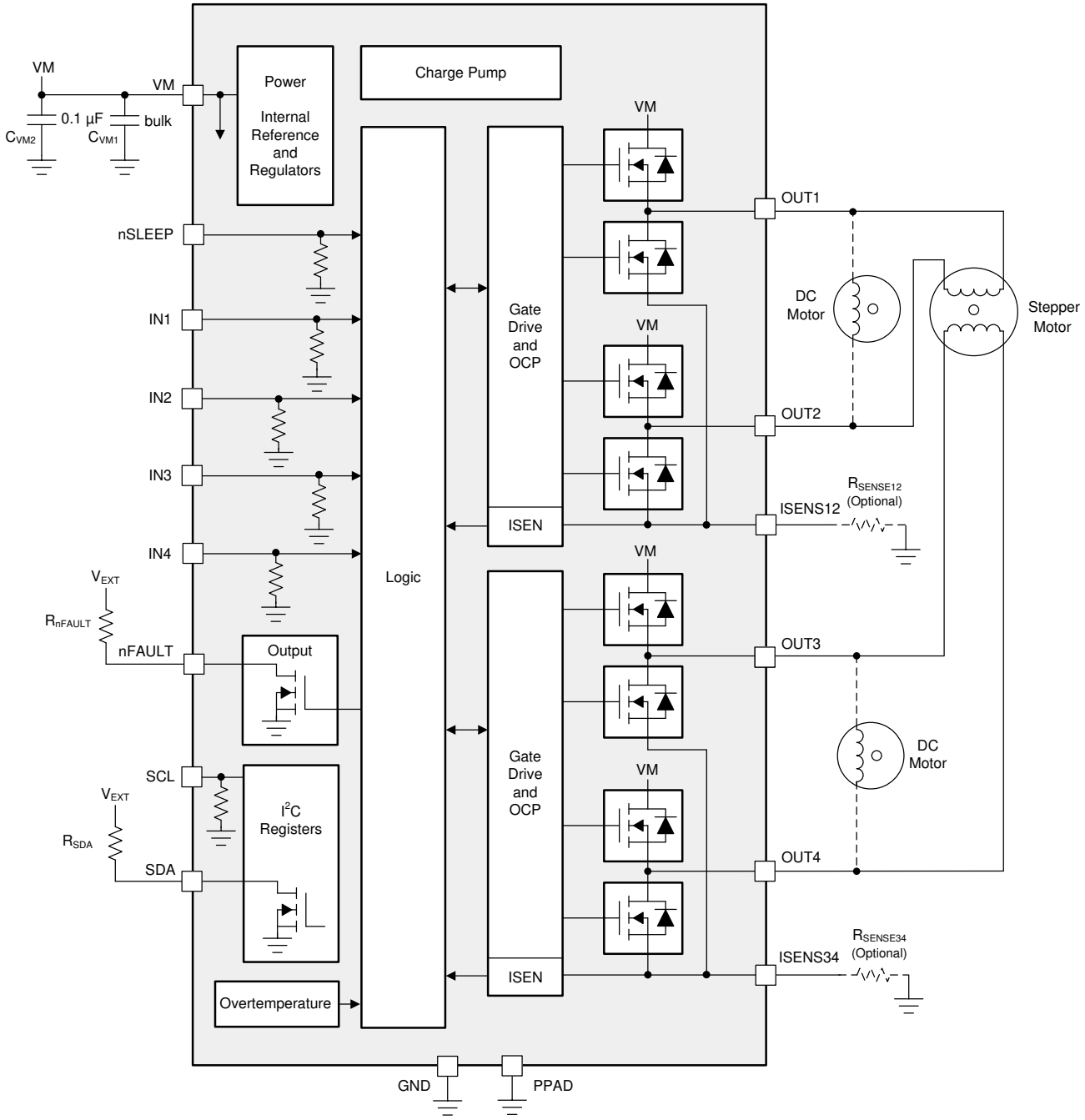



**Figure 7-2. Block Diagram for DRV8847S**


Copyright © 2023 Texas Instruments Incorporated

## 7.3 Feature Description

Table 7-1 lists the recommended values of the external components for the gate driver.

**Table 7-1. DRV8847 External Components**

| COMPONENT | PIN 1 | PIN 2 | RECOMMENDED |
|---|---|---|---|
| $C_{VM1}$ | VM | GND | 10-µF (minimum) VM-rated capacitor |
| $C_{VM2}$ | VM | GND | 0.1-µF VM-rated ceramic capacitor |
| $R_{nFAULT}$ | VEXT(1) | nFAULT | >1 kΩ |
| $R_{ISEN12}$ | ISEN12 | GND | Sense resistor, see the *Section 8.2* for sizing |
| $R_{ISEN34}$ | ISEN34 | GND | Sense resistor, see the *Section 8.2* for sizing |

(1) VEXT is not a pin on the DRV8847 device, but a pullup resistor on the VEXT external supply voltage is required for the open-drain output, nFAULT.

### 7.3.1 PWM Motor Drivers

The DRV8847 device has two identical H-bridge motor drivers with current-control PWM circuitry. Figure 7-3 shows a block diagram of the circuitry.

The two H-bridges can also be used as four independent half-bridges depending upon the interface option. The ISENxx pin can be only used together with two half-bridges.

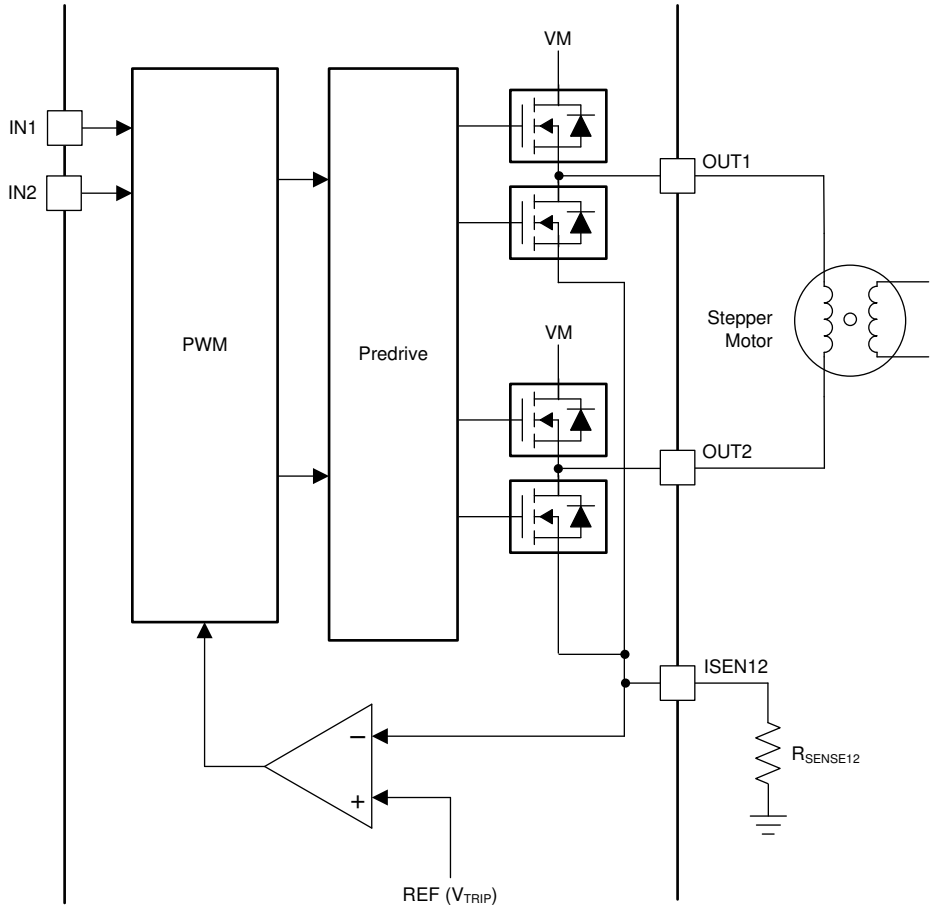



**Figure 7-3. PWM Motor Driver Circuitry**

### 7.3.2 Bridge Operation

The full-bridge can operate in four different operating modes: forward, reverse, coast (fast decay), and brake (slow decay) operation.

#### *7.3.2.1 Forward Operation*

This operating mode refers to the forward rotation of the motor such that the current flows from terminal A (OUT1 or OUT3) to terminal B (OUT2 or OUT4) as shown in Figure 7-4. In this mode, terminal A is connected to VM, and terminal B is connected to ground.

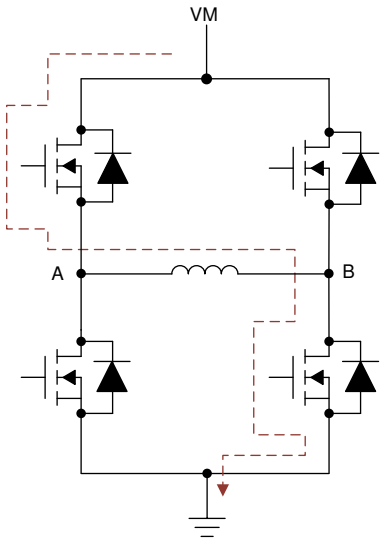



**Figure 7-4. Forward Operation**

#### *7.3.2.2 Reverse Operation*

This operating mode refers to the reverse rotation of the motor such that the current flows from terminal B (OUT2 or OUT4) to terminal A (OUT1 or OUT3) as shown in Figure 7-5. In this mode, terminal A is connected to ground, and terminal B is connected to VM.

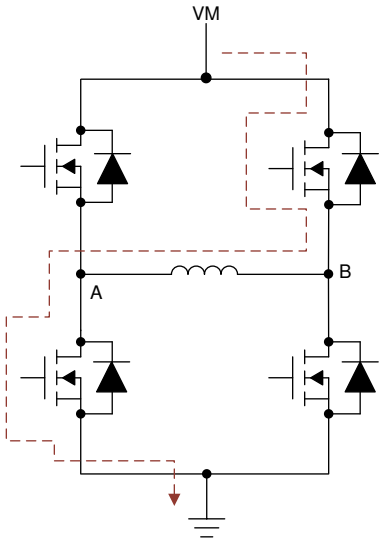



**Figure 7-5. Reverse Operation**


Copyright © 2023 Texas Instruments Incorporated

#### 7.3.2.3 Coast Operation (Fast Decay)

In this operating mode, all the FETs of the full-bridges are in the high impedance (Hi-Z) state. The motor also goes to the Hi-Z state, and the motor starts coasting. This operating mode also helps to decay the motor current faster and is therefore also referred to as a fast decay mode. If the motor was initially connected in forward operation (current flows from terminal A to terminal B) and if the coast operation is applied, then, because of the inductive nature of the motor load, the current continues to flow in the same direction (A to B), and the anti-parallel diodes of the alternate FETs start conducting as shown in Figure 7-6. This flow of current through anti-parallel diodes lets the current decrease rapidly because of the higher negative potential created by the supply voltage, VM.

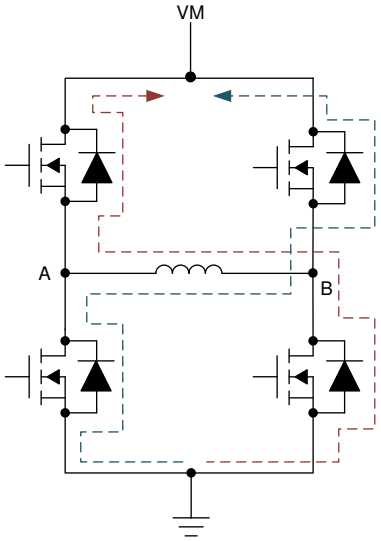



**Figure 7-6. Coast Operation (Fast Decay)**

#### 7.3.2.4 Brake Operation (Slow Decay)

This operating mode is realized by switching on both of the low-side FETs of the full-bridge as shown in Figure 7-7. A current circulation path is provided when both low-side FETs are turned on. Due to this circulation path, the current decays to the ground using the resistance of the motor and of the low-side FET. Because this current decay is less when compared to the coast operation because of the low potential difference, this mode is also referred to as the slow decay mode.

Copyright © 2023 Texas Instruments Incorporated

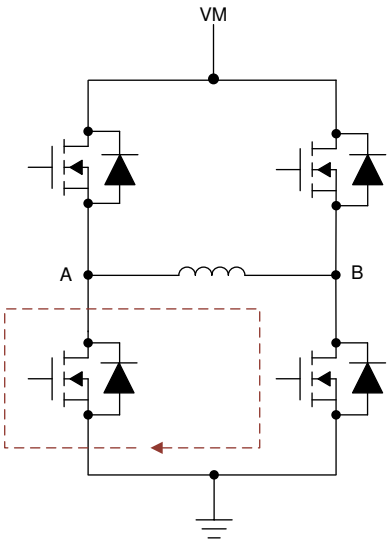



**Figure 7-7. Brake Operation (Slow Decay)**


Copyright © 2023 Texas Instruments Incorporated

### 7.3.3 Bridge Control

The DRV8847 device can be configured in four different operating modes depending on user requirements. The MODE and IN3 pins are used to configure the DRV8847 in one of the four different interfaces: a 4-pin interface, a 2-pin interface, a parallel bridge interface, and the independent bridge interface. Mode selection is done using the $I^2C$ registers in the DRV8847S device variant (see the *Section 7.5* section). Table 7-2 lists the configurations to select the operating mode of the bridges.

**Note**

On the DRV88471, the bridge control mode is fixed to the 4-pin interface.

**Table 7-2. Bridge Mode Selection (DRV8847 Hardware Device Variant)**

| nSLEEP | MODE | IN3 | INTERFACE |
|---|---|---|---|
| 0 | X | X | Sleep mode |
| 1 | 0 | X | 4-pin interface |
| 1 | 1 | 0 | 2-pin interface |
| 1 | 1 | 1 | Parallel bridge interface |
| 1 | Z | X | Independent bridge interface |

**Note**

The MODE pin is not latched during driver operation. Therefore, TI does not recommend connecting this pin to a controller to use at any time.

#### *7.3.3.1 4-Pin Interface*

In the 4-pin interface, the DRV8847 device is configured to drive a stepper motor or two BDC motors with fully functional modes. To configure 4-pin interface operation, connect the MODE pin to ground and use the IN1, IN2, IN3, and IN4 pins to control the drivers. In this mode, the stepper or brushed DC motor can operate with all four modes (forward, reverse, coast, and brake mode) and the stepper motor can operate in either full-stepping mode or the non-circulating half-stepping mode. Sense resistors can be connected to the ISEN12 and ISEN34 pins for independent current regulation in bridge-12 and bridge-34 respectively.

Use this interface option for the following loads:

- Stepper motor in full-stepping mode (with or without current regulation)
- Stepper motor in half-stepping mode (with or without current regulation)
- Single or dual BDC motor (with or without current regulation) with full functional BDC modes (forward, reverse, brake, and coast mode)

Table 7-3 lists the configurations for 4-pin interface operation and Figure 7-8 shows the application diagram for 4-pin interface operation.

**Table 7-3. 4-Pin Interface (MODE = 0)**

| nSLEEP | IN1 | IN2 | IN3 | IN4 | OUT1 | OUT2 | OUT3 | OUT4 | FUNCTION (DC MOTOR) |
|---|---|---|---|---|---|---|---|---|---|
| 0 | X | X | X | X | Z | Z | Z | Z | Sleep mode |
| 1 | 0 | 0 | | | Z | Z | | | Motor coast (fast decay) |
| 1 | 0 | 1 | | | L | H | | | Reverse direction |
| 1 | 1 | 0 | | | H | L | | | Forward direction |
| 1 | 1 | 1 | | | L | L | | | Motor brake (slow decay) |
| 1 | | | 0 | 0 | | | Z | Z | Motor coast (fast decay) |
| 1 | | | 0 | 1 | | | L | H | Reverse direction |
| 1 | | | 1 | 0 | | | H | L | Forward direction |
| 1 | | | 1 | 1 | | | L | L | Motor brake (slow decay) |

Copyright © 2023 Texas Instruments Incorporated

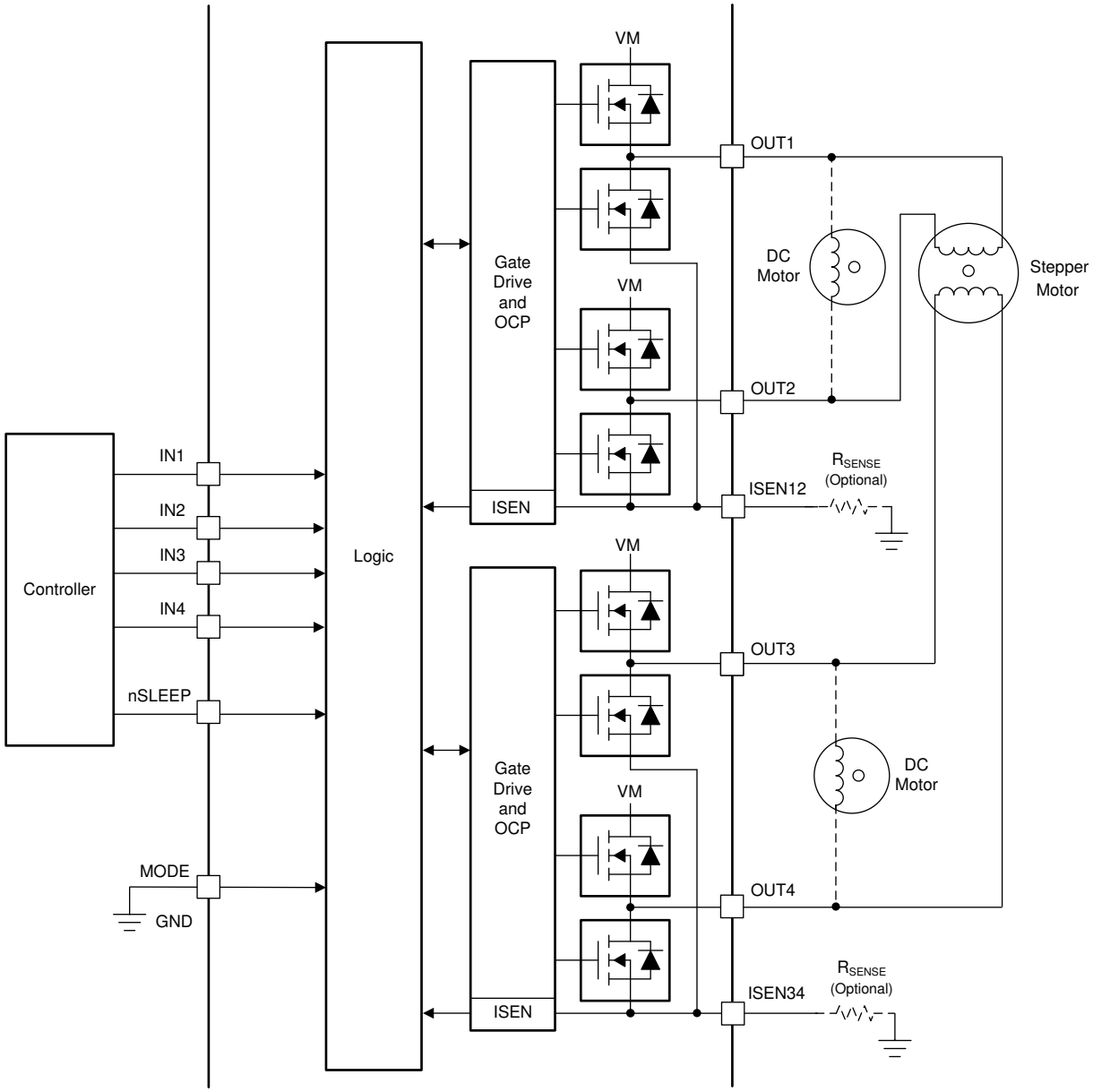



**Figure 7-8. 4-Pin Interface Operation**

### *7.3.3.2 2-Pin Interface*

In the 2-pin interface, the DRV8847 device is configured to drive a stepper motor or two BDC motors with a lower number of control inputs from the microcontroller. To configure the 2-pin interface operation, connect the MODE pin to the external supply (3.3 V or 5 V), connect the IN3 pin to the ground, and use the IN1 and IN2 pins to control the driver. In this mode, the stepper or brushed DC motor operates in only two modes (forward mode and reverse mode) i.e. only full-step operation is supported for the stepper motor. This 2-pin interface is very useful for low GPIO applications such as refrigerator dampers. Sense resistors can be connected to the ISEN12 and ISEN34 pins for current regulation.

Use this interface option for the following loads:

- Stepper motor in full stepping mode (with or without current regulation)
- Single or dual BDC motor (with or without current regulation) with reduced functional BDC modes (forward and reverse mode only)


Copyright © 2023 Texas Instruments Incorporated

Table 7-4 lists the configurations for 2-pin interface operation and Figure 7-9 shows the application diagram for 2-pin interface operation.

**Table 7-4. 2-Pin Interface (MODE = 1, IN3 = 0)**

| nSLEEP | IN1 | IN2 | IN3 | IN4 | OUT1 | OUT2 | OUT3 | OUT4 | FUNCTION (DC MOTOR) |
|---|---|---|---|---|---|---|---|---|---|
| 0 | X | X | X | X | Z | Z | Z | Z | Sleep mode |
| 1 | 0 | | 0 | X | L | H | | | Reverse direction |
| 1 | 1 | | 0 | X | H | L | | | Forward direction |
| 1 | | 0 | 0 | X | | | L | H | Reverse direction |
| 1 | | 1 | 0 | X | | | H | L | Forward direction |

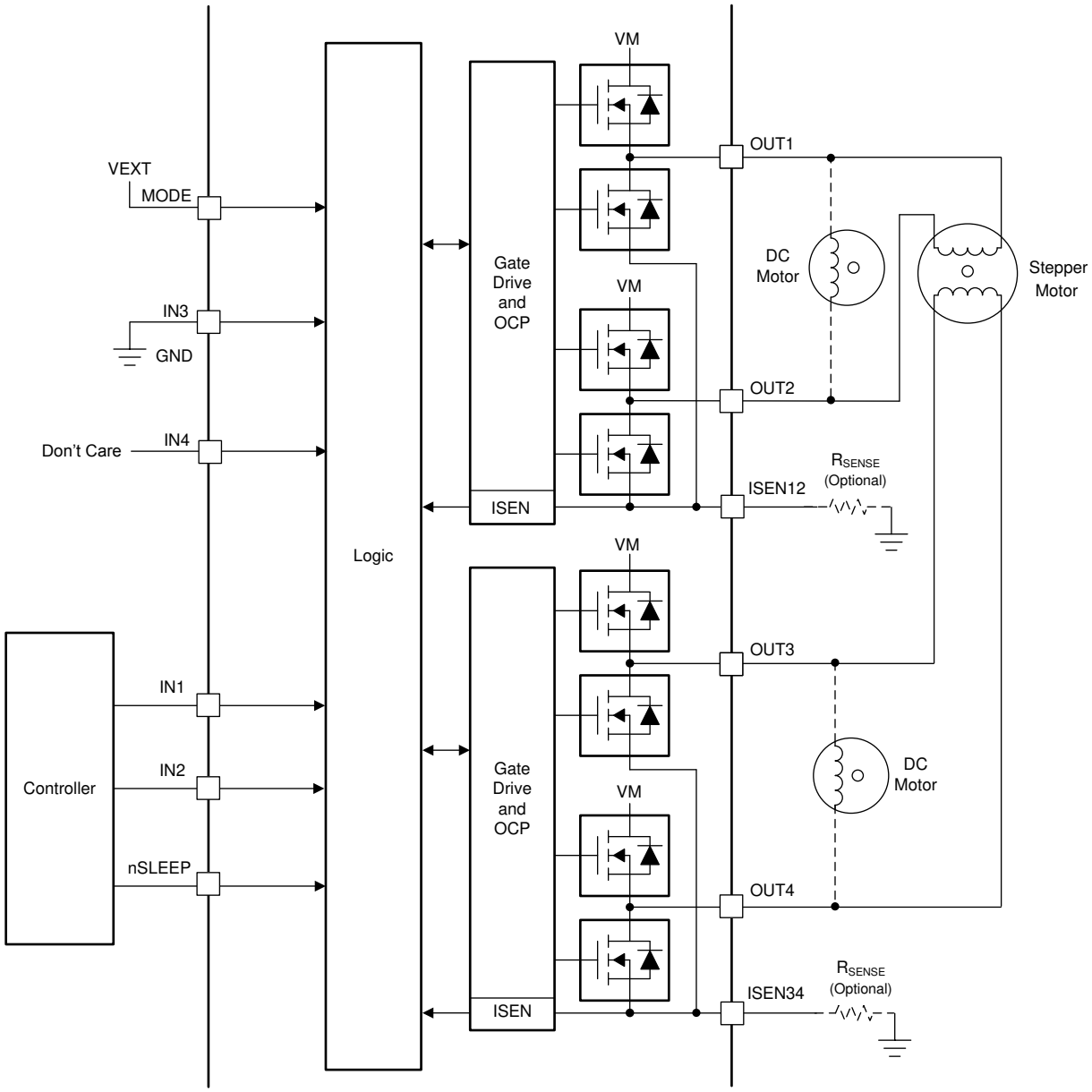



**Figure 7-9. 2-Pin Interface Operation**

**Note**

In this mode, two of the OUTx pins are always 'ON' if the device is in a non-sleep state (nSLEEP = HIGH). Therefore, to completely de-energize the motor-coils connected to OUTx pins, the user has to pull-down the nSLEEP pin.

#### *7.3.3.3 Parallel Bridge Interface*

In the parallel bridge interface, the DRV8847 device is configured to drive a higher current BDC motor by using the driver in parallel to deliver twice the motor current. To go to parallel bridge interface operation, connect the MODE and IN3 pins to the external supply (3.3 V or 5 V) and use the IN1 and IN2 pins to control the driver. This mode can deliver the full functionality of the BDC motor control with all four modes (forward, reverse, coast, and brake mode).

Use this interface option for the following loads:

- One high current BDC motor (with or without current regulation) with full functional BDC modes (forward, reverse, brake, and coast mode)
- Two independent BDC motors operating together (with or without current regulation) with full functional BDC modes (forward, reverse, brake, and coast mode)

Table 7-5 lists the configurations for parallel bridge interface operation, and Figure 7-10 shows the application diagram for parallel bridge interface operation.

**Table 7-5. Parallel Interface (MODE = 1, IN3 = 1)**

| nSLEEP | IN1 | IN2 | IN3 | IN4 | OUT1 | OUT2 | OUT3 | OUT4 | FUNCTION (DC MOTOR) |
|---|---|---|---|---|---|---|---|---|---|
| 0 | X | X | X | X | Z | Z | Z | Z | Sleep mode |
| 1 | 0 | 0 | 1 | X | Z | Z | Z | Z | Motor coast (fast decay) |
| 1 | 0 | 1 | 1 | X | L | H | L | H | Reverse direction |
| 1 | 1 | 0 | 1 | X | H | L | H | L | Forward direction |
| 1 | 1 | 1 | 1 | X | L | L | L | L | Motor brake (slow decay) |


Copyright © 2023 Texas Instruments Incorporated

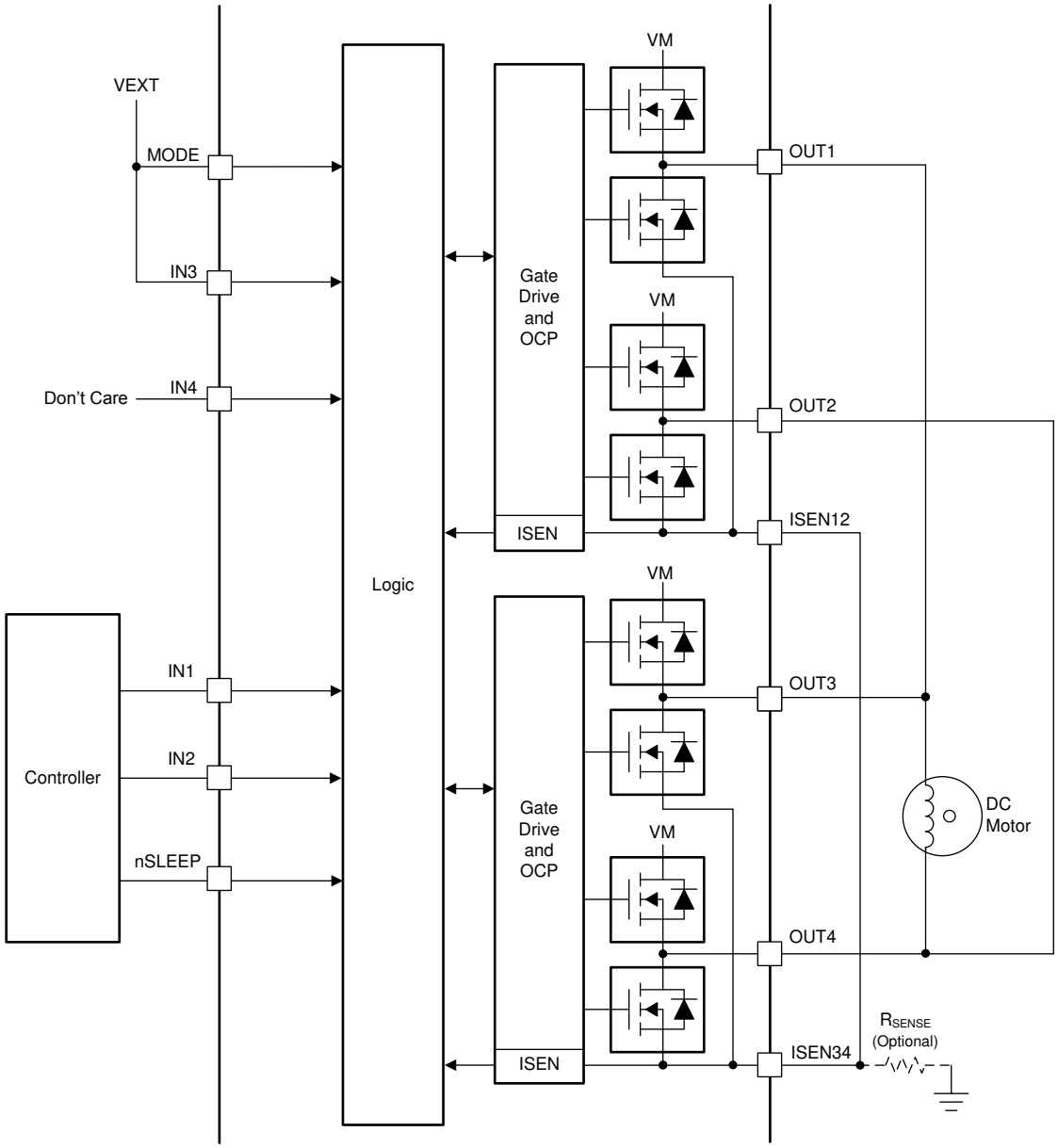



**Figure 7-10. Parallel Mode Operation**

### *7.3.3.4 Independent Bridge Interface*

In the independent bridge interface, the DRV8847 device is configured for independent half-bridge operation. To configure independent bridge interface operation, leave the MODE pin unconnected (Hi-Z state) and use the IN1, IN2, IN3, and IN4 pins to independently control the OUT1, OUT2, OUT3, and OUT4 pins respectively. Only two output states of the OUTx pin can be controlled (either connected to VM or connected to GND). This mode is used to drive independent loads such as relays and solenoids.

Use this interface option for the following loads:

- Relay or solenoid coils connected between OUTx and VM/ground pin without current regulation
- Single or dual BDC motor (with or without current regulation) with three functional BDC modes (forward, reverse, and braking mode only)
- Stepper motor in full-stepping mode (with or without current regulation)
- Stepper motor in half-stepping mode (with or without current regulation) using brake mode

Copyright © 2023 Texas Instruments Incorporated

Table 7-6 lists the configurations for independent bridge interface operation and Figure 7-11 shows the application diagram for independent bridge interface operation.

**Table 7-6. Independent Bridge Interface (MODE = Hi-Z)**

| nSLEEP | IN1 | IN2 | IN3 | IN4 | OUT1 | OUT2 | OUT3 | OUT4 | FUNCTION (DC MOTOR) |
|---|---|---|---|---|---|---|---|---|---|
| 0 | X | X | X | X | Z | Z | Z | Z | Sleep mode |
| 1 | 0 | | | | L | | | | OUT1 connected to GND |
| 1 | 1 | | | | H | | | | OUT1 connected to VM |
| 1 | | 0 | | | | L | | | OUT2 connected to GND |
| 1 | | 1 | | | | H | | | OUT2 connected to VM |
| 1 | | | 0 | | | | L | | OUT3 connected to GND |
| 1 | | | 1 | | | | H | | OUT3 connected to VM |
| 1 | | | | 0 | | | | L | OUT4 connected to GND |
| 1 | | | | 1 | | | | H | OUT4 connected to VM |


Copyright © 2023 Texas Instruments Incorporated

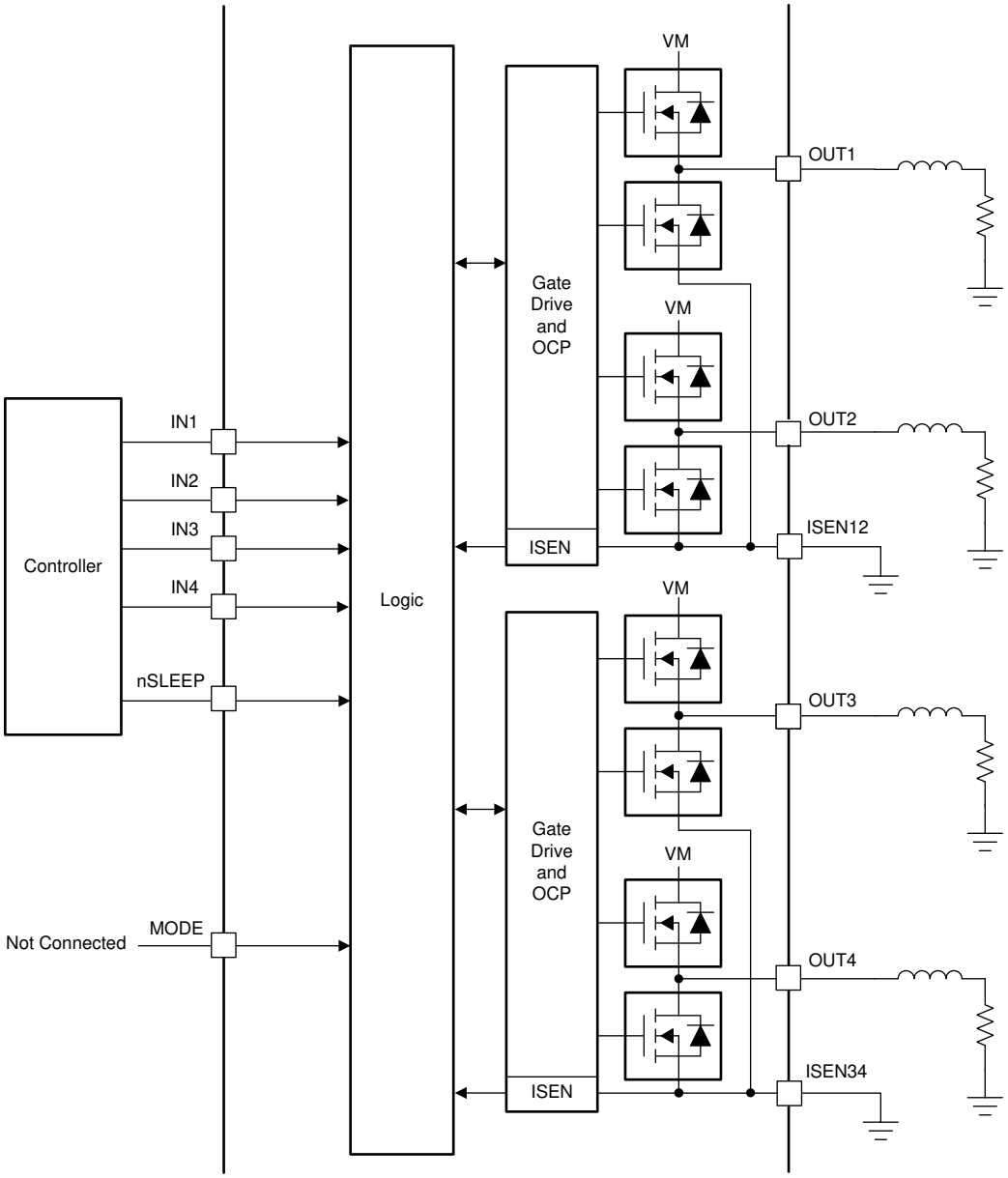



**Figure 7-11. Independent Bridge Interface**

### 7.3.4 Current Regulation

The current through the motor windings is regulated by a fixed off-time PWM current regulation circuit. With brushed DC motors, current regulation can be used to limit the stall current (which is also the start-up current) of the motor.

Current regulation works as follows: When an H-bridge is enabled, current rises through the winding at a rate dependent on the supply voltage and inductance of the winding. If the current reaches the current trip threshold, the bridge disables the current for a time $t_{OFF}$ before starting the next PWM cycle.

**Note**

Immediately after the current is enabled, the voltage on the ISENxx pin is ignored for a while ($t_{BLANK}$) before enabling the current sense circuitry. This blanking time also sets the minimum on-time of the PWM cycle.

Copyright © 2023 Texas Instruments Incorporated

The PWM trip current is set by a comparator which compares the voltage across a current sense resistor connected to the ISENxx pin with a reference voltage. This reference voltage ($V_{TRIP}$) is generated on-chip and decides the current trip level.

The full-scale trip current in a winding is calculated as shown in Equation 1.

$$I_{TRIP} = \text{Torque} \frac{V_{TRIP}}{R_{SENSExx}} \quad (1)$$

where

- $I_{TRIP}$ is the regulated current.
- $V_{TRIP}$ is the internally generated trip voltage.
- $R_{SENSExx}$ is the resistance of the sense resistor.
- Torque is the torque scalar, the value of which depends on the input on the TRQ pin. TRQ = 100% for TRQ pin connected to GND (DRV8847) or TRQ bit set to 0 (DRV8847S) and TRQ = 50% connected to $V_{EXT}$ (DRV8847) or TRQ bit set to 1 (DRV8847S).

For example, if the $V_{TRIP}$ voltage is 150 mV and the value of the sense resistor is 150 mΩ, the full-scale trip current is 1 A (150 mV / (150 mΩ) = 1 A).

**Note**

If the current control is not needed, connect the ISENxx pins directly to the ground.

### 7.3.5 Current Recirculation and Decay Modes

During PWM current trip operation, the H-bridge is enabled to drive current through the motor winding until the trip threshold of the current regulation is reached. After the trip current threshold is reached, the drive current is interrupted, but, because of the inductive nature of the motor, the current must continue to flow for some time. This continuous flow of current is called recirculation current. A mixed decay allows better current regulation by optimizing the current ripple by using fast and slow decay.

Mixed decay is a combination of fast and slow decay modes. In fast decay mode, the anti-parallel diodes of the opposite FETs are conducting on to let the current decay faster as shown in Figure 7-12 (see case 2). In slow decay mode, the winding current is recirculated by enabling both low-side FETs in the bridge (see case 3 in Figure 7-12). Mixed decay starts with fast decay, and then goes to slow decay. In the DRV8847 device, the mixed decay ratio is 25% fast decay and 75% slow decay as shown in Figure 7-13.


Copyright © 2023 Texas Instruments Incorporated

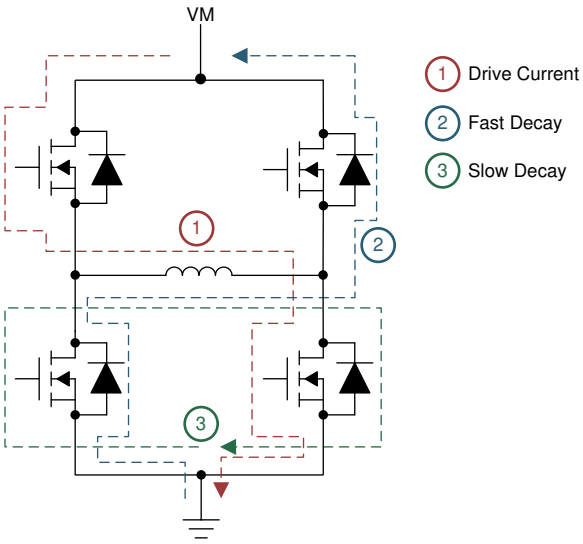



**Figure 7-12. Decay Modes**

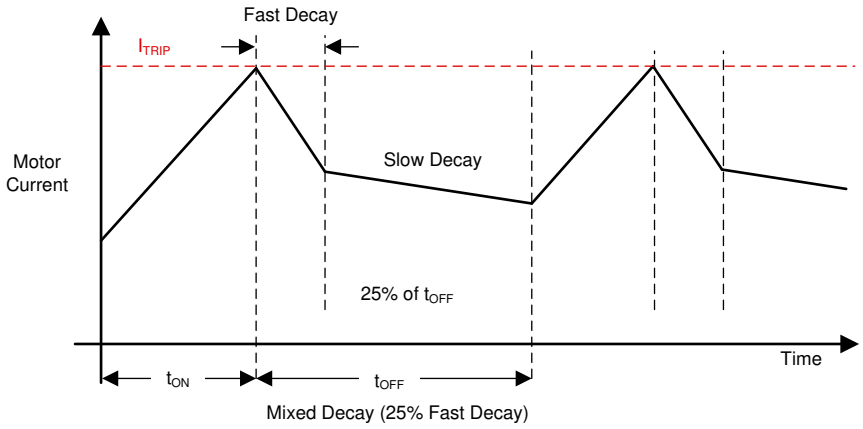



**Figure 7-13. Mixed Decay**

**Note**

The current regulation scheme uses a single sense resistor and hence always works for two-half bridges even when used in an "Independent Bridge Interface". It is recommended that current regulations not be used for loads using independent half bridges.

### 7.3.6 Torque Scalar

The torque scalar is used to dynamically adjust the output current through a digital input pin, TRQ. This torque scalar decreases the trip reference value of the output current to 50% (whenever the TRQ pin is pulled-high). A torque scalar can be used to scale the holding torque of the stepper motor. For the $I^2C$ device variant (DRV8847S), this feature is implemented through an $I^2C$ register.

**Note**

On the DRV88471, the torque scalar value is fixed to 100%.

When the TRQ pin is pulled-low (or the TRQ bit is reset in the DRV8847S device variant), the trip current is calculated using Equation 2.

Copyright © 2023 Texas Instruments Incorporated

$$I_{TRIP} = \frac{Torque \times V_{TRIP}}{R_{SENSExx}} \quad (2)$$

When the TRQ pin is pulled-high (or the TRQ bit is set in the DRV8847S device variant), the trip current is calculated using Equation 3.

$$I_{TRIP} = 0.5 \frac{V_{TRIP}}{R_{SENSExx}} \quad (3)$$


Copyright © 2023 Texas Instruments Incorporated

### 7.3.7 Stepping Modes

The DRV8847 device is used to drive a stepper motor in full-stepping mode or non-circulating half-stepping mode using the following bridge configurations:

- Full-stepping mode (with or without current regulation)
  - Using 4-pin interface configuration
  - Using 2-pin interface configuration
- Half-stepping mode (with or without current regulation)
  - Using 4-pin interface configuration

#### *7.3.7.1 Full-Stepping Mode (4-Pin Interface)*

In full-stepping mode, the full-bridge operates in either of two modes (forward or reverse mode) with a phase shift of 90° between the two windings.

In 4-pin interface, the PWM input is applied to the IN1, IN2, IN3, and IN4 pins as shown in Figure 7-14 and the driver operates only in forward (FRW) and reverse (REV) mode.

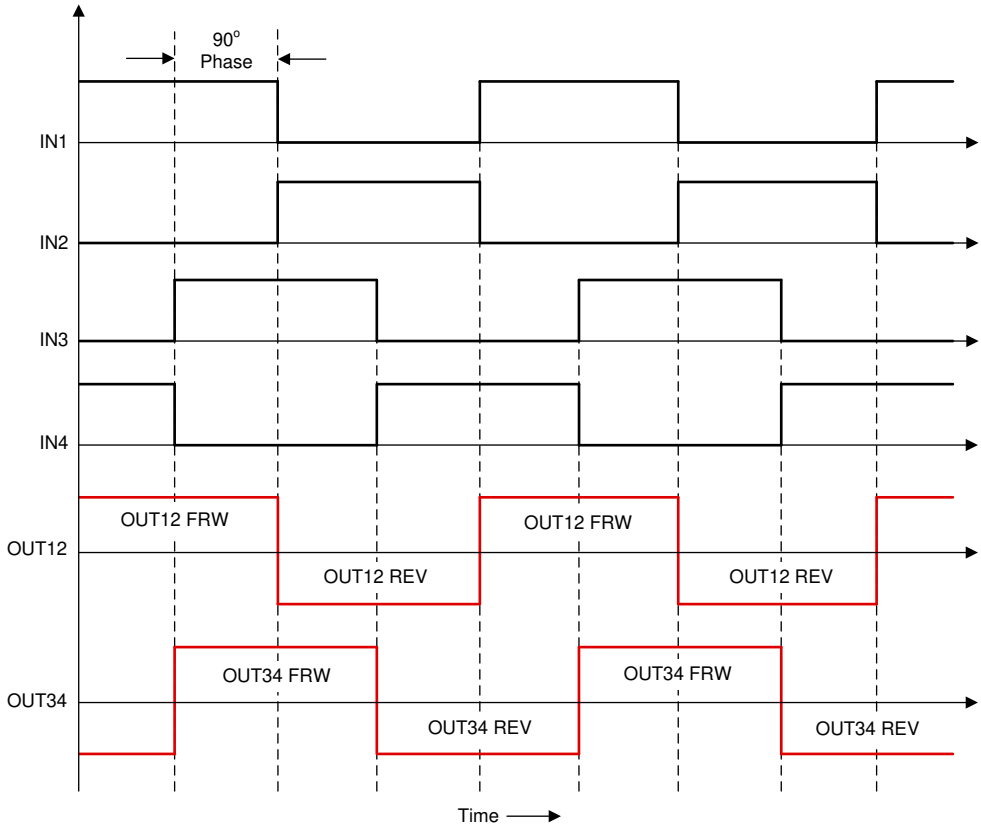



**Figure 7-14. Full-Stepping Mode Using 4-Pin Interface**

Copyright © 2023 Texas Instruments Incorporated

### 7.3.7.2 Full-Stepping Mode (2-Pin Interface)

In full-stepping using the 2-pin interface, the PWM input is only applied to the IN1 and IN2 pins, and the IN3 is connected to ground (see the *Figure 7-9* section). Figure 7-15 shows the full-stepping mode of stepper motor using the 2-pin interface

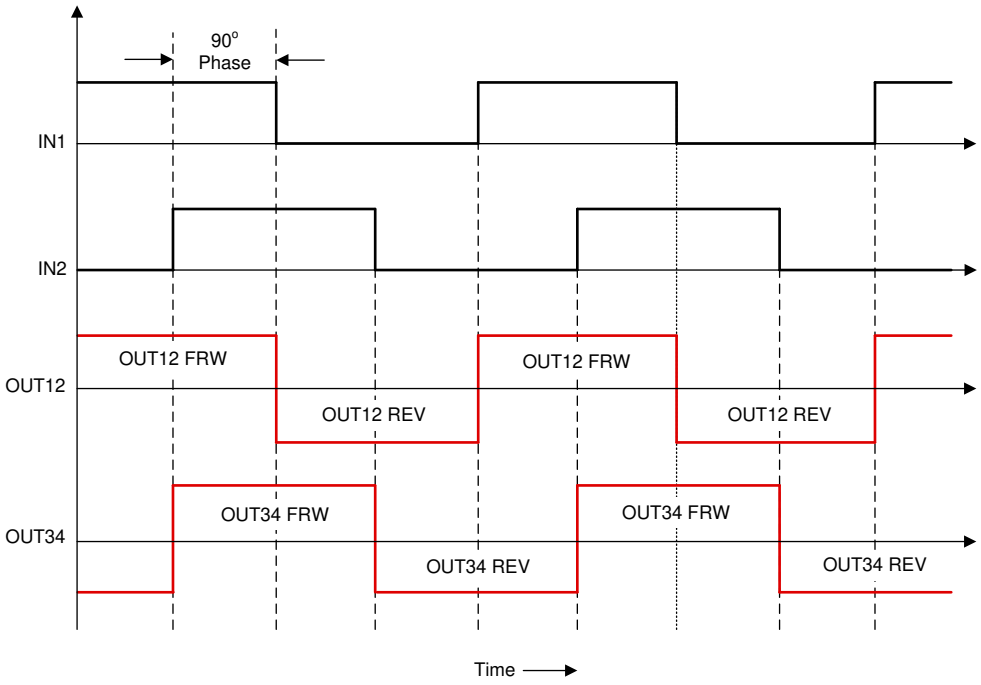



**Figure 7-15. Full-Stepping Mode Using 2-Pin Interface**


Copyright © 2023 Texas Instruments Incorporated

### *7.3.7.3 Half-Stepping Mode (With Non-Driving Fast Decay)*

In half-stepping mode, the full-bridge operates in one of the three modes (forward, reverse, or coast mode) with a phase shift of 45° between the two windings.

In 4-pin interface, the PWM input is connected to the IN1, IN2, IN3, and IN4 pins as shown in Figure 7-16, and the driver operates in forward, reverse, and coast mode.

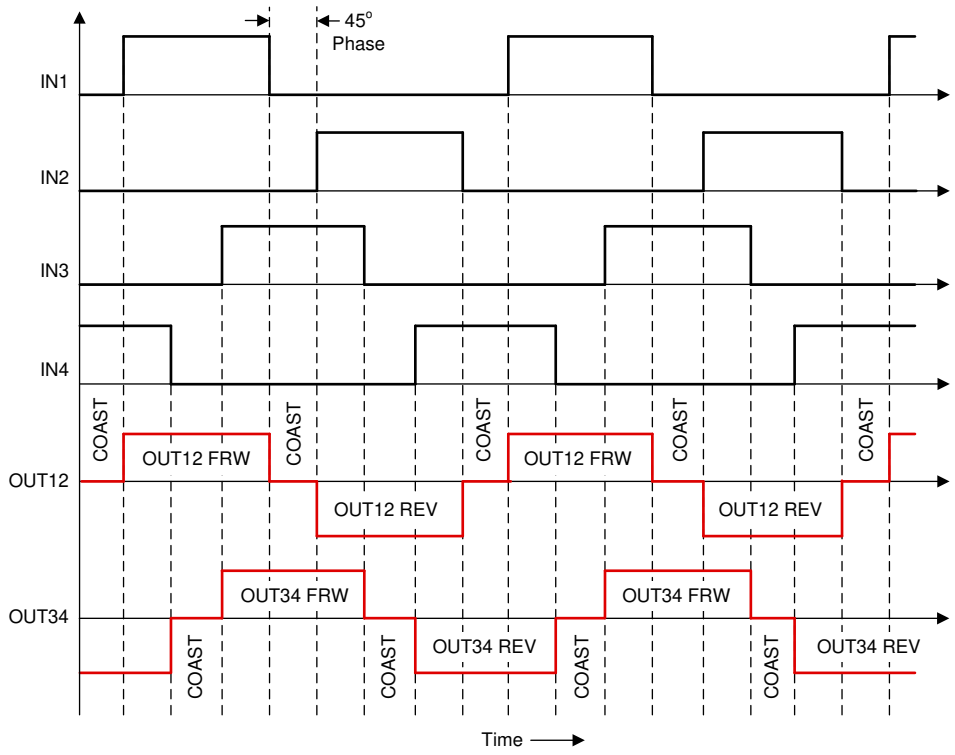



**Figure 7-16. Half-Stepping Mode Using 4-Pin Interface (With Non-Driving Fast Decay)**

### 7.3.7.4 Half-Stepping Mode (With Non-Driving Slow Decay)

In this half-stepping mode, the non-driving state is slow decay (braking mode). Therefore, the full-bridge operates in one of the three modes (forward, reverse, or brake mode) with a phase shift of 45° between the two windings.

In 4-pin interface, the PWM input is connected to the IN1, IN2, IN3, and IN4 pins as shown in Figure 7-17, and the driver operates in forward, reverse, and brake mode.

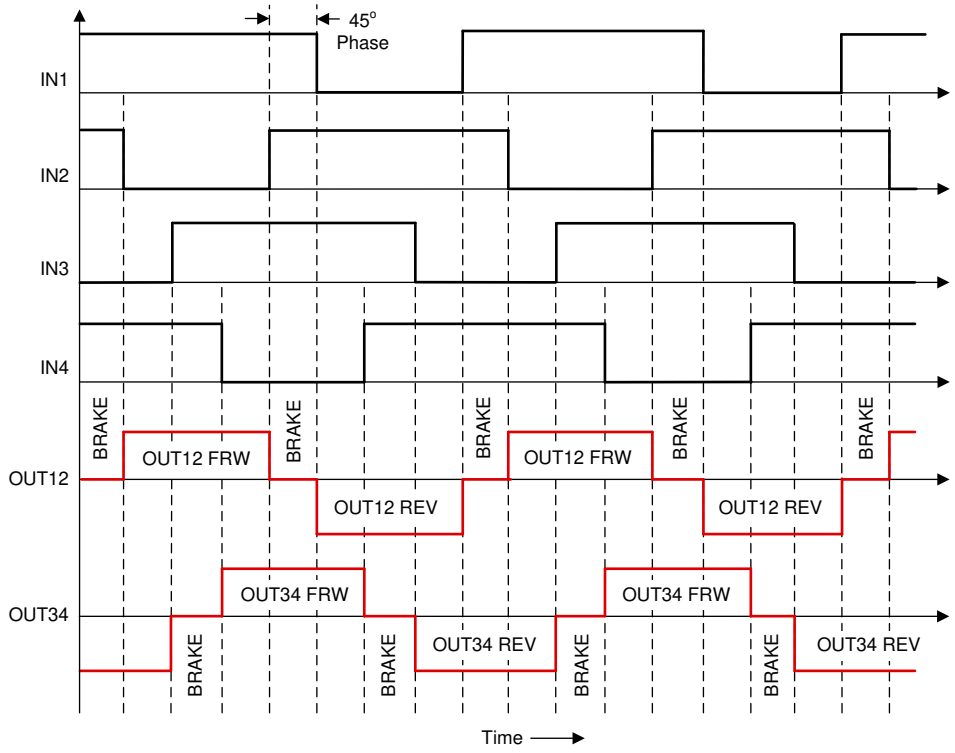



**Figure 7-17. Half-Stepping Mode Using 4-Pin Interface (With Non-Driving Slow Decay)**


Copyright © 2023 Texas Instruments Incorporated

### 7.3.8 Motor Driver Protection Circuits

The DRV8847 device is protected against VM undervoltage, overcurrent, open load, and over temperature events.

#### *7.3.8.1 Overcurrent Protection (OCP)*

The DRV8847 is protected against overcurrent by overcurrent protection trip. The OCP circuit on each FET disables the current flow through the FET by removing the gate drive. If this overcurrent detection continues for longer than the OCP deglitch time ($t_{OCP}$), all FETs in the H-bridge (or half-bridge in the independent interface) are disabled and the nFAULT pin is driven low. The DRV8847 device stays disabled until the retry time $t_{RETRY}$ occurs whereas the DRV8847S device has a programmable option for auto-retry or the latch mode.

##### 7.3.8.1.1 OCP Automatic Retry (Hardware Device and Software Device (OCPR = 0b))

After an OCP event in this mode, the corresponding half-bridges, full-bridge, or both bridges (depending on the MODE bits) are disabled and the nFAULT pin is driven low (see Table 7-13 and Table 7-14). The OCP and corresponding OCPx bits are latched high in the $I^2C$ registers (see the *Section 7.6* section). Normal operation resumes automatically (motor driver operation and the nFAULT pin is released) after the $t_{RETRY}$ time elapses as shown in Figure 7-18. The OCP and OCPx bits remain latched until the $t_{RETRY}$ period expires.

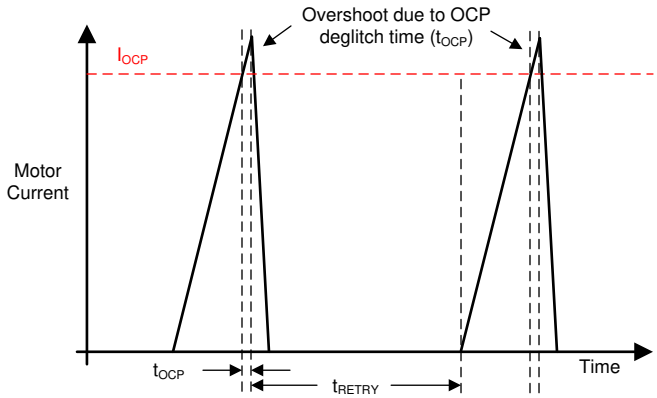



**Figure 7-18. OCP Operation**

##### 7.3.8.1.2 OCP Latch Mode (Software Device (OCPR = 1b))

OCP latch mode is only available in the DRV8847S device. After an OCP event, the corresponding half-bridges, full-bridge, or both bridges (depending on the MODE bits) are disabled and the nFAULT pin is driven low. The OCP and corresponding OCPx bits are latched high in the $I^2C$ registers (see the *Section 7.6* section). Normal operation continues (motor driver operation and the nFAULT pin is released) when the OCP condition is removed and a clear faults command is issued through the CLR_FLT bit.

##### 7.3.8.1.3

**Note**

For supply voltage, $V_{VM}$ > 16.5-V, if the OUTx current (FET current) exceeds 4-A, then the device operation is pushed beyond the safe operating area (SOA) of the device. User has to ensure that the FET-current is below 4-A for device safe operation for supply voltage above 16.5-V.

#### *7.3.8.2 Thermal Shutdown (TSD)*

If the die temperature exceeds thermal shutdown limits ($T_{TSD}$), all FETs in the H-bridge are disabled and the nFAULT pin is driven low. After the die temperature decreases to a value within the specified limits, normal operation resumes automatically. The nFAULT pin is released after operation starts again.

Copyright © 2023 Texas Instruments Incorporated

### 7.3.8.3 VM Undervoltage Lockout (VM_UVLO)

Whenever the voltage on the VM pin falls below the UVLO falling threshold voltage, $V_{UVLO}$, all circuitry in the device is disabled, and all internal logic is reset. Operation continues when the $V_{VM}$ voltage rises above the UVLO rising threshold as shown in Figure 7-19. The nFAULT pin is driven low during an undervoltage condition and is released after operation starts again.

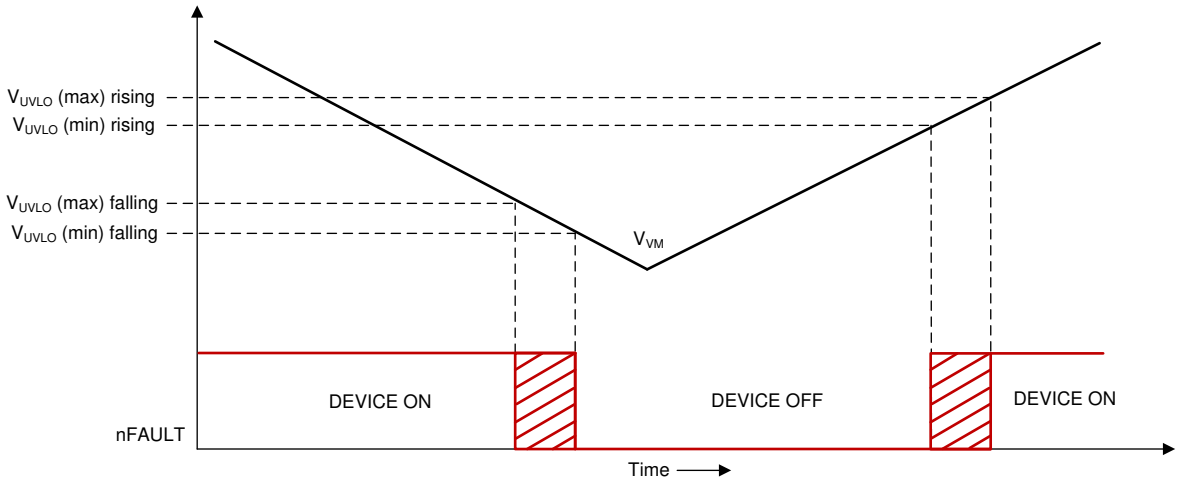



**Figure 7-19. VM UVLO Operation**

### 7.3.8.4 Open Load Detection (OLD)

An open load detection feature is also implemented in this device. This diagnostic test runs at device power up or when the DRV8847 device comes out from sleep mode (rising edge on the nSLEEP pin). The OLD diagnostic test can run any time in the I$^2$C variant device (DRV8847S) using the OLDOD (OLD On Demand) bit.

The OLD implementation is done on the full-bridge and the half-bridge. In the DRV8847 device, during an open-load condition, the half-bridges, full-bridge, or both bridges (depending on the MODE pin) are always operating and the nFAULT pin is pulled-low. The user must reset the power to release the nFAULT pin by doing the OLD sequence again. Table 7-7 lists the different OLD scenarios for the DRV8847 device.

In the DRV8847S device, the user can program the full-bridge or half-bridge to be in the operating mode or the Hi-Z state, whenever an open-load condition is detected by using the OLDBO (OLD Bridge Operation) bit. Moreover, the nFAULT signaling on the OLD bit can be disabled using the OLDFD (OLD Fault Disable) bit. For detailed I$^2$C register settings, see the *Section 7.6* section. Table 7-8 lists the different OLD scenarios for the DRV8847S device.

**Note**

For accurate OLD operation, the user must ensure that the motor is stationary (or current in connected load becomes zero) before the open load on-demand command is executed.


Copyright © 2023 Texas Instruments Incorporated

**Table 7-7. Open Load Detection in DRV8847**

| INTERFACE | LOAD TYPE | OLD | BRIDGE OPERATION | nFAULT |
|---|---|---|---|---|
| 4-pin 2-pin | Full-Bridge Connected | NO | YES | NO |
| | Half-Bridge Connected | NO | YES | NO |
| | Bridge Open | YES | YES | YES |
| | One Half-Bridge Open | YES | YES | YES |
| Parallel bridge | Full-Bridge Connected | NO | YES | NO |
| | Half-Bridge Connected | NO | YES | NO |
| | Bridge Open | YES | YES | YES |
| | One Half-Bridge Open | YES | YES | YES |
| Independent bridge | Full-Bridge Connected | NO | YES | NO |
| | Half-Bridge Connected | NO | YES | NO |
| | Bridge Open | YES | YES | YES |
| | One Half-Bridge Open | YES | YES | YES |

**Table 7-8. Open Load Detection in DRV8847S (Full-bridge-12)**

| INTERFACE | LOAD TYPE | OLD | BRIDGE OPERATION(1) | | nFAULT | OLD BITS | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | OLDBO = 0b | OLDBO = 1b | | OLD1 | OLD2 | OLD3 | OLD4 |
| 4-pin 2-pin | Full-bridge connected | NO | YES | YES | NO | 0b | 0b | X | X |
| | Half-bridge connected | NO | YES | YES | NO | 0b | 0b | X | X |
| | Bridge open | YES | YES | NO | YES | 1b | 1b | X | X |
| | One half-bridge open | YES | YES | NO | YES | 1b or 0b (2) | 0b or 1b | X | X |
| Parallel bridge | Full-bridge connected | NO | YES | YES | NO | 0b | 0b | X | X |
| | Half-bridge connected | NO | YES | YES | NO | 0b | 0b | X | X |
| | Bridge open | YES | YES | NO | YES | 1b | 1b | X | X |
| | One half-Bridge Open | YES | YES | NO | YES | 1b or 0b | 0b or 1b | X | X |
| Independent bridge | Full-Bridge Connected | NO | YES | YES | NO | 0b | 0b | X | X |
| | Half-Bridge Connected | NO | YES | YES | NO | 0b | 0b | X | X |
| | Bridge Open | YES | YES | NO | YES | 1b | 1b | X | X |
| | One Half-Bridge Open | YES | YES | NO | YES | 1b or 0b | 0b or 1b | X | X |

(1) The operation of the bridge is subjected to the selected mode type:
- In 4-pin or 2-pin interface, the corresponding bridge is in the operating or Hi-Z state.
- In parallel bridge (BDC) interface, both bridges are in the operating or Hi-Z state.
- In independent bridge interface, the corresponding half-bridge is in the operating or Hi-Z state.

(2) Depending on which half-bridge is open, the corresponding bit in the $I^2C$ register is set.

The open-load detect sequence comprise of three detection states in which the driver ensures that any of the load is either connected or open as follows.

Copyright © 2023 Texas Instruments Incorporated

#### 7.3.8.4.1 Full-Bridge Open Load Detection

As shown in Figure 7-20, during device wakeup, a constant current source pulls the OUT1 pin to the AVDD (internal) fixed voltage which allows current flow from OUT1 to OUT2 terminal. The current drawn is completely dependent on the motor resistance between OUT1 and OUT2. Depending on this current and the comparator threshold voltage ($V_{OL_HS}$ and $V_{OL_LS}$), the comparator output OL1_HS and OL2_LS are either set or reset which determines the open load status. Table 7-9 shows the states of OL1_HS and OL2_LS for the open load detect. This test executes before the $t_{WAKE}$ or $t_{ON}$ time has elapsed. When an open load is detected, the nFAULT pin is latched low until the device is power cycled or device reset with nSLEEP pin. A similar implementation is done for the OUT3 and OUT4 pins.

**Table 7-9. Open Load Detection for Full-Bridge Connection**

| OL1_HS | OL2_LS | OLD STATUS |
|---|---|---|
| 0 | 0 | NO OLD |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | OLD |


Copyright © 2023 Texas Instruments Incorporated

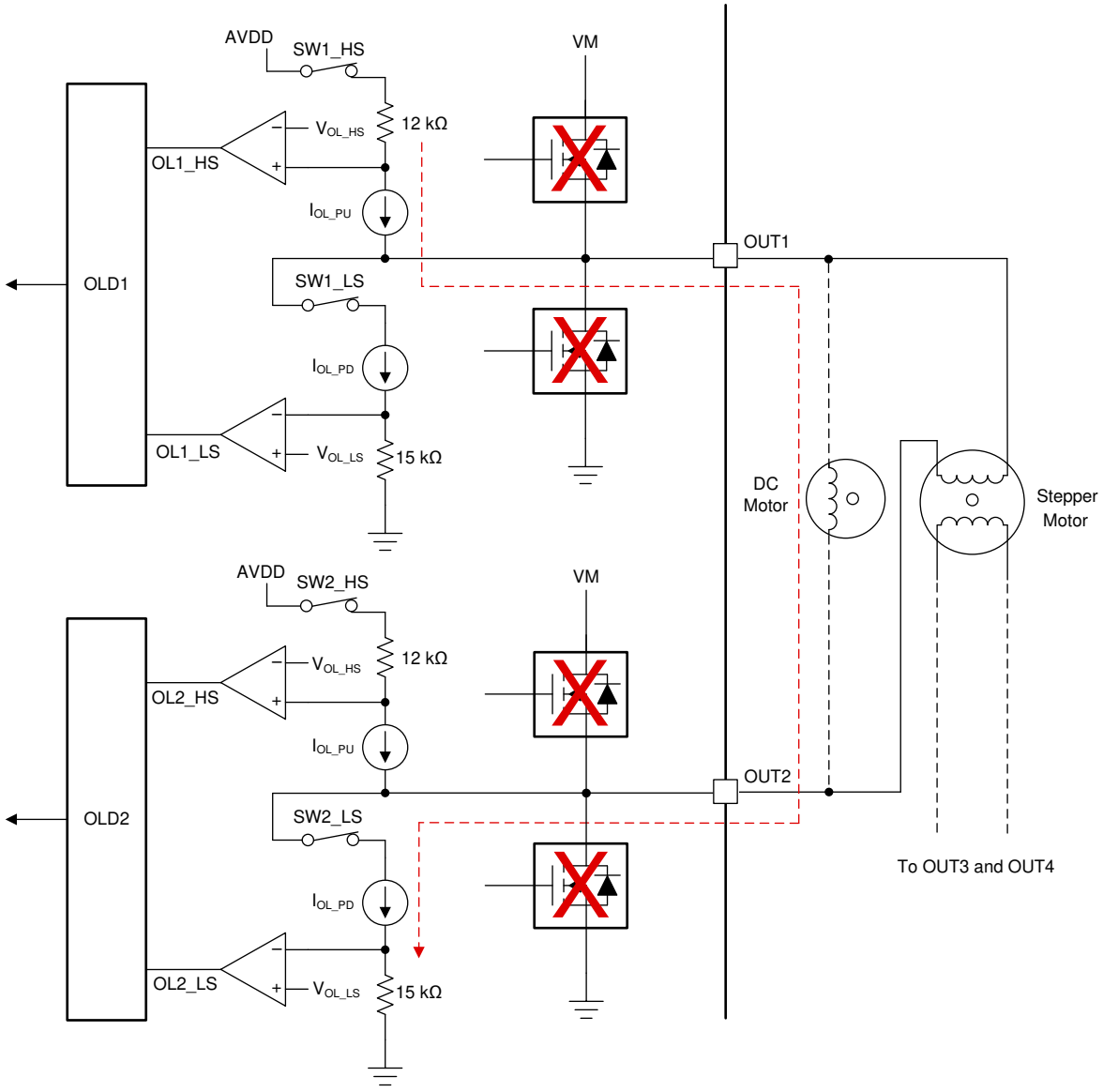



**Figure 7-20. Open Load Detect Circuit for Full-Bridge Connection**

**Note**

AVDD voltage is the internal regulator voltage and is determined as min ($V_{VM}$, 4.2 V). Hence, for supply voltage ($V_{VM}$) higher than 4.2 V, this voltage is fixed at 4.2 V else it is equal to supply voltage ( $V_{VM}$).

#### 7.3.8.4.2 Load Connected to VM

For detection of the VM connected load, a constant current source pull-down the OUT1 node as shown in Figure 7-21. This allows the current to flow from VM to OUT1 depending upon the value of load resistor ($R_L$) connected between OUT1 and VM. Higher current (not open load) will allow the OL1_LS comparator to set and higher current resets the comparator output as shown in Table 7-10 for open load detection.

**Table 7-10. Open Load Detection for VM Connected Load**

| OL1_LS | OLD STATUS |
|---|---|
| 0 | NO OLD |

**Table 7-10. Open Load Detection for VM Connected Load (continued)**

| OL1_LS | OLD STATUS |
|---|---|
| 1 | OLD |

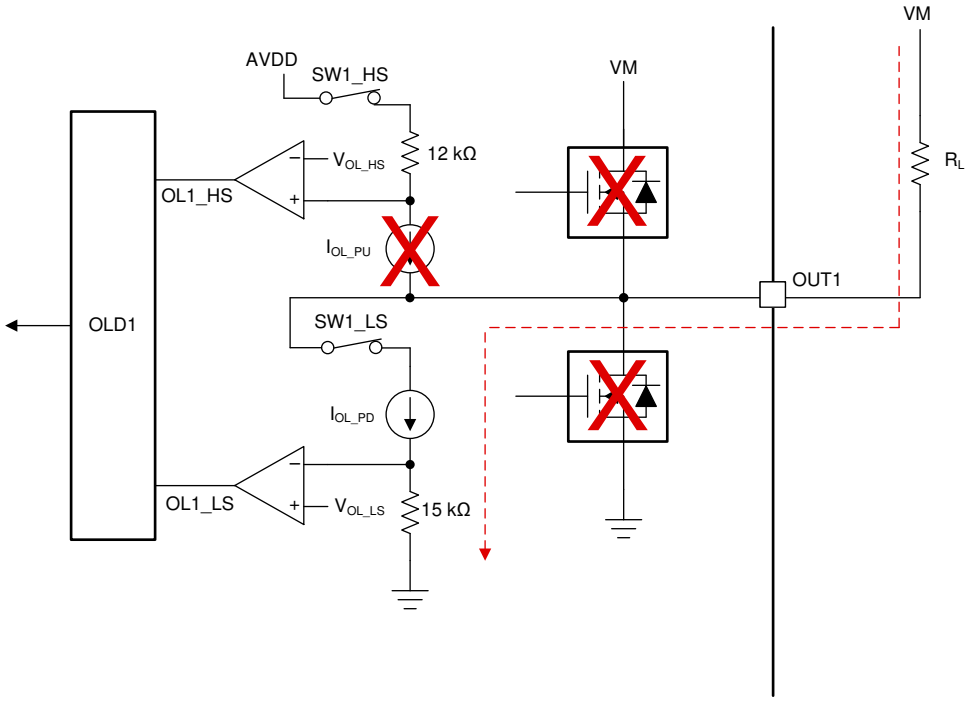



**Figure 7-21. Open Load Detect Circuit for Load Connected to VM**


Copyright © 2023 Texas Instruments Incorporated

#### 7.3.8.4.3 Load Connected to GND

For detection of the GND connected load, the OUT1 node is pulled-up by the internal current source and the internal (4.2-V) fixed voltage as shown in Figure 7-22. This allows the current to flow from OUT1 to GND depending upon the value of load resistor ($R_L$) connected between OUT1 and GND. Higher current (not open load) will allow the OL1_HS comparator to set and higher current resets the comparator output as shown in Table 7-11.

**Table 7-11. Open Load Detection for GND Connected Load**

| OL1_HS | OLD STATUS |
|---|---|
| 0 | NO OLD |
| 1 | OLD |

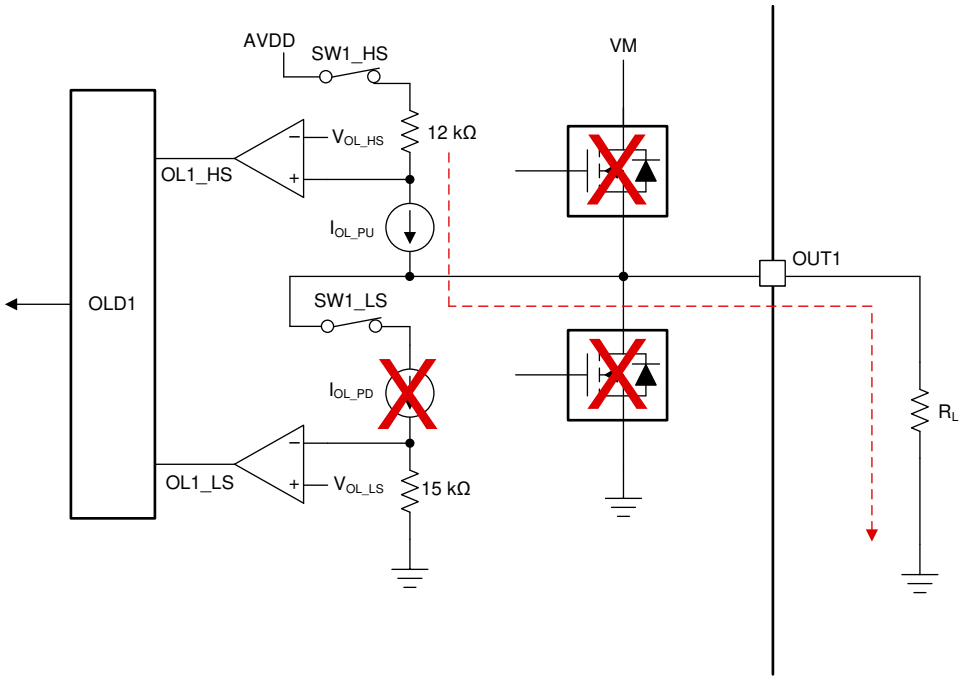



**Figure 7-22. Open Load Detect Circuit for Load Connected to GND**

## 7.4 Device Functional Modes

The DRV8847 device is active until the nSLEEP pin is pulled logic low. In sleep mode, the internal circuitry (charge pump and regulators) is disabled and all internal FETs are disabled (Hi-Z state).

The device goes to operating mode automatically if the nSLEEP pin is pulled logic high. $t_{WAKE}$ must elapse before the device is ready for inputs. The nFAULT pin asserts for small duration during power-up. Various functional modes are described in Table 7-12.

The DRV8847 device goes to a fault mode in the event of VM undervoltage (UVLO), overcurrent (OCP), open-load detection (OLD), and thermal shutdown (TSD). The functionality of each fault depends on the type of fault listed in Table 7-13 for the DRV8847 device and Table 7-14 for the DRV8847S device.

**Note**

The $t_{SLEEP}$ time must elapse before the device goes to sleep mode.

**Table 7-12. Functional Modes**

| MODE | CONDITION | H-BRIDGE | INTERNAL CIRCUITS |
|---|---|---|---|
| Operating | 2.7 V < $V_{VM}$ < 18 V<br>nSLEEP pin = 1 | Operating | Operating |
| Sleep | 2.7 V < $V_{VM}$ < 18 V<br>nSLEEP pin = 0 | Disabled | Disabled |
| Fault | Any fault condition met | Depends on fault | Depends on fault |

**Table 7-13. Fault Support for DRV8847**

| FAULT | INTERFACE | CONDITION | REPORT | H-BRIDGE | INTERNAL CIRCUITS | RECOVERY |
|---|---|---|---|---|---|---|
| VM undervoltage (VM_UVLO) | All interfaces | VM < $V_{UVLO}$ | nFAULT | Both H-bridges in Hi-Z state | Shutdown | **Automatic:** VM > $V_{UVLO}$ |
| Overcurrent (OCP) | 4-pin<br>2-pin | I > $I_{OCP}$ | nFAULT | Corresponding H-bridges in Hi-Z state | Operating | **Automatic:** $t_{RETRY}$ |
| | Parallel bridge | | | Both H-bridges in Hi-Z state | | |
| | Independent bridge | | | Corresponding half-bridges in Hi-Z state | | |
| Open load detect (OLD) | 4-pin | Full-bridge open | nFAULT | H-bridge in operating mode | Operating | **Power cycle / RESET:** OUTx Connected |
| | 2-pin Parallel bridge | Full-bridges open | nFAULT | Both H-bridges in operating mode | | |
| | Independent bridge | Half-bridge open | nFAULT | Half-bridge in operating mode | | |
| Thermal shutdown (TSD) | All interfaces | $T_J$ > $T_{TSD}$ (min 150°C) | nFAULT | Both H-bridges in Hi-Z state | Operating | $T_J$ < $T_{TSD}$ ($T_{HYS}$ typ 40°C) |


Copyright © 2023 Texas Instruments Incorporated

**Table 7-14. Fault Support for DRV8847S**

| FAULT | MODE | CONDITION | REPORT | H-BRIDGE | INTERNAL CIRCUITS | RECOVERY |
|---|---|---|---|---|---|---|
| VM undervoltage (VM_UVLO) | All interfaces | VM < $V_{UVLO}$ | nFAULT | Both H-bridges in Hi-Z state | Shutdown | **Automatic:** VM > $V_{UVLO}$ |
| Overcurrent (OCP) | 4-pin 2-pin | I > $I_{OCP}$ | nFAULT | Corresponding H-bridges in Hi-Z state | Operating | **Automatic:** $t_{RETRY}$ |
| | Parallel bridge | | | Both H-bridges in Hi-Z state | | |
| | Independent bridge Interface | | | Corresponding half-bridges in Hi-Z state | | |
| Open load detect (OLD) | 4-pin | Full-bridge open | nFAULT | H-bridge in operating or Hi-Z state(1) | Operating | **Power cycle / RESET:** OUTx Connected |
| | 2-pin Parallel bridge | Full-bridges open | nFAULT | Both H-bridges in operating or Hi-Z state | | |
| | Independent bridge | Half-bridge open | nFAULT | Half-bridge in operating or Hi-Z state | | |
| Thermal shutdown (TSD) | All interfaces | $T_J$ > $T_{TSD}$ (min 150°C) | nFAULT | Both H-bridges in Hi-Z state | Operating | $T_J$ < $T_{TSD}$ ($T_{HYS}$ typ 40°C) |

(1) The state of the bridge in OLD is dependent on the OLDBO bit as listed in Table 7-19.

Copyright © 2023 Texas Instruments Incorporated

## 7.5 Programming

This section applies only to the DRV8847S device ($I^2C$ variant).

### 7.5.1 $I^2C$ Communication

#### *7.5.1.1 $I^2C$ Write*

To write on the I2C bus, the master device sends a START condition on the bus with the address of the 7-bit slave device. Also, the last bit (the R/W bit) is set to 0b, which signifies a write. After the slave sends the acknowledge bit, the master device then sends the register address of the register to be written. The slave device sends an acknowledge (ACK) signal again which notifies the master device that the slave device is ready. After this process, the master device sends 8-bit write data and terminates the transmission with a STOP condition.

**Figure 7-23. $I^2C$ Write Sequence**

#### *7.5.1.2 $I^2C$ Read*

To read from a slave device, the master device must first communicate to the slave device which register will be read from. This communication is done by the master starting the transmission similarly to the write process which is by setting the address with the R/W bit equal to 0b (signifying a write). The master device then sends the register address of the register to be read from. When the slave device acknowledges this register address, the master device sends a START condition again, followed by the slave address with the R/W bit set to 1b (signifying a read). After this process, the slave device acknowledges the read request and the master device releases the SDA bus, but continues supplying the clock to the slave device.

During this part of the transaction, the master device becomes the master-receiver, and the slave device becomes the slave-transmitter. The master device continues sending out the clock pulses, but releases the SDA line so that the slave device can transmit data. At the end of the byte, the master device send a negative-acknowledge (NACK) signal, signaling to the slave device to stop communications and release the bus. The master device then sends a STOP condition.

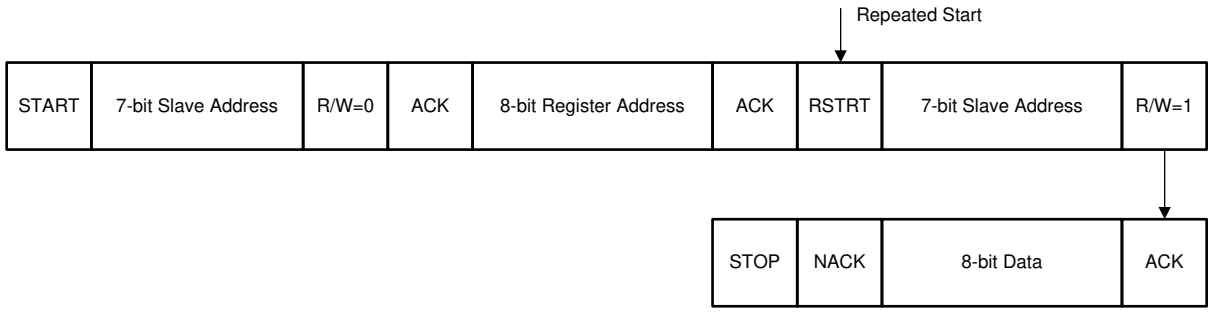



**Figure 7-24. $I^2C$ Read Sequence**


Copyright © 2023 Texas Instruments Incorporated

### 7.5.2 Multi-Slave Operation

Multi-slave operation is used to control multiple DRV8847S devices through one $I^2C$ line as shown in Figure 7-25. The default device address of the DRV8847 device is 0x60 (7-bit address). Therefore, any DRV8847S device can be accessed using this address. The steps for multi-slave configuration for programming device-1 out of 4 connected devices (as shown in Figure 7-25) are as follows:

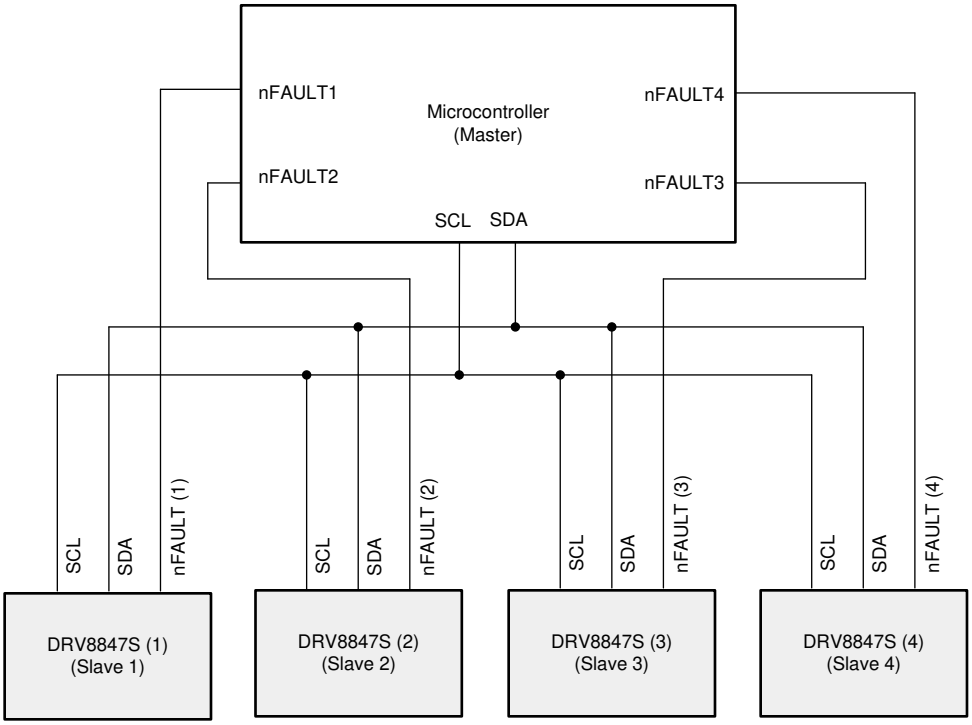



**Figure 7-25. Multi-Slave Operation of DRV8847S**

- The DRV8847S device variant is configured for multi-slave operation by writing the DISFLT bit (IC2_CON register) of all connected devices to 1b. This step will disable the nFAULT output pin of all DRV8847S, to avoid any race condition between master and slave $I^2C$ device.
- Pull the nFAULT pins (nFAULT2, nFAULT3, and nFAULT4 pins) of three devices (2, 3, and 4) to low to release the $I^2C$ buses of the slave device (device-2, device-3 and device-4). Now only device-1 is connected to master.
- Since, only one device, DRV8847S (1), is connected to the controller, and, therefore, its slave address can be reprogrammed from default 0x60 (7-bit address) to another unique address.
- Similarly, the slave address (SLAVE_ADDR) of the other three devices (device-2, device-3 and device-4) can be reprogrammed sequentially to unique addresses by a combination of nFAULT pins.
- When all slave addresses are reprogrammed, write the DISFLT bit to 0b (IC2_CON register). This will enable the nFAULT output pin for fault flagging.
- All the nFAULT pins are released and a multi-slave setup is complete. Now all connected slave devices can be accessed using the newly reprogrammed address.
- The above steps should be repeated for any device in case of a power reset (nSLEEP). .

Copyright © 2023 Texas Instruments Incorporated

## 7.6 Register Map

Table 7-15 lists the memory-mapped I²c registers for the DRV8847 device. The I²C registers are used to configure the DRV8847S device and for device diagnostics.

**Note**

Do not modify reserved registers or addresses not listed in the register map (Table 7-15). Writing to these registers may have unintended effects. For all reserved bits, the default value is 0b.

**Table 7-15. I²C Registers**

| Address | Acronym | Register Name | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Access | Section |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x00 | SLAVE_ADDR | Slave Address | RSVD | SLAVE_ADDR | | | | | | | RW | |
| 0x01 | IC1_CON | IC1 Control | TRQ | IN4 | IN3 | IN2 | IN1 | I2CBC | MODE | | RW | Go |
| 0x02 | IC2_CON | IC2 Control | CLRFLT | DISFLT | RSVD | DECAY | OCPR | OLDOD | OLDFD | OLDBO | RW | Go |
| 0x03 | SLR_STATUS1 | Slew Rate and Fault Status-1 | RSVD | SLR | RSVD | nFAULT | OCP | OLD | TSDF | UVLOF | RW | Go |
| 0x04 | STATUS2 | Fault Status-2 | OLD4 | OLD3 | OLD2 | OLD1 | OCP4 | OCP3 | OCP2 | OCP1 | R | Go |

Complex bit access types are encoded to fit into small table cells. Table 7-16 shows the codes that are used for access types in this section.

**Table 7-16. Access Type Codes**

| Access Type | Code | Description |
|---|---|---|
| Read Type | | |
| R | R | Read |
| Write Type | | |
| W | W | Write |
| Reset or Default Value | | |
| *-n* | | Value after reset or the default value |


Copyright © 2023 Texas Instruments Incorporated

### 7.6.1 Slave Address Register (Address = 0x00) [reset = 0x60]

Slave Address is shown in Figure 7-26 and described in Table 7-17.

**Figure 7-26. Slave Address Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RSVD | SLAVE_ADDR | | | | | | |
| R-0b | R/W-1100000b | | | | | | |

**Table 7-17. Slave Address Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RSVD | R | 0b | Reserved |
| 6-0 | SLAVE_ADDR | R/W | 1100000b | Slave address (8 bit)<br>The default value is 0x60 |

### 7.6.2 IC1 Control Register (Address = 0x01) [reset = 0x00]

IC1 Control is shown in Figure 7-27 and described in Table 7-18.

**Figure 7-27. IC1 Control Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TRQ | IN4 | IN3 | IN2 | IN1 | I2CBC | MODE | |
| R/W-0b | R/W-0b | R/W-0b | R/W-0b | R/W-0b | R/W-0b | R/W-00b | |

**Table 7-18. IC1 Control Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | TRQ | R/W | 0b | 0b = Torque scalar set to 100%<br>1b = Torque scalar set to 50% |
| 6 | IN4 | R/W | 0b | The INx bits are used to control the bridge operation. |
| 5 | IN3 | R/W | 0b | The INx bits are used to control the bridge operation. |
| 4 | IN2 | R/W | 0b | The INx bits are used to control the bridge operation. |
| 3 | IN1 | R/W | 0b | The INx bits are used to control the bridge operation. |
| 2 | I2CBC | R/W | 0b | 0b = Bridge control configured by using the INx pins<br>1b = Bridge control configured by using the INx bits |
| 1-0 | MODE | R/W | 00b | 00b = 4-pin interface<br>01b = 2-pin interface<br>10b = Parallel interface<br>11b = Independent mode |

Copyright © 2023 Texas Instruments Incorporated

### 7.6.3 IC2 Control Register (Address = 0x02) [reset = 0x00]

IC2 Control is shown in Figure 7-28 and described in Table 7-19.

**Figure 7-28. IC2 Control Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CLRFLT | DISFLT | RSVD | DECAY | OCPR | OLDOD | OLDFD | OLDBO |
| R/W-0b | R/W-0b | R-0b | R/W-0b | R/W-0b | R/W-0b | R/W-0b | R/W-0b |

**Table 7-19. IC2 Control Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | CLRFLT | R/W | 0b | Set this bit to issue a clear FAULT command. This command clears all FAULT bits other than the OLD and OLDx bits. This bit reset to 0b after clearing all the faults.<br>0b = No clear FAULT command issued<br>1b = Clear FAULT command issued |
| 6 | DISFLT | R/W | 0b | 0b = nFAULT pin not disable<br>1b = nFAULT pin is disabled |
| 5 | RSVD | R | 0b | Reserved |
| 4 | DECAY | R/W | 0b | 0b = 25% fast decay<br>1b = 100% slow decay |
| 3 | OCPR | R/W | 0b | 0b = OCP auto retry mode<br>1b = OCP latch mode |
| 2 | OLDOD | R/W | 0b | 0b = Idle<br>1b = OLD on-demand is activated |
| 1 | OLDFD | R/W | 0b | 0b = Fault signaling on OLD<br>1b = No fault signaling on OLD |
| 0 | OLDBO | R/W | 0b | 0b = Bridge operating on OLD<br>1b = Bridge Hi-Z on OLD |


Copyright © 2023 Texas Instruments Incorporated

### 7.6.4 Slew-Rate and Fault Status-1 Register (Address = 0x03) [reset = 0x40]

Fault Status-1 is shown in Figure 7-29 and described in Table 7-20.

**Figure 7-29. Fault Status-1 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RSVD | SLR | RSVD | nFAULT | OCP | OLD | TSDF | UVLOF |
| R-0b | R/W-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R-0b |

**Table 7-20. Fault Status-1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RSVD | R | 0b | Reserved |
| 6 | SLR | R/W | 0b | 0b = 150 ns<br>1b = 300 ns |
| 5 | RSVD | R | 0b | Reserved |
| 4 | nFAULT | R | 0b | 0b = No FAULT detected (mirrors the nFAULT pin)<br>1b = FAULT detected |
| 3 | OCP | R | 0b | 0b = No OCP detected<br>1b = OCP detected |
| 2 | OLD | R | 0b | 0b = No open load detected<br>1b = Open load detected |
| 1 | TSDF | R | 0b | 0b = No TSD fault detected<br>1b = TSD fault detected |
| 0 | UVLOF | R | 0b | 0b = No UVLO fault detected<br>1b = UVLO fault detected |

Copyright © 2023 Texas Instruments Incorporated

### 7.6.5 Fault Status-2 Register (Address = 0x04) [reset = 0x00]

Fault Status-2 is shown in Figure 7-30 and described in Table 7-21.

**Figure 7-30. Fault Status-2 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OLD4 | OLD3 | OLD2 | OLD1 | OCP4 | OCP3 | OCP2 | OCP1 |
| R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R-0b |

**Table 7-21. Fault Status-2 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | OLD4 | R | 0b | 0b = No open load detected on OUT4<br>1b = Open load detected on OUT4 |
| 6 | OLD3 | R | 0b | 0b = No open load detected on OUT3<br>1b = Open load detected on OUT3 |
| 5 | OLD2 | R | 0b | 0b = No open load detected on OUT2<br>1b = Open load detected on OUT2 |
| 4 | OLD1 | R | 0b | 0b = No open load detected on OUT1<br>1b = Open load detected on OUT1 |
| 3 | OCP4 | R | 0b | 0b = No OCP detected on OUT4<br>1b = OCP detected on OUT4 |
| 2 | OCP3 | R | 0b | 0b = No OCP detected on OUT3<br>1b = OCP detected on OUT3 |
| 1 | OCP2 | R | 0b | 0b = No OCP detected on OUT2<br>1b = OCP detected on OUT2 |
| 0 | OCP1 | R | 0b | 0b = No OCP detected on OUT1<br>1b = OCP detected on OUT1 |


Copyright © 2023 Texas Instruments Incorporated

# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The DRV8847 device is used in applications for stepper or brushed DC motor control.

## 8.2 Typical Application

The user can configure the DRV8847 for stepper motor and dual BDC motor applications as described in this section.

### 8.2.1 Stepper Motor Application

Figure 8-1 shows the typical application of the DRV8847 device to drive a stepper motor.

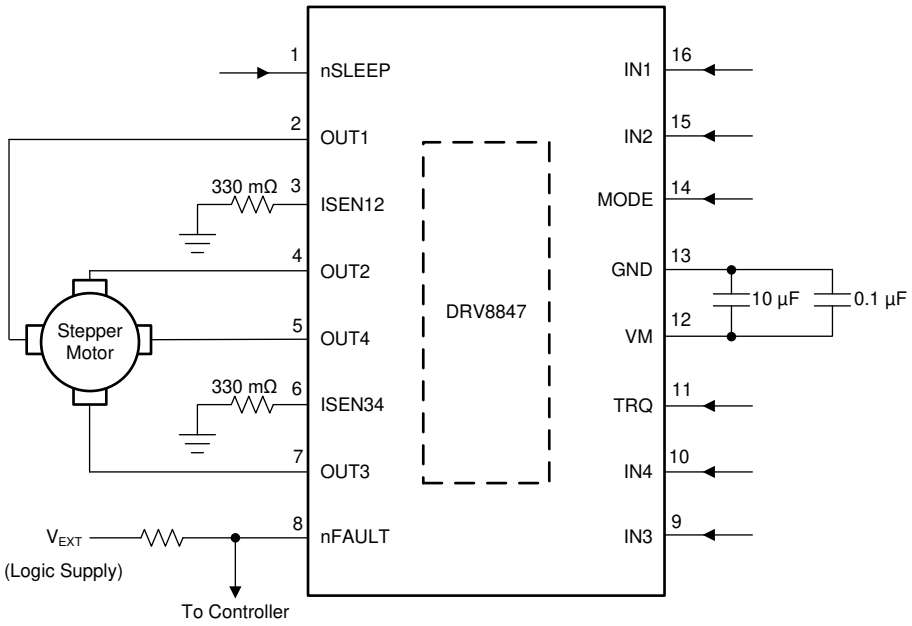



**Figure 8-1. Typical Application Schematic of Device Driving Stepper Motor**

#### *8.2.1.1 Design Requirements*

Table 8-1 lists design input parameters for system design.

**Table 8-1. Design Parameters**

| DESIGN PARAMETER | REFERENCE | EXAMPLE VALUE |
|---|---|---|
| Motor supply voltage | $V_M$ | 12 V |
| Motor winding resistance | $R_L$ | 34 Ω/phase |
| Motor winding inductance | $L_L$ | 33 mH/phase |
| Motor RMS current | $I_{RMS}$ | 350 mA |
| Target trip current | $I_{TRIP}$ | 350 mA |
| Trip current reference voltage (internal voltage) | $V_{TRIP}$ | 150 mV |

Copyright © 2023 Texas Instruments Incorporated

#### 8.2.1.2 Detailed Design Procedure


Copyright © 2023 Texas Instruments Incorporated

#### 8.2.1.2.1 Stepping Modes

The DRV8410 DRV8411 DRV8411A is used to drive a stepper motor in full-stepping mode or non-circulating half-stepping mode using the following bridge configurations:

- Full-stepping mode
- Half-stepping mode with slow decay
- Half-stepping mode with fast decay

##### *8.2.1.2.1.1 Full-Stepping Operation*

In full-stepping mode, the full-bridge operates in either of two modes (forward or reverse mode) with a phase shift of 90° between the two windings. Full stepping is simplest stepper control mode to implement in firmware and offers the best performance at high speeds.

The controller applies the PWM input to the AIN1, AIN2, BIN1, and BIN2 pins as shown in Figure 8-2 and the driver operates only in forward (FRW) and reverse (REV) mode.

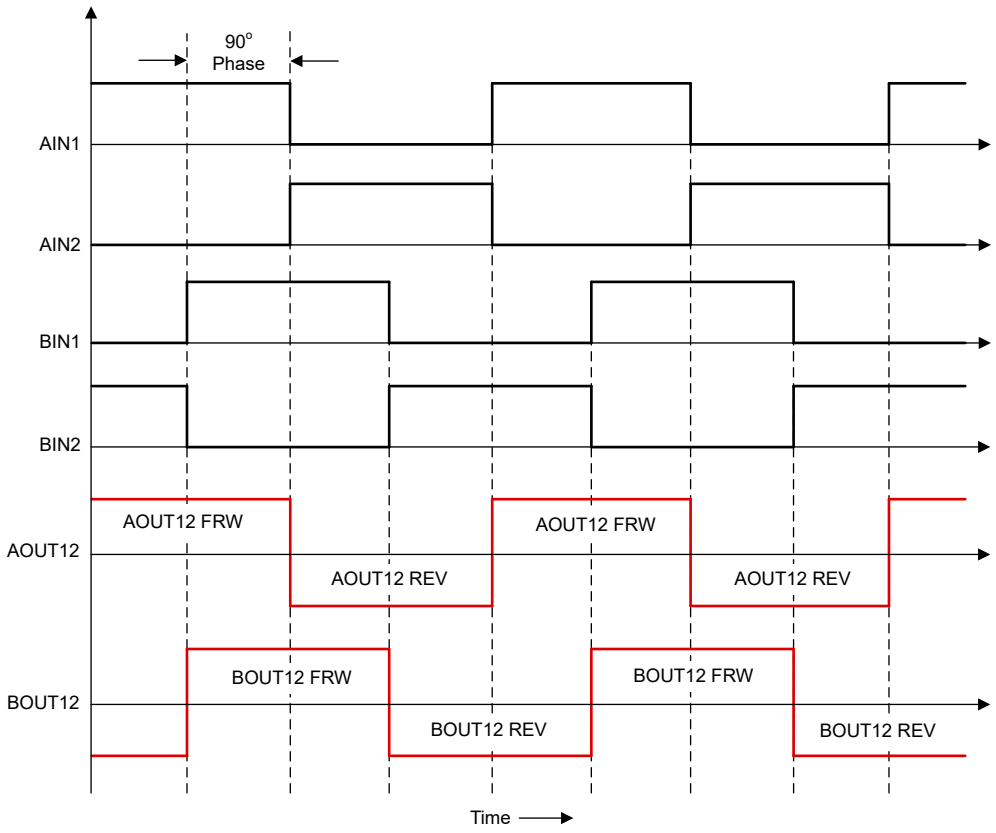



**Figure 8-2. Timing Diagram for Full-Stepping**

#### *8.2.1.2.1.2 Half-Stepping Operation with Fast Decay*

In half-stepping mode, the full-bridge operates in one of the three modes (forward, reverse, or coast mode) to position the rotor half-way between two full-step positions. The coast state allows the current in the motor winding to decay quickly to 0 A. This mode is best-used when half-stepping at high speeds.

The controller applies the PWM input to the AIN1, AIN2, BIN1, and BIN2 pins as shown in Figure 8-3, and the driver operates in forward, reverse, and coast mode.

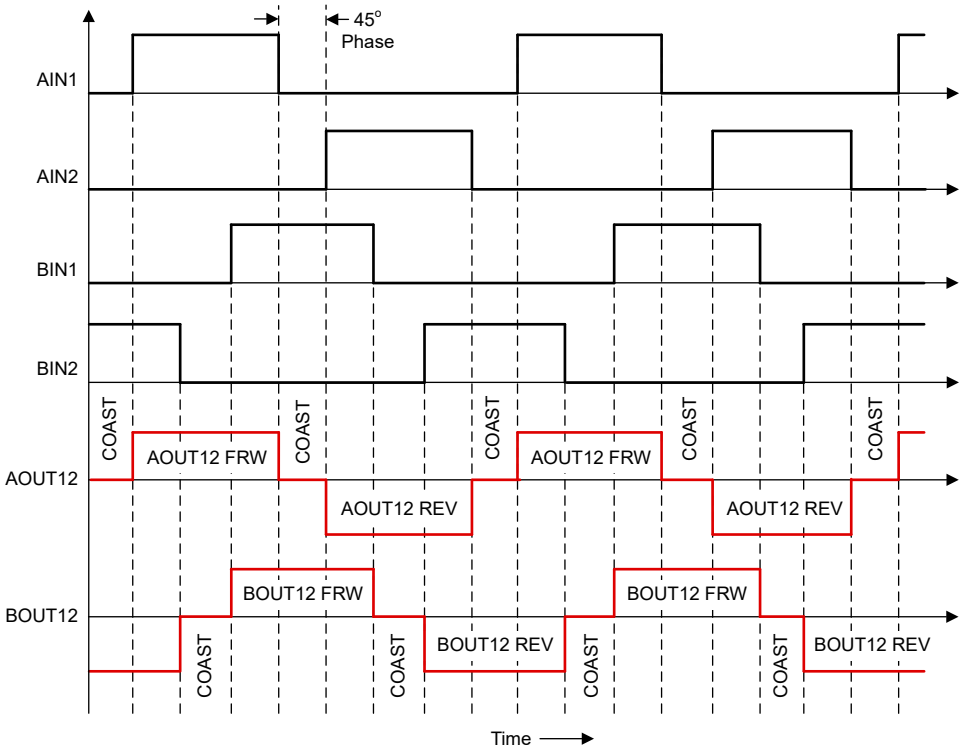



**Figure 8-3. Timing Diagram for Half-Stepping with Fast Decay**


Copyright © 2023 Texas Instruments Incorporated

#### *8.2.1.2.1.3 Half-Stepping Operation with Slow Decay*

In this half-stepping mode, the driver achieves the 0-A state using the slow decay control state (known as "brake mode" for BDC driving). Therefore, the full-bridge operates in one of the three modes (forward, reverse, or brake/slow-decay mode) to position the rotor half-way between two full-step positions. The slow decay state allows the current in the motor winding to decay slowly to 0 A. This mode is best-used when half-stepping at slow speeds and may help to reduce stepper noise and vibration.

The controller applies the PWM input to the AIN1, AIN2, BIN1, and BIN2 pins as shown in Figure 8-4, and the driver operates in forward, reverse, and brake mode.

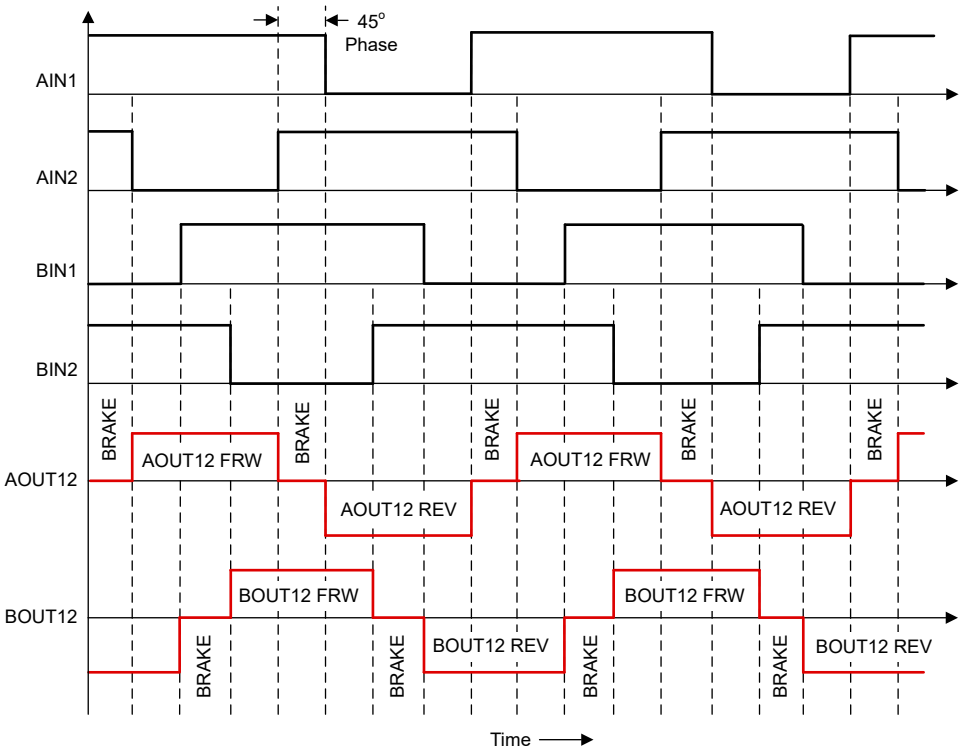



**Figure 8-4. Timing Diagram for Half-Stepping with Slow Decay**

#### 8.2.1.2.2 Current Regulation

The trip current ($I_{TRIP}$) is the maximum current driven through either winding. The amount of this current depends on the sense resistor value ($R_{SENSExx}$) as shown in Equation 4 (Considering torque setting (TRQ) as 100%).

$$I_{TRIP} = \frac{\text{Torque} \times V_{TRIP}}{R_{SENSExx}} \tag{4}$$

The $I_{TRIP}$ current is set by a comparator which compares the voltage across the $R_{SENSExx}$ resistor to a reference voltage. To avoid saturation of the motor, the $I_{TRIP}$ current must be calculated as shown in Equation 5.

$$I_{TRIP} = \frac{V_{VM}}{R_L\ (\Omega) + R_{DS(ON)_HS}\ (\Omega) + R_{DS(ON)_LS}\ (\Omega) + R_{SENSExx}\ (\Omega)} \tag{5}$$

where

- $V_{VM}$ is the motor supply voltage.
- $R_L$ is the motor winding resistance.
- $R_{DS(ON)_HS}$ and $R_{DS(ON)_LS}$ are the high-side and low-side on-state resistance of the FET.

Copyright © 2023 Texas Instruments Incorporated

For an $I_{TRIP}$ value of 350 mA, the value of the sense resistor ($R_{SENSExx}$) is calculated as shown in Equation 6.

$$R_{SENSE12} = R_{SENSE34} = \frac{V_{TRIP}}{I_{TRIP}} = \frac{150\ mV}{350\ mA} = 428.6\ m\Omega \quad (6)$$

Select the closest available value of 440 mΩ for the sense resistors. Selecting this value will effect the current accuracy by 2.8%.


Copyright © 2023 Texas Instruments Incorporated

### 8.2.1.3 Application Curves

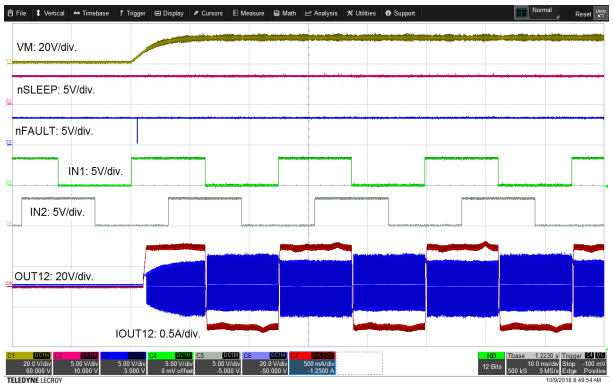



**Figure 8-5. Device Power-up with Supply Voltage (VM)**

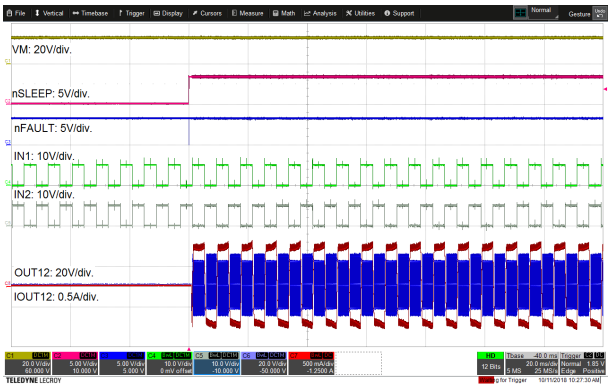



**Figure 8-6. Device Power-up with nSLEEP**

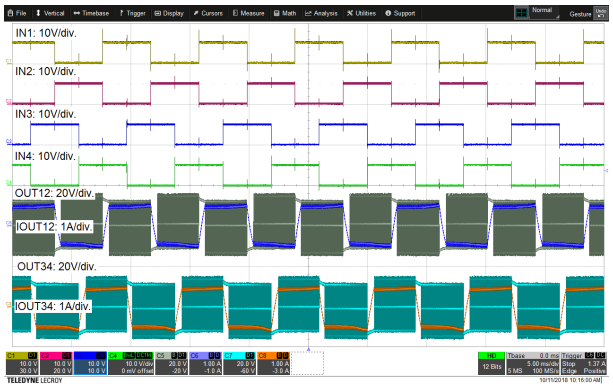



**Figure 8-7. Stepper Motor Full-Step Operation**

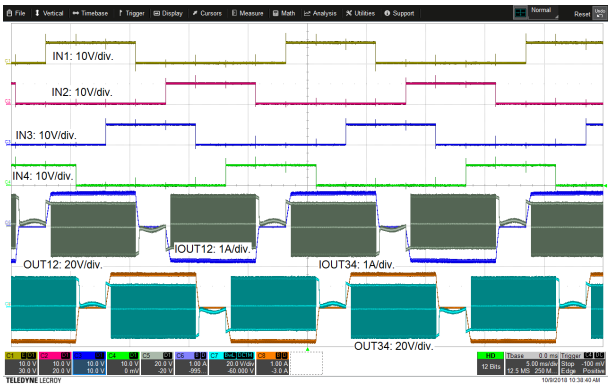



**Figure 8-8. Stepper Motor Half-Step Operation With Off-State as Hi-Z**

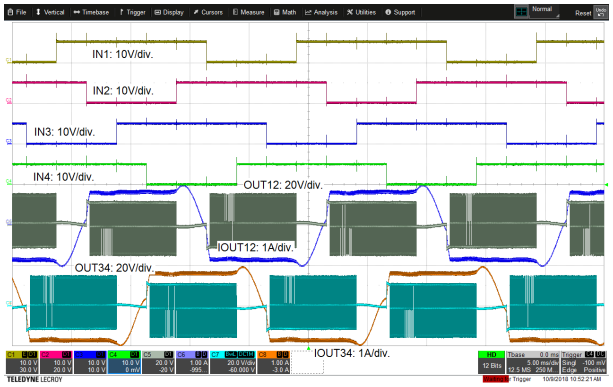



**Figure 8-9. Stepper Motor Half-Step Operation With Off-State as Brake**

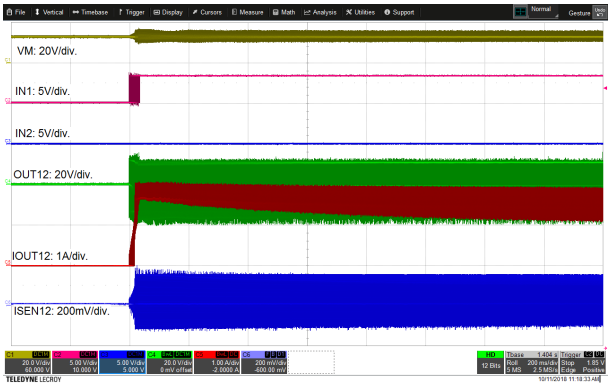



**Figure 8-10. Brushed DC Motor Operation in Parallel Mode Showing Current Regulation at 2-A**

Copyright © 2023 Texas Instruments Incorporated

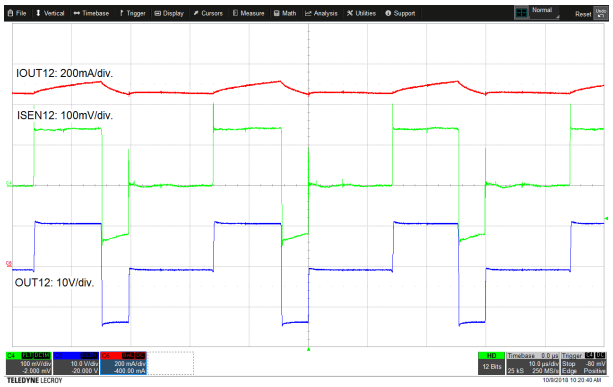



**Figure 8-11. Zoomed Waveform Showing Current Regulation**

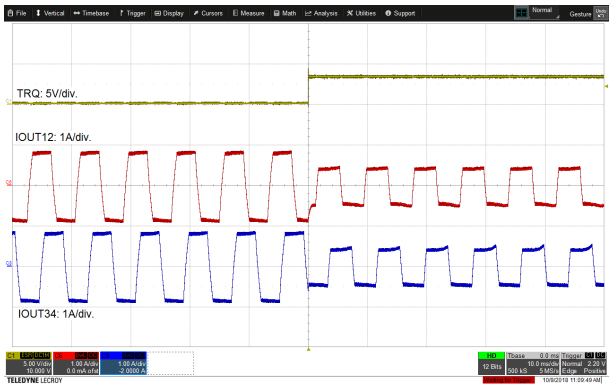



**Figure 8-12. Torque Pin Functionality for Current Scaling**

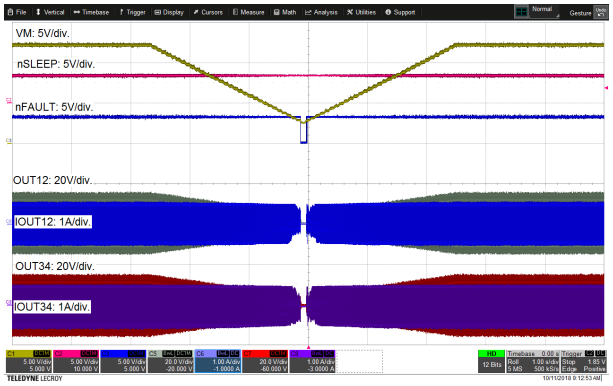



**Figure 8-13. Undervoltage Lockout Operation**

**Figure 8-14. Open Load Detect Operation**

**Figure 8-15. Over Current Protection and Recovery**

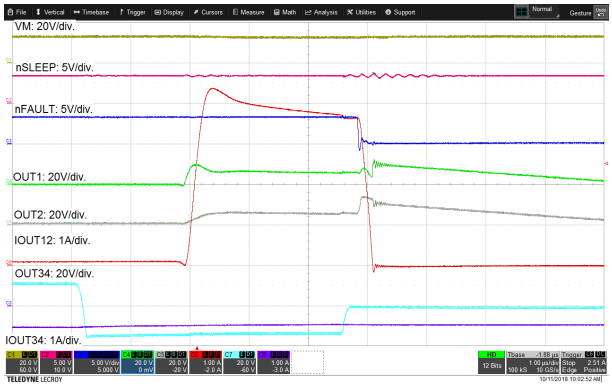



**Figure 8-16. Zoomed Waveform of Over Current Protection**


Copyright © 2023 Texas Instruments Incorporated

### 8.2.2 Dual BDC Motor Application

Figure 8-17 shows the typical application of DRV8847 device to drive dual BDC motors.

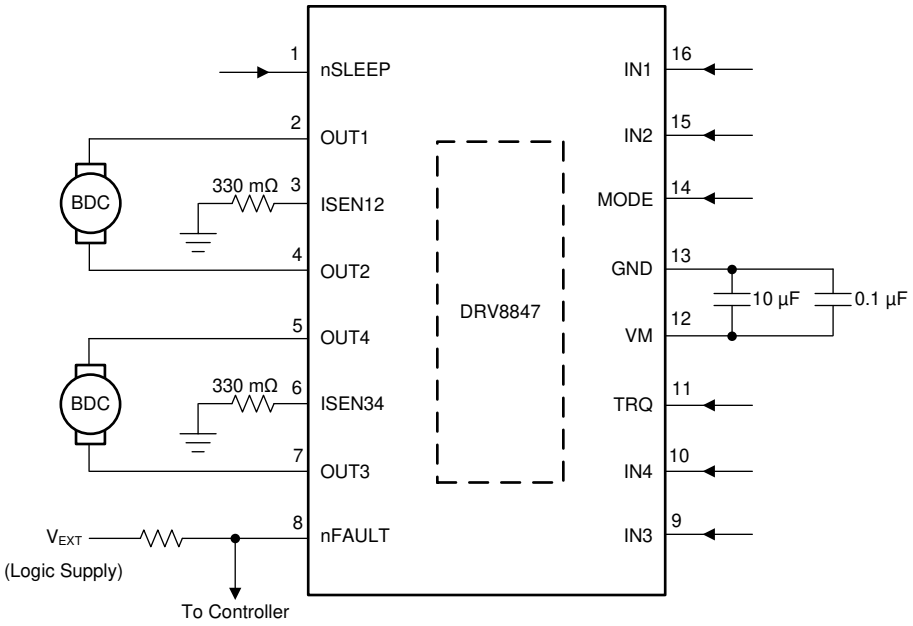



**Figure 8-17. Typical Application Schematic of Device Driving Two BDC Motors**

#### *8.2.2.1 Design Requirements*

Table 8-2 lists the design input parameters for system design.

**Table 8-2. Design Parameters**

| DESIGN PARAMETER | REFERENCE | EXAMPLE VALUE |
|---|---|---|
| Motor supply voltage | $V_M$ | 12 V |
| Motor winding resistance | $R_L$ | 13.2 Ω |
| Motor winding inductance | $L_L$ | 500 µH |
| Motor RMS current | $I_{RMS}$ | 490 mA |
| Motor start-up current | $I_{START}$ | 900 mA |
| Target trip current | $I_{TRIP}$ | 1.2 A |
| Trip current reference voltage (internal voltage) | $V_{TRIP}$ | 150 mV |

#### *8.2.2.2 Detailed Design Procedure*

##### 8.2.2.2.1 Motor Voltage

The motor voltage used in an application depends on the rating of the selected motor and the desired revolutions per minute (RPM). A higher voltage spins a brushed DC motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

##### 8.2.2.2.2 Current Regulation

The trip current ($I_{TRIP}$) is the maximum current driven through either winding. Because the peak current (start current) of the motor is 900 mA, the $I_{TRIP}$ current level is selected to be just greater than the peak current. The selected $I_{TRIP}$ value for this example is 1.2 A. Therefore, use Equation 7 to select the value of the sense resistors ($R_{SENSE12}$ and $R_{SENSE34}$) connected to the ISEN12 and ISEN34 pins.

Copyright © 2023 Texas Instruments Incorporated

$$R_{SENSE12} = R_{SENSE34} = \frac{V_{TRIP}}{I_{TRIP}} = \frac{150\ mV}{1.2\ A} = 125\ m\Omega \quad (7)$$

#### 8.2.2.2.3 Sense Resistor

For optimal performance, the sense resistor must:

- Be a surface mount component
- Have low inductance
- Be rated for high enough power
- Be placed closely to the motor driver

The power dissipated by the sense resistor equals $I_{RMS}{}^2 \times R$. In this example, the peak current is 900 mA, the RMS motor current is 490 mA, and the sense resistor value is 125 mΩ. Therefore, the sense resistors ($R_{SENSE12}$ and $R_{SENSE34}$) dissipate 30 mW (490 $mA^2$ × 125 mΩ = 30 mW). The power quickly increases with higher current levels.

Resistors typically have a rated power within some ambient temperature range, along with a derated power curve for high ambient temperatures. When a printed circuit board (PCB) is shared with other components generating heat, margin should be added. For best practice, measure the actual sense resistor temperature in a final system, along with the power MOSFETs, because those components are often the hottest.

Because power resistors are larger and more expensive than standard resistors, the common practice is to use multiple standard resistors in parallel, between the sense node and ground. This practice distributes the current and heat dissipation.

### 8.2.3 Open Load Implementation

This section presents the open load detection circuit and the operation. The open load detection diagnostic test runs during the device power up or when the DRV8847 device comes out from sleep mode. In the $I^2C$ variant device (DRV8847S), the OLD diagnostic test can run any instant of time using the $I^2C$ register bits.

#### *8.2.3.1 Open Load Detection Circuit*

OLD circuit consists of four main components i.e. current source (and current sink), series sequencing switches (sequenced by the digital core), resistors and comparators. For ground (GND) connected load, the current source ($I_{OL_PU}$) pulls up the OUTx node to internal regulator voltage (AVDD) and allows the current to flow from internal regulator voltage (AVDD) to ground via the connected load as shown in Figure 8-18. Moreover, for the supply (VM) connected load, the current sink ($I_{OL_PD}$) pulls down the current from supply voltage (VM) to ground via the connected load as shown in Figure 8-20. The resistance of the load connected at the OUTx terminal will change the source / sink current and indirectly the voltage drop across two resistors (12-kΩ and 15-kΩ). This voltage drop across resistors is compared with the reference voltage ($V_{OL_HS}$ and $V_{OL_LS}$) by the internal comparators to give the output as OL1_HS and OL1_LS. This comparator output is fed to the open load digital circuit to determine the open load condition.

**Note**

Following are the values of various parameter shown above: AVDD voltage = 4.2-V, $I_{OL_PU}$ = 200-µA, $I_{OL_PD}$ = 230-µA, $V_{OL_HS}$ = 2.3-V, $V_{OL_LS}$ = 1.2-V.

Note that the values taken above are at the typical condition of supply voltage and temperature. Refer to "Typical Characteristics" section in Section 6 for detailed specifications.

#### *8.2.3.2 OLD for Ground Connected Load*

Figure 8-18 shows the ground connected load with internal OLD circuit. When high-side open load sequence is activated (i.e. SW1_HS is on and SW1_LS is off), the current source ($I_{OL_PU}$) pulls up the OUT1 node to internal regulator voltage (AVDD) and current flows from internal regulator voltage (AVDD) to ground via the connected load ($R_L$). Now, depending upon if the load is present or not, there can be three cases as follows:


Copyright © 2023 Texas Instruments Incorporated

#### 8.2.3.2.1 Half Bridge Open

If no-load is connected at the OUT1, then no current flows from AVDD. This pulls up the positive terminal of OL1_HS comparator to 4.2-V (AVDD). This if compared with 2.3-V ($V_{OL_HS}$) sets the comparator output to "1", which signifies an open load detect.

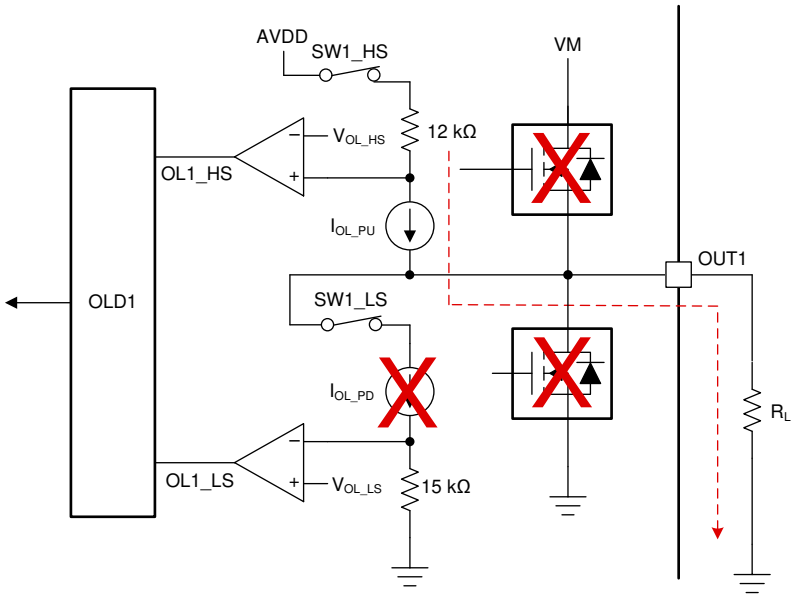



**Figure 8-18. Open Load Detect Circuit for Load Connected to Ground (GND)**

#### 8.2.3.2.2 Half Bridge Short

If OUT1 pin is shorted to ground, then pull-up current of 200-µA ($I_{OL_PU}$) flows from AVDD. Due to this, there is a voltage drop at the positive terminal of OL1_HS comparator as:

$$V_{OL1_HS}(+) = V_{AVDD} - I_{OL_PU} \times 12k\Omega \tag{8}$$

Using Equation 8, the $V_{OL1_HS}$(+) is calculated as shown in Equation 9,

$$V_{OL1_HS}(+) = 4.2V - 200\mu A \times 12k\Omega = 1.8V \tag{9}$$

This voltage, if compared with 2.3-V ($V_{OL_HS}$) reset the OL1_HS comparator output to "0", which signifies a no open load detect.

#### 8.2.3.2.3 Load Connected

If a resistive load ($R_L$) is connected between OUT1 and GND, then current flowing from AVDD depends on load reistance ($R_L$) as:

$$I_{LOAD} = \frac{V_{AVDD}}{R_L + 12k\Omega} \tag{10}$$

Now, if the voltage drop at positive terminal of OL1_HS comparator is higher than 2.3-V ($V_{OL_HS}$), the comparator sets output to "1" showing as open load. Hence, the voltage required to trip the OL1_HS comparator is calculated as:

$$V_{OL_HS} < V_{AVDD} - I_{LOAD} \times 12k\Omega \tag{11}$$

Copyright © 2023 Texas Instruments Incorporated

By putting Equation 10 to Equation 11,

$$V_{OL_HS} < V_{AVDD} - \frac{V_{AVDD} \times 12k\Omega}{R_L + 12k\Omega} \tag{12}$$

By solving Equation 12, the load resistance ($R_L$) is expressed as,

$$R_L > \frac{V_{AVDD} \times 12k\Omega}{V_{AVDD} - V_{OL_HS}} - 12k\Omega \tag{13}$$

By putting the values of $V_{AVDD}$ and $V_{OL_HS}$ in Equation 13, the load resistance ($R_L$) is calculated as 14.52-kΩ. Hence, any resisitive load connected between OUTx and GND above this value is shown as an open-load.

**Note**

The values of these parameters are taken for a typical case for understanding. These parameters changes with supply voltage and temperature. User has to consider a design margin based on the above calculations.

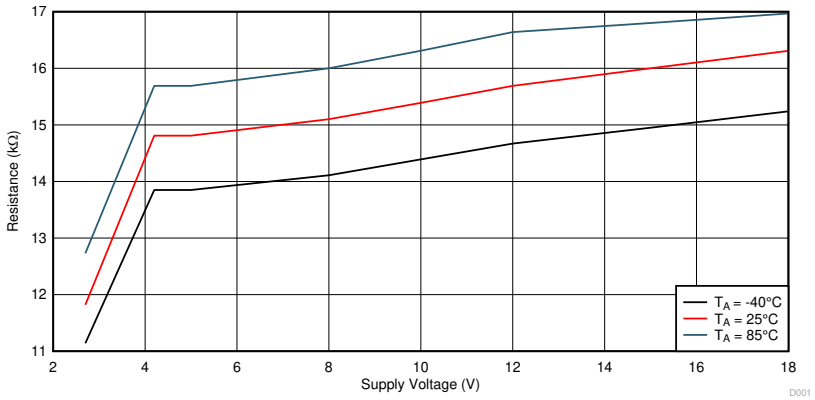



**Figure 8-19. Resistance Threshold's for Open Load Detect in Ground (GND) Connected Load**

### *8.2.3.3 OLD for Supply (VM) Connected Load*

Figure 8-20 shows the supply (VM) connected load with internal OLD circuit. When low-side open load sequence is activated (i.e. SW1_HS is off and SW1_LS is on), the current sink ($I_{OL_PD}$) pulls down the OUT1 node to supply voltage ($V_{VM}$) and current flows from supply (VM) to ground via the connected load ($R_L$). Now, depending upon if the load is present or not, there can be three cases as follows:


Copyright © 2023 Texas Instruments Incorporated

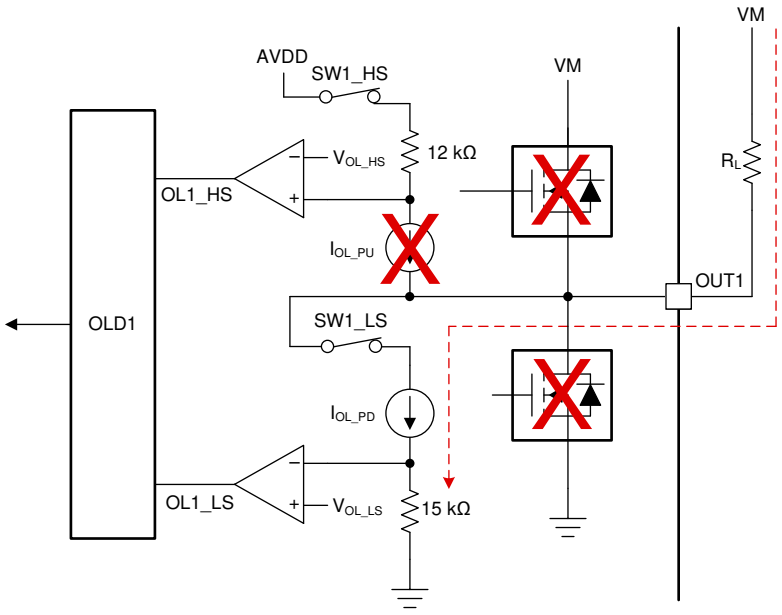



**Figure 8-20. Open Load Detect Circuit for Load Connected to Supply Voltage (VM)**

#### 8.2.3.3.1 Half Bridge Open

If no-load is connected at the OUT1, then no current flows from supply (VM). This pulls down the negative terminal of OL1_LS comparator to 0-V (GND). This if compared with 1.2-V ($V_{OL_LS}$) sets the comparator output to "1", which signifies an open load detect.

#### 8.2.3.3.2 Half Bridge Short

If OUT1 pin is shorted to supply (VM), then pull-down current of 230-µA ($I_{OL_LS}$) flows from supply (VM). Due to this, there is a voltage drop at the negative terminal of OL1_LS comparator as:

$$V_{OL1_LS}(-) = I_{OL_PD} \times 15k\Omega \tag{14}$$

Using Equation 14, the $V_{OL1_LS}$(-) is calculated as shown in Equation 15,

$$V_{OL1_LS}(-) = 230\mu A \times 15k\Omega = 3.45V \tag{15}$$

This voltage, if compared with 1.2-V ($V_{OL_LS}$) reset the OL1_LS comparator output to "0", signifying a no open load detect.

#### 8.2.3.3.3 Load Connected

If a resistive load ($R_L$) is connected between OUT1 and VM, then current flowing from supply (VM) is as:

$$I_{LOAD} = \frac{V_{VM}}{R_L + 15k\Omega} \tag{16}$$

Now, if the voltage drop at negative terminal of OL1_LS comparator is lower than 1.2-V ($V_{OL_LS}$), the comparator sets output to "1" showing open load. Hence, the voltage required to trip OL1_LS comparator is calculated as:

$$V_{OL_LS} > I_{LOAD} \times 15k\Omega \tag{17}$$

By putting Equation 16 to Equation 17,

Copyright © 2023 Texas Instruments Incorporated

$$V_{OL_LS} > \frac{V_{VM} \times 15k\Omega}{R_L + 15k\Omega} \quad (18)$$

By solving Equation 18, the load resistance ($R_L$) is expressed as,

$$R_L > \frac{V_{VM} \times 15k\Omega}{V_{OL_LS}} - 15k\Omega \quad (19)$$

By putting the values of $V_{VM}$ and $V_{OL_HS}$ in Equation 19, the load resistance ($R_L$) is calculated as 135-kΩ for supply voltage ($V_{VM}$) of 12-V. Hence, any resistive load connected between VM and OUTx above this value (at $V_{VM}$ = 12-V) is shown as an open-load.

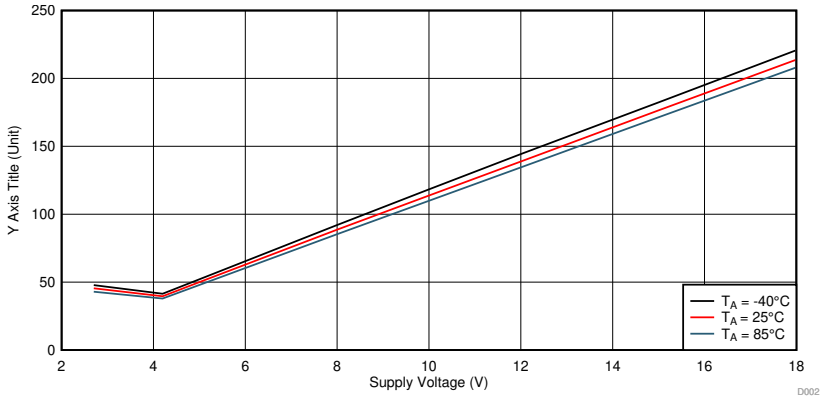



**Figure 8-21. Resistance Threshold's for Open Load Detect in Supply (VM) Connected Load**

**Note**

In the open load detection for load connected to supply (VM) configuration, the resistive load threshold for an open load also depends on the supply voltage ($V_{VM}$).

#### *8.2.3.4 OLD for Full Bridge Connected Load*

Figure 8-22 shows the load connected as a full bridge configuration with internal OLD circuit. Full-bridge open load sequence consists of turning-on the high-side switch (SW1_HS) of half-bridge-1 and low-side switch (SW2_LS) of half-bridge-2 together. In a similar manner, the full-bridge open-load sequence for the other half bridge with turning-on the high-side switch (SW2_HS) of half-bridge-2 and low-side switch (SW1_LS) of half-bridge-1 together is executed. Now, depending on the load presence, three cases are considered:

##### 8.2.3.4.1 Full Bridge Open

If no-load is connected between the OUT1 and OUT2 terminals, then no current flows from internal regulator (AVDD). Now, the voltage-drop at the positive terminal of high side comparator of half-bridge-1 (OL1_HS) and the negative terminal of low side comparator of half-bridge-2 (OL2_LS) will be as follows:

###### *8.2.3.4.1.1 High side comparator of half-bridge-1 (OL1_HS)*

Since no current is flowing from the internal regulator (AVDD), the voltage at the OUT1 node (which is also the positive terminal of OL1_HS comparator) is clamped to 4.2-V (i.e. AVDD). This if compared with 2.3-V ($V_{OL_HS}$) sets the comparator output to "1".

###### *8.2.3.4.1.2 Low side comparator of half-bridge-2 (OL2_LS)*

For an open load condition, no current flows through the SW2_LS switch, which pulls down the negative terminal of OL2_LS comparator to 0-V (GND). This if compared with 1.2-V ($V_{OL_LS}$) sets the comparator output to "1".


Copyright © 2023 Texas Instruments Incorporated

Now, if both the comparator outputs (OL1_HS and OL2_LS) is high, it signifies an open load.

#### 8.2.3.4.2 Full Bridge Short

If there is short between the OUT1 and OUT2 terminals, then a short current ($I_{SC}$) will flows from internal regulator (AVDD) depending upon the high-side (12-kΩ) and low-side (15-kΩ) resistors as,

$$I_{SC} = \frac{V_{AVDD}}{15k\Omega + 12k\Omega} = \frac{V_{AVDD}}{27k\Omega} \tag{20}$$

Hence the short-current flowing using Equation 20 is calculated as,

$$I_{SC} = \frac{V_{AVDD}}{27k\Omega} = \frac{4.2V}{27k\Omega} = 155.56\mu A \tag{21}$$

Now, the voltage-drop at the positive terminal of high side comparator of half-bridge-1 (OL1_HS) and the negative terminal of low side comparator of half-bridge-2 (OL2_LS) will be as follows:

##### *8.2.3.4.2.1 High side comparator of half-bridge-1 (OL1_HS)*

Now, the pull up current of $I_{SC}$ (155.56-µA) is flowing from the internal regulator (AVDD), therefore the voltage at the positive terminal of OL1_HS comparator (which is also the OUT1 node) is calculated as,

$$V_{OL1_HS}(+) = V_{AVDD} - I_{SC} \times 12k\Omega \tag{22}$$

using Equation 22, the $V_{OL1_HS}$(+) is calculated as,

$$V_{OL1_HS}(+) = 4.2V - 155.56\mu A \times 12k\Omega = 2.33V \tag{23}$$

This voltage, if compared with 2.3-V ($V_{OL_HS}$) sets the OL1_HS comparator output to "1".

##### *8.2.3.4.2.2 Low side comparator of half-bridge-2 (OL2_LS)*

The pull down current of $I_{SC}$ (155.56-µA) is flowing from the internal regulator (AVDD) to the SW2_LS switch, therefore the voltage at the negative terminal of OL2_LS comparator is calculated as,

$$V_{OL2_LS}(-) > I_{SC} \times 15k\Omega \tag{24}$$

Using Equation 24, the $V_{OL2_LS}$ is calculated as,

$$V_{OL2_LS}(-) = 155.56\mu A \times 15k\Omega = 2.33V \tag{25}$$

This voltage, if compared with 1.2-V ($V_{OL_LS}$) reset the OL2_LS comparator output to "0".

Since, OL1_HS comparator shows an output "1" and OL2_LS comparator shows and output "0", therefore this case is considered as no-open load.

Copyright © 2023 Texas Instruments Incorporated

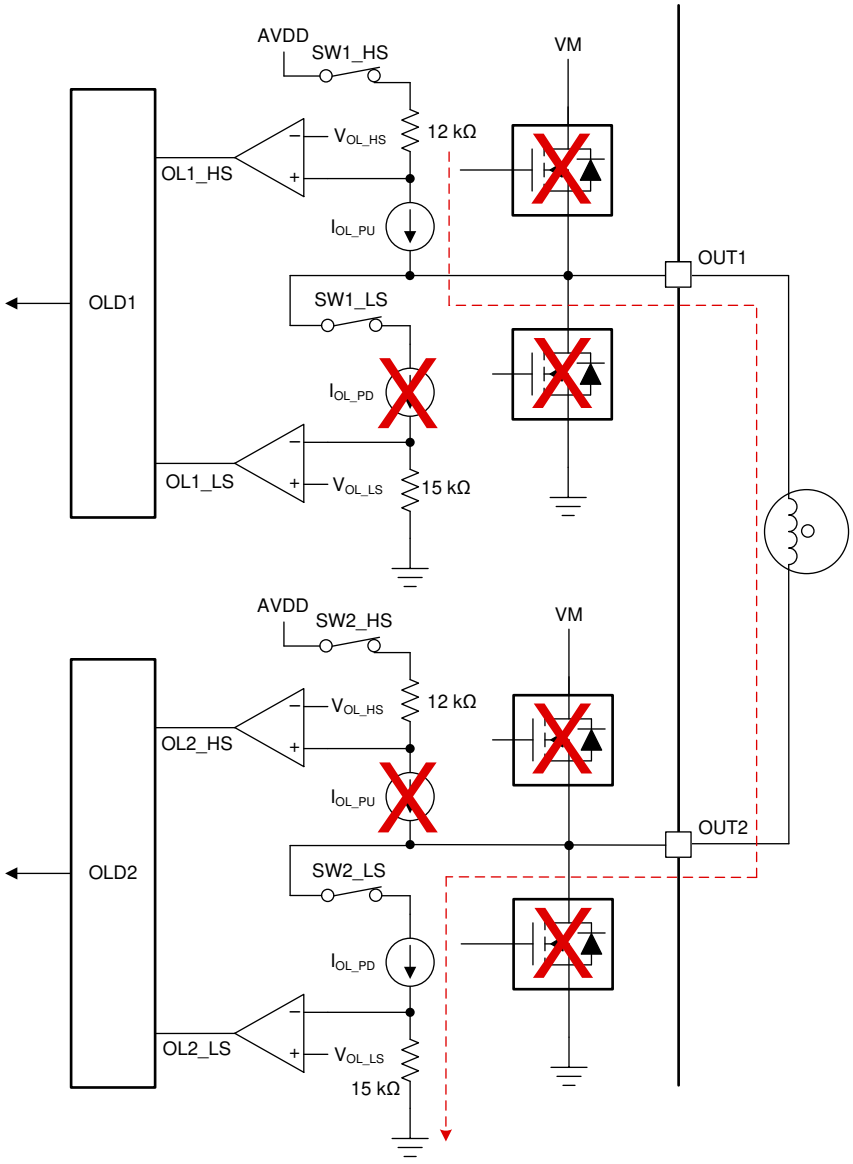



**Figure 8-22. Open Load Detect Circuit for Motor Connected in Full Bridge Configuration**

#### 8.2.3.4.3 Load Connected in Full Bridge

If there is a load ($R_L$) connected between the OUT1 and OUT2 terminals, then a load current ($I_L$) is calculated as,

$$I_{LOAD} = \frac{V_{AVDD}}{12k\Omega + R_L + 15k\Omega} = \frac{V_{AVDD}}{R_L + 27k\Omega} \quad (26)$$

Now, the voltage-drop at the positive terminal of high side comparator of half-bridge-1 (OL1_HS) and the negative terminal of low side comparator of half-bridge-2 (OL2_LS) will be as follows:

##### *8.2.3.4.3.1 High side comparator of half-bridge-1 (OL1_HS)*

If the voltage drop at positive terminal of OL1_HS comparator is higher than 2.3-V ($V_{OL_HS}$), the comparator sets output to "1" (for open load). Hence, the voltage required to trip the OL1_HS comparator is calculated as:


Copyright © 2023 Texas Instruments Incorporated

$$V_{OL_HS} < V_{AVDD} - I_{LOAD} \times 12k\Omega \quad (27)$$

By putting Equation 26 into Equation 27,

$$V_{OL_{HS}} < V_{AVDD} - \frac{V_{AVDD} \times 12k\Omega}{R_L + 27k\Omega} \quad (28)$$

By solving Equation 28, the load resistance ($R_L$) is expressed as,

$$R_L > \frac{V_{AVDD} \times 12k\Omega}{V_{AVDD} - V_{OL_HS}} - 27k\Omega \quad (29)$$

By putting the values of $V_{AVDD}$ and $V_{OL_HS}$ in Equation 29, the load resistance ($R_L$) is calculated as (-)10.2-kΩ. Since, the value of resistance is negative, therefore, the voltage at positive terminal of OL1_HS comparator is always higher than $V_{OL_HS}$ and comparator output is always high ("1").

#### *8.2.3.4.3.2 Low side comparator of half-bridge-2 (OL2_LS)*

If the voltage drop at negative terminal of OL2_LS comparator is lower than 1.2-V ($V_{OL_LS}$), the comparator sets output to "1" showing as open load. Hence, the voltage required to trip the OL2_LS comparator is calculated as:

$$V_{OL_LS} > I_{LOAD} \times 15k\Omega \quad (30)$$

By putting Equation 26 to Equation 30,

$$V_{OL_LS} > \frac{V_{AVDD} \times 15k\Omega}{R_L + 27k\Omega} \quad (31)$$

By solving Equation 31, the load resistance ($R_L$) is expressed as,

$$R_L > \frac{V_{AVDD} \times 15k\Omega}{V_{OL_LS}} - 27k\Omega \quad (32)$$

By putting the values of $V_{AVDD}$ and $V_{OL_LS}$ in Equation 32, the load resistance ($R_L$) is calculated as 25.5-kΩ. Therefore, the output of OL2_HS comparator sets to 1, if the load resistance is greater than 25.5-kΩ.

Since, the OL1_HS comparator always outputs "1", therefore, the open load status is solely dependent on the output of OL2_HS comparator. If OL2_HS comparator output is "1", then an open load is detected.

Copyright © 2023 Texas Instruments Incorporated

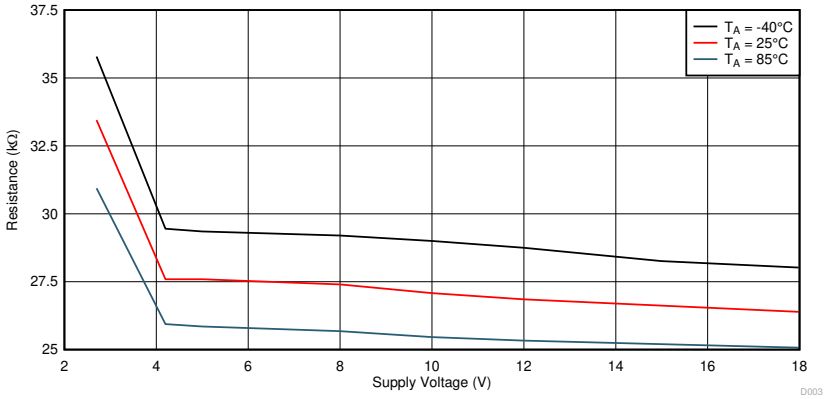



**Figure 8-23. Resistance Threshold's for Open Load Detect for Load Connected in Full-Bridge Configuration**


Copyright © 2023 Texas Instruments Incorporated

## Power Supply Recommendations

The DRV8847 device is designed to operate from an input voltage supply ($V_{VM}$) range from 2.7 V to 18 V. Place a 0.1-µF ceramic capacitor rated for VM as close to the DRV8847 device as possible. In addition, a bulk capacitor with a value of at least 10 µF must be included on the VM pin.

### 9.1 Bulk Capacitance Sizing

Bulk capacitance sizing is an important factor in motor drive system design. The amount of bulk capacitance depends on a variety of factors including:

- Type of power supply
- Acceptable supply voltage ripple
- Parasitic inductance in the power supply wiring
- Type of motor (brushed DC, brushless DC, stepper)
- Motor start-up current
- Motor braking method

The inductance between the power supply and motor drive system limits the rate that current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. Size the bulk capacitance to meet acceptable voltage ripple levels.

The data sheet provides a recommended minimum value, but system-level testing is required to determine the appropriate-sized bulk capacitor.

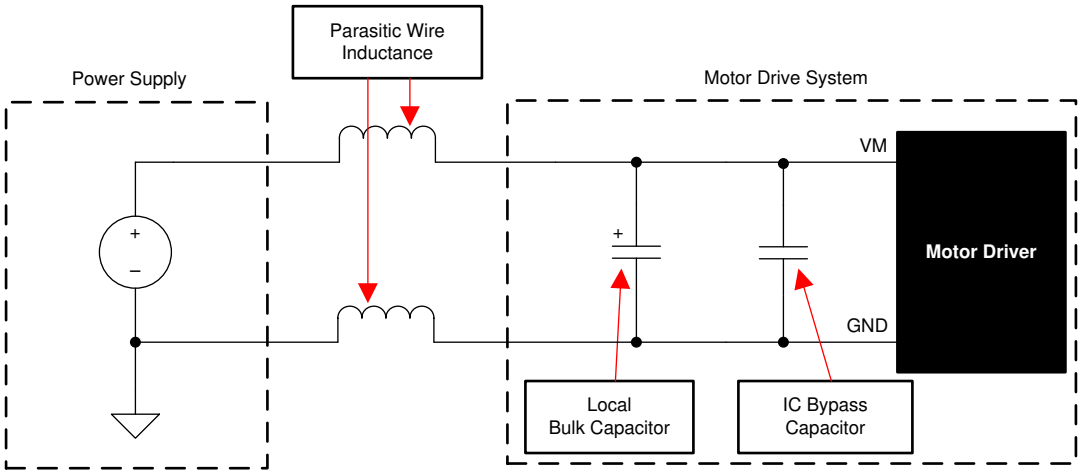



**Figure 9-1. Setup of Motor Drive System With External Power Supply**

Copyright © 2023 Texas Instruments Incorporated

# 9 Layout

## 9.1 Layout Guidelines

Bypass the VM pin to ground using a low-ESR ceramic bypass capacitor with a recommended value of 10 µF and rated for VM. Place this capacitor as close to the VM pin as possible with a thick trace or ground plane connection to the device GND pin.

## 9.2 Layout Example

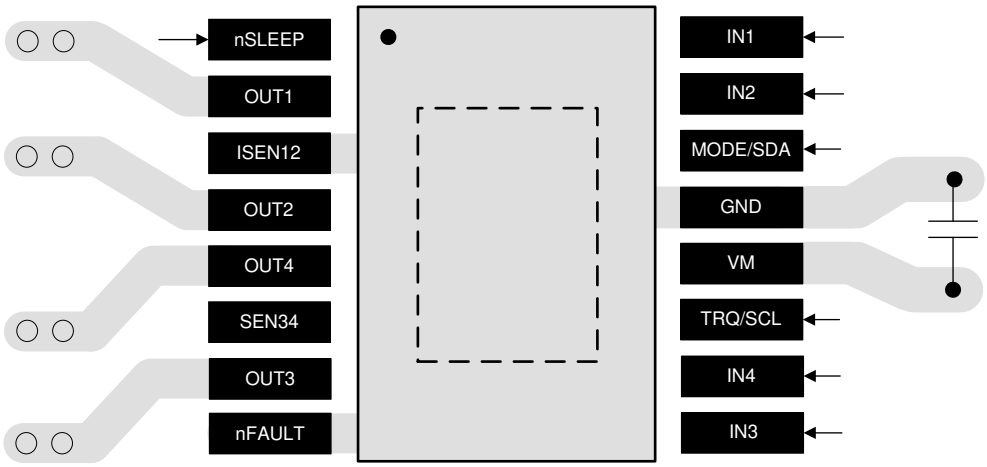



**Figure 9-1. Layout Recommendation of 16-Pin TSSOP Package for Single-Layer Board**

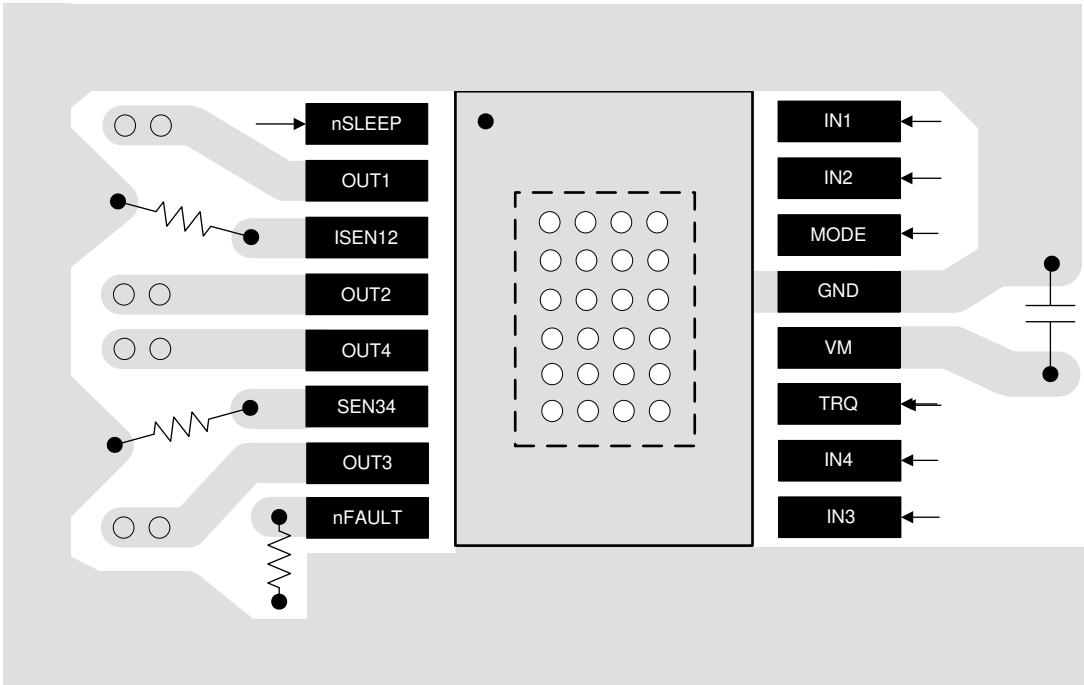



**Figure 9-2. Layout Recommendation of 16-Pin HTSSOP Package for Double-Layer Board**


Copyright © 2023 Texas Instruments Incorporated

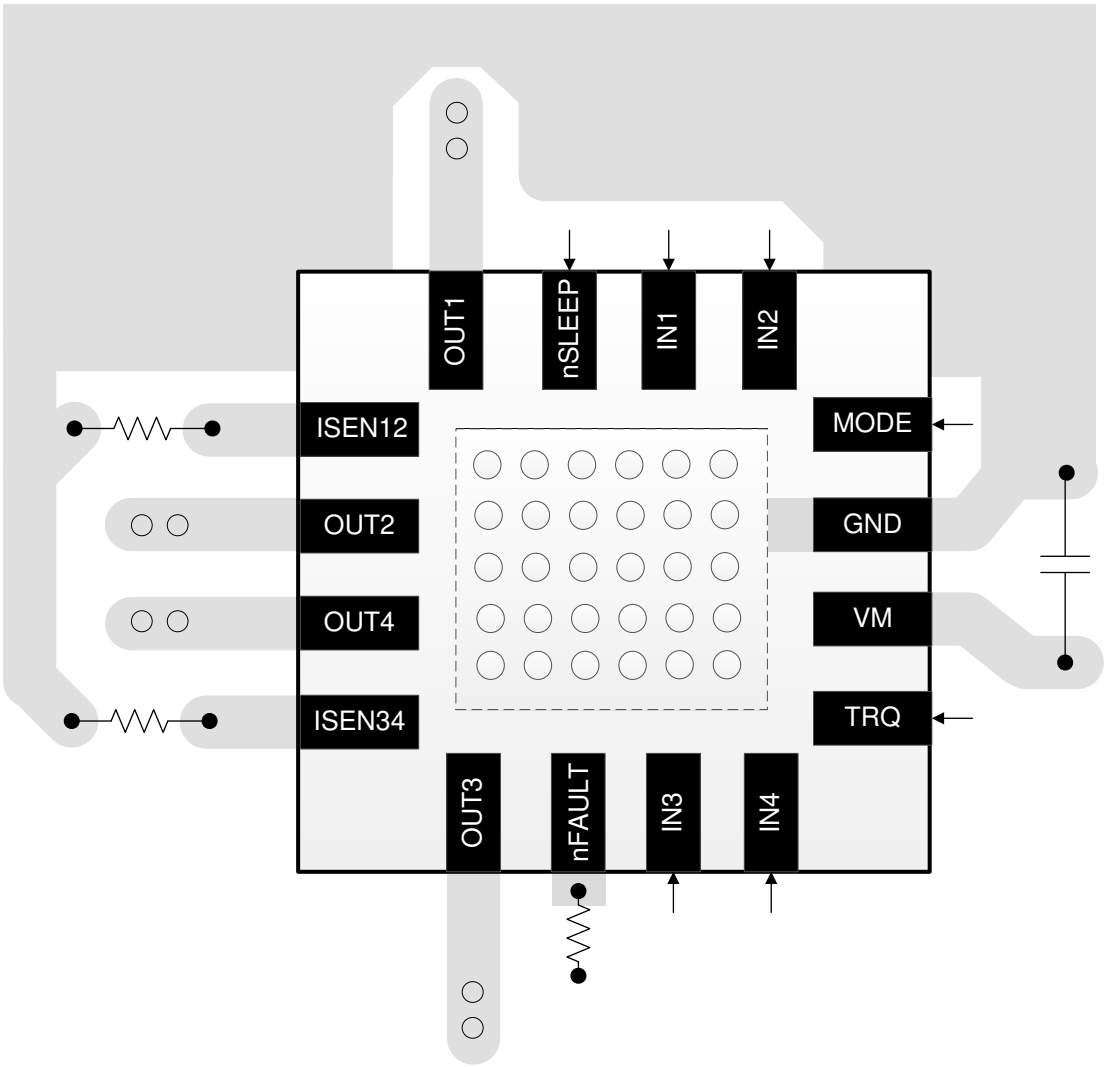



**Figure 9-3. Layout Recommendation of 16-Pin QFN Package for Double-Layer Board**

Copyright © 2023 Texas Instruments Incorporated

## 9.3 Thermal Considerations

### 9.3.1 Maximum Output Current

In actual operation, the maximum output current that is achievable with a motor driver is a function of the die temperature. This die temperature is greatly affected by ambient temperature and PCB design. Essentially, the maximum motor current is the amount of current that results in a power dissipation level that, along with the thermal resistance of the package and PCB, keeps the die at a low enough temperature to avoid thermal shutdown.

The dissipation ratings given in the data sheet can be used as a guide to calculate the approximate maximum power dissipation that can be expected without putting the device in thermal shutdown for several different PCB constructions. However, for accurate data, the actual PCB design must be analyzed through measurement or thermal simulation.

### 9.3.2 Thermal Protection

The DRV8847 device has thermal shutdown (TSD) as described in the *Section 9.3.1* section. If the die temperature exceeds approximately 150°C, the device is disabled until the temperature decreases 40°C.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heat-sinking, or too high an ambient temperature.

## 9.4 Power Dissipation

Power dissipation in the DRV8847 device is dominated by the DC power dissipated in the output FET resistance ($R_{DS(ON)_HS}$ and $R_{DS(ON)_LS}$). Additional power is dissipated because of PWM switching losses. These losses are dependent on the PWM frequency, rise and fall times, and VM supply voltages. These switching losses are typically on the order of 10% to 30% of the DC power dissipation.

Use Equation 33 to estimate the DC power dissipation of one H-bridge.

$$P_{TOT} = R_{DS(ON)_LS} \times I_{OUT(RMS)}^{2} + R_{DS(ON)_HS} \times I_{OUT(rms)}^{2} \quad (33)$$

where

- $P_{TOT}$ is the total power dissipation
- $I_{OUT(RMS)}$ is the RMS output current being applied to motor
- $R_{DS(ON)_HS}$ and $R_{DS(ON)_LS}$ are the high-side and low-side on-state resistance of the FET

**Note**

The value of $R_{DS(ON)_HS}$ and $R_{DS(ON)_LS}$ increases with temperature. Therefore, as the device heats, the power dissipation increases. This relationship must be considered when sizing the heat-sink.


Copyright © 2023 Texas Instruments Incorporated

# 10 Device and Documentation Support

## 10.1 Device Support (Optional)

### 10.1.1 Development Support (Optional)

### 10.1.2 Device Nomenclature (Optional)

## 10.2 Documentation Support

### 10.2.1 Related Documentation

For related documentation see the following:

- 
- Texas Instruments, *DRV8847EVM User's Guide*
- Texas Instruments, *DRV8847EVM and DRV8847SEVM Software User's Guide*
- Texas Instruments, *Small Motors in Large Appliances* TI TechNote

## 10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 10.4 Community Resources

## 10.5 Trademarks

PowerPAD™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2023 Texas Instruments Incorporated

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| DRV88471RTER | Active | Production | WQFN (RTE) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | 88471 |
| DRV88471RTER.A | Active | Production | WQFN (RTE) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 88471 |
| DRV8847PWPR | Active | Production | HTSSOP (PWP) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 125 | 8847PWP |
| DRV8847PWPR.A | Active | Production | HTSSOP (PWP) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 8847PWP |
| DRV8847PWPRG4 | Active | Production | HTSSOP (PWP) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 8847PWP |
| DRV8847PWPRG4.A | Active | Production | HTSSOP (PWP) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to -40 | 8847PWP |
| DRV8847PWR | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 125 | 8847PW |
| DRV8847PWR.A | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 8847PW |
| DRV8847PWRG4 | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 8847PW |
| DRV8847PWRG4.A | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 8847PW |
| DRV8847RTER | Active | Production | WQFN (RTE) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 8847 |
| DRV8847RTER.A | Active | Production | WQFN (RTE) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 8847 |
| DRV8847SPWR | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 125 | 8847SPW |
| DRV8847SPWR.A | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 8847SPW |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

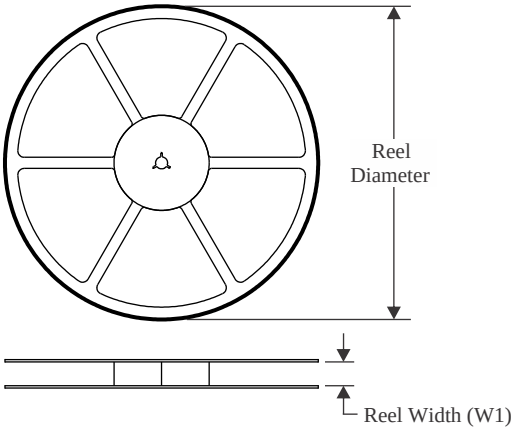
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

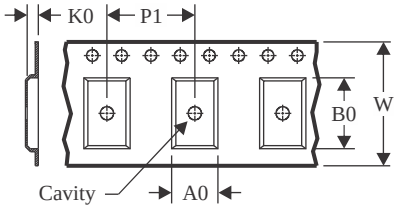
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

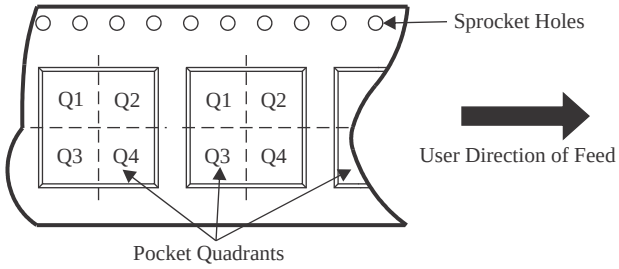



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

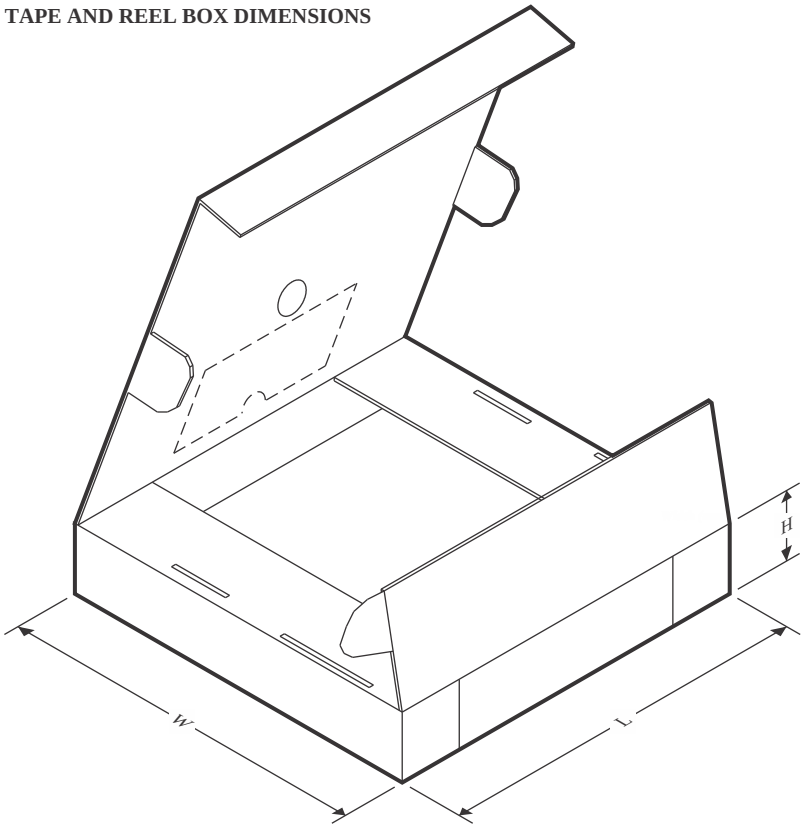
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DRV88471RTER | WQFN | RTE | 16 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| DRV88471RTER | WQFN | RTE | 16 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| DRV8847PWPR | HTSSOP | PWP | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| DRV8847PWPR | HTSSOP | PWP | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| DRV8847PWPRG4 | HTSSOP | PWP | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| DRV8847PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| DRV8847PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| DRV8847PWRG4 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| DRV8847RTER | WQFN | RTE | 16 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| DRV8847SPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.3 | 1.6 | 8.0 | 12.0 | Q1 |
| DRV8847SPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

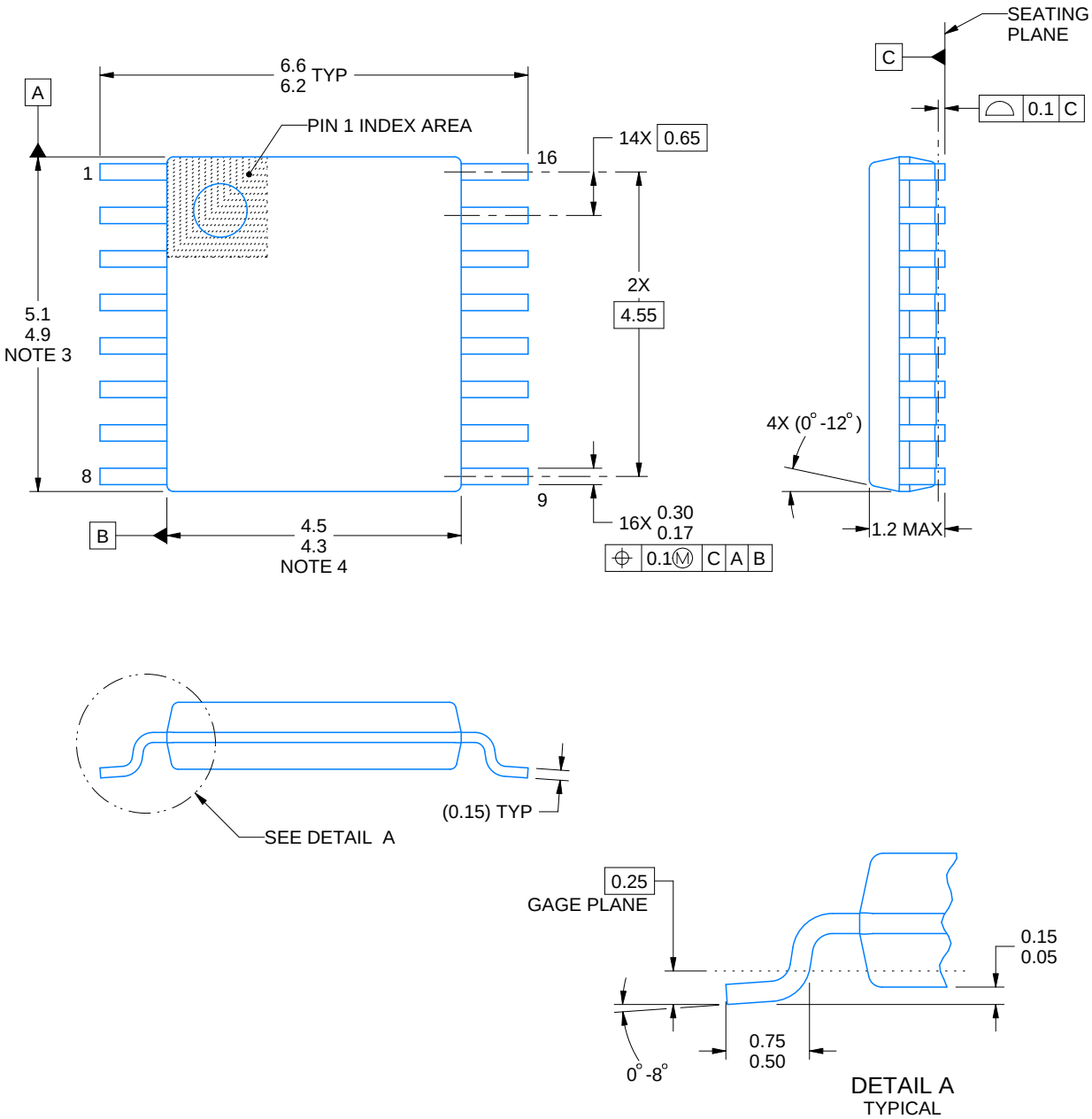
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| DRV88471RTER | WQFN | RTE | 16 | 3000 | 367.0 | 367.0 | 35.0 |
| DRV88471RTER | WQFN | RTE | 16 | 3000 | 356.0 | 356.0 | 36.0 |
| DRV8847PWPR | HTSSOP | PWP | 16 | 2000 | 356.0 | 356.0 | 36.0 |
| DRV8847PWPR | HTSSOP | PWP | 16 | 2000 | 353.0 | 353.0 | 32.0 |
| DRV8847PWPRG4 | HTSSOP | PWP | 16 | 2000 | 353.0 | 353.0 | 32.0 |
| DRV8847PWR | TSSOP | PW | 16 | 2000 | 353.0 | 353.0 | 32.0 |
| DRV8847PWR | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| DRV8847PWRG4 | TSSOP | PW | 16 | 2000 | 353.0 | 353.0 | 32.0 |
| DRV8847RTER | WQFN | RTE | 16 | 3000 | 360.0 | 360.0 | 36.0 |
| DRV8847SPWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| DRV8847SPWR | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |

# PACKAGE OUTLINE

## PW0016A

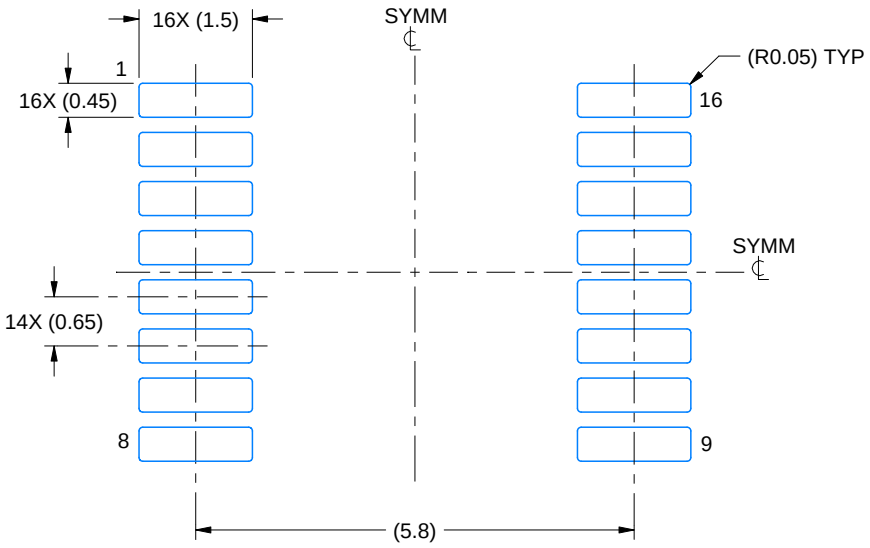
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

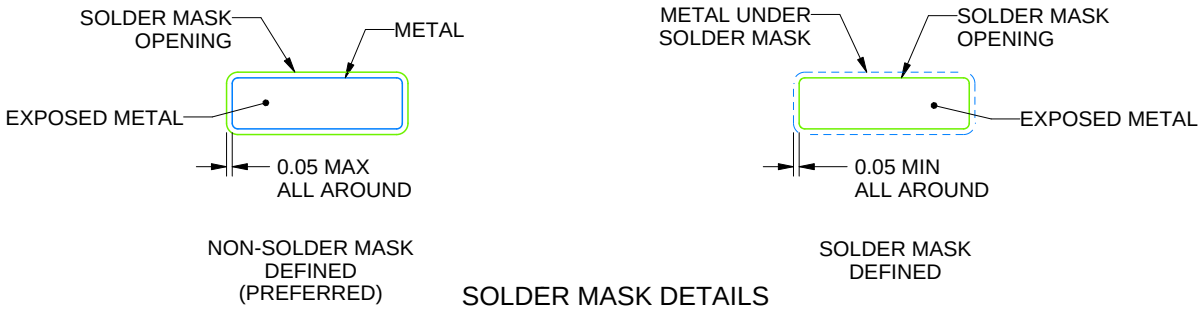



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

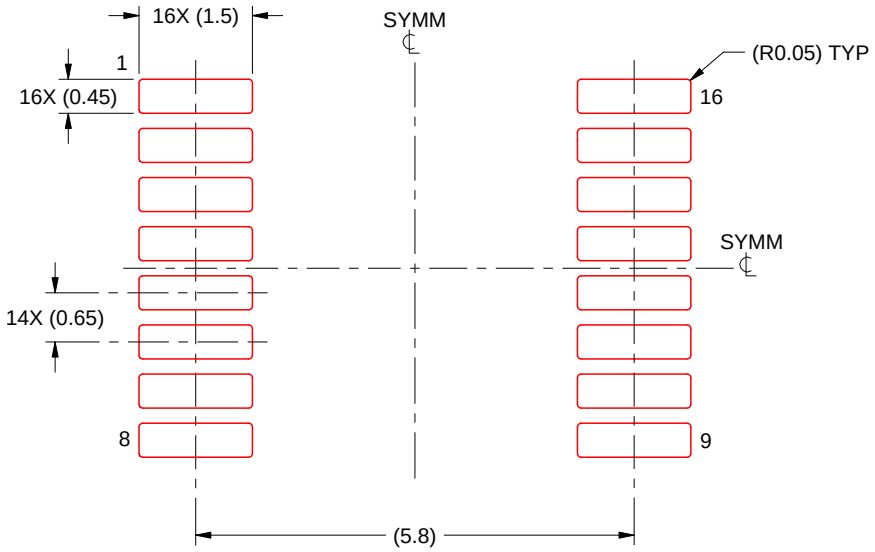



SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

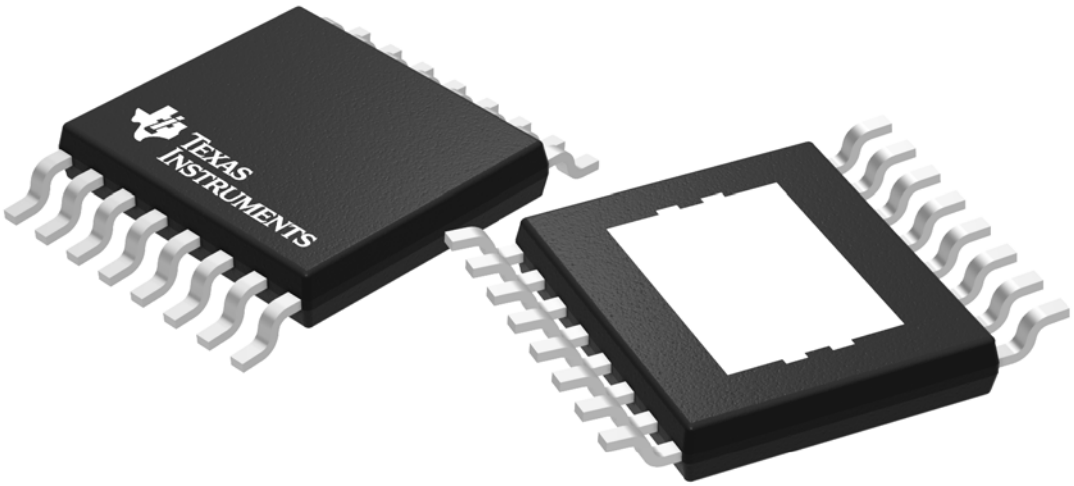
4220204/B 12/2023

NOTES: (continued)

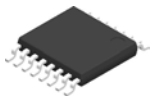
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PWP 16 PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

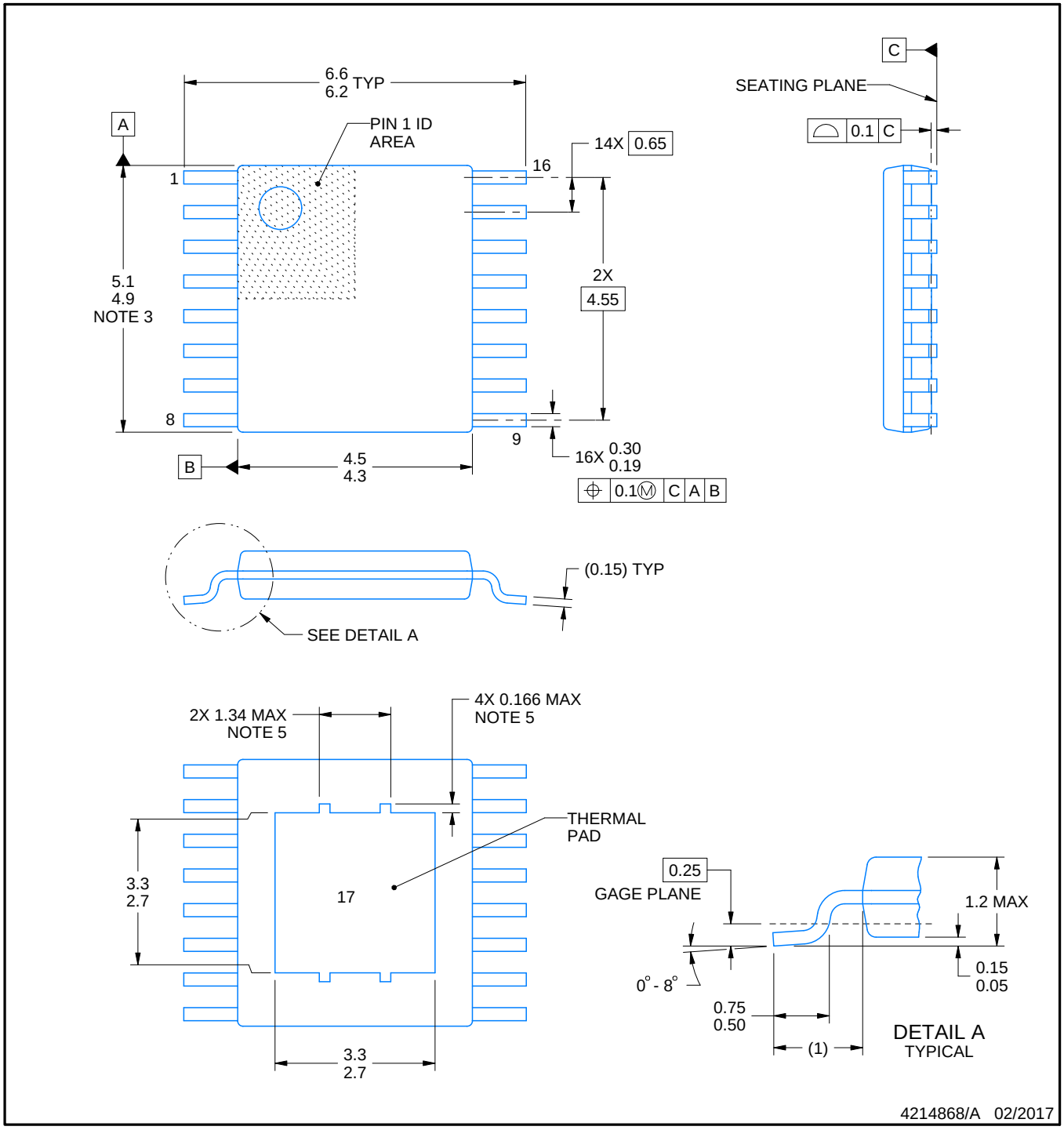


# PACKAGE OUTLINE

## PWP0016A

## PowerPAD ™ HTSSOP - 1.2 mm max height

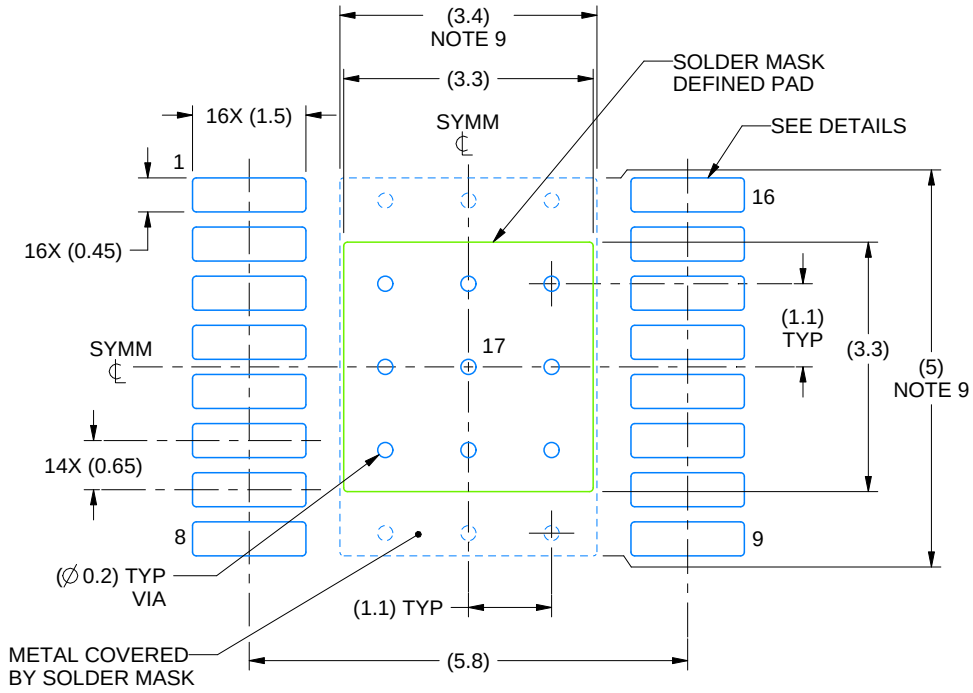
PLASTIC SMALL OUTLINE



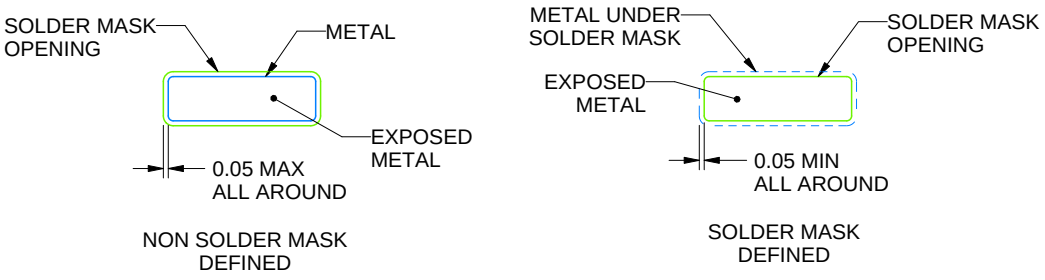

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X

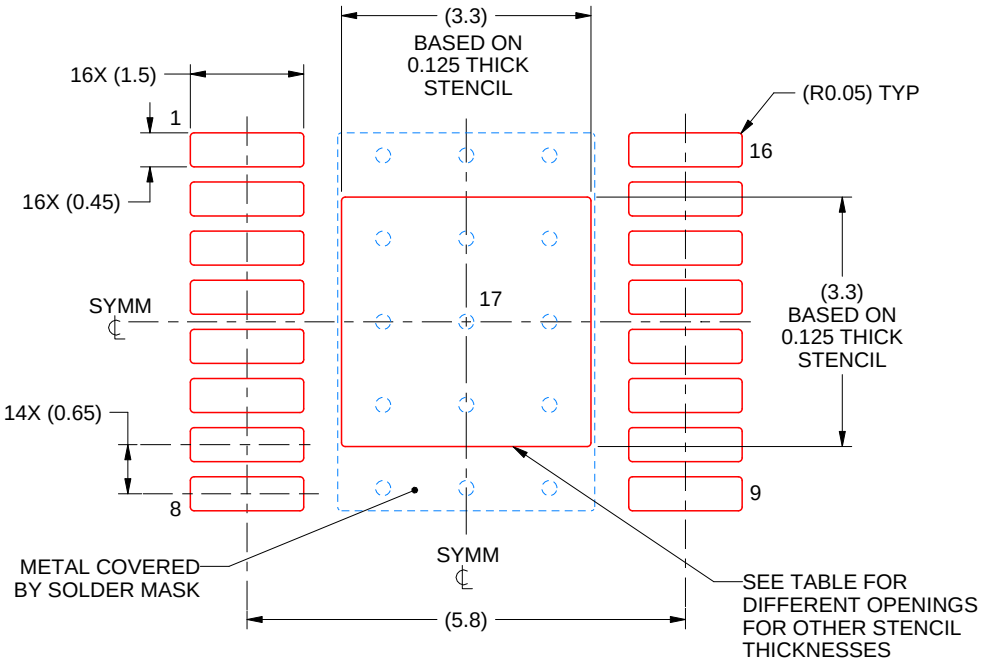



SOLDER MASK DETAILS
PADS 1-16

4214868/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.




SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 3.69 X 3.69 |
| 0.125 | 3.3 X 3.3 (SHOWN) |
| 0.15 | 3.01 X 3.01 |
| 0.175 | 2.79 X 2.79 |

4214868/A 02/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

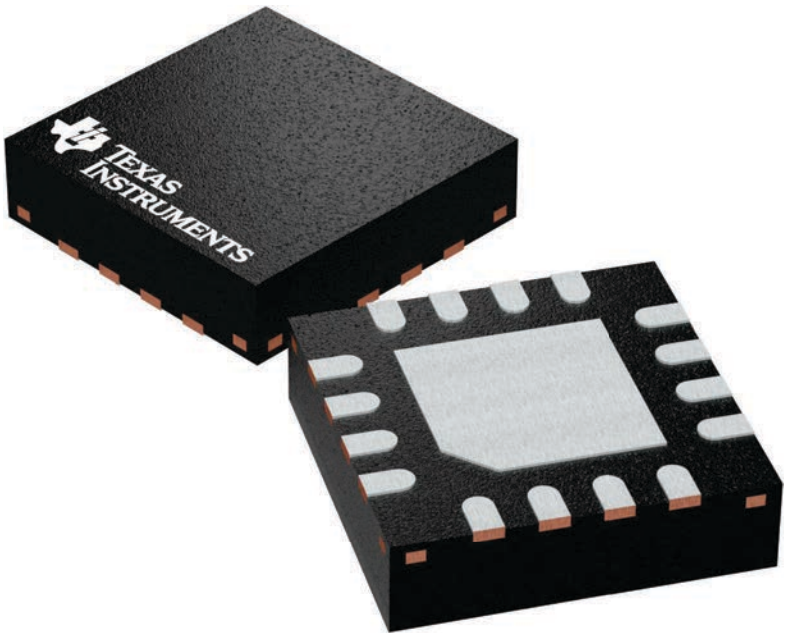
## RTE 16

## WQFN - 0.8 mm max height

**3 x 3, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



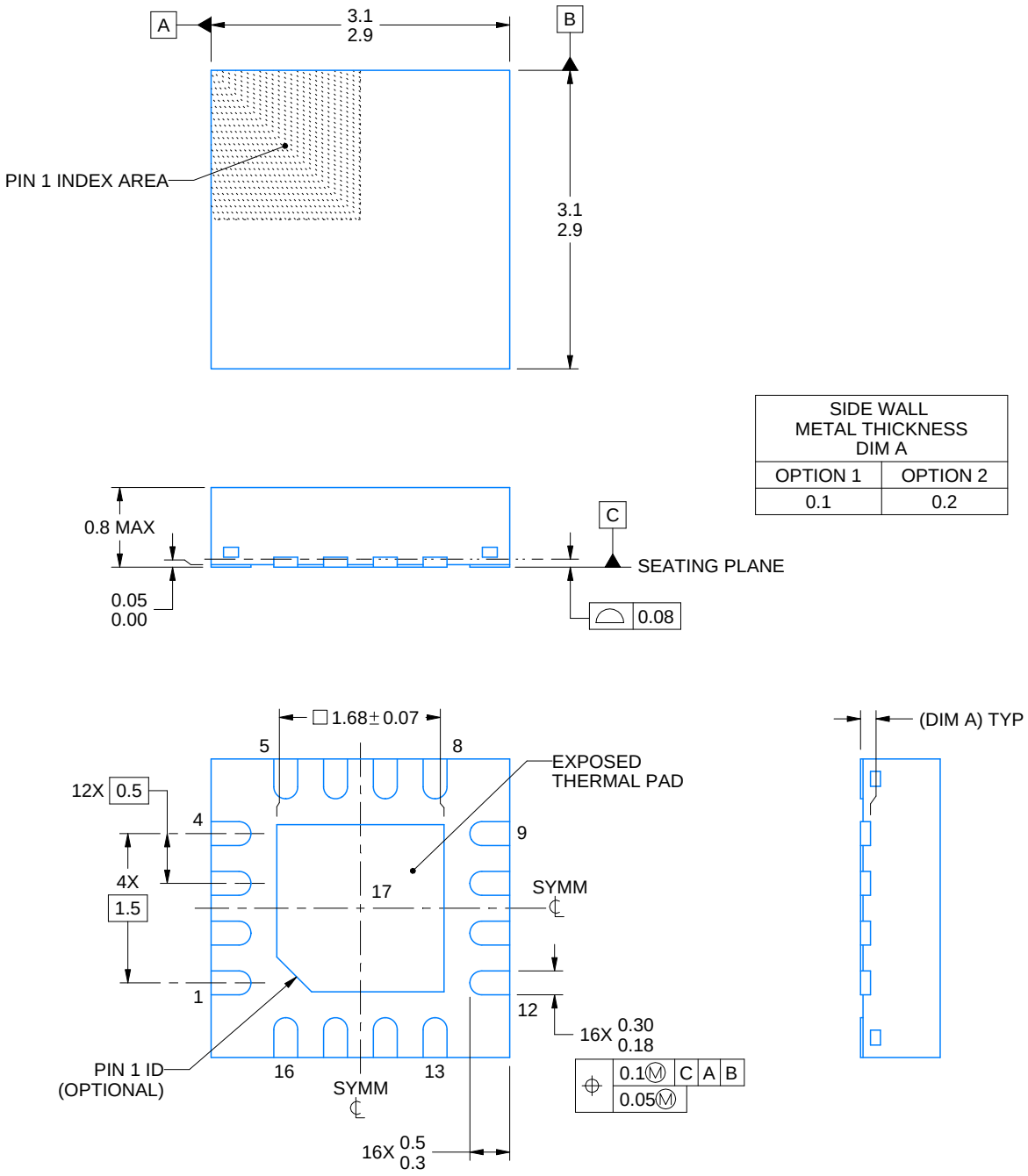

4225944/A

# RTE0016C

# PACKAGE OUTLINE

## WQFN - 0.8 mm max height

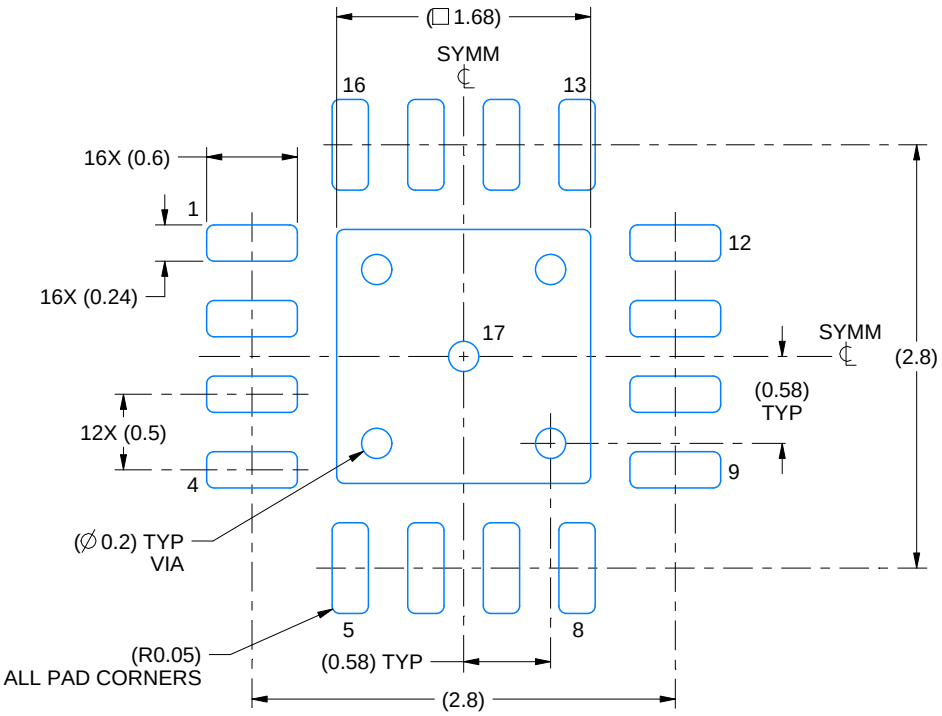
PLASTIC QUAD FLATPACK - NO LEAD



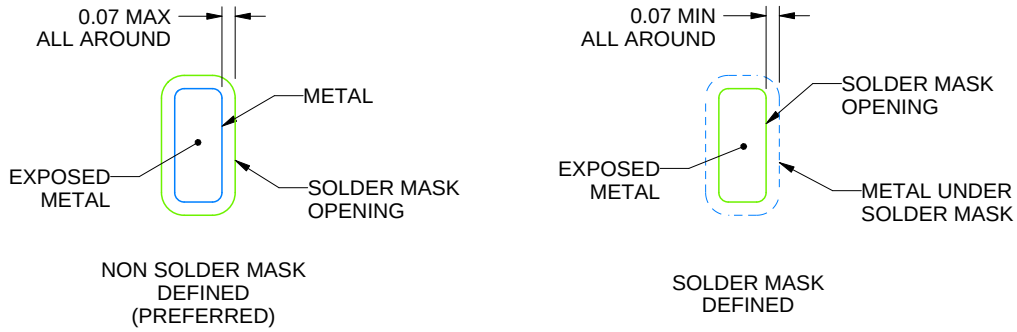

4219117/B 04/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

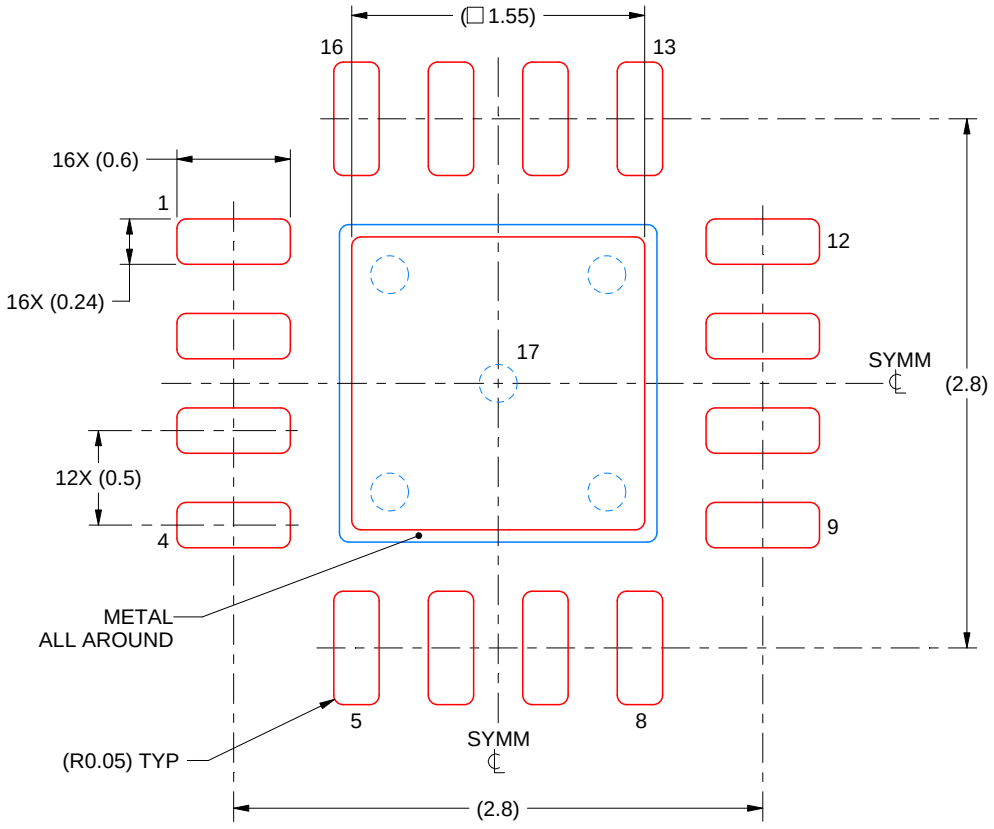



SOLDER MASK DETAILS

4219117/B 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/B 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025