# DS100KR800 8-Channel Repeater for Data-Rates Up to 10.3 Gbps

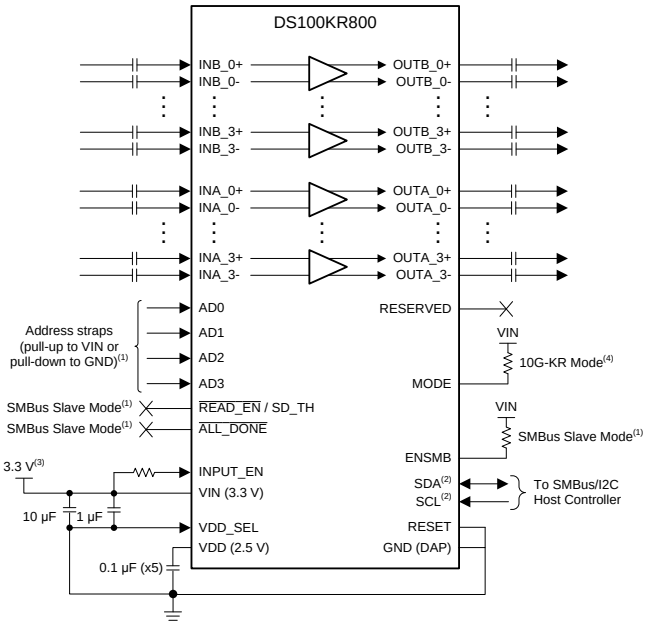
## 1 Features

- Comprehensive Product Family:
  - DS125BR820: 8-Channel Repeater
  - DS125BR401A: 4x Lane Repeater
  - DS125BR111: 1x Lane Repeater
- Transparent Management of 10G-KR (802.3ap) Link Training Protocol
- 65 mW/Channel (Typical) Power Consumption
- Advanced Signal Conditioning Features
  - Receive Equalization up to 36 dB at 5 GHz
  - Transmit De-emphasis up to –12 dB
  - Transmit Voltage Control: 700 mV to 1300 mV
- Programmable Through Pin Selection, EEPROM or SMBus Interface
- Selectable 2.5-V or 3.3-V Supply Voltage
- –40°C to +85°C Operating Temperature Range
- Flow-thru Pinout in Leadless WQFN Package

## 2 Applications

- Front-Port 40G-CR4/SR4/LR4 Link Extensions
- Backplane 40G-KR4 Link Extensions

### Simplified Functional Block Diagram




(1) Schematic shows connection for SMBus Slave Mode (ENSMB=1 kW to VIN)
For SMBus Master Mode or Pin Mode configuration, the connections are different.
(2) SMBus signals need to be pulled up elsewhere in the system.
(3) Schematic requires different connections for 2.5 V mode.
(4) Schematic requires pull-down resistor for 10G Mode.

## 3 Description

The DS100KR800 device is a high performance repeater designed to support 8-channel (unidirectional), 10G-KR, and other high-speed interface serial protocols up to 10.3 Gbps. The continuous time linear equalizer (CTLE) of the receiver provides a boost of up to 36 dB at 5 GHz (10.3125 Gbps) in each of its eight channels. This equalizer is capable of opening an input eye that is completely closed due to inter symbol interference (ISI) induced by interconnect medium such as long backplanes or cables. The transmitter provides a de-emphasis boost of up to –12 dB and output voltage amplitude control from 700 mV to 1300 mV.

When operating in 10G-KR mode, the DS100KR800 transparently allows the host controller and the end point to optimize the full link and negotiate transmit equalizer coefficients as defined in the 802.3ap standard. This seamless management of the link training protocol ensures system level interoperability with minimum latency.

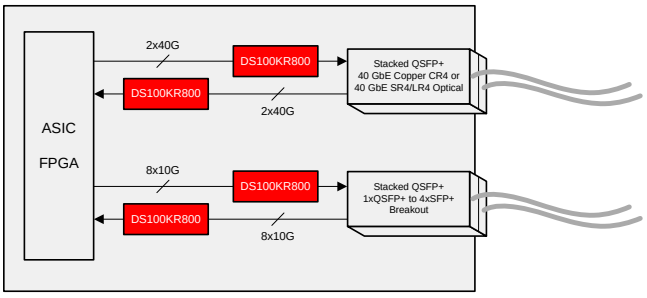
The programmable settings can be applied through pin settings, SMBus ($I^2C$) protocol or an external EEPROM. When operating in the EEPROM mode, the configuration information is automatically loaded on power-up. This eliminates the need for an external microprocessor or software driver.

### Device Information(1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| DS100KR800 | WQFN (54) | 10.00 mm × 5.50 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Typical Application Block Diagram



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision D (April 2013) to Revision E** — **Page**

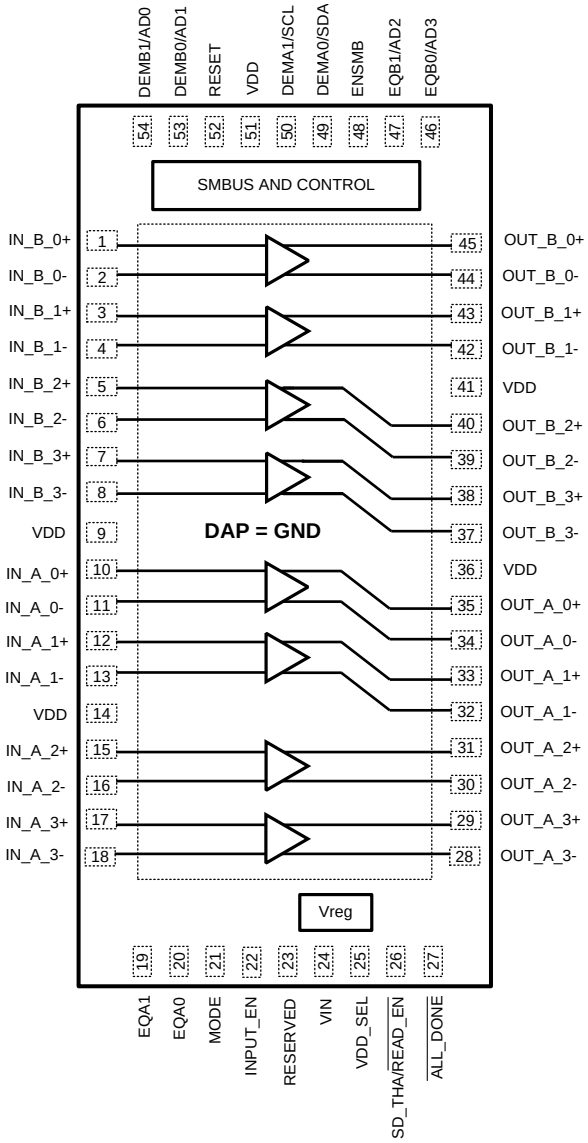
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed Signal detect pattern at 8 Gbps ... 7

**Changes from Revision C (April 2013) to Revision D** — **Page**

- Changed layout of National Data Sheet to TI format ... 1

# 5 Pin Configuration and Functions

**NJY Package**
**54-Pin WQFN**
**Top View**



## Pin Functions: Common Connections[1][2][3][4]

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| **DIFFERENTIAL HIGH SPEED INPUTS AND OUTPUTS** | | | |
| IN_A_0+, IN_A_0-,<br>IN_A_1+, IN_A_1-,<br>IN_A_2+, IN_A_2-,<br>IN_A_3+, IN_A_3- | 10, 11,<br>12, 13,<br>15, 16,<br>17, 18 | I | Inverting and noninverting differential inputs to bank A equalizer. A gated on-chip 50-Ω termination resistor connects INA_n+ to VDD and INA_n- to VDD when enabled. AC coupling required on high-speed I/O. |
| IN_B_0+, IN_B_0-,<br>IN_B_1+, IN_B_1-,<br>IN_B_2+, IN_B_2-,<br>IN_B_3+, IN_B_3-, | 1, 2,<br>3, 4,<br>5, 6,<br>7, 8 | I | Inverting and noninverting differential inputs to bank B equalizer. A gated on-chip 50-Ω termination resistor connects INB_n+ to VDD and INB_n- to VDD when enabled. AC coupling required on high-speed I/O. |
| OUT_A_0+, OUT_A_0-,<br>OUT_A_1+, OUT_A_1-,<br>OUT_A_2+, OUT_A_2-,<br>OUT_A_3+, OUT_A_3- | 35, 34,<br>33, 32,<br>31, 30,<br>29, 28 | O | Inverting and noninverting 50-Ω driver bank A outputs with de-emphasis. Compatible with AC-coupled CML inputs. AC coupling required on high-speed I/O. |
| OUT_B_0+, OUT_B_0-,<br>OUT_B_1+, OUT_B_1-,<br>OUT_B_2+, OUT_B_2-,<br>OUT_B_3+, OUT_B_3-, | 45, 44,<br>43, 42,<br>40, 39,<br>38, 37 | O | Inverting and noninverting 50-Ω driver bank B outputs with de-emphasis. Compatible with AC-coupled CML inputs. AC coupling required on high-speed I/O. |
| **CONTROL PINS — SHARED (LVCMOS)** | | | |
| ENSMB | 48 | I, LVCMOS | System Management Bus (SMBus) enable pin<br>Tie 1 kΩ to VDD = Register Access SMBus Slave mode<br>FLOAT = Read External EEPROM (Master SMBUS Mode)<br>Tie 1 kΩ to GND = Pin Mode |
| **CONTROL PINS — BOTH PIN AND SMBus MODES (LVCMOS)** | | | |
| RESET | 52 | I, LVCMOS | LOW = Device is enabled (Normal Operation)<br>HIGH = Low Power Mode |
| VDD_SEL | 25 | I, FLOAT | Controls the internal regulator<br>Float = 2.5-V mode<br>Tie GND = 3.3-V mode |
| **POWER** | | | |
| GND | DAP | Power | Ground pad (DAP - die attach pad). |
| VDD | 9, 14, 36, 41, 51 | Power | Power supply pins CML/analog<br>2.5-V mode, connect to 2.5 V<br>3.3-V mode, connect 0.1-µF cap to each VDD pin |
| VIN | 24 | Power | In 3.3-V mode, feed 3.3 V to VIN<br>In 2.5-V mode, leave floating. |

(1) LVCMOS inputs without the *Float* conditions must be driven to a logic low or high at all times or operation is not ensured.
(2) Input edge rate for LVCMOS/FLOAT inputs must be faster than 50 ns from 10–90%.
(3) For 3.3-V mode operation, VIN pin = 3.3 V and the VDD for the 4-level input is 3.3 V.
(4) For 2.5-V mode operation, VDD pin = 2.5 V and the VDD for the 4-level input is 2.5 V.

### Pin Functions: SMBus/EEPROM Control

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| **ENSMB = 1 (SMBUS MODE)** | | | |
| AD0-AD3 | 54, 53, 47, 46 | I, LVCMOS | ENSMB master or slave mode<br>User set SMBus Slave Address Inputs in SMBus mode. |
| $\overline{\text{READ\_EN}}$ | 26 | I, 4-LEVEL, LVCMOS | When using an external EEPROM, a transition from high to low starts the load from the external EEPROM |
| SCL | 50 | I, LVCMOS, O, OPEN-Drain | ENSMB master or slave mode<br>SMBUS clock input pin is enabled.<br>Clock output when loading EEPROM configuration (master mode). |
| SDA | 49 | I, LVCMOS, O, OPEN-Drain | ENSMB master or slave mode<br>The SMBus bidirectional SDA pin is enabled. Data input or open-drain output. |
| **ENSMB = 0 (PIN MODE)** | | | |
| MODE | 21 | I, 4-LEVEL, LVCMOS | Tie 1 kΩ to VDD = 10G-KR mode operation<br>Tie 1 kΩ to GND = 10G mode operation |
| SD_TH | 26 | I, 4-LEVEL, LVCMOS | Controls the internal signal detect threshold<br>See Table 4 |
| **CONTROL PINS — BOTH PIN AND SMBus MODES (LVCMOS)** | | | |
| INPUT_EN | 22 | I, 4-LEVEL, LVCMOS | Tie 1 kΩ to VDD = normal operation |
| **OUTPUTS** | | | |
| $\overline{\text{ALL\_DONE}}$ | 27 | O, LVCMOS | Valid register load status output<br>HIGH = external EEPROM load failed<br>LOW = external EEPROM load passed |

### Pin Functions: Pin Control

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| **ENSMB = 0 (PIN MODE)** | | | |
| DEMA0, DEMA1, DEMB0, DEMB1 | 49, 50, 53, 54 | I, 4-LEVEL, LVCMOS | DEMA[1:0] and DEMB[1:0] control the level of de-emphasis of the output driver when in Gen1/2 mode. The pins are only active when ENSMB is deasserted (low). The 8 channels are organized into two banks. Bank A is controlled with the DEMA [1:0] pins and bank B is controlled with the DEMB[1:0] pins. When ENSMB is high the SMBus registers provide independent control of each channel. The DEMA[1:0] pins are converted to SMBUS SCL/SDA and DEMB[1:0] pins are converted to AD0, AD1 inputs.<br>See Table 3 |
| EQA0, EQA1, EQB0, EQB1 | 20, 19, 46, 47 | I, 4-LEVEL, LVCMOS | EQA[1:0] and EQB[1:0] control the level of equalization on the input pins. The pins are active only when ENSMB is deasserted (low). The 8 channels are organized into two banks. Bank A is controlled with the EQA[1:0] pins and bank B is controlled with the EQB[1:0] pins. When ENSMB is high the SMBus registers provide independent control of each channel. The EQB[1:0] pins are converted to SMBUS AD2/ AD3 inputs.<br>See Table 2 |
| MODE | 21 | I, 4-LEVEL, LVCMOS | Tie 1 kΩ to VDD = 10G-KR mode operation<br>Tie 1 kΩ to GND = 10G mode operation |
| SD_TH | 26 | I, 4-LEVEL, LVCMOS | Controls the internal signal detect threshold<br>See Table 4 |
| **CONTROL PINS — BOTH PIN AND SMBus MODES (LVCMOS)** | | | |
| INPUT_EN | 22 | I, 4-LEVEL, LVCMOS | Tie 1 kΩ to VDD = normal operation |
| RESERVED | 23 | I, FLOAT | Float = normal operation |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

See (1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage (VDD = 2.5-V mode) | | –0.5 | 2.75 | V |
| Supply voltage (VIN = 3.3-V mode) | | –0.5 | 4 | V |
| LVCMOS input or output voltage | | –0.5 | 4 | V |
| CML input voltage | | –0.5 | (VDD + 0.5) | V |
| CML input current | | –30 | 30 | ma |
| Junction temperature | | | 125 | °C |
| Lead temperature | Soldering (4 sec.)(2) | | 260 | °C |
| Derate NJY0054A package | | | 52.6 | mW/°C |
| Storage temperature, $T_{stg}$ | | –40 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For soldering specifications: see product folder at SNOA549.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±3000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±1000 | |
| | | Machine model, STD - JESD22-A115-A | ±200 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage | 2.5-V mode | 2.375 | 2.5 | 2.625 | V |
| | 3.3-V mode | 3.0 | 3.3 | 3.6 | V |
| Ambient temperature | | –40 | 25 | 85 | °C |
| SMBus (SDA, SCL) | | | | 3.6 | V |
| Supply noise up to 50 MHz(1) | | | | 100 | mVp-p |

(1) Allowed supply noise (mVp-p sine wave) under typical conditions.

## 6.4 Thermal Information

| THERMAL METRIC(1) | | DS100KR800 NJY (WQFN) 54 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance, No Airflow, 4-layer JEDEC | 26.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 10.8 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 4.4 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.2 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 4.3 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 1.5 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Electrical Characteristics

See (1)(2)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP(3) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **POWER** | | | | | | | |
| PD | Power dissipation | EQ enabled, VOD = 1 Vp-p, INPUT_EN = 1, RESET = 0 | VDD = 2.5-V supply | | 500 | 700 | mW |
| | | | VIN = 3.3-V supply | | 660 | 900 | mW |
| **LVCMOS / LVTTL DC SPECIFICATIONS** | | | | | | | |
| $V_{ih}$ | High level Input voltage | 3.3-V mode operation (VIN = 3.3 V) | | 2 | | 3.6 | V |
| $V_{il}$ | Low level Input voltage | 3.3-V mode operation (VIN = 3.3 V) | | 0 | | 0.8 | V |
| $V_{oh}$ | High level output voltage (ALL_DONE pin) | $I_{oh}$ = –4 mA | | 2 | | | V |
| $V_{ol}$ | Low level output voltage (ALL_DONE pin) | $I_{ol}$ = 4 mA | | | | 0.4 | V |
| $I_{ih}$ | Input high current (RESET pin) | VIN = 3.6 V, LVCMOS = 3.6 V | | –15 | | 15 | µA |
| | Input high current with internal resistors (4–level input pin) | VIN = 3.6 V, LVCMOS = 3.6 V | | 20 | | 150 | µA |
| $I_{il}$ | Input low current (RESET pin) | VIN = 3.6 V, LVCMOS = 0 V | | –15 | | 15 | µA |
| | Input low current with internal resistors (4–level input pin) | VIN = 3.6 V, LVCMOS = 0 V | | –160 | | –40 | µA |
| **CML RECEIVER INPUTS (IN_n+, IN_n-)** | | | | | | | |
| $RL_{rx\text{-}diff}$ | RX package pins plus Si differential return loss | 0.05 GHz - 7.5 GHz | | | –15 | | dB |
| | | 7.5 GHz - 15 GHz | | | –5 | | dB |
| RLrx-cm | Common-mode RX return loss | 0.05 GHz - 5 GHz | | | –10 | | dB |
| Zrx-dc | RX DC common-mode impedance | Tested at VDD = 0 | | 40 | 50 | 60 | Ω |
| Zrx-diff-dc | RX DC differential mode impedance | Tested at VDD = 0 | | 80 | 100 | 120 | Ω |
| Vrx-diff-dc | Differential RX peak-to-peak voltage | Tested at pins | | 0.6 | | 1.2 | V |
| Vrx-signal-det-diff-pp | Signal detect assert level for active data signal | SD_TH = F (float), 0101 pattern at 8 Gbps | | | 180 | | mVp-p |
| Vrx-idle-det-diff-pp | Signal detect deassert level for electrical idle | SD_TH = F (float), 0101 pattern at 8 Gbps | | | 110 | | mVp-p |
| **HIGH SPEED OUTPUTS** | | | | | | | |
| $V_{tx\text{-}diff\text{-}pp}$ | Output voltage differential swing | Differential measurement with Out_n+ and OUT_n-, terminated by 50Ω to GND, AC-Coupled, VID = 1 Vp-p, DEM0 = 1, DEM1 = 0 | | 0.8 | 1 | 1.2 | Vp-p |
| $V_{tx\text{-}de\text{-}ratio\_3.5}$ | TXde-emphasis ratio | VOD = 1 Vp-p, DEM0 = 0, DEM1 = R | | | −3.5 | | dB |
| $V_{tx\text{-}de\text{-}ratio\_6}$ | TX de-emphasis ratio | VOD = 1 Vp-p, DEM0 = R, DEM1= R | | | –6 | | dB |
| $t_{TX\text{-}DJ}$ | Deterministic jitter | VID = 800 mV, PRBS15 pattern, 8.0 0.05 Gbps, VOD = 1 V, UIpp EQ = 0x00, DE = 0 dB (no input or output trace loss) | | | 0.05 | | UIpp |

(1) Ensured by device characterization.
(2) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics* conditions and/or notes. Typical specifications are estimations only and are not ensured.
(3) Typical values represent most likely parametric norms at VDD = 2.5V, TA = 25°C., and at the *Recommended Operation Conditions* at the time of product characterization and are not ensured.

## Electrical Characteristics (continued)

See (1)(2)

| PARAMETER | | TEST CONDITIONS | MIN | TYP (3) | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{TX-RJ}$ | Random jitter | VID = 800 mV, 0101 pattern, 8.0 Gbps, 0.3 VOD = 1 V, ps RMS EQ = 0x00, DE = 0 dB, (no input or output trace loss) | | 0.3 | | ps RMS |
| $T_{TX-RISE-FALL}$ | Transmitter rise/fall time | 20% to 80% of differential output voltage | 35 | 45 | | ps |
| $T_{RF-MISMATCH}$ | Transmitter rise/fall mismatch | 20% to 80% of differential output voltage | | 0.01 | 0.1 | UI |
| $RL_{TX-DIFF}$ | Differential return loss | 0.05 GHz - 7.5 GHz | | –15 | | dB |
| | | 7.5 GHz - 15 GHz | | –5 | | dB |
| $RL_{TX-CM}$ | Common-mode return loss | 0.05 GHz - 5 GHz | | –10 | | dB |
| $Z_{TX-DIFF-DC}$ | DC differential TX impedance | | | 100 | | Ω |
| $V_{TX-CM-AC-PP}$ | TX AC common-mode voltage | VOD = 1 Vp-p, DEM0 = 1, DEM1 = 0 | | | 100 | mVp p |
| $I_{TX-SHORT}$ | Transmitter short circuit current-limit | Total current the transmitter can supply when shorted to VDD or GND | | 20 | | mA |
| $T_{PDEQ}$ | Differential propagation delay | EQ = 00, (4) | | 200 | | ps |
| $T_{LSK}$ | Lane-to-lane skew | T = 25°C, VDD = 2.5 V | | 25 | | ps |
| $T_{PPSK}$ | Part-to-part propagation delay skew | T = 25°C, VDD = 2.5 V | | 40 | | ps |
| **EQUALIZATION** | | | | | | |
| DJE1 | Residual deterministic jitter at 10.3 Gbps | 35-in 4 mil FR4, VID = 0.8 Vp-p, PRBS15, EQ = 1F'h, DEM = 0 dB | | 0.3 | | UI |
| DJE2 | Residual deterministic jitter at 10.3 Gbps | 10 meters 30 awg cable, VID = 0.8 Vp-p, PRBS15, EQ = 2F'h, DEM = 0 dB | | 0.3 | | UI |
| **DE-EMPHASIS** | | | | | | |
| DJD1 | Residual deterministic jitter at 10.3 Gbps | 20-in 4 mil FR4, VID = 0.8 Vp-p, PRBS15, EQ = 00, VOD = 1 Vp-p, DEM = −9 dB | | 0.1 | | UI |

(4) Propagation Delay measurements will change slightly based on the level of EQ selected. EQ = 00 will result in the shortest propagation delays.

## 6.6 Electrical Characteristics – Serial Management Bus Interface

Over recommended operating supply and temperature ranges unless other specified.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SERIAL BUS INTERFACE DC SPECIFICATIONS** | | | | | | |
| $V_{IL}$ | Data, clock input low voltage | | | | 0.8 | V |
| $V_{IH}$ | Data, clock input high voltage | | 2.1 | | 3.6 | V |
| $I_{PULLUP}$ | Current through pullup resistor or current source | High power specification | 4 | | | mA |
| $V_{DD}$ | Nominal bus voltage | | 2.375 | | 3.6 | V |
| $I_{LEAK-Bus}$ | Input leakage per bus segment | See (1) | –200 | | 200 | µA |
| $I_{LEAK-Pin}$ | Input leakage per device pin | | | –15 | | µA |
| $C_I$ | Capacitance for SDA and SCL | See (1) (2) | | | 10 | pF |

(1) Recommended value.
(2) Recommended maximum capacitance load per bus segment is 400pF.

## Electrical Characteristics – Serial Management Bus Interface (continued)

Over recommended operating supply and temperature ranges unless other specified.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $R_{TERM}$ | External termination resistance pull to $V_{DD}$ = 2.5 V ± 5% OR 3.3 V ± 10% | Pullup $V_{DD}$ = 3.3 V, See (1) (2) (3) | | 2000 | | Ω |
| | | Pullup $V_{DD}$ = 2.5 V, See (1) (2) (3) | | 1000 | | Ω |

(3) Maximum termination voltage should be identical to the device supply voltage.

## 6.7 Timing Requirements – Serial Bus Interface Timing Specifications

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| FSMB | Bus operating frequency | ENSMB = VDD (slave mode) | | | 400 | kHz |
| | | ENSMB = FLOAT (master mode) | 280 | 400 | 520 | kHz |
| $T_{BUF}$ | Bus free time between stop and start condition | | 1.3 | | | µs |
| $T_{HD:STA}$ | Hold time after (repeated) start condition. After this period, the first clock is generated. | At $I_{PULLUP}$, maximum | 0.6 | | | µs |
| $T_{SU:STA}$ | Repeated start condition set-up time | | 0.6 | | | µs |
| $T_{SU:STO}$ | Stop condition set-up time | | 0.6 | | | µs |
| $T_{HD:DAT}$ | Data hold time | | 0 | | | ns |
| $T_{SU:DAT}$ | Data set-up time | | 100 | | | ns |
| $T_{LOW}$ | Clock low period | | 1.3 | | | µs |
| $T_{HIGH}$ | Clock high period | See (1) | 0.6 | | 50 | µs |
| $t_F$ | Clock/Data fall time | See (1) | | | 300 | ns |
| $t_R$ | Clock/Data rise time | See (1) | | | 300 | ns |
| $t_{POR}$ | Time in which a device must be operational after power-on reset | See (1) (2) | | | 500 | ms |

(1) Compatible with SMBus 2.0 physical layer specification. See System Management Bus (SMBus) Specification Version 2.0, section 3.1.1 SMBus common AC specifications for details.
(2) Ensured by Design. Parameter not tested in production.

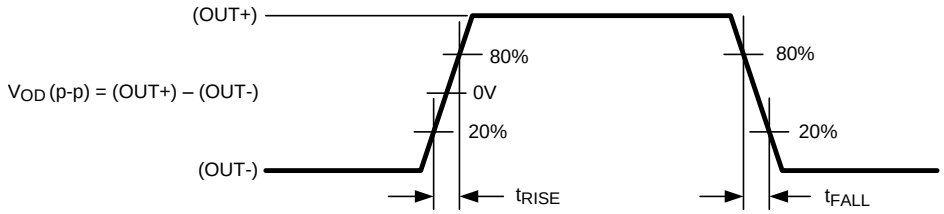



**Figure 1. CML Output and Rise and Fall Transition Time**

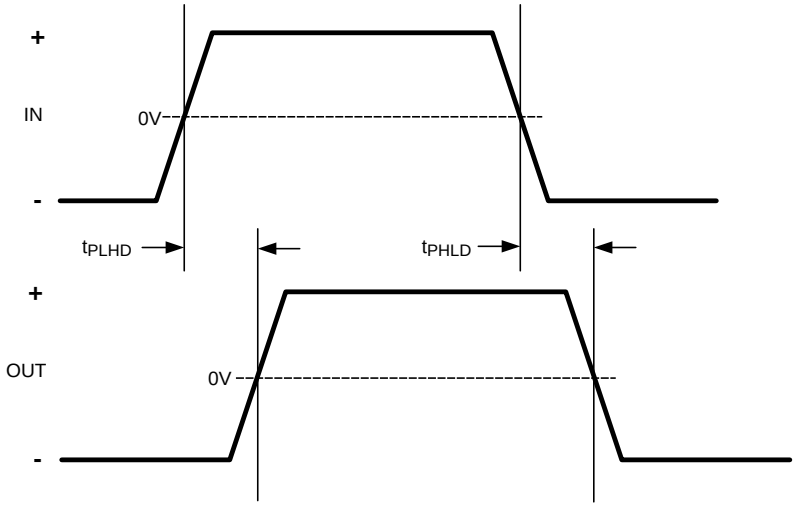



**Figure 2. Propagation Delay Timing Diagram**

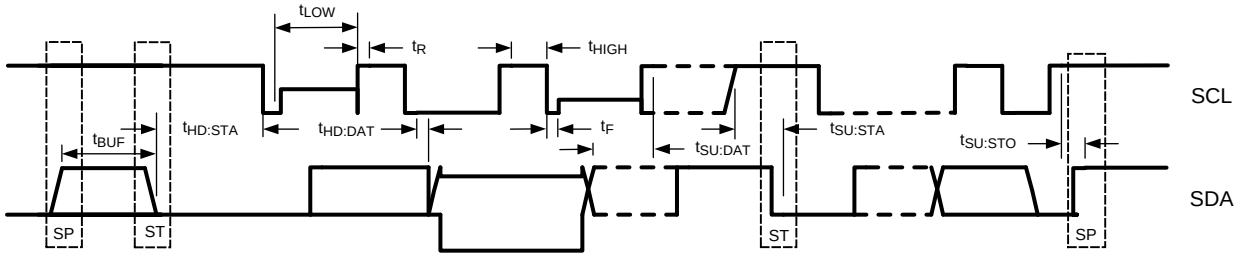



**Figure 3. SMBus Timing Parameters**

## 6.8 Typical Characteristics

### 6.8.1 Electrical Performance

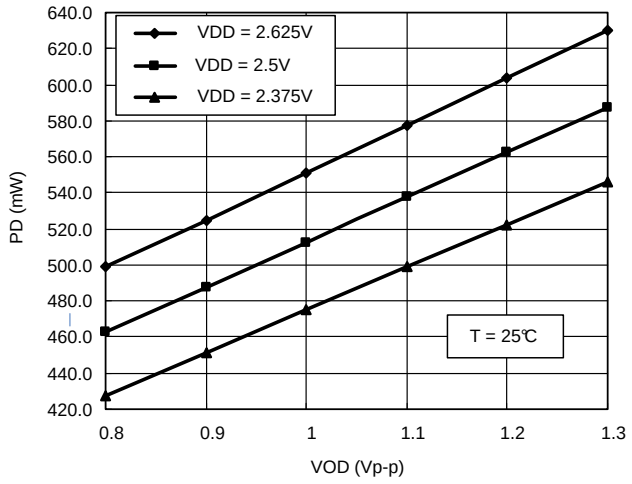



**Figure 4. Power Dissipation (PD) vs Output Differential Voltage (VOD)**

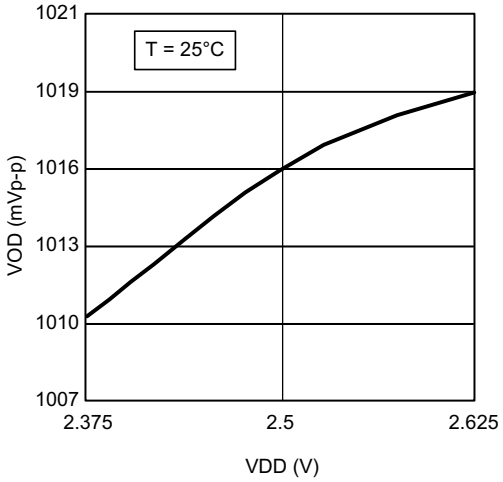



**Figure 5. Output Differential Voltage (VOD = 1 Vp-p) vs Supply Voltage (VDD)**

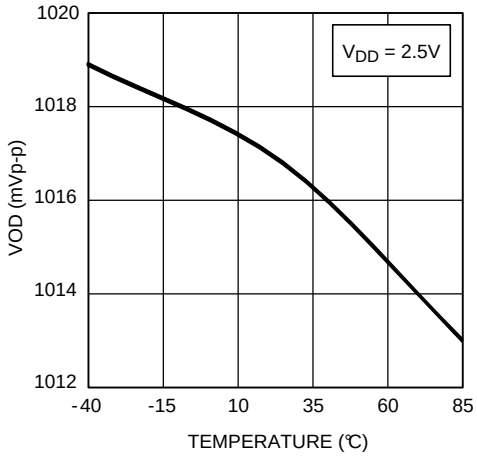


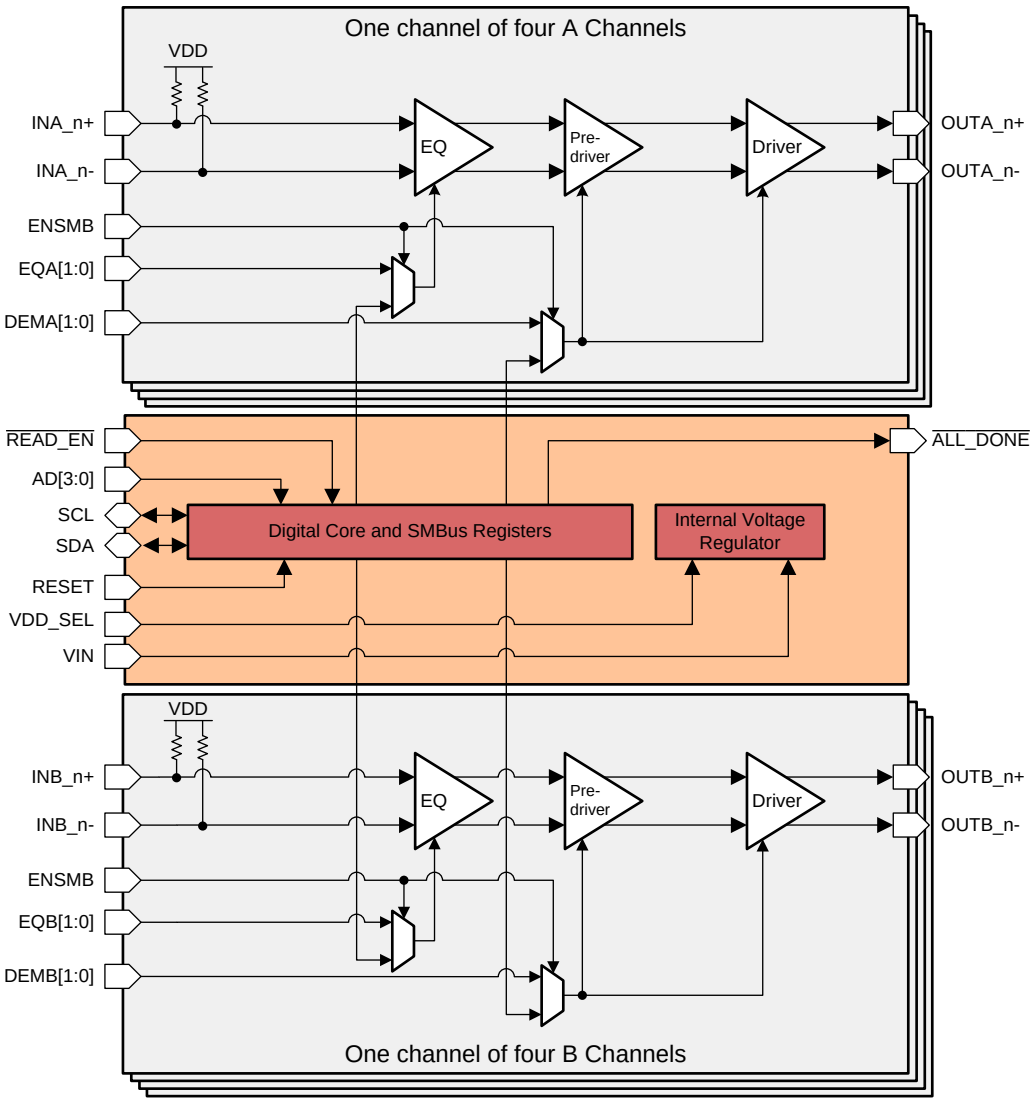

**Figure 6. Output Differential Voltage (VOD = 1 Vp-p) vs Temperature**

# 7 Detailed Description

## 7.1 Overview

The DS100KR800 is a low-power media compensation, 8-channel repeater optimized for 10G–KR. The DS100KR800 compensates for lossy FR-4 printed-circuit-board backplanes and balanced cables. The DS100KR800 operates in 3 modes: Pin control mode (ENSMB = 0), SMBus slave mode (ENSMB = 1) and SMBus master mode (ENSMB = float) to load register information from external EEPROM; refer to SMBUS master mode for additional information.

## 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 4-Level Input Configuration Guidelines

The 4-level input pins use a resistor divider to help set the four valid control levels and provide a wider range of control settings when ENSMB = 0. There is an internal 30-kΩ pullup and a 60-kΩ pulldown connected to the package pin. These resistors, together with the external resistor connection, combine to achieve the desired voltage level. By using the 1-kΩ pulldown, 20-kΩ pulldown, no connect, and 1-kΩ pullup, the optimal voltage levels for each of the four input states are achieved as shown in Table 1.

**Table 1. 4–Level Control Pin Settings**

| LEVEL | SETTING | RESULTING PIN VOLTAGE | |
|---|---|---|---|
| | | 3.3-V MODE | 2.5-V MODE |
| 0 | Tie 1 kΩ to GND | 0.1 V | 0.08 V |
| R | Tie 20 kΩ to GND | 1/3 x $V_{IN}$ | 1/3 x $V_{DD}$ |
| F | Float (leave pin open) | 2/3 x $V_{IN}$ | 2/3 x $V_{DD}$ |
| 1 | Tie 1 kΩ to $V_{IN}$ or $V_{DD}$ | $V_{IN}$ – 0.05 V | $V_{DD}$ – 0.04 V |

The typical 4-level input thresholds are as follows:

- Internal Threshold between 0 and R = 0.2 × $V_{IN}$ or $V_{DD}$
- Internal Threshold between R and F = 0.5 × $V_{IN}$ or $V_{DD}$
- Internal Threshold between F and 1 = 0.8 × $V_{IN}$ or $V_{DD}$

In order to minimize the start-up current associated with the integrated 2.5-V regulator, the 1-kΩ pullup and pulldown resistors are recommended. If several four level inputs require the same setting, it is possible to combine two or more 1-kΩ resistors into a single lower value resistor. As an example, combining two inputs with a single 500-Ω resistor is a valid way to save board space.

## 7.4 Device Functional Modes

### 7.4.1 Pin Control Mode

When in pin mode (ENSMB = 0) , the repeater is configurable with external pins. Equalization and de-emphasis can be selected through pin for each side independently. When de-emphasis is asserted VOD is automatically adjusted per the Table 3. The receiver electrical idle detect threshold is also adjustable through the SD_TH pin.

### 7.4.2 SMBUS Mode

When in SMBus mode (ENSMB = 1), the VOD (output amplitude), equalization, de-emphasis, and termination disable features are all programmable on a individual lane basis, instead of grouped by A or B as in the pin mode case. Upon assertion of ENSMB the MODE, EQx and DEMx functions revert to register control immediately. The EQx and DEMx pins are converted to AD0-AD3 SMBus address inputs. The other external control pins remain active unless their respective registers are written to and the appropriate override bit is set, in which case they are ignored until ENSMB is driven low (pin mode). On power-up and when ENSMB is driven low all registers are reset to their default state. If RESET is asserted while ENSMB is high, the registers retain their current state.

Equalization settings accessible through the pin controls were chosen to meet the needs of most applications. If additional fine tuning or adjustment is needed, additional equalization settings can be accessed through the SMBus registers. Each input has a total of 256 possible equalization settings. The tables show the 16 setting when the device is in pin mode. When using SMBus mode, the equalization, VOD and de-Emphasis levels are set by registers.

The input control pins have been enhanced to have 4 different levels and provide a wider range of control settings when ENSMB=0.

## Device Functional Modes (continued)

**Table 2. Equalizer Settings**

| LEVEL | EQA1 EQB1 | EQA0 EQB0 | EQ – 8 BITS [7:0] | dB AT 1 GHz | dB AT 3 GHz | dB AT 5 GHz | SUGGESTED USE |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0000 0000 = 0x00 | 1.7 | 4.2 | 5.3 | FR4 < 5 inch trace |
| 2 | 0 | R | 0000 0001 = 0x01 | 2.8 | 6.6 | 8.7 | FR4 5 inch 5–mil trace |
| 3 | 0 | Float | 0000 0010 = 0x02 | 4.1 | 8.6 | 10.6 | FR4 5 inch 4–mil trace |
| 4 | 0 | 1 | 0000 0011 = 0x03 | 5.1 | 9.8 | 11.7 | FR4 10 inch 5–mil trace |
| 5 | R | 0 | 0000 0111 = 0x07 | 6.2 | 12.4 | 15.6 | FR4 10 inch 4–mil trace |
| 6 | R | R | 0001 0101 = 0x15 | 5.1 | 12 | 16.6 | FR4 15 inch 4–mil trace |
| 7 | R | Float | 0000 1011 = 0x0B | 7.7 | 15 | 18.3 | FR4 20 inch 4–mil trace |
| 8 | R | 1 | 0000 1111 = 0x0F | 8.8 | 16.5 | 19.7 | FR4 25 to 30 inch 4–mil trace |
| 9 | Float | 0 | 0101 0101 = 0x55 | 6.3 | 14.8 | 20.3 | FR4 30 inch 4–mil trace |
| 10 | Float | R | 0001 1111 = 0x1F | 9.9 | 19.2 | 23.6 | FR4 35 inch 4–mil trace |
| 11 | Float | Float | 0010 1111 = 0x2F | 11.3 | 21.7 | 25.8 | 10m, 30awg cable |
| 12 | Float | 1 | 0011 1111 = 0x3F | 12.4 | 23.2 | 27 | 10m – 12m cable |
| 13 | 1 | 0 | 1010 1010 = 0xAA | 11.9 | 24.1 | 29.1 | |
| 14 | 1 | R | 0111 1111 = 0x7F | 13.6 | 26 | 30.7 | |
| 15 | 1 | Float | 1011 1111 = 0xBF | 15.1 | 28.3 | 32.7 | |
| 16 | 1 | 1 | 1111 1111 = 0xFF | 16.1 | 29.7 | 33.8 | |

**Table 3. De-emphasis Settings**

| LEVEL | DEMA1 DEMB1 | DEMA0 DEMB0 | VOD Vp-p | DEM dB | INNER AMPLITUDE Vp-p | SUGGESTED USE |
|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0.8 | 0 | 0.8 | FR4 <5 inch 4–mil trace |
| 2 | 0 | R | 0.9 | 0 | 0.9 | FR4 <5 inch 4–mil trace |
| 3 | 0 | Float | 0.9 | –3.5 | 0.6 | FR4 10 inch 4–mil trace |
| 4 | 0 | 1 | 1 | 0 | 1 | FR4 <5 inch 4–mil trace |
| 5 | R | 0 | 1 | –3.5 | 0.7 | FR4 10 inch 4–mil trace |
| 6 | R | R | 1 | –6 | 0.5 | FR4 15 inch 4–mil trace |
| 7 | R | Float | 1.1 | 0 | 1.1 | FR4 <5 inch 4–mil trace |
| 8 | R | 1 | 1.1 | –3.5 | 0.7 | FR4 10 inch 4–mil trace |
| 9 | Float | 0 | 1.1 | –6 | 0.6 | FR4 15 inch 4–mil trace |
| 10 | Float | R | 1.2 | 0 | 1.2 | FR4 <5 inch 4–mil trace |
| 11 | Float | Float | 1.2 | –3.5 | 0.8 | FR4 10 inch 4–mil trace |
| 12 | Float | 1 | 1.2 | –6 | 0.6 | FR4 15 inch 4–mil trace |
| 13 | 1 | 0 | 1.3 | 0 | 1.3 | FR4 <5 inch 4–mil trace |
| 14 | 1 | R | 1.3 | –3.5 | 0.9 | FR4 10 inch 4–mil trace |
| 15 | 1 | Float | 1.3 | –6 | 0.7 | FR4 15 inch 4–mil trace |
| 16 | 1 | 1 | 1.3 | –9 | 0.5 | FR4 20 inch 4–mil trace |

**Table 4. Signal Detect Threshold Level (1)**

| SD_TH | SMBus REG BIT [3:2] AND [1:0] | ASSERT LEVEL (TYP) | DEASSERT LEVEL (TYP) |
|---|---|---|---|
| 0 | 10 | 210 mVp-p | 150 mVp-p |
| R | 01 | 160 mVp-p | 100 mVp-p |
| F (default) | 00 | 180 mVp-p | 110 mVp-p |
| 1 | 11 | 190 mVp-p | 130 mVp-p |

(1) Note: VDD = 2.5 V, 25°C and 0101 pattern at 8 Gbps

## 7.5 Programming

### 7.5.1 SMBUS Master Mode

The DS100KR800 devices support reading directly from an external EEPROM device by implementing SMBus Master mode. When using the SMBus master mode, the DS100KR800 will read directly from specific location in the external EEPROM. When designing a system for using the external EEPROM, the user needs to follow these specific guidelines.

- Set ENSMB = Float — enable the SMBUS master mode.
- The external EEPROM device address byte must be 0xA0'h and capable of 1-MHz operation at 2.5-V and 3.3-V supply. The maximum allowed size is 8 kbits (1024 bytes).
- Set the AD[3:0] inputs for SMBus address byte. When the AD[3:0] = 0000'b, the device address byte is B0'h.

When tying multiple DS100KR800 devices to the SDA and SCL bus, use these guidelines to configure the devices.

- Use SMBus AD[3:0] address bits so that each device can loaded it's configuration from the EEPROM. Example below is for 4 device

  U1: AD[3:0] = 0000 = 0xB0'h,

  U2: AD[3:0] = 0001 = 0xB2'h,

  U3: AD[3:0] = 0010 = 0xB4'h,

  U4: AD[3:0] = 0011 = 0xB6'h
- Use a pullup resistor on SDA and SCL; value = 2 kΩ
- Daisy-chain READEN# (pin 26) and ALL_DONE# (pin 27) from one device to the next device in the sequence so that they do not compete for the EEPROM at the same time.
  1. Tie READEN# of the 1st device in the chain (U1) to GND
  2. Tie ALL_DONE# of U1 to READEN# of U2
  3. Tie ALL_DONE# of U2 to READEN# of U3
  4. Tie ALL_DONE# of U3 to READEN# of U4
  5. Optional: Tie ALL_DONE# output of U4 to a LED to show the devices have been loaded successfully

Below is an example of a 2 kbits (256 × 8-bit) EEPROM in hex format for the DS100KR800 device. The first 3 bytes of the EEPROM always contain a header common and necessary to control initialization of all devices connected to the I2C bus. CRC enable flag to enable/disable CRC checking. If CRC checking is disabled, a fixed pattern (8'hA5) is written or read instead of the CRC byte from the CRC location, to simplify the control. There is a MAP bit to flag the presence of an address map that specifies the configuration data start in the EEPROM. If the MAP bit is not present the configuration data start address is derived from the DS100KR800 address and the configuration data size. A bit to indicate an EEPROM size > 256 bytes is necessary to properly address the EEPROM. There are 37 bytes of data size for each DS100KR800 device.

```
:20000000000010000000407002FAD4002FAD4002FAD4002FAD409805F5A8005F5A8005F5AD0
:20002000 8005F5A800005454 0000000000000000000000000000000000000000000000F6
:20006000000000000000000000000000000000000000000000000000000000000000000080
:20008000000000000000000000000000000000000000000000000000000000000000000060
:2000A000000000000000000000000000000000000000000000000000000000000000000040
:2000C000000000000000000000000000000000000000000000000000000000000000000020
:2000E000000000000000000000000000000000000000000000000000000000000000000000
:20004000000000000000000000000000000000000000000000000000000000000000000A0
```

**NOTE**

The maximum EEPROM size supported is 8 kbits (1024 x 8 bits). For more information in regards to EEPROM programming and the hex format, see SNLA228.

## 7.6 Register Maps

### 7.6.1 System Management Bus (SMBus) and Configuration Registers

The System Management Bus interface is compatible to SMBus 2.0 physical layer specification. ENSMB = 1 kΩ to VDD to enable SMBus slave mode and allow access to the configuration registers.

The DS100KR800 has the AD[3:0] inputs in SMBus mode. These pins are the user set SMBUS slave address inputs. The AD[3:0] pins have internal pulldown. When left floating or pulled low the AD[3:0] = 0000'b, the device default address byte is B0'h. Based on the SMBus 2.0 specification, the DS100KR800 has a 7-bit slave address. The LSB is set to 0'b (for a WRITE). The device supports up to 16 address byte, which can be set with the AD[3:0] inputs. Below are the 16 addresses.

**Table 5. Device Slave Address Bytes**

| AD[3:0] SETTINGS | ADDRESS BYTES (HEX) |
|---|---|
| 0000 | B0 |
| 0001 | B2 |
| 0010 | B4 |
| 0011 | B6 |
| 0100 | B8 |
| 0101 | BA |
| 0110 | BC |
| 0111 | BE |
| 1000 | C0 |
| 1001 | C2 |
| 1010 | C4 |
| 1011 | C6 |
| 1100 | C8 |
| 1101 | CA |
| 1110 | CC |
| 1111 | CE |

The SDA, SCL pins are 3.3-V tolerant, but are not 5-V tolerant. External pullup resistor is required on the SDA. The resistor value can be from 1 kΩ to 5 kΩ depending on the voltage, loading and speed. The SCL may also require an external pullup resistor and it depends on the Host that drives the bus.

#### *7.6.1.1 Transfer of Data Through the SMBus*

During normal operation the data on SDA must be stable during the time when SCL is High.

There are three unique states for the SMBus:

**START:** A High-to-Low transition on SDA while SCL is High indicates a message START condition.

**STOP:** A Low-to-High transition on SDA while SCL is High indicates a message STOP condition.

**IDLE:** If SCL and SDA are both High for a time exceeding $t_{BUF}$ from the last detected STOP condition or if they are High for a total exceeding the maximum specification for $t_{HIGH}$ then the bus will transfer to the IDLE state.

#### *7.6.1.2 SMBus Transactions*

The device supports WRITE and READ transactions. See Table 6 for register address, type (Read/Write, Read Only), default value and function information.

#### *7.6.1.3 Writing a Register*

To write a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a 0 indicating a WRITE.
2. The Device (Slave) drives the ACK bit (0).

3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit (0).
5. The Host drive the 8-bit data byte.
6. The Device drives an ACK bit (0).
7. The Host drives a STOP condition.

The WRITE transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

#### *7.6.1.4 Reading a Register*

To read a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a 0 indicating a WRITE.
2. The Device (Slave) drives the ACK bit (0).
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit (0).
5. The Host drives a START condition.
6. The Host drives the 7-bit SMBus Address, and a 1 indicating a READ.
7. The Device drives an ACK bit 0.
8. The Device drives the 8-bit data value (register contents).
9. The Host drives a NACK bit 1 indicating end of the READ transfer.
10. The Host drives a STOP condition.

The READ transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

See Table 6 for more information.

**Table 6. SMbus Register Description Table**

| ADDRESS | REGISTER NAME | BIT | FIELD | TYPE | DEFAULT | EEPROM REG BIT | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| 0x00 | Observation | 7 | Reserved | R/W | 0x00 | | Set bit to 0 |
| | | 6:3 | Address Bit AD[3:0] | R | | | Observation of AD[3:0] bits<br>[6]: AD3<br>[5]: AD2<br>[4]: AD1<br>[3]: AD0 |
| | | 2 | EEPROM Read Done | R | | | 1 = Device completed the read from external EEPROM |
| | | 1 | Reserved | R/W | | | Set bit to 0 |
| | | 0 | Reserved | R/W | | | Set bit to 0 |
| 0x01 | PWDN Channels | 7:0 | PWDN CHx | R/W | 0x00 | Yes | Power Down per Channel<br>[7]: CH7 – CHA_3<br>[6]: CH6 – CHA_2<br>[5]: CH5 – CHA_1<br>[4]: CH4 – CHA_0<br>[3]: CH3 – CHB_3<br>[2]: CH2 – CHB_2<br>[1]: CH1 – CHB_1<br>[0]: CH0 – CHB_0<br>0x00 = all channels enabled<br>0xFF = all channels disabled<br>Note: Override PWDN pin and enable register control through Reg 0x02[0] |
| 0x02 | Override RESET | 7 | Reserved | R/W | 0x00 | | Set bit to 0 |
| | | 6 | Reserved | | | | Set bit to 0 |
| | | 5:2 | Reserved | | | Yes | Set bits to 0 |
| | | 1 | Reserved | | | | Set bit to 0 |
| | | 0 | Override RESET | | | Yes | 1 = Block RESET pin control (Register control enabled)<br>0 = Allow RESET pin control (Register control disabled) |
| 0x03 | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x04 | Reserved | 7:0 | Reserved | R/W | 0x00 | Yes | Set bits to 0 |
| 0x05 | Reserved | 7:0 | Reserved | R/W | 0x00 | | Reserved |
| 0x06 | Slave Register Control | 7:5 | Reserved | R/W | 0x10 | | Set bits to 0 |
| | | 4 | Reserved | | | Yes | Set bit to 1 |
| | | 3 | Register Enable | | | | 1 = Enable SMBus Slave Mode Register Control<br>0 = Disable SMBus Slave Mode Register Control<br>**Note: In order to change VOD, DEM, and EQ of the channels in slave mode, this bit must be set to 1.** |
| | | 2:0 | Reserved | | | | Set bits to 0 |

**Table 6. SMbus Register Description Table (continued)**

| ADDRESS | REGISTER NAME | BIT | FIELD | TYPE | DEFAULT | EEPROM REG BIT | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| 0x07 | Digital Reset and Control | 7 | Reserved | R/W | 0x01 | | Set bit to 0 |
| | | 6 | Reset Registers | | | | 1 = Self clearing reset for SMBus registers (register settings return to default values) |
| | | 5 | Reserved | | | | Set bit to 0 |
| | | 4:0 | Reserved | | | | Set bits to 0 0001'b |
| 0x08 | Override Pin Control | 7 | Reserved | R/W | 0x00 | | Set bit to 0 |
| | | 6 | Override SD_TH | | | Yes | 1 = Block SD_TH pin control (Register control enabled)<br>0 = Allow SD_TH pin control (Register control disabled) |
| | | 5:2 | Reserved | | | Yes | Set bits to 0 |
| | | 1 | Override DEM | | | Yes | 1 = Block DEM pin control (Register control enabled)<br>0 = Allow DEM pin control (Register control disabled) |
| | | 0 | Reserved | | | Yes | Set bit to 0 |
| 0x09-0x0A | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x0B | Reserved | 7 | Reserved | R/W | 0x00 | | Set bit to 0 |
| | | 6:0 | Reserved | R/W | 0x70 | Yes | Set bits to 111 0000'b |
| 0x0C-0x0D | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x0E | Reserved | 7:6 | Reserved | R/W | 0x00 | | Set bits to 0 |
| | | 5:4 | Reserved | | | Yes | Set bits to 0 |
| | | 3:2 | Reserved | | | Yes | Set bits to 0 |
| | | 1:0 | Reserved | | | | Set bits to 0 |
| 0x0F | CH0 - CHB_0 EQ | 7:0 | EQ Control | R/W | 0x2F | Yes | INB_0 EQ Control - total of 256 levels.<br>See . |
| 0x10 | CH0 - CHB_0 VOD | 7 | Short Circuit Protection | R/W | 0xAD | Yes | 1 = Enable the short circuit protection<br>0 = Disable the short circuit protection |
| | | 6:3 | Reserved | | | Yes | Set bits to 0101'b |
| | | 2:0 | VOD Control | | | Yes | OUTB_0 VOD Control:<br>000'b = 0.7 V<br>001'b = 0.8 V<br>010'b = 0.9 V<br>011'b = 1.0 V<br>100'b = 1.1 V<br>101'b = 1.2 V (default)<br>110'b = 1.3 V<br>111'b = 1.4 V |

**Table 6. SMbus Register Description Table (continued)**

| ADDRESS | REGISTER NAME | BIT | FIELD | TYPE | DEFAULT | EEPROM REG BIT | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| 0x11 | CH0 - CHB_0 DEM | 7 | Reserved | R | 0x02 | | Set bit to 0 |
| | | 6:5 | Reserved | | | | Set bits to 0 |
| | | 4:3 | Reserved | R/W | | | Set bits to 0 |
| | | 2:0 | DEM Control | | | Yes | OUTB_0 DEM Control<br>000'b = 0 dB<br>001'b = –1.5 dB<br>010'b = –3.5 dB (default)<br>011'b = –5 dB<br>100'b = –6 dB<br>101'b = –8 dB<br>110'b = –9 dB<br>111'b = –12 dB |
| 0x12 | CH0 - CHB_0 SD_TH | 7 | Reserved | R/W | 0x00 | Yes | Set bit to 0 |
| | | 6:4 | Reserved | | | | Set bits to 0 |
| | | 3:2 | Signal Detect Status Assert Threshold | | | Yes | Status Assert threshold<br>00'b = 180 mVp-p (default)<br>01'b = 160 mVp-p<br>10'b = 210 mVp-p<br>11'b = 190 mVp-p<br>Note: Override SD_TH pin and enable register control through Reg 0x08[6] |
| | | 1:0 | Signal Detect Status Deassert Threshold | | | Yes | Status Deassert threshold<br>00'b = 110 mVp-p (default)<br>01'b = 100 mVp-p<br>10'b = 150 mVp-p<br>11'b = 130 mVp-p<br>Note: Override SD_TH pin and enable register control through Reg 0x08[6] |
| 0x13-0x14 | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x15 | Reserved | 7:6 | Reserved | R/W | 0x00 | | Set bits to 0 |
| | | 5:4 | Reserved | | | Yes | Set bits to 0 |
| | | 3:2 | Reserved | | | Yes | Set bits to 0 |
| | | 1:0 | Reserved | | | | Set bits to 0 |
| 0x16 | CH1 - CHB_1 EQ | 7:0 | EQ Control | R/W | 0x2F | Yes | INB_1 EQ Control - total of 256 levels.<br>See . |

**Table 6. SMbus Register Description Table (continued)**

| ADDRESS | REGISTER NAME | BIT | FIELD | TYPE | DEFAULT | EEPROM REG BIT | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| 0x17 | CH1 - CHB_1 VOD | 7 | Short Circuit Protection | R/W | 0xAD | Yes | 1 = Enable the short circuit protection<br>0 = Disable the short circuit protection |
| | | 6:3 | Reserved | | | Yes | Set bits to 0101'b |
| | | 2:0 | VOD Control | | | Yes | OUTB_1 VOD Control:<br>000'b = 0.7 V<br>001'b = 0.8 V<br>010'b = 0.9 V<br>011'b = 1.0 V<br>100'b = 1.1 V<br>101'b = 1.2 V (default)<br>110'b = 1.3 V<br>111'b = 1.4 V |
| 0x18 | CH1 - CHB_1 DEM | 7 | Reserved | R | 0x02 | | Set bit to 0 |
| | | 6:5 | Reserved | | | | Set bits to 0 |
| | | 4:3 | Reserved | R/W | | | Set bits to 0 |
| | | 2:0 | DEM Control | | | Yes | OUTB_1 DEM Control<br>000'b = 0 dB<br>001'b = –1.5 dB<br>010'b = –3.5 dB (default)<br>011'b = –5 dB<br>100'b = –6 dB<br>101'b = –8 dB<br>110'b = –9 dB<br>111'b = –12 dB |
| 0x19 | CH1 - CHB_1 SD_TH | 7 | Reserved | R/W | 0x00 | Yes | Set bit to 0 |
| | | 6:4 | Reserved | | | | Set bits to 0 |
| | | 3:2 | Signal Detect Status Assert Threshold | | | Yes | Status Assert threshold<br>00'b = 180 mVp-p (default)<br>01'b = 160 mVp-p<br>10'b = 210 mVp-p<br>11'b = 190 mVp-p<br>Note: Override SD_TH pin and enable register control through Reg 0x08[6] |
| | | 1:0 | Signal Detect Status Deassert Threshold | | | Yes | Status Deassert threshold<br>00'b = 110 mVp-p (default)<br>01'b = 100 mVp-p<br>10'b = 150 mVp-p<br>11'b = 130 mVp-p<br>Note: Override SD_TH pin and enable register control through Reg 0x08[6] |
| 0x1A-0x1B | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |

**Table 6. SMbus Register Description Table (continued)**

| ADDRESS | REGISTER NAME | BIT | FIELD | TYPE | DEFAULT | EEPROM REG BIT | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| 0x1C | Reserved | 7:6 | Reserved | R/W | 0x00 | | Set bits to 0 |
| | | 5:4 | Reserved | | | Yes | Set bits to 0 |
| | | 3:2 | Reserved | | | Yes | Set bits to 0 |
| | | 1:0 | Reserved | | | | Set bits to 0 |
| 0x1D | CH2 - CHB_2 EQ | 7:0 | EQ Control | R/W | 0x2F | Yes | INB_2 EQ Control - total of four levels.<br>See . |
| 0x1E | CH2 - CHB_2 VOD | 7 | Short Circuit Protection | R/W | 0xAD | Yes | 1 = Enable the short circuit protection<br>0 = Disable the short circuit protection |
| | | 6:3 | Reserved | | | Yes | Set bits to 0101'b |
| | | 2:0 | VOD Control | | | Yes | OUTB_2 VOD Control:<br>000'b = 0.7 V<br>001'b = 0.8 V<br>010'b = 0.9 V<br>011'b = 1.0 V<br>100'b = 1.1 V<br>101'b = 1.2 V (default)<br>110'b = 1.3 V<br>111'b = 1.4 V |
| 0x1F | CH2 - CHB_2 DEM | 7 | Reserved | R | 0x02 | | Set bit to 0 |
| | | 6:5 | Reserved | | | | Set bits to 0 |
| | | 4:3 | Reserved | R/W | | | Set bits to 0 |
| | | 2:0 | DEM Control | | | Yes | OUTB_2 DEM Control<br>000'b = 0 dB<br>001'b = –1.5 dB<br>010'b = –3.5 dB (default)<br>011'b = –5 dB<br>100'b = –6 dB<br>101'b = –8 dB<br>110'b = –9 dB<br>111'b = –12 dB |

**Table 6. SMbus Register Description Table (continued)**

| ADDRESS | REGISTER NAME | BIT | FIELD | TYPE | DEFAULT | EEPROM REG BIT | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| 0x20 | CH2 - CHB_2 SD_TH | 7 | Reserved | R/W | 0x00 | Yes | Set bit to 0 |
| | | 6:4 | Reserved | | | | Set bits to 0 |
| | | 3:2 | Signal Detect Status Assert Threshold | | | Yes | Status Assert threshold<br>00'b = 180 mVp-p (default)<br>01'b = 160 mVp-p<br>10'b = 210 mVp-p<br>11'b = 190 mVp-p<br>Note: Override SD_TH pin and enable register control through Reg 0x08[6] |
| | | 1:0 | Signal Detect Status Deassert Threshold | | | Yes | Status Deassert threshold<br>00'b = 110 mVp-p (default)<br>01'b = 100 mVp-p<br>10'b = 150 mVp-p<br>11'b = 130 mVp-p<br>Note: Override SD_TH pin and enable register control through Reg 0x08[6] |
| 0x21-0x22 | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x23 | Reserved | 7:6 | Reserved | R/W | 0x00 | | Set bits to 0 |
| | | 5:4 | Reserved | | | Yes | Set bits to 0 |
| | | 3:2 | Reserved | | | Yes | Set bits to 0 |
| | | 1:0 | Reserved | | | | Set bits to 0 |
| 0x24 | CH3 - CHB_3 EQ | 7:0 | EQ Control | R/W | 0x2F | Yes | INB_3 EQ Control - total of 256 levels.<br>See . |
| 0x25 | CH3 - CHB_3 VOD | 7 | Short Circuit Protection | R/W | 0xAD | Yes | 1 = Enable the short circuit protection<br>0 = Disable the short circuit protection |
| | | 6:3 | Reserved | | | Yes | Set bits to 0101'b |
| | | 2:0 | VOD Control | | | Yes | OUTB_3 VOD Control:<br>000'b = 0.7 V<br>001'b = 0.8 V<br>010'b = 0.9 V<br>011'b = 1.0 V<br>100'b = 1.1 V<br>101'b = 1.2 V (default)<br>110'b = 1.3 V<br>111'b = 1.4 V |

**Table 6. SMbus Register Description Table (continued)**

| ADDRESS | REGISTER NAME | BIT | FIELD | TYPE | DEFAULT | EEPROM REG BIT | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| 0x26 | CH3 - CHB_3 DEM | 7 | Reserved | R | 0x02 | | Set bit to 0 |
| | | 6:5 | Reserved | | | | Set bits to 0 |
| | | 4:3 | Reserved | R/W | | | Set bits to 0 |
| | | 2:0 | DEM Control | | | Yes | OUTB_3 DEM Control<br>000'b = 0 dB<br>001'b = –1.5 dB<br>010'b = –3.5 dB (default)<br>011'b = –5 dB<br>100'b = –6 dB<br>101'b = –8 dB<br>110'b = –9 dB<br>111'b = –12 dB |
| 0x27 | CH3 - CHB_3 SD_TH | 7 | Reserved | R/W | 0x00 | Yes | Set bit to 0 |
| | | 6:4 | Reserved | | | | Set bits to 0 |
| | | 3:2 | Signal Detect Status Assert Threshold | | | Yes | Status Assert threshold<br>00'b = 180 mVp-p (default)<br>01'b = 160 mVp-p<br>10'b = 210 mVp-p<br>11'b = 190 mVp-p<br>Note: Override SD_TH pin and enable register control through Reg 0x08[6] |
| | | 1:0 | Signal Detect Status Deassert Threshold | | | Yes | Status Deassert threshold<br>00'b = 110 mVp-p (default)<br>01'b = 100 mVp-p<br>10'b = 150 mVp-p<br>11'b = 130 mVp-p<br>Note: Override SD_TH pin and enable register control through Reg 0x08[6] |
| 0x28 | Signal Detect Status Control | 7 | Reserved | R/W | 0x0C | | Set bit to 0 |
| | | 6 | Override Fast Signal Detect | | | Yes | Set bit to 0 |
| | | 5:4 | High SD_TH Status | | | Yes | Enable Higher Range of Signal Detect Status Thresholds<br>[5]: CH0 - CH3<br>[4]: CH4 - CH7 |
| | | 3:2 | Fast Signal Detect Status | | | Yes | Enable Fast Signal Detect Status<br>[3]: CH0 - CH3<br>[2]: CH4 - CH7<br>Note: In Fast Signal Detect, assert/deassert response occurs after approximately 3-4 ns |
| | | 1:0 | Reduced SD Status Gain | | | Yes | Enable Reduced Signal Detect Status Gain<br>[1]: CH0 - CH3<br>[0]: CH4 - CH7 |
| 0x29-0x2A | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |

**Table 6. SMbus Register Description Table (continued)**

| ADDRESS | REGISTER NAME | BIT | FIELD | TYPE | DEFAULT | EEPROM REG BIT | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| 0x2B | Reserved | 7:6 | Reserved | R/W | 0x00 | | Set bits to 0 |
| | | 5:4 | Reserved | | | Yes | Set bits to 0 |
| | | 3:2 | Reserved | | | Yes | Set bits to 0 |
| | | 1:0 | Reserved | | | | Set bits to 0 |
| 0x2C | CH4 - CHA_0 EQ | 7:0 | EQ Control | R/W | 0x2F | Yes | INA_0 EQ Control - total of 256 levels.<br>See . |
| 0x2D | CH4 - CHA_0 VOD | 7 | Short Circuit Protection | R/W | 0xAD | Yes | 1 = Enable the short circuit protection<br>0 = Disable the short circuit protection |
| | | 6:3 | Reserved | | | Yes | Set bits to 0101'b |
| | | 2:0 | VOD Control | | | Yes | OUTA_0 VOD Control:<br>000'b = 0.7 V<br>001'b = 0.8 V<br>010'b = 0.9 V<br>011'b = 1.0 V<br>100'b = 1.1 V<br>101'b = 1.2 V (default)<br>110'b = 1.3 V<br>111'b = 1.4 V |
| 0x2E | CH4 - CHA_0 DEM | 7 | Reserved | R | 0x02 | | Set bit to 0 |
| | | 6:5 | Reserved | | | | Set bits to 0 |
| | | 4:3 | Reserved | R/W | | | Set bits to 0 |
| | | 2:0 | DEM Control | | | Yes | OUTA_0 DEM Control<br>000'b = 0 dB<br>001'b = –1.5 dB<br>010'b = –3.5 dB (default)<br>011'b = –5 dB<br>100'b = –6 dB<br>101'b = –8 dB<br>110'b = –9 dB<br>111'b = –12 dB |

**Table 6. SMbus Register Description Table (continued)**

| ADDRESS | REGISTER NAME | BIT | FIELD | TYPE | DEFAULT | EEPROM REG BIT | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| 0x2F | CH4 - CHA_0 SD_TH | 7 | Reserved | R/W | 0x00 | Yes | Set bit to 0 |
| | | 6:4 | Reserved | | | | Set bits to 0 |
| | | 3:2 | Signal Detect Status Assert Threshold | | | Yes | Status Assert threshold<br>00'b = 180 mVp-p (default)<br>01'b = 160 mVp-p<br>10'b = 210 mVp-p<br>11'b = 190 mVp-p<br>Note: Override SD_TH pin and enable register control through Reg 0x08[6] |
| | | 1:0 | Signal Detect Status Deassert Threshold | | | Yes | Status Deassert threshold<br>00'b = 110 mVp-p (default)<br>01'b = 100 mVp-p<br>10'b = 150 mVp-p<br>11'b = 130 mVp-p<br>Note: Override SD_TH pin and enable register control through Reg 0x08[6] |
| 0x30-0x31 | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x32 | Reserved | 7:6 | Reserved | R/W | 0x00 | | Set bits to 0 |
| | | 5:4 | Reserved | | | Yes | Set bits to 0 |
| | | 3:2 | Reserved | | | Yes | Set bits to 0 |
| | | 1:0 | Reserved | | | | Set bits to 0 |
| 0x33 | CH5 - CHA_1 EQ | 7:0 | EQ Control | R/W | 0x2F | Yes | INA_1 EQ Control - total of 256 levels.<br>See . |
| 0x34 | CH5 - CHA_1 VOD | 7 | Short Circuit Protection | R/W | 0xAD | Yes | 1 = Enable the short circuit protection<br>0 = Disable the short circuit protection |
| | | 6:3 | Reserved | | | Yes | Set bits to 0101'b |
| | | 2:0 | VOD Control | | | Yes | OUTA_1 VOD Control:<br>000'b = 0.7 V<br>001'b = 0.8 V<br>010'b = 0.9 V<br>011'b = 1.0 V<br>100'b = 1.1 V<br>101'b = 1.2 V (default)<br>110'b = 1.3 V<br>111'b = 1.4 V |

**Table 6. SMbus Register Description Table (continued)**

| ADDRESS | REGISTER NAME | BIT | FIELD | TYPE | DEFAULT | EEPROM REG BIT | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| 0x35 | CH5 - CHA_1 DEM | 7 | Reserved | R | 0x02 | | Set bit to 0 |
| | | 6:5 | Reserved | | | | Set bits to 0 |
| | | 4:3 | Reserved | R/W | | | Set bits to 0 |
| | | 2:0 | DEM Control | | | Yes | OUTA_1 DEM Control<br>000'b = 0 dB<br>001'b = –1.5 dB<br>010'b = –3.5 dB (default)<br>011'b = –5 dB<br>100'b = –6 dB<br>101'b = –8 dB<br>110'b = –9 dB<br>111'b = –12 dB |
| 0x36 | CH5 - CHA_1 SD_TH | 7 | Reserved | R/W | 0x00 | Yes | Set bit to 0 |
| | | 6:4 | Reserved | | | | Set bits to 0 |
| | | 3:2 | Signal Detect Status Assert Threshold | | | Yes | Status Assert threshold<br>00'b = 180 mVp-p (default)<br>01'b = 160 mVp-p<br>10'b = 210 mVp-p<br>11'b = 190 mVp-p<br>Note: Override SD_TH pin and enable register control through Reg 0x08[6] |
| | | 1:0 | Signal Detect Status Deassert Threshold | | | Yes | Status Deassert threshold<br>00'b = 110 mVp-p (default)<br>01'b = 100 mVp-p<br>10'b = 150 mVp-p<br>11'b = 130 mVp-p<br>Note: Override SD_TH pin and enable register control through Reg 0x08[6] |
| 0x37-0x38 | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x39 | Reserved | 7:6 | Reserved | R/W | 0x00 | | Set bits to 0 |
| | | 5:4 | Reserved | | | Yes | Set bits to 0 |
| | | 3:2 | Reserved | | | Yes | Set bits to 0 |
| | | 1:0 | Reserved | | | | Set bits to 0 |
| 0x3A | CH6 - CHA_2 EQ | 7:0 | EQ Control | R/W | 0x2F | Yes | INA_2 EQ Control - total of 256 levels.<br>See . |

**Table 6. SMbus Register Description Table (continued)**

| ADDRESS | REGISTER NAME | BIT | FIELD | TYPE | DEFAULT | EEPROM REG BIT | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| 0x3B | CH6 - CHA_2 VOD | 7 | Short Circuit Protection | R/W | 0xAD | Yes | 1 = Enable the short circuit protection<br>0 = Disable the short circuit protection |
| | | 6:3 | Reserved | | | Yes | Set bits to 0101'b |
| | | 2:0 | VOD Control | | | Yes | OUTA_2 VOD Control: VOD / VID Ratio<br>000'b = 0.7 V<br>001'b = 0.8 V<br>010'b = 0.9 V<br>011'b = 1.0 V<br>100'b = 1.1 V<br>101'b = 1.2 V (default)<br>110'b = 1.3 V<br>111'b = 1.4 V |
| 0x3C | CH6 - CHA_2 DEM | 7 | Reserved | R | 0x02 | | Set bit to 0 |
| | | 6:5 | Reserved | | | | Set bits to 0 |
| | | 4:3 | Reserved | R/W | | | Set bits to 0 |
| | | 2:0 | DEM Control | | | Yes | OUTA_2 DEM Control<br>000'b = 0 dB<br>001'b = –1.5 dB<br>010'b = –3.5 dB (default)<br>011'b = –5 dB<br>100'b = –6 dB<br>101'b = –8 dB<br>110'b = –9 dB<br>111'b = –12 dB |
| 0x3D | CH6 - CHA_2 SD_TH | 7 | Reserved | R/W | 0x00 | Yes | Set bit to 0 |
| | | 6:4 | Reserved | | | | Set bits to 0 |
| | | 3:2 | Signal Detect Status Assert Threshold | | | Yes | Status Assert threshold<br>00'b = 180 mVp-p (default)<br>01'b = 160 mVp-p<br>10'b = 210 mVp-p<br>11'b = 190 mVp-p<br>Note: Override SD_TH pin and enable register control through Reg 0x08[6] |
| | | 1:0 | Signal Detect Status Deassert Threshold | | | Yes | Status Deassert threshold<br>00'b = 110 mVp-p (default)<br>01'b = 100 mVp-p<br>10'b = 150 mVp-p<br>11'b = 130 mVp-p<br>Note: Override SD_TH pin and enable register control through Reg 0x08[6] |
| 0x3E-0x3F | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |

**Table 6. SMbus Register Description Table (continued)**

| ADDRESS | REGISTER NAME | BIT | FIELD | TYPE | DEFAULT | EEPROM REG BIT | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| 0x40 | Reserved | 7:6 | Reserved | R/W | 0x00 | | Set bits to 0 |
| | | 5:4 | Reserved | | | Yes | Set bits to 0 |
| | | 3:2 | Reserved | | | Yes | Set bits to 0 |
| | | 1:0 | Reserved | | | | Set bits to 0 |
| 0x41 | CH7 - CHA_3 EQ | 7:0 | EQ Control | R/W | 0x2F | Yes | INA_3 EQ Control - total of 256 levels.<br>See . |
| 0x42 | CH7 - CHA_3 VOD | 7 | Short Circuit Protection | R/W | 0xAD | Yes | 1 = Enable the short circuit protection<br>0 = Disable the short circuit protection |
| | | 6:3 | Reserved | | | Yes | Set bits to 0101'b |
| | | 2:0 | VOD Control | | | Yes | OUTA_3 VOD Control:<br>000'b = 0.7 V<br>001'b = 0.8 V<br>010'b = 0.9 V<br>011'b = 1.0 V<br>100'b = 1.1 V<br>101'b = 1.2 V (default)<br>110'b = 1.3 V<br>111'b = 1.4 V |
| 0x43 | CH7 - CHA_3 DEM | 7 | Reserved | R | 0x02 | | Set bit to 0 |
| | | 6:5 | Reserved | | | | Set bits to 0 |
| | | 4:3 | Reserved | R/W | | | Set bits to 0 |
| | | 2:0 | DEM Control | | | Yes | OUTA_3 DEM Control<br>000'b = 0 dB<br>001'b = –1.5 dB<br>010'b = –3.5 dB (default)<br>011'b = –5 dB<br>100'b = –6 dB<br>101'b = –8 dB<br>110'b = –9 dB<br>111'b = –12 dB |

**Table 6. SMbus Register Description Table (continued)**

| ADDRESS | REGISTER NAME | BIT | FIELD | TYPE | DEFAULT | EEPROM REG BIT | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| 0x44 | CH7 - CHA_3 SD_TH | 7 | Reserved | R/W | 0x00 | Yes | Set bit to 0 |
| | | 6:4 | Reserved | | | | Set bits to 0 |
| | | 3:2 | Signal Detect Status Assert Threshold | | | Yes | Status Assert threshold<br>00'b = 180 mVp-p (default)<br>01'b = 160 mVp-p<br>10'b = 210 mVp-p<br>11'b = 190 mVp-p<br>Note: Override SD_TH pin and enable register control through Reg 0x08[6] |
| | | 1:0 | Signal Detect Status Deassert Threshold | | | Yes | Status Deassert threshold<br>00'b = 110 mVp-p (default)<br>01'b = 100 mVp-p<br>10'b = 150 mVp-p<br>11'b = 130 mVp-p<br>Note: Override SD_TH pin and enable register control through Reg 0x08[6] |
| 0x45 | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x46 | Reserved | 7:0 | Reserved | R/W | 0x38 | | Set bits to 0x38 |
| 0x47 | Reserved | 7:4 | Reserved | R/W | 0x00 | | Set bits to 0 |
| | | 3:0 | Reserved | | | Yes | Set bits to 0 |
| 0x48 | Reserved | 7:6 | Reserved | R/W | 0x05 | Yes | Set bits to 0 |
| | | 5:0 | Reserved | R/W | | | Set bits to 00 0101'b |
| 0x49-0x4B | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x4C | Reserved | 7:3 | Reserved | R/W | 0x00 | Yes | Set bits to 0 |
| | | 2:1 | Reserved | R/W | | | Set bits to 0 |
| | | 0 | Reserved | R/W | | Yes | Set bits to 0 |
| 0x4D-0x50 | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x51 | Device ID | 7:5 | VERSION | R | 0x45 | | 010'b |
| | | 4:0 | ID | | | | 0 0101'b |
| 0x52-0x55 | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |
| 0x56 | Reserved | 7:0 | Reserved | R/W | 0x10 | | Set bits to 0x10 |
| 0x57 | Reserved | 7:0 | Reserved | R/W | 0x64 | | Set bits to 0x64 |
| 0x58 | Reserved | 7:0 | Reserved | R/W | 0x21 | | Set bits to 0x21 |
| 0x59 | Reserved | 7:1 | Reserved | R/W | 0x00 | | Set bits to 0 |
| | | 0 | Reserved | | | Yes | Set bit to 0 |
| 0x5A | Reserved | 7:0 | Reserved | R/W | 0x54 | Yes | Set bits to 0x54 |
| 0x5B | Reserved | 7:0 | Reserved | R/W | 0x54 | Yes | Set bits to 0x54 |
| 0x5C-0x61 | Reserved | 7:0 | Reserved | R/W | 0x00 | | Set bits to 0 |

**Table 7. EEPROM Register Map - Single Device With Default Value**

| EEPROM ADDRESS BYTE | | | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Description | | 0x00 | CRC_EN | Address Map Present | EEPROM > 256 Bytes | Reserved | DEVICE COUNT[3] | DEVICE COUNT[2] | DEVICE COUNT[1] | DEVICE COUNT[0] |
| Default Value | 0x00 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | | 0x01 | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| Default Value | 0x00 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | | 0x02 | Max EEPROM Burst size[7] | Max EEPROM Burst size[6] | Max EEPROM Burst size[5] | Max EEPROM Burst size[4] | Max EEPROM Burst size[3] | Max EEPROM Burst size[2] | Max EEPROM Burst size[1] | Max EEPROM Burst size[0] |
| Default Value | 0x00 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | | 0x03 | PWDN_CH7 | PWDN_CH6 | PWDN_CH5 | PWDN_CH4 | PWDN_CH3 | PWDN_CH2 | PWDN_CH1 | PWDN_CH0 |
| SMBus Register | | | 0x01[7] | 0x01[6] | 0x01[5] | 0x01[4] | 0x01[3] | 0x01[2] | 0x01[1] | 0x01[0] |
| Default Value | 0x00 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | | 0x04 | Reserved | Reserved | Reserved | Reserved | Ovrd_RESET | Reserved | Reserved | Reserved |
| SMBus Register | | | 0x02[5] | 0x02[4] | 0x02[3] | 0x02[2] | 0x02[0] | 0x04[7] | 0x04[6] | 0x04[5] |
| Default Value | 0x00 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | | 0x05 | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Ovrd_SD_TH | Reserved |
| SMBus Register | | | 0x04[4] | 0x04[3] | 0x04[2] | 0x04[1] | 0x04[0] | 0x06[4] | 0x08[6] | 0x08[5] |
| Default Value | 0x04 | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| Description | | 0x06 | Reserved | Reserved | Reserved | Ovrd_DEM | Reserved | Reserved | Reserved | Reserved |
| SMBus Register | | | 0x08[4] | 0x08[3] | 0x08[2] | 0x08[1] | 0x08[0] | 0x0B[6] | 0x0B[5] | 0x0B[4] |
| Default Value | 0x07 | | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| Description | | 0x07 | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| SMBus Register | | | 0x0B[3] | 0x0B[2] | 0x0B[1] | 0x0B[0] | 0x0E[5] | 0x0E[4] | 0x0E[3] | 0x0E[2] |
| Default Value | 0x00 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | | 0x08 | CH0_EQ_7 | CH0_EQ_6 | CH0_EQ_5 | CH0_EQ_4 | CH0_EQ_3 | CH0_EQ_2 | CH0_EQ_1 | CH0_EQ_0 |
| SMBus Register | | | 0x0F[7] | 0x0F[6] | 0x0F[5] | 0x0F[4] | 0x0F[3] | 0x0F[2] | 0x0F[1] | 0x0F[0] |
| Default Value | 0x2F | | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |

**Table 7. EEPROM Register Map - Single Device With Default Value (continued)**

| EEPROM ADDRESS BYTE | | | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Description | | 0x09 | CH0_SCP | Reserved | Reserved | Reserved | Reserved | CH0_VOD_2 | CH0_VOD_1 | CH0_VOD_0 |
| SMBus Register | | | 0x10[7] | 0x10[6] | 0x10[5] | 0x10[4] | 0x10[3] | 0x10[2] | 0x10[1] | 0x10[0] |
| Default Value | 0xAD | | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| Description | | 0x0A | CH0_DEM_2 | CH0_DEM_1 | CH0_DEM_0 | Reserved | CH0_THa_1 | CH0_THa_0 | CH0_THd_1 | CH0_THd_0 |
| SMBus Register | | | 0x11[2] | 0x11[1] | 0x11[0] | 0x12[7] | 0x12[3] | 0x12[2] | 0x12[1] | 0x12[0] |
| Default Value | 0x40 | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | | 0x0B | Reserved | Reserved | Reserved | Reserved | CH1_EQ_7 | CH1_EQ_6 | CH1_EQ_5 | CH1_EQ_4 |
| SMBus Register | | | 0x15[5] | 0x15[4] | 0x15[3] | 0x15[2] | 0x16[7] | 0x16[6] | 0x16[5] | 0x16[4] |
| Default Value | 0x02 | | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| Description | | 0x0C | CH1_EQ_3 | CH1_EQ_2 | CH1_EQ_1 | CH1_EQ_0 | CH1_SCP | Reserved | Reserved | Reserved |
| SMBus Register | | | 0x16[3] | 0x16[2] | 0x16[1] | 0x16[0] | 0x17[7] | 0x17[6] | 0x17[5] | 0x17[4] |
| Default Value | 0xFA | | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| Description | | 0x0D | Reserved | CH1_VOD_2 | CH1_VOD_1 | CH1_VOD_0 | CH1_DEM_2 | CH1_DEM_1 | CH1_DEM_0 | Reserved |
| SMBus Register | | | 0x17[3] | 0x17[2] | 0x17[1] | 0x17[0] | 0x18[2] | 0x18[1] | 0x18[0] | 0x19[7] |
| Default Value | 0xD4 | | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| Description | | 0x0E | CH1_THa_1 | CH1_THa_0 | CH1_THd_1 | CH1_THd_0 | Reserved | Reserved | Reserved | Reserved |
| SMBus Register | | | 0x19[3] | 0x19[2] | 0x19[1] | 0x19[0] | 0x1C[5] | 0x1C[4] | 0x1C[3] | 0x1C[2] |
| Default Value | 0x00 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | | 0x0F | CH2_EQ_7 | CH2_EQ_6 | CH2_EQ_5 | CH2_EQ_4 | CH2_EQ_3 | CH2_EQ_2 | CH2_EQ_1 | CH2_EQ_0 |
| SMBus Register | | | 0x1D[7] | 0x1D[6] | 0x1D[5] | 0x1D[4] | 0x1D[3] | 0x1D[2] | 0x1D[1] | 0x1D[0] |
| Default Value | 0x2F | | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| Description | | 0x10 | CH2_SCP | Reserved | Reserved | Reserved | Reserved | CH2_VOD_2 | CH2_VOD_1 | CH2_VOD_0 |
| SMBus Register | | | 0x1E[7] | 0x1E[6] | 0x1E[5] | 0x1E[4] | 0x1E[3] | 0x1E[2] | 0x1E[1] | 0x1E[0] |
| Default Value | 0xAD | | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| Description | | 0x11 | CH2_DEM_2 | CH2_DEM_1 | CH2_DEM_0 | Reserved | CH2_THa_1 | CH2_THa_0 | CH2_THd_1 | CH2_THd_0 |
| SMBus Register | | | 0x1F[2] | 0x1F[1] | 0x1F[0] | 0x20[7] | 0x20[3] | 0x20[2] | 0x20[1] | 0x20[0] |
| Default Value | 0x40 | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 7. EEPROM Register Map - Single Device With Default Value (continued)**

| EEPROM ADDRESS BYTE | | | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Description | | 0x12 | Reserved | Reserved | Reserved | Reserved | CH3_EQ_7 | CH3_EQ_6 | CH3_EQ_5 | CH3_EQ_4 |
| SMBus Register | | | 0x23[5] | 0x23[4] | 0x23[3] | 0x23[2] | 0x24[7] | 0x24[6] | 0x24[5] | 0x24[4] |
| Default Value | 0x02 | | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| Description | | 0x13 | CH3_EQ_3 | CH3_EQ_2 | CH3_EQ_1 | CH3_EQ_0 | CH3_SCP | Reserved | Reserved | Reserved |
| SMBus Register | | | 0x24[3] | 0x24[2] | 0x24[1] | 0x24[0] | 0x25[7] | 0x25[6] | 0x25[5] | 0x25[4] |
| Default Value | 0xFA | | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| Description | | 0x14 | Reserved | CH3_VOD_2 | CH3_VOD_1 | CH3_VOD_0 | CH3_DEM_2 | CH3_DEM_1 | CH3_DEM_0 | Reserved |
| SMBus Register | | | 0x25[3] | 0x25[2] | 0x25[1] | 0x25[0] | 0x26[2] | 0x26[1] | 0x26[0] | 0x27[7] |
| Default Value | 0xD4 | | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| Description | | 0x15 | CH3_THa_1 | CH3_THa_0 | CH3_THd_1 | CH3_THd_0 | ovrd_fast_SD | hi_idle_SD CH0-3 | hi_idle_SD CH4-7 | fast_SD CH0-3 |
| SMBus Register | | | 0x27[3] | 0x27[2] | 0x27[1] | 0x27[0] | 0x28[6] | 0x28[5] | 0x28[4] | 0x28[3] |
| Default Value | 0x01 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Description | | 0x16 | fast_SD CH4-7 | lo_gain_SD CH0-3 | lo_gain_SD CH4-7 | Reserved | Reserved | Reserved | Reserved | CH4_EQ_7 |
| SMBus Register | | | 0x28[2] | 0x28[1] | 0x28[0] | 0x2B[5] | 0x2B[4] | 0x2B[3] | 0x2B[2] | 0x2C[7] |
| Default Value | 0x80 | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | | 0x17 | CH4_EQ_6 | CH4_EQ_5 | CH4_EQ_4 | CH4_EQ_3 | CH4_EQ_2 | CH4_EQ_1 | CH4_EQ_0 | CH4_SCP |
| SMBus Register | | | 0x2C[6] | 0x2C[5] | 0x2C[4] | 0x2C[3] | 0x2C[2] | 0x2C[1] | 0x2C[0] | 0x2D[7] |
| Default Value | 0x5F | | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| Description | | 0x18 | Reserved | Reserved | Reserved | Reserved | CH4_VOD_2 | CH4_VOD_1 | CH4_VOD_0 | CH4_DEM_2 |
| SMBus Register | | | 0x2D[6] | 0x2D[5] | 0x2D[4] | 0x2D[3] | 0x2D[2] | 0x2D[1] | 0x2D[0] | 0x2E[2] |
| Default Value | 0x5A | | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| Description | | 0x19 | CH4_DEM_1 | CH4_DEM_0 | Reserved | CH4_THa_1 | CH4_THa_0 | CH4_THd_1 | CH4_THd_0 | Reserved |
| SMBus Register | | | 0x2E[1] | 0x2E[0] | 0x2F[7] | 0x2F[3] | 0x2F[2] | 0x2F[1] | 0x2F[0] | 0x32[5] |
| Default Value | 0x80 | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | | 0x1A | Reserved | Reserved | Reserved | CH5_EQ_7 | CH5_EQ_6 | CH5_EQ_5 | CH5_EQ_4 | CH5_EQ_3 |
| SMBus Register | | | 0x32[4] | 0x32[3] | 0x32[2] | 0x33[7] | 0x33[6] | 0x33[5] | 0x33[4] | 0x33[3] |
| Default Value | 0x05 | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

**Table 7. EEPROM Register Map - Single Device With Default Value (continued)**

| EEPROM ADDRESS BYTE | | | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Description | | 0x1B | CH5_EQ_2 | CH5_EQ_1 | CH5_EQ_0 | CH5_SCP | Reserved | Reserved | Reserved | Reserved |
| SMBus Register | | | 0x33[2] | 0x33[1] | 0x33[0] | 0x34[7] | 0x34[6] | 0x34[5] | 0x34[4] | 0x34[3] |
| Default Value | 0xF5 | | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| Description | | 0x1C | CH5_VOD_2 | CH5_VOD_1 | CH5_VOD_0 | CH5_DEM_2 | CH5_DEM_1 | CH5_DEM_0 | Reserved | CH5_THa_1 |
| SMBus Register | | | 0x34[2] | 0x34[1] | 0x34[0] | 0x35[2] | 0x35[1] | 0x35[0] | 0x36[7] | 0x36[3] |
| Default Value | 0xA8 | | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| Description | | 0x1D | CH5_THa_0 | CH5_THd_1 | CH5_THd_0 | Reserved | Reserved | Reserved | Reserved | CH6_EQ_7 |
| SMBus Register | | | 0x36[2] | 0x36[1] | 0x36[0] | 0x39[5] | 0x39[4] | 0x39[3] | 0x39[2] | 0x3A[7] |
| Default Value | 0x00 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | | 0x1E | CH6_EQ_6 | CH6_EQ_5 | CH6_EQ_4 | CH6_EQ_3 | CH6_EQ_2 | CH6_EQ_1 | CH6_EQ_0 | CH6_SCP |
| SMBus Register | | | 0x3A[6] | 0x3A[5] | 0x3A[4] | 0x3A[3] | 0x3A[2] | 0x3A[1] | 0x3A[0] | 0x3B[7] |
| Default Value | 0x5F | | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| Description | | 0x1F | Reserved | Reserved | Reserved | Reserved | CH6_VOD_2 | CH6_VOD_1 | CH6_VOD_0 | CH6_DEM_2 |
| SMBus Register | | | 0x3B[6] | 0x3B[5] | 0x3B[4] | 0x3B[3] | 0x3B[2] | 0x3B[1] | 0x3B[0] | 0x3C[2] |
| Default Value | 0x5A | | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| Description | | 0x20 | CH6_DEM_1 | CH6_DEM_0 | Reserved | CH6_THa_1 | CH6_THa_0 | CH6_THd_1 | CH6_THd_0 | Reserved |
| SMBus Register | | | 0x3C[1] | 0x3C[0] | 0x3D[7] | 0x3D[3] | 0x3D[2] | 0x3D[1] | 0x3D[0] | 0x40[5] |
| Default Value | 0x80 | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | | 0x21 | Reserved | Reserved | Reserved | CH7_EQ_7 | CH7_EQ_6 | CH7_EQ_5 | CH7_EQ_4 | CH7_EQ_3 |
| SMBus Register | | | 0x40[4] | 0x40[3] | 0x40[2] | 0x41[7] | 0x41[6] | 0x41[5] | 0x41[4] | 0x41[3] |
| Default Value | 0x05 | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| Description | | 0x22 | CH7_EQ_2 | CH7_EQ_1 | CH7_EQ_0 | CH7_SCP | Reserved | Reserved | Reserved | Reserved |
| SMBus Register | | | 0x41[2] | 0x41[1] | 0x41[0] | 0x42[7] | 0x42[6] | 0x42[5] | 0x42[4] | 0x42[3] |
| Default Value | 0xF5 | | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| Description | | 0x23 | CH7_VOD_2 | CH7_VOD_1 | CH7_VOD_0 | CH7_DEM_2 | CH7_DEM_1 | CH7_DEM_0 | Reserved | CH7_THa_1 |
| SMBus Register | | | 0x42[2] | 0x42[1] | 0x42[0] | 0x43[2] | 0x43[1] | 0x43[0] | 0x44[7] | 0x44[3] |
| Default Value | 0xA8 | | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |

**Table 7. EEPROM Register Map - Single Device With Default Value (continued)**

| EEPROM ADDRESS BYTE | | | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Description | | 0x24 | CH7_THa_0 | CH7_THd_1 | CH7_THd_0 | Reserved | Reserved | Reserved | Reserved | Reserved |
| SMBus Register | | | 0x44[2] | 0x44[1] | 0x44[0] | 0x47[3] | 0x47[2] | 0x47[1] | 0x47[0] | 0x48[7] |
| Default Value | 0x00 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | | 0x25 | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| SMBus Register | | | 0x48[6] | 0x4C[7] | 0x4C[6] | 0x4C[5] | 0x4C[4] | 0x4C[3] | 0x4C[0] | 0x59[0] |
| Default Value | 0x00 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Description | | 0x26 | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| SMBus Register | | | 0x5A[7] | 0x5A[6] | 0x5A[5] | 0x5A[4] | 0x5A[3] | 0x5A[2] | 0x5A[1] | 0x5A[0] |
| Default Value | 0x54 | | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| Description | | 0x27 | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| SMBus Register | | | 0x5B[7] | 0x5B[6] | 0x5B[5] | 0x5B[4] | 0x5B[3] | 0x5B[2] | 0x5B[1] | 0x5B[0] |
| Default Value | 0x54 | | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |

**Table 8. Example of EEPROM for 4 Devices Using 2 Address Maps(1)**

| EEPROM ADDRESS | ADDRESS (HEX) | EEPROM DATA | COMMENTS |
|---|---|---|---|
| 0 | 00 | 0x43 | CRC_EN = 0, Address Map = 1, >256 bytes = 0, Device Count[3:0] = 3 |
| 1 | 01 | 0x00 | |
| 2 | 02 | 0x08 | EEPROM Burst Size |
| 3 | 03 | 0x00 | CRC not used |
| 4 | 04 | 0x0B | Device 0 Address Location |
| 5 | 05 | 0x00 | CRC not used |
| 6 | 06 | 0x0B | Device 1 Address Location |
| 7 | 07 | 0x00 | CRC not used |
| 8 | 08 | 0x30 | Device 2 Address Location |
| 9 | 09 | 0x00 | CRC not used |
| 10 | 0A | 0x30 | Device 3 Address Location |
| 11 | 0B | 0x00 | Begin Device 0, 1 - Address Offset 3 |
| 12 | 0C | 0x00 | |
| 13 | 0D | 0x04 | |
| 14 | 0E | 0x07 | |
| 15 | 0F | 0x00 | |
| 16 | 10 | 0x00 | EQ CHB0 = 00 |
| 17 | 11 | 0xAB | VOD CHB0 = 1.0 V |
| 18 | 12 | 0x00 | DEM CHB0 = 0 (0 dB) |
| 19 | 13 | 0x00 | EQ CHB1 = 00 |
| 20 | 14 | 0x0A | VOD CHB1 = 1.0 V |
| 21 | 15 | 0xB0 | DEM CHB1 = 0 (0 dB) |
| 22 | 16 | 0x00 | |
| 23 | 17 | 0x00 | EQ CHB2 = 00 |
| 24 | 18 | 0xAB | VOD CHB2 = 1.0 V |
| 25 | 19 | 0x00 | DEM CHB2 = 0 (0 dB) |
| 26 | 1A | 0x00 | EQ CHB3 = 00 |
| 27 | 1B | 0x0A | VOD CHB3 = 1.0 V |
| 28 | 1C | 0xB0 | DEM CHB3 = 0 (0 dB) |
| 29 | 1D | 0x01 | |
| 30 | 1E | 0x80 | |
| 31 | 1F | 0x01 | EQ CHA0 = 00 |
| 32 | 20 | 0x56 | VOD CHA0 = 1.0 V |
| 33 | 21 | 0x00 | DEM CHA0 = 0 (0 dB) |
| 34 | 22 | 0x00 | EQ CHA1 = 00 |
| 35 | 23 | 0x15 | VOD CHA1 = 1.0 V |
| 36 | 24 | 0x60 | DEM CHA1 = 0 (0 dB) |
| 37 | 25 | 0x00 | |
| 38 | 26 | 0x01 | EQ CHA2 = 00 |
| 39 | 27 | 0x56 | VOD CHA2 = 1.0 V |
| 40 | 28 | 0x00 | DEM CHA2 = 0 (0 dB) |
| 41 | 29 | 0x00 | EQ CHA3 = 00 |
| 42 | 2A | 0x15 | VOD CHA3 = 1.0 V |
| 43 | 2B | 0x60 | DEM CHA3 = 0 (0 dB) |
| 44 | 2C | 0x00 | |

(1) Note: CRC_EN = 0, Address Map = 1, >256 byte = 0, Device Count[3:0] = 3. This example has all 8–channels set to EQ = 00 (min boost), VOD = 1.0 V, DEM = 0 (0 dB) and multiple device can point to the same address map.

**Table 8. Example of EEPROM for 4 Devices Using 2 Address Maps(1) (continued)**

| EEPROM ADDRESS | ADDRESS (HEX) | EEPROM DATA | COMMENTS |
|---|---|---|---|
| 45 | 2D | 0x00 | |
| 46 | 2E | 0x54 | |
| 47 | 2F | 0x54 | End Device 0, 1 - Address Offset 39 |
| 48 | 30 | 0x00 | Begin Device 2, 3 - Address Offset 3 |
| 49 | 31 | 0x00 | |
| 50 | 32 | 0x04 | |
| 51 | 33 | 0x07 | |
| 52 | 34 | 0x00 | |
| 53 | 35 | 0x00 | EQ CHB0 = 00 |
| 54 | 36 | 0xAB | VOD CHB0 = 1.0 V |
| 55 | 37 | 0x00 | DEM CHB0 = 0 (0 dB) |
| 56 | 38 | 0x00 | EQ CHB1 = 00 |
| 57 | 39 | 0x0A | VOD CHB1 = 1.0 V |
| 58 | 3A | 0xB0 | DEM CHB1 = 0 (0 dB) |
| 59 | 3B | 0x00 | |
| 60 | 3C | 0x00 | EQ CHB2 = 00 |
| 61 | 3D | 0xAB | VOD CHB2 = 1.0 V |
| 62 | 3E | 0x00 | DEM CHB2 = 0 (0 dB) |
| 63 | 3F | 0x00 | EQ CHB3 = 00 |
| 64 | 40 | 0x0A | VOD CHB3 = 1.0 V |
| 65 | 41 | 0xB0 | DEM CHB3 = 0 (0 dB) |
| 66 | 42 | 0x01 | |
| 67 | 43 | 0x80 | |
| 68 | 44 | 0x01 | EQ CHA0 = 00 |
| 69 | 45 | 0x56 | VOD CHA0 = 1.0 V |
| 70 | 46 | 0x00 | DEM CHA0 = 0 (0 dB) |
| 71 | 47 | 0x00 | EQ CHA1 = 00 |
| 72 | 48 | 0x15 | VOD CHA1 = 1.0 V |
| 73 | 49 | 0x60 | DEM CHA1 = 0 (0 dB) |
| 74 | 4A | 0x00 | |
| 75 | 4B | 0x01 | EQ CHA2 = 00 |
| 76 | 4C | 0x56 | VOD CHA2 = 1.0 V |
| 77 | 4D | 0x00 | DEM CHA2 = 0 (0 dB) |
| 78 | 4E | 0x00 | EQ CHA3 = 00 |
| 79 | 4F | 0x15 | VOD CHA3 = 1.0 V |
| 80 | 50 | 0x60 | DEM CHA3 = 0 (0 dB) |
| 81 | 51 | 0x00 | |
| 82 | 52 | 0x00 | |
| 83 | 53 | 0x54 | |
| 84 | 54 | 0x54 | End Device 2, 3 - Address Offset 39 |

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The DS100KR800 is a high-performance circuit capable of delivering excellent performance. Pay careful attention to the details associated with high-speed design as well as providing a clean power supply. Refer to the information below and Revision 4 of the LVDS Owner's Manual for more detailed information on high-speed design tips to address signal integrity design issues.

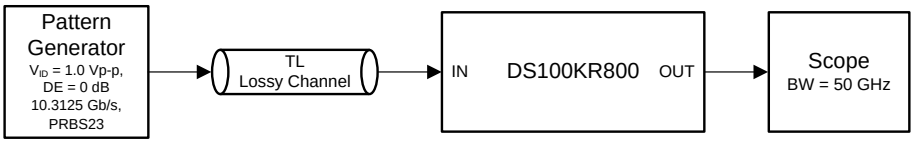



**Figure 7. Test Set-Up Connections Diagram**


**Figure 8. Test Set-Up Connections Diagram**

## 8.2 Typical Application

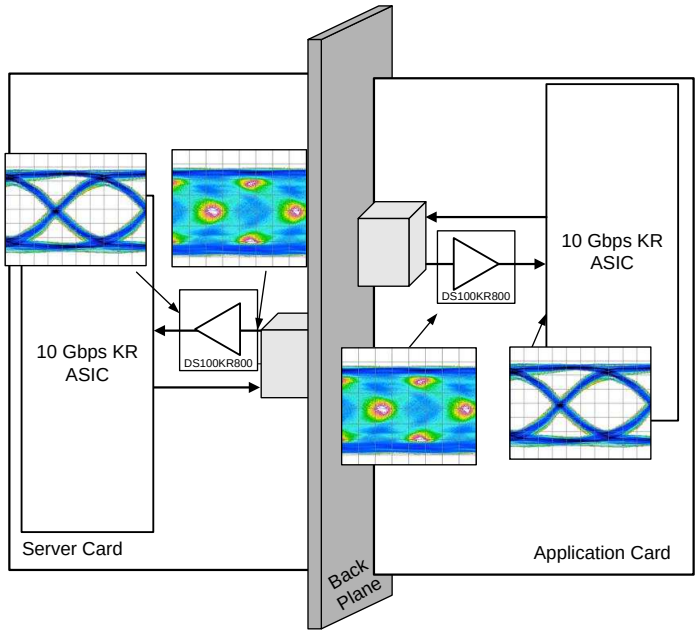



**Figure 9. Ethernet Backplane**

## Typical Application (continued)

### 8.2.1 Design Requirements

As with any high-speed design, there are many factors which influence the overall performance. Below are a list of critical areas for consideration and study during design.

- Use 100-Ω impedance traces. Generally these are very loosely coupled to ease routing length differences.
- Place AC-coupling capacitors near to the receiver end of each channel segment to minimize reflections.
- The maximum body size for AC-coupling capacitors is 0402.
- Back-drill connector vias and signal vias to minimize stub length.
- Use Reference plane vias to ensure a low inductance path for the return current.

### 8.2.2 Detailed Design Procedure

The DS100KR800 is designed to be placed at an offset location with respect to the overall channel attenuation. In order to optimize performance, the repeater requires tuning to extend the reach of the cable or trace length while also recovering a solid eye opening. To tune the repeater, the settings mentioned in Table 2 and Table 3 are recommended as a default starting point for most applications. Once these settings are configured, additional tuning of the EQ and, to a lesser extent, VOD may be required to optimize the repeater performance for each specific application environment.

Examples of the repeater performance as a generic high-speed datapath repeater are shown in the performance curves in the *Application Curves*.

### 8.2.3 Application Curves

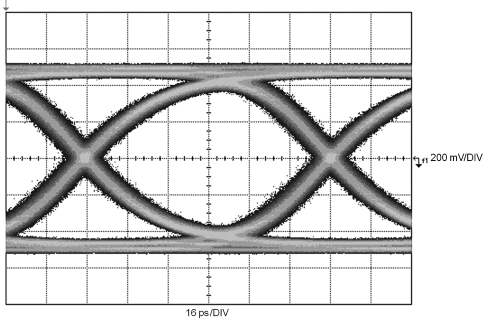



**Figure 10. TL = 20 inch 4–mil FR4 Trace, DS100KR800 Settings: EQ[1:0] = R, R = 15'h, DEM[1:0] = Float, Float**

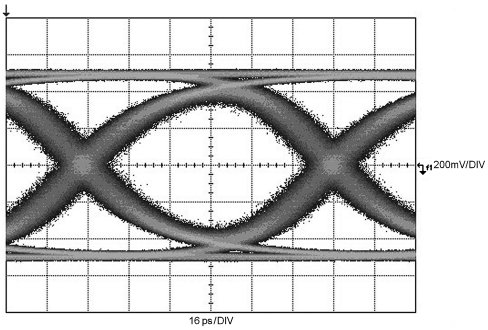



**Figure 11. TL = 30 inch 4–mil FR4 Trace, DS100KR800 Settings: EQ[1:0] = Float, R = 1F'h, DEM[1:0] = Float, Float**

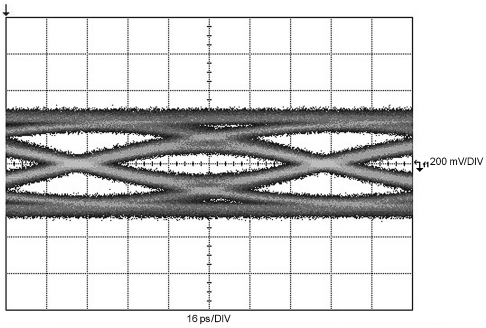



**Figure 12. TL1 = 20 inch 4–mil FR4 Trace, TL2 = 15 inch 4–mil FR4 Trace, DS100KR800 Settings: EQ[1:0] = R, R = 15'h, DEM[1:0] = Float, Float**

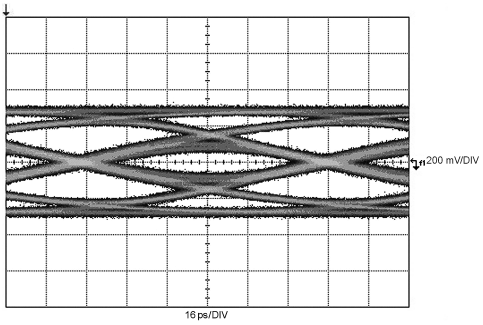



**Figure 13. TL1 = 30 inch 4–mil FR4 Trace, TL2 = 15 Inch 4–mil FR4 Trace, DS100KR800 Settings: EQ[1:0] = Float, R = 1F'h, DEM[1:0] = Float, Float**

# 9 Power Supply Recommendations

## 9.1 3.3-V or 2.5-V Supply Mode Operation

The DS1000KR800 has an optional internal voltage regulator to provide the 2.5-V supply to the device. In 3.3-V mode, the VIN pin = 3.3 V is used to supply power to the device and the VDD pins should be left open. The internal regulator will provide the 2.5 V to the VDD pins of the device and a 0.1-µF capacitor is needed at each of the five VDD pins for power supply de-coupling (total capacitance should be ≤ 0.5 µF), and the VDD pins should be left open. The VDD_SEL pin must be tied to GND to enable the internal regulator. In 2.5-V mode, the VIN pin should be left open and 2.5-V supply must be applied to the VDD pins. The VDD_SEL pin must be left open (no connect) to disable the internal regulator.

The DS100KR800 can be configured for 2.5-V operation or 3.3-V operation. The lists below outline required connections for each supply selection.

For 3.3-V mode of operation, use the following steps:

1. Tie VDD_SEL = 0 with 1-kΩ resistor to GND.
2. Feed 3.3-V supply into VIN pin. Local 1.0-µF decoupling at VIN is recommended.
3. See information on VDD bypass below.
4. SDA and SCL pins should connect pullup resistor to VIN
5. Any 4-Level input which requires a connection to Logic 1 should use a 1-kΩ resistor to VIN

For 2.5-V mode of operation, use the following steps:

1. VDD_SEL = Float
2. VIN = Float
3. Feed 2.5-V supply into VDD pins.
4. See information on VDD bypass below.
5. SDA and SCL pins connect pullup resistor to VDD for 2.5-V uC SMBus IO
6. SDA and SCL pins connect pullup resistor to VDD for 3.3-V uC SMBus IO
7. Any 4-Level input which requires a connection to Logic 1 should use a 1-kΩ resistor to VDD

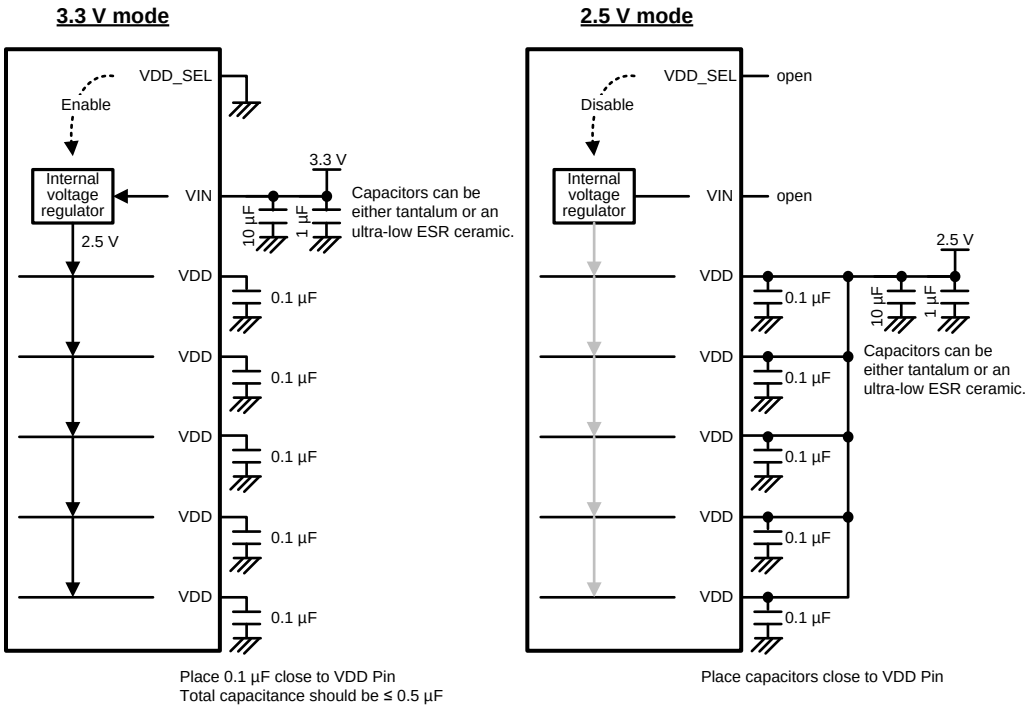



**Figure 14. 3.3-V or 2.5-V Supply Connection Diagram**

### 9.2 Power Supply Bypassing

Two approaches are recommended to ensure that the DS100KR800 is provided with an adequate power supply bypass. First, the supply ( $V_{DD}$) and ground (GND) pins should be connected to power planes routed on adjacent layers of the printed-circuit-board. Second, pay careful attention to supply bypassing through the proper use of bypass capacitors is required. A 0.1-µF bypass capacitor should be connected to each $V_{DD}$ pin such that the capacitor is placed as close as possible to the device. Small body size capacitors (such as 0402) reduce the parasitic inductance of the capacitor and also help in placement close to the $V_{DD}$ pin. If possible, the layer thickness of the dielectric should be minimized so that the $V_{DD}$ and GND planes create a low inductance supply with distributed capacitance.

## 10 Layout

### 10.1 Layout Guidelines

The differential inputs and outputs are designed with 100-Ω differential terminations. Therefore, they should be connected to interconnects with controlled differential impedance of approximately 85-110 Ω. It is preferable to route differential lines primarily on one layer of the board, particularly for the input traces. The use of vias should be avoided if possible. If vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair. Whenever differential vias are used, the layout must also provide for a low inductance path for the return currents as well. Route the differential signals away from other signals and noise sources on the printed-circuit-board. To minimize the effects of crosstalk, a 5:1 ratio or greater should be maintained between inter-pair spacing and trace width. See *AN-1187 Leadless Leadframe Package (LLP)* Application Report (SNOA401) for additional information on QFN (WQFN) packages.

The DS100KR800 pinout promotes easy high-speed routing and layout. To optimize DS100KR800 performance refer to the following guidelines:

1. Place local VIN and VDD capacitors as close as possible to the device supply pins. Often the best location is directly under the DS100KR800 pins to reduce the inductance path to the capacitor. In addition, bypass capacitors may share a via with the DAP GND to minimize ground loop inductance.
2. Differential pairs going into or out of the DS100KR800 should have adequate pair-to-pair spacing to minimize crosstalk.
3. Use return current via connections to link reference planes locally. This ensures a low inductance return current path when the differential signal changes layers.
4. Optimize the via structure to minimize trace impedance mismatch.
5. Place GND vias around the DAP perimeter to ensure optimal electrical and thermal performance.
6. Use small body size AC-coupling capacitors when possible — 0402 or smaller size is preferred. The AC-coupling capacitors should be placed closer to the Rx on the channel.

Figure 15 depicts different transmission line topologies which can be used in various combinations to achieve the optimal system performance. Impedance discontinuities at the differential via can be minimized or eliminated by increasing the swell around each hole and providing for a low inductance return current path. When the via structure is associated with thick backplane PCB, further optimization such as back drilling is often used to reduce the detrimental high-frequency effects of stubs on the signal path.

## 10.2 Layout Example

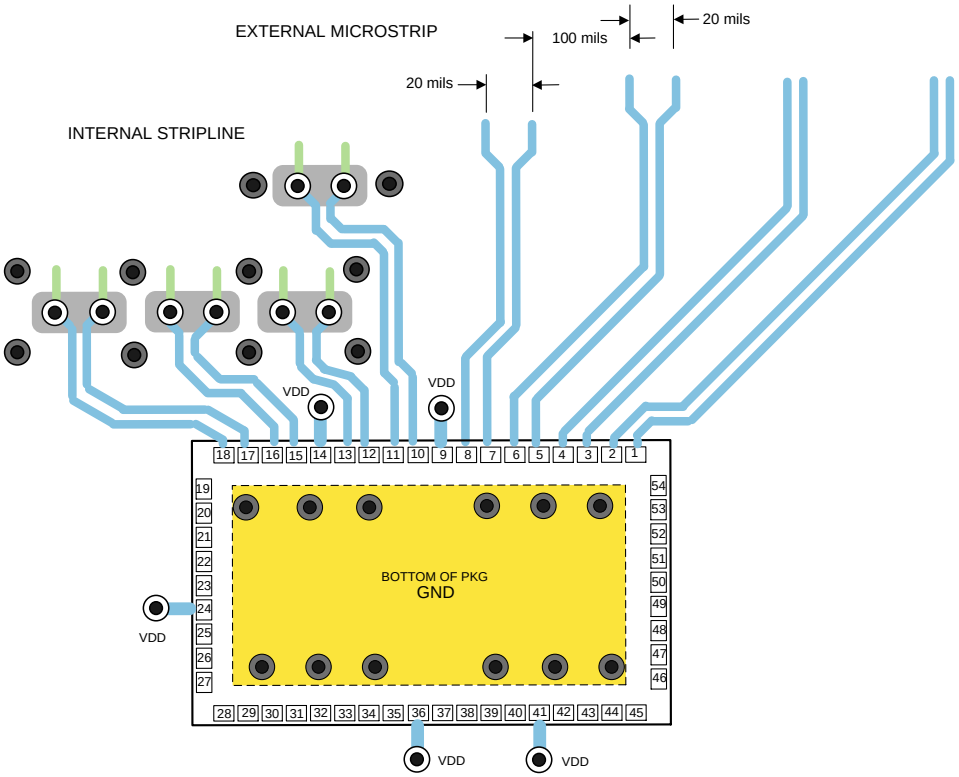



**Figure 15. Typical Routing Options**

# 11 Device and Documentation Support

## 11.1 Documentation Support

### 11.1.1 Related Documentation

For related documentation, see the following:

- *Absolute Maximum Ratings for Soldering* (SNOA549)
- *Understanding EEPROM Programming for High Speed Repeaters and Mux Buffers* (SNLA228)
- AN-1187 *Leadless Leadframe Package (LLP) Application Report* (SNOA401)

## 11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DS100KR800SQ/NOPB | ACTIVE | WQFN | NJY | 54 | 2000 | RoHS & Green | SN | Level-2-260C-1 YEAR | -40 to 85 | DS100KR800SQ | Samples |
| DS100KR800SQE/NOPB | ACTIVE | WQFN | NJY | 54 | 250 | RoHS & Green | SN | Level-2-260C-1 YEAR | -40 to 85 | DS100KR800SQ | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

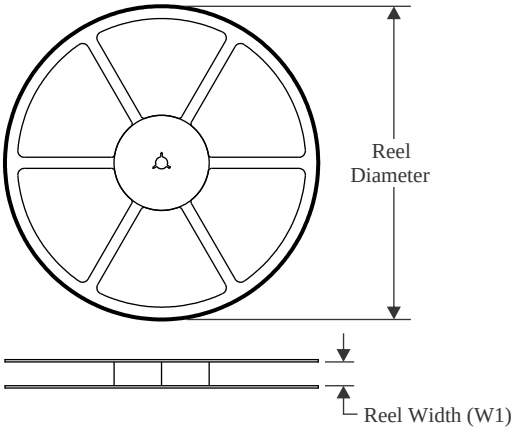
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

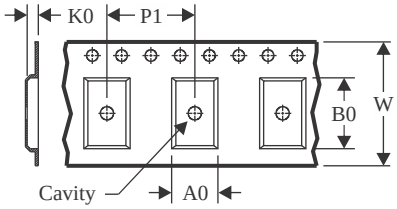
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

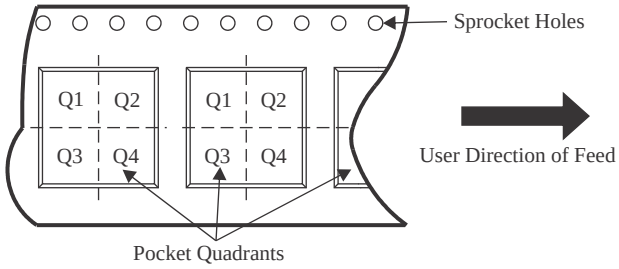



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

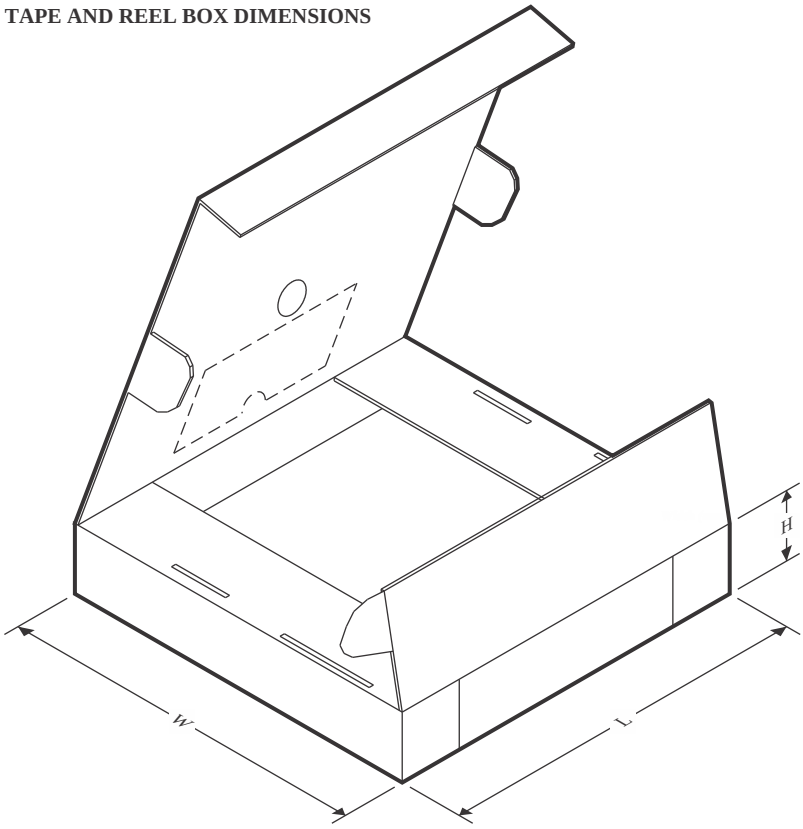
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

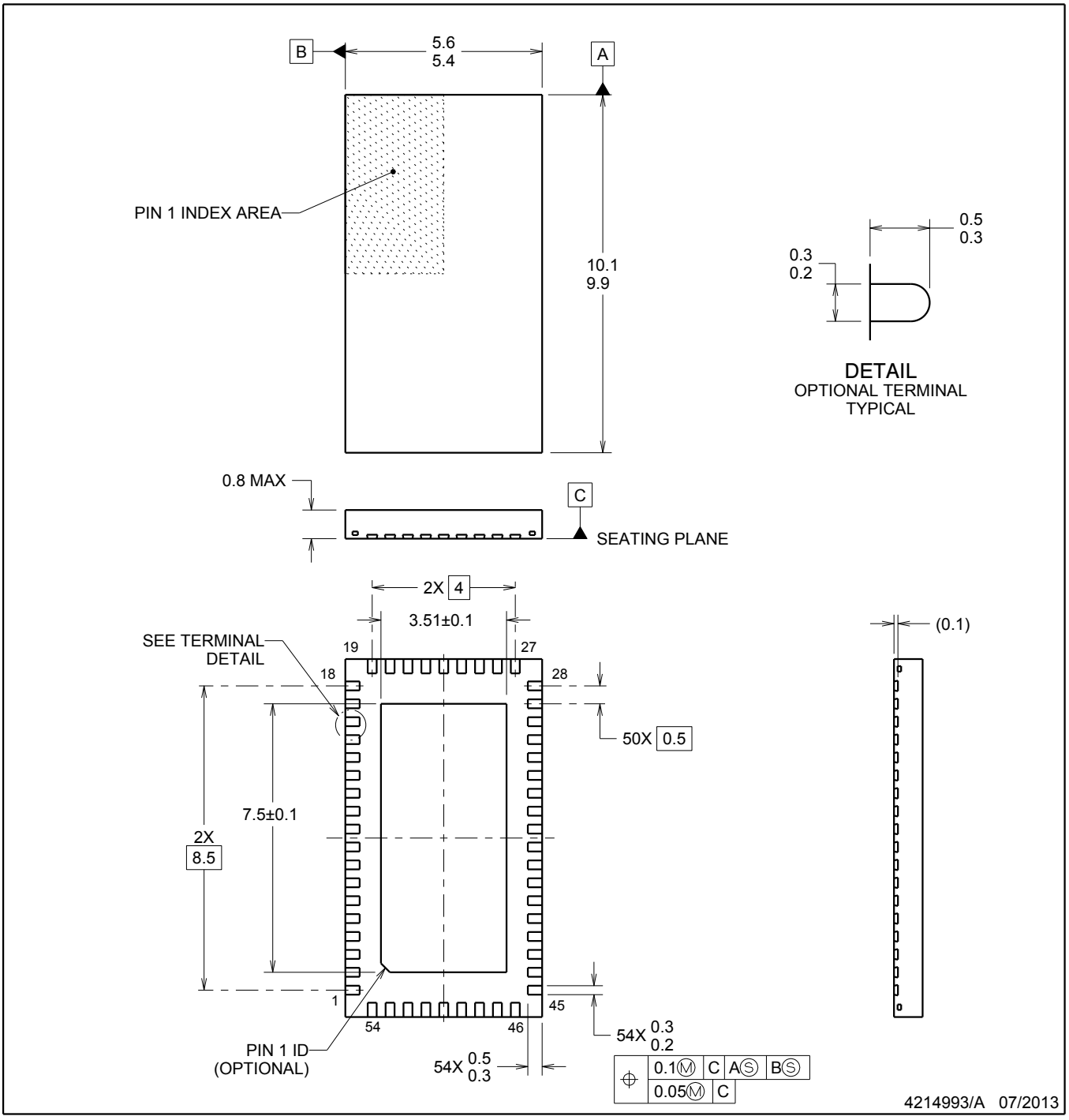
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DS100KR800SQ/NOPB | WQFN | NJY | 54 | 2000 | 330.0 | 16.4 | 5.8 | 10.3 | 1.0 | 12.0 | 16.0 | Q1 |
| DS100KR800SQE/NOPB | WQFN | NJY | 54 | 250 | 178.0 | 16.4 | 5.8 | 10.3 | 1.0 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



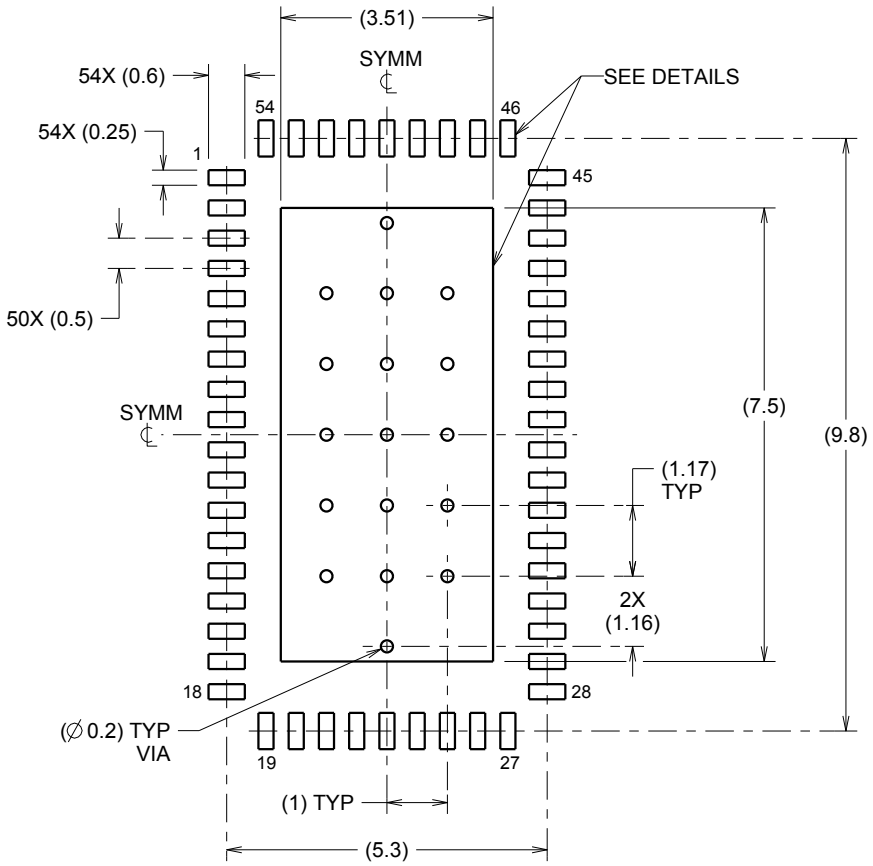

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| DS100KR800SQ/NOPB | WQFN | NJY | 54 | 2000 | 356.0 | 356.0 | 36.0 |
| DS100KR800SQE/NOPB | WQFN | NJY | 54 | 250 | 208.0 | 191.0 | 35.0 |

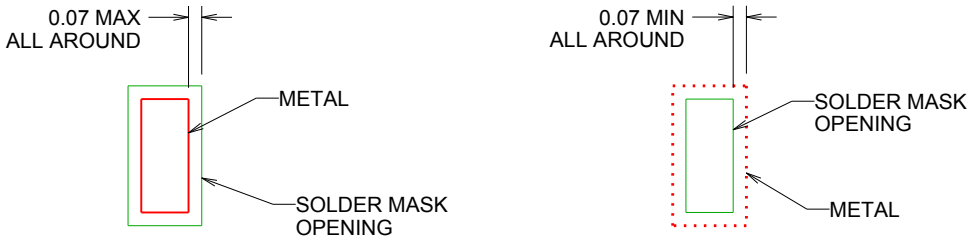



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
SCALE:8X




NON SOLDER MASK
DEFINED
(PREFERRED)

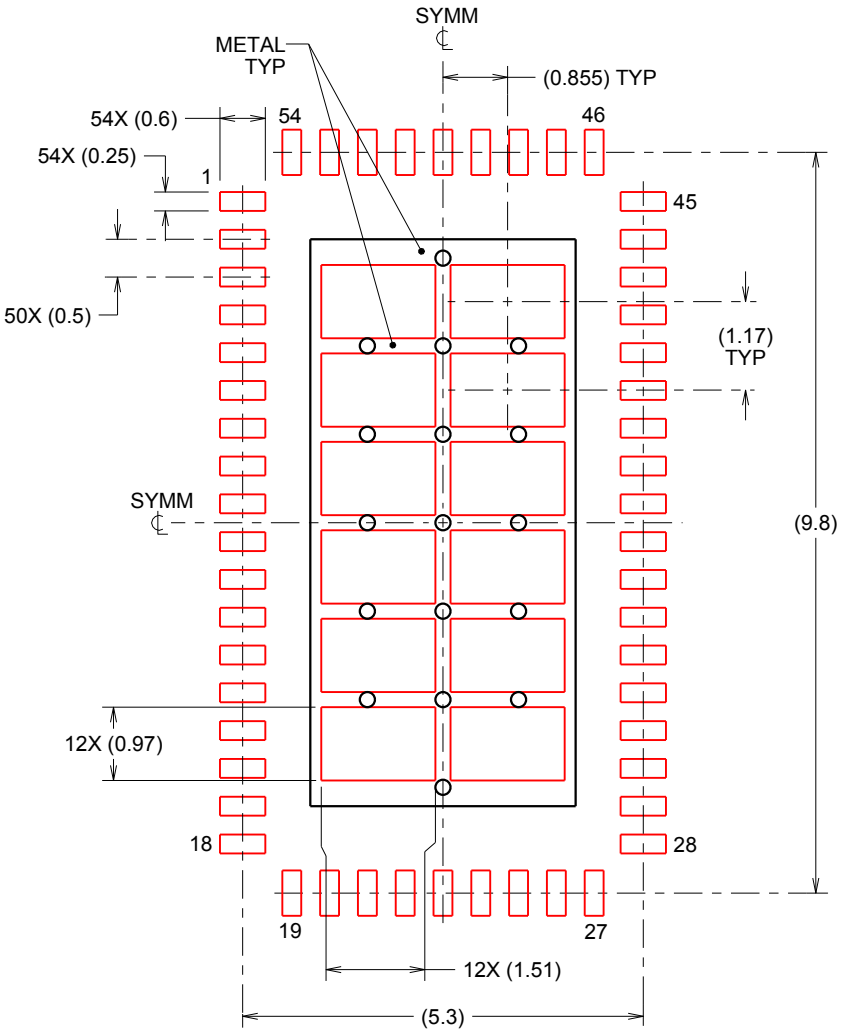
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214993/A 07/2013

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).




SOLDERPASTE EXAMPLE
BASED ON 0.125mm THICK STENCIL

EXPOSED PAD
67% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

4214993/A 07/2013

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265