

## DS26C31MQML CMOS Quad TRI-STATE Differential Line Driver

Check for Samples: [DS26C31MQML](#)

### FEATURES

- TTL Input Compatible
- Outputs Will Not Load Line When  $V_{CC} = 0V$
- Meets the Requirements of EIA Standard RS-422
- Operation from Single 5V Supply
- TRI-STATE Outputs for Connection to System Buses
- Low Quiescent Current

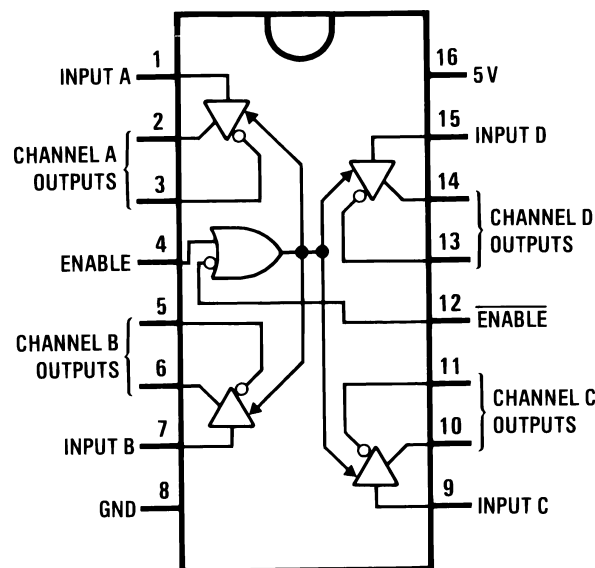
### DESCRIPTION

The DS26C31 is a quad differential line driver designed for digital data transmission over balanced lines. The DS26C31 meets all the requirements of EIA standard RS-422 while retaining the low power characteristics of CMOS. The DS26C31 is compatible with EIA standard RS-422; however, one exception in test methodology is taken. This enables the construction of serial and terminal interfaces while maintaining minimal power consumption.

The DS26C31 accepts TTL or CMOS input levels and translates these to RS-422 output levels. This part uses special output circuitry that enables the drivers to power down without loading down the bus. This device has enable and disable circuitry common to all four drivers. The DS26C31 is pin compatible to the AM26LS31 and the DS26LS31.

All inputs are protected against damage due to electrostatic discharge by diodes to  $V_{CC}$  and ground.

### Connection Diagram



**Figure 1. CDIP, CLGA Packages- Top View**  
See Package Numbers NFE0016A, NAD0016A

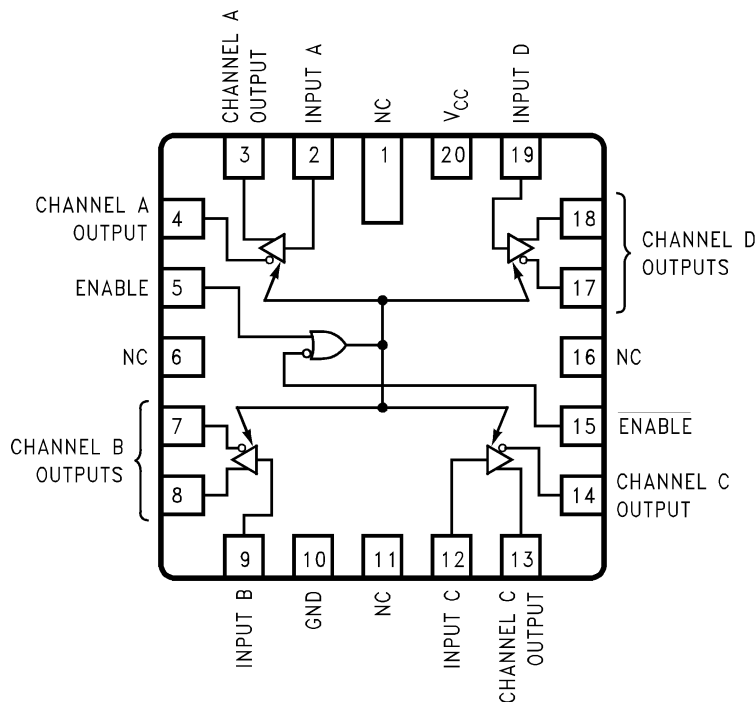


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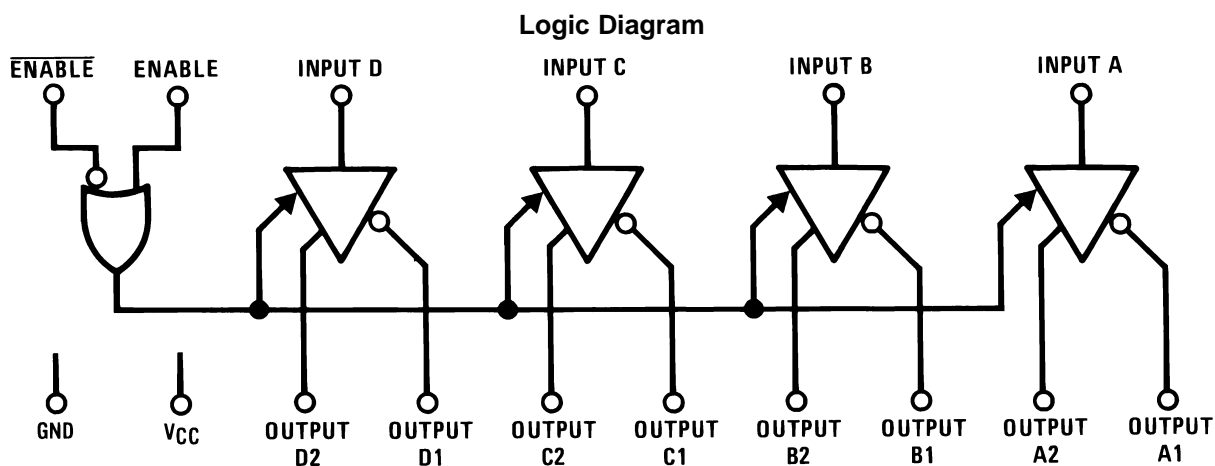
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**Figure 2. 20-Lead LCCC Package- Top View**  
See Package Number NAJ0020A



**Truth Table <sup>(1)</sup>**

ENABLE	ENABLE	Input	Non-Inverting Output	Inverting Output
L	H	X	Z	Z
All other combinations of enable inputs		L	L	H
		H	H	L

- (1) L = Low logic state  
X = Irrelevant  
H = High logic state  
Z = TRI-STATE (high impedance)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings<sup>(1)(2)</sup>

Supply Voltage ( $V_{CC}$ )	–0.5V to 7.0V
DC Input Voltage ( $V_I$ )	–1.5V to $V_{CC} + 0.5V$
DC Output Voltage ( $V_O$ )	–0.5V to 7V
Clamp Diode Current ( $I_{IK}$ , $I_{OK}$ )	±20 mA
DC Output Current, per pin ( $I_O$ )	±150 mA
DC $V_{CC}$ or Gnd Current, per pin ( $I_{CC}$ )	±150 mA
Storage Temperature Range ( $T_{Stg}$ )	–65°C ≤ $T_A$ ≤ +150°C
Lead Temperature ( $T_L$ ) Soldering, 4 sec.	260°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not verify specific performance limits. For verified specifications and test conditions, see the Electrical Characteristics. The verified specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- (2) Unless otherwise specified, all voltages are referenced to ground. All currents into device pins are positive, all currents out of device pins are negative.

## Operating Conditions

	Min	Max	Units
Supply Voltage ( $V_{CC}$ )	4.50	5.50	V
DC Input or Output Voltage ( $V_I$ , $V_O$ )	0	$V_{CC}$	V
Operating Temperature Range ( $T_A$ )	–55	+125	°C

## Quality Conformance Inspection

**Table 1. Mil-Std-883, Method 5005 - Group A**

Subgroup	Description	Temp °C
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	–55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	–55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	–55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	–55
12	Settling time at	+25
13	Settling time at	+125
14	Settling time at	–55

**DS26C31M Electrical Characteristics DC Parameters**

Parameter		Test Conditions	Notes	Min	Max	Unit	Sub-groups
$V_{IH}$	Logical "1" Input Voltage			2.0		V	1, 2, 3
$V_{IL}$	Logical "0" Input Voltage				0.8	V	1, 2, 3
$V_{OH}$	Logical "1" Output Voltage	$V_I = V_{IH}$ or $V_{IL}$ , $V_{CC} = 4.5V$ , $I_O = -20mA$		2.5		V	1, 2, 3
$V_{OL}$	Logical "0" Output Voltage	$V_I = V_{IH}$ or $V_{IL}$ , $I_O = 20mA$ , $V_{CC} = 4.5V$			0.5	V	1, 2, 3
$V_T$	Differential Output Voltage	$R_L = 100\Omega$ , $V_{CC} = 4.5V$	(1)	2.0		V	1, 2, 3
$ V_T  -  \bar{V}_T $	Difference in Differential Output	$R_L = 100\Omega$ , $V_{CC} = 4.5V$	(1)		0.4	V	1, 2, 3
$V_{OS}$	Common Mode Output Voltage	$R_L = 100\Omega$ , $V_{CC} = 5.5V$	(1)		3.0	V	1, 2, 3
$ V_{OS} - \bar{V}_{OS} $	Diff in Common Mode Output	$R_L = 100\Omega$ , $V_{CC} = 5.5V$	(1)		0.4	V	1, 2, 3
$I_I$	Input Current	$V_I = V_{CC}$ , Gnd, $V_{IH}$ , or $V_{IL}$ , $V_{CC} = 5.5V$			$\pm 1.0$	$\mu A$	1, 2, 3
$I_{CC}$	Quiescent Power Supply Current	$I_O = 0\mu A$ , $V_I = V_{CC}$ or Gnd, $V_{CC} = 5.5V$	(2)		500	$\mu A$	1, 2, 3
		$I_O = 0\mu A$ , $V_I = 2.4V$ or $0.5V$ , $V_{CC} = 5.5V$	(2)		2.1	mA	1, 2, 3
$I_{OZ}$	TRI-STATE Output Leakage Current	$V_O = V_{CC}$ or Gnd, Enable = $V_{IL}$ , $V_{CC} = 5.5V$ , Enable = $V_{IH}$			$\pm 5.0$	$\mu A$	1, 2, 3
$I_{SC}$	Output Short Circuit Current	$V_I = V_{CC}$ or Gnd, $V_{CC} = 5.5V$	(1), (3)	-30	-150	mA	1, 2, 3
$I_{Off}$	Output Leakage Current "Power Off"	$V_{CC} = 0V$ , $V_O = 6V$			100	$\mu A$	1, 2, 3
		$V_{CC} = 0V$ , $V_O = 0V$			-100	$\mu A$	1, 2, 3

(1) See EIA Specification RS-422 for exact test conditions.

(2) Measured per input. All other inputs at  $V_{CC}$  or GND.

(3) This is the current sourced when a high output is shorted to ground. Only one output at a time should be shorted.

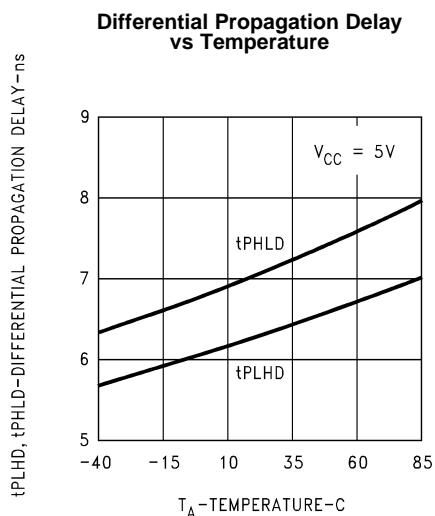
**DS26C31M Electrical Characteristics AC Parameters - Propagation Delay Time (see Figure 26)**The following conditions apply, unless otherwise specified.  $V_{CC} = 5V$ ,  $t_R \leq 6ns$ ,  $t_F \leq 6ns$ 

Parameter		Test Conditions	Notes	Min	Max	Unit	Sub-groups
$t_{PLH}$	Input to Output Prop Delay	Figure 27			14	ns	9, 10, 11
$t_{PHL}$	Input to Output Prop Delay	Figure 27			14	ns	9, 10, 11
	Skew		(1)		3.0	ns	9, 10, 11
$t_{TLH}$	Output Rise Time	Figure 29			14	ns	9, 10, 11
$t_{THL}$	Output Fall Time	Figure 29			14	ns	9, 10, 11
$t_{PZH}$	Output Enable Time	Figure 28			22	ns	9, 10, 11
$t_{PZL}$	Output Enable Time	Figure 28			28	ns	9, 10, 11
$t_{PHZ}$	Output Disable Time	Figure 28	(2)		12	ns	9, 10, 11
$t_{PLZ}$	Output Disable Time	Figure 28	(2)		14	ns	9, 10, 11

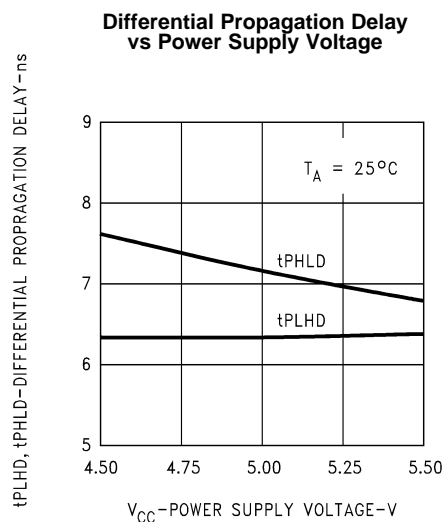
(1) Skew is defined as the difference in propagation delays between complimentary outputs at the 50% point.

(2) Output disable time is the delay from ENABLE or  $\bar{ENABLE}$  being switched to the output transistors turning off.

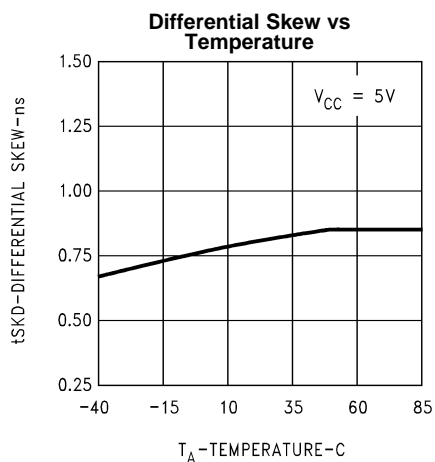
## Typical Performance Characteristics



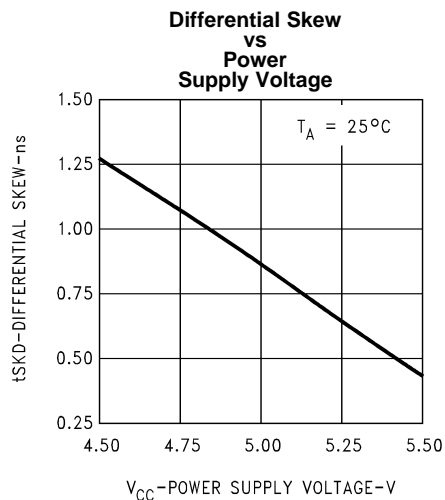
**Figure 3.**



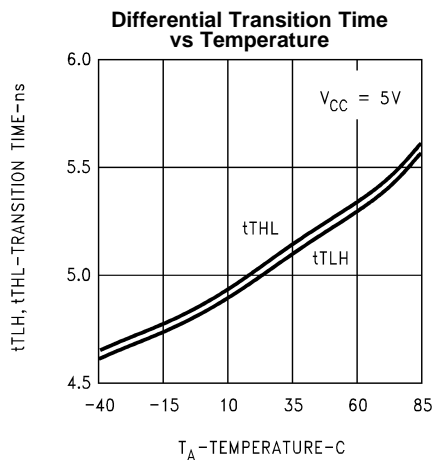
**Figure 4.**



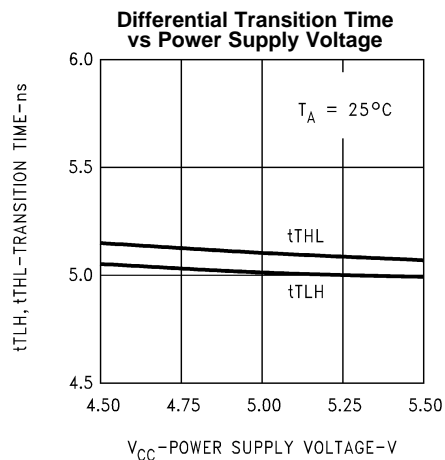
**Figure 5.**



**Figure 6.**



**Figure 7.**



**Figure 8.**

## Typical Performance Characteristics (continued)

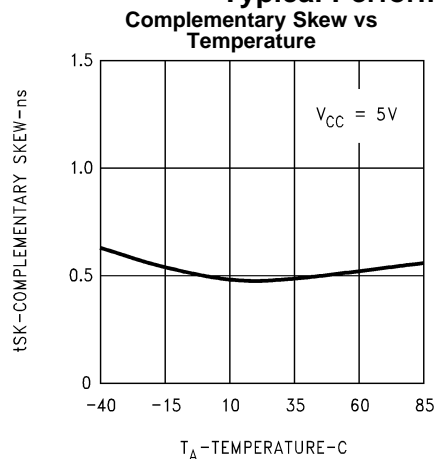


Figure 9.

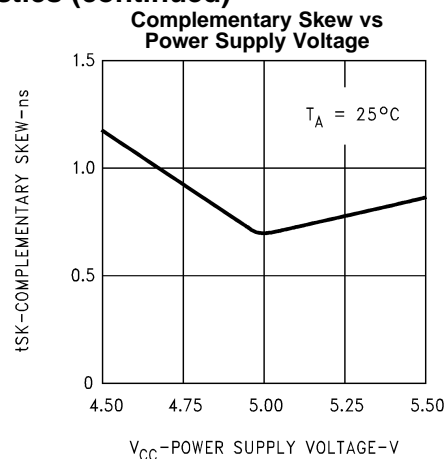


Figure 10.

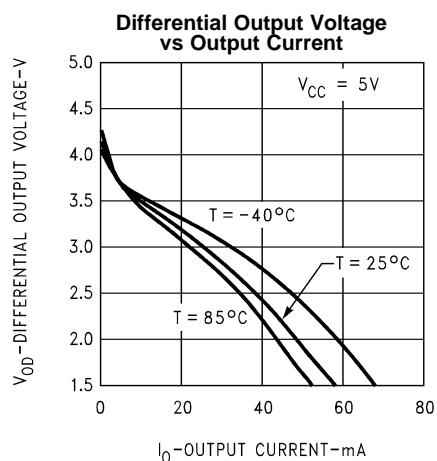


Figure 11.

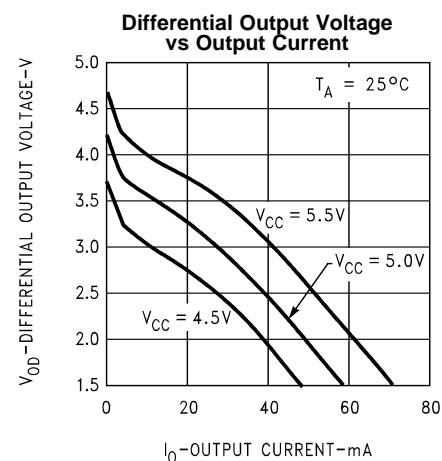


Figure 12.

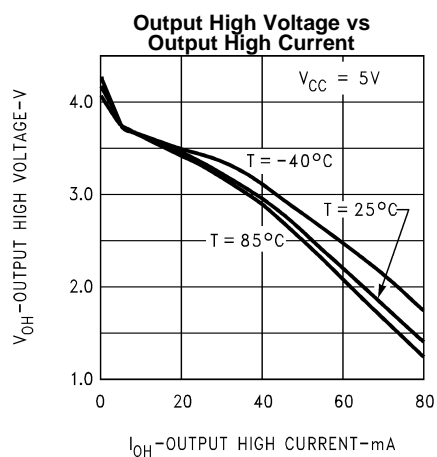


Figure 13.

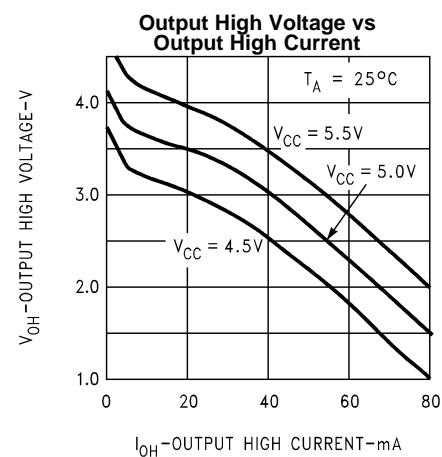
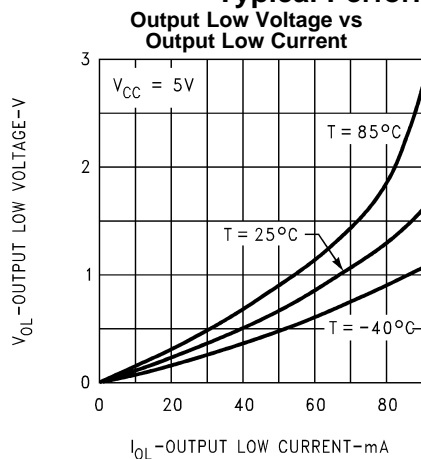
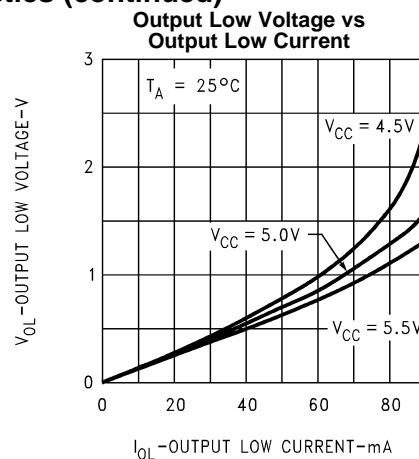


Figure 14.

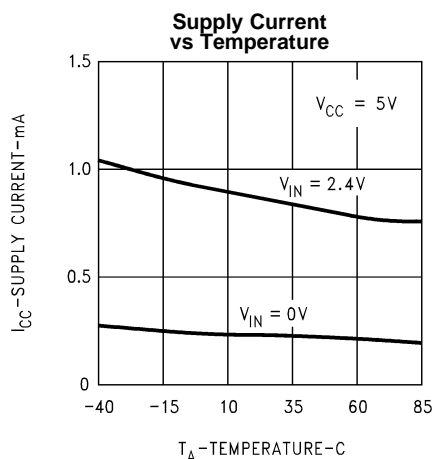
## Typical Performance Characteristics (continued)



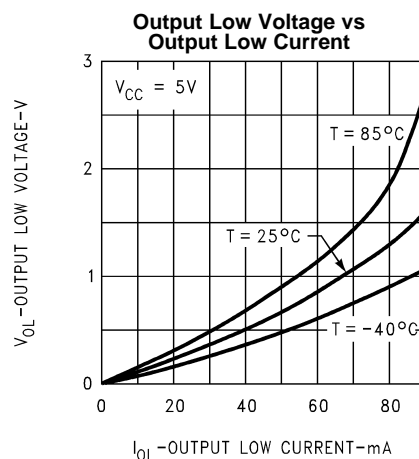
**Figure 15.**



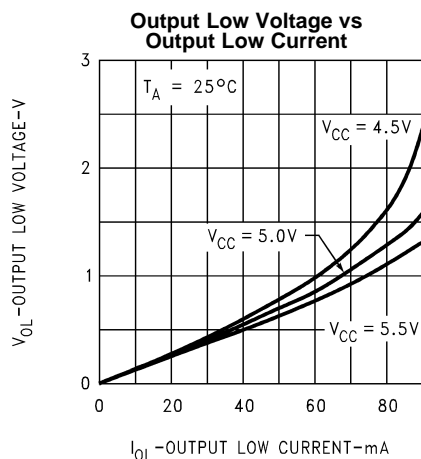
**Figure 16.**



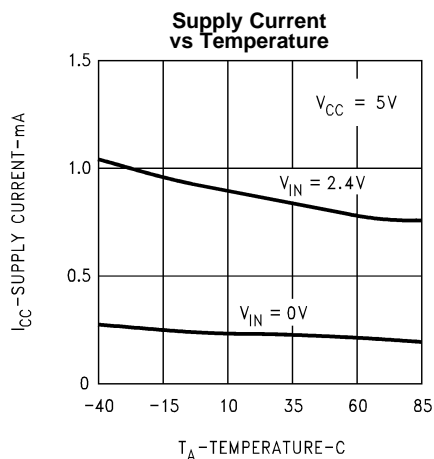
**Figure 17.**



**Figure 18.**



**Figure 19.**



**Figure 20.**

## Typical Performance Characteristics (continued)

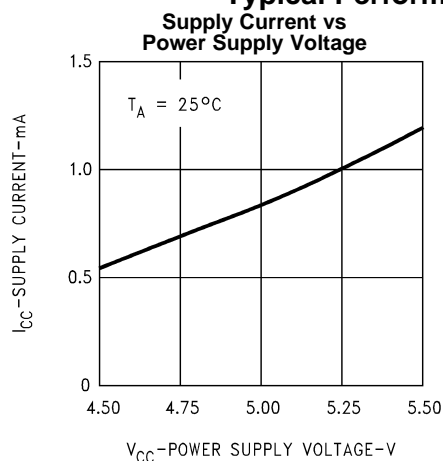


Figure 21.

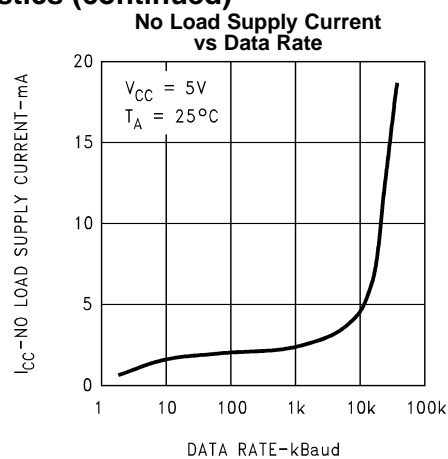


Figure 22.

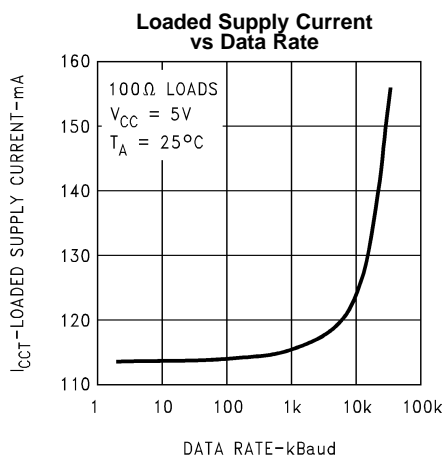


Figure 23.

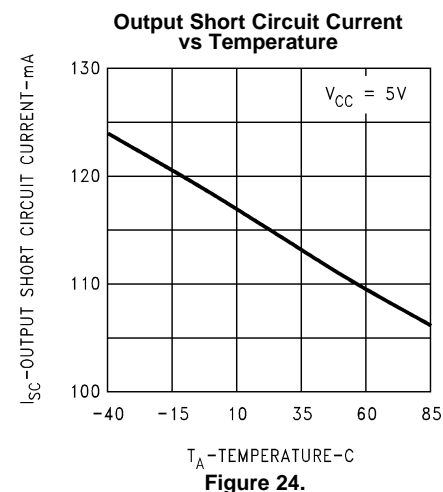


Figure 24.

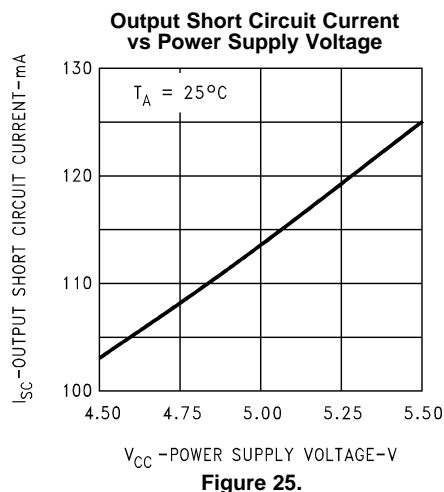
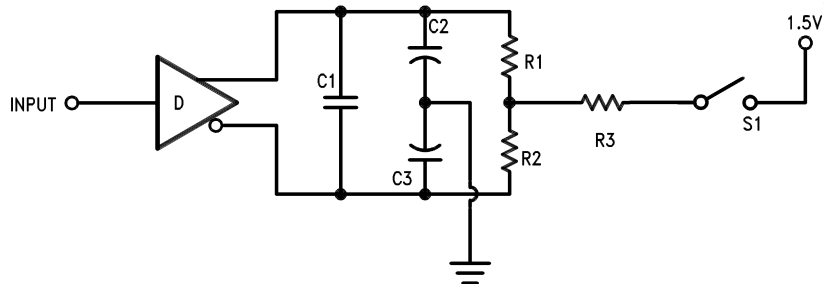


Figure 25.

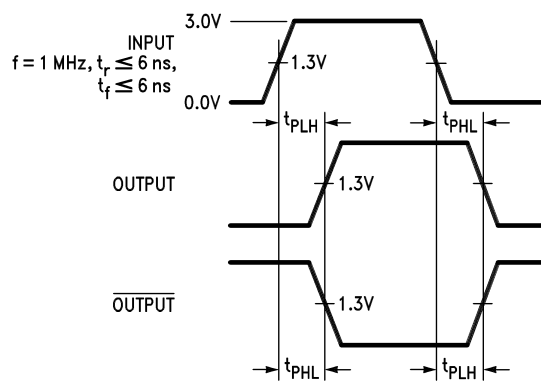


## AC TEST CIRCUIT AND SWITCHING TIME WAVEFORMS

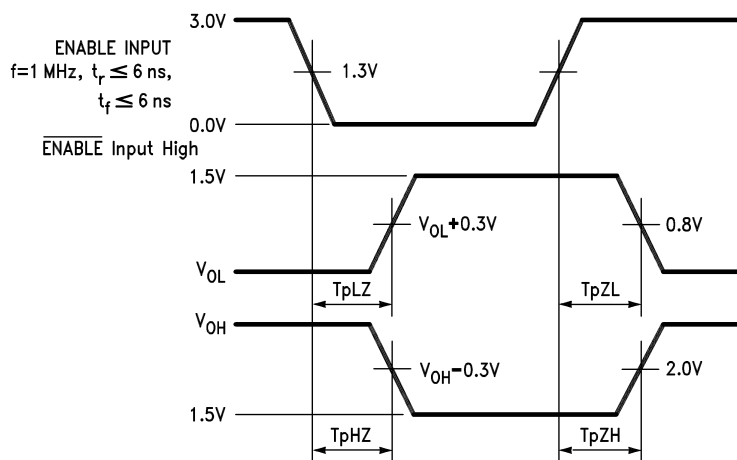


**Note:** C1 = C2 = C3 = 40 pF (Including Probe and Jig Capacitance), R1 = R2 = 50Ω, R3 = 500Ω.

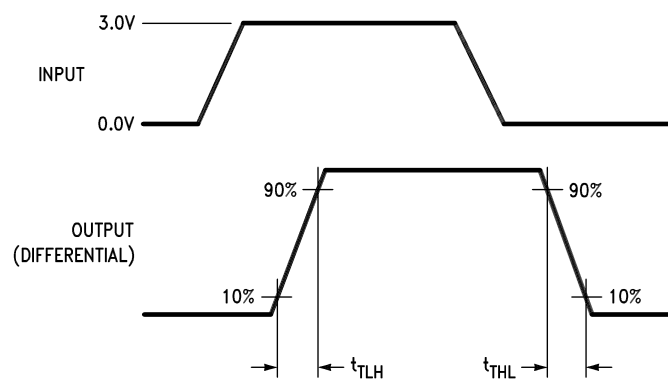
**Figure 26. AC Test Circuit**



**Figure 27. Propagation Delays**



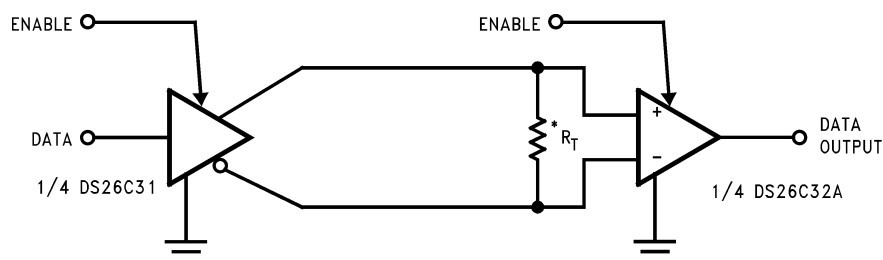
**Figure 28. Enable and Disable Times**



Input pulse;  $f = 1 \text{ MHz}$ , 50%;  $t_r \leq 6 \text{ ns}$ ,  $t_f \leq 6 \text{ ns}$

**Figure 29. Differential Rise and Fall Times**

### TYPICAL APPLICATIONS



\* $R_T$  is optional although highly recommended to reduce reflection.

**Figure 30. Two-Wire Balanced System, RS-422**

## REVISION HISTORY

**Table 2. Revision History**

Released	Revision	Section	Changes
10/26/2010	A	New Release, Corporate format	1 MDS data sheets converted into one Corp. data sheet format. MNDS26C31M-X Rev 0B0 will be archived.

**Changes from Original (April 2013) to Revision A**
**Page**

- Changed layout of National Data Sheet to TI format ..... [10](#)

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">DS26C31ME/883</a>	Active	Production	LCCC (NAJ)   20	50   TUBE	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	DS26C31ME/ 883 Q 5962-91639 01M2A ACO 01M2A >T
DS26C31ME/883.A	Active	Production	LCCC (NAJ)   20	50   TUBE	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	DS26C31ME/ 883 Q 5962-91639 01M2A ACO 01M2A >T
<a href="#">DS26C31MJ/883</a>	Active	Production	CDIP (NFE)   16	25   TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	DS26C31MJ/883 5962-9163901MEA Q
DS26C31MJ/883.A	Active	Production	CDIP (NFE)   16	25   TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	DS26C31MJ/883 5962-9163901MEA Q
<a href="#">DS26C31MW/883</a>	Active	Production	CFP (NAD)   16	19   TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	DS26C31MW /883 Q 5962-91639 01MFA ACO 01MFA >T
DS26C31MW/883.A	Active	Production	CFP (NAD)   16	19   TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	DS26C31MW /883 Q 5962-91639 01MFA ACO 01MFA >T

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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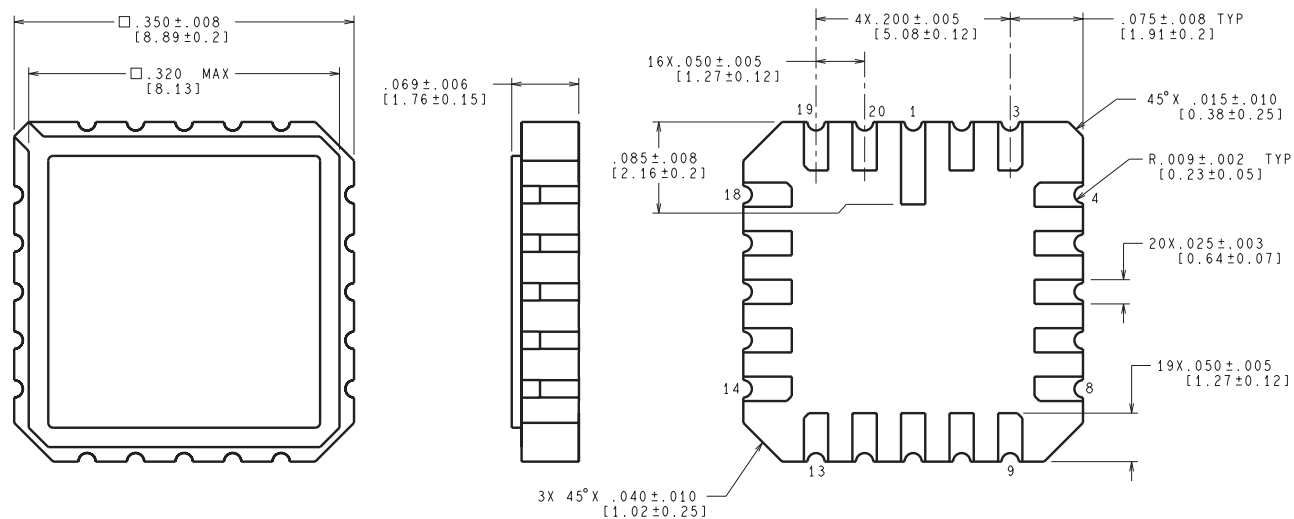
## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
DS26C31ME/883	NAJ	LCCC	20	50	470	11	3810	0
DS26C31ME/883.A	NAJ	LCCC	20	50	470	11	3810	0
DS26C31MJ/883	NFE	CDIP	16	25	506.98	15.24	13440	NA
DS26C31MJ/883	NFE	CDIP	16	25	506.98	15.24	13440	NA
DS26C31MJ/883.A	NFE	CDIP	16	25	506.98	15.24	13440	NA
DS26C31MJ/883.A	NFE	CDIP	16	25	506.98	15.24	13440	NA
DS26C31MW/883	NAD	CFP	16	19	502	23	9398	9.78
DS26C31MW/883.A	NAD	CFP	16	19	502	23	9398	9.78

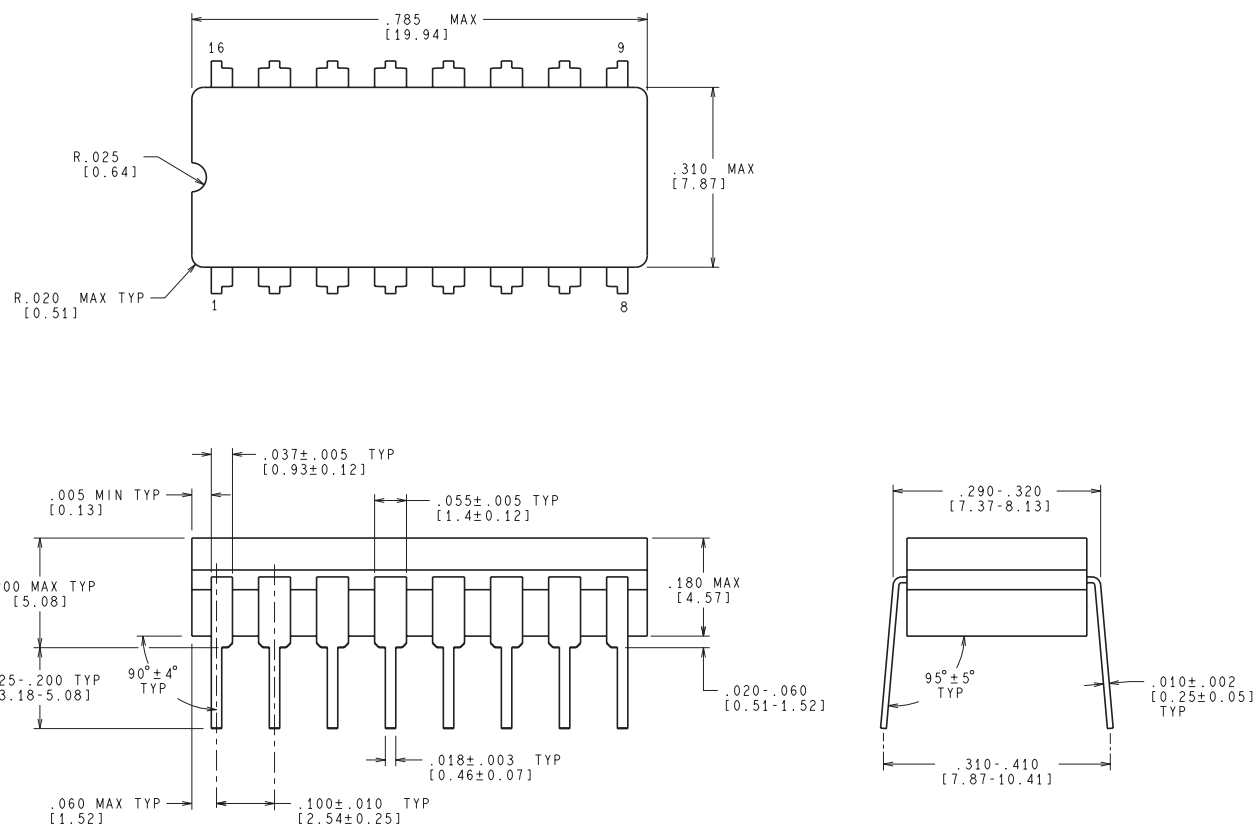
NAJ0020A



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VALUES IN [ ] ARE MILLIMETERS

E20A (Rev F)

NFE0016A

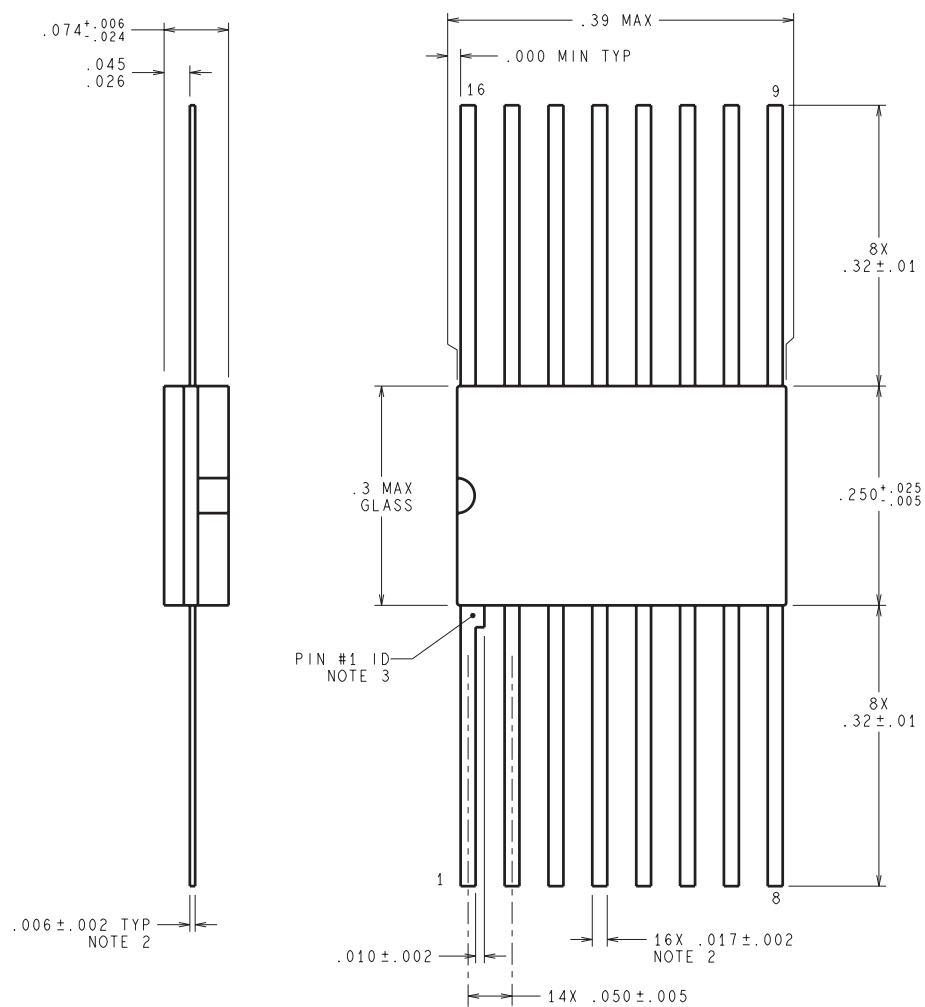


CONTROLLING DIMENSION IS INCH  
VALUES IN [ ] ARE MILLIMETERS

J16A (REV L)



NAD0016A



DIMENSIONS ARE IN INCHES

W16A (Rev T)

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