DS26F32MQML Quad Differential Line Receivers

Check for Samples: DS26F32MQML

FEATURES

- **Input Voltage Range of ±7.0V (Differential or Common Mode) ±0.2V Sensitivity over the Input Voltage Range**
- **High Input Impedance**
- **Operation from Single +5.0V Supply**
- **Input Pull-Down Resistor Prevents Output Oscillation on Unused Channels**
- **TRI-STATE Outputs, with Choice of Complementary Enables, for Receiving Directly onto a Data Bus**

DESCRIPTION

The DS26F32 is a quad differential line receiver designed to meet the requirements of EIA Standards RS-422 and RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

The DS26F32 offers improved performance due to the use of state-of-the-art L-FAST bipolar technology. The L-FAST technology allows for higher speeds and lower currents by utilizing extremely short gate delay times. Thus, the DS26F32 features lower power, extended temperature range, and improved specifications.

The device features an input sensitivity of 200 mV over the input common mode range of ±7.0V. The DS26F32 provides an enable function common to all four receivers and TRI-STATE outputs with 8.0 mA sink capability. Also, a fail-safe input/output relationship keeps the outputs high when the inputs are open.

The DS26F32 offers optimum performance when used with the DS26F31 Quad Differential Line Driver.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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Connection Diagrams

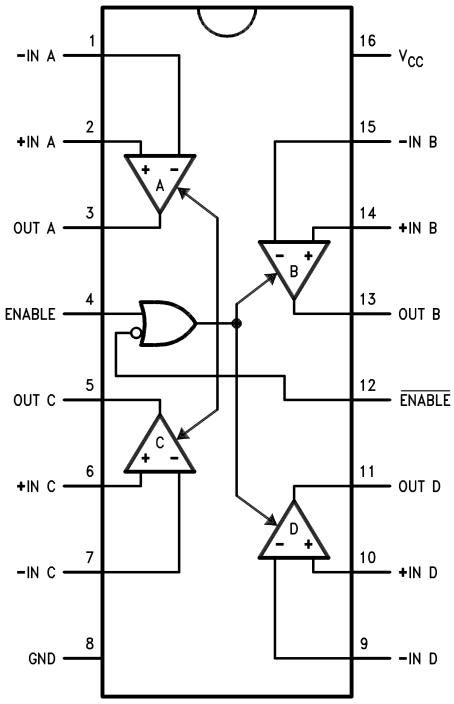

Figure 1. 16-Lead CDIP Package-Top View
See Package Number NAC0016A, NFE0016A, or NAD0016A

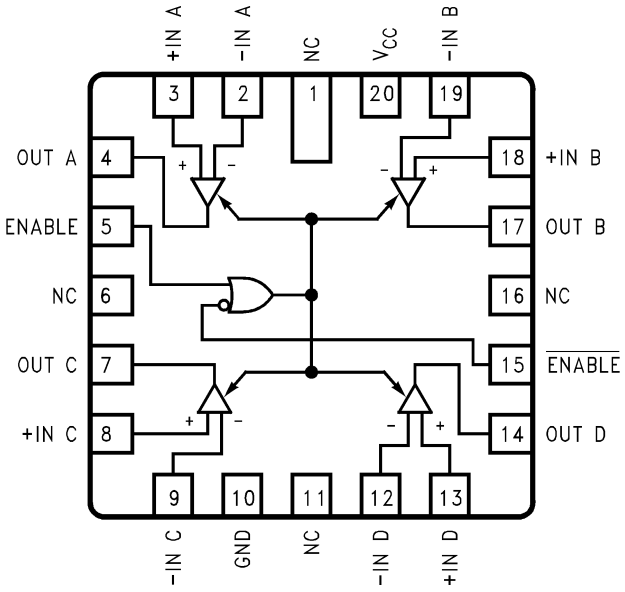

Figure 2. 20-Lead LCCC Package-Top View
See Package Number NAJ0020A

Table 1. Function Table (Each Receiver)(1)

Differential Inputs	Enables		Outputs
$V_{ID} = (V_I+) - (V_I-)$	E	$\overline{E}$	OUT
$V_{ID} \geq 0.2V$	H	X	H
	X	L	H
$V_{ID} \leq -0.2V$	H	X	L
	X	L	L
X	L	H	Z

(1) H = High Level
L = Low Level
X = Immaterial

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings (1)

Storage Temperature Range	−65°C ≤ T_A ≤ +150°C
Operating Temperature Range	−55°C ≤ T_A ≤ +125°C
Lead Temperature (soldering, 60 sec)	300°C
Supply Voltage	7.0V
Common Mode Voltage Range	±25V
Differential Input Voltage	±25V
Enable Voltage	7.0V
Output Sink Current	50 mA
Maximum Power Dissipation ($P_{D\ max}$at 25°C) (2), (3)	500 mW
Thermal Resistance	
θ_{JA}	
NFE0016A package	100°C/W
NAD0016A package	142°C/W
NAJ0020A package	87°C/W
θ_{JC}	
Junction-to- case	See MIL-STD-1835

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not verify specific performance limits. For verified specifications and test conditions, see the Electrical Characteristics. The verified specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) Derate J package 10.0mW/°C above +25°C, derate W package 7.1mW/°C above +25°C, derate E package 11.5mW/°C above +25°C.
(3) Power dissipation must be externally controlled at elevated temperatures.

Recommended Operating Range

Operating Temperature	−55°C ≤ T_A ≤ +125°C
Supply Voltage	4.5V to 5.5V

Table 2. Radiation Features

DS26F32MJRQMLV	100 krads (Si)
DS26F32MWRQMLV	100 krads (Si)
DS26F32MWGRQMLV	100 krads (Si)

Table 3. Quality Conformance Inspection Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp °C
1	Static tests at	25
2	Static tests at	125
3	Static tests at	-55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	-55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	-55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	-55
12	Settling time at	25
13	Settling time at	125
14	Settling time at	-55

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DS26F32 Electrical Characteristics DC Parameters

The following conditions apply, unless otherwise specified.

DC: V_{CC} = 5V (1)

Parameter		Test Conditions	Notes	Min	Max	Units	Sub-groups
I_{In}	Input Current	Pin under test V_{CC} = 4.5V, V_I = 15V Other inputs -15V ≤ V_I ≤ +15V			2.3	mA	1, 2, 3
		Pin under test V_{CC} = 5.5V, V_I = -15V Other inputs -15V ≤ V_I ≤ +15V			-2.8	mA	1, 2, 3
I_{IL}	Logical "0" Enable Current	V_{CC} = 5.5V, V_{En} = 0.4V			-360	µA	1, 2, 3
I_{IH}	Logical "1" Enable Current	V_{CC} = 5.5V, V_I = 2.7V			10	µA	1, 2, 3
I_I	Logical "1" Enable Current	V_{CC} = 5.5V, V_I = 5.5V			50	µA	1, 2, 3
V_{IK}	Input Clamp Voltage (Enable)	V_{CC} = 4.5V, I_I = -18mA			-1.5	V	1, 2, 3
V_{OH}	Logical "1" Output Voltage	V_{CC} = 4.5V, I_{OH} = -440µA, ΔV_I = 1V, $V\overline{En}$ = .8 = V_{En}		2.5		V	1, 2, 3
V_{OL}	Logical "0" Output Voltage	V_{CC} = 4.5V, $V\overline{En}$ =0.8V = V_{En}, I_{OL} = 4mA, ΔV_I = -1V			0.4	V	1, 2, 3
		V_{CC} = 4.5V, $V\overline{En}$ = 8V = V_{En}, I_{OL} = 8mA, ΔV_I = -1V			.45	V	1, 2, 3
I_{CC}	Supply Current	V_{CC} = 5.5V, All V_I = Gnd, V_{En} = 0V, $V\overline{En}$ = 2V			50	mA	1, 2, 3
I_{OZ}	Off-State Output Current	V_{CC} = 5.5V, V_O = 0.4V, V_{En} = 0.8V, $V\overline{En}$ = 2V			-20	µA	1, 2, 3
		V_{CC} = 5.5V, V_O = 2.4V, V_{En} = 0.8V, $V\overline{En}$ = 2V			20	µA	1, 2, 3
R_I	Input Resistance	-15 ≤ V_{CM} ≤ 15V		14		KΩ	1, 2, 3
V_{Th}	Differential Input Voltage	V_{CC} = 4.5V, V_{OUT} = V_{OL} or V_{OH} -7V ≤ V_{CM} ≤ 7V, V_{En} = $V\overline{En}$ = 2.5V	(2)	-0.2	0.2	V	1, 2, 3
		V_{CC} = 5.5V, V_{OUT} = V_{OL} or V_{OH} -7V ≤ V_{CM} ≤ 7V, V_{En} = $V\overline{En}$ = 2.5V	(2)	-0.2	0.2	V	1, 2, 3
V_{IL}	Logical "0" Input Voltage (Enable)	V_{CC} = 5.5V	(2)		0.8	V	1, 2, 3
V_{IH}	Logical "1" Input Voltage (Enable)	V_{CC} = 4.5V	(2)	2.0		V	1, 2, 3
$I_{SC\ Min}$	Output Short Circuit Current	V_{CC} = 4.5V, V_O = 0V, ΔV_I = 1V		-15		mA	1, 2, 3
$I_{SC\ Max}$	Output Short Circuit Current	V_{CC} = 5.5V, V_O = 0V, ΔV_I = 1V			-85	mA	1, 2, 3

(1) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are specified only for the conditions as specified in Mil-Std-883, Method 1019.5, Condition A

(2) Parameter tested go-no-go only.

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DS26F32 Electrical Characteristics AC Parameters

The following conditions apply, unless otherwise specified.
AC: V_{CC} = 5V (1)

Parameter		Test Conditions	Notes	Min	Max	Units	Sub-groups
t_{PLH}		C_L = 50pF	(2)		23	nS	9
			(2)		31	nS	10, 11
		C_L = 15pF	(3)		22	nS	9
			(3)		30	nS	10, 11
t_{PHL}		C_L = 50pF	(2)		23	nS	9
			(2)		31	nS	10, 11
		C_L = 15pF	(3)		22	nS	9
			(3)		30	nS	10, 11
t_{PZH}	Enable Time	C_L = 50pF	(2)		18	nS	9
			(2)		29	nS	10, 11
		C_L = 15pF	(3)		16	nS	9
			(3)		27	nS	10, 11
t_{PZL}	Enable Time	C_L = 50pF	(2)		20	nS	9
			(2)		29	nS	10, 11
		C_L = 15pF	(3)		18	nS	9
			(3)		27	nS	10, 11
t_{PHZ}	Disable Time	C_L = 50pF	(2)		55	nS	9
			(2)		62	nS	10, 11
		C_L = 5pF	(3)		20	nS	9
			(3)		27	nS	10, 11
t_{PLZ}	Disable Time	C_L = 50pF	(2)		30	nS	9
			(2)		42	nS	10, 11
		C_L = 5pF	(3)		18	nS	9
			(3)		30	nS	10, 11

(1) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are specified only for the conditions as specified in Mil-Std-883, Method 1019.5, Condition A
(2) Tested at 50pF, system capacitance exceeds 5pF to 15pF.
(3) Tested at 50pF specifies limit at 15pF & 5pF.

DS26F32 Electrical Characteristics DC Drift Parameters

This section applies to -QMLV devices only. Devices shall be read & recorded at T_A = 25°C before and after each burn-in and shall not change by more than the limits indicated. The delta rejects shall be included in the PDA calculation.

Parameter		Test Conditions	Notes	Min	Max	Units	Sub-groups
V_{OH}	Logical "1" Output Voltage	V_{CC} = 4.5V, I_{OH} = -440µA, ΔV_I = 1V, $\overline{VEn}$ = 0.8V = V_{En}		-250	250	mV	1
V_{OL}	Logical "0" Output Voltage	V_{CC} = 4.5V, I_{OL} = 4mA, ΔV_I = -1V, $\overline{VEn}$ = 0.8V = V_{En}		-45	45	mV	1
		V_{CC} = 4.5V, I_{OL} = 8mA, ΔV_I = -1V, $\overline{VEn}$ = 0.8V = V_{En}		-45	45	mV	1
I_I	Input Current	Pin under test V_{CC} = 4.5V, V_I = 15V Other inputs -15V ≤ V_I ≤ +15V		-0.28	0.28	mA	1
		Pin under test V_{CC} = 5.5V, V_I = -15V Other inputs -15V ≤ V_I ≤ +15V		-0.28	0.28	mA	1

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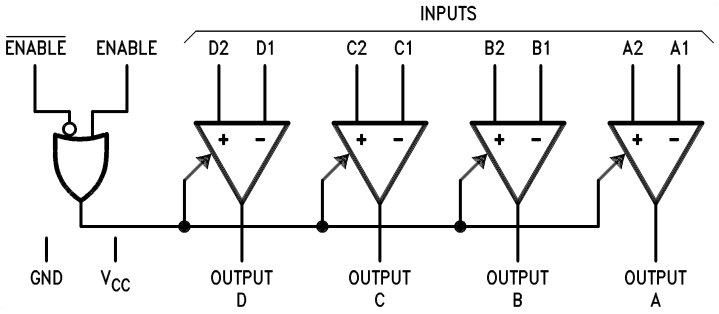
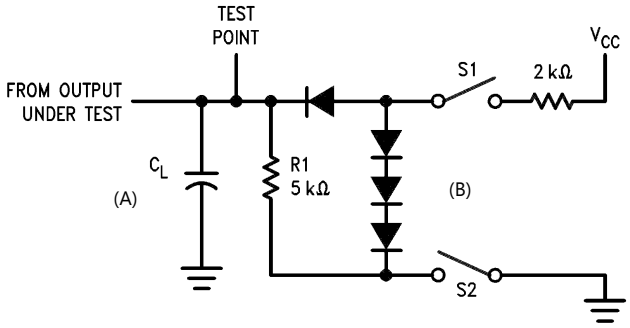


Figure 3. Logic Symbol



C_L includes probe and jig capacitance.

A. Parameter tested go-no-go only.

B. Tested at 50pF specifies limit at 15pF and 5pF.

Figure 4. Load Test Circuit for Three-State Outputs

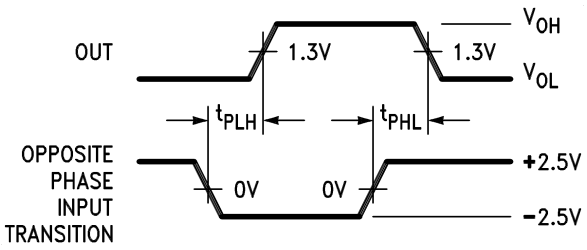


Diagram shown for $\overline{\text{ENABLE}}$ Low.

S1 and S2 of Load Circuit are closed except where shown.

Pulse Generator of all Pulses: Rate ≤ 1.0 MHz, Z_O = 50Ω, t_r ≤ 6.0 ns, t_f ≤ 6.0 ns.

Figure 5. Propagation Delay

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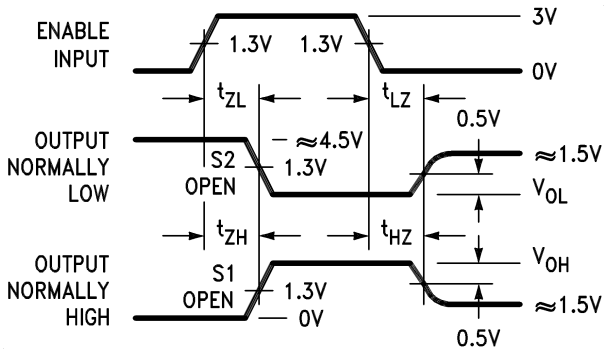


Diagram shown for $\overline{\text{ENABLE}}$ Low.

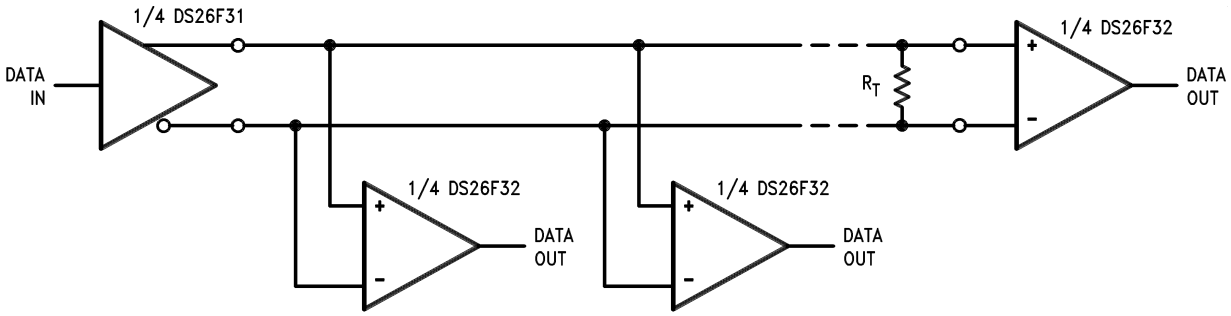
S1 and S2 of Load Circuit are closed except where shown.

Pulse Generator of all Pulses: Rate ≤ 1.0 MHz, Z_O = 50Ω, t_r ≤ 6.0 ns, t_f ≤ 6.0 ns.

All diodes are IN916 or IN3064.

Figure 6. Enable and Disable Times

TYPICAL APPLICATION



REVISION HISTORY

Released	Revision	Section	Originator	Changes
3/01/06	*	New Release, Corporate format	L. Lytle	1 MDS data sheet converted into one Corp. data sheet format. MNDS26F32M-X-RH Rev 0C0 will be archived.
4/15/2013	A		TIS	Changed layout of National Data Sheet to TI format

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-7802005M2A	Active	Production	LCCC (NAJ) | 20	50 | TUBE	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	DS26F32ME/ 883 Q 5962-78020 05M2A ACO 05M2A >T
5962-7802005MFA	Active	Production	CFP (NAD) | 16	19 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	DS26F32MW /883 Q 5962-78020 05MFA ACO 05MFA >T
5962R7802005VEA	Active	Production	CDIP (NFE) | 16	25 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	DS26F32MJRQMLV 5962R7802005VEA Q
5962R7802005VFA	Active	Production	CFP (NAD) | 16	19 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	DS26F32MWR QMLV Q 5962R78020 05VFA ACO 05VFA >T
DS26F32 MW8	Active	Production	WAFERSALE (YS) | 0	1 | OTHER	-	Call TI	Level-1-NA-UNLIM	-55 to 125	
DS26F32ME/883	Active	Production	LCCC (NAJ) | 20	50 | TUBE	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	DS26F32ME/ 883 Q 5962-78020 05M2A ACO 05M2A >T
DS26F32MJRQMLV	Active	Production	CDIP (NFE) | 16	25 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	DS26F32MJRQMLV 5962R7802005VEA Q
DS26F32MJRQMLV.A	Active	Production	CDIP (NFE) | 16	25 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	DS26F32MJRQMLV 5962R7802005VEA Q
DS26F32MW/883	Active	Production	CFP (NAD) | 16	19 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	DS26F32MW /883 Q 5962-78020 05MFA ACO 05MFA >T

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS26F32MWRQMLV	Active	Production	CFP (NAD) | 16	19 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	DS26F32MWR QMLV Q 5962R78020 05VFA ACO 05VFA >T
DS26F32MWRQMLV.A	Active	Production	CFP (NAD) | 16	19 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	DS26F32MWR QMLV Q 5962R78020 05VFA ACO 05VFA >T

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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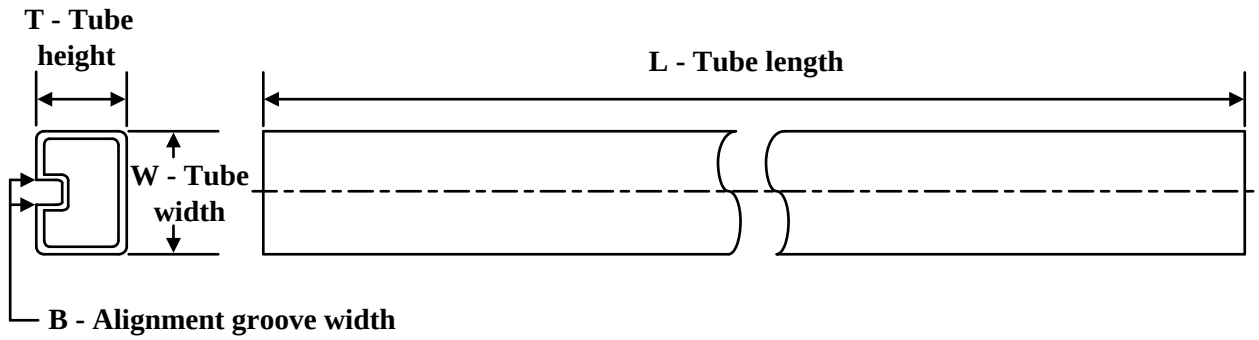
OTHER QUALIFIED VERSIONS OF DS26F32MQML, DS26F32MQML-SP :

- Military : DS26F32MQML
- Space : DS26F32MQML-SP

NOTE: Qualified Version Definitions:

- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-7802005M2A	NAJ	LCCC	20	50	470	11	3810	0
5962-7802005MFA	NAD	CFP	16	19	502	23	9398	9.78
5962R7802005VEA	NFE	CDIP	16	25	506.98	15.24	13440	NA
5962R7802005VFA	NAD	CFP	16	19	502	23	9398	9.78
DS26F32ME/883	NAJ	LCCC	20	50	470	11	3810	0
DS26F32MJRQMLV	NFE	CDIP	16	25	506.98	15.24	13440	NA
DS26F32MJRQMLV.A	NFE	CDIP	16	25	506.98	15.24	13440	NA
DS26F32MW/883	NAD	CFP	16	19	502	23	9398	9.78
DS26F32MWRQMLV	NAD	CFP	16	19	502	23	9398	9.78
DS26F32MWRQMLV.A	NAD	CFP	16	19	502	23	9398	9.78

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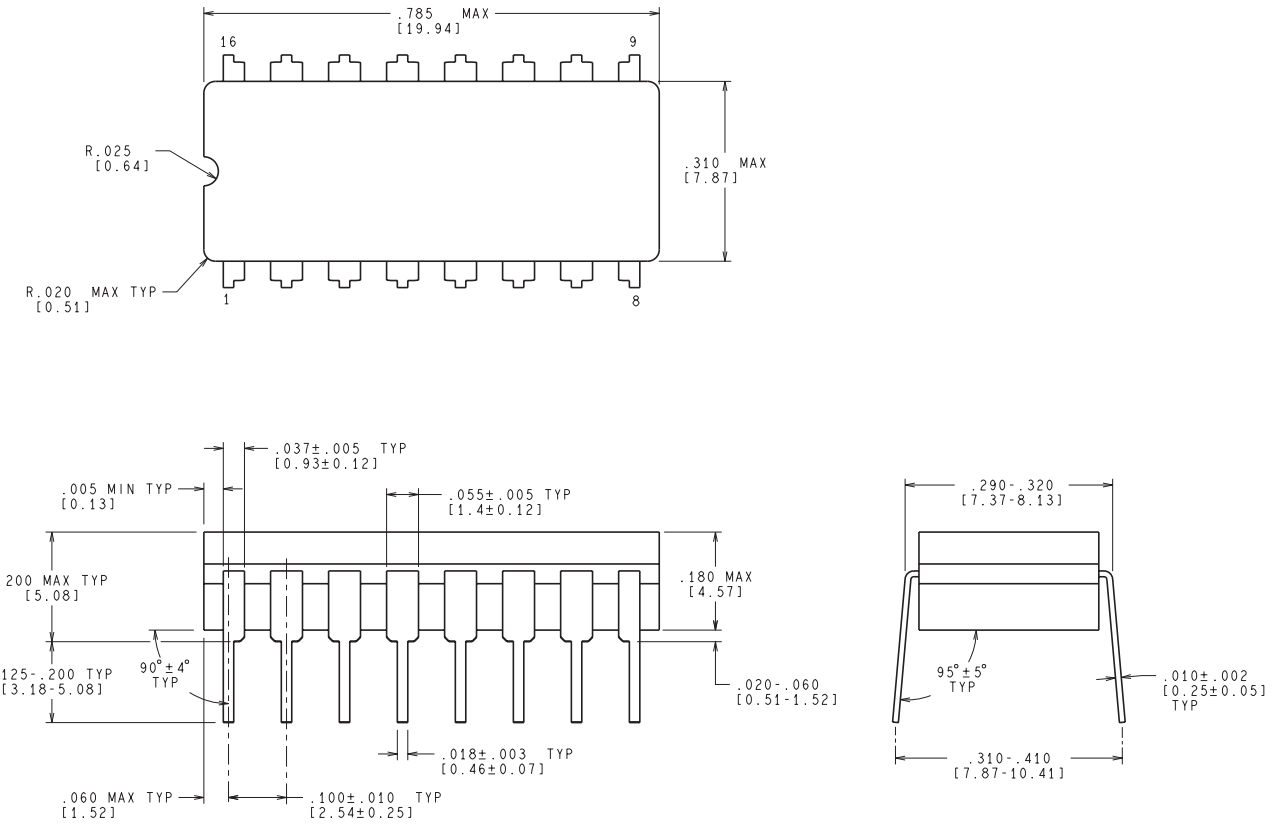

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J16A (REV L)

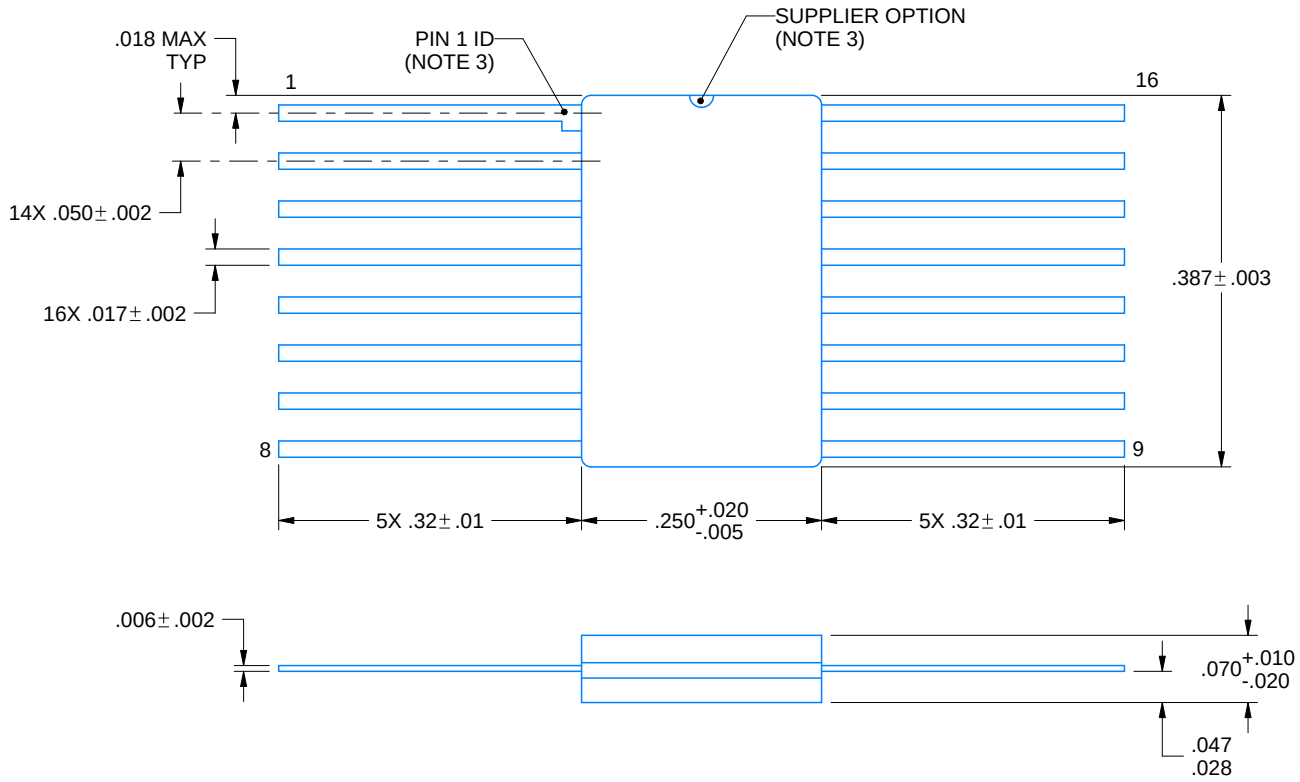
NAD0016A



PACKAGE OUTLINE

CFP - 2.03 mm max height

CERAMIC FLATPACK



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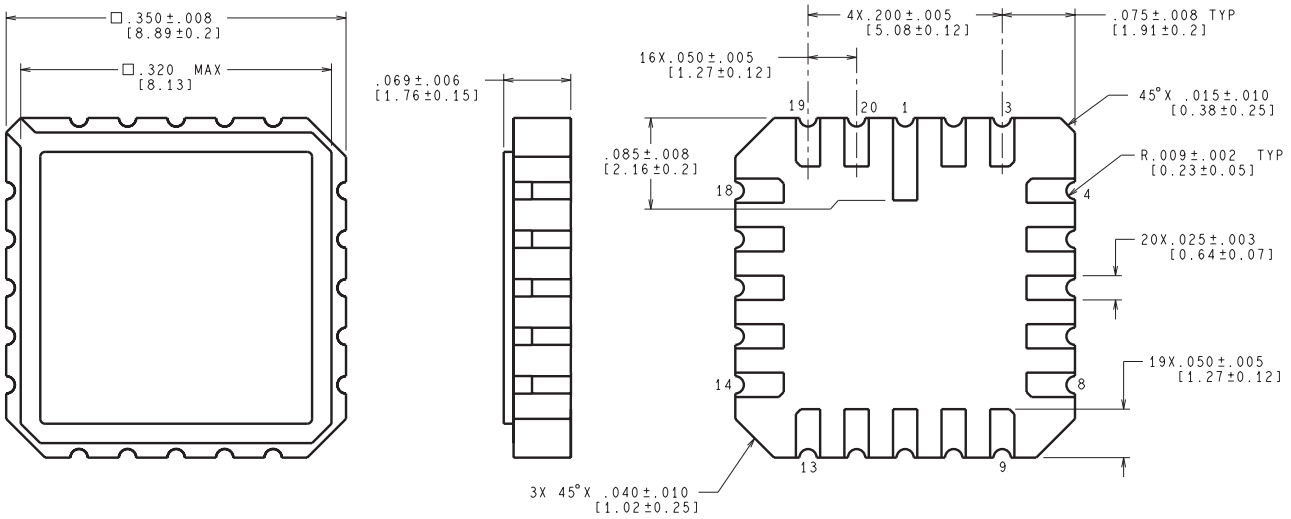
NOTES:

1. All linear dimensions are in inches. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead 1 identification shall be:
   a) A notch or other mark within this area
   b) A tab on lead 1, either side

NAJ0020A



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