DS90C032QML LVDS Quad CMOS Differential Line Receiver

Check for Samples: DS90C032QML

FEATURES

- **Single Event Latchup (SEL) Immune 120 MeV-cm²/mg**
- **High Impedance LVDS Inputs with Power-Off.**
- **Accepts Small Swing (330 mV) Differential Signal Levels**
- **Low Power Dissipation**
- **Low Differential Skew**
- **Low Chip to Chip Skew**
- **Pin Compatible with DS26C32A**
- **Compatible with IEEE 1596.3 SCI LVDS Standard**

DESCRIPTION

The DS90C032 is a quad CMOS differential line receiver designed for applications requiring ultra low power dissipation and high data rates.

The DS90C032 accepts low voltage differential input signals and translates them to CMOS (TTL compatible) output levels. The receiver supports a TRI-STATE function that may be used to multiplex outputs. The receiver also supports OPEN Failsafe and terminated (100Ω) input Failsafe with the addition of external failsafe biasing. Receiver output will be HIGH for both Failsafe conditions.

The DS90C032 provides power-off high impedance LVDS inputs. This feature assures minimal loading effect on the LVDS bus lines when VCC is not present.

The DS90C032 and companion line driver (DS90C031) provide a new alternative to high power pseudo-ECL devices for high speed point-to-point interface applications.

Connection Diagrams

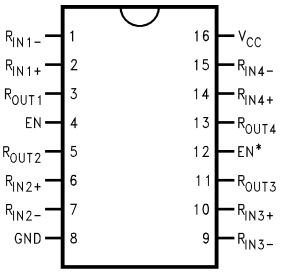


Figure 1. Dual-In-Line
See Package Number NAD0016A & NAC0016A

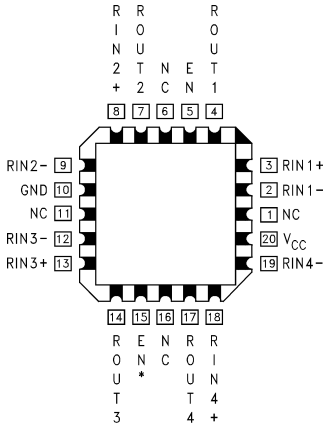


Figure 2. LCCC Package
See Package Number NAJ0020A

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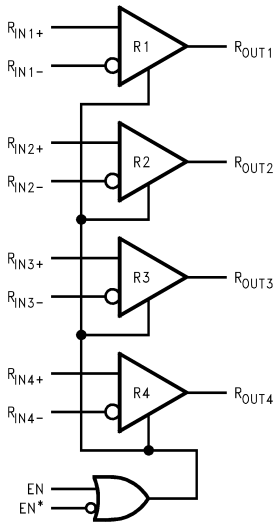
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Functional Diagram and Truth Table

Block Diagram



Receiver

ENABLES		INPUTS	OUTPUT
EN	**EN***	**$R_{I+} - R_{I-}$**	**R_O**
L	H	X	Z
All other combinations of ENABLE inputs		$V_{ID} \geq 0.1V$	H
		$V_{ID} \leq -0.1V$	L

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)

Supply Voltage (V_{CC})	−0.3V to +6V
Input Voltage (R_I+, R_I−)	−0.3V to +5.8V
Enable Input Voltage (EN, EN*)	−0.3V to (V_{CC} +0.3V)
Output Voltage (R_O)	−0.3V to (V_{CC} +0.3V)
Storage Temperature Range (T_{Stg})	−65°C ≤ T_A ≤ +150°C
Maximum Lead Temperature, Soldering (4 seconds)	+260°C
Maximum Package Power Dissipation at +25°C(2)	
LCCC Package	1830 mW
CLGA (NAD)	1400 mW
CLGA (NAC)	1400 mW
Thermal Resistance	
θ_{JA}	
LCCC Package	82°C/W
CLGA (NAD)	145°C/W
CLGA (NAC)	145°C/W
θ_{JC}	
LCCC Package	20°C/W
CLGA (NAD)	20°C/W
CLGA (NAC)	20°C/W
ESD Rating(3)	2KV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) Derate LCCC at 12.2mW/°C above +25°C. Derate CLGA at 6.8mW/°C above +25°C
(3) Human body model, 1.5 kΩ in series with 100 pF.

Recommended Operating Conditions

	Min	Typ	Max
Supply Voltage (V_{CC})	+4.5V	+5.0V	+5.5V
Receiver Input Voltage	Gnd		2.4V
Operating Free Air Temperature (T_A)	−55°C	+25°C	+125°C

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Quality Conformance Inspection

Table 1. Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Settling time at	+25
13	Settling time at	+125
14	Settling time at	-55

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DS90C032 Electrical Characteristics, DC Parameters(1)

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{ThL}	Differential Input Low Threshold	V_{CM} = +1.2V	See(2)		-100	mV	1, 2, 3
V_{ThH}	Differential Input High Threshold	V_{CM} = +1.2V	See(2)		100	mV	1, 2, 3
I_{In}	Input Current (Input Pins)	V_{CC}=5.5V, V_I = 2.4V			±10	µA	1, 2, 3
		V_{CC} = 5.5V, V_I = 0			±10	µA	1, 2, 3
		V_{CC} = 0.0V, V_I = 2.4V			±10	µA	1, 2, 3
		V_{CC} = 0.0V, V_I = 0.0V			±10	µA	1, 2, 3
V_{OH}	Output High Voltage	V_{CC}= 4.5V, I_{OH} = -0.4 mA, V_{ID} = 200mV		3.8		V	1, 2, 3
V_{OL}	Output Low Voltage	V_{CC} = 4.5, I_{OL} = 2 mA, V_{ID} = -200mV			0.3	V	1, 2, 3
I_{OS}	Output Short Circuit Current	Enabled, V_O = 0V		-15	-100	mA	1, 2, 3
I_{OZ}	Output TRI-STATE Current	Disabled, V_O = 0V or V_{CC}			±10	µA	1, 2, 3
V_{IH}	Input High Voltage		See(2)	2.0		V	1, 2, 3
V_{IL}	Input Low Voltage		See(2)		0.8	V	1, 2, 3
I_I	Input Current (Enable Pins)	V_{CC} = 5.5V			±10	µA	1, 2, 3
V_{CL}	Input Clamp Voltage	I_{CI} = -18mA			-1.5	V	1, 2, 3
I_{CC}	No Load Supply Current	EN, EN* = V_{CC} or Gnd, Inputs Open			11	mA	1, 2, 3
		EN, EN* = 2.4 or 0.5, Inputs Open			11	mA	1, 2, 3
I_{CCZ}	No Load Supply Current Receivers Disabled	EN = Gnd, EN* = V_{CC} , Inputs Open			11	mA	1, 2, 3

(1) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the “Post Radiation Limits” table. Radiation end point limits for the noted parameters are ensured only for the conditions, as specified.
(2) Tested during V_{OH} and V_{OL} tests.

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DS90C032 Electrical Characteristics, AC Parameters(1)

The following conditions apply, unless otherwise specified.
AC: V_{CC} = 4.5V / 5.0V / 5.5V, C_L = 20pF

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
t_{PHLD}	Differential Propagation Delay High to Low	V_{ID} = 200mV, Input pulse = 1.1V to 1.3V, V_I = 1.2V (0V differential) to V_O = 1/2 V_{CC}		1.0	8.0	ns	9, 10, 11
t_{PLHD}	Differential Propagation Delay Low to High	V_{ID} = 200mV, Input pulse = 1.1V to 1.3V, V_I = 1.2V (0V differential) to V_O = 1/2 V_{CC}		1.0	8.0	ns	9, 10, 11
t_{SkD}	Differential Skew $\lvert t_{PHLD} - t_{PLHD} \rvert$	C_L = 20pF, V_{ID} = 200mV			3.0	ns	9, 10, 11
t_{Sk1}	Channel to Channel Skew	C_L = 20pF, V_{ID} = 200mV	See(2)		3.0	ns	9, 10, 11
t_{Sk2}	Chip to Chip Skew	C_L = 20pF, V_{ID} = 200mV	See(3)		7.0	ns	9, 10, 11
t_{PLZ}	Disable Time Low to Z	Input pulse = 0V to 3.0V, V_O = V_{OL}+ 0.5V, R_L = 1KΩ to V_{CC}, V_I = 1.5V			20	ns	9, 10, 11
t_{PHZ}	Disable Time High to Z	Input pulse = 0V to 3.0V, V_I = 1.5V, V_O = V_{OH}- 0.5V, R_L = 1KΩ to Gnd			20	ns	9, 10, 11
t_{PZH}	Enable Time Z to High	Input pulse = 0V to 3.0V, V_I = 1.5V, V_O = 50%, R_L = 1KΩ to Gnd			20	ns	9, 10, 11
t_{PZL}	Enable Time Z to Low	Input pulse = 0V to 3.0V, V_I = 1.5V, V_O = 50%, R_L = 1KΩ to V_{CC}			20	ns	9, 10, 11

(1) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the “Post Radiation Limits” table. Radiation end point limits for the noted parameters are ensured only for the conditions, as specified.
(2) Channel-to-Channel Skew is defined as the difference between the propagation delay of one channel and that of the others on the same chip with an event on the inputs.
(3) Chip-to-Chip Skew is defined as the difference between the minimum and maximum specified differential propagation delays.

DS90C032 Electrical Characteristics, AC/DC Post Radiation Limits(1)

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
I_{CC}	No Load Supply Current	EN, EN* = V_{CC} or Gnd, Inputs Open			20	mA	1
		EN, EN* = 2.4 or 0.5, Inputs Open			20	mA	1
I_{CCZ}	No Load Supply Current Receivers Disabled	EN = Gnd, EN* = V_{CC}, Inputs Open			20	mA	1

(1) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the “Post Radiation Limits” table. Radiation end point limits for the noted parameters are ensured only for the conditions, as specified.

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Parameter Measurement Information

Figure 3.

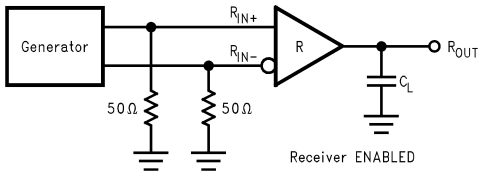


Figure 4. Receiver Propagation Delay and Transition Time Test Circuit

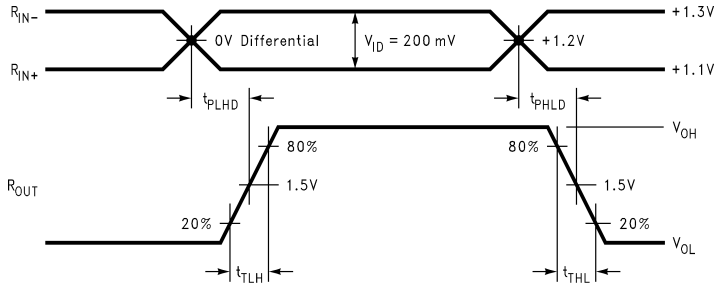
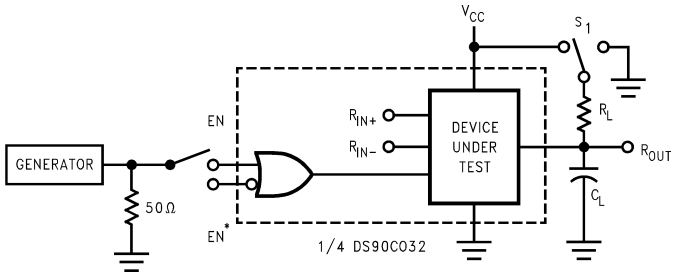


Figure 5. Receiver Propagation Delay and Transition Time Waveforms



A. C_L includes load and test jig capacitance.

B. $S_1 = V_{CC}$ for t_{PZL} and t_{PLZ} measurements.

C. S_1 = Gnd for t_{PZH} and t_{PHZ} measurements.

Figure 6. Receiver TRI-STATE Delay Test Circuit

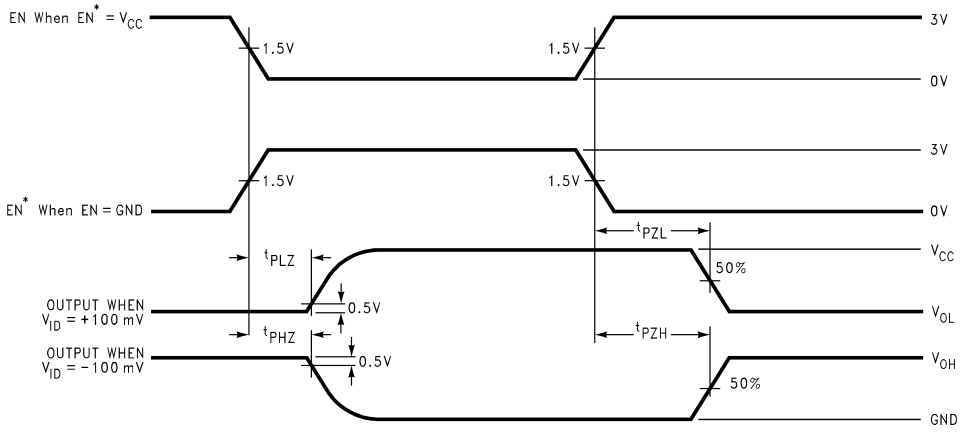


Figure 7. Receiver TRI-STATE Delay Waveforms

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Typical Performance Characteristics

Output High Voltage vs Power Supply Voltage

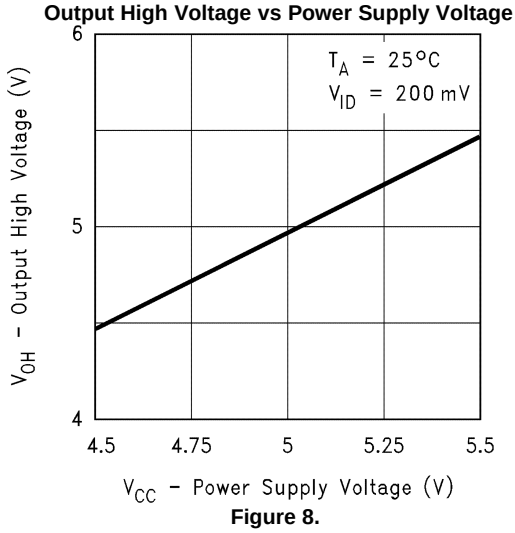


Figure 8.

Output High Voltage vs Ambient Temperature

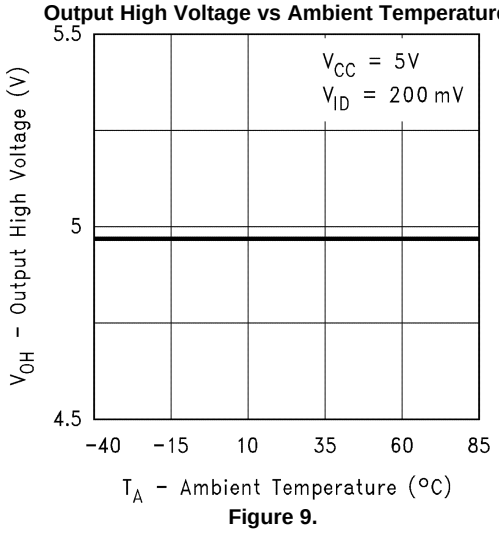


Figure 9.

Output Low Voltage vs Power Supply Voltage

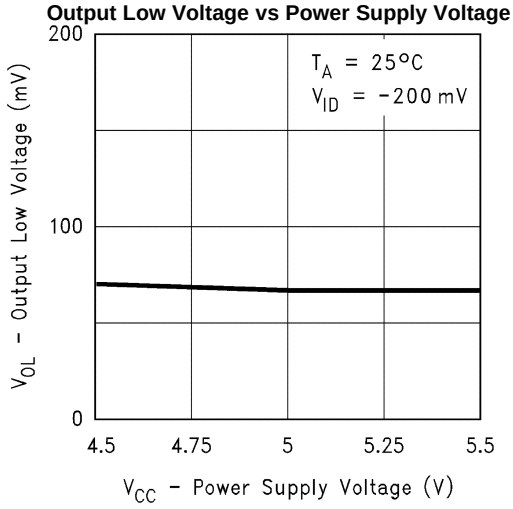


Figure 10.

Output Low Voltage vs Ambient Temperature

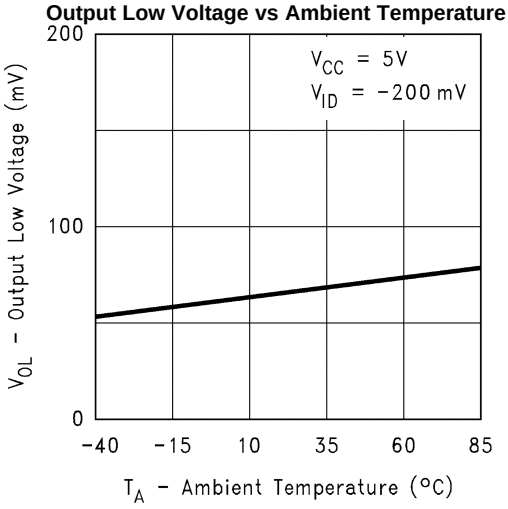


Figure 11.

Output Short Circuit Current vs Power Supply Voltage

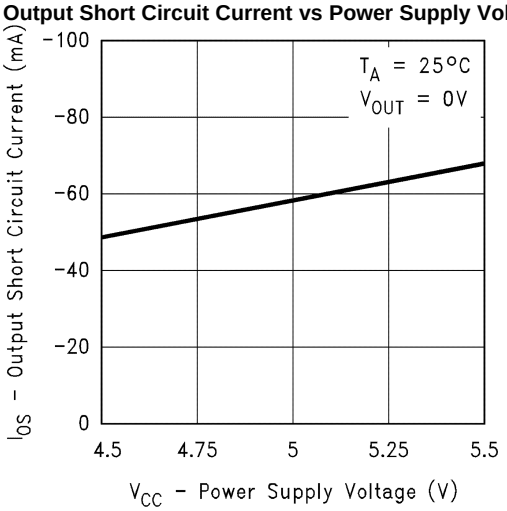


Figure 12.

Output Short Circuit Current vs Ambient Temperature

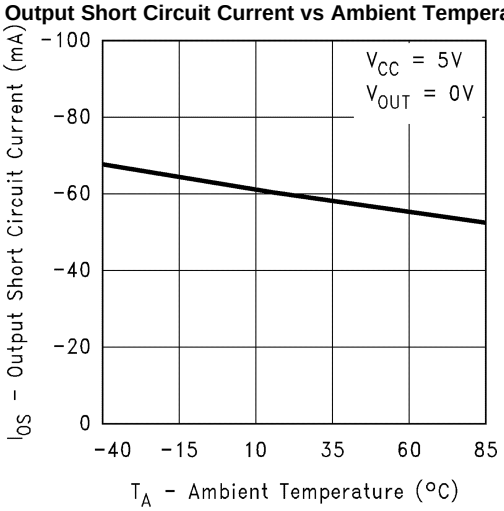


Figure 13.

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Typical Performance Characteristics (continued)

Differential Propagation Delay vs Power Supply Voltage

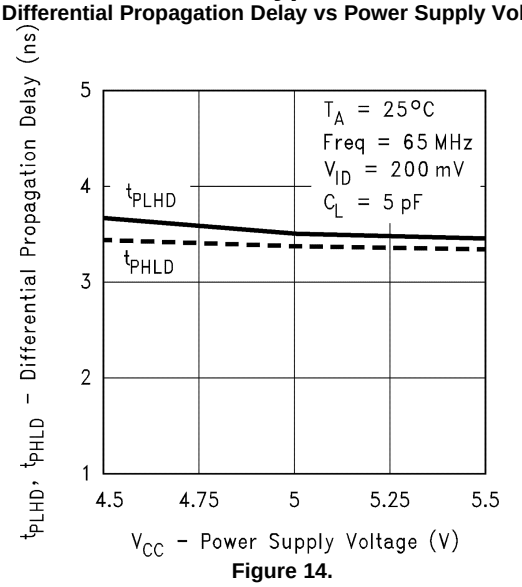


Figure 14.

Differential Propagation Delay vs Ambient Temperature

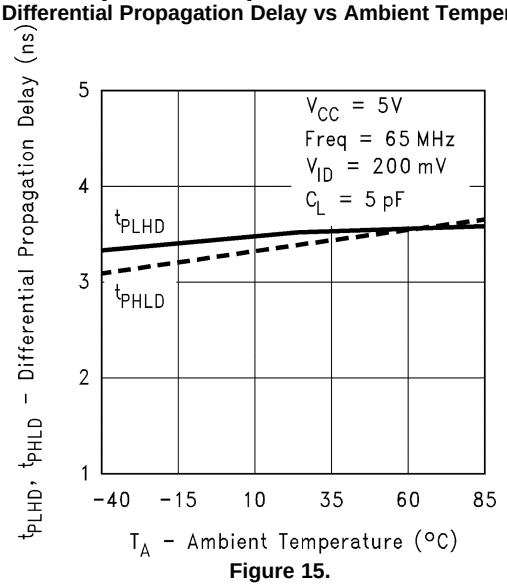


Figure 15.

Differential Skew vs Power Supply Voltage

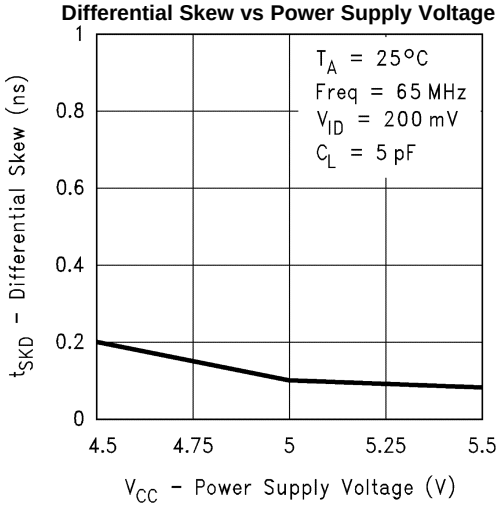


Figure 16.

Differential Skew vs Ambient Temperature

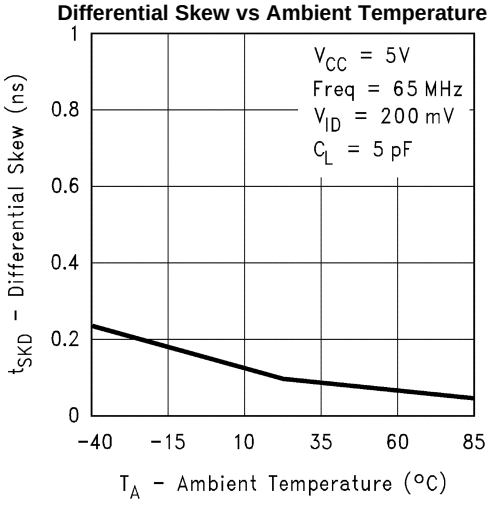


Figure 17.

Transition Time vs Power Supply Voltage

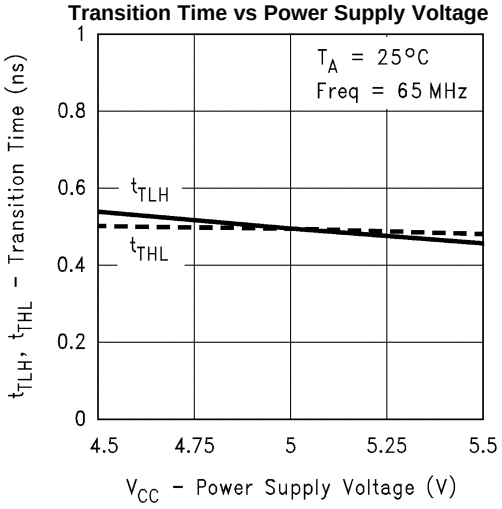


Figure 18.

Transition Time vs Ambient Temperature

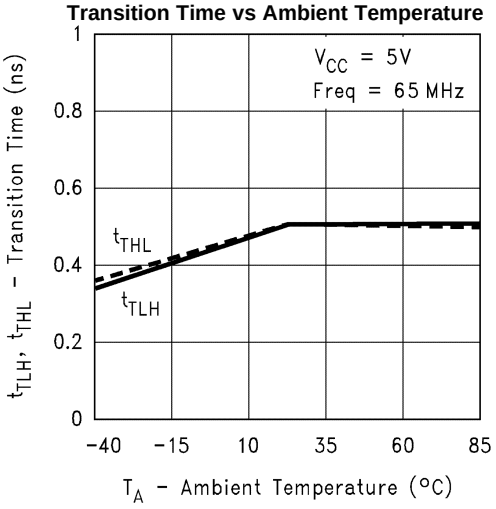


Figure 19.

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TYPICAL APPLICATION

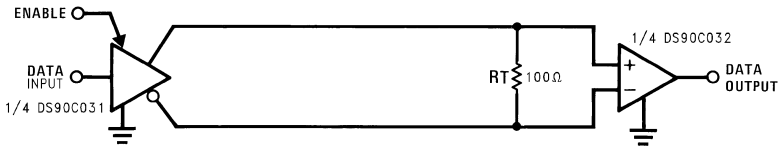


Figure 20. Point-to-Point Application

APPLICATIONS INFORMATION

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in *Figure 20.* This configuration provides a clean signaling environment for the quick edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically the characteristic impedance of the media is in the range of 100Ω. A termination resistor of 100Ω should be selected to match the media, and is located as close to the receiver input pins as possible. The termination resistor converts the current sourced by the driver into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

The DS90C032 differential line receiver is capable of detecting signals as low as 100 mV, over a ±1V common-mode range centered around +1.2V. This is related to the driver offset voltage which is typically +1.2V. The driven signal is centered around this voltage and may shift ±1V around this center point. The ±1V shifting may be the result of a ground potential difference between the driver's ground reference and the receiver's ground reference, the common-mode effects of coupled noise, or a combination of the two. Both receiver input pins should honor their specified operating input voltage range of 0V to +2.4V (measured from each pin to ground), exceeding these limits may turn on the ESD protection circuitry which will clamp the bus voltages.

Receiver Failsafe

The LVDS receiver is a high gain, high speed device that amplifies a small differential signal (20mV) to CMOS logic levels. Due to the high gain and tight threshold of the receiver, care should be taken to prevent noise from appearing as a valid signal.

The receiver’s internal failsafe circuitry is designed to source/sink a small amount of current, providing failsafe protection (a stable known state of HIGH output voltage) for floating and terminated (100Ω) receiver inputs in low noise environment (differential noise < 10mV).

- **Open Input Pins**

  TheDS90C032 is a quad receiver device, and if an application requires only 1, 2 or 3 receivers, the unused channel(s) inputs should be left OPEN. Do not tie unused receiver inputs to ground or any other voltages. The input is biased by internal high value pull up and pull down resistors to set the output to a HIGH state. This internal circuitry will ensure a HIGH, stable output state for open inputs.
- **Terminated Input**

  The DS90C032 requires external failsafe biasing for terminated input failsafe.

  Terminated input failsafe is the case of a receiver that has a 100Ω termination across its inputs and the driver is in the following situations. Unplugged from the bus, or the driver output is in TRI-STATE or in power-off condition. The use of external biasing resistors provide a small bias to set the differential input voltage while the line is un-driven, and therefore the receiver output will be in HIGH state. If the driver is removed from the bus but the cable is still present and floating, the unplugged cable can become a floating antenna that can pick up noise. The LVDS receiver is designed to detect very small amplitude and width signals and recover them to standard logic levels. Thus, if the cable picks up more than 10mV of differential noise, the receiver may respond. To insure that any noise is seen as commonmode and not differential, a balanced interconnect and twisted pair cables is recommended, as they help to ensure that noise is coupled common to both lines and rejected by the receivers.
- **Operation in environment with greater than 10mV differential noise**

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TI recommends external failsafe biasing on its LVDS receivers for a number of system level and signal quality reasons. First, only an application that requires failsafe biasing needs to employ it. Second, the amount of failsafe biasing is now an application design parameter and can be custom tailored for the specific application. In applications in low noise environments, they may choose to use a very small bias if any. For applications with less balanced interconnects and/or in high noise environments they may choose to boost failsafe further. TI's "LVDS Owner's Manual provides detailed calculations for selecting the proper failsafe biasing resistors. Third, the common-mode voltage is biased by the resistors during the un-driven state. This is selected to be close to the nominal driver offset voltage (VOS). Thus when switching between driven and un-driven states, the common-mode modulation on the bus is held to a minimum.

For additional Failsafe Biasing information, please refer to Application Note AN-1194 (SNLA051) for more detail.

Pin Descriptions

Pin No. (SOIC)	Name	Description
2, 6, 10, 14	R_{I+}	Non-inverting receiver input pin
1, 7, 9, 15	R_{I-}	Inverting receiver input pin
3, 5, 11, 13	R_O	Receiver output pin
4	EN	Active high enable pin, OR-ed with EN*
12	EN*	Active low enable pin, OR-ed with EN
16	V_{CC}	Power supply pin, +5V ± 10%
8	Gnd	Ground pin

Radiation Environments

Careful consideration should be given to environmental conditions when using a product in a radiation environment.

Total Ionizing Dose

Radiation hardness assured (RHA) products are those part numbers with a total ionizing dose (TID) level specified in the Ordering Information table on the front page. Testing and qualification of these products is done on a wafer level according to MIL-STD-883G, Test Method 1019.7, Condition A and the "Extended room temperature anneal test" described in section 3.11 for application environment dose rates less than 0.19 rad(Si)/s. Wafer level TID data is available with lot shipments.

Single Event Latch-Up and Functional Interrupt

One time single event latch-up (SEL) and single event functional interrupt (SEFI) testing was preformed according to EIA/JEDEC Standard, EIA/JEDEC57. The linear energy transfer threshold (LETth) shown in the Features on the front page is the maximum LET tested. A test report is available upon request.

Single Event Upset

A report on single event upset (SEU) is available upon request.

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Table 2. Revision History

Released	Revision	Section	Changes
3/01/06	A	New Release, Corporate format	1 MDS data sheet converted into Corp. data sheet format. MNDS90C032-X-RH Rev 1B1 will be archived.
10/10/06	B	Applications Information - Pg. 10, Physical Dimensions - Pg. 12	Deleted Shorted Inputs paragraph - page 10. Updated Physical Dimensions package drawings E20A, W16A to current revision - page 12. Revision A will be Archived.
9/28/2010	C	Receiver Table - Pg. 2, Application Information - Pg. 9 & 10 Order Information Table, General Description, Applications Information section	Deleted Full Fail-safe OPEN/SHORT or terminated - Page 2. & Paragraph RECEIVER FAIL-SAFE and 1, 2, 3 - Page 9 & 10. Revision B will be Archived. Copied general description and Receiver Failsafe from commercial d/s DS90C032B, dated Sept. 2003. Removed Code K devices. Added Radiation Environments paragraph to data sheet. Revision C will be Archived.
4/12/2013	D	New revision	Changed layout of National Data Sheet to TI format

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9583401Q2A	Active	Production	LCCC (NAJ) | 20	50 | TUBE	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	DS90C032E -QML Q 5962-95834 01Q2A ACO 01Q2A >T
5962-9583401VFA	Active	Production	CFP (NAD) | 16	19 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	DS90C032W-QMLV Q 5962-95834 01VFA ACO 01VFA >T
5962L9583401VFA	Active	Production	CFP (NAD) | 16	19 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	DS90C032WL QMLV Q 5962L95834 01VFA ACO 01VFA >T
5962L9583401VZA	Active	Production	CFP (NAC) | 16	88 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	DS90C032WGL QMLV Q 5962L95834 01VZA ACO 01VZA >T
DS90C032 MDR	Active	Production	DIESALE (Y) | 0	30 | OTHER	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	
DS90C032-MDR.A	Active	Production	DIESALE (Y) | 0	30 | OTHER	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	
DS90C032E-QML	Active	Production	LCCC (NAJ) | 20	50 | TUBE	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	DS90C032E -QML Q 5962-95834 01Q2A ACO 01Q2A >T
DS90C032E-QML.A	Active	Production	LCCC (NAJ) | 20	50 | TUBE	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	DS90C032E -QML Q 5962-95834 01Q2A ACO 01Q2A >T

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS90C032W-QMLV	Active	Production	CFP (NAD) | 16	19 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	DS90C032W- QMLV Q 5962-95834 01VFA ACO 01VFA >T
DS90C032W-QMLV.A	Active	Production	CFP (NAD) | 16	19 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	DS90C032W- QMLV Q 5962-95834 01VFA ACO 01VFA >T
DS90C032WGLQMLV	Active	Production	CFP (NAC) | 16	88 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	DS90C032WGL QMLV Q 5962L95834 01VZA ACO 01VZA >T
DS90C032WGLQMLV.A	Active	Production	CFP (NAC) | 16	88 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	DS90C032WGL QMLV Q 5962L95834 01VZA ACO 01VZA >T
DS90C032WLQMLV	Active	Production	CFP (NAD) | 16	19 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	DS90C032WL QMLV Q 5962L95834 01VFA ACO 01VFA >T
DS90C032WLQMLV.A	Active	Production	CFP (NAD) | 16	19 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	DS90C032WL QMLV Q 5962L95834 01VFA ACO 01VFA >T

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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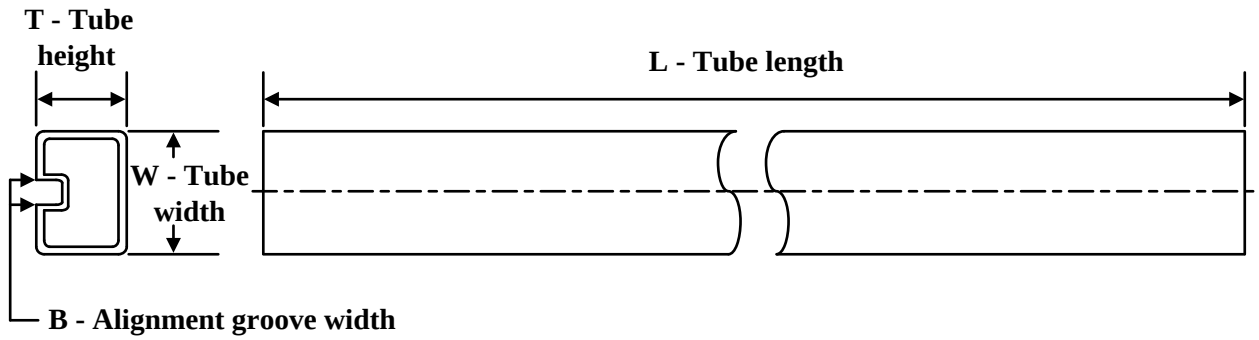
OTHER QUALIFIED VERSIONS OF DS90C032QML, DS90C032QML-SP :

- Military : DS90C032QML
- Space : DS90C032QML-SP

NOTE: Qualified Version Definitions:

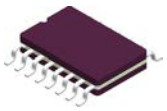
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9583401Q2A	NAJ	LCCC	20	50	470	11	3810	0
5962-9583401VFA	NAD	CFP	16	19	502	23	9398	9.78
5962L9583401VFA	NAD	CFP	16	19	502	23	9398	9.78
DS90C032E-QML	NAJ	LCCC	20	50	470	11	3810	0
DS90C032E-QML.A	NAJ	LCCC	20	50	470	11	3810	0
DS90C032W-QMLV	NAD	CFP	16	19	502	23	9398	9.78
DS90C032W-QMLV.A	NAD	CFP	16	19	502	23	9398	9.78
DS90C032WLQMLV	NAD	CFP	16	19	502	23	9398	9.78
DS90C032WLQMLV.A	NAD	CFP	16	19	502	23	9398	9.78

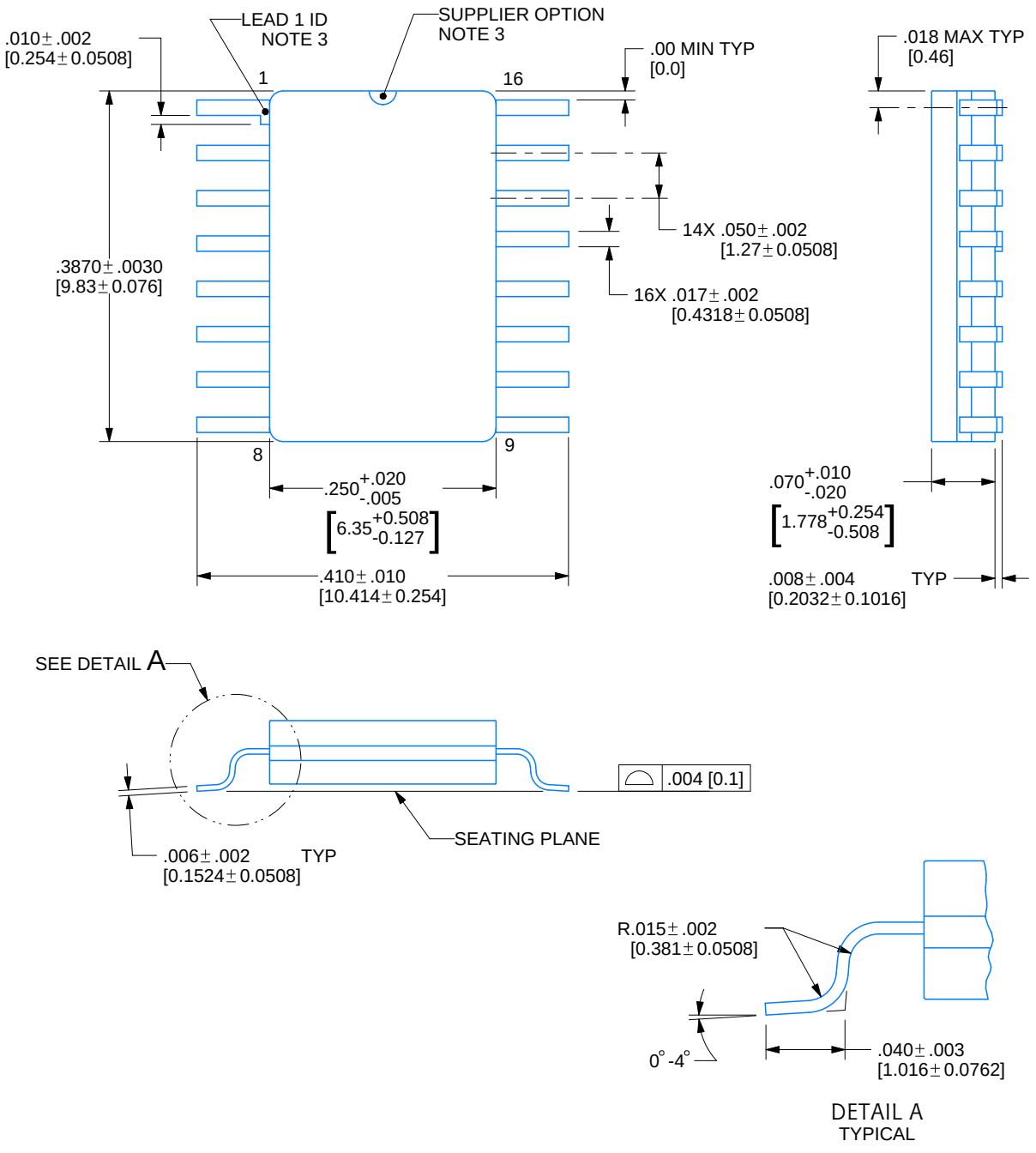


PACKAGE OUTLINE

NAC0016A

CFP - 2.33mm max height

CERAMIC FLATPACK



4215198/C 08/2022

NOTES:

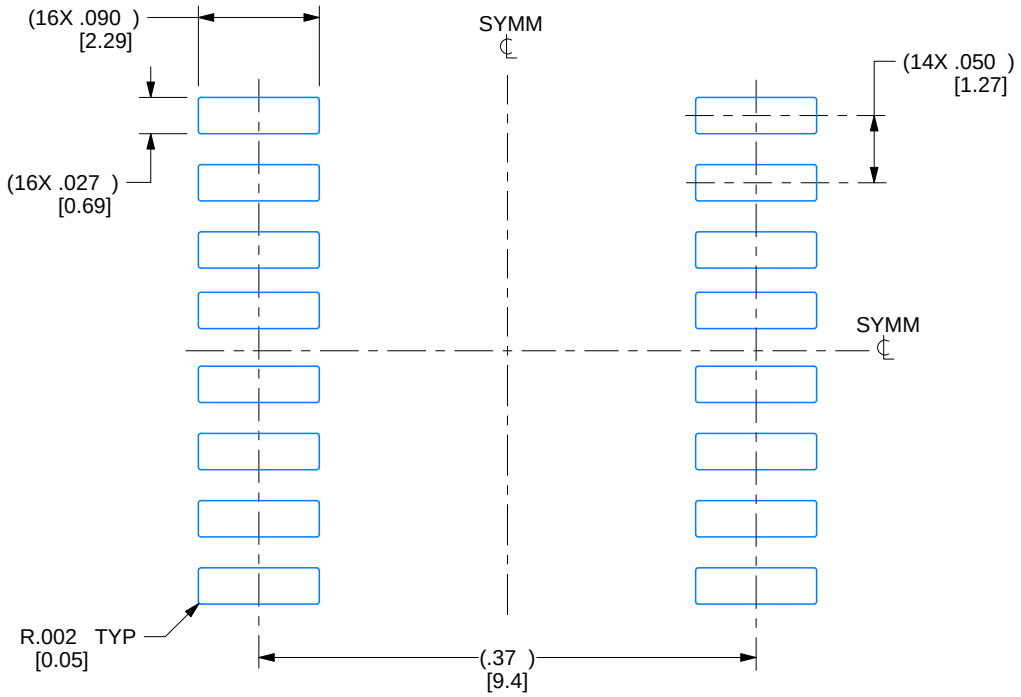
1. Controlling dimension is Inch. Values in [ ] are milimeters. Dimensions in ( ) for reference only.
2. For solder thickness and composition, see the "Lead Finish Composition/Thickness" link in the packaging section of the Texas Instruments website
3. Lead 1 identification shall be:
   a) A notch or other mark within this area
   b) A tab on lead 1, either side
4. No JEDEC registration as of December 2021

EXAMPLE BOARD LAYOUT

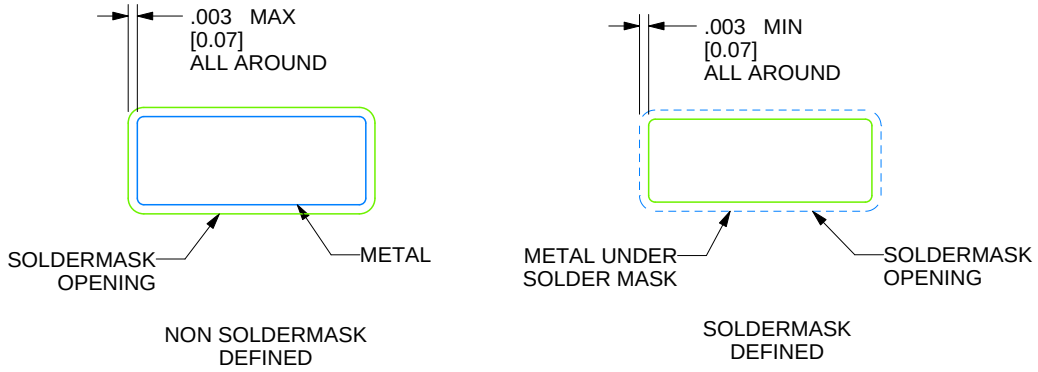
NAC0016A

CFP - 2.33mm max height

CERAMIC FLATPACK



RECOMMENDED LAND PATTERN



4215198/C 08/2022

REVISIONS

REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	2197879	12/30/2021	TINA TRAN / ANIS FAUZI
B	NO CHANGE TO DRAWING; REVISION FOR YODA RELEASE;	2198832	02/15/2022	K. SINCERBOX
C	.387± .003 WAS .39000± .00012;	2200917	08/08/2022	D. CHIN / K. SINCERBOX

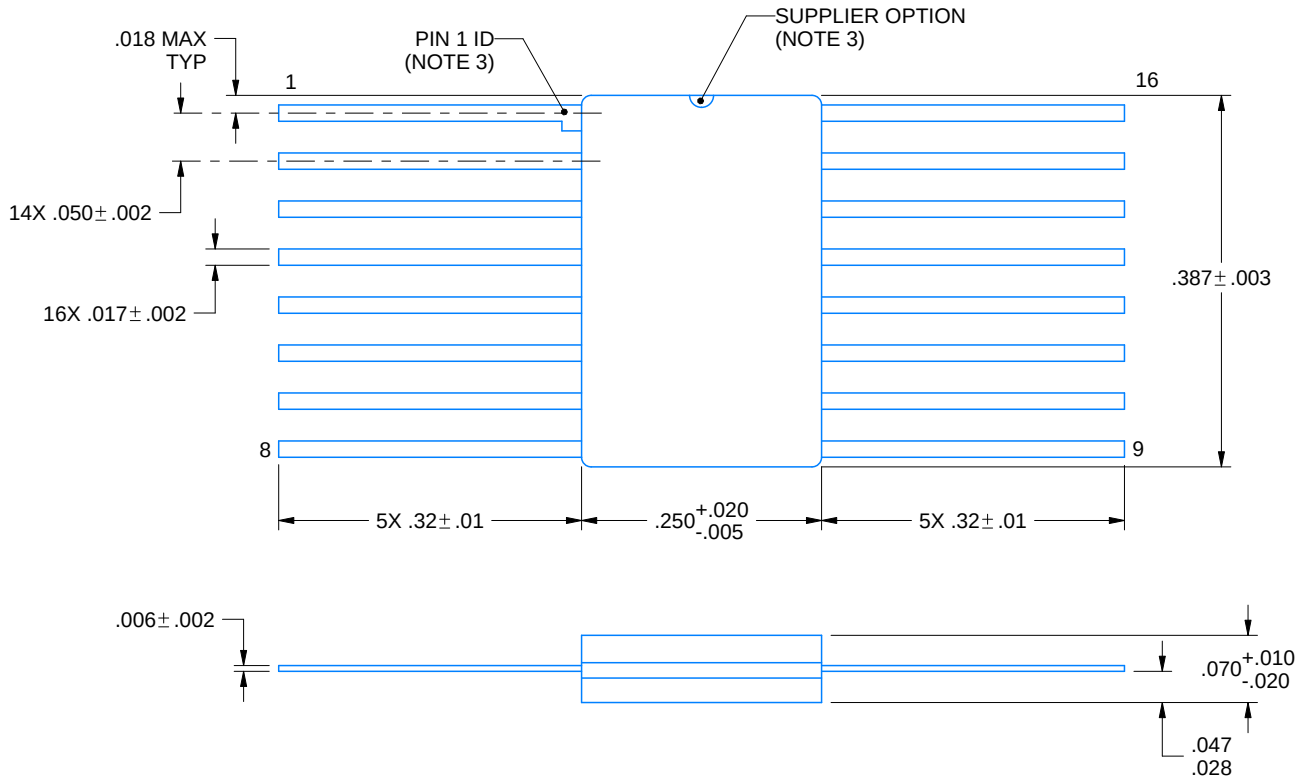
NAD0016A



PACKAGE OUTLINE

CFP - 2.03 mm max height

CERAMIC FLATPACK

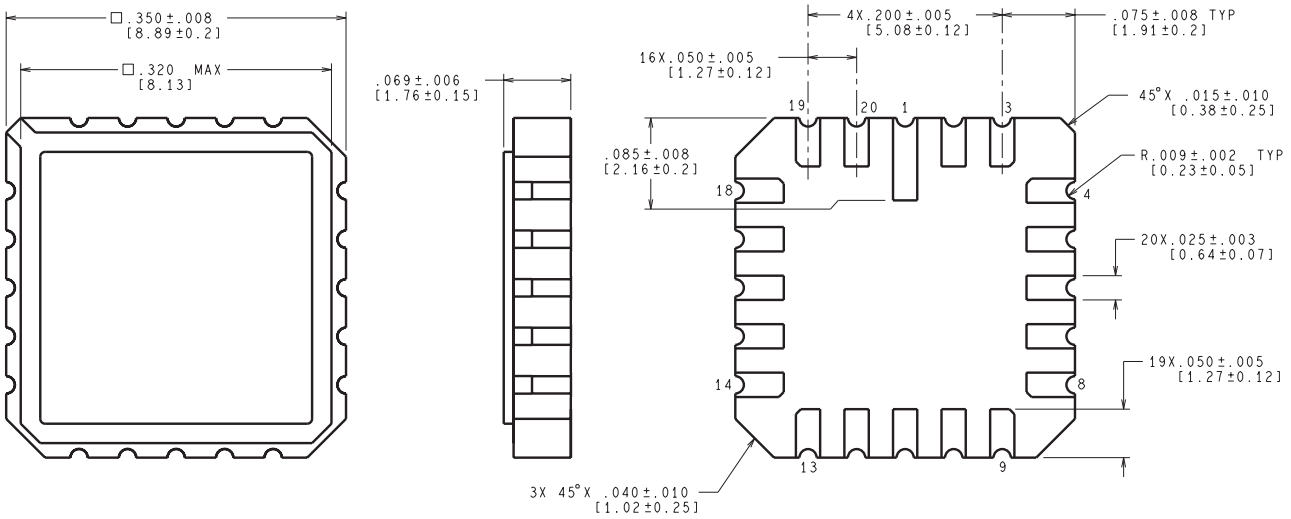


4215193/A 07/2026

NOTES:

1. All linear dimensions are in inches. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead 1 identification shall be:
   a) A notch or other mark within this area
   b) A tab on lead 1, either side

NAJ0020A



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

E20A (Rev F)

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