EMB1499Q Bidirectional Current DC-DC Controller

Check for Samples: EMB1499Q

FEATURES

- **60-V Maximum Stack Operating Voltage**
- **Bidirectional Balancing Current**
- **Fully Synchronous Operation**
- **Active Clamp Signal**
- **250-kHz Switching Frequency**
- **Fault Detection Includes Two Separate UVLO Cells (One for Each External Supply), Primary and Secondary Side Current Limit, OVP/UVP Sense on Cell Being Charged, Thermal Shutdown, and Watchdog Timer**
- **Balancing Current User-selectable Through External Voltage**
- **EMB1499Q is an Automotive Grade Product that is AEC-Q100 Grade 1 Qualified (–40°C to +125°C Operating Junction Temperature)**

APPLICATIONS

- **Li-Ion Battery Management Systems**
- **Hybrid and Electric Vehicles**
- **Grid Storage**

DESCRIPTION

The EMB1499Q bidirectional current dc/dc controller IC works in conjunction with the EMB1428 switch matrix gate driver IC to support TI's switch matrix based active cell balancing scheme for a battery management system. The EMB1499Q provides three PWM MOSFET gate signals to a bidirectional forward converter so that its output current, either positive or negative, is regulated around a user-defined magnitude. This inductor current is channeled by the EMB1428 through the switch matrix to the cell that needs to be charged or discharged. In a typical scheme, the EMB1499Q-based forward converter exchanges energy between a single cell and the battery stack to which it belongs, with a maximum stack voltage of up to 60 V. The switching frequency is fixed at 250 kHz. The EMB1499Q senses cell voltage, inductor current and stack current and provides protection from abnormal conditions during balancing.

The EMB1499Q also provides an active clamp timing signal to control an external FET driver for the primary-side active clamp FET. The EMB1499Q is enabled and disabled by the EMB1428. Fault conditions detected by the EMB1499Q are communicated to the EMB1428 through the DONE and FAULT pins.

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Typical Application

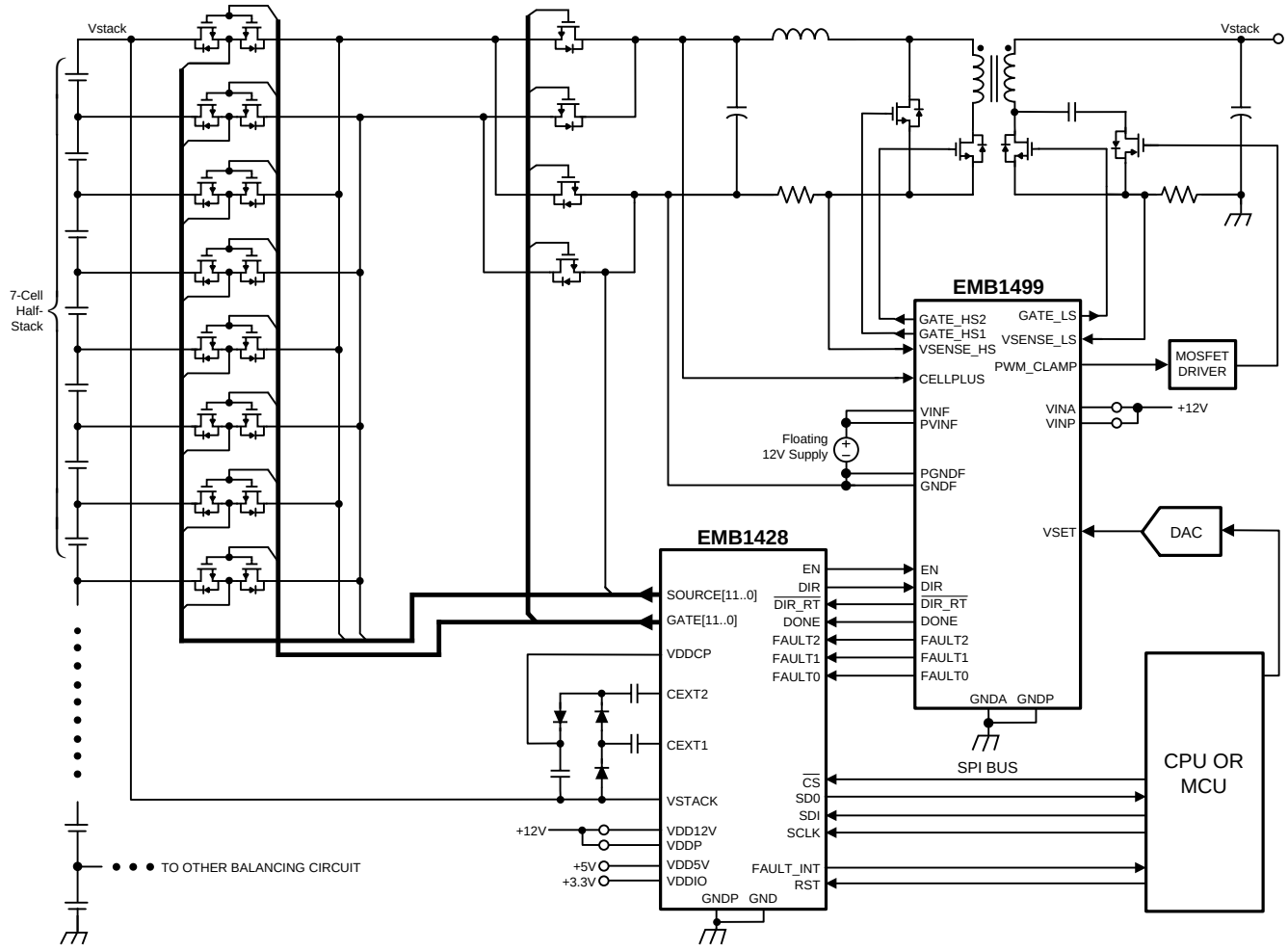


Figure 1. Typical Application

Connection Diagram

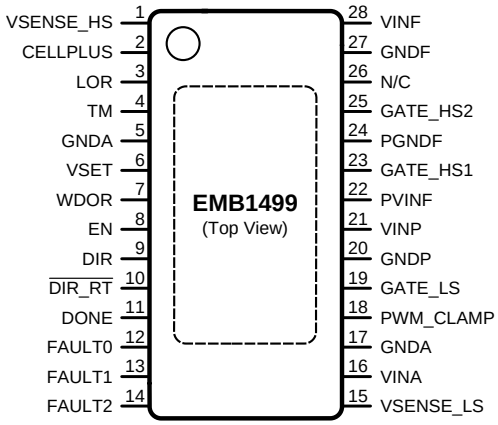


Figure 2. 28-Pin HTSSOP
See PWP Package

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PIN DESCRIPTIONS

Pin	Name	Description	Application Information
1	VSENSE_HS	Secondary side current sense input	Connect to transformer side of secondary sense resistor
2	CELLPLUS	Senses the cell voltage, used for OVP/UVP fault detection	Connect to top of secondary side of the converter. This is the top of the cell being charged.
3	LOR	Fault latch override input	Grounded for normal operation.
4	TM	Test mode input	Grounded for normal operation.
5, 17	GNDA	IC signal ground	Connect to module ground at board level.
6	VSET	Control voltage for adjusting the balancing current	This voltage is set by the user.
7	WDOR	Watchdog timer override	Grounded for normal operation.
8	EN	Input from EMB1428, signals charge or discharge cycle to begin.	Rising edge of this signal clears all fault latches, the DONE latch, and initiates charge or discharge current. Falling edge of this signal causes the charge current to ramp down to zero, then asserts the DONE signal, causing shutdown.
9	DIR	Input from EMB1428, determines the direction of the converter output current	"High" indicates charge mode, "Low" indicates discharge mode.
10	$\overline{\text{DIR_RT}}$	Output to EMB1428, inverted copy of the DIR signal	Used as a handshake signal to ensure DIR signal has been received correctly.
11	DONE	Output to EMB1428, indicates that the balancing current has ramped down towards zero.	When the EMB1499Q is disabled by toggling the EN pin low, the chip goes into a 'soft shutdown', ramping the charging current down within several hundred microseconds. When the current has ramped down, the EMB1499Q shuts down and the DONE signal latches high. The DONE latch is cleared at the next rising edge of the EN signal.
12,13,14	FAULT[0,1,2]	Outputs to EMB1428, three bit digital fault code	If a fault condition is detected, the proper three bit word is latched into the FAULT pins and the EMB1499Q is shut down. The FAULT pins are cleared by the rising edge of the EN input.
15	VSENSE_LS	Primary side current sense input	Connect to transformer side of primary sense resistor.
16	VINA	External 12V supply	Powers all internal circuitry besides the primary gate side driver. VINA and VINP should be connected together at the board level.
18	PWM_CLAMP	Output, PWM signal used to control primary side active clamp (external driver required)	
19	GATE_LS	Output, gate signal for external primary side power FET	
20	GNDP	IC power ground	Provides ground return for primary side gate driver. Connect to board level ground.
21	VINP	External 12V supply	Powers the primary side gate driver. VINP and VINA should be connected together at the board level.
22	PVINF	External floating 12V supply	This floating supply must be referenced to the bottom of the transformer secondary. Supplies power to the secondary side gate drivers. PVINF and VINF should be connected together at the board level.
23	GATE_HS1	Output, gate signal for external secondary side power FET	
24	PGNDF	Floating power ground	Connect to secondary side of converter. Provides the ground return for the secondary side gate drivers.
25	GATE_HS2	Output, gate signal for external secondary side power FET	
26	N/C	No connect	No connect pin. Do not connect
27	GNDF	Floating signal ground	Connected to secondary side of converter. Provides ground reference for all internal circuitry that floats with the transformer secondary except the secondary side gate drivers.
28	VINF	External floating 12V supply	This floating supply must be referenced to the bottom of the transformer secondary. Supplies power to all internal circuitry that floats with the transformer secondary except the secondary side gate drivers. PVINF and VINF should be connected together at the board level.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)

VINA, VINP to GND		-0.5V to 15V
VINF, PVINF to GNDF		-0.5V to 15V
GNDF to GND		-0.5V to 60V
VSENSE_LS to GND		-0.5V to 0.5V
VSENSE_HS to GNDF		-0.5V to 0.5V
VSET to GND		-0.5V to 7.5V
CELLPLUS to GNDF		-0.5V to 7.5V
All other inputs to GND		-0.5V to 15V
ESD Rating(2)	Human Body Model	±2kV
Soldering Information	Junction Temperature	150°C
	Storage Temperature	-65°C to 150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/ or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the recommended Operating Ratings is not implied. The recommended Operating Ratings indicate conditions at which the device is functional and should not be operated beyond such conditions.

(2) The human body model is a 100pF capacitor discharged through a 1.5 kΩ resistor into each pin. Test method is per JESD22–A114.

OPERATING RATINGS

VINA, VINP to GND	10V to 14V
VINF, PVINF to GNDF	10V to 14V
GNDF to GND	0V to 56V
VSENSE_LS to GND	-0.2V to 0.2V
VSENSE_HS to GNDF	-0.2V to 0.2V
VSET to GND	1V to 2.2V
CELLPLUS to GNDF	0V to 6V
All other inputs to GND	0V to 14V
Junction Temperature (T_J)	-40°C to 125°C

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ELECTRICAL CHARACTERISTICS

Limits in standard type are for TJ = 25°C only; limits in boldface type apply over the junction temperature (TJ) range of −40°C to +125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at TJ = 25°C, and are provided for reference purposes only. For all tests, VINA = VINP = VINF = PVINF = 12V unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Units
Feedback Voltage						
V_{SENSE_HS}	Feedback Voltage	VSET = 2V	45	50	55	mV
		VSET = 1.2V	24	30	36	mV
Switching Parameters						
F_{SW}	Switching Frequency		220	250	290	kHz
D_{MAX}	Maximum Duty Cycle	Charge Direction		91		%
		Discharge Direction		91		%
D_{MIN}	Minimum Duty Cycle	Charge Direction		4		%
		Discharge Direction		3		%
Operating Thresholds						
UVLO	Under-voltage Lockout	VINA, VINP, VINF, PVINF Rising			10.8	V
		VINA, VINP, VINF, PVINF Falling	5			V
V_{EN_TH}	Enable Threshold	EN Rising			1.55	V
		EN Falling	0.45			V
V_{DIR_TH}	Direction Threshold	DIR Rising			2.75	V
		DIR Falling	2.2			V
Quiescent Currents						
I_{Q_VINA}	VINA Quiescent Current (Operating)	VSET = 2V, VSENSE_HS = 0V		2	2.8	mA
	VINA Quiescent Current (Shutdown)	EN = 0V		<1	2.3	µA
I_{Q_VINP}	VINP Quiescent Current (Shutdown)	VEN = 0V		<1	2.3	µA
I_{Q_VINF}	VINF Quiescent Current (Operating)	VSET = 2V, VSENSE_HS = 0V		1.5	1.9	mA
	VINF Quiescent Current (Shutdown)	EN = 0V		<1	2	µA
I_{Q_PVINF}	VPINF Quiescent Current (Shutdown)	EN = 0V		<1	2.5	µA
$I_{Q_CELLPLUS}$	CELLPLUS Quiescent Current (Operating)	VSET = 2V, VSENSE_HS = 0V		18	30	µA
Fault Detection						
V_{CL_LS}	Primary Side Current Limit		100	132	170	mV
V_{CL_HS}	Secondary Side Current Limit		95	136	185	mV
V_{OVP}	Cell OVP Threshold Voltage	CELLPLUS Rising	4.5	5.5	7	V
		CELLPLUS Falling		5		V

(1) Typical specifications represent the most likely parametric norm at 25°C operation.

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ELECTRICAL CHARACTERISTICS (continued)

Limits in standard type are for TJ = 25°C only; limits in boldface type apply over the junction temperature (TJ) range of −40°C to +125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at TJ = 25°C, and are provided for reference purposes only. For all tests, VINA = VINP = VINF = PVINF = 12V unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Units
V_{UVP}	Cell UVP Threshold Voltage	CELLPLUS Rising		1.17		V
		CELLPLUS Falling	0.55	0.74	0.95	V
t_{WD}	Watchdog Timeout			8		s
T_{SD}	Thermal Shutdown			165		°C
Output Drivers						
$R_{ON_LS_HIGH}$	Primary Side Driver Pull-up Output Resistance	IGATE_LS = 100mA	3.6	5.5	8.4	Ω
$R_{ON_LS_LOW}$	Primary Side Driver Pull-down Output Resistance	IGATE_LS = 100mA	1.1	1.7	3.2	Ω
$R_{ON_HS1_HIGH}$	Secondary Side Driver (HS1) Pull-up Output Resistance	IGATE_LS = 100mA	7	11	16	Ω
$R_{ON_HS1_LOW}$	Secondary Side Driver (HS1) Pull-down Output Resistance	IGATE_LS = 100mA	1.1	1.7	3.2	Ω
$R_{ON_HS2_HIGH}$	Secondary Side Driver (HS2) Pull-up Output Resistance	IGATE_LS = 100mA	7	11	16	Ω
$R_{ON_HS2_LOW}$	Secondary Side Driver (HS2) Pull-down Output Resistance	IGATE_LS = 100mA	0.9	1.5	3	Ω

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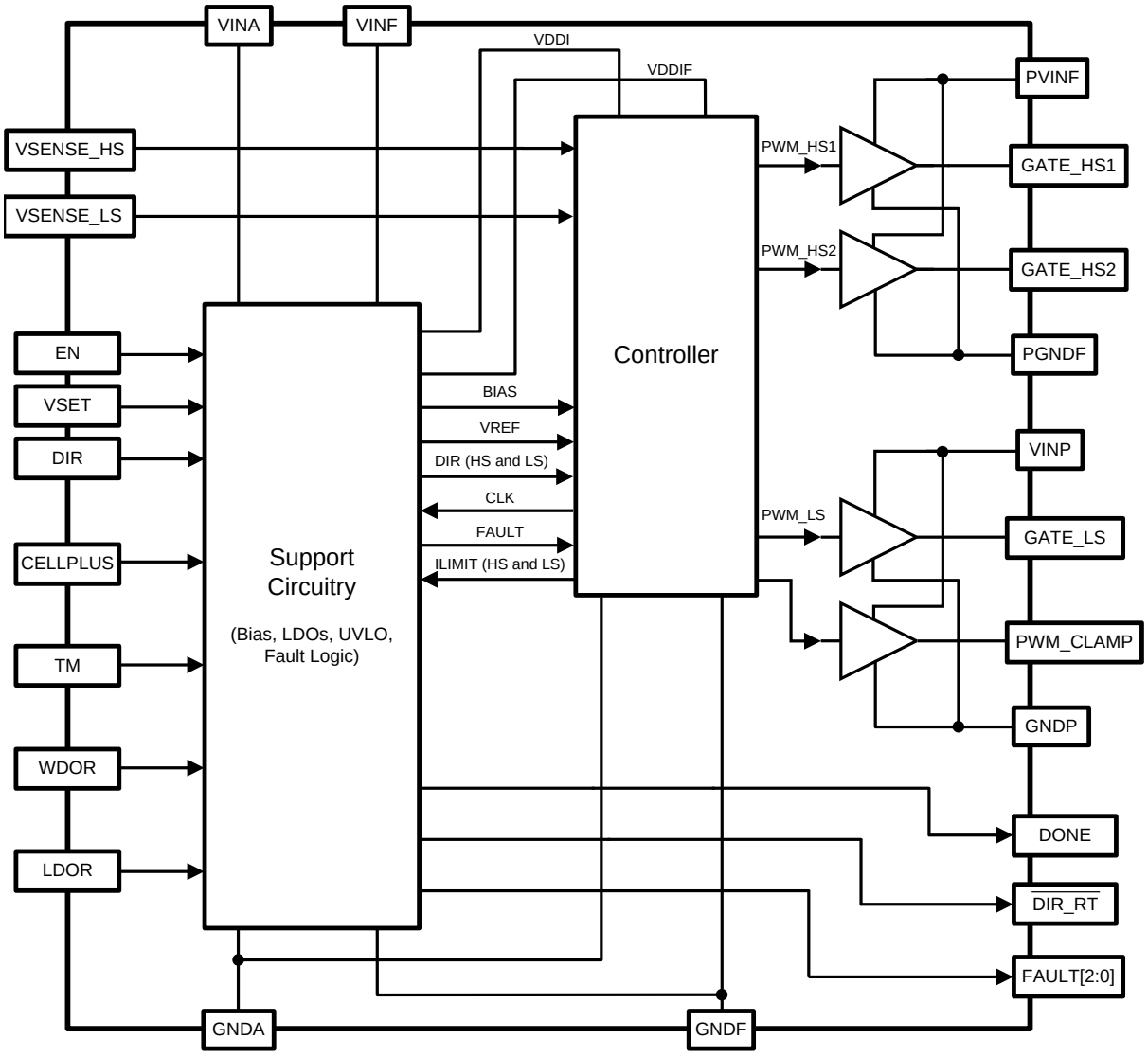


Figure 3. Top-level Block Diagram

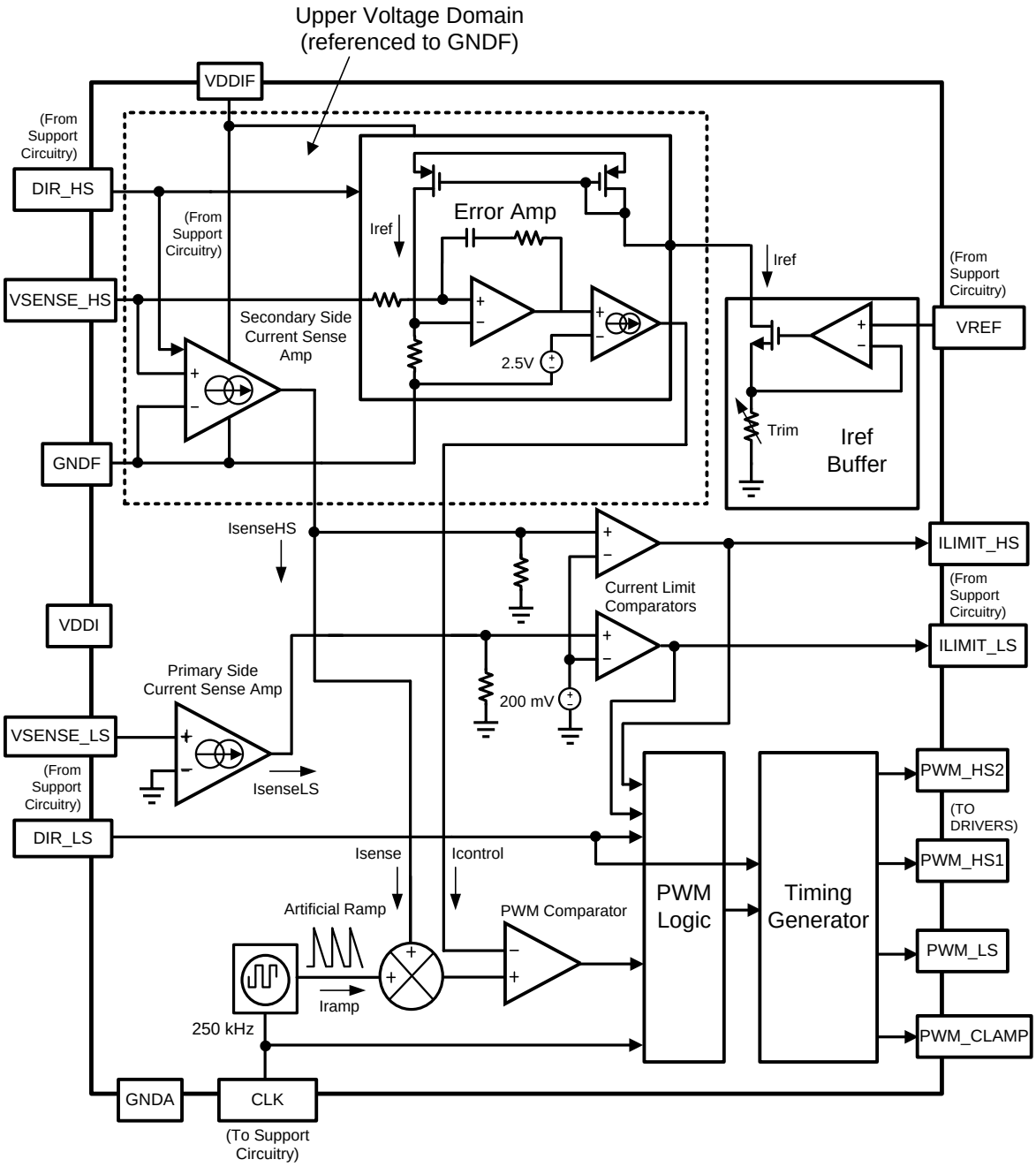


Figure 4. Controller Block Diagram

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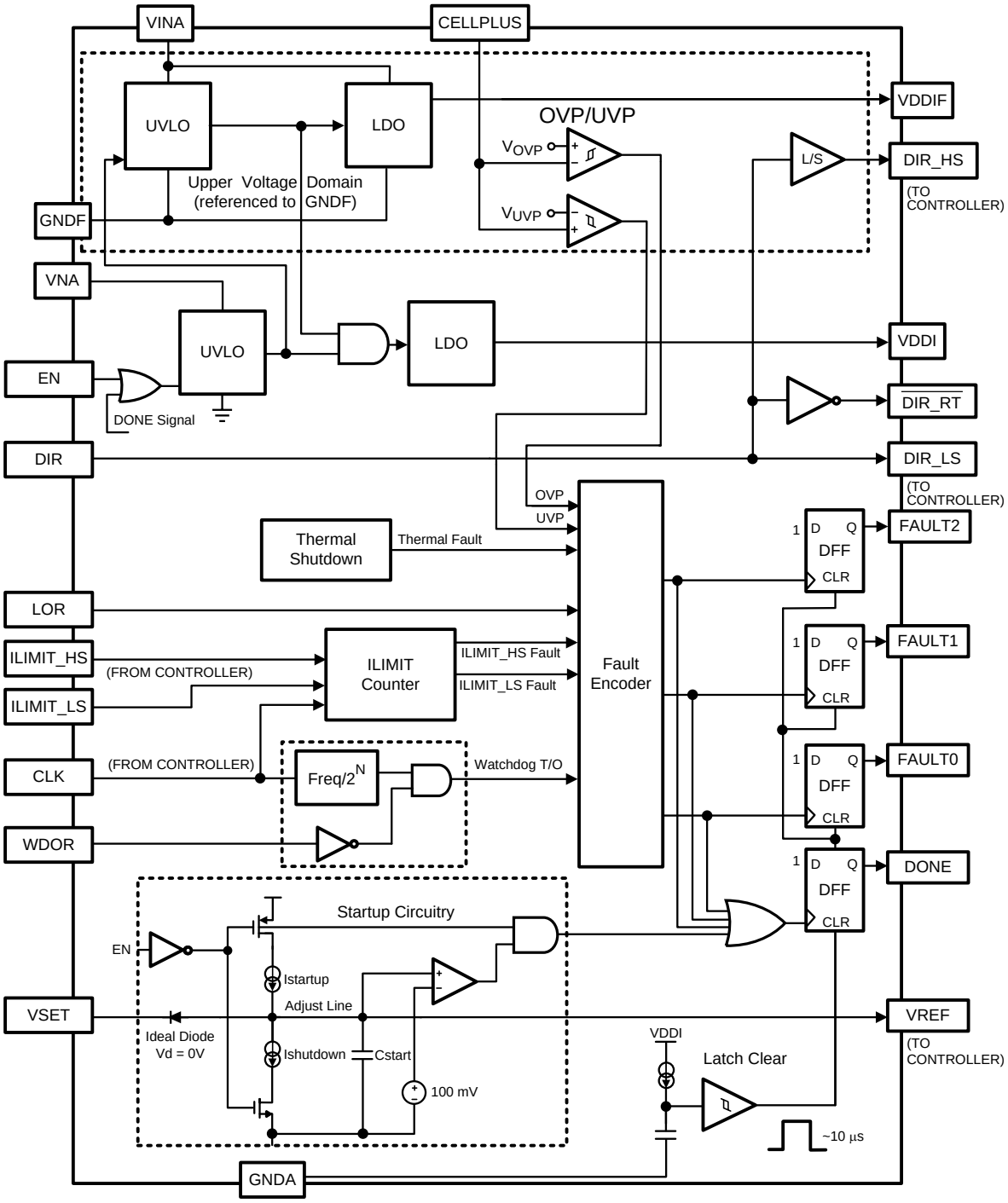


Figure 5. Support Circuitry Block Diagram

APPLICATION INFORMATION

The EMB1499Q and the EMB1428 work in conuction to control an active balancing circuit for up to 7 battery cells connected in series. See Typical Application (Figure 1) for the typical system architecture. The EMB1499Q is a PWM controller that regulates the inductor current in the bidirectional forward converter. The EMB1428 provides 12 floating gate drivers that are needed for the control of the FET switch matrix in the circuit. In a typical application, the forward converter has the inductor side (also called “secondary side”, “floating side” or “high side”) connected to the switch matrix and the other side (also called “primary side”, “non-floating side” or “low side”) to the battery stack. With such an arrangement, every cell balancing action is an energy exchange between a cell and the whole stack. The EMB1499Q can handle up to 56V between the top cell’s negative terminal and the bottom of the stack (bottom cell negative terminal).

Driving the EN pin high initiates the normal operating cycle. Once EN goes high, the EMB1499Q drives the DONE pin low. A normal operation cycle begins when the EMB1499Q DONE pin is driven low upon seeing the EN pin go high. The IC will then set the DIR_RT pin to the logic opposite of the DIR pin. This completes the initial handshaking with the EMB1428. The EMB1499Q will then start toggling the gate signals and the PWM_CLAMP signal and ramp the inductor current toward the target current magnitude set by the VSET pin, and in the polarity set by the DIR pin. After a few seconds (less than 8 sec.) of constant current operation, the EMB1499Q sees its EN pin de-asserted by the EMB1428 and it will immediately start to ramp down the inductor current toward zero. When the inductor current is typically 5% of steady state value, the EMB1499Q will pull the DONE pin high to the EMB1428 that the forward converter has shut off. This completes one normal operation cycle for the EMB1499Q.

During operation, the DONE pin will be driven high and the converter shutdown if the following abnormalities are detected during normal operation: over current, over voltage, under voltage, watchdog timeout, and thermal shutdown. The EMB1428 will then assert its FAULT_INT to inform the system controller of this EMB1499Q Error and read the fault code on the EMB1499Q FAULT pins.

To provide extra protection to the battery management system, the EMB1499Q has a built-in watchdog timer and will automatically shut down the forward converter after 8 seconds of continuous operation. To keep charging or discharging the same cell for more than 8 seconds, the microcontroller has to issue a stop and start command at least once every 8 seconds.

The EMB1499Q needs two separate 12V supplies (10V to 14V) to function. One of the 12V supplies is referenced to the stack ground and the other the floating ground.

Block Descriptions

This section contains descriptions of the individual circuit blocks in the EMB1499Q.

Voltage Domain Definitions

The EMB1499Q has been divided into two voltage domains. In this document the two domains are called the upper voltage domain and the lower voltage domain.

The upper voltage domain refers to all circuitry that is referenced to GNDF, which is the floating ground. The floating ground is connected to the bottom of the secondary side of the isolated converter. This is also the negative side of the current cell being charged. The circuitry in this domain is powered by VINF, which is an external floating supply. There is also an internal regulator powered from VINF that creates an internal floating 5V rail.

The lower voltage domain refers to all circuitry that is ground referenced. This domain is required to interface with all signals to and from the microcontroller and EMB1428, as these signals are ground referenced. Most of the circuitry in this domain is powered either directly from VINA or from an internal 5V rail powered by VINA. The primary side driver is powered from VINP.

All interfaces between the upper and lower voltage domains require level shift circuitry implemented internally within the EMB1499Q.

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FET Gate Drivers

The EMB1499Q includes one primary side gate driver and two secondary side gate drivers. A logic signal for the driver of a primary side active clamp FET is also available. Input PWM signal for each of the three gate drivers is level shifted from the internal digital supply rail (VDD) to the external power rail, either PVINF or VINP. Each driver output buffer contains shoot through protection. All drivers are forced into an off state if any power rail goes lower than the UVLO threshold.

Timing Generator

Depending on the desired direction of the balancing current (as dictated by the state of the DIR pin), the timing generator will adjust the relative timing of the gate signals and PWM_CLAMP signal.

Based on the state of the DIR pin, the internal logic of the EMB1499Q assigns one of the gate signals as the “control” signal and the others as the “synchronous” signals. The “control” signal is used to establish the required duty cycle and the “synchronous” signals are timed relative to the “control” signal with the proper dead times or overlap times. These two signal types are also treated differently by the internal logic for the purposes of startup, shutdown, and fault handling.

Figure 6 and Figure 7 show typical relative timings for the gate signals in both balancing directions. Also noted in each figure is the assignment of the “control” signal for the balancing current direction. Note that these diagrams are ideal, indicating negligible capacitive loading on the pins. In reality, these gate signals would have finite rise and fall times that are dictated by the C_G of the external MOSFET and the output resistance of the internal driver (consult the ELECTRICAL CHARACTERISTICS for the R_{ON} data).

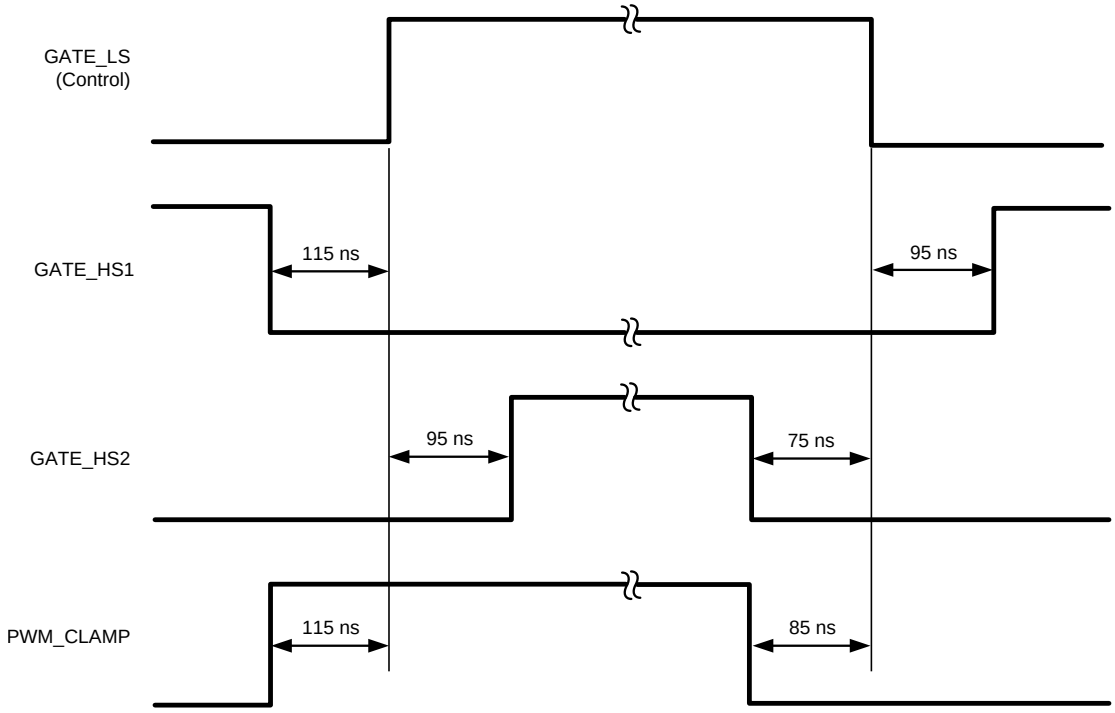


Figure 6. Charge Direction (DIR high)

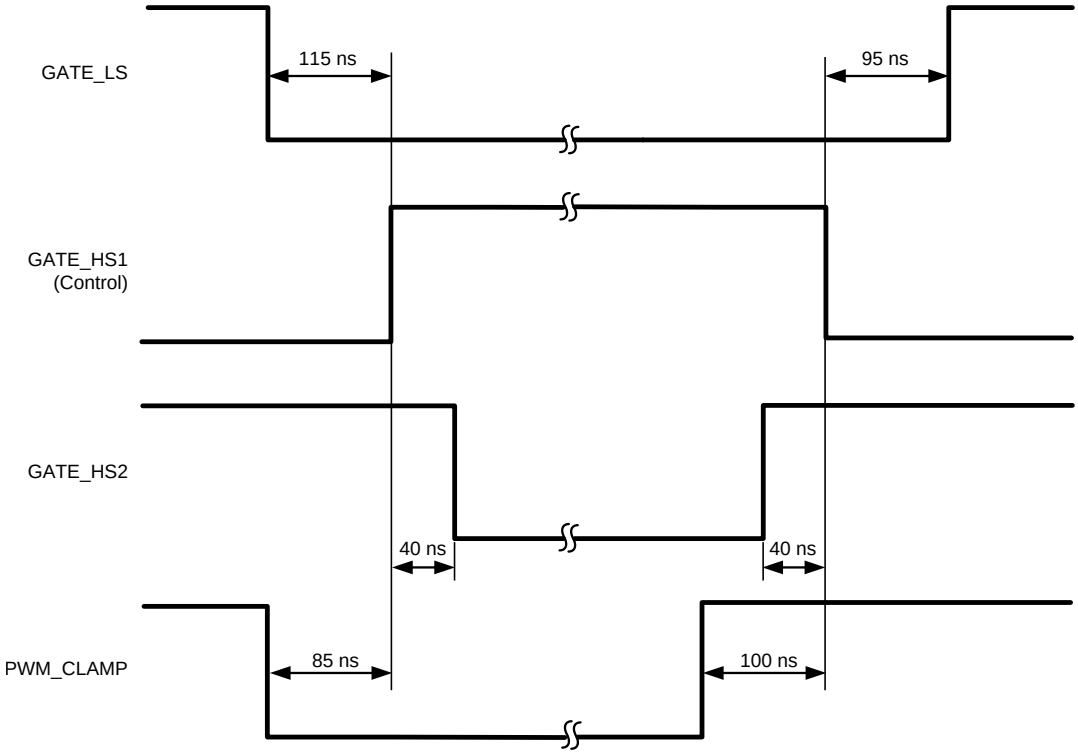


Figure 7. Discharge Direction (DIR low)

It should be noted here that for proper operation of the active clamp, an external delay network is required in series with the external active clamp driver that delays the turn-on transition of the active clamp transistor (falling edge of the PWM_CLAMP signal) by a specified amount. This is discussed in detail in the Application Hints.

PWM Controller Blocks

The DC voltage appearing at VREF (determined by applied to the VSET pin) sets the desired inductor current. As can be seen in the Controller Block Diagram (Figure 4), the VREF voltage is transformed into a GNDF referenced voltage through a current mirror (Iref, 25 µA) and that voltage is compared with the voltage across the secondary side sense resistor. The difference between the two signals is fed to the error amplifier as the error signal. The amplified and filtered/ compensated error signal becomes the current command signal and is compared at the PWM comparator with sensed inductor current. The feedback loop forces the error toward zero which means the inductor current will be regulated at the desired level set by VREF. The current sense amplifier that senses the inductor current switches polarity when there is a change in the DIR logic level, so as to achieve the bidirectional operation. There is also an internal soft start voltage ramp that forces a gradual turn-on and turn-off of the inductor current. The final reference appearing at the error amplifier is determined by the lower of the said soft start voltage ramp and the voltage at VREF.

Current Limit Comparators

As shown in the Controller Block Diagram (Figure 4), both primary and secondary side currents of the forward converter are internally turned into current sources by the current sense amplifiers. The current sources flow into two resistors whose voltages are then compared with a 200mV reference by two current limit comparators. The trigger point for both primary and secondary currents is typically 134mV across each sense resistor.

PWM Comparator

The EMB1499Q employs a Peak Current Mode control method. Basically the amplified inductor current (IsenseHS) is compared to the current command (Icontrol) at the PWM comparator, generating the PWM signal for gate drivers. To prevent a potential half-switching frequency (sub-harmonic) oscillation issue associated with peak current control, an artificial ramp is added on top of the sensed inductor current before the latter is compared with the current command.

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Startup Circuitry

The startup circuitry (Figure 5) performs three functions. The ramp generator charges an internal Cstart capacitor during startup, generating a gradually increasing voltage ramp until the voltage reaches VSET value and is clamped by it. This voltage ramp is used by the controller block to generate the ramp in the current reference and bring up the inductor current in a soft start manner. The ramp generator also discharges the internal Cstart capacitor during shutdown. The down slope in the VREF voltage as a result of the discharge will cause the inductor current to ramp down gradually. Besides the ramp generator, there is also a comparator that will toggle if the Cstart voltage dips below 100mV. This is to flag that the shutdown is considered complete. The startup circuitry also generates a starthold pulse, which is a 10 µs long pulse that is activated upon the assertion of the EN pin. While this pulse is active, the DONE and FAULT pins are held in the clear state, and the part is not allowed to switch.

UVLO Blocks

The EMB1499Q has two under-voltage lockout (UVLO) blocks each monitoring one external 12V supply. Block UVLO_LS monitors VINA with respect to GNDA and block UVLO_HS monitors VINF with respect to GNDF. UVLO_HS will not be activated until UVLO_LS shows that VINA has crossed the UVLO rirsing threshold voltage. UVLO_LS is activated if either EN is high or DONE is low. When UVLO_LS has a positive output, bias current is sent to the UVLO_HS to activate it. Once both UVLOs have positive outputs, the internal chip enable signals are activated, internal rails are powered up and gate drivers are unlocked.

Enable/Shutdown Sequencing

Shutdown Behavior

The standard shutdown sequence can be described as follows:

1. Initial State: DONE low, EN high, part operating in steady state.
2. The EMB1428 drops EN signal low.
3. Inductor current ramps down (typically 300 µs).
4. When inductor current has ramped sufficiently low, the EMB1499Q shuts down and DONE signal is asserted high to tell the EMB1499Q that the shutdown process has finished, and can accept new commands.
5. DONE signal remains latched high, and is not cleared until the next enable sequence.

Enable Behavior

The standard enable sequence can be described as follows:

1. Initial State: DONE high, EN low, external supplies above UVLO voltage (from previous shutdown sequence).
2. The EMB1428 asserts EN high.
3. EN activates the UVLO blocks, which then allow the internal rails to power up.
4. Internal “starthold” pulse remains high for first 10us, clears DONE latch and all fault latches.
5. When “starthold” drops low, part is allowed to start up normally, and all output latches are now free to be clocked.

Fault Detection and Fault Codes

The fault detection circuitry of the EMB1499Q consists of a three-bit encoder which has as its input six different fault modes. Its output is a digital word which is passed to the system microcontroller through the EMB1428. The fault codes (FAULT[2:0])that are passed can be read as follows:

000 = No Fault 001 = Primary Side Current Limit

010 = Secondary Side Current Limit

011 = Thermal Shutdown

100 = Watchdog Timeout

101 = UVP Fault

110 = OVP Fault The fault detection process can be described as follows:

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1. Fault signals passed into the three-bit encoder
2. Internal fault signal passed to PWM logic and all gates are forced off and latched
3. Internal fault signal passed to the soft start comparator and asserts start-low, and therefore latches DONE output high
4. Three-bit fault word is level shifted to the external supply, and external fault code is latched into output buffer for FAULT 0..2 pins.
5. The EMB1428 reads the fault code on the FAULT 0..2 pins and drops EN voltage, shutting the EMB1499Q down
6. Fault code and DONE signal remain latched until next startup cycle

Secondary OVP/UVP

This block senses the voltage of the cell being charged/discharged. If this voltage is outside a predefined range, a fault is detected and the IC is disabled.

Current Limit Counter

The current limit counter monitors both the primary and secondary side current limit signals. The counter is reset every 32 clock pulses. If a specified number of current limit events are detected (4 for primary side and 8 for secondary side) within this 32 clock pulse window, a fault is flagged and the part is disabled.

Watchdog Timer

The purpose of this block is to create a maximum running time of 8 seconds for the chip. This timer is created by using a string of flip-flops to count clock pulses. After 221 clock pulses (typically 8 seconds at 250kHz switching frequency), if EN is still high, a fault is flagged and the IC is shut down.

Thermal Shutdown

This block senses the internal temperature of the die and flag output if that temperature exceeds a predetermined threshold, TSD. If this fault flag is activated, the IC will shut down and charging operation will cease.

Application Hints

Setting the Balancing Current (VSET and Secondary Sense Resistor)

If the secondary side of the forward converter is connected to battery cells via a switch matrix, the cell balancing current is equal to the steady state value of the main inductor current. Two external parameters determine the balancing current (Ibalancing): the voltage at the VSET pin and the secondary side sense resistance (RSENSE2). The voltage at the VSET pin controls the reference voltage at the error amplifier, and therefore the voltage at the VSENSE_HS pin. The equation for selecting the secondary side sense resistance is:

$$R_{SENSE2} = \frac{V_{SENSEHS}}{I_{balancing}}$$

The equation for selecting the secondary side sense resistance is:

$$V_{SENSE_HS} = \frac{V_{SET}}{40}$$

Supported values for VSET range from 1V to 2.2V. However, the EMB1499Q is factory trimmed at VSET = 2V. Therefore, it is recommended to use VSET = 2V for highest balancing current accuracy. See ELECTRICAL CHARACTERISTICS for specified tolerances on VSENSE_HS when for VSET = 2V and 1.2V. Due to switching noise present at the secondary side current sense resistor, it is possible that current values are slightly different for different directions of balancing, even if VSET is constant. In such a case, it is recommended that a calibration be conducted at the system level so that a slightly different VSET is programmed when changing the direction of balancing.

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Primary Sense Resistor Selection

The primary sense resistor should be chosen in conjunction with the secondary sense resistor so that the ratio between the two resistors is approximately equal to the transformer turns ratio. For example if the secondary sense resistor is 10mΩ, and the transformer turns ratio is 3.5:1 (recommended for a 14 cell application – see the Transformer Selection section), the primary sense resistor should be chosen to be approximately 35mΩ.

Inductor Selection

The value of the inductor, along with the converter input/output voltages, determines the AC ripple of the inductor current. A good practice is to choose an inductance value so that the peak-to-peak ripple falls somewhere between 20% and 40% of the steady state balancing current during typical operation. If the transformer turns ratio is selected properly (see the Transformer Selection section), and assuming a typical 250kHz switching frequency, then the equation relating inductance to current ripple for the EMB1499Q can be reduced to:

$$L = 3 \times 10^{-6}\text{sec-1} \times V_{CELL} \times \Delta i_L$$

where V_{CELL} is the typical cell voltage in the given application, and Δi_L is the peak-to-peak current ripple value. The EMB1499Q utilizes peak current mode control, which means that the inductor current is sampled in real time and used for loop control. In this type of control method, the slope of the sensed inductor current ripple is an important parameter. This sensed slope is inversely proportional to the inductor value, and directly proportional to the gain of the current sense path. In other words:

$$\frac{dI_{SENSE}}{dt} \alpha \frac{R_{SENSE2}A_i}{L}$$

Where I_{SENSE} is the sensed inductor current, R_{SENSE2} is the secondary side sense resistor value, and A_i is the gain of the internal current sense amplifier.

In order to ensure stability of the internal current sense loop, it is recommended that the slope of the sensed inductor current remain somewhat constant if external component values are changed. From the above equation, this means that if the value of the secondary sense resistor is increased (possibly to achieve lower balancing current), then the value of the output inductor should be increased with approximately the same scale.

In addition, it is important to choose an inductor that can support the peak output current without saturating. Inductor saturation will cause a sudden reduction in the inductance value, and cause the converter to operate incorrectly. It is also recommended to choose an inductor with minimal DC winding resistance in order to minimize conduction losses and maximize efficiency.

Transformer Selection

The EMB1499Q is designed to work optimally with a transformer turns ratio of 3.5:1 when operating within a stack of 14 cells. In order to maintain proper peak currents and voltage stresses on the drains of the power MOSFETs, it is recommended that this relationship between turns ratio and number of cells be maintained. In other words, follow the following equation when choosing a turns ratio for the transformer:

$$n = 0.25 \times \text{NumCells}$$

In the typical application, the forward transformer for the EMB1499Q has a minimum primary side inductance of 190µH. To ensure proper operation, it is recommended to use this as the minimum inductance specification for a 14 cell solution. It is reasonable to scale this inductance with the number of cells in the stack. For example, for a 7 cell stack a minimum primary inductance of 95µH can be used. It is also recommended that the leakage inductance of the transformer be less than or equal to 1% of the winding inductance.

In a typical 5A design, the primary side DC winding resistance should be less than typical 60mΩ, and the secondary side resistance typical 12mΩ. In order to ensure reasonable efficiency and to ensure properly gauged wires are used in the transformer, it is recommended to follow this specification. It is reasonable to scale these resistance specifications for constant DC power dissipation with different balancing currents.

Power MOSFET Selection

For optimal balance transfer efficiency, the power MOSFETs should be selected to provide the lowest possible conduction and switching power losses. For the purpose of MOSFET selection, a good criterion to use is the tradeoff between switch on resistance (R_{DSON}) and gate charge (Q_G). These parameters can be used to estimate the total conduction and gate charge losses for each MOSFET, which should be minimized:

$$P_{LOSS} = I_{RMS}2 \times R_{DSON} + Q_G \times F_{SW}$$

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Where F_{SW} is the switching frequency of the EMB1499Q (typically 250kHz), and I_{DS} is the RMS drain current in each MOSFET during steady state. The following equations can be used to provide a first order estimation of the RMS drain current in each MOSFET: Primary switching NMOS:

$$I_{RMS} \approx \frac{I_{balancing}}{2 \times NumCells}$$

Secondary switching NMOS:

$$I_{RMS} \approx \frac{I_{balancing}}{\sqrt{2}}$$

Active Clamp PMOS:

$$I_{RMS} \cong 25ms \times V_{CELL_MAX}$$

Where V_{CELL_MAX} is the maximum operating voltage of any cell in the stack.

In addition to power dissipation concerns, and assuming that the transformer turns ratio has been chosen correctly (see the Transformer Selection section), the power MOSFETs have the following additional requirements:

- All power MOSFETS must have absolute max rating for V_{GS} of at least 20V
- Primary MOSFETS (switching and active clamp) must have drain-source voltage rating of at least 2.5 times the maximum operating stack voltage.
- Secondary MOSFETs must have a drain-source voltage rating of at least 30V, gate resistance no more than 3Ω, and be avalanche robust (i.e., have an Avalanche Energy rating (E_{AR}) specified in the datasheet).

Input Capacitor Selection

Ceramic capacitors are required for proper operation due to their low ESR (equivalent series resistance). The voltage rating of the capacitor should exceed the maximum stack voltage in an application with proper de-rating. For example, in a 14 cell Li-ion application, the maximum stack voltage would be approximately 60V. Therefore, a 100V rated capacitor would be recommended. It is advisable to use at least 6.6µF of capacitance. Optimum performance will be achieved by using multiple smaller value capacitors in parallel to minimize series resistance and inductance.

For proper performance, X5R or X7R ceramics are recommended.

Output Capacitor Selection

As with the input capacitors, ceramic capacitors are required (X5R or X7R recommended). Since the maximum operating cell voltage of a Li-ion cell is 4.2V, a voltage rating of 6.3V or higher is recommended.

It is required to use at least 10µF of capacitance. Optimum performance will be achieved by using multiple smaller value capacitors in parallel to minimize series resistance and inductance.

Clamp Capacitor Selection

As with the input and output capacitors, a ceramic capacitor is also required for the clamp capacitor. Assuming that the transformer turns ratio has been chosen correctly (see the Transformer Selection section), the voltage rating of the capacitor should be at least 2.5 times the maximum operating voltage of the battery stack.

For example, in a 14 cell solution with a maximum operating cell voltage of 4.2V, the maximum operating voltage of the stack is 58.8V. Therefore, the voltage rating of the capacitor should be at least 2.5 * 58.8V = 147V. So for a 14 cell solution, a voltage rating of 200V (the next closest common voltage rating) is recommended. The recommended capacitance value for the clamp capacitor is 0.1µF.

Active Clamp Driver

The active clamp driver path consists of a delay circuit, gate driver, and a passive level shifting network. See Figure 8 below for the recommended circuit.

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The delay network should provide approximately 300ns to 400ns delay to the turn-on transition of the clamp PFET, and minimal delay to the turn-off transition. The recommended driver for this application is the EMB1412 from Texas Instruments. It is important to configure the driver in an inverting configuration. A passive level-shifting network is required in order to provide a negative gate voltage for the clamp PFET. It consists of a 0.1µF AC coupling capacitor, a clamping diode, and a 1kΩ resistor to provide a DC path to ground for the gate of the clamp PFET.

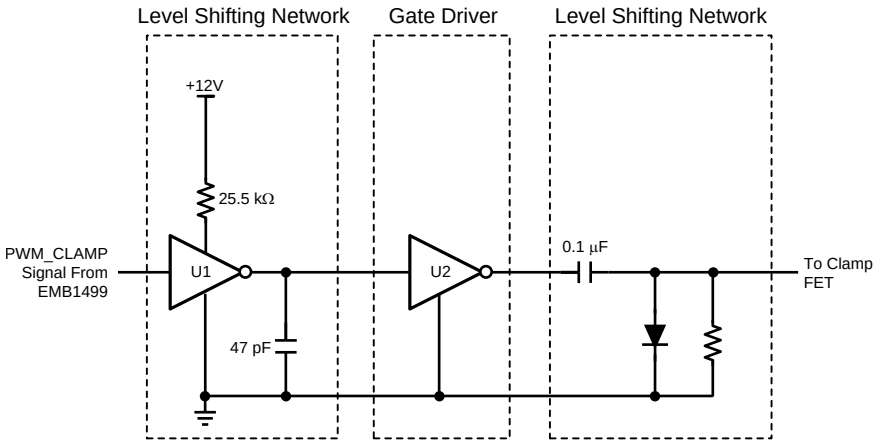


Figure 8. Active Clamp Driver Circuit

Continuous Balancing Operation

If it is desired to continually balance a particular cell for longer than the internal watchdog timeout of the EMB1499Q (typically 8 seconds), the EN pin of the EMB1499Q needs to be toggled within a period less than 8 seconds.

At the system level, this can be done by sending a “stop balancing” command to the EMB1428 gate driver chip, followed by “start balancing” command prior to the EMB1499Q timeout. Simply sending a new “start balancing” command without first sending the “stop balancing” command will not cause the EN pin of the EMB1499Q to toggle. If the EN pin does not toggle, the balancing will time out.

PCB Layout Recommendations

Besides following general switching power supply layout practices, below are recommendations for the EMB1499Q:

1. Run the gate traces in parallel with their associated ground planes for as much of the total runs as possible
2. Keep current sensing traces away from high dv/dt nodes such as the drains of power FETs
3. Place adequate copper underneath power FETs to help with thermal dissipation
4. Place numerous 8-mil vias in the PCB pad beneath the EMB1499Q and connect them to the corresponding ground plane(s) on all layers to help with thermal dissipation
5. Place the EMB1499Q within a couple inches of the power FETs to reduce board parasitics.

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REVISION HISTORY

Changes from Revision A (May 213) to Revision B	Page
• Changed package drawing from PW to PWP, and package type from TSSOP to HTSSOP	2

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
EMB1499QMH/NOPB	Active	Production	HTSSOP (PWP) | 28	48 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	EMB1499 QMH
EMB1499QMH/NOPB.A	Active	Production	HTSSOP (PWP) | 28	48 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	EMB1499 QMH
EMB1499QMHE/NOPB	Active	Production	HTSSOP (PWP) | 28	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	EMB1499 QMH
EMB1499QMHE/NOPB.A	Active	Production	HTSSOP (PWP) | 28	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	EMB1499 QMH
EMB1499QMHX/NOPB	Active	Production	HTSSOP (PWP) | 28	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	EMB1499 QMH
EMB1499QMHX/NOPB.A	Active	Production	HTSSOP (PWP) | 28	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	EMB1499 QMH

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

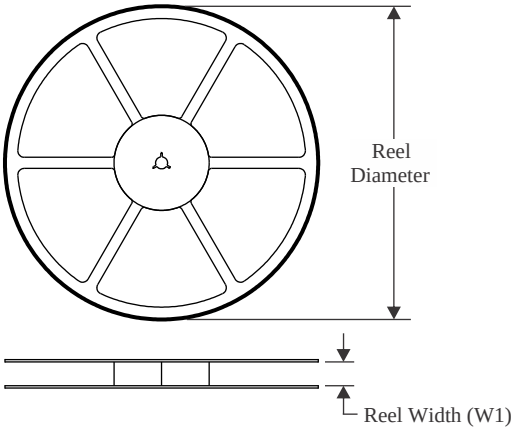
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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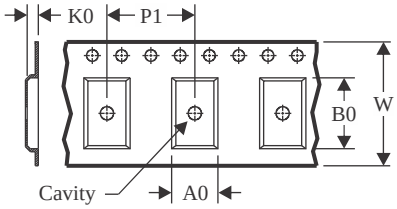
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

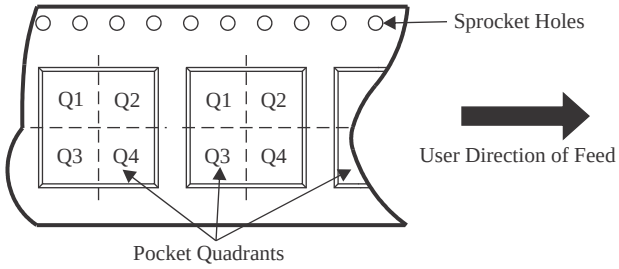


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

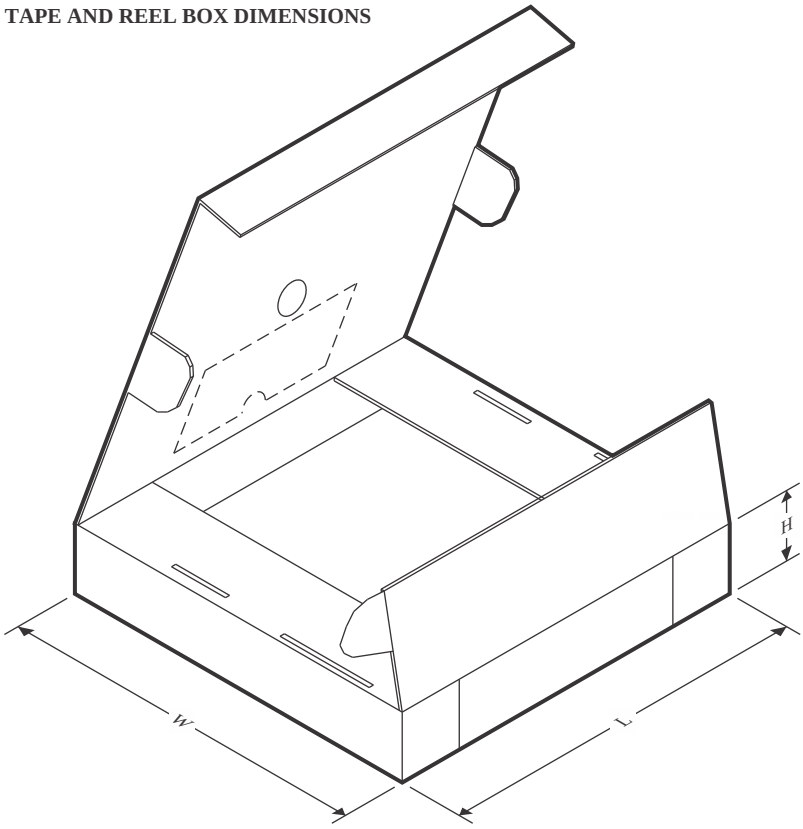
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
EMB1499QMHE/NOPB	HTSSOP	PWP	28	250	178.0	16.4	6.95	10.0	1.7	8.0	16.0	Q1
EMB1499QMHX/NOPB	HTSSOP	PWP	28	2500	330.0	16.4	6.95	10.0	1.7	8.0	16.0	Q1

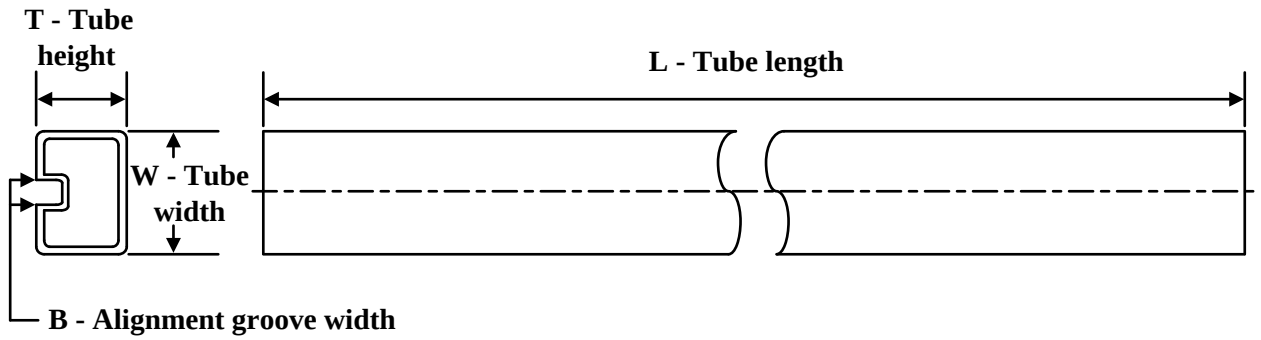
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
EMB1499QMHE/NOPB	HTSSOP	PWP	28	250	210.0	185.0	35.0
EMB1499QMHX/NOPB	HTSSOP	PWP	28	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
EMB1499QMH/NOPB	PWP	HTSSOP	28	48	495	8	2514.6	4.06
EMB1499QMH/NOPB.A	PWP	HTSSOP	28	48	495	8	2514.6	4.06

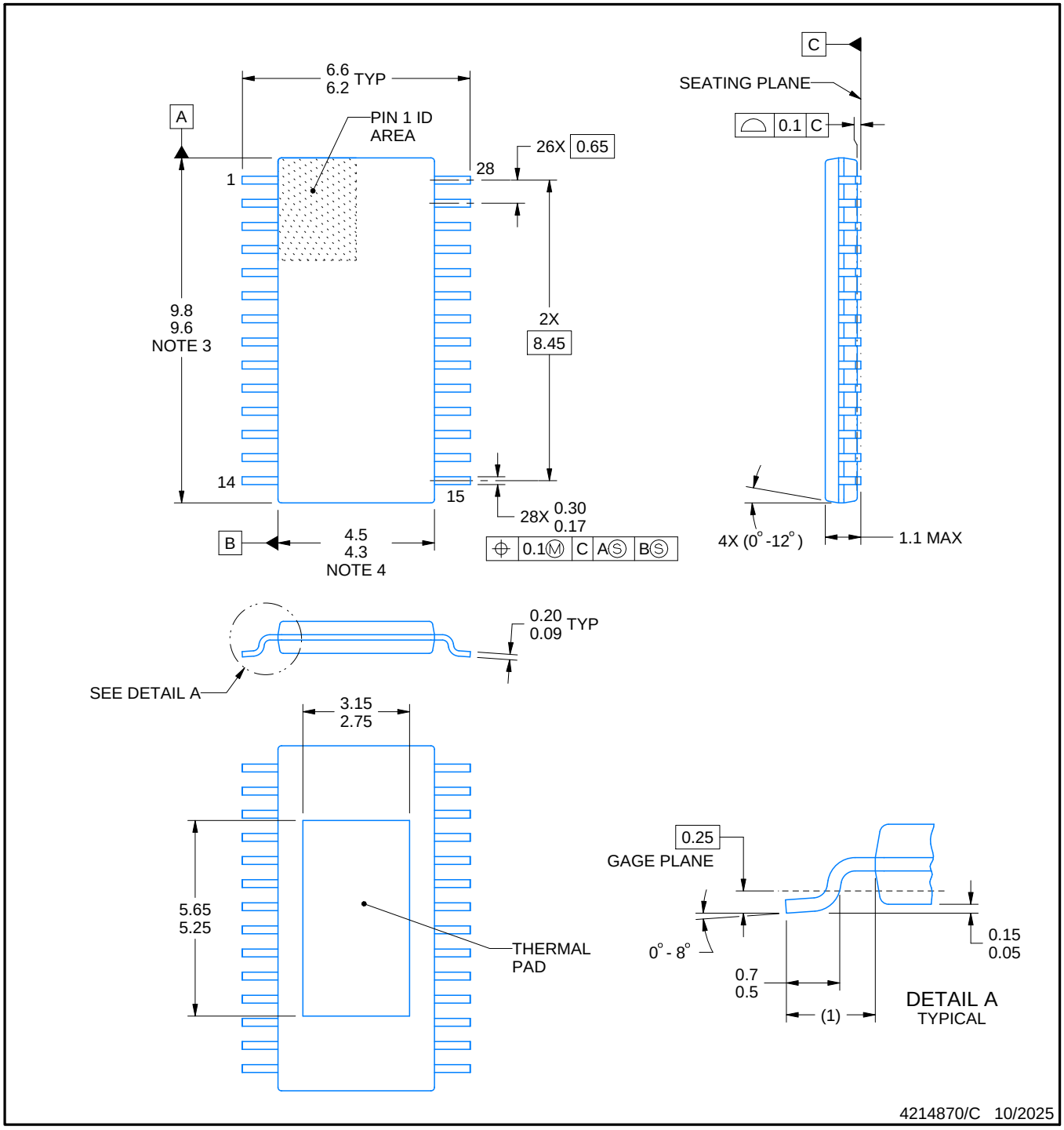


PACKAGE OUTLINE

PWP0028A

PowerPAD™ - 1.1 mm max height

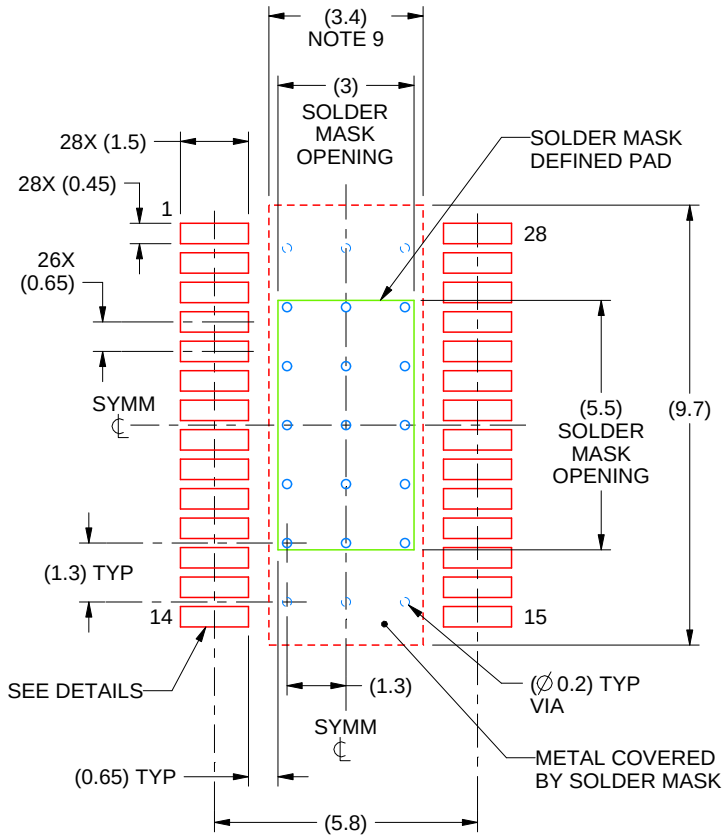
PLASTIC SMALL OUTLINE



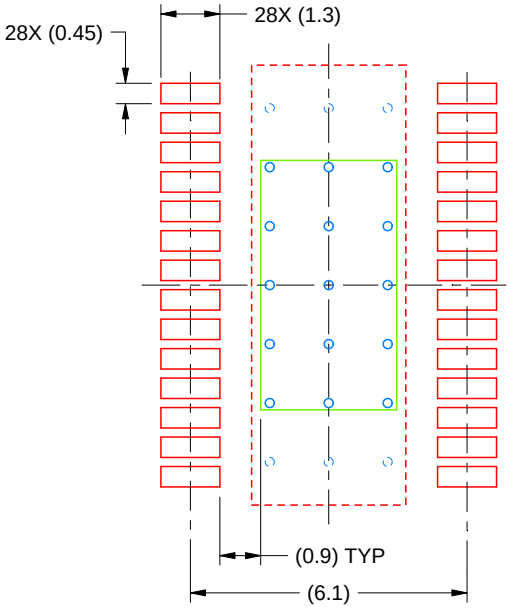
NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MO-153, variation AET.

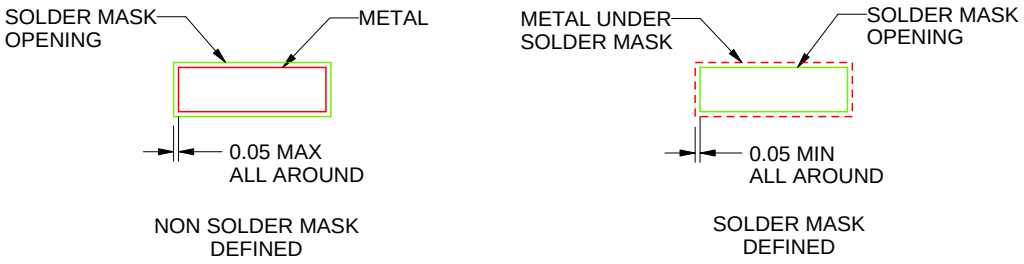


IPC-7351 NOMINAL
0.65 CLEARANCE CREEPAGE



HV / ISOLATION OPTION
0.9 CLEARANCE CREEPAGE
OTHER DIMENSIONS IDENTICAL TO IPC-7351

LAND PATTERN EXAMPLE
SCALE:6X

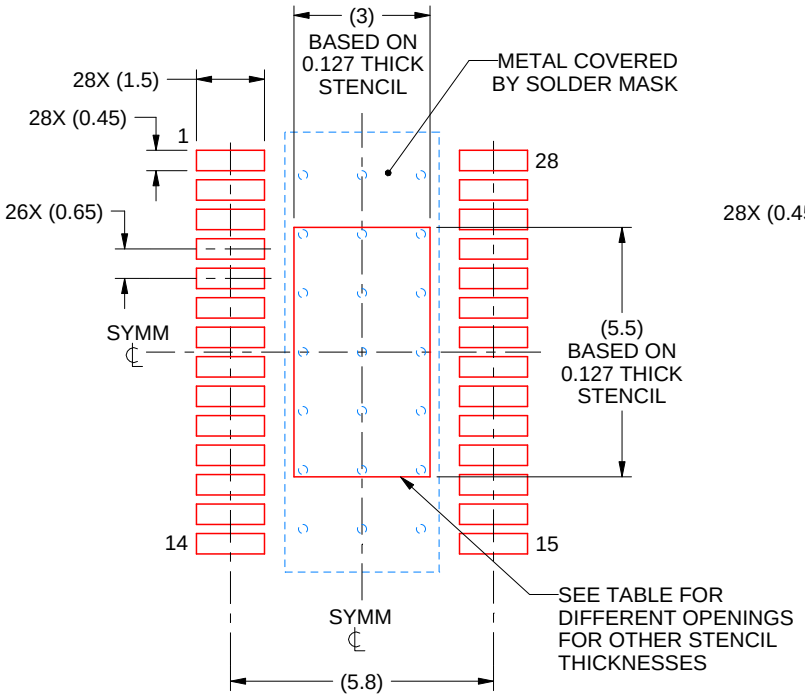


SOLDER MASK DETAILS

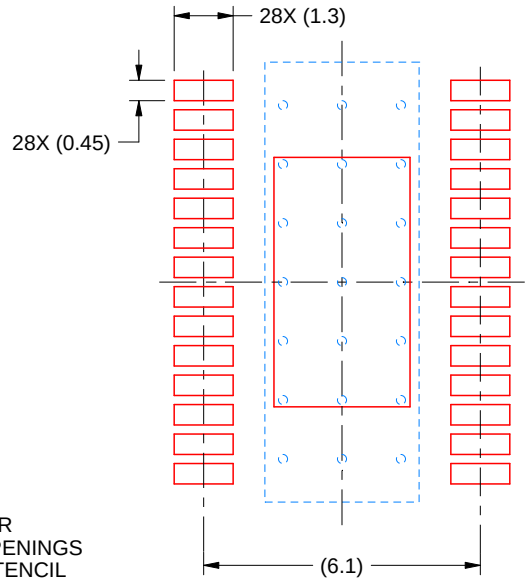
4214870/C 10/2025

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



IPC-7351 NOMINAL
0.65 CLEARANCE CREEPAGE



HV / ISOLATION OPTION
0.9 CLEARANCE CREEPAGE
OTHER DIMENSIONS IDENTICAL TO IPC-7351

SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.55 X 6.37
0.127	3.0 X 5.5 (SHOWN)
0.152	2.88 X 5.16
0.178	2.66 X 4.77

4214870/C 10/2025

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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