ESD351 1-Channel 30 kV ESD Protection Diode with Low Clamping Voltage in 0402 Package

1 Features

- IEC 61000-4-2 Level 4 ESD Protection
  - ±30-kV Contact Discharge
  - ±30-kV Air Gap Discharge
- IEC 61000-4-4 EFT Protection
  - 80 A (5/50 ns)
- IEC 61000-4-5 Surge Protection
  - 6 A (8/20 µs)
- IO Capacitance: 1.8 pF (Typical)
- DC Breakdown Voltage: 4.5 V (Minimum)
- Low Leakage Current: 0.1 nA (Typical)
- Extremely Low ESD Clamping Voltage
  - 6.5 V at 16-A TLP (I/O Pin to GND)
  - R_{DYN}: 0.1 Ω (I/O Pin to GND)
- Industrial Temperature Range: –40°C to +125°C
- Industry Standard 0402 Package (DFN1006P2)

2 Applications

- End Equipment
  - Wearables
  - Industrial and Service Robots
  - Laptops and Desktops
  - Mobile and Tablets
  - Set-Top Boxes
  - DVR and NVR
  - TV and Monitors
  - EPOS (Electronic Point of Sale)
- Interfaces
  - USB 2.0/1.1
  - GPIO
  - Pushbuttons
  - Audio

3 Description

The ESD351 is a uni-directional TVS ESD protection diode featuring low dynamic resistance R_{DYN} and low clamping voltage. The ESD351 is rated to dissipate ESD strikes up to 30 kV (Contact and Air) level per the IEC 61000-4-2 standard. The ultra-low dynamic resistance (0.1 Ω) and extremely low clamping voltage (6.5 V at 16-A TLP) ensure system level protection against transient events. This device has a capacitance of 1.8 pF (typical) making it ideal for protecting interfaces such as USB 2.0.

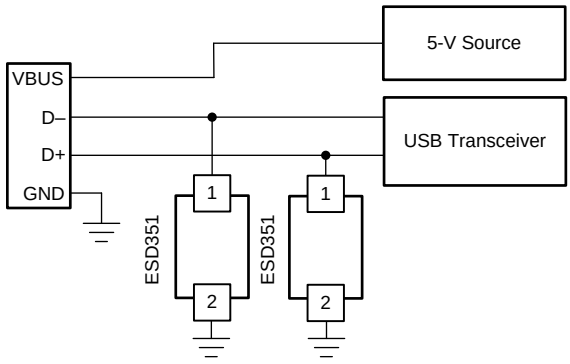
The ESD351 is offered in the industry standard 0402 (DPY/DFN1006P2) package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ESD351	X1SON (2)	0.60 mm × 1.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical USB 2.0 Application Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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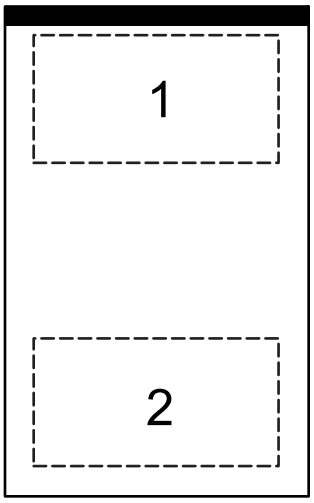
4 Revision History

DATE	REVISION	NOTES
July 2018	*	Initial release.

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5 Pin Configuration and Functions

DPY Package
2-Pin X1SON
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IO	I/O	ESD Protected Channel. Connect this pin to the line being protected.
2	GND	GND	Connect this pin to Ground

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Electrical Fast Transient	IEC 61000-4-4 Peak Current at 25 °C		80	A
Surge Pulse	IEC 61000-4-5 Surge (tp 8/20 µs) Peak Power at 25 °C		36	W
	IEC 61000-4-5 Surge (tp 8/20 µs) Peak Current at 25 °C		6	A
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings -JEDEC Specifications

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, allpins(1)	±2500	V
		Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings - IEC Specifications

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±30000	V
		IEC 61000-4-2 Air Discharge, all pins	±30000	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	0		3.6	V
T_A	Operating Free Air Temperature	–40		125	°C

6.5 Thermal Information

THERMAL METRIC(1)		ESD351 DPY (X1SON) 2 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	409.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	216.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	140.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	81.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	140.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.6 Electrical Characteristics

At TA = 25°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} < 50 nA, across operating temperature range			3.6	V
$I_{LEAKAGE}$	Leakage current at 3.6 V	V_{IO} = 3.6 V, I/O to GND		0.1	10	nA
V_{BRF}	Breakdown voltage, I/O to GND (1)	I_{IO} = 1 mA	4.5		7.5	V
V_{FWD}	Forward Voltage, GND to I/O (1)	I_{IO} = 1 mA		0.8		V
V_{HOLD}	Holding voltage, I/O to GND (2)	I_{IO} = 1 mA		5.1		V
V_{CLAMP}	Clamping voltage	I_{PP} = 6 A (8/20 µs Surge), I/O to GND		6.1		V
		I_{PP} = 16 A (100 ns TLP), I/O to GND		6.5		V
		I_{PP} = 16 A (100 ns TLP), GND to I/O		2.5		V
R_{DYN}	Dynamic resistance	I/O to GND, 100 ns TLP, between 10 to 20 A I_{PP}		0.1		Ω
		GND to I/O , 100 ns TLP, between 10 to 20 A I_{PP}		0.08		Ω
C_{LINE}	Line capacitance, IO to GND	V_{IO} = 0 V, V_{p-p} = 30 mV, f = 1 MHz		1.8	2.2	pF

(1) V_{BRF} and V_{BRR} are defined as the voltage obtained at 1 mA when sweeping the voltage up, before the device latches into the snapback state

(2) V_{HOLD} is defined as the voltage when 1 mA is applied, after the device has successfully latched into the snapback state.

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6.7 Typical Characteristics



Figure 1. TLP I-V Curve, I/O Pin to GND (t_p = 100 ns)

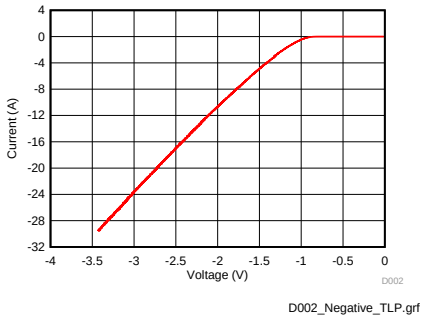


Figure 2. TLP I/V Curve, GND to I/O Pin (t_p = 100 ns)

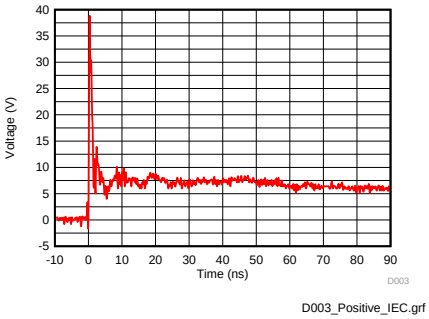


Figure 3. 8-kV IEC 61000-4-2 Clamping Voltage, I/O pin to GND

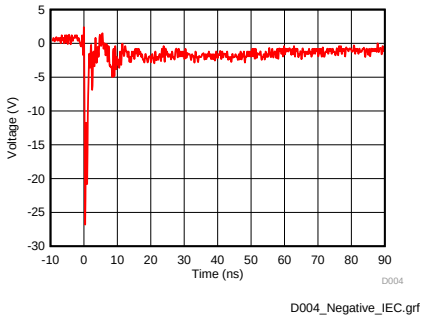


Figure 4. 8-kV IEC 61000-4-2 Clamping Voltage, GND to I/O Pin

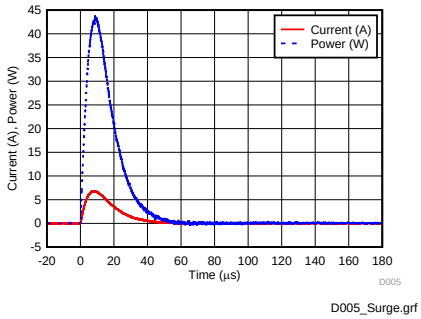


Figure 5. Surge Curve (IEC 61000-4-5, t_p = 8/20 µs), I/O Pin to GND

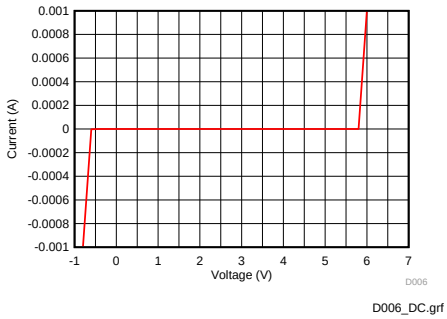


Figure 6. DC IV-Curve, I/O Pin to GND

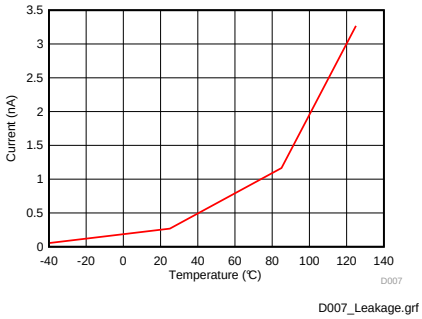


Figure 7. Leakage Current at 3.6 V Bias Voltage Across Temperature, I/O Pin to GND

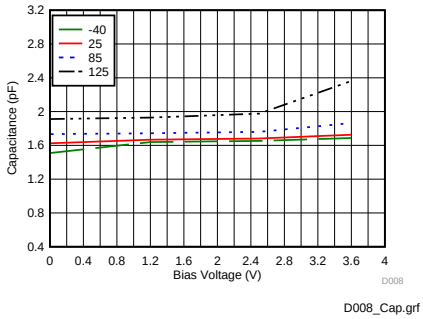


Figure 8. Capacitance Vs. Bias Voltage at Different Temperatures (°C)

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Typical Characteristics (continued)

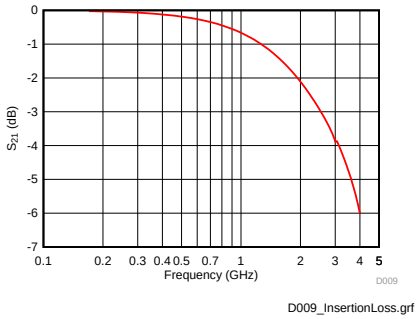


Figure 9. Insertion Loss Vs. Frequency

7 Detailed Description

7.1 Overview

The ESD351 is a uni-directional ESD Protection Diode with 30 kV IEC 61000-4-2 level (Contact and Air) with ultra-low clamping voltage in a 1 mm × 0.6 mm package. The ultra-low clamping makes this device capable of protecting any ESD-sensitive pins.

7.2 Functional Block Diagram



7.3 Feature Description

ESD351 provides ESD protection up to ±30-kV contact and ±30-kV air gap per IEC 61000-4-2 standard. During an ESD event, ESD diode connected to the I/O pin turns on and diverts the current to ground. Additionally, ESD351 also provides protection against IEC 61000-4-5 Surge currents up to 6 A (8/20µs waveform) and up to 80 A per IEC 61000-4-4 (5/50 ns waveform, 4 kV with 50-Ω impedance) electrical fast transient (EFT) standard. The capacitance between the I/O pin and ground is 1.8 pF (typical) and 2.2 pF (maximum). The device features a low leakage current of 0.1 nA (typical) and 50 nA (maximum, across operating temperature range) with a bias of 3.6 V. The ESD diode at the I/O pin protects the ESD-sensitive devices by clamping the voltage to a low value of 6.5 V (I_{PP} = 16 A 100 ns TLP). The layout of this device makes it simple and easy to add protection to an existing layout. The packages offers flow-through routing, requiring minimal modification to an existing layout.

7.4 Device Functional Modes

The ESD351 is a passive integrated circuit that triggers when voltages are above V_{BRF} or below V_{FWD}. During ESD events, voltages as high as ±30 kV (contact or air) can be directed to ground via the internal diode network. When the voltages on the protected line fall below the trigger levels of ESD351 (usually within 10s of nano-seconds) the device reverts to passive.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The ESD351 is a diode type TVS which is used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

8.2 Typical Application

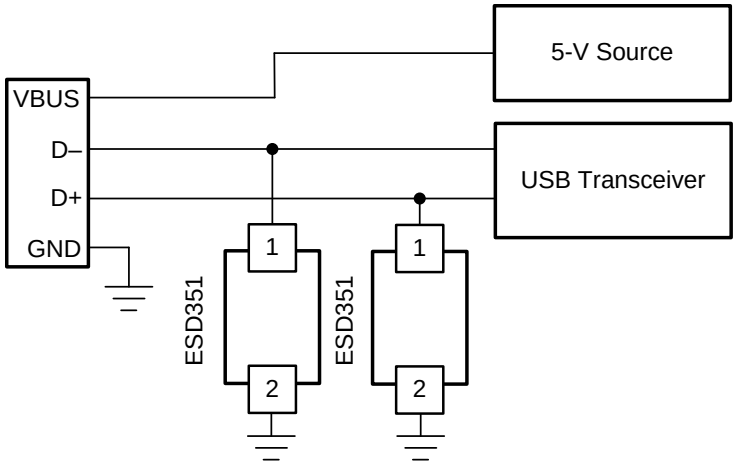


Figure 10. USB 2.0 ESD Schematic

8.2.1 Design Requirements

For this design example, two ESD351 devices are being used in a USB 2.0 application. This provides a complete ESD protection scheme.

Given the USB 2.0 application, the parameters listed in Table 1 are known.

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on DP-DM lines	0 V to 3.6 V
Operating frequency on DP-DM lines	up to 240 MHz

8.2.2 Detailed Design Procedure

8.2.2.1 Signal Range

The ESD351 supports signal ranges between 0 V and 3.6 V, which supports the USB 2.0 signal pair on the USB 2.0 application.

8.2.2.2 Operating Frequency

The ESD351 has a 1.8 pF (typical) capacitance, which supports the USB 2.0 data rates of 480 Mbps.

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8.2.3 Application Curve

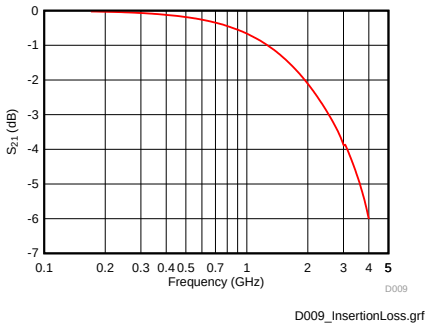


Figure 11. Insertion Loss

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9 Power Supply Recommendations

The ESD351 is a passive ESD device so there is no need to power it. Take care not to violate the recommended I/O specification (0 V to 3.6 V) to ensure the device functions properly.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example

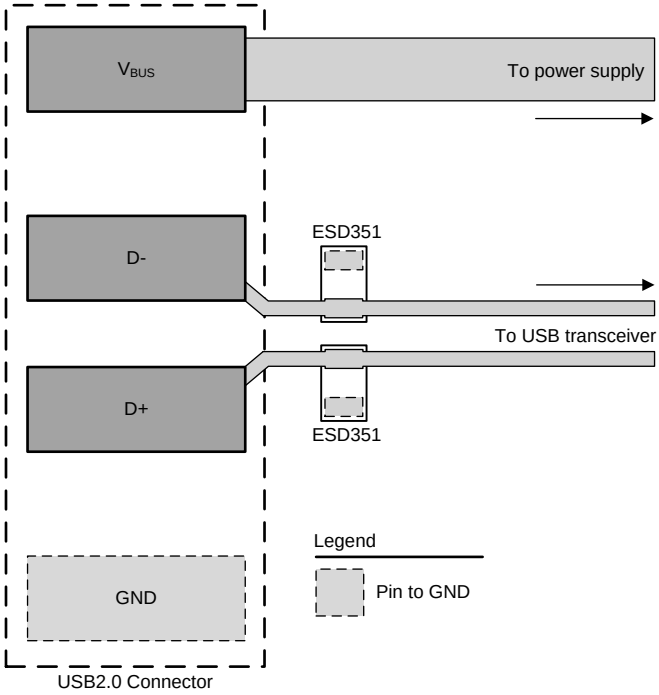


Figure 12. USB 2.0 ESD Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

Generic ESD Device Evaluation Module, SLVUBG5

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

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11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ESD351DPYR	Active	Production	X1SON (DPY) | 2	10000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DE
ESD351DPYR.B	Active	Production	X1SON (DPY) | 2	10000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	DE
ESD351DPYRG4	Active	Production	X1SON (DPY) | 2	10000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DE
ESD351DPYRG4.B	Active	Production	X1SON (DPY) | 2	10000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DE

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

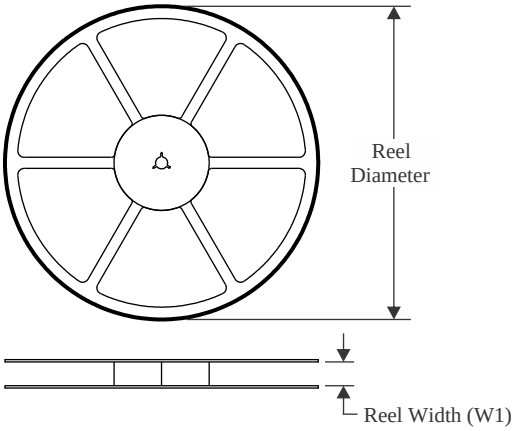
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

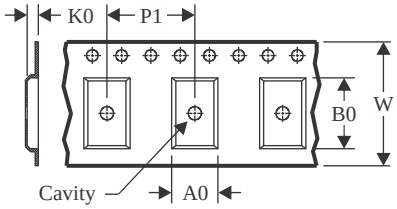
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

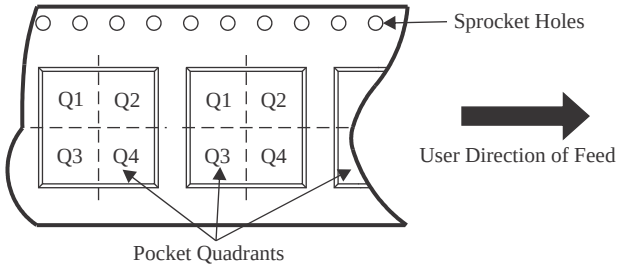


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

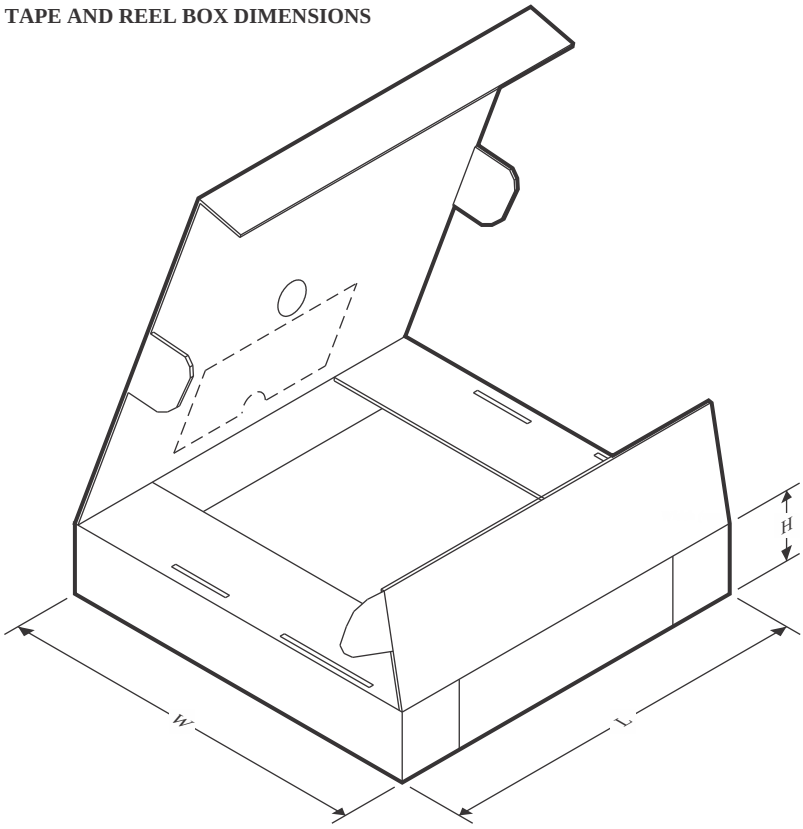
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD351DPYR	X1SON	DPY	2	10000	178.0	8.4	0.7	1.15	0.47	2.0	8.0	Q1
ESD351DPYR	X1SON	DPY	2	10000	178.0	8.4	0.67	1.15	0.46	2.0	8.0	Q2
ESD351DPYR	X1SON	DPY	2	10000	180.0	8.4	0.7	1.1	0.47	2.0	8.0	Q1
ESD351DPYRG4	X1SON	DPY	2	10000	180.0	8.4	0.67	1.15	0.46	2.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD351DPYR	X1SON	DPY	2	10000	205.0	200.0	33.0
ESD351DPYR	X1SON	DPY	2	10000	208.0	191.0	35.0
ESD351DPYR	X1SON	DPY	2	10000	203.2	196.8	33.3
ESD351DPYRG4	X1SON	DPY	2	10000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DPY 2

X1SON - 0.45 mm max height

1 x 0.6 mm

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



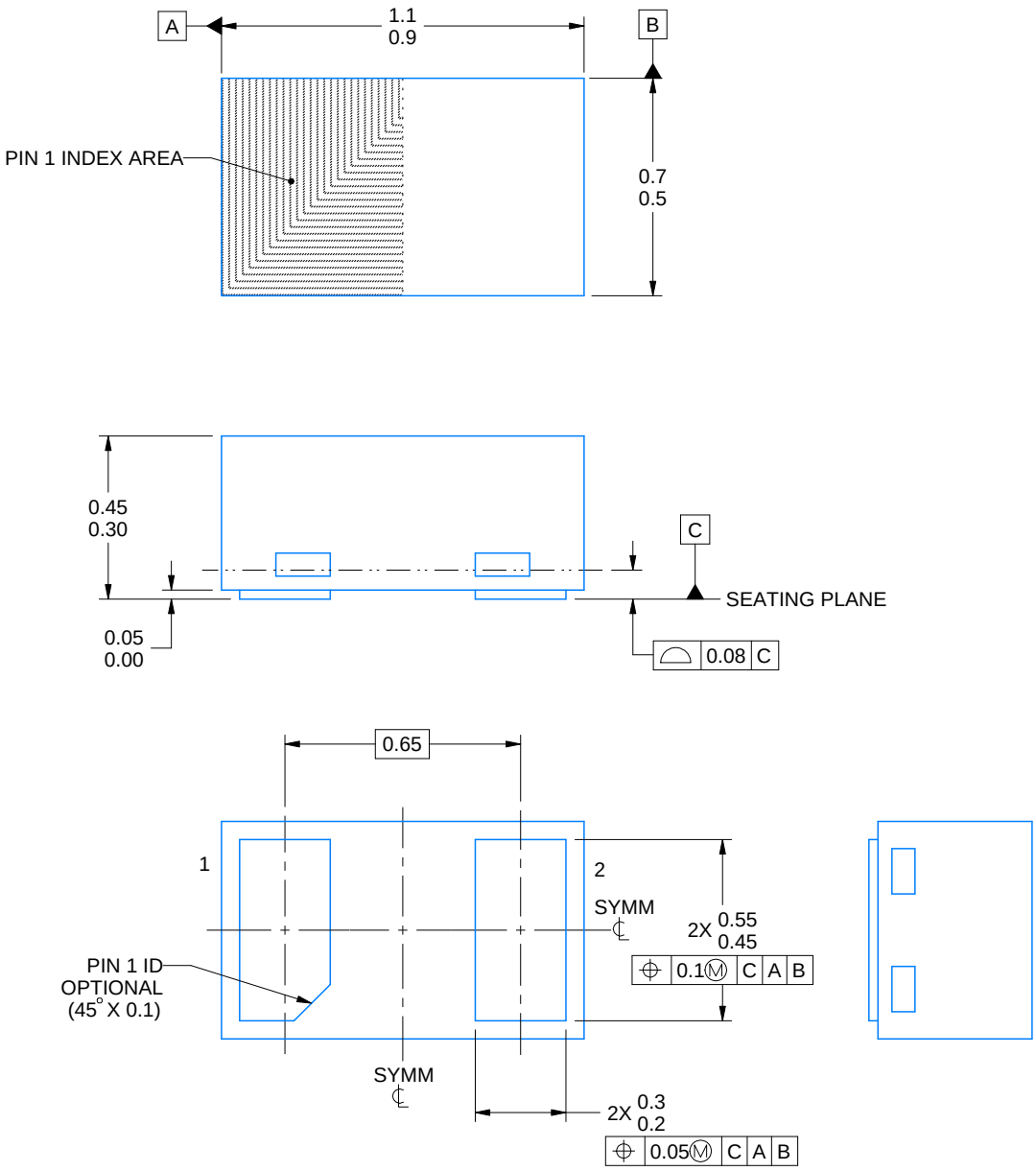
4231484/A

PACKAGE OUTLINE

DPY0002A

X1SON - 0.45 mm max height

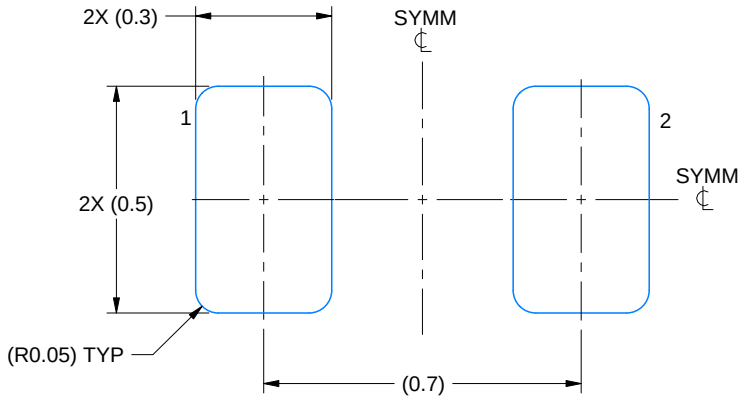
PLASTIC SMALL OUTLINE - NO LEAD



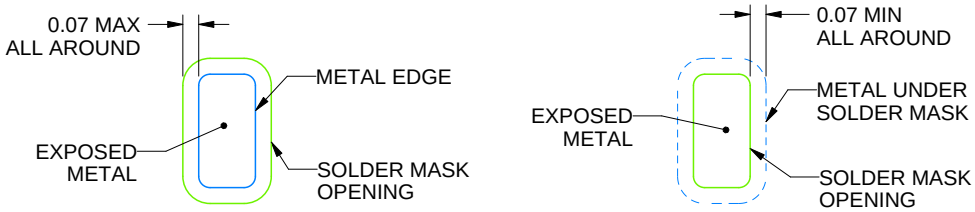
4224561/C 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X

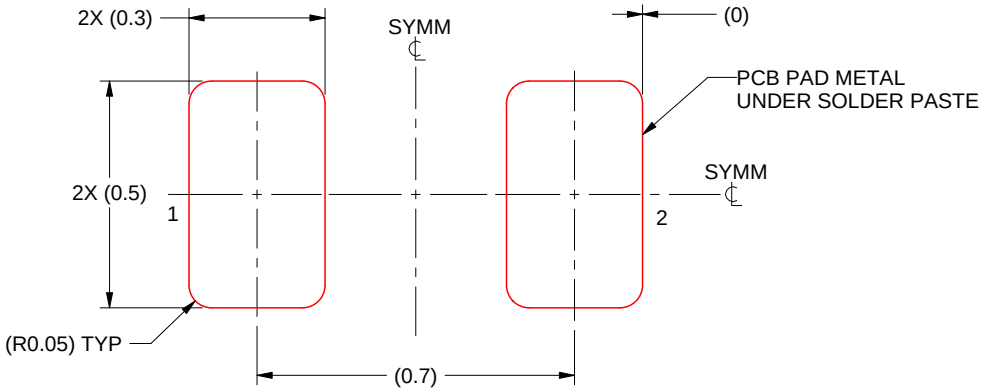


SOLDER MASK DETAILS

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NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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