High Accuracy
INSTRUMENTATION AMPLIFIER

FEATURES

● **LOW DRIFT: 0.25µV/°C max**
● **LOW OFFSET VOLTAGE: 25µV max**
● **LOW NONLINEARITY: 0.002%**
● **LOW NOISE: 13nV/√Hz**
● **HIGH CMR: 106dB AT 60Hz**
● **HIGH INPUT IMPEDANCE: $10^{10}\Omega$**
● **14-PIN PLASTIC, CERAMIC DIP, SOL-16, AND TO-100 PACKAGES**

APPLICATIONS

● **STRAIN GAGES**
● **THERMOCOUPLES**
● **RTDs**
● **REMOTE TRANSDUCERS**
● **LOW-LEVEL SIGNALS**
● **MEDICAL INSTRUMENTATION**

DESCRIPTION

The INA101 is a high accuracy instrumentation amplifier designed for low-level signal amplification and general purpose data acquisition. Three precision op amps and laser-trimmed metal film resistors are integrated on a single monolithic integrated circuit.

The INA101 is packaged in TO-100 metal, 14-pin plastic and ceramic DIP, and SOL-16 surface-mount packages. Commercial, industrial and military temperature range models are available.
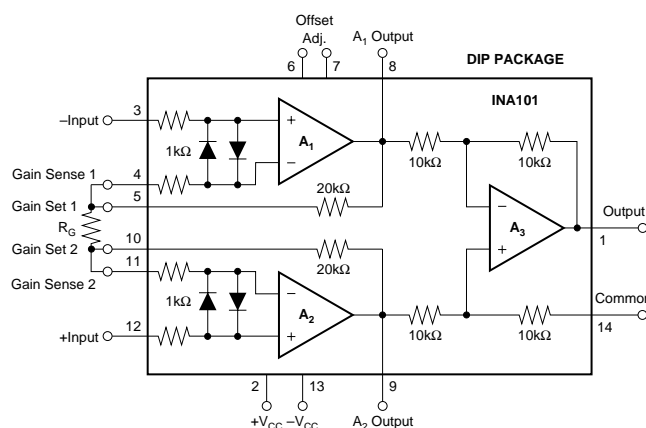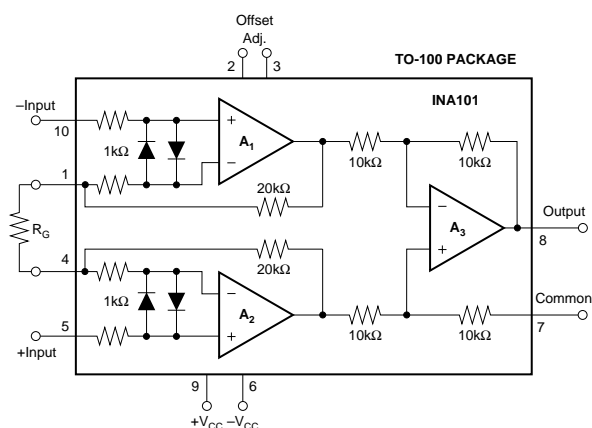
SPECIFICATIONS

ELECTRICAL

At +25°C with ±15VDC power supply and in circuit of Figure 1, unless otherwise noted.

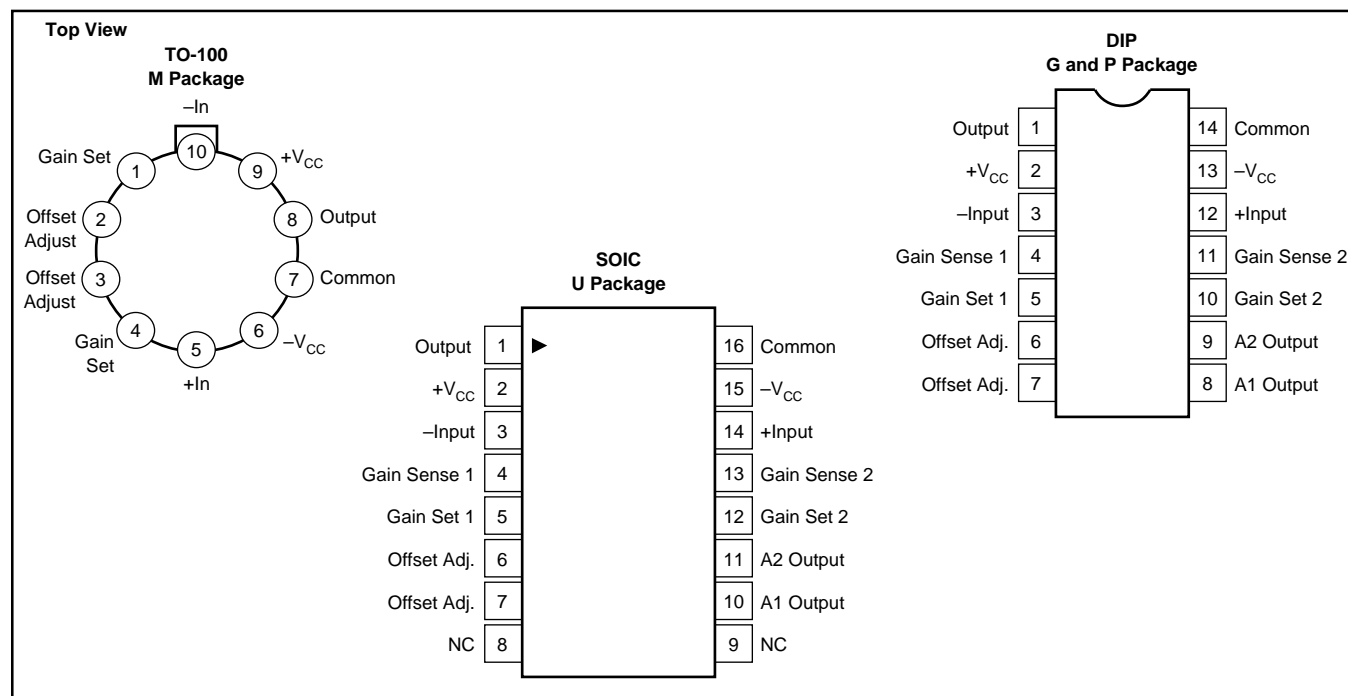| PARAMETER	INA101AM, AG MIN	TYP	MAX	INA101SM, SG MIN	TYP	MAX	INA101CM, CG MIN	TYP	MAX	INA101HP, KU MIN	TYP	MAX	UNITS
GAIN													
Range of Gain	1		1000	*	*	*	*	*	*	*	*	*	V/V
Gain Equation		$G = 1 + (40k/R_G)$			*			*			*		V/V
Error from Equation, DC[1]		$\pm(0.04 + 0.00016G$ $-0.02/G)$	$\pm(0.1 + 0.0003G$ $-0.05/G)$		*	*		*	*		$\pm(0.1 +$ $0.00015G)$ $-0.05/G$	$\pm(0.3 +$ $0.0002G)$ $-0.10/G$	%
Gain Temp. Coefficient[3]													
G = 1		2	5		*	*		*	*		*	*	ppm/°C
G = 10		20	100		*	*		10	*		*	*	ppm/°C
G = 100		22	110		*	*		11	*		*	*	ppm/°C
G = 1000		22	110		*	*		11	*		*	*	ppm/°C
Nonlinearity, DC[2]		$\pm(0.002 + 10^{-5} G)$	$\pm(0.005 + 2 \times 10^{-5} G)$		$\pm(0.001$ $+10^{-5} G)$	$\pm(0.002$ $+10^{-5} G)$		$\pm(0.001$ $+10^{-5} G)$	$\pm(0.002$ $+10^{-5} G)$		*	*	% of p-p FS
RATED OUTPUT													
Voltage	±10	±12.5		*	*		*	*		*	*		V
Current	±5	±10		*	*		*	*		*	*		mA
Output Impedance		0.2			*			*			*		Ω
Capacitive Load		1000			*			*			*		pF
INPUT OFFSET VOLTAGE													
Initial Offset at +25°C		$\pm(25 + 200/G)$	$\pm(50 + 400/G)$		$\pm 10+$ $100/G$	$\pm(25$ $+200/G)$		$\pm(10+$ $100/G$	$\pm(25 +$ $200/G)$		$\pm(125 +$ $450/G)$	$\pm(250 +$ $900/G)$	μV
vs Temperature			$\pm(2 + 20/G)$			$\pm(0.75$ $+ 10/G)$			$\pm(0.25 +$ $10/G)$		$\pm(2 + 20/G)$		μV/°C
vs Supply		$\pm(1 + 20/G)$			*			*			*		μV/V
vs Time		$\pm(1 + 20/G)$			*			*			*		μV/mo
INPUT BIAS CURRENT													
Initial Bias Current													
(each input)		±15	±30		±10	*		±5	±20		*	*	nA
vs Temperature		±0.2			*			*			*		nA/°C
vs Supply		±0.1			*			*			*		nA/V
Initial Offset Current		±15	±30		±10	*		±5	±20		*	*	nA
vs Temperature		±0.5			*			*			*		nA/°C
INPUT IMPEDANCE													
Differential		$10^{10} \| 3$			*			*			*		Ω | pF
Common-mode		$10^{10} \| 3$			*			*			*		Ω | pF
INPUT VOLTAGE RANGE													
Range, Linear Response	±10	±12		*	*		*	*		*	*		V
CMR with 1kΩ Source Imbalance													
DC to 60Hz, G = 1	80	90		*	*		*	*		65	85		dB
DC to 60Hz, G = 10	96	106		*	*		*	*		90	95		dB
DC to 60Hz, G = 100 to 1000	106	110		*	*		*	*		100	105		dB
INPUT NOISE													
Input Voltage Noise													
f_B = 0.01Hz to 10Hz		0.8			*			*			*		μV, p-p
Density, G = 1000													
f_O = 10Hz		18			*			*			*		nV/√Hz
f_O = 100Hz		15			*			*			*		nV/√Hz
f_O = 1kHz		13			*			*			*		nV/√Hz
Input Current Noise													
f_B = 0.01Hz to 10Hz		50			*			*			*		pA, p-p
Density													
f_O = 10Hz		0.8			*			*			*		pA/√Hz
f_O = 100Hz		0.46			*			*			*		pA/√Hz
f_O = 1kHz		0.35			*			*			*		pA/√Hz
DYNAMIC RESPONSE													
Small Signal, ±3dB Flatness													
G = 1		300			*			*			*		kHz
G = 10		140			*			*			*		kHz
G = 100		25			*			*			*		kHz
G = 1000		2.5			*			*			*		kHz
Small Signal, ±1% Flatness													
G = 1		20			*			*			*		kHz
G = 10		10			*			*			*		kHz
G = 100		1			*			*			*		kHz
G = 1000		200			*			*			*		Hz
Full Power, G = 1 to 100		6.4			*			*			*		kHz
Slew Rate, G = 1 to 100	0.2	0.4		*	*		*	*		*	*		V/μs
Settling Time (0.1%)													
G = 1		30	40		*	*		*	*		*	*	μs
G = 100		40	55		*	*		*	*		*	*	μs
G = 1000		350	470		*	*		*	*		*	*	μs
Settling Time (0.01%)													
G = 1		30	45		*	*		*	*		*	*	μs
G = 100		50	70		*	*		*	*		*	*	μs
G = 1000		500	650		*	*		*	*		*	*	μs
POWER SUPPLY													
Rated Voltage		±15			*			*			*		V
Voltage Range	±5		±20	*		*	*		*	*		*	V
Current, Quiescent[2]		±6.7	±8.5		*	*		*	*		*	*	mA
TEMPERATURE RANGE[5]													
Specification	−25		+85	−55		+125	*		*	0		+70	°C
Operation	−55		+125	*		*	*		*	−25		+85	°C
Storage	−65		+150	*		*	*		*	−40		+85	°C

* Specifications same as for INA101AM, AG.

NOTES: (1) Typically the tolerance of R_G will be the major source of gain error. (2) Nonlinearity is the maximum peak deviation from the best straight-line as a percentage of peak-to-peak full scale output. (3) Not including the TCR of R_G. (4) Adjustable to zero at any one gain. (5) θ_{JC} output stage = 113°C/W, θ_{JC} quiescent circuitry = 19°C/W, θ_{CA} = 83°C/W.

PIN CONFIGURATIONS

Top View

TO-100
M Package

Gain Set (1)
Offset Adjust (2)
Offset Adjust (3)
Gain Set (4)
(5) +In
(6) −V_{CC}
(7) Common
(8) Output
(9) +V_{CC}
(10) −In

SOIC
U Package

Output	1	►	16	Common
+V_{CC}	2		15	−V_{CC}
−Input	3		14	+Input
Gain Sense 1	4		13	Gain Sense 2
Gain Set 1	5		12	Gain Set 2
Offset Adj.	6		11	A2 Output
Offset Adj.	7		10	A1 Output
NC	8		9	NC

DIP
G and P Package

Output	1		14	Common
+V_{CC}	2		13	−V_{CC}
−Input	3		12	+Input
Gain Sense 1	4		11	Gain Sense 2
Gain Set 1	5		10	Gain Set 2
Offset Adj.	6		9	A2 Output
Offset Adj.	7		8	A1 Output

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... ±20V
Power Dissipation 600mW
Input Voltage Range .... ±V_{CC}
Output Short Circuit (to ground) .... Continuous
Operating Temperature M, G Package .... −55°C to +125°C
  P, U Package .... −25°C to +85°C
Storage Temperature M, G Package .... −65°C to +150°C
  P, U Package .... −40°C to +85°C
Lead Temperature (soldering, 10s) M, G, P Package .... +300°C
Lead Temperature (wave soldering, 3s) U Package .... +260°C

 ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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TYPICAL PERFORMANCE CURVES

At +25°C, $V_{CC} = \pm15V$ unless otherwise noted.

GAIN NONLINEARITY vs GAIN

GAIN vs FREQUENCY

CMR vs FREQUENCY

WARM-UP DRIFT vs TIME

QUIESCENT CURRENT vs SUPPLY

STEP RESPONSE
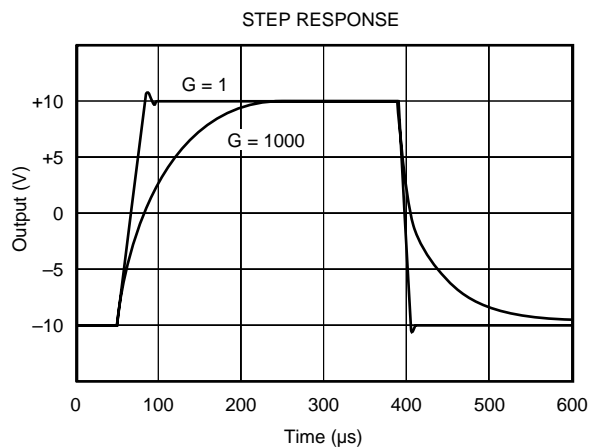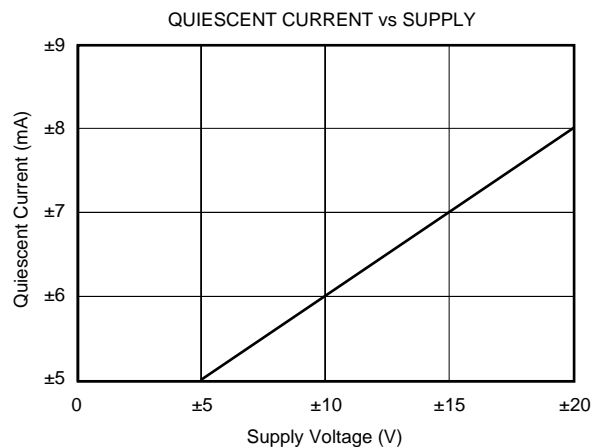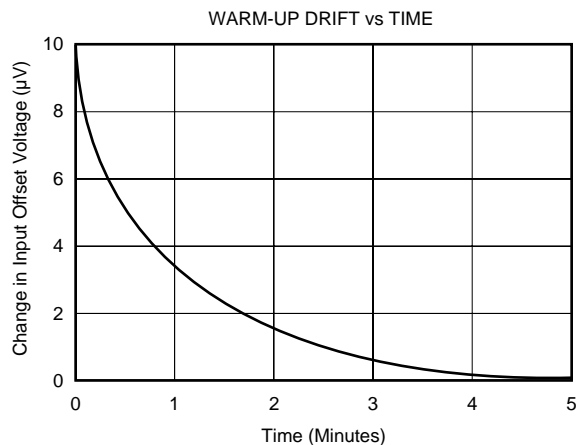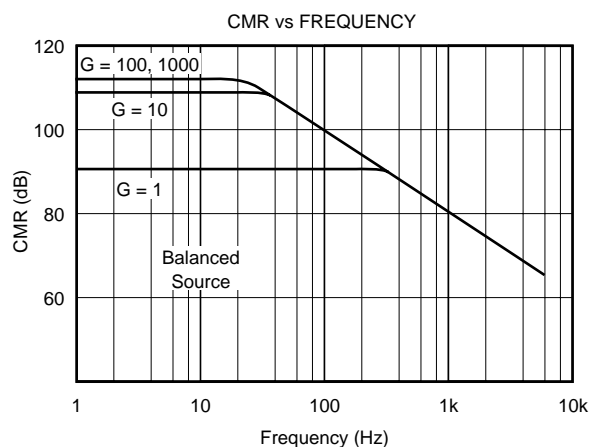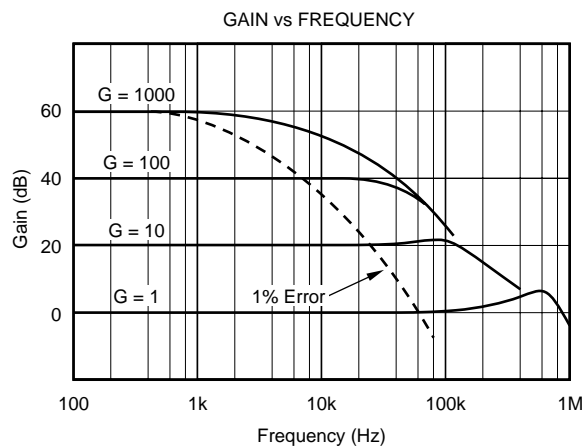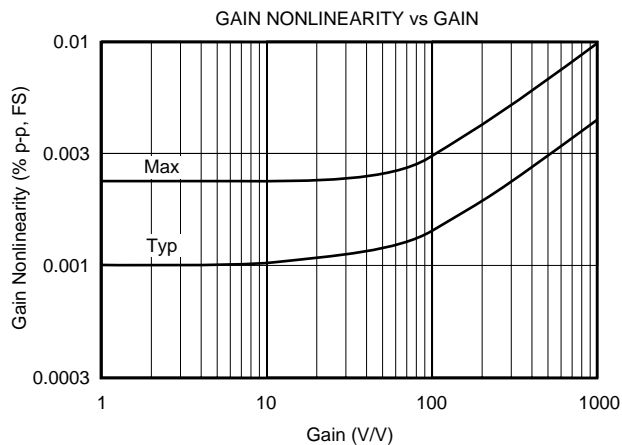
TYPICAL PERFORMANCE CURVES (CONT)

At +25°C, $V_{CC} = \pm 15V$ unless otherwise noted.

SETTLING TIME vs GAIN

$R_L = 2k\Omega$
$C_L = 1000pF$

0.01%

0.1%

1%

Settling Time (μs)

Gain (V/V)

OUTPUT NOISE vs GAIN

Output Noise Voltage (mV, rms)

$R_S = 1M\Omega$

$R_S = 1000k\Omega$

$R_S = 10k\Omega$

$R_S = 0$

Gain (V/V)

INPUT NOISE VOLTAGE
vs FREQUENCY (100 ≤ GAIN ≤ 1000)

Input Noise Voltage (nV/$\sqrt{Hz}$)

Frequency (Hz)
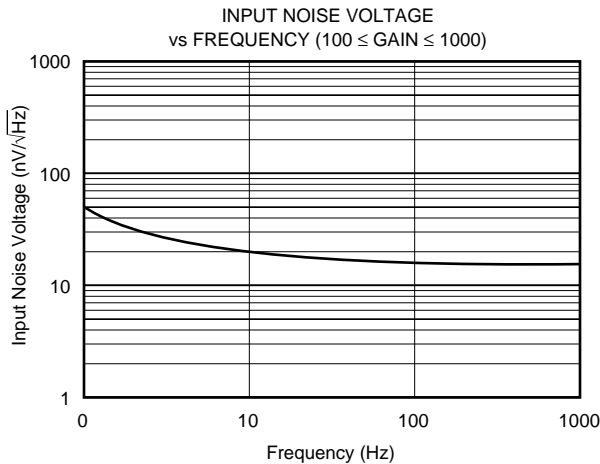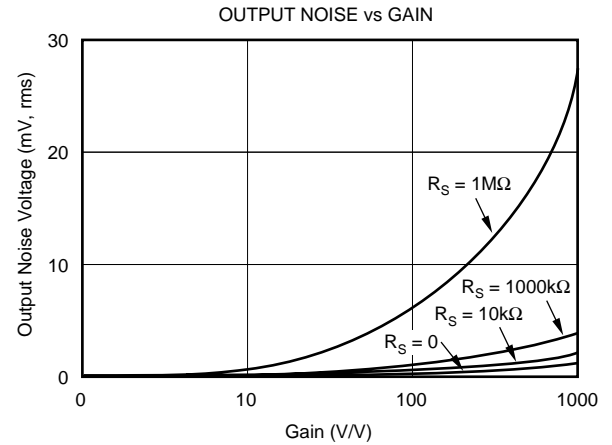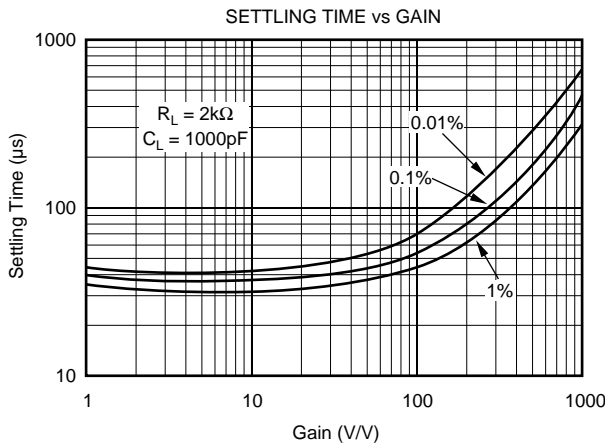
APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA101. (Pin numbers shown are for the TO-100 metal package.) Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output Common terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance greater than 0.1Ω in series with the Common pin will cause common-mode rejection to fall below 106dB.

SETTING THE GAIN

Gain of the INA101 is set by connecting a single external resistor, R_G:

$$G = 1 + \frac{40k\Omega}{R_G} \qquad (1)$$

The $40k\Omega$ term in equation (1) comes from the sum of the two internal feedback resistors. These are on-chip metal film resistors which are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA101.

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. R_G's contribution to gain accuracy and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance which will contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater. The gain sense connections on the DIP and SOL-16 packages (see Figure 2) reduce the gain error produced by wiring or socket resistance.

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OFFSET TRIMMING

The INA101 is laser trimmed for low offset voltage and drift. Most applications require no external offset adjustment. Figure 2 shows connection of an optional potentiometer connected to the Offset Adjust pins for trimming the input offset voltage. (Pin numbers shown are for the DIP package.) Use this adjustment to null the offset voltage in high gain (G ≥ 100) with both inputs connected to ground. Do not use this adjustment to null offset produced by the source or other system offset since this will increase the offset voltage drift by 0.3µV/°C per 100µV of adjusted offset.

Offset of the output amplifier usually dominates when the INA101 is used in unity gain (G = 1). The output offset voltage can be adjusted with the optional trim circuit connected to the Common pin as shown in Figure 2. The voltage applied to Common terminal is summed with the output. Low impedance must be maintained at this node to assure good common-mode rejection. The op amp connected as a buffer provides low impedance.

THERMAL EFFECTS ON OFFSET VOLTAGE

To achieve lowest offset voltage and drift, prevent air currents from circulating near the INA101. Rapid changes in temperature will produce a thermocouple effect on the package leads that will degrade offset voltage and drift. A shield or cover that prevents air currents from flowing near the INA101 will assure best performance.
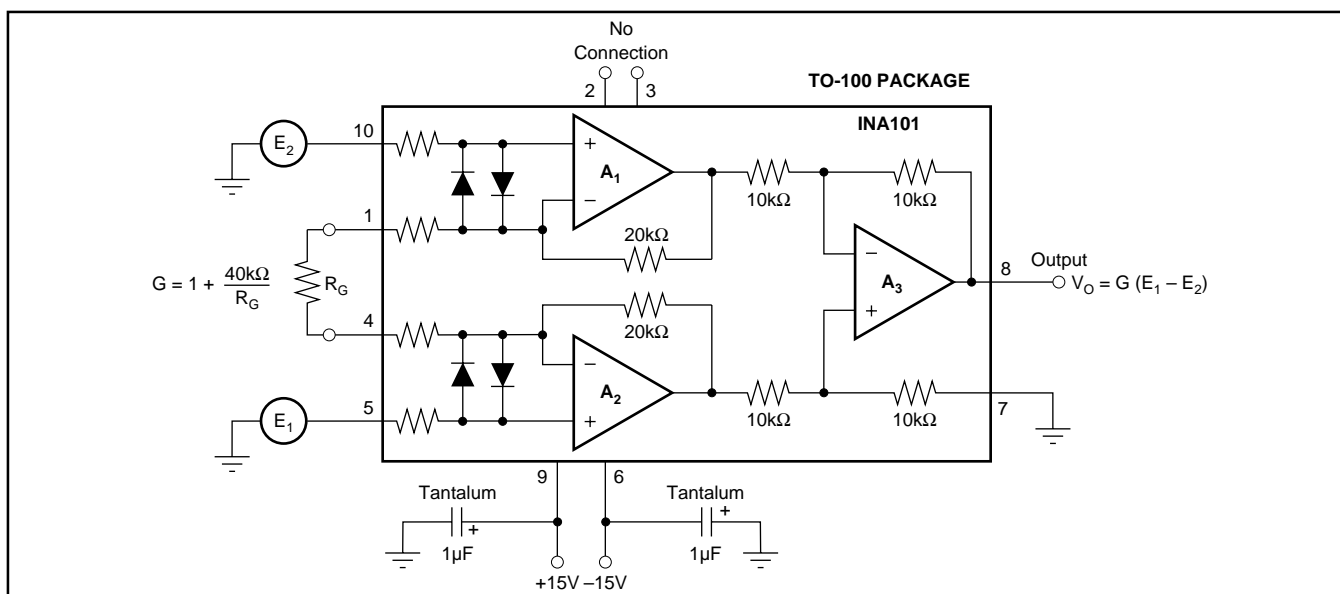
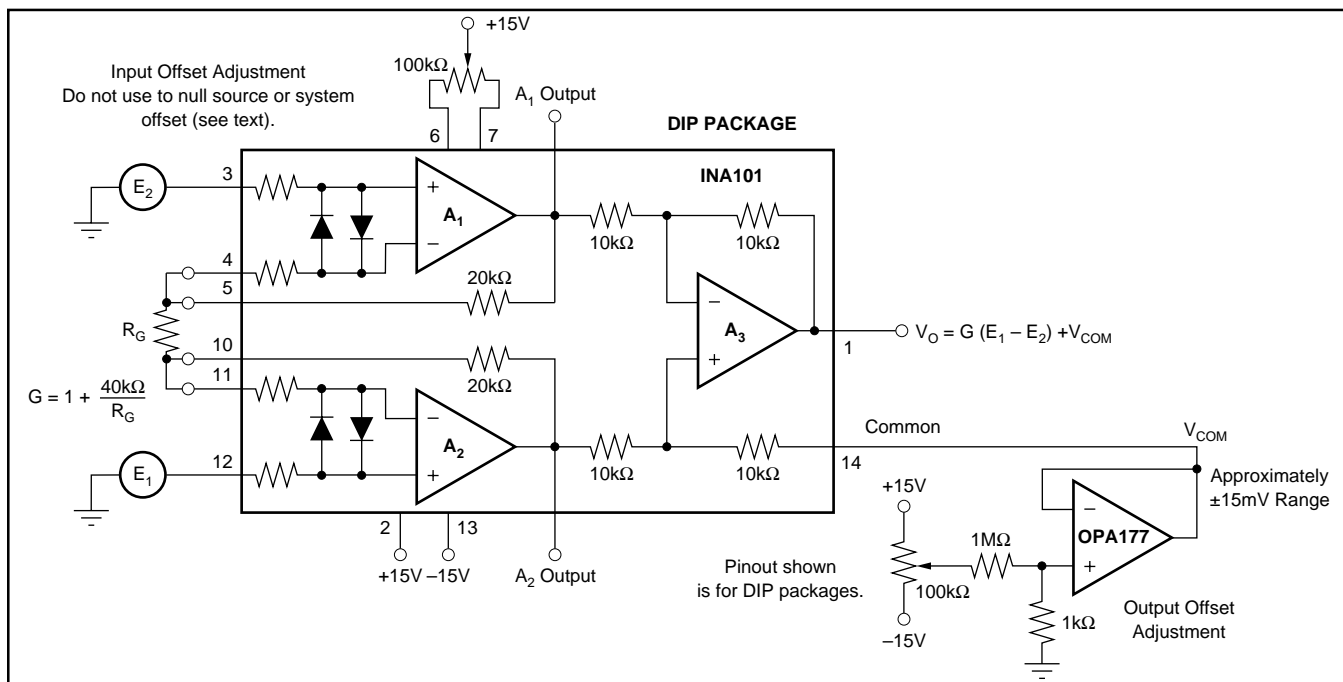

FIGURE 1. Basic Connections.

FIGURE 2. Optional Trimming of Input and Output Offset Voltage.

INA101

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PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA101AG	Active	Production	CDIP SB (JD) | 14	24 | TUBE	Yes	AU	N/A for Pkg Type	-	INA101AG
INA101AG.A	Active	Production	CDIP SB (JD) | 14	24 | TUBE	Yes	AU	N/A for Pkg Type	-55 to 125	INA101AG
INA101AM	Active	Production	TO-100 (LME) | 10	20 | TUBE	Yes	Call TI	N/A for Pkg Type	-	INA101AM
INA101AM.A	Active	Production	TO-100 (LME) | 10	20 | TUBE	Yes	Call TI	N/A for Pkg Type	-55 to 125	INA101AM
INA101CM	Active	Production	TO-100 (LME) | 10	20 | TUBE	Yes	Call TI	N/A for Pkg Type	-	INA101CM
INA101CM.A	Active	Production	TO-100 (LME) | 10	20 | TUBE	Yes	Call TI	N/A for Pkg Type	-55 to 125	INA101CM
INA101HP	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	INA101HP
INA101HP.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	INA101HP
INA101KU	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-	INA101KU
INA101KU.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	INA101KU
INA101KU/1K	Active	Production	SOIC (DW) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-	INA101KU
INA101KU/1K.A	Active	Production	SOIC (DW) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	INA101KU
INA101SM	Active	Production	TO-100 (LME) | 10	20 | TUBE	Yes	AU	N/A for Pkg Type	-	INA101SM
INA101SM.A	Active	Production	TO-100 (LME) | 10	20 | TUBE	Yes	AU	N/A for Pkg Type	-55 to 125	INA101SM

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA101KU/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA101KU/1K	SOIC	DW	16	1000	353.0	353.0	32.0

TUBE

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
INA101AG	JD	CDIP SB	14	24	506.98	15.24	12290	NA
INA101AG.A	JD	CDIP SB	14	24	506.98	15.24	12290	NA
INA101AM	LME	TO-CAN	10	20	532.13	21.59	889	NA
INA101AM.A	LME	TO-CAN	10	20	532.13	21.59	889	NA
INA101CM	LME	TO-CAN	10	20	532.13	21.59	889	NA
INA101CM.A	LME	TO-CAN	10	20	532.13	21.59	889	NA
INA101HP	N	PDIP	14	25	506	13.97	11230	4.32
INA101HP.A	N	PDIP	14	25	506	13.97	11230	4.32
INA101KU	DW	SOIC	16	40	507	12.83	5080	6.6
INA101KU.A	DW	SOIC	16	40	507	12.83	5080	6.6
INA101SM	LME	TO-CAN	10	20	532.13	21.59	889	NA
INA101SM.A	LME	TO-CAN	10	20	532.13	21.59	889	NA

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