INA745x 40V, 16-Bit, Precision I²C Output Digital Power Monitor With EZShunt™ Technology

1 Features

- Low loss integrated shunt resistor
  - Internal resistance: 800µΩ, T_A = 25°C
  - Continuous current: ±35A, T_A = 25°C
  - Peak measurement capability: ±39.32A
- Current monitoring accuracy: A/B Grade (maximum)
  - Offset current: ±6.25mA / ±62.5mA
  - Offset drift: ±30µA/°C (A and B Grades)
  - System gain error: ±0.75% / ±1.25%
  - Common-mode rejection: ±0.125 / ±1.25mA/V
- Power monitoring accuracy: A/B Grade, (maximum)
  - ±0.9% / ±1.6% at 25°C, full scale
- Energy and charge accuracy: A/B Grade, (maximum)
  - ±1.4% / ±2.1% at 25°C, full scale
- Temperature sensor: ±1.5°C (maximum at 25°C)
- Precision oscillator: ±0.5% (maximum at 25°C)
- Programmable conversion time and averaging
- 2.94MHz high-speed I²C interface with 16 pin-selectable addresses
- Operates from a 2.7V to 5.5V supply:
  - Operational current: 640µA (typical)
  - Shutdown current: 5µA (maximum)

2 Applications

- Power delivery
- Grid infrastructure
- Industrial battery packs
- Test equipment
- Telecom equipment
- Enterprise servers

3 Description

The INA745x is a digital power monitor with an integrated current sensing element along with a 16-bit delta-sigma ADC specifically designed for current-sensing applications. The device can measure full-scale currents up to ±39.32A with common-mode voltage support from –0.1V to +40V.

The INA745x reports current, bus voltage, die temperature, power, energy and charge accumulation while employing a precision ±0.5% integrated oscillator, all while performing the needed calculations in the background. The integrated temperature sensor is ±2.5°C accurate over the junction temperature range.

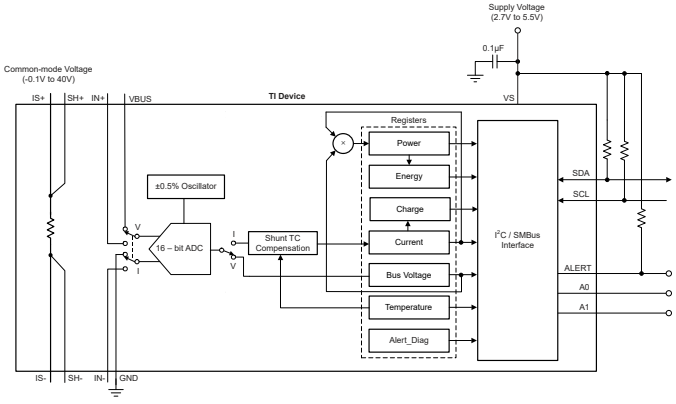
The low offset and gain drift design of the INA745x allows the device to be used in precise systems that do not undergo multi-temperature calibration during manufacturing.

The device allows for selectable ADC conversion times from 50µs to 4.12ms as well as sample averaging from 1x to 1024x, which further helps reduce the noise of the measured data.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
INA745A, INA745B	REL (QFN, 14)	5.00mm × 3.00mm

(1) For all available packages, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Block Diagram

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4 Pin Configuration and Functions

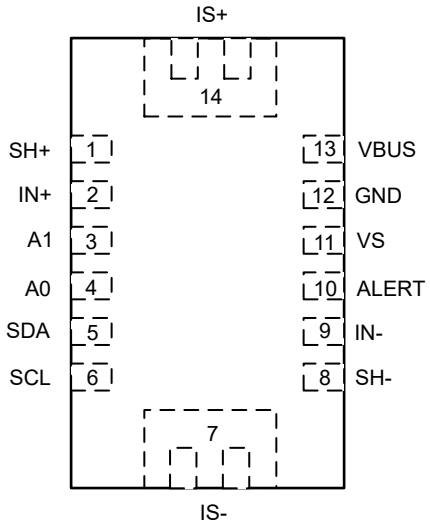


Figure 4-1. REL Package 14-Pin QFN Top View

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	SH+	Analog output	Shunt positive sense connection
2	IN+	Analog input	Positive input to digital power monitor.
3	A1	Digital input	I^2C address pin. Connect to GND, SCL, SDA, or VS.
4	A0	Digital input	I^2C address pin. Connect to GND, SCL, SDA, or VS.
5	SDA	Digital input/output	Open-drain bidirectional I^2C data.
6	SCL	Digital input	I^2C clock input.
7	IS–	Analog input	Negative high current shunt connection.
8	SH–	Analog output	Shunt negative sense connection.
9	IN–	Analog input	Negative input to digital power monitor.
10	ALERT	Digital output	Open-drain alert output, default state is active low.
11	VS	Power supply	Power supply, 2.7V to 5.5V.
12	GND	Ground	Ground.
13	VBUS	Analog input	Bus voltage input.
14	IS+	Analog input	Positive high current shunt connection.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Supply voltage		6	V
V_{IN+}, V_{IN-} (2)	Common mode voltage	–0.3	42	V
V_{ALERT}	ALERT	–0.3	Vs + 0.3	V
V_{IO}	SDA, SCL	–0.3	6	V
I_{IN}	Input current into any pin, excluding IS+ and IS–		5	mA
I_{OUT}	Digital output current		10	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) VIN+ and VIN– are the voltages at the IN+ and IN– pins, respectively.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2500	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input voltage	–0.1		40	V
V_S	Operating supply voltage	2.7		5.5	V
T_A	Specified ambient temperature	–40		125	°C

5.4 Thermal Information

THERMAL METRIC(1) (2)		INA745 REL (QFN) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	103.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	66.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	6.1	°C/W
Y_{JB}	Junction-to-board characterization parameter	65.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.
(2) Thermal metrics are relative to the internal die and are conservative relative to the heating that would occur from the package leadframe shunt. For more details on heating, see the Safe Operating Area section.

5.5 Electrical Characteristics

at T_A = 25 °C, V_S = 3.3 V, I_{SENSE} = 0 A, V_{CM} = $V_{IN–}$ = V_{BUS}= 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
CMRR	Common-mode rejection	–0.1 V < V_{CM} < 40 V, T_A = –40°C to +125°C	A devices		±25	±60	µA/V
			B devices		±0.5	±1.25	mA/V
I_{os}	Input offset current	T_{CT} > 280 µs	A devices		±0.9	±6.25	mA
			B devices		±7.5	±62.5	mA
dV_{os}/dT	Input offset current drift	T_A = –40°C to +125°C			±5	±30	µA/°C
PSRR	Input offset current vs power supply	V_S = 2.7 V to 5.5 V, T_A = –40°C to +125°C			±0.1	±4	mA/V
V_{os_bus}	V_{BUS} offset voltage	V_{BUS} = 20 mV			±2	±5	mV
dV_{os}/dT	V_{BUS} offset voltage drift	T_A = –40°C to +125°C	A devices		±8	±40	µV/°C
			B devices		±20	±100	µV/°C
PSRR	V_{BUS} offset voltage vs power supply	V_S = 2.7 V to 5.5 V			±1.1	±4	mV/V
DC ACCURACY							
G_{SERR}	System current sense gain error	I_{SENSE} = –25A to +25 A, V_{CM} = 12 V	A devices		±0.1	±0.75	%
G_{SERR}	System current sense gain error	I_{SENSE} = –25A to +25 A, V_{CM} = 12 V	B devices		±0.1	±1.25	%
G_{S_DRFT}	System current sense gain error drift	–40°C ≤ T_A ≤ 125°C				±75	ppm/°C
G_{BERR}	V_{BUS} voltage gain error	V_{BUS} = 0 V to 40 V	A devices		±0.01	±0.075	%
		V_{BUS} = 0 V to 40 V, –40°C ≤ T_A ≤ 125°C			±0.01	±0.35	%
		V_{BUS} = 0 V to 40 V	B devices		±0.01	±0.3	%
		V_{BUS} = 0 V to 40 V, –40°C ≤ T_A ≤ 125°C			±0.01	±0.8	%
G_{B_DRFT}	V_{BUS} voltage gain error drift	–40°C ≤ T_A ≤ 125°C	A devices			±25	ppm/°C
			B devices			±50	ppm/°C
Z_{BUS}	VBUS pin input impedance	Device enabled with active conversions			1		MΩ
P_{TME}	Power total measurement error (TME)	T_A = 25°C, at full scale	A devices			±0.9	%
			B devices			±1.6	%
E_{TME}	Energy and charge TME	T_A = 25°C, at full scale power	A devices			±1.4	%
			B devices			±2.1	%
	ADC resolution				16		Bits
	1 LSB step size	Current			1.2		mA
		Bus voltage			3.125		mV
		Temperature			125		m°C
		Power			240		µW
		Energy			3.84		mJ
		Charge			75		µC
T_{CT}	ADC conversion-time(1)	Conversion time field = 0h			50		µs
		Conversion time field = 1h			84		
		Conversion time field = 2h			150		
		Conversion time field = 3h			280		
		Conversion time field = 4h			540		
		Conversion time field = 5h			1052		
		Conversion time field = 6h			2074		
		Conversion time field = 7h			4120		
INL	Integral Non-Linearity	Bus voltage measurement			±2		m%

at T_A = 25 °C, V_S = 3.3 V, I_{SENSE} = 0 A, V_{CM} = $V_{IN–}$ = V_{BUS}= 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DNL	Differential Non-Linearity	Bus voltage measurement		0.2		LSB
CLOCK SOURCE						
F_{OSC}	Internal oscillator frequency			1		MHz
OSC_{TOL}	Internal oscillator frequency tolerance	T_A = 25°C			±0.5	%
		T_A = –40°C to +125°C			±1	%
TEMPERATURE SENSOR						
	Measurement range		–40		+150	°C
	Temperature accuracy	T_A = 25°C		±0.15	±1.5	°C
		T_A= –40°C to +125°C		±0.2	±2.5	°C
INTEGRATED SHUNT						
	Internal kelvin resistance	SH+ to SH–, T_A = 25°C		800		µΩ
	Pin to pin package resistance	IS+ to IS–, T_A = 25°C	800	1000	1300	µΩ
	Maximum continuous current	–40°C ≤ T_A ≤ 125°C			±25	A
	Short time overload change(2)	I_{SENSE} = 50 A for 5 seconds		±0.003		%
	Change due to temperature cycling	–65°C ≤ T_A ≤ 150°C, 500 cycles		±0.05		%
	Resistance change to solder heat	260°C solder, 10 s		±0.1		%
	High temperature exposure change	1000 hours, T_A = 150°C		±0.015		%
POWER SUPPLY						
V_S	Supply voltage		2.7		5.5	V
V_{POR}	POR Voltage Level	Supply rising		1.26		V
I_Q	Quiescent current	I_{SENSE} = 0 V		640	750	µA
		I_{SENSE} = 0 V, T_A = –40°C to +125°C			1	mA
I_{QSD}	Quiescent current, shutdown	Shutdown mode		2.8	5	µA
T_{POR}	Device start-up time	Power-up (NPOR)		300		µs
		From shutdown mode		60		
DIGITAL INPUT / OUTPUT						
V_{IH}	Logic input level, high	SDA, SCL	1.2		5.5	V
V_{IL}	Logic input level, low		GND		0.4	V
V_{OL}	Logic output level, low	I_{OL} = 3 mA	GND		0.4	V
I_{IO_LEAK}	Digital leakage input current	0 ≤ V_{IN} ≤ V_S	–1		1	µA

(1) Subject to oscillator accuracy and drift
(2) Tested on device EVM, see Section 6.3.2.

5.6 Timing Requirements (I^2C)

		MIN	NOM	MAX	UNIT
I^2C BUS (FAST MODE)					
$F_{(SCL)}$	I^2C clock frequency	1		400	kHz
$t_{(BUF)}$	Bus free time between STOP and START conditions	600			ns
$t_{(HDSTA)}$	Hold time after a repeated START condition. After this period, the first clock is generated.	100			ns
$t_{(SUSTA)}$	Repeated START condition setup time	100			ns
$t_{(SUSTO)}$	STOP condition setup time	100			ns
$t_{(HDDAT)}$	Data hold time	10		900	ns
$t_{(SUDAT)}$	Data setup time	100			ns
$t_{(LOW)}$	SCL clock low period	1300			ns
$t_{(HIGH)}$	SCL clock high period	600			ns
t_F	Data fall time			300	ns
t_F	Clock fall time			300	ns
t_R	Clock rise time			300	ns
I^2C BUS (HIGH-SPEED MODE)					
$F_{(SCL)}$	I^2C clock frequency	10		2940	kHz
$t_{(BUF)}$	Bus free time between STOP and START conditions	160			ns
$t_{(HDSTA)}$	Hold time after a repeated START condition. After this period, the first clock is generated.	100			ns
$t_{(SUSTA)}$	Repeated START condition setup time	100			ns
$t_{(SUSTO)}$	STOP condition setup time	100			ns
$t_{(HDDAT)}$	Data hold time	10		125	ns
$t_{(SUDAT)}$	Data setup time	20			ns
$t_{(LOW)}$	SCL clock low period	200			ns
$t_{(HIGH)}$	SCL clock high period	60			ns
t_F	Data fall time			80	ns
t_F	Clock fall time			40	ns
t_R	Clock rise time			40	ns

5.7 Timing Diagram

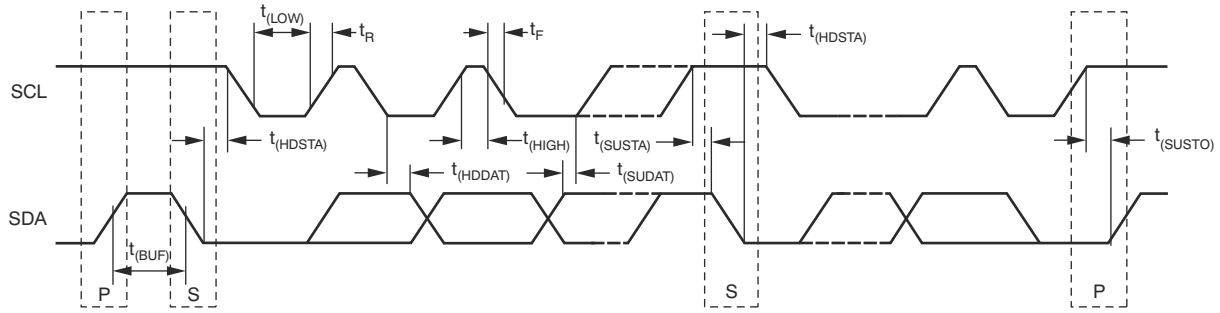


Figure 5-1. I^2C Timing Diagram

5.8 Typical Characteristics

at T_A = 25°C, V_{VS} = 3.3V, V_{CM} = 12V, V_{SENSE} = 0, and V_{VBUS} = 12V (unless otherwise noted)

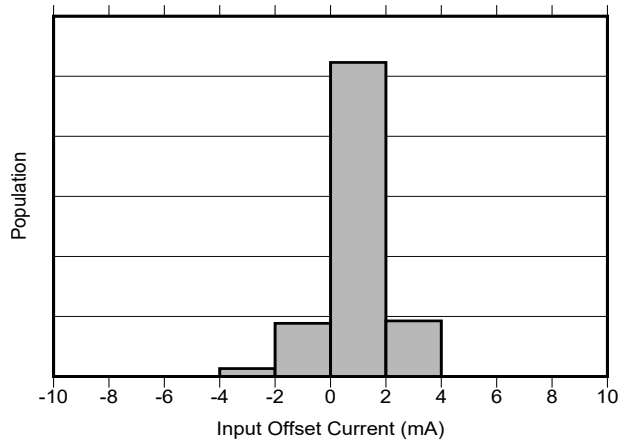


Figure 5-2. Shunt Input Offset Current Production Distribution

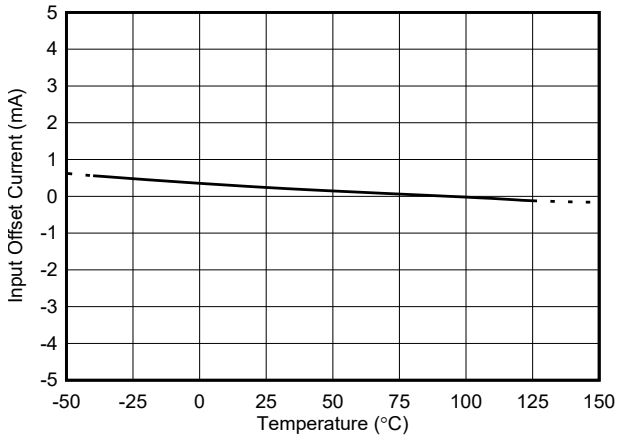


Figure 5-3. Input Offset Current vs Temperature

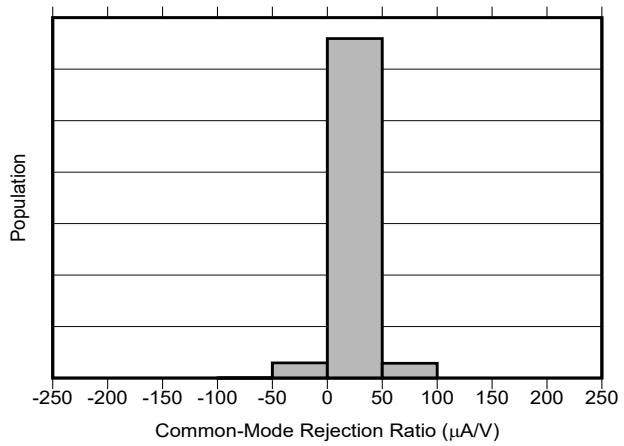


Figure 5-4. Common-Mode Rejection Ratio Production Distribution

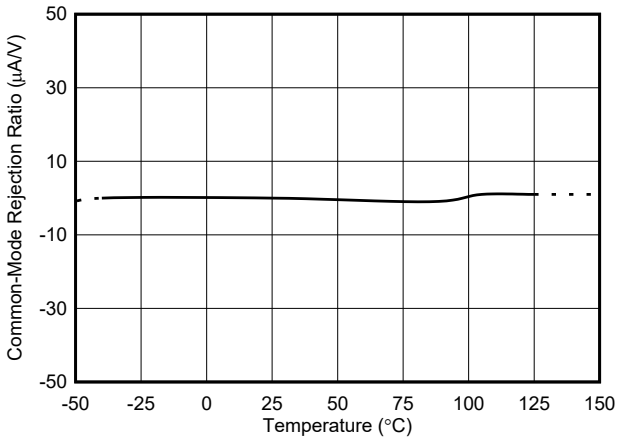


Figure 5-5. Current Common-Mode Rejection Ratio vs Temperature

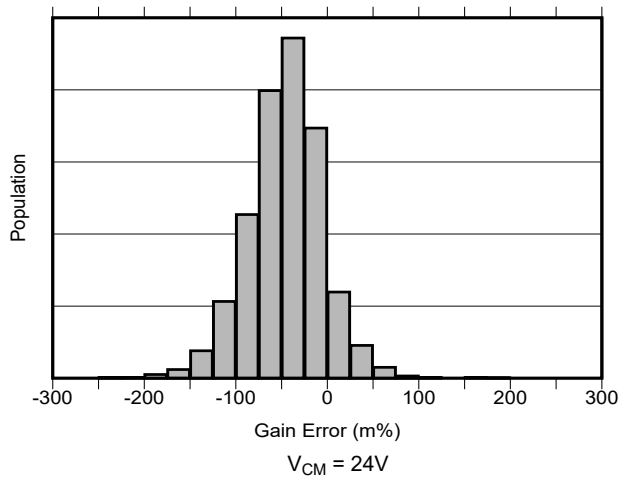


Figure 5-6. Current Gain Error Production Distribution

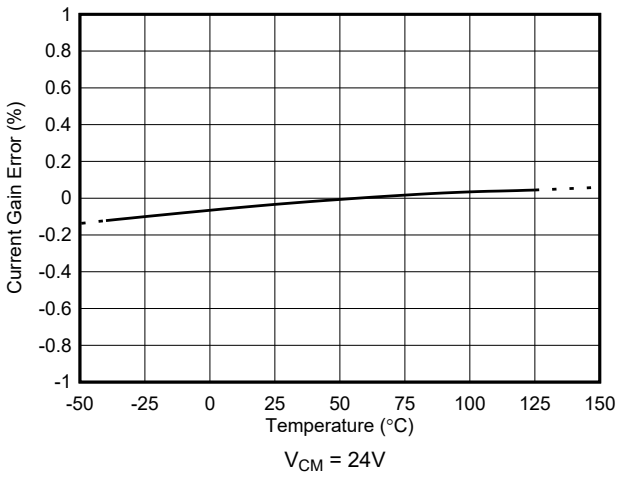


Figure 5-7. Current Gain Error vs Temperature

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_{VS} = 3.3V, V_{CM} = 12V, V_{SENSE} = 0, and V_{VBUS} = 12V (unless otherwise noted)

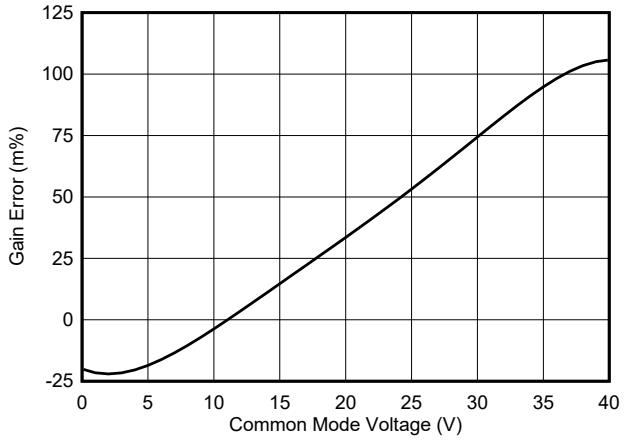


Figure 5-8. Current Gain Error vs Common-Mode Voltage

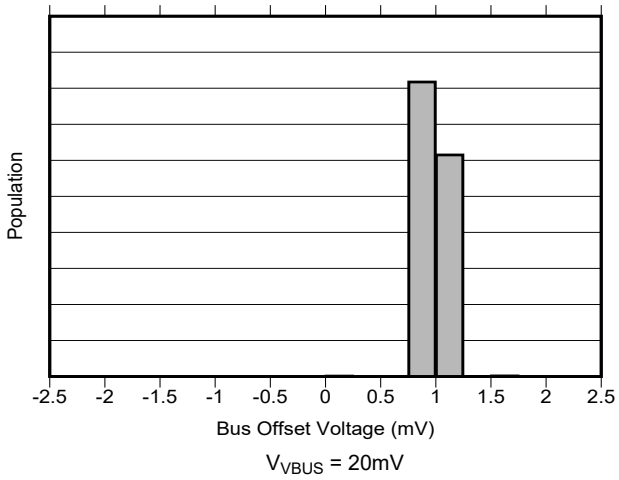


Figure 5-9. Bus Input Offset Voltage Production Distribution

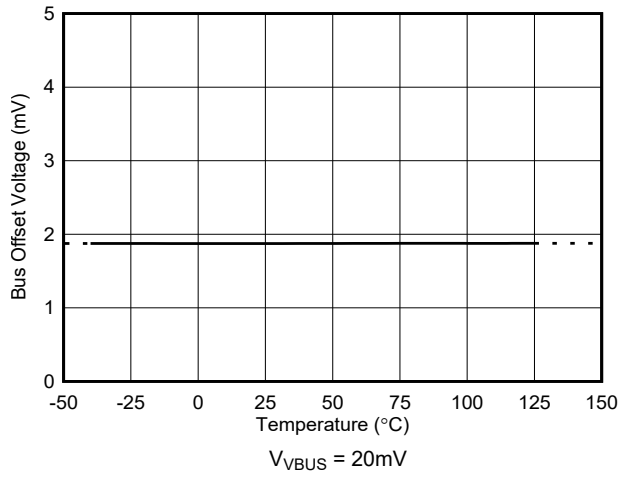


Figure 5-10. Bus Input Offset Voltage vs Temperature

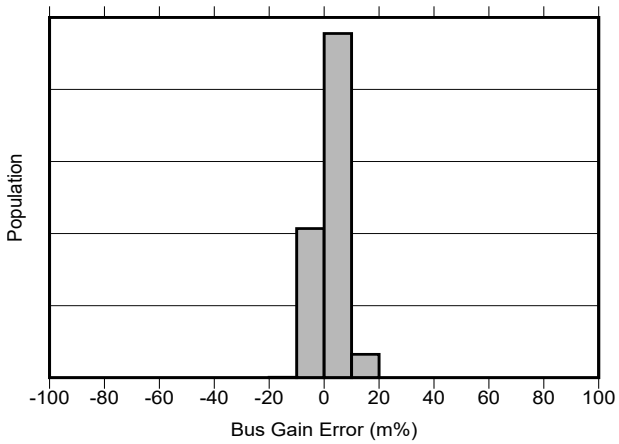


Figure 5-11. Bus Input Gain Error Production Distribution

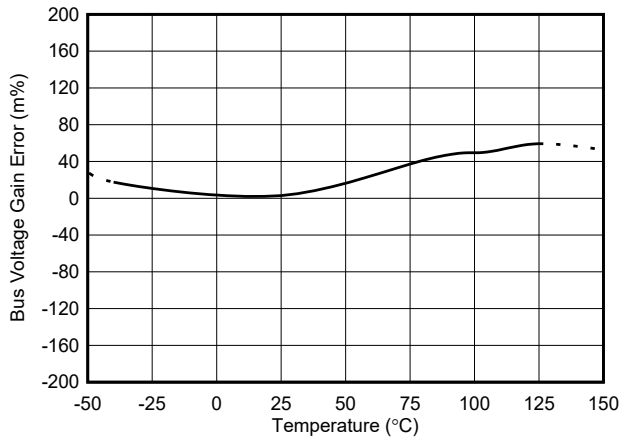


Figure 5-12. Bus Input Gain Error vs Temperature

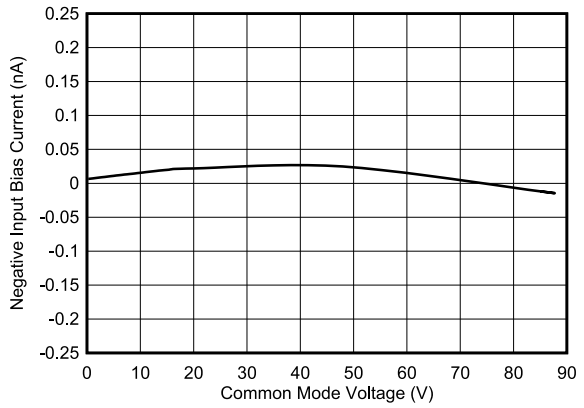


Figure 5-13. Input Bias Current (IB+ or IB–) vs Common-Mode Voltage

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_{VS} = 3.3V, V_{CM} = 12V, V_{SENSE} = 0, and V_{VBUS} = 12V (unless otherwise noted)

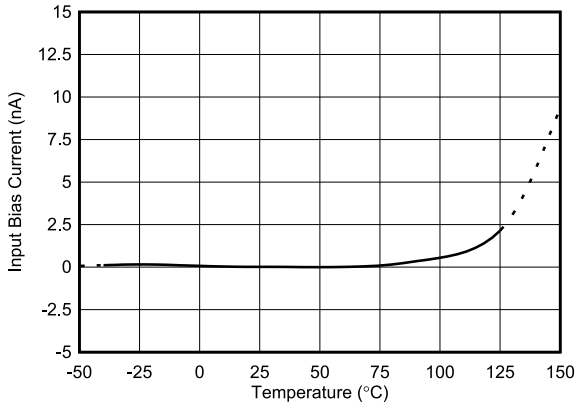


Figure 5-14. Input Bias Current vs Temperature

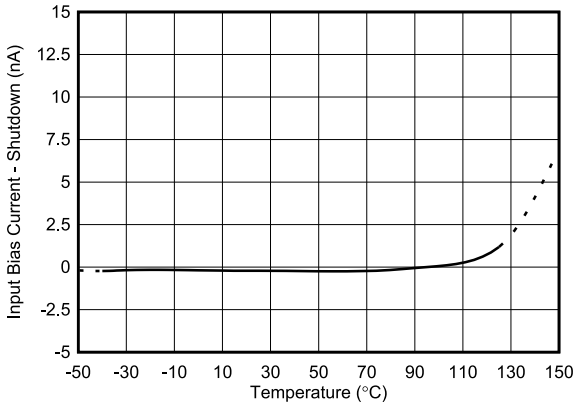


Figure 5-15. Input Bias Current vs Temperature, Shutdown

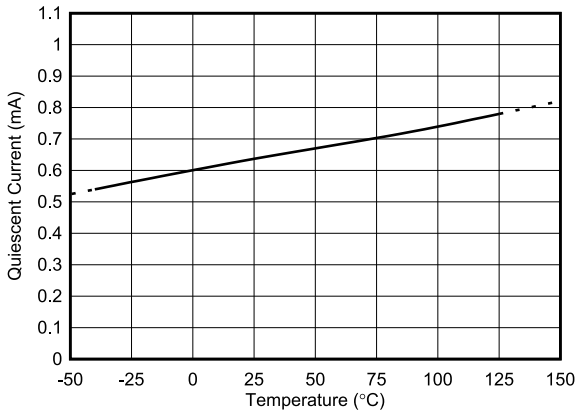


Figure 5-16. Active I_Q vs Temperature

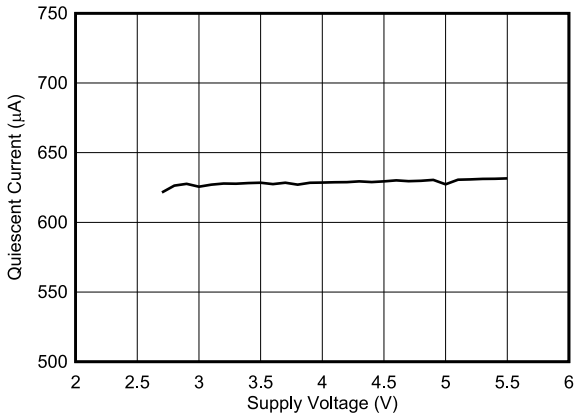


Figure 5-17. Active I_Q vs Supply Voltage

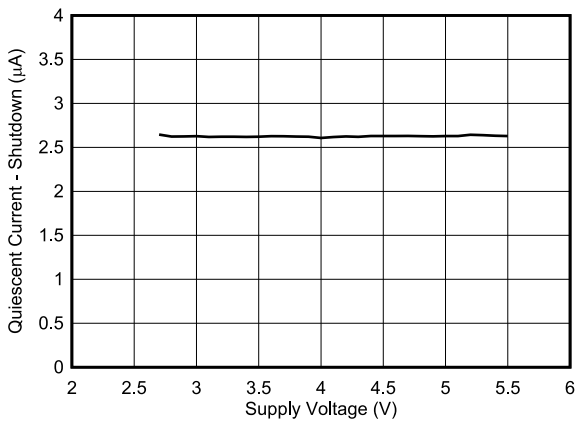


Figure 5-18. Shutdown I_Q vs Supply Voltage

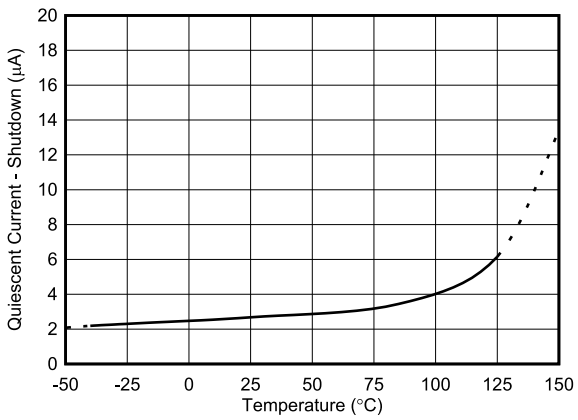


Figure 5-19. Shutdown I_Q vs Temperature

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_{VS} = 3.3V, V_{CM} = 12V, V_{SENSE} = 0, and V_{VBUS} = 12V (unless otherwise noted)

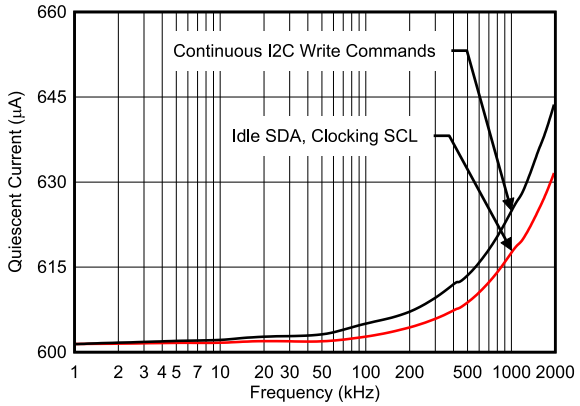


Figure 5-20. Active I_Q vs Clock Frequency

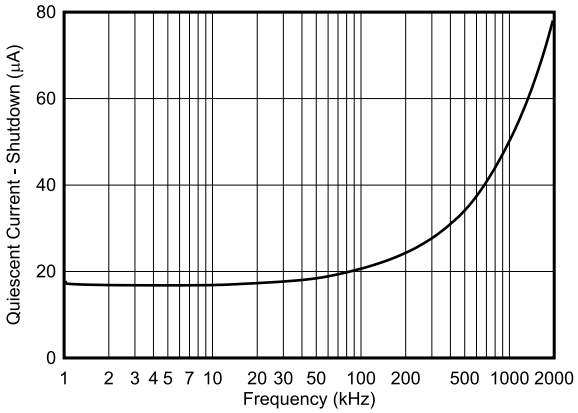


Figure 5-21. Shutdown I_Q vs Clock Frequency

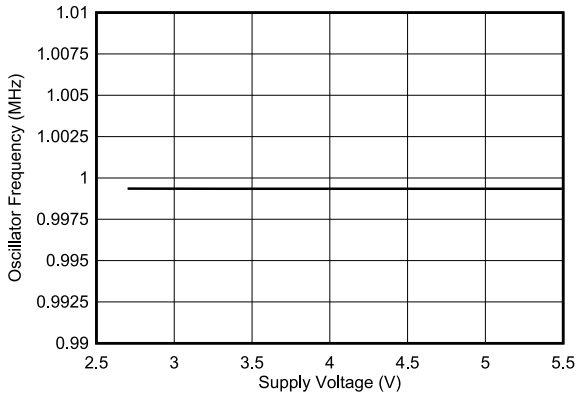


Figure 5-22. Internal Clock Frequency vs Power Supply

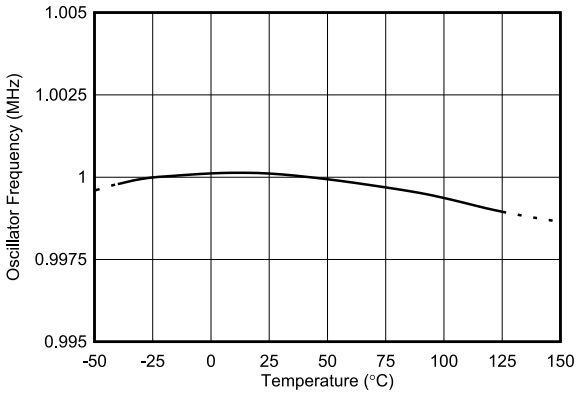


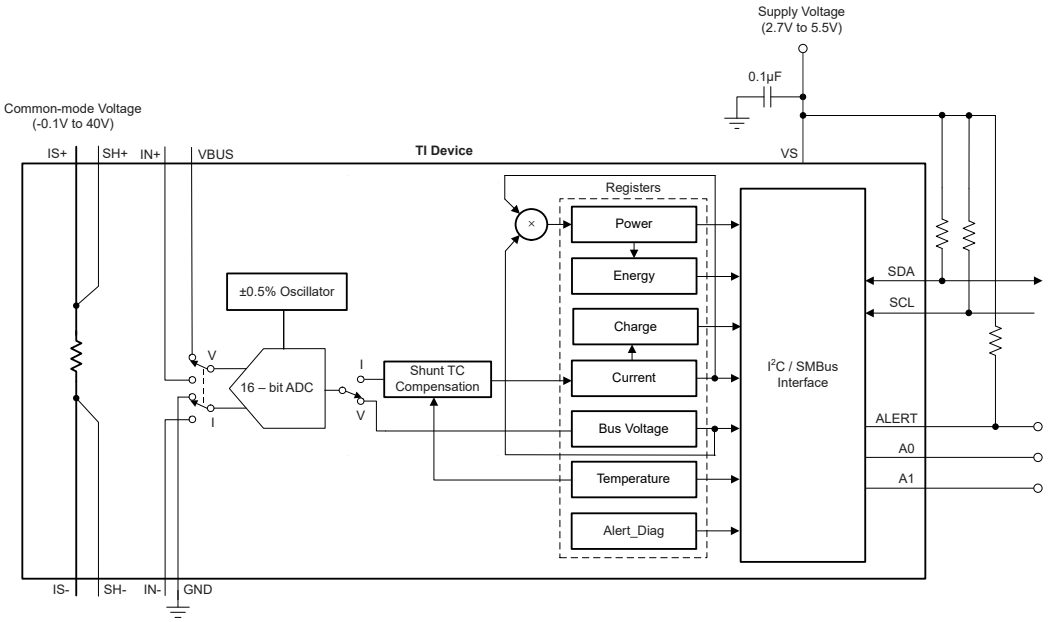
Figure 5-23. Internal Clock Frequency vs Temperature

6 Detailed Description

6.1 Overview

The INA745x device is a digital current sense amplifier with an integrated current sensing element. The device measures current, bus voltage and internal temperature while calculating power, energy and charge necessary for accurate decision making in precisely controlled systems. Programmable registers allow flexible configuration for measurement precision as well as continuous or triggered operation. Detailed register information is found in *Register Maps*.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Integrated Shunt Resistor

The INA745x is a precise, low-drift, digital power monitor that provides accurate measurements over the entire specified ambient temperature range of –40°C to 125°C. The integrated current-sensing resistor is internally compensated to provide measurement stability over temperature, while simplifying printed circuit board (PCB) layout and size constraints.

Access to the on-chip current-sensing resistor is provided by the IS+ and IS- pins. This resistor features internal sense connections that are brought out on the SH+ and SH- pins. Access to the digital power monitor is provided by the IN+ and IN- pins. When the shunt sense connections are connected to the digital power monitor inputs, the sensed voltage is calibrated and temperature compensated to achieve a high level of accuracy. The construction of this resistor does not allow the device to be used as a stand-alone component for accurate current measurement. The INA745x is system-calibrated to verify that the current-sensing resistor and digital power monitor are both precisely matched to one another.

The nominal pin-to-pin resistance from IS+ to IS- is approximately 1mΩ, while the internal resistance seen by the SH+ and SH- pins is nominally 800µΩ. The power dissipation requirements of the system and package are based on the total package resistance between the IS+ and IS– pins.

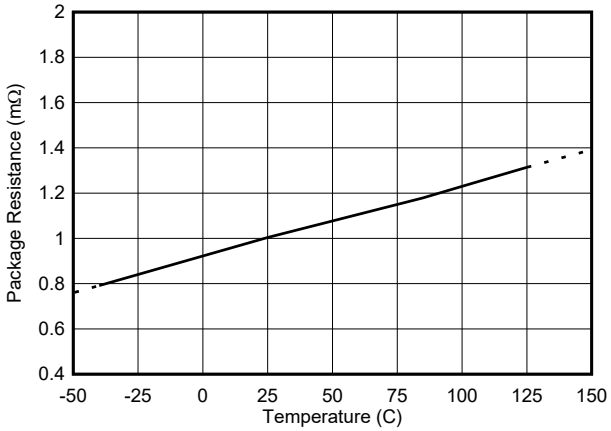


Figure 6-1. IS+ to IS– Package Resistance vs Temperature

The internal compensation of the INA745x corrects for pin-to-pin resistance increases with temperature, achieving low drift over the ambient temperature range.

The INA745x is most accurate when measuring currents around 15A to 20A. As currents increase, the error in the current measurement also increases. Figure 6-2 shows how the gain error of the INA745x varies with the shunt current for all device options.

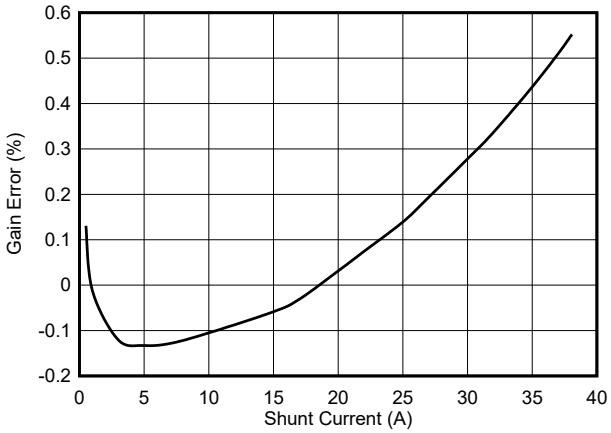


Figure 6-2. Gain Error vs Shunt Current

The shape of this curve varies based on the PCB design. Designs with better thermal performance typically flatten this curve.

The temperature coefficient of the shunt is compensated by sampling the junction temperature and internally applying a correction factor based on this temperature to the reported current measurements. During transient currents, the shunt heats faster than the temperature sensor. This temporary difference in temperatures results in higher values in the reported current until the temperature stabilizes. Figure 6-3 shows the sampled output response during a current step from 0A to 22.5A

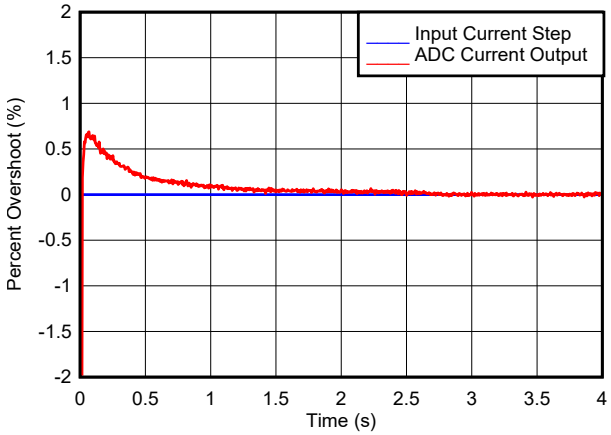


Figure 6-3. Device Current Transient Overshoot

The transient overshoot is similar to what is observed in analog output current sense amplifiers. Understanding that this overshoot occurs when setting an overcurrent alert threshold to avoid false triggers is important.

6.3.2 Safe Operating Area

The heat generated by the device power dissipation limits the maximum current that can be safely handled by the package. The current consumed to power the device is low, therefore the primary source of heating is due to the current flow through the internal shunt resistor. The maximum safe-operating current level shown in Figure 6-4 is set to verify that the heat generated in the package is limited so that the internal junction temperature of the silicon does not exceed 150°C. This data is collected on the INA745x evaluation module (SENS109A).

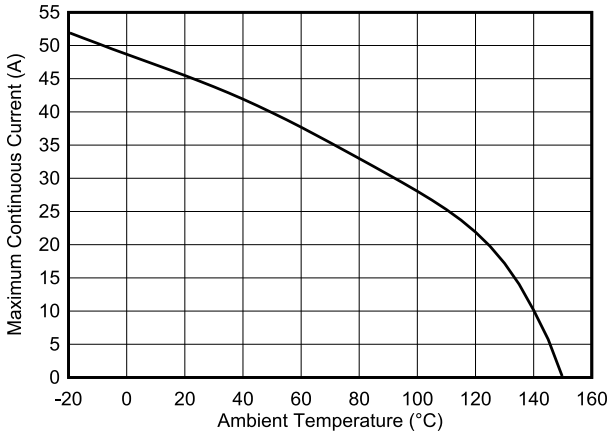


Figure 6-4. Maximum Continuous Shunt Current vs Ambient Temperature

Even though the shunt can withstand currents greater than 35A, the current measurement capability is limited by ADC full scale range of 39.32A. The ADC full scale range is also a function of temperature (see Figure 8-1).

In applications with overcurrent transients, the peak amplitude and duration of the overcurrent event is important to determine the device heating. Figure 6-5 shows the peak pulse current versus pulse duration that the device can withstand before the maximum junction temperature of 150°C is exceeded. The data shown in this curve is collected at T_A =-40°C, 25°C, and 125°C using the INA745x evaluation module (SENS109A).

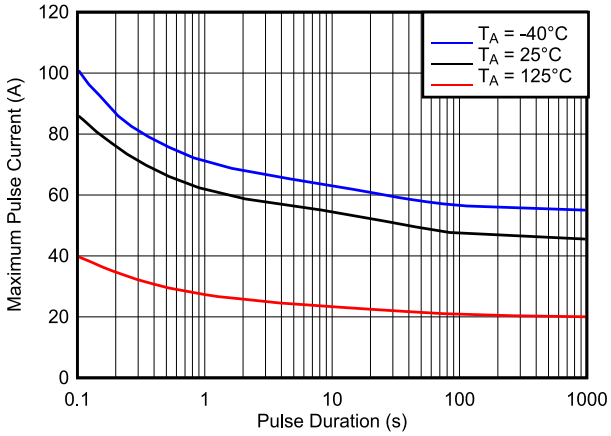


Figure 6-5. Maximum Pulse Current vs Pulse Duration (Single Event)

6.3.3 Versatile Measurement Capability

The INA745x operates off a 2.7V to 5.5V supply but can measure voltage and current on rails as high as 40V. The current is measured by sensing the voltage drop across an internal shunt resistor. The input stage of the INA745x is designed such that the input common-mode voltage can be higher than the device supply voltage, V_S. The common-mode voltage range at the inputs is –0.1V to 40V to support both high-side and low-side current measurements. There are no special considerations for power-supply sequencing because the common-mode input range and device supply voltage are independent of each other; therefore the bus voltage can be present with the supply voltage off (and reciprocally) without damaging the device.

The device also measures the bus supply voltage through the VBUS pin and temperature through the integrated temperature sensor. The current is calculated from the voltage drop across the internal shunt resistor which is sensed by the IN+ and IN– pins, while the bus voltage is measured with respect to device ground. Monitored bus voltages can range from 0V to 40V, while monitored temperatures can range from –40°C to 150°C.

Shunt voltage, bus voltage, and internal temperature measurements are multiplexed internally to a single ADC (see Figure 6-6).

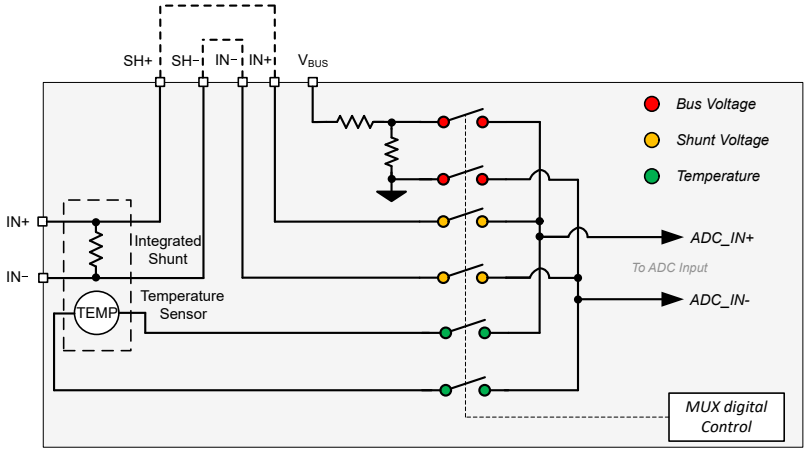


Figure 6-6. High-Voltage Input Multiplexer

6.3.4 Internal Measurement and Calculation Engine

The current and charge are calculated from the voltage drop measured across the internal resistive element, while the power and energy are calculated after a bus voltage measurement. Power and energy are calculated based on the previous current calculation and the latest bus voltage measurement.

The current, bus voltage, and temperature values are immediate results when the number of averages is set to 1 (see Figure 6-7). However, when averaging is used, each ADC measurement is an intermediate result which is stored in the corresponding averaging registers. Following every ADC sample, the newly-calculated values for current, voltage, and temperature are appended to the corresponding averaging registers until the set number of averages is achieved. After all of the samples have been measured, the average current and voltage is determined, the power is calculated, and the results are loaded to the corresponding output registers where the results can then be read.

The energy and charge values are accumulated for each conversion cycle. Therefore the INA745x averaging function is not applied to these.

Calculations for power, charge and energy are performed in the background and do not add to the overall conversion time.

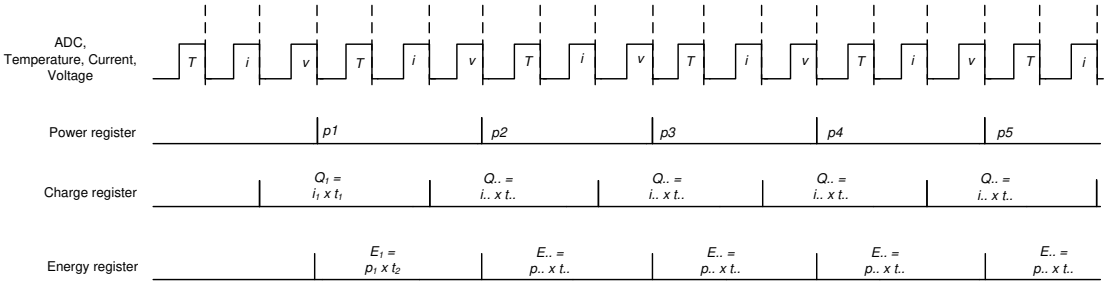


Figure 6-7. Power, Energy and Charge Calculation Scheme

6.3.5 High-Precision Delta-Sigma ADC

The integrated ADC is a high-performance, low-offset, low-drift, delta-sigma ADC designed to support bidirectional current measurement. The measured inputs are selected through the high-voltage input multiplexer to the ADC inputs (see Figure 6-6). The ADC architecture enables lower drift measurement across temperature and consistent offset measurements across common-mode voltage, temperature, and power supply variations. A low-offset ADC is preferred in current sensing applications to provide a near 0V offset voltage that maximizes the useful dynamic range of the system.

The INA745x measures the die temperature, current, and bus voltage. An internal temperature measurement is made before each current measurement. Temperature compensation is then applied to the current measurement to achieve low drift performance. The MODE bits setting in the ADC_CONFIG register permit selecting modes to convert only the current or bus voltage to further allow the user to configure the monitoring function to fit the specific application requirements. After an ADC conversion is complete, the converted values independently update in the corresponding registers where the values can be read through the digital interface at the time of conversion end if no averaging is selected.

The conversion times for shunt voltage, bus voltage, and temperature inputs are set independently from 50µs to 4.12ms depending on the values programmed in the ADC_CONFIG register. The value for current is calculated after both the temperature and shunt voltage measurements are made. The total time to get the current measurement is the sum of the conversion times for these two parameters. Enabled measurement inputs are converted sequentially, which means the total time to convert all inputs depends on the conversion time for each input and the number of inputs enabled. When averaging is used, the intermediate values are subsequently stored in an averaging accumulator, and the conversion sequence repeats until the number of averages is reached. After all of the averaging is complete, the final values are updated in the corresponding registers that can then be read. These values remain in the data output registers until the values are replaced by the next fully completed conversion results. In this case, reading the data output registers does not affect a conversion in progress.

The ADC has two conversion modes—continuous and triggered—set by the MODE bits in the ADC_CONFIG register. In continuous-conversion mode, the ADC continuously converts the input measurements and updates the output registers as described above in an indefinite loop. In triggered-conversion mode, the ADC converts

the input measurements as described above, after which the ADC enters into shutdown mode until another single-shot trigger is generated by writing to the MODE bits. Writing the MODE bits interrupts and restarts triggered or continuous conversions that are in progress. The values from the device can be read at any time because data from the last conversion remains available until the next conversion is complete. The Conversion Ready flag is set after all conversions and averaging are complete.

The Conversion Ready flag (CNVRF) clears under these conditions:

- Writing to the ADC_CONFIG register (except for selecting shutdown mode); or
- Reading the DIAG_ALRT Register

While the INA745x device is used in either one of the conversion modes, a dedicated digital engine is calculating the current, power, charge and energy values in the background as described in *Internal Measurement and Calculation Engine*. In triggered mode, the accumulation registers (ENERGY and CHARGE) are invalid, as the device does not keep track of elapsed time. For applications that require critical measurements in regards to accumulation of time for energy and charge measurements, the device must be configured to use continuous conversion mode, as the accumulated results are continuously updated and can provide true system representation of charge and energy consumption in a system. All of the calculations are performed in the background and do not contribute to conversion time.

For applications that must synchronize with other components in the system, the INA745x conversion can be delayed by programming the CONVDLY bits in the CONFIG register in the range between 0ms (no delay) and 510ms. The resolution in programming the conversion delay is 2ms. The conversion delay is set to 0ms by default. Conversion delay can assist in measurement synchronization when multiple external devices are used for voltage or current monitoring purposes. In applications where time-aligned voltage and current measurements are needed, two devices can be used with the current measurement delayed such that the external voltage and current measurements occur at approximately the same time. Keep in mind that even though the internal time base for the ADC is precise, synchronization is lost over time due to internal and external time base mismatch.

6.3.5.1 Low Latency Digital Filter

The device integrates a low-pass digital filter that performs both decimation and filtering on the ADC output data, which helps with noise reduction. The digital filter is automatically adjusted for the different output data rates and always settles within one conversion cycle. The user has the flexibility to choose different output conversion time periods T_{CT} from 50µs to 4.12ms. With this configuration the first amplitude notch is determined by the selected conversion time period and defined as f_{NOTCH}= 1 / T_{CT}) while in single conversion mode. This means that the filter cut-off frequency scales proportionally with the data output rate. Figure 6-8 shows the filter response when the 1.052ms conversion time period is selected.

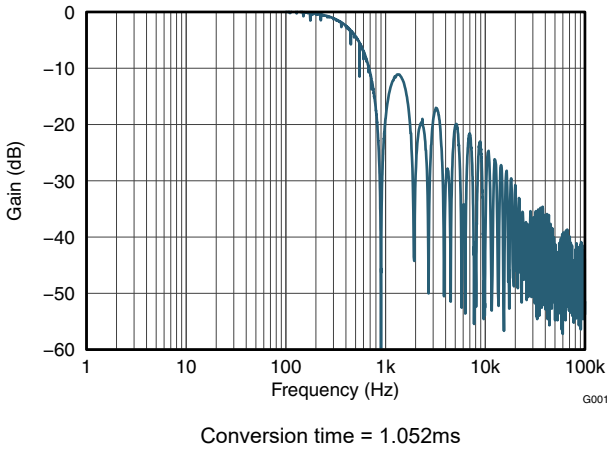


Figure 6-8. ADC Frequency Response

6.3.5.2 Flexible Conversion Times and Averaging

ADC conversion times for bus voltage can be set independently from 50µs to 4.12ms. The total conversion time for current includes an additional conversion time for temperature, and can be varied from 100µs to 8.24ms. The flexibility in conversion time allows for robust operation in a variety of noisy environments. The device also allows for programmable averaging times from a single conversion all the way to an average of 1024 conversions. The amount of averaging selected applies uniformly to all active measurement inputs. The ADC_CONFIG register shown in Table 7-4 provides additional details on the supported conversion times and averaging modes. The INA745x effective resolution of the ADC can be increased by increasing the conversion time and increasing the number of averages. Figure 6-9 and Figure 6-10 shown below illustrate the effect of conversion time and averaging on a constant input signal.

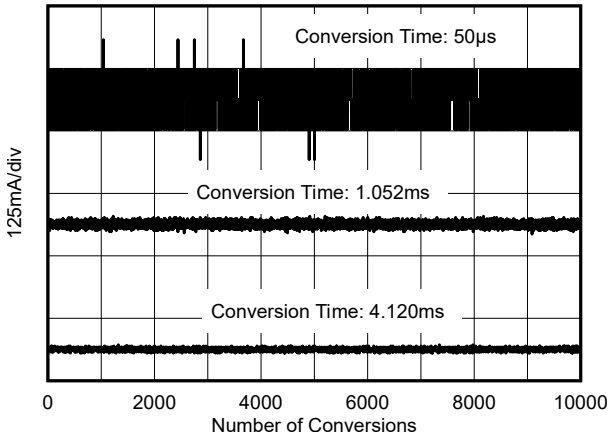


Figure 6-9. Noise vs Conversion Time (Averaging = 1)

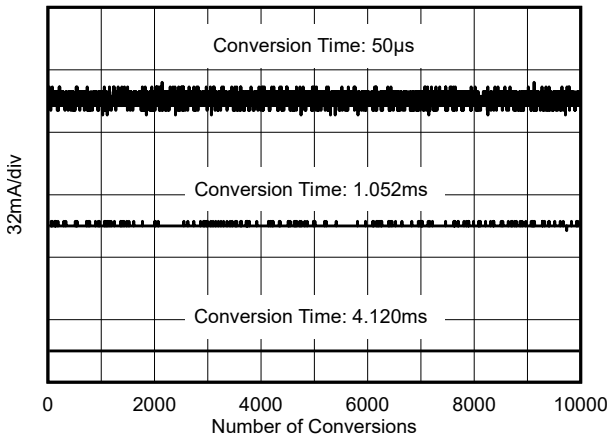


Figure 6-10. Noise vs Conversion Time (Averaging = 128)

Settings for the conversion time and number of conversions averaged impact the effective measurement resolution. For more detailed information on how averaging reduces noise and increases the effective number of bits (ENOB) see *ADC Output Data Rate and Noise Performance*.

6.3.6 Integrated Precision Oscillator

The internal timebase of the device is provided by an internal oscillator that is trimmed to less than 0.5% tolerance at room temperature. The precision oscillator is the timing source for ADC conversions, as well as the time-count used for calculation of energy and charge. The digital filter response varies with conversion time; therefore the precise clock verifies that the filter response and notch frequency consistency across temperature. On power up, the internal oscillator and ADC take roughly 300µs to reach <1% error stability. After the clock stabilizes, the ADC data output is accurate to the electrical specifications provided in *Specifications*.

6.3.7 Multi-Alert Monitoring and Fault Detection

The INA745x includes a multipurpose, open-drain ALERT output pin that can be used to report multiple diagnostics, or to indicate that the ADC conversion is complete. The diagnostics listed in Table 6-1 are constantly monitored and can be reported through the ALERT pin whenever the monitored output value crosses the associated out-of-range threshold.

Table 6-1. ALERT Diagnostics Description

INA745x DIAGNOSTIC	STATUS BIT IN DIAG_ALRT REGISTER (RO)	OUT-OF-RANGE THRESHOLD REGISTER (R/W)	REGISTER DEFAULT VALUE
Current Under-Limit	CURRENTUL	CUL	0x8000 h (2's complement)
Current Over-Limit	CURRENTOL	COL	0x7FFF h (2's complement)
Bus Voltage Over-Limit	BUSOL	BOVL	0x7FFF h (2's complement, positive values only)
Bus Voltage Under-Limit	BUSUL	BUVL	0x0000 h (2's complement, positive values only)
Temperature Over-Limit	TMPOL	TEMP_LIMIT	0xFFFF h (2's complement, positive values only)
Power Over-Limit	POL	PWR_LIMIT	0x7FFF h (2's complement)

A read of the DIAG_ALRT register is used to determine which diagnostic has triggered the ALERT pin. This register, shown in Table 7-11, is also used to monitor other associated diagnostics as well as configure some ALERT pin functions.

- Alert latch enable — In case the ALERT pin is triggered, this function holds the value of the pin even after all diagnostic conditions have cleared. A read of the DIAG_ALRT register resets the status of the ALERT pin. This function is enabled by setting the ALATCH bit.
- Conversion ready enable — Enables the ALERT pin to assert when an ADC conversion has completed and output values are ready to be read through the digital interface. This function is enabled by setting the CNVR bit. The conversion completed events can also be read through the CNVRF bit regardless of the CNVR bit setting.
- Alert comparison on averaged output — Allows the out-of-range threshold value to be compared to the averaged data values produced by the ADC. This function helps to additionally remove noise from the output data when compared to the out-of-range threshold to avoid false alerts due to noise. However, the diagnostic is delayed due to the time needed for averaging. This function is enabled by setting the SLOWALERT bit.
- Alert polarity — Allows the device to invert the active state of the ALERT pin. Note that the ALERT pin is an open-drain output that must be pulled up by a resistor. The ALERT pin is active-low by default and can be configured for active high function using the APOL control bit.

Other diagnostic functions that are not reported by the ALERT pin but are available by reading the DIAG_ALRT register:

- Math overflow — Indicated by the MATHOF bit, reports when an arithmetic operation has caused an internal register overflow.
- Memory status — Indicated by the MEMSTAT bit, monitors the health of the device non-volatile trim memory. This bit always reads '1' when the device is operating properly.
- Energy overflow — Indicated by the ENERGYOF bit, reports when the ENERGY register has reached an overflow state due to data accumulation.
- Charge overflow — Indicated by the CHARGEOF bit, reports when the CHARGE register has reached an overflow state due to data accumulation.

When the ALERT pin is configured to report the ADC conversion complete event, the ALERT pin becomes a multipurpose reporting output. Figure 6-11 shows an example where the device reports ADC conversion complete events while the INA745x device is subject to an overcurrent event, bus undervoltage event, overtemperature event and over power-limit event.

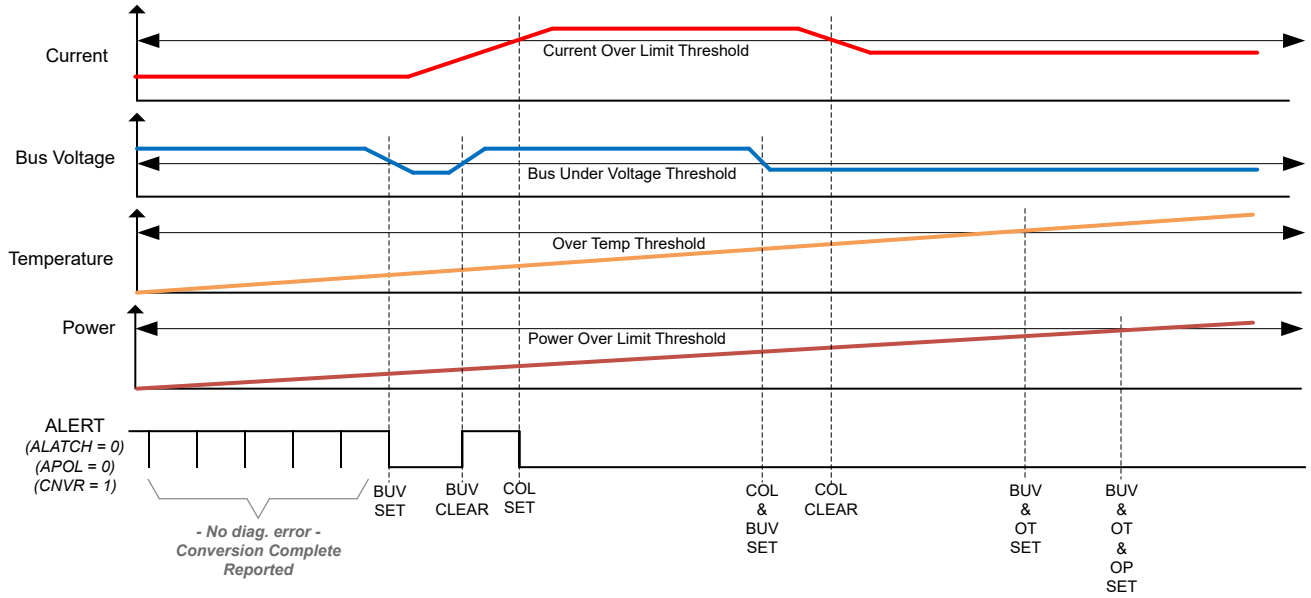


Figure 6-11. Multi-Alert Configuration

6.4 Device Functional Modes

6.4.1 Shutdown Mode

In addition to the two conversion modes (continuous and triggered), the device also has a shutdown mode (selected by the MODE bits in ADC_CONFIG register) that reduces the quiescent current to less than 5µA and turns off current into the device inputs, reducing the impact of supply drain when the device is not being used. The registers of the device can be written to and read from while the device is in shutdown mode. The device remains in shutdown mode until another triggered conversion command or continuous conversion command is received.

The device can be triggered to perform conversions while in shutdown mode. When a conversion is triggered, the ADC starts the conversion. When the conversion completes, the device returns to the shutdown state.

Note that the shutdown current is specified with an inactive communications bus. Active clock and data activity increases the current consumption as a function of the bus frequency.

6.4.2 Power-On Reset

Power-on reset (POR) is asserted when V_S drops below 1.26V (typical) at which all of the registers are reset to the default values. A manual device reset can be initiated by setting the RST bit in the CONFIG register. The default power-up register values are shown in the reset column for each register description. Links to the register descriptions are shown in *Register Maps*.

6.5 Programming

6.5.1 I²C Serial Interface

The INA745x operates only as a target on both the SMBus and I²C interfaces. Connections to the bus are made through the open-drain SDA and SCL lines. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. Although the device integrates spike suppression into the digital I/O lines, proper layout techniques help minimize the amount of coupling into the communication lines. This noise introduction can occur from capacitive coupling signal edges between the two

communication lines themselves or from other switching noise sources present in the system. Routing traces in parallel with ground in between layers on a printed circuit board (PCB) typically reduces the effects of coupling between the communication lines. Shielded communication lines reduce the possibility of unintended noise coupling into the digital I/O lines that can be incorrectly interpreted as start or stop commands.

The INA745x supports the transmission protocol for fast mode (1kHz to 400kHz) and high-speed mode (1kHz to 2.94MHz). All data bytes are transmitted most significant byte first and follow the SMBus 3.0 transfer protocol.

To communicate with the INA745x , the controller must first address targets through a target address byte. The target address byte consists of seven address bits and a direction bit that indicates whether the action is to be a read or write operation.

The device has two address pins, A0 and A1. Table 6-2 lists the pin logic levels for each of the 16 possible addresses. The device samples the state of pins A0 and A1 on every bus communication. Establish the pin state before any activity on the interface occurs. When connecting the SDA pin to either A0 or A1 to set the device address, an additional hold time of 100ns is required on the MSB of the I^2C address to provide correct device addressing.

Table 6-2. Address Pins and Target Addresses

A1	A0	TARGET DEVICE ADDRESS
GND	GND	1000000
GND	VS	1000001
GND	SDA	1000010(1)
GND	SCL	1000011
VS	GND	1000100
VS	VS	1000101
VS	SDA	1000110(1)
VS	SCL	1000111
SDA	GND	1001000(1)
SDA	VS	1001001(1)
SDA	SDA	1001010(1)
SDA	SCL	1001011(1)
SCL	GND	1001100
SCL	VS	1001101
SCL	SDA	1001110(1)
SCL	SCL	1001111

(1) Any address using SDA requires an initial hold time of 100ns on the MSB of the address.

6.5.1.1 Writing to and Reading Through the I^2C Serial Interface

Accessing a specific register on the INA745x is accomplished by writing the appropriate value to the register pointer. Refer to *Register Maps* for a complete list of registers and corresponding addresses. The value for the register pointer (as shown in Figure 6-14) is the first byte transferred after the target address byte with the R/$\overline{W}$ bit low. Every write operation to the device requires a value for the register pointer.

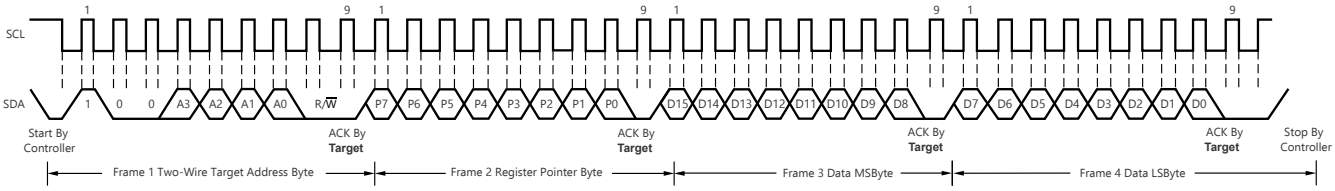
Writing to a register begins with the first byte transmitted by the controller. This byte is the target address, with the R/$\overline{W}$ bit low. The device then acknowledges receipt of a valid address. The next byte transmitted by the controller is the address of the register to be accessed. This register address value updates the register pointer to the desired internal device register. The next two bytes are written to the register addressed by the register pointer. The device acknowledges receipt of each data byte. The controller can terminate data transfer by generating a start or stop condition.

When reading from the device, the last value stored in the register pointer by a write operation determines which register is read during a read operation. To change the register pointer for a read operation, a new value must

be written to the register pointer. This write is accomplished by issuing a target address byte with the R/$\overline{W}$ bit low, followed by the register pointer byte. No additional data are required. The controller then generates a start condition and sends the address byte for the target with the R/$\overline{W}$ bit high to initiate the read command. The next byte is transmitted by the target and is the most significant byte of the register indicated by the register pointer. This byte is followed by an *Acknowledge* from the controller; then the target transmits the least significant byte. The controller can or can not acknowledge receipt of the second data byte. The controller can terminate data transfer by generating a *Not-Acknowledge* after receiving any data byte, or generating a start or stop condition. If repeated reads from the same register are desired, continually sending the register pointer bytes is not necessary; the device retains the register pointer value until the value is changed by the next write operation.

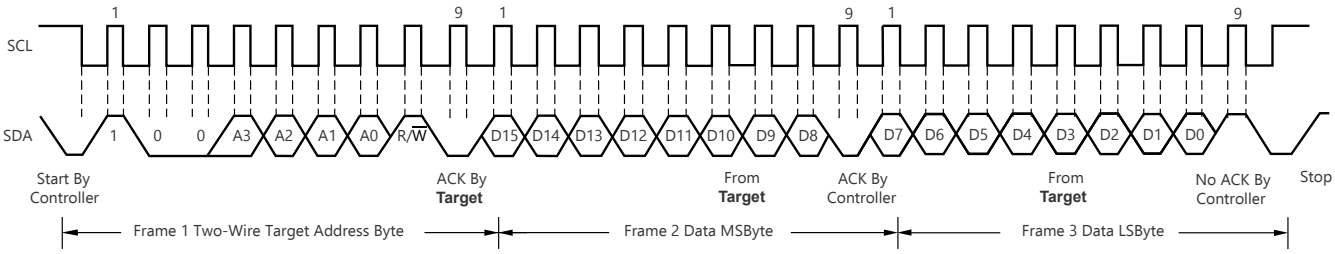
Figure 6-12 shows the write operation timing diagram. Figure 6-13 shows the read operation timing diagram. These diagrams are shown for reading and writing to 16-bit registers.

Register bytes are sent most significant byte (MSB) first, followed by the least significant byte (LSB).



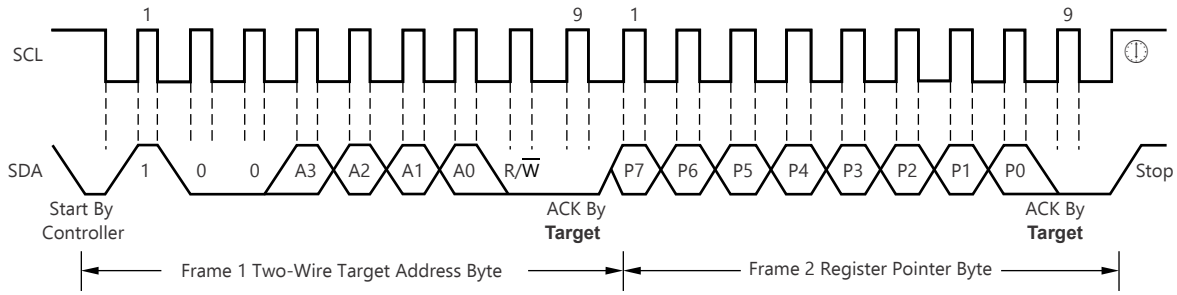
A. The value of the target address byte is determined by the settings of the A0 and A1 pins. Refer to Table 6-2.
B. The device does not support packet error checking (PEC) or perform clock stretching.

Figure 6-12. Timing Diagram for Write Word Format



A. The value of the target address byte is determined by the settings of the A0 and A1 pins. Refer to Table 6-2.
B. Read data is from the last register pointer location. If a new register is desired, the register pointer must be updated. See Figure 6-14.
C. ACK by the controller can also be sent.
D. The device does not support packet error checking (PEC) or perform clock stretching.

Figure 6-13. Timing Diagram for Read Word Format



A. The value of the target address byte is determined by the settings of the A0 and A1 pins. Refer to Table 6-2.

Figure 6-14. Typical Register Pointer Set

6.5.1.2 High-Speed I²C Mode

When the bus is idle, both the SDA and SCL lines are pulled high by the pullup resistors. The controller generates a start condition followed by a valid serial byte containing high-speed (HS) controller code *00001XXX*. This transmission is made in fast (400kHz) or standard (100kHz) (F/S) mode at no more than 400kHz. The INA745x does not acknowledge the HS controller code, but the INA745x does recognize the code and switches the internal filters to support 2.94MHz operation.

The controller then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S mode, except that transmission speeds up to 2.94MHz are allowed. Instead of using a stop condition, use repeated start conditions to maintain the bus in HS-mode. A stop condition ends the HS-mode and switches all the internal filters of the device to support the F/S mode.

6.5.1.3 SMBus Alert Response

The INA745x is designed to respond to the SMBus Alert Response address. The SMBus Alert Response provides a quick fault identification for simple targets. When an Alert occurs, the controller can broadcast the Alert Response target address (0001 100) with the Read/Write bit set high. Following this Alert Response, any target that generates an alert acknowledges the Alert Response and sending the address on the bus.

The Alert Response can activate several different targets simultaneously, similar to the I²C General Call. If more than one target attempts to respond, bus arbitration rules apply. The losing device does not generate an Acknowledge and continues to hold the Alert line low until that device wins arbitration.

7 Register Maps

7.1 INA745x Registers

Table 7-1 lists the INA745x registers. All register locations not listed in Table 7-1 must be considered as reserved locations and the register contents must not be modified.

Table 7-1. INA745x Registers

Address	Acronym	Register Name	Register Size (bits)	Section
0h	CONFIG	Configuration	16	Go
1h	ADC_CONFIG	ADC Configuration	16	Go
5h	VBUS	Bus Voltage Measurement	16	Go
6h	DIETEMP	Temperature Measurement	16	Go
7h	CURRENT	Current Result	16	Go
8h	POWER	Power Result	24	Go
9h	ENERGY	Energy Result	40	Go
Ah	CHARGE	Charge Result	40	Go
Bh	DIAG_ALRT	Diagnostic Flags and Alert	16	Go
Ch	COL	Current Over-Limit Threshold	16	Go
Dh	CUL	Current Under-Limit Threshold	16	Go
Eh	BOVL	Bus Overvoltage Threshold	16	Go
Fh	BUVL	Bus Undervoltage Threshold	16	Go
10h	TEMP_LIMIT	Temperature Over-Limit Threshold	16	Go
11h	PWR_LIMIT	Power Over-Limit Threshold	16	Go
3Eh	MANUFACTURER_ID	Manufacturer ID	16	Go

Complex bit access types are encoded to fit into small table cells. Table 7-2 shows the codes that are used for access types in this section.

Table 7-2. INA745x Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.1.1 Configuration (CONFIG) Register (Address = 0h) [reset = 30h]

The CONFIG register is shown in Table 7-3.

Return to the Summary Table.

Table 7-3. CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RST	R/W	0h	Reset Bit. Setting this bit to '1' generates a system reset that is the same as power-on reset. Resets all registers to default values. 0h = Normal Operation 1h = System Reset sets registers to default values This bit self-clears.
14	RSTACC	R/W	0h	Resets the contents of accumulation registers ENERGY and CHARGE to 0 0h = Normal Operation 1h = Clears registers to default values for ENERGY and CHARGE registers
13-6	CONVDLY	R/W	0h	Sets the Delay for initial ADC conversion in steps of 2ms. 0h = 0s 1h = 2ms FFh = 510ms
5	RESERVED	R	1h	Reserved. Always reads 1.
4	RESERVED	R	1h	Reserved. Always reads 1.
3-0	RESERVED	R	0h	Reserved. Always reads 0.

7.1.2 ADC Configuration (ADC_CONFIG) Register (Address = 1h) [reset = FB68h]

The ADC_CONFIG register is shown in Table 7-4.

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Table 7-4. ADC_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	MODE	R/W	Fh	The user can set the MODE bits for continuous or triggered mode on bus voltage, shunt voltage or temperature measurement. 0h = Shutdown 1h = Triggered bus voltage, single shot 2h = Reserved 3h = Reserved 4h = Triggered temperature, single shot 5h = Triggered temperature and bus voltage, single shot 6h = Triggered temperature and current, single shot 7h = Triggered temperature, current and bus voltage, single shot 8h = Shutdown 9h = Continuous bus voltage only Ah = Reserved Bh = Reserved Ch = Continuous temperature only Dh = Continuous bus voltage and temperature Eh = Continuous temperature and current Fh = Continuous temperature, current, and bus voltage

Table 7-4. ADC_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-9	VBUSCT	R/W	5h	Sets the conversion time of the bus voltage measurement. 0h = 50µs 1h = 84µs 2h = 150µs 3h = 280µs 4h = 540µs 5h = 1052µs 6h = 2074µs 7h = 4120µs
8-6	VSENCT	R/W	5h	Sets the conversion time of the shunt resistor voltage. Works in conjunction with the temperature conversion time. Total conversion time for a current measurement is the sum of VSENCT and TCT selections. 0h = 50µs 1h = 84µs 2h = 150µs 3h = 280µs 4h = 540µs 5h = 1052µs 6h = 2074µs 7h = 4120µs
5-3	TCT	R/W	5h	Sets the conversion time of the temperature measurement. Works in conjunction with the shunt voltage conversion time for current measurements. Total conversion time for a current measurement is the sum of VSENCT and TCT selections. 0h = 50µs 1h = 84µs 2h = 150µs 3h = 280µs 4h = 540µs 5h = 1052µs 6h = 2074µs 7h = 4120µs
2-0	AVG	R/W	0h	Selects ADC sample averaging count. The averaging setting applies to all active inputs. When >0h, the output registers are updated after the averaging has completed. 0h = 1 1h = 4 2h = 16 3h = 64 4h = 128 5h = 256 6h = 512 7h = 1024

7.1.3 Bus Voltage Measurement (VBUS) Register (Address = 5h) [reset = 0h]

The VBUS register is shown in Table 7-5.

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Table 7-5. VBUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	VBUS	R	0h	Bus voltage output. Two's complement value, however always positive. Conversion factor: 3.125mV/LSB

7.1.4 Temperature Measurement (DIETEMP) Register (Address = 6h) [reset = 0h]

The DIETEMP register is shown in Table 7-6.

Return to the Summary Table.

Table 7-6. DIETEMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	DIETEMP	R	0h	Internal die temperature measurement. Two's complement value. Conversion factor: 125m°C/LSB
3-0	RESERVED	R	0h	Reserved. Always reads 0.

7.1.5 Current Result (CURRENT) Register (Address = 7h) [reset = 0h]

The CURRENT register is shown in Table 7-7.

Return to the Summary Table.

Table 7-7. CURRENT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CURRENT	R	0h	Calculated current output in Amperes. Two's complement value. Conversion factor: 1.2mA/LSB.

7.1.6 Power Result (POWER) Register (Address = 8h) [reset = 0h]

The POWER register is shown in Table 7-8.

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Table 7-8. POWER Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	POWER	R	0h	Calculated power output. Output value in Watts. Unsigned representation. Positive value. Conversion factor: 240µW/LSB.

7.1.7 Energy Result (ENERGY) Register (Address = 9h) [reset = 0h]

The ENERGY register is shown in Table 7-9.

Return to the Summary Table.

Table 7-9. ENERGY Register Field Descriptions

Bit	Field	Type	Reset	Description
39-0	ENERGY	R	0h	Calculated energy output. Output value is in Joules.Unsigned representation. Positive value. Conversion factor: 3.84mJ/LSB.

7.1.8 Charge Result (CHARGE) Register (Address = Ah) [reset = 0h]

The CHARGE register is shown in Table 7-10.

Return to the Summary Table.

Table 7-10. CHARGE Register Field Descriptions

Bit	Field	Type	Reset	Description
39-0	CHARGE	R	0h	Calculated charge output. Output value is in Coulombs.Two's complement value. Conversion factor: 75µC//LSB.

7.1.9 Diagnostic Flags and Alert (DIAG_ALRT) Register (Address = Bh) [reset = 0001h]

The DIAG_ALRT register is shown in Table 7-11.

Return to the Summary Table.

Table 7-11. DIAG_ALRT Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ALATCH	R/W	0h	When the Alert Latch Enable bit is set to Transparent mode, the Alert pin and Flag bit reset to the idle state when the fault has been cleared. When the Alert Latch Enable bit is set to Latch mode, the Alert pin and Alert Flag bit remain active following a fault until the DIAG_ALRT Register has been read. 0h = Transparent 1h = Latched
14	CNVR	R/W	0h	Setting this bit high configures the Alert pin to be asserted when the Conversion Ready Flag (bit 1) is asserted, indicating that a conversion cycle has completed. 0h = Disables conversion ready flag on ALERT pin 1h = Enables conversion ready flag on ALERT pin
13	SLOWALERT	R/W	0h	When enabled, ALERT function is asserted on the completed averaged value. This gives the flexibility to delay the ALERT until after the averaged value. 0h = ALERT comparison on non-averaged (ADC) value 1h = ALERT comparison on averaged value
12	APOL	R/W	0h	Alert Polarity bit sets the Alert pin polarity. 0h = Normal (active-low, open-drain) 1h = Inverted (active-high, open-drain)
11	ENERGYOF	R	0h	This bit indicates the health of the ENERGY register. If the 40-bit ENERGY register has overflowed this bit is set to 1. 0h = Normal 1h = Overflow Clears by setting the RSTACC field in the Configuration register.
10	CHARGEOF	R	0h	This bit indicates the health of the CHARGE register. If the 40-bit CHARGE register has overflowed this bit is set to 1. 0h = Normal 1h = Overflow Clears by setting the RSTACC field in the Configuration register.

Table 7-11. DIAG_ALRT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	MATHOF	R	0h	This bit is set to 1 if an arithmetic operation resulted in an overflow error. This bit indicates that current and power data can be invalid. 0h = Normal 1h = Overflow Must be manually cleared by triggering another conversion or by clearing the accumulators with the RSTACC bit.
8	RESERVED	R	0h	Reserved. Always read 0.
7	TMPOL	R	0h	This bit is set to 1 if the temperature measurement exceeds the threshold limit in the temperature over-limit register. 0h = Normal 1h = Overtemperature Event When ALATCH =1 this bit is cleared by reading or writing to this register.
6	CURRENTOL	R	0h	This bit is set to 1 if the current measurement exceeds the threshold limit in the current over-limit register. 0h = Normal 1h = Overcurrent Event When ALATCH =1 this bit is cleared by reading or writing to this register.
5	CURRENTUL	R	0h	This bit is set to 1 if the current measurement falls below the threshold limit in the current under-limit register. 0h = Normal 1h = Undercurrent Event When ALATCH =1 this bit is cleared by reading or writing to this register.
4	BUSOL	R	0h	This bit is set to 1 if the bus voltage measurement exceeds the threshold limit in the bus over-limit register. 0h = Normal 1h = Bus Over-Limit Event When ALATCH =1 this bit is cleared by reading or writing to this register.
3	BUSUL	R	0h	This bit is set to 1 if the bus voltage measurement falls below the threshold limit in the bus under-limit register. 0h = Normal 1h = Bus Under-Limit Event When ALATCH =1 this bit is cleared by reading or writing to this register.
2	POL	R	0h	This bit is set to 1 if the power measurement exceeds the threshold limit in the power limit register. 0h = Normal 1h = Power Over-Limit Event When ALATCH =1 this bit is cleared by reading or writing to this register.
1	CNVRF	R	0h	This bit is set to 1 if the conversion is completed. 0h = Normal 1h = Conversion is complete When ALATCH =1 this bit is cleared by reading or writing to this register or starting a new triggered conversion.
0	MEMSTAT	R	1h	This bit is set to 0 if a checksum error is detected in the device trim memory space. 0h = Memory Checksum Error 1h = Normal Operation

7.1.10 Current Over-Limit Threshold (COL) Register (Address = Ch) [reset = 7FFFh]

If negative values are entered in this register, then a current measurement of 0A trips this alarm. When using negative values for the undercurrent and overcurrent thresholds be aware that the overcurrent threshold must be set to the larger (that is, less negative) of the two values. The COL register is shown in Table 7-12.

Return to the Summary Table.

Table 7-12. COL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	COL	R/W	7FFFh	Sets the threshold for comparison of the value to detect over current condition (overcurrent protection). Two's complement value. Conversion factor: 1.2mA/LSB

7.1.11 Current Under-Limit Threshold (CUL) Register (Address = Dh) [reset = 8000h]

The CUL register is shown in Table 7-13.

Return to the Summary Table.

Table 7-13. CUL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CUL	R/W	8000h	Sets the threshold for comparison of the value to detect undercurrent condition. Two's complement value. Conversion factor: 1.2mA/LSB

7.1.12 Bus Overvoltage Threshold (BOVL) Register (Address = Eh) [reset = 7FFFh]

The BOVL register is shown in Table 7-14.

Return to the Summary Table.

Table 7-14. BOVL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	0h	Reserved. Always reads 0.
14-0	BOVL	R/W	7FFFh	Sets the threshold for comparison of the value to detect Bus Overvoltage (overvoltage protection). Unsigned representation, positive value only. Conversion factor: 3.125mV/LSB.

7.1.13 Bus Undervoltage Threshold (BUVL) Register (Address = Fh) [reset = 0h]

The BUVL register is shown in Table 7-15.

Return to the Summary Table.

Table 7-15. BUVL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	0h	Reserved. Always reads 0.
14-0	BUVL	R/W	0h	Sets the threshold for comparison of the value to detect Bus Undervoltage (undervoltage protection). Unsigned representation, positive value only. Conversion factor: 3.125mV/LSB.

7.1.14 Temperature Over-Limit Threshold (TEMP_LIMIT) Register (Address = 10h) [reset = 7FFFh]

The TEMP_LIMIT register is shown in Table 7-16.

Return to the Summary Table.

Table 7-16. TEMP_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	TOL	R/W	7FFh	Sets the threshold for comparison of the value to detect over temperature measurements. Two's complement value. The value entered in this field compares directly against the value from the DIETEMP register to determine if an overtemperature condition exists. Conversion factor: 125m°C/LSB.
3-0	Reserved	R	0	Reserved, always reads 0

7.1.15 Power Over-Limit Threshold (PWR_LIMIT) Register (Address = 11h) [reset = FFFFh]

The PWR_LIMIT register is shown in Table 7-17.

Return to the Summary Table.

Table 7-17. PWR_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	POL	R/W	FFFFh	Sets the threshold for comparison of the value to detect power over-limit measurements. Unsigned representation, positive value only. The value entered in this field compares directly against the value from the POWER register to determine if an over-power condition exists. Conversion factor: 256 × Power LSB or 61.44mW/LSB

7.1.16 Manufacturer ID (MANUFACTURER_ID) Register (Address = 3Eh) [reset = 5449h]

The MANUFACTURER_ID register is shown in Table 7-18.

Return to the Summary Table.

Table 7-18. MANUFACTURER_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MANFID	R	5449h	Reads back TI in ASCII.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Device Measurement Range and Resolution

The INA745x has a full scale ADC range for current measurements of ±39.32A. However, the maximum value that can be measured is limited by the operating junction temperature (see Figure 8-1).

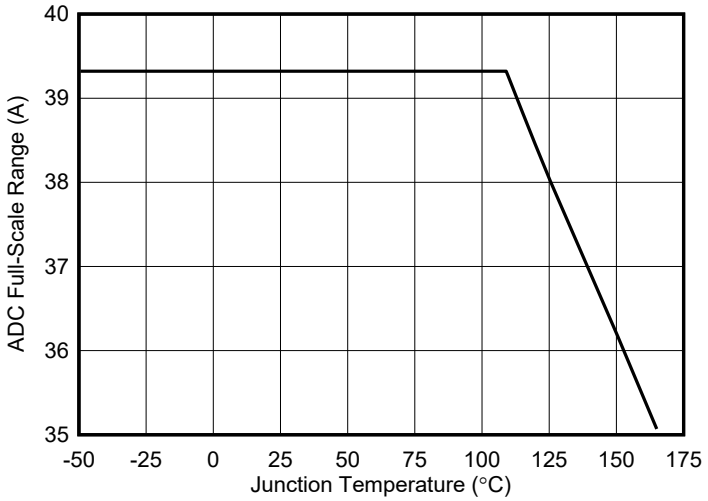


Figure 8-1. Maximum ADC Current Reading vs Junction Temperature (Typical Characteristic)

Table 8-1 shows the full scale value for shunt, bus, and temperature measurements, along with the associated step size.

Table 8-1. Register Full Scale Values and Resolution

PARAMETER	REGISTER ADDRESS	SIZE	FULL SCALE VALUE	RESOLUTION
Current	7h	16 bit, signed	±39.32A	1.2mA/LSB
Bus voltage	5h	16 bit, signed, always positive	0V to 40V	3.125mV/LSB
Die Temperature	6h	12 bit, signed	–40°C to 150°C	125m°C/LSB
Power	8h	24 bit, unsigned	4026.53W	240µW/LSB
Energy	9h	40 bit, unsigned	4222.125MJ	3.840mJ/LSB
Charge	Ah	40 bit, unsigned	82.463MC	75µC/LSB

The internal die temperature sensor register range extends from –256°C to 256°C but is limited by the junction temperature range of –40°C to 150°C. Likewise, the bus voltage measurement range extends up to 102.4V but is limited by silicon to 40V.

Current, bus voltage, temperature, power, energy and charge measurements can be read through the corresponding address registers. Values are calculated by multiplying the returned value by the corresponding LSB size.

Signed values are represented in 2's complement format.

Upon overflow, the ENERGY register rolls over and starts from zero. This register value can also be reset at any time by setting the RSTACC bit in the CONFIG register.

An overflow event in the CHARGE register is indicated by the CHARGEOF bit. If an overflow condition occurs, the CHARGE register needs to be manually reset by setting the RSTACC bit in the CONFIG register.

For a design example using these equations refer to *Detailed Design Procedure*.

8.1.2 ADC Output Data Rate and Noise Performance

The INA745x noise performance and effective resolution depend on the ADC conversion time. The device also supports digital averaging which can further help decrease digital noise. The flexibility of the device to select ADC conversion time and data averaging offers increased signal-to-noise ratio and achieves the highest dynamic range with lowest offset. The profile of the noise at lower signals levels is dominated by the system noise that is comprised mainly of 1/f noise or white noise. The INA745x effective resolution of the ADC can be increased by increasing the conversion time and increasing the number of averages.

Table 8-2 summarizes the output data rate conversion settings supported by the device. The fastest conversion setting is 50µs. Typical noise-free resolution is represented as Effective Number of Bits (ENOB) based on device measured data. The ENOB is calculated based on noise peak-to-peak values, which verifies that full noise distribution is taken into consideration.

Table 8-2. INA745x Noise Performance

ADC CONVERSION TIME PERIOD [µs]	OUTPUT SAMPLE AVERAGING [SAMPLES]	OUTPUT SAMPLE PERIOD [ms]	NOISE-FREE ENOB CURRENT MEASUREMENT
50	1	0.05	9.9
84		0.084	10.3
150		0.15	10.9
280		0.28	11.8
540		0.54	12.0
1052		1.052	12.5
2074		2.074	13.1
4120		4.12	13.7
50	4	0.2	11.1
84		0.336	11.4
150		0.6	12.1
280		1.12	12.8
540		2.16	13.4
1052		4.208	13.7
2074		8.296	14.7
4120		16.48	14.7
50	16	0.8	12.2
84		1.344	13.1
150		2.4	13.4
280		4.48	13.7
540		8.64	14.1
1052		16.832	14.7
2074		33.184	15.7
4120		65.92	15.7

Table 8-2. INA745x Noise Performance (continued)

ADC CONVERSION TIME PERIOD [µs]	OUTPUT SAMPLE AVERAGING [SAMPLES]	OUTPUT SAMPLE PERIOD [ms]	NOISE-FREE ENOB CURRENT MEASUREMENT
50	64	3.2	13.1
84		5.376	13.7
150		9.6	14.1
280		17.92	14.7
540		34.56	15.7
1052		67.328	15.7
2074		132.736	15.7
4120		263.68	15.7
50	128	6.4	13.4
84		10.752	14.1
150		19.2	14.7
280		35.84	15.7
540		69.12	15.7
1052		134.656	15.7
2074		265.472	15.7
4120		527.36	15.7
50	256	12.8	14.1
84		21.504	14.7
150		38.4	15.7
280		71.68	15.7
540		138.24	15.7
1052		269.312	15.7
2074		530.944	15.7
4120		1054.72	15.7
50	512	25.6	14.1
84		43	15.7
150		76.8	15.7
280		143.36	15.7
540		276.48	15.7
1052		538.624	15.7
2074		1061.888	15.7
4120		2109.44	16.0
50	1024	51.2	15.7
84		86.016	15.7
150		153.6	15.7
280		286.72	15.7
540		552.96	15.7
1052		1077.248	15.7
2074		2123.776	16.0
4120		4218.88	16.0

8.2 Typical Application

The low offset voltage and low input bias current of the INA745x allow accurate monitoring of a wide range of currents. Figure 8-2 shows a circuit example for monitoring currents in a high-side configuration.

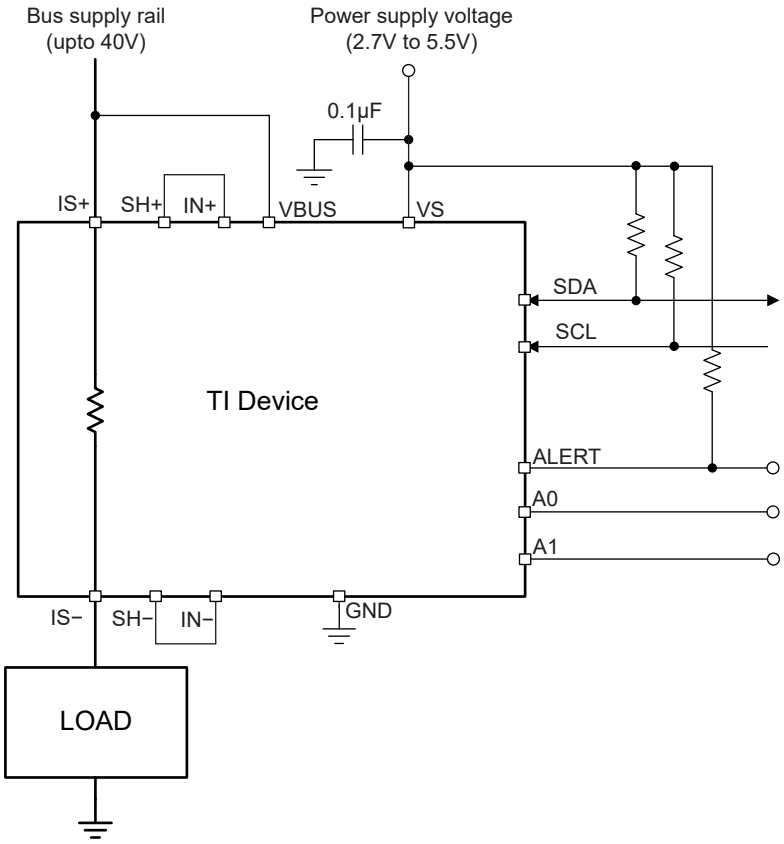


Figure 8-2. INA745x High-Side Sensing Application Diagram

8.2.1 Design Requirements

The design requirements for the circuit shown in Figure 8-2 are listed in Table 8-3.

Table 8-3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Power-supply voltage (V_S)	5V
Bus supply rail (V_{CM})	12V
Bus supply rail overvoltage fault threshold	16V
Average Current	18A
Overcurrent fault threshold (I_{MAX})	21A
Temperature	85°C
Charge Accumulation Period	15 minutes

8.2.2 Detailed Design Procedure

8.2.2.1 Configure the Device

The first step to program the INA745x is to properly set the device and ADC configuration registers. On initial power up, the CONFIG and ADC_CONFIG registers are set to the reset values as shown in Table 7-3 and Table 7-4. In this default power-on state the device is set with the ADC continuously converting the temperature, current, and bus voltage. If the default power-up conditions do not meet the design requirements, these registers must be set properly after each V_S power cycle event.

8.2.2.2 Set Desired Fault Thresholds

Fault thresholds are set by programming the desired trip threshold into the corresponding fault register. Table 6-1 lists the supported fault registers.

An overcurrent threshold is set by programming the Current Over-Limit Threshold register (COL). Divide the overcurrent limit value by the current LSB size to calculate the value needed to program the register.

In this example, the desired overcurrent limit threshold is 21A. The Current LSB size is 1.2mA/LSB, therefore the value that must be programmed into Current Over-Limit (COL) register is 21A / 1.2mA/LSB = 17500d or 445Ch.

An overvoltage fault threshold on the bus voltage is set by programming the bus overvoltage limit register (BOVL). In this example, the desired over voltage threshold is 16V. Divide the target threshold voltage by the correct LSB value to calculate the value needed to program the register. For this example, the target value for the BOVL register is 16V / 3.125mV = 5120d (1400h).

When setting the power over-limit value, the LSB size used to calculate the value needed in the limit registers is 256 times greater than the power LSB. This is because the power register is 24 bits in length while the power fault limit register is 16 bits.

Values stored in the alert limit registers are set to the default values after V_S power cycle events and must be reprogrammed each time power is applied.

8.2.2.3 Calculate Returned Values

Multiply the returned value by the LSB value to calculate the parametric values. Table 8-4 below shows the returned values for this application example assuming the design requirements shown in Table 8-3.

Table 8-4. Calculating Returned Values

PARAMETER	RETURNED VALUE	LSB VALUE	CALCULATED VALUE
Current (A)	15000d, 3A98h	1.2mA/LSB	18A
Bus voltage (V)	3840d, F00h	3.125mV/LSB	12V
Power (W)	900000d, DBBA0h	240µW/LSB	216W
Energy (J)	50625000d, 30479E8h	3.84mJ/LSB	194400J
Charge (C)	216000000d, CDFE600 h	75µC/LSB	16200C
Temperature (°C)	680d, 2A8h	125m°C/LSB	85°C

Current, Bus Voltage (positive only), Charge, and Temperature return values in 2's complement format. In a 2's complement format, a 1 in the most significant bit of the returned value represents a negative value in binary. These values can be converted to decimal by first iwnverting all the bits and adding 1 to obtain the unsigned binary value. This value must then be converted to decimal with the negative sign applied.

8.2.3 Application Curves

Figure 8-3 and Figure 8-4 show the ALERT pin response to an overcurrent fault with a conversion time of 50µs for the temperature, shunt voltage, and bus voltage measurements with averaging set to 1. This configuration results in a total conversion time of 150µs for all three measurements. For these scope shots, persistence is enabled on the ALERT channel to show the variation in the alert response for many sequential fault events. The alert response time can change depending on the value of the current before fault occurs as well as the how much the fault condition exceeds the programmed fault threshold. Figure 8-3 shows the response time for an overcurrent fault when the fault condition greatly exceeds the programmed threshold, while Figure 8-4 shows the overcurrent response time when the fault slightly exceeds the programmed threshold. Variation in the alert response exists because the external fault event is not synchronized to the internal ADC conversion start. Also the ADC is constantly sampling to get a result, so the response time for fault events starting from zero is slower than fault events starting from values near the set fault threshold. In applications where the alert timing is critical for overcurrent events, the worst-case alert response is equal to $2 \times t_{conv\_current} + t_{conv\_temp} + t_{conv\_voltage} + 25\mu s$. An additional 25µs is added to allow for background math calculations. This equation does not account for the 1% oscillator tolerance and is only valid for cases where the overcurrent signal is greater than the conversion threshold and noise. The measurement noise is a function of the conversion time. See Section 6.3.5.2 and Section 8.1.2 for additional information.

Figure 8-4 shows a slightly longer worst case alert response because the alert threshold is within the noise band of the device measurement and signal.

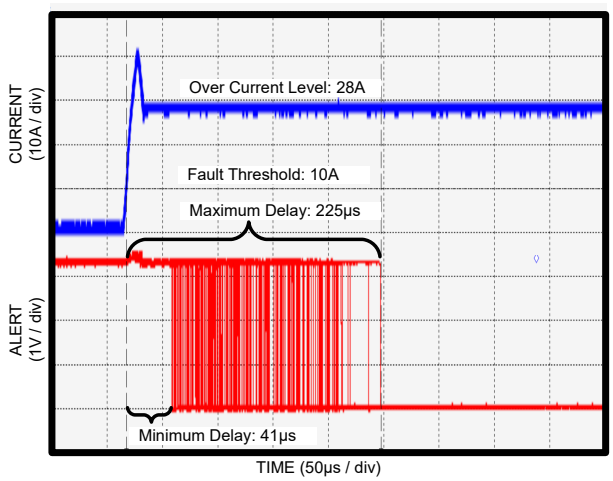


Figure 8-3. Alert Response Time (Sampled Values Significantly Above Threshold)

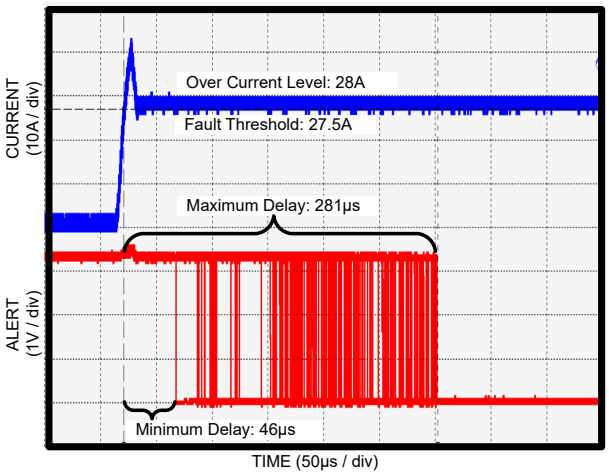


Figure 8-4. Alert Response Time (Sampled Values Slightly Above Threshold)

8.3 Power Supply Recommendations

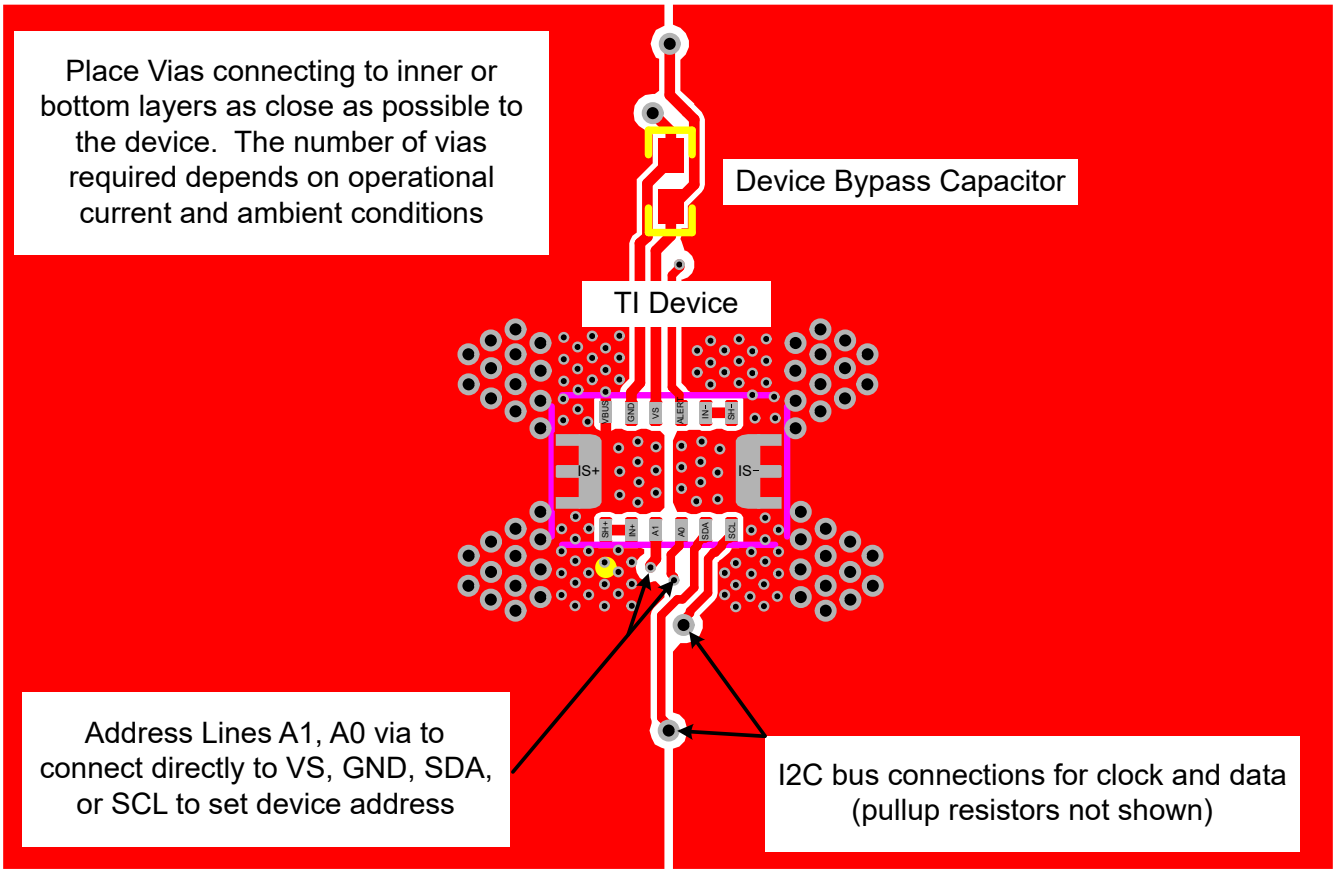
The input circuitry of the device can accurately measure signals on common-mode voltages beyond the power-supply voltage, V_S. For example, the voltage applied to the V_S power supply terminal can be 5V, whereas the load power-supply voltage being monitored (the common-mode voltage) can be as high as 40V. Note that the device can also withstand the full 0V to 40V range at the input terminals, regardless of whether the device has power applied or not. Avoid applications where the GND pin is disconnected while device is actively powered.

8.4 Layout

8.4.1 Layout Guidelines

Place the required power-supply bypass capacitors as close as possible to the supply and ground terminals of the device. A typical value for this supply bypass capacitor is 0.1µF. Applications with noisy or high-impedance power supplies can require additional decoupling capacitors to reject power-supply noise.

8.4.2 Layout Example



1. All vias close to the pin pads must be tented.
2. All vias are either 8 mil/18 mil or 15 mil/25 mil with a 5 mill annular ring.
3. The distance between the IS+ and IS– power pours is 8 mil.
4. See EVM User's Guide for more specific layout recommendations and layers.

Figure 8-5. INA745x Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December 2023) to Revision B (August 2025)	Page
• Changed the data sheet status from Production Mixed to Production Data	1
• Reworded Low Latency Digital Filter section and corrected F_{NOTCH} equation	17
• Updated CONFIG Register Field Descriptions table to show correct default value	24
• Updated DIAG_ALRT Register Field Descriptions table to provide additional information	24
• Added *Documentation Support* and *Related Documentation* sections	39

Changes from Revision * (July 2023) to Revision A (December 2023)	Page
• Changed the data sheet status from Advanced Information to Production Mixed	1
• Changed the B grade device status from Advanced Information to Production Data	1

11 Mechanical, Packaging, and Orderable Information

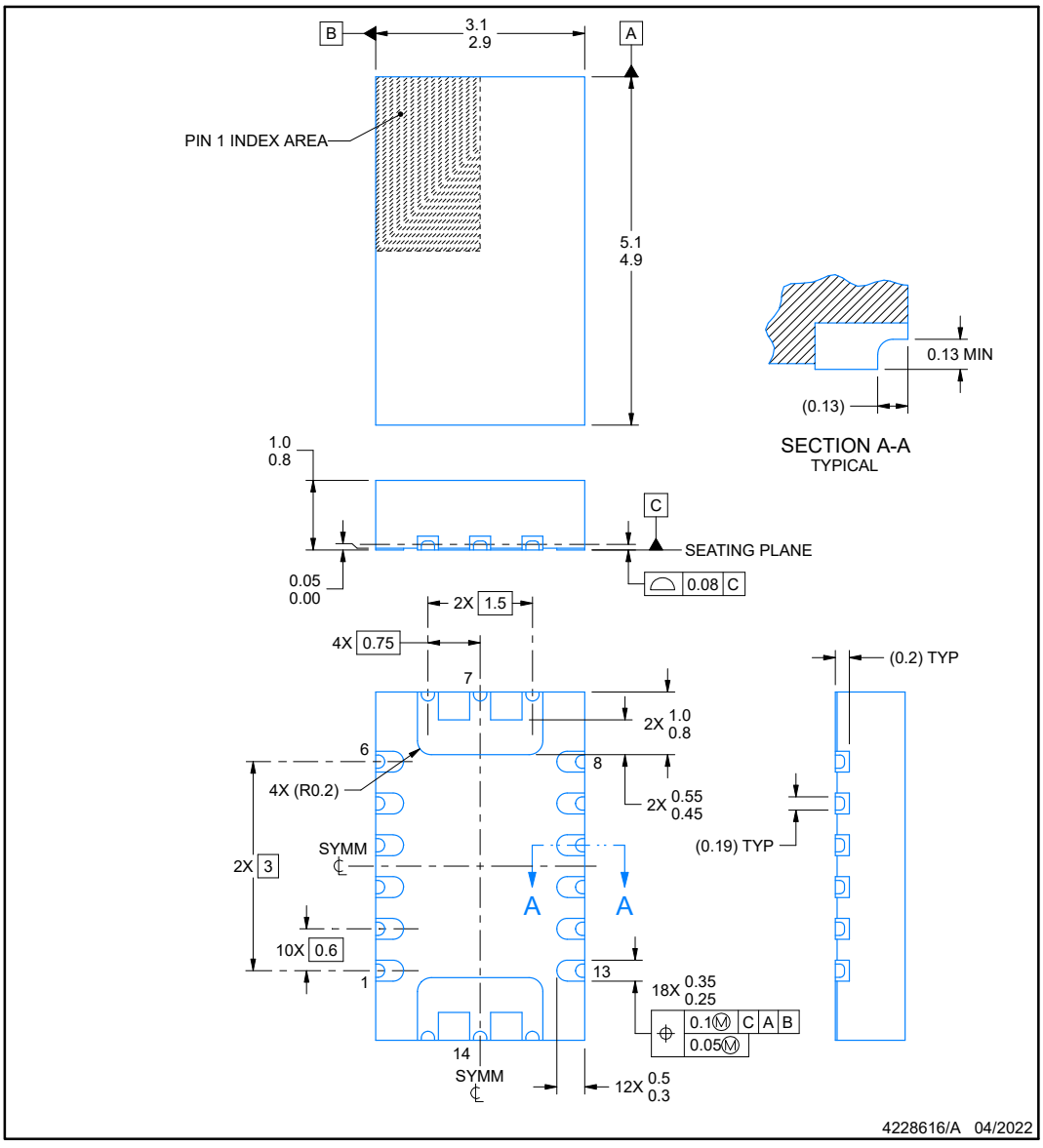
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

REL0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



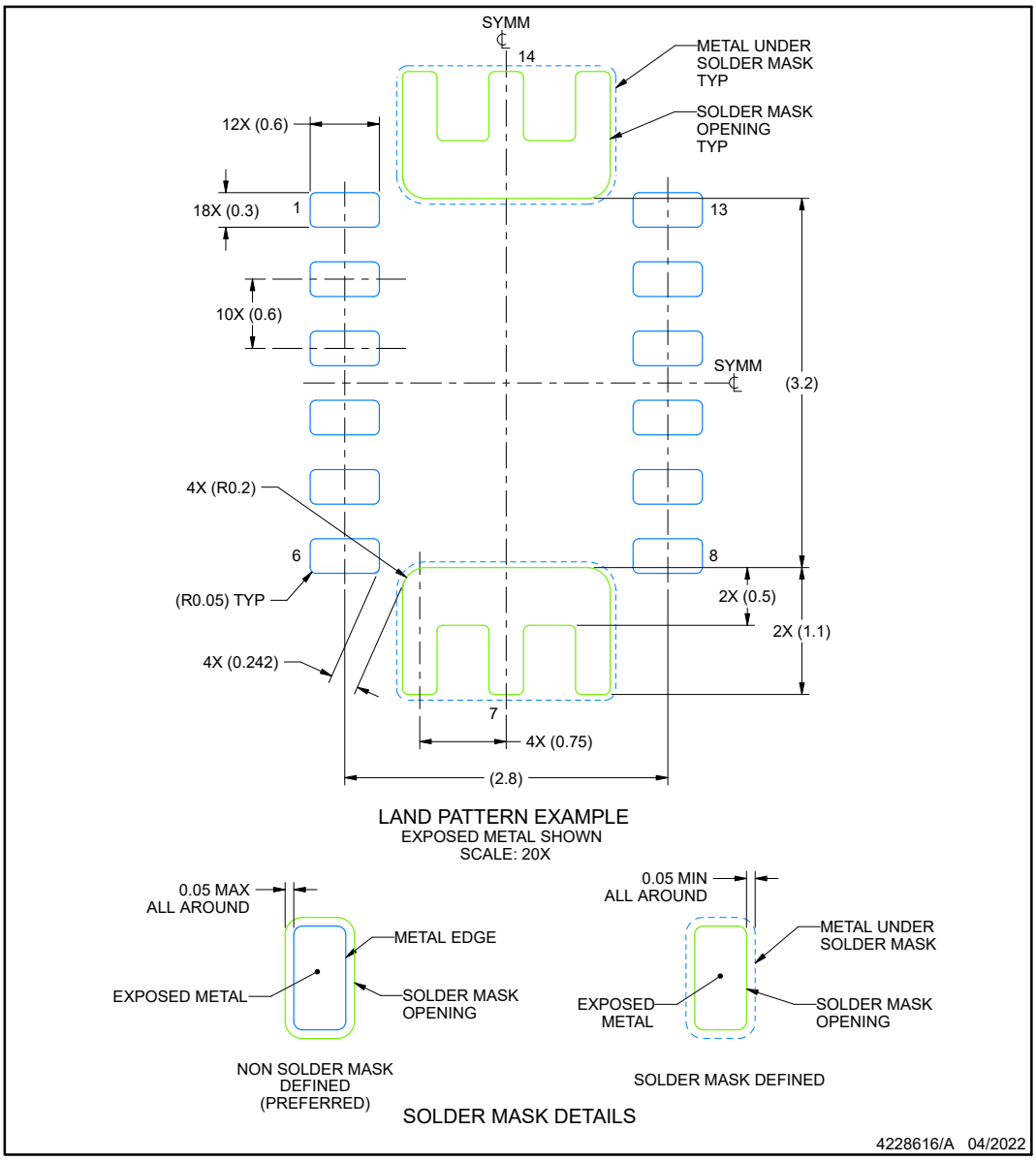
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

REL0014A — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



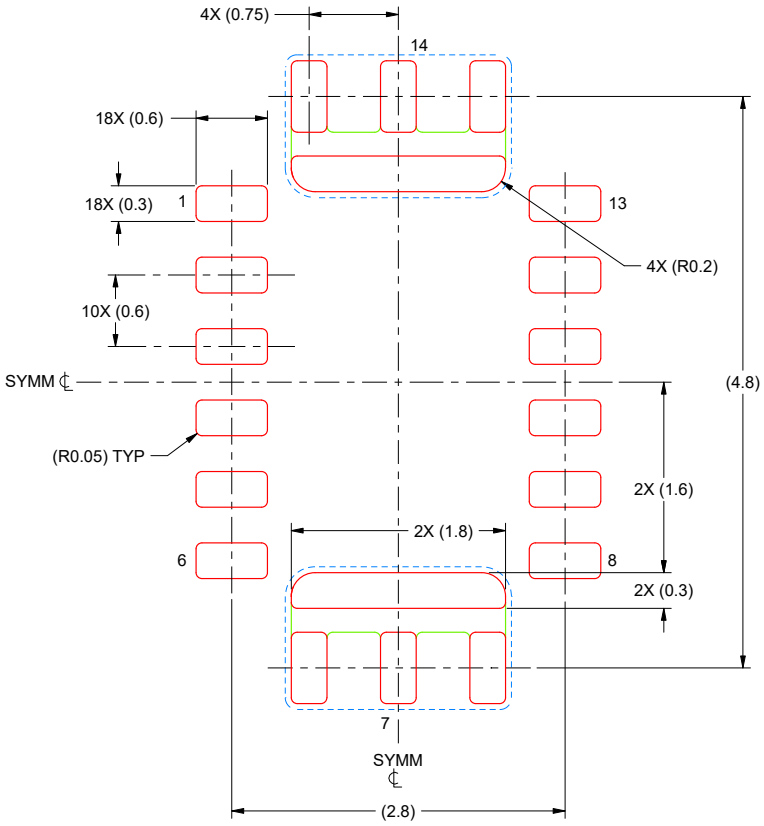
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

REL0014A — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

4228616/A 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA745AIRELR	Active	Production	VQFN (REL) | 14	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I745A
INA745BIRELR	Active	Production	VQFN (REL) | 14	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I745B
INA745BIRELR.A	Active	Production	VQFN (REL) | 14	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I745B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF INA745A, INA745B :

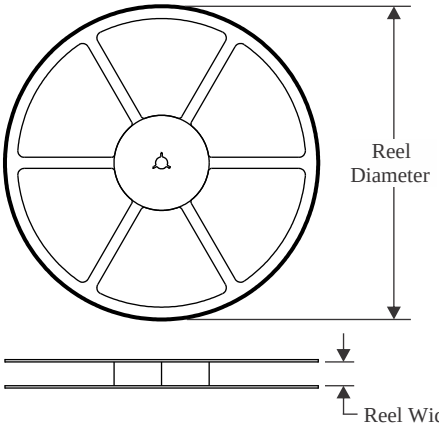
- Automotive : INA745A-Q1, INA745B-Q1

NOTE: Qualified Version Definitions:

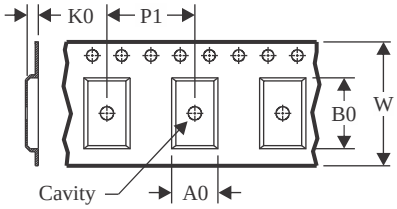
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

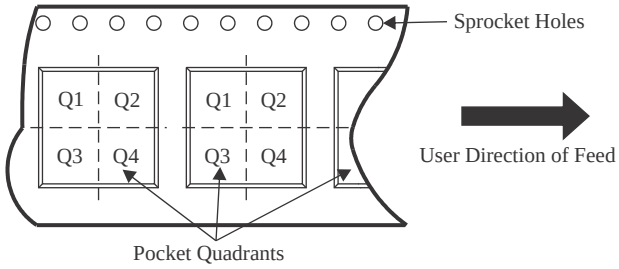


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

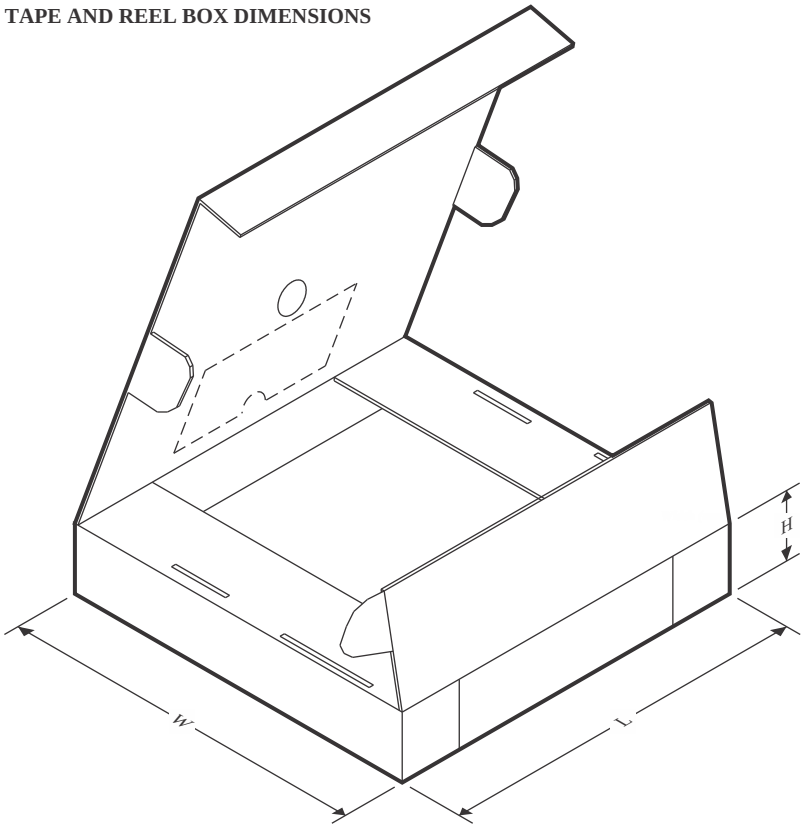
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA745AIRELR	VQFN	REL	14	5000	330.0	12.4	3.2	5.25	1.2	8.0	12.0	Q1
INA745BIRELR	VQFN	REL	14	5000	330.0	12.4	3.2	5.25	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

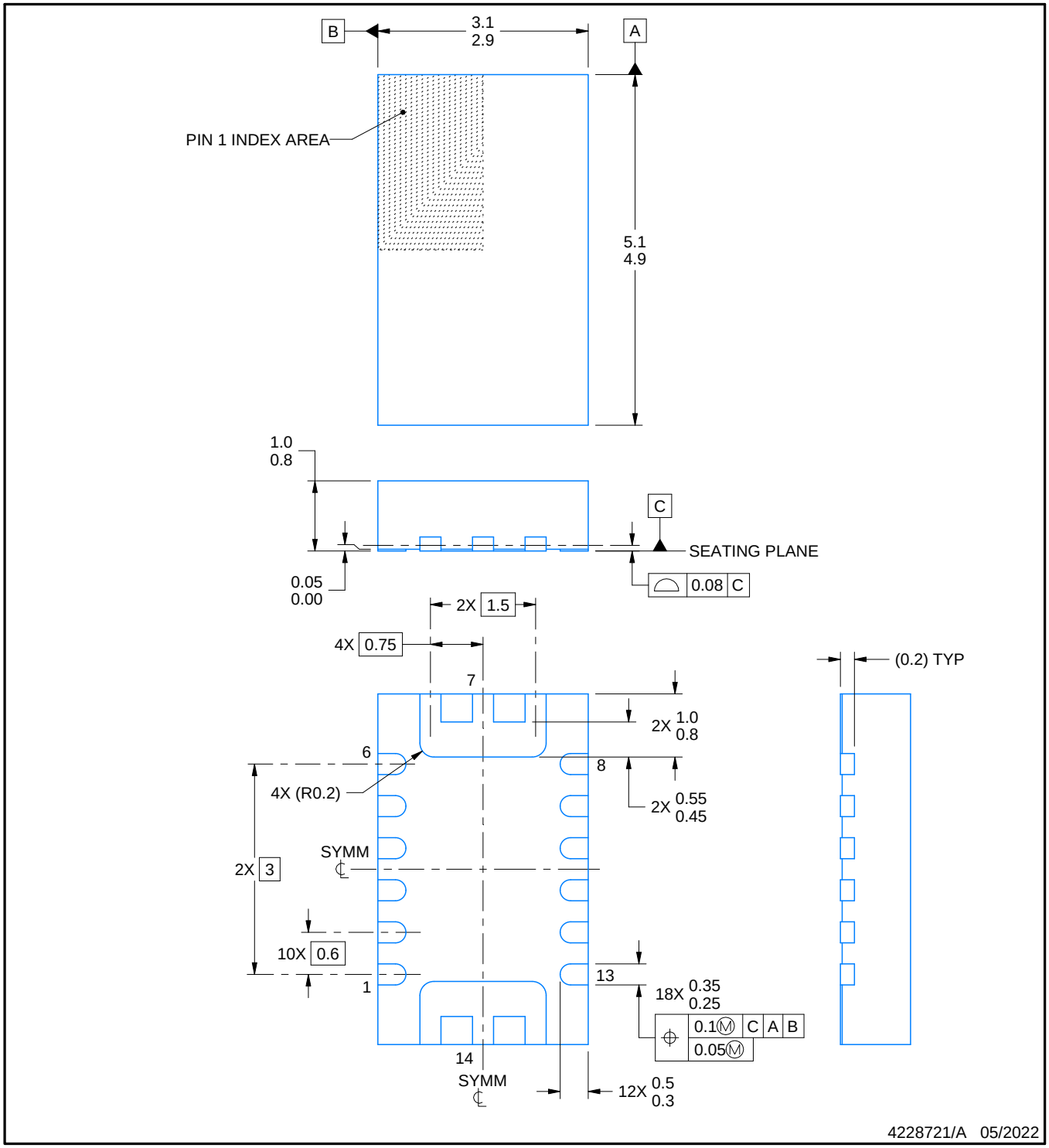
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA745AIRELR	VQFN	REL	14	5000	367.0	367.0	35.0
INA745BIRELR	VQFN	REL	14	5000	367.0	367.0	35.0

REL0014B

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

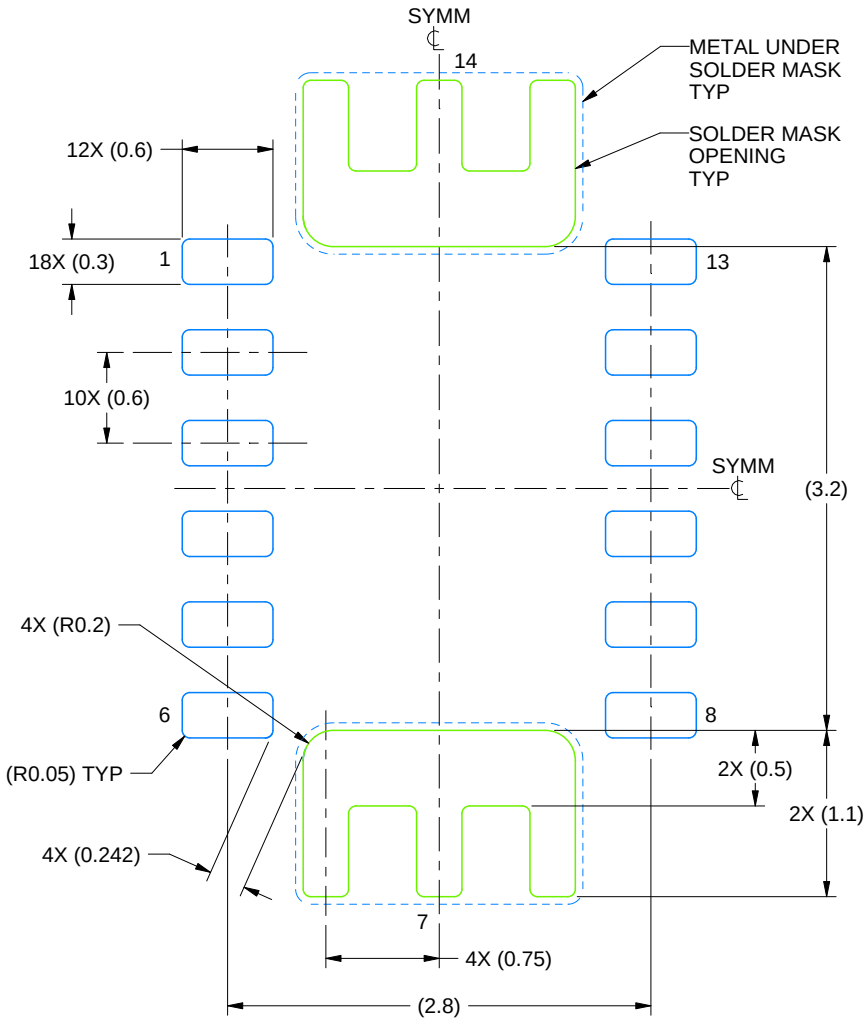
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

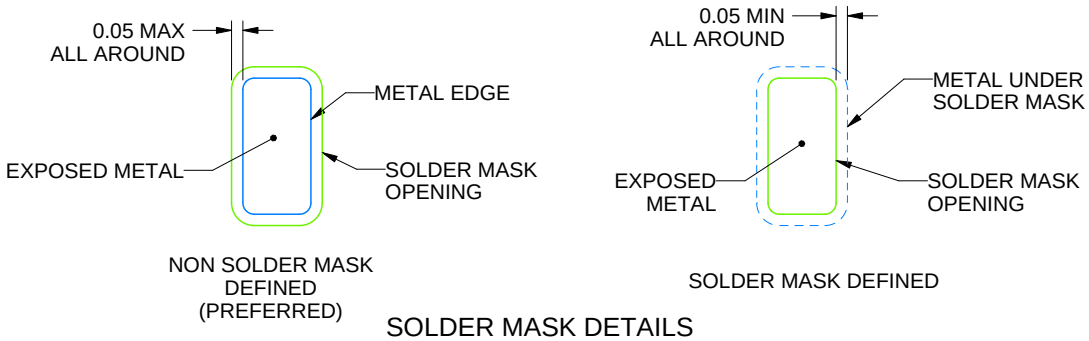
REL0014B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4228721/A 05/2022

NOTES: (continued)

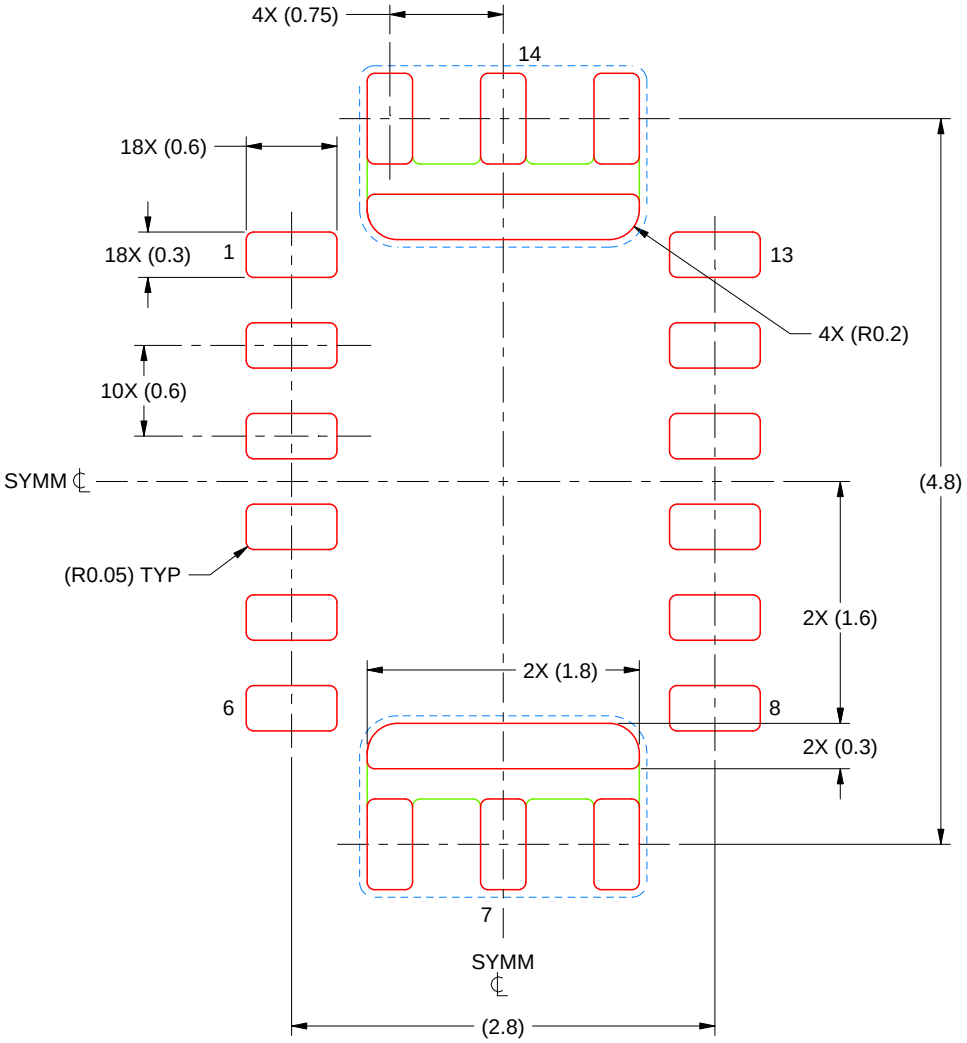
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

REL0014B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

4228721/A 05/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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