ISO722x Dual-Channel Digital Isolators

1 Features

- 1, 5, 25, and 150Mbps Signaling Rate Options
  - Low Channel-to-Channel Output Skew; 1ns Max
  - Low Pulse-Width Distortion (PWD); 1ns Max
  - Low Jitter Content; 1ns Typ at 150Mbps
- 50kV/µs Typical Transient Immunity
- Operates with 2.8V (C-Grade), 3.3V, or 5V Supplies
- 4kV ESD Protection
- High Electromagnetic Immunity
- –40°C to +125°C Operating Range
- Typical 28-Year Life at Rated Voltage (see Isolation Lifetime Projection)
- Safety Related Certifications
  - DIN EN IEC 60747-17 (VDE 0884-17) conformity per VDE
  - UL 1577 component recognition program
  - IEC 61010-1, IEC 62368-1 certifications

2 Applications

- Factory Automation
  - Modbus
  - Profibus™
  - DeviceNet™ Data Buses
- Computer Peripheral Interface
- Servo Control Interface
- Data Acquisition

3 Description

The ISO7220x and ISO7221x family devices are dual-channel digital isolators. To facilitate PCB layout, the channels are oriented in the same direction in the ISO7220x and in opposite directions in the ISO7221x. These devices have a logic input and output buffer separated by TI's silicon-dioxide (SiO_2) isolation barrier, providing galvanic isolation of up to $4000V_{PK}$ per VDE. Used in conjunction with isolated power supplies, these devices block high voltage and isolate grounds, as well as prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry.

A binary input signal is conditioned, translated to a balanced signal, then differentiated by the isolation barrier. Across the isolation barrier, a differential comparator receives the logic transition information, then sets or resets a flip-flop and the output circuit accordingly. A periodic update pulse is sent across the barrier to verify that the proper dc level of the output. If this dc-refresh pulse is not received every 4µs, the input is assumed to be unpowered or not being actively driven, and the failsafe circuit drives the output to a logic high state.

The resulting time constant provide fast operation with signaling rates available from 0Mbps (DC) to 150Mbps (The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps). The A-option, B-option, and C-option devices have TTL input thresholds and a noise filter at the input that prevents transient pulses from being passed to the output of the device. The M-option devices have CMOS $V_{CC}/2$ input thresholds and do not have the input noise filter and the additional propagation delay.

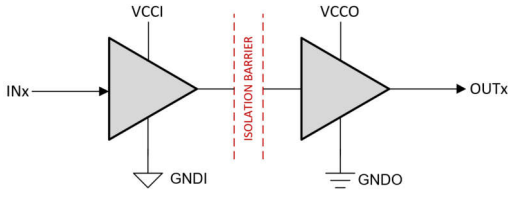
The ISO7220x and ISO7221x family of devices require two supply voltages of 2.8V (C-Grade), 3.3V, 5V, or any combination. All inputs are 5V tolerant when supplied from a 2.8V or 3.3V supply and all outputs are 4mA CMOS.

The ISO7220x and ISO7221x family of devices are characterized for operation over the ambient temperature range of –40°C to +125°C.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)	PACKAGE SIZE(2)
ISO7220x	D (SOIC, 8)	4.90mm × 3.91mm	4.9mm × 6mm
ISO7221x			

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



V_{CCI} and GNDI are supply and ground connections respectively for the input channels.
V_{CCO} and GNDO are supply and ground connections respectively for the output channels.

Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

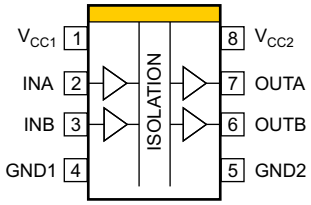


Figure 4-1. ISO7220x D Package 8-Pin SOIC Top View

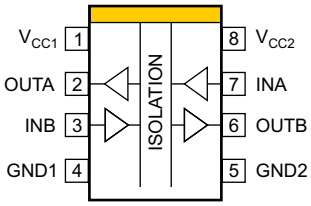


Figure 4-2. ISO7221x D Package 8-Pin SOIC Top View

Table 4-1. Pin Functions

PIN			Type[1]	DESCRIPTION
NAME	ISO7220x	ISO7221x		
INA	2	7	I	Input, channel A
INB	3	3	I	Input, channel B
GND1	4	4	—	Ground connection for V_{CC1}
GND2	5	5	—	Ground connection for V_{CC2}
OUTA	7	2	O	Output, channel A
OUTB	6	6	O	Output, channel B
V_{CC1}	1	1	—	Power supply, V_{CC1}
V_{CC2}	8	8	—	Power supply, V_{CC2}

(1) I = Input; O = Output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2), V_{CC1}, V_{CC2}	–0.5	6	V
V_I	Voltage at IN, OUT	–0.5	V_{CC} + 0.5(3)	V
I_O	Output current	–15	15	mA
T_J	Maximum junction temperature		170	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
(3) Maximum voltage must not exceed 6 V.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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5.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage(2), V_{CC1}, V_{CC2}	ISO722xA, ISO722xB, ISO722xM	3		5.5	V
		ISO722xC	2.8		5.5	
I_{OH}	High-level output current		–4			mA
I_{OL}	Low-level output current				4	mA
t_{ui}	Input pulse width(1)	ISO722xA	1			µs
		ISO722xB	200			ns
		ISO722xC	40			
		ISO722xM	6.67			
$1/t_{ui}$	Signaling rate(1)	ISO722xA	0		1000	kbps
		ISO722xB	0		5	Mbps
		ISO722xC	0		25	
		ISO722xM	0		150	
V_{IH}	High-level input voltage	ISO722xA, ISO722xB, ISO722xC	2		5.5	V
V_{IL}	Low-level input voltage	ISO722xA, ISO722xB, ISO722xC	0		0.8	V
V_{IH}	High-level input voltage	ISO722xM	0.7 x V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage	ISO722xM	0		0.3 x V_{CC}	V
T_J	Junction temperature		–40		150	°C
H	External magnetic field-strength immunity per IEC 61000-4-8 and IEC 61000-4-9 certification				1000	A/m

(1) Typical signaling rate and Input pulse width are measured at ideal conditions at 25°C.
(2) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.
For the 2.8-V operation, V_{CC1} or V_{CC2} is specified at 2.8 V.

5.4 Thermal Information

THERMAL METRIC(1)			ISO7220x ISO7221x	UNIT
			D (SOIC)	
			8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	Low-K Thermal Resistance(2)	212	°C/W
		High-K Thermal Resistance	122	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		69.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		47.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter		15.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter		47.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

(2) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.

5.5 Power Ratings

V_{CC1} = V_{CC2} = 5.5 V, T_J = 150C, C_L = 15 pF, Input a 150 Mbps 50% duty cycle square wave

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Device power dissipation, ISO722xM				390	mW

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5.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	4	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	0.008	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0884-17); IEC 60112	≥400	V
	Material group		II	
	Overvoltage category	Rated mains voltage ≤150 V_{RMS}	I-IV	
		Rated mains voltage ≤300 V_{RMS}	I-III	
		Rated mains voltage ≤400 V_{RMS}	I-II	
DIN EN IEC 60747-17 (VDE 0884-17):(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	560	V_{PK}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t= 1 s (100% production)	4000	V_{PK}
q_{pd}	Apparent charge(3)	Method a: After I/O safety test subgroup 2/3 $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤5	pC
		Method a: After environmental tests subgroup 1 $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.3 \times V_{IORM}$, t_m = 10 s	≤5	
		Method b: At routine test (100% production); $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s; $V_{pd(m)} = 1.5 \times V_{IORM}$, t_m = 1s (method b1) or $V_{pd(m)} = V_{ini}$, $t_m = t_{ini}$ (method b2)	≤5	
C_{IO}	Barrier capacitance, input to output(4)	V_{IO} = 0.4 sin (2πft), f = 1 MHz	1	pF
R_{IO}	Isolation resistance, input to output(4)	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$ = 2500 V_{RMS}, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$ = 3000 V_{RMS}, t = 1 s (100% production)	2500	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for *basic electrical insulation* only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Apparent charge is electrical discharge caused by a partial discharge (pd).
(4) All pins on each side of the barrier tied together creating a two-terminal device

5.7 Safety-Related Certifications

VDE	CSA	UL
Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to IEC 62368-1	Certified according to UL 1577 Component Recognition Program
Basic certificate: 40047657	Master contract number: 220991	File number: E181974

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5.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 212°C/W, V_I = 5.5 V, T_J = 170°C, T_A = 25°C, see Figure 5-1			124	mA
		$R_{\theta JA}$ = 212°C/W, V_I = 3.6 V, T_J = 170°C, T_A = 25°C, see Figure 5-1			190	
T_S	Safety temperature				150	°C

(1) The safety-limiting constraint is the maximum junction temperature specified in the data sheet. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

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5.9 Electrical Characteristics—5-V V_{CC1} and V_{CC2} Supplies

V_{CC1} and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	V_{CC1} supply current	ISO7220x quiescent, V_I = V_{CC} or 0 V, no load		1	2	mA
		ISO7221 quiescent, V_I = V_{CC} or 0 V, no load		8.5	17	
		ISO7220A and ISO7220B 1 Mbps, 0.5-MHz input clock signal, no load		2	3	mA
		ISO7221A, ISO7221B 1 Mbps, 0.5-MHz input clock signal, no load		10	18	
		ISO7220C, ISO7220M 25 Mbps, 12.5-MHz input clock signal, no load		4	9	mA
		ISO7221C and ISO7221M 25 Mbps, 12.5-MHz input clock signal, no load		12	22	
I_{CC2}	V_{CC2} supply current	ISO7220x quiescent, V_I = V_{CC} or 0 V, no load		16	31	mA
		ISO7221x quiescent, V_I = V_{CC} or 0 V, no load		8.5	17	
		ISO7220A and ISO7220B 1 Mbps, 0.5-MHz input clock signal, no load		17	32	mA
		ISO7221A, ISO7221B 1 Mbps, 0.5-MHz input clock signal, no load		10	18	
		ISO7220C, ISO7220M 25 Mbps, 12.5-MHz input clock signal, no load		20	34	mA
		ISO7221C and ISO7221M 25 Mbps, 12.5-MHz input clock signal, no load		12	22	
V_{OH}	High-level output voltage	I_{OH} = –4 mA, See Figure 6-1	V_{CC} – 0.8	4.6		V
		I_{OH} = –20 µA, See Figure 6-1	V_{CC} – 0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See Figure 6-1		0.2	0.4	V
		I_{OL} = 20 µA, See Figure 6-1		0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis			150		mV
I_{IH}	High-level input current	IN from 0 V to V_{CC}			10	µA
I_{IL}	Low-level input current	IN from 0 V to V_{CC}	–10			µA
C_I	Input capacitance to ground	IN at V_{CC}, V_I = 0.4 sin (2πft), f = 2MHz.		1		pF
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V, See Figure 6-3	25	50		kV/µs

5.10 Electrical Characteristics—5-V V_{CC1} and 3.3-V V_{CC2} Supply

V_{CC1} at 5 V ± 10%, V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	V_{CC1} supply current	ISO7220x quiescent, V_I = V_{CC} or 0 V, no load		1	2	mA
		ISO7221x quiescent, V_I = V_{CC} or 0 V, no load		8.5	17	
		ISO7220A and ISO7220B 1 Mbps, 0.5-MHz input clock signal, no load		2	3	mA
		ISO7221A and ISO7221B 1 Mbps, 0.5-MHz input clock signal, no load		10	18	
		ISO7220C and ISO7220M 25 Mbps, 12.5-MHz input clock signal, no load		4	9	mA
		ISO7221C and ISO7221M 25 Mbps, 12.5-MHz input clock signal, no load		12	22	
I_{CC2}	V_{CC2} supply current	ISO7220x quiescent, V_I = V_{CC} or 0 V, no load		8	18	mA
		ISO7221x quiescent, V_I = V_{CC} or 0 V, no load		4.3	9.5	
		ISO7220A and ISO7220B 1 Mbps, 0.5-MHz input clock signal, no load		9	19	mA
		ISO7221A and ISO7221B 1 Mbps, 0.5-MHz input clock signal, no load		5	11	
		ISO7220C and ISO7220M 25 Mbps, 12.5-MHz input clock signal, no load		10	20	mA
		ISO7221C and ISO7221M 25 Mbps, 12.5-MHz input clock signal, no load		6	12	

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V_{CC1} at 5 V ± 10%, V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	ISO7220x, ISO7221x (3.3-V side), I_{OH} = –4 mA, See Figure 6-1	V_{CC} – 0.4			V
		ISO7221x (5-V side), I_{OH} = –4 mA, See Figure 6-1	V_{CC} – 0.8			
		All devices, I_{OH} = –20 µA, See Figure 6-1	V_{CC} – 0.1			
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See Figure 6-1			0.4	V
		I_{OL} = 20 µA, See Figure 6-1			0.1	
$V_{I(HYS)}$	Input voltage hysteresis			150		mV
I_{IH}	High-level input current	IN from 0 V to V_{CC}			10	µA
I_{IL}	Low-level input current	IN from 0 V to V_{CC}	–10			µA
C_I	Input capacitance to ground	IN at V_{CC}, V_I = 0.4 sin (2πft), f = 2MHz.		1		pF
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V, See Figure 6-3	15	40		kV/µs

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5.11 Electrical Characteristics—3.3-V V_{CC1} and 5-V V_{CC2} Supply

V_{CC1} at 3.3 V ± 10%, V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	V_{CC1} supply current	ISO7220x quiescent, V_I = V_{CC} or 0 V, no load		0.6	1	mA
		ISO7221x quiescent, V_I = V_{CC} or 0 V, no load		4.3	9.5	
		ISO7220A and ISO7220B 1 Mbps, 0.5-MHz input clock signal, no load		1	2	mA
		ISO7221A and ISO7221B 1 Mbps, 0.5-MHz input clock signal, no load		5	11	
		ISO7220C and ISO7220M 25 Mbps, 12.5-MHz input clock signal, no load		2	4	mA
		ISO7221C and ISO7221M 25 Mbps, 12.5-MHz input clock signal, no load		6	12	
I_{CC2}	V_{CC2} supply current	ISO7220x quiescent, V_I = V_{CC} or 0 V, no load		16	31	mA
		ISO7221x quiescent, V_I = V_{CC} or 0 V, no load		8.5	17	
		ISO7220A and ISO7220B 1 Mbps, 0.5-MHz input clock signal, no load		18	32	mA
		ISO7221A and ISO7221B 1 Mbps, 0.5-MHz input clock signal, no load		10	18	
		ISO7220C and ISO7220M 25 Mbps, 12.5-MHz input clock signal, no load		20	34	mA
		ISO7221C and ISO7221M 25 Mbps, 12.5-MHz input clock signal, no load		12	22	
V_{OH}	High-level output voltage	ISO7220x and ISO7221x (5-V side), I_{OH} = –4 mA, See Figure 6-1	V_{CC} – 0.8			V
		ISO7221x (3.3-V side), I_{OH} = –4 mA, See Figure 6-1	V_{CC} – 0.4			
		All devices, I_{OH} = –20 µA, See Figure 6-1	V_{CC} – 0.1			
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See Figure 6-1			0.4	
		I_{OL} = 20 µA, See Figure 6-1		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis			150		mV
I_{IH}	High-level input current	IN from 0 V or V_{CC}			10	µA
I_{IL}	Low-level input current	IN from 0 V or V_{CC}	–10			µA
C_I	Input capacitance to ground	IN at V_{CC}, V_I = 0.4 sin (2πft), f = 2MHz.		1		pF
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V, See Figure 6-3	15	40		kV/µs

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5.12 Electrical Characteristics—3.3-V V_{CC1} and V_{CC2} Supplies

V_{CC1} and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted.)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	V_{CC2} supply current	ISO7220x quiescent, V_I = V_{CC} or 0 V, no load		0.6	1	mA
		ISO7221x quiescent, V_I = V_{CC} or 0 V, no load		4.3	9.5	
		ISO7220A and ISO7220B 1 Mbps, 0.5-MHz input clock signal, no load		1	2	mA
		ISO7221A and ISO7221B 1 Mbps, 0.5-MHz input clock signal, no load		5	11	
		ISO7220C and ISO7220M 25 Mbps, 12.5-MHz input clock signal, no load		2	4	mA
		ISO7221C and ISO7221M 25 Mbps, 12.5-MHz input clock signal, no load		6	12	
I_{CC2}	V_{CC2} supply current	ISO7220x quiescent, V_I = V_{CC} or 0 V, no load		8	18	mA
		ISO7221x quiescent, V_I = V_{CC} or 0 V, no load		4.3	9.5	
		ISO7220A and ISO7220B 1 Mbps, 0.5-MHz input clock signal, no load		9	19	mA
		ISO7221A and ISO7221B 1 Mbps, 0.5-MHz input clock signal, no load		5	11	
		ISO7220C and ISO7220M 25 Mbps, 12.5-MHz input clock signal, no load		10	20	mA
		ISO7221C and ISO7221M 25 Mbps, 12.5-MHz input clock signal, no load		6	12	
V_{OH}	High-level output voltage	I_{OH} = –4 mA, See Figure 6-1	V_{CC} – 0.4	3		V
		I_{OH} = –20 µA, See Figure 6-1	V_{CC} – 0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See Figure 6-1		0.2	0.4	
		I_{OL} = 20 µA, See Figure 6-1		0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis			150		mV
I_{IH}	High-level input current	IN from 0 V or V_{CC}			10	µA
I_{IL}	Low-level input current	IN from 0 V or V_{CC}	–10			µA
C_I	Input capacitance to ground	IN at V_{CC}, V_I = 0.4 sin (2πft), f = 2MHz.		1		pF
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V, See Figure 6-3	15	40		kV/µs

(1) For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

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5.13 Electrical Characteristics—2.8-V V_{CC1} and V_{CC2} Supplies

V_{CC1} and V_{CC2} at 2.8 V (over recommended operating conditions unless otherwise noted.) 2.8-V operation is only specified for ISO722xC with production screening starting in January 2012. The first two digits of the Lot Trace Code (YMSLLLLG4) written on top of each device can be used to identify year and month of production respectively.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	V_{CC1} supply current	ISO7220C quiescent, V_I = V_{CC} or 0 V, no load		0.4	0.9	mA
		ISO7221C quiescent, V_I = V_{CC} or 0 V, no load		3.7	7.5	
		ISO7220C 25 Mbps, 12.5-MHz input clock signal, no load		1.5	3.5	mA
		ISO7221C 25 Mbps, 12.5-MHz input clock signal, no load		4.5	10	
I_{CC2}	V_{CC2} supply current	ISO7220C quiescent, V_I = V_{CC} or 0 V, no load		6.8	15	mA
		ISO7221C quiescent, V_I = V_{CC} or 0 V, no load		3.7	7.5	
		ISO7220C 25 Mbps, 12.5-MHz input clock signal, no load		9	17	mA
		ISO7221C 25 Mbps, 12.5-MHz input clock signal, no load		4.5	10	
V_{OH}	High-level output voltage	I_{OH} = –4 mA, See Figure 6-1	V_{CC} – 0.6	2.55		V
		I_{OH} = –20 µA, See Figure 6-1	V_{CC} – 0.1	2.8		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See Figure 6-1		0.25	0.6	
		I_{OL} = 20 µA, See Figure 6-1		0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis			150		mV
I_{IH}	High-level input current	IN from 0 V or V_{CC}			10	µA
I_{IL}	Low-level input current	IN from 0 V or V_{CC}	–10			µA
C_I	Input capacitance to ground	IN at V_{CC}, V_I = 0.4 sin (2πft), f = 2MHz.		1		pF
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V, See Figure 6-3	10	30		kV/µs

5.14 Switching Characteristics—5-V V_{CC1} and V_{CC2} Supplies

V_{CC1} and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO722xA, see Figure 6-1	252	405	600	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)			1	18	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO722xB, see Figure 6-1	35	55	70	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)			1	3	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO722xC, see Figure 6-1	21	32	42	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)			1	2	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO722xM, see Figure 6-1	6	10	16	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)			0.5	1	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO722xA			180	ns
		ISO722xB			17	
		ISO722xC			10	
		ISO722xM			3	
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO7220A		3	15	ns
		ISO7220B		0.6	3	
		ISO7220C			2	
		ISO7220M		0.2	1	
t_r	Output signal rise time	See Figure 6-1		2.3		ns
t_f	Output signal fall time			2.3		ns
t_{fs}	Failsafe output delay time from input power loss	See Figure 6-2		3		µs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO722xM, 150 Mbps PRBS NRZ data, 5-bit max same polarity input, both channels, See Figure 6-4, Figure 5-13		1		ns
		ISO722xM, 150 Mbps unrestricted bit run length data input, both channels, See Figure 6-4		2		

(1) Also referred to as pulse skew.

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(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified pins of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

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5.15 Switching Characteristics—5-V V_{CC1} and 3.3-V V_{CC2} Supply

V_{CC1} at 5 V ± 10%, V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO722xA, see Figure 6-1	253	410	585	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)			1	18	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO722xB, see Figure 6-1	35	58	75	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)			1	3	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO722xC, see Figure 6-1	21	36	48	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)			1	2	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO722xM, see Figure 6-1	7	12	20	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)			0.5	1	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO722xA			180	ns
		ISO722xB			17	
		ISO722xC			10	
		ISO722xM			5	
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO7220A		3	15	ns
		ISO7220B		0.6	3	
		ISO7220C			2	
		ISO7220M		0.2	1	
t_r	Output signal rise time	See Figure 6-1		2.3		ns
t_f	Output signal fall time			2.3		ns
t_{fs}	Failsafe output delay time from input power loss	See Figure 6-2		3		µs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO722xM, 150 Mbps PRBS NRZ data, 5-bit max same polarity input, both channels, See Figure 6-4, Figure 5-13		1		ns
		ISO722xM, 150 Mbps unrestricted bit run length data input, both channels, See Figure 6-4		2		

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified pins of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

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5.16 Switching Characteristics—3.3-V_{CC1} and 5-V V_{CC2} Supplies

V_{CC1} at 3.3 V ± 10%, V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO722xA, see Figure 6-1	268	395	605	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)			1	22	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO722xB, see Figure 6-1	38	58	75	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)			1	4	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO722xC, see Figure 6-1	21	36	48	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)			1	3	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO722xM, see Figure 6-1	7	12	21	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)			0.5	1	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO722xA			190	ns
		ISO722xB			17	
		ISO722xC			10	
		ISO722xM			5	
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO7220A		3	15	ns
		ISO7220B		0.6	3	
		ISO7220C			2.5	
		ISO7220M		0.2	1	
t_r	Output signal rise time	See Figure 6-1		2.3		ns
t_f	Output signal fall time			2.3		ns
t_{fs}	Failsafe output delay time from input power loss	See Figure 6-2		3		µs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO722xM, 150 Mbps PRBS NRZ data, 5-bit max same polarity input, both channels, see Figure 6-4, Figure 5-13		1		ns
		ISO722xM, 150 Mbps unrestricted bit run length data input, both channels, see Figure 6-4		2		

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified pins of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

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5.17 Switching Characteristics—3.3-V V_{CC1} and V_{CC2} Supplies

V_{CC1} and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO722xA, see Figure 6-1	267	400	610	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)			1	22	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO722xB, see Figure 6-1	37	62	78	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)			1	4	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO722xC, see Figure 6-1	23	40	52	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)			1	3	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO722xM, see Figure 6-1	8	16	25	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)			0.5	1	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO722xA			190	ns
		ISO722xB			17	
		ISO722xC			10	
		ISO722xM			5	
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO7220A		3	15	ns
		ISO7220B		0.6	3	
		ISO7220C			3.5	
		ISO7220M		0.2	1	
t_r	Output signal rise time	See Figure 6-1		2.3		ns
t_f	Output signal fall time			2.3		ns
t_{fs}	Failsafe output delay time from input power loss	See Figure 6-2		3		µs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO722xM, 150 Mbps PRBS NRZ data, 5-bit max same polarity input, both channels, See Figure 6-4, Figure 5-13		1		ns
		ISO722xM, 150 Mbps unrestricted bit run length data input, both channels, See Figure 6-4		2		

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified pins of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

5.18 Switching Characteristics—2.8-V V_{CC1} and V_{CC2} Supplies

V_{CC1} and V_{CC2} at 2.8 V (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO722xC, see Figure 6-1	25	45	65	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)			1.5	5	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO722xC			12	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO7220C		0.2	5	ns
t_r	Output signal rise time	See Figure 6-1		2.3		ns
t_f	Output signal fall time			2.3		ns
t_{fs}	Failsafe output delay time from input power loss	See Figure 6-2		4.6		µs

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified pins of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

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5.19 Insulation Characteristics Curves

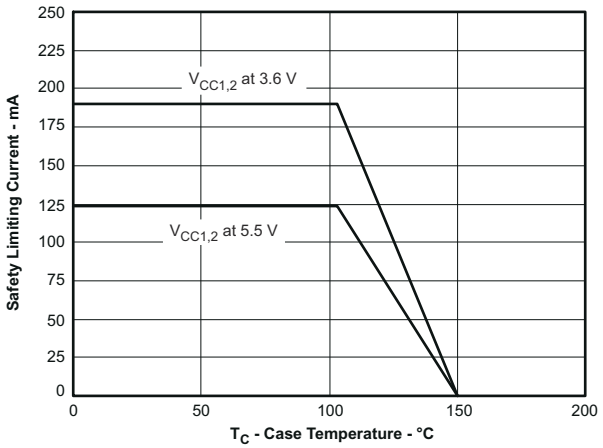


Figure 5-1. Thermal Derating Curve for Limiting Current per VDE

5.20 Typical Characteristics

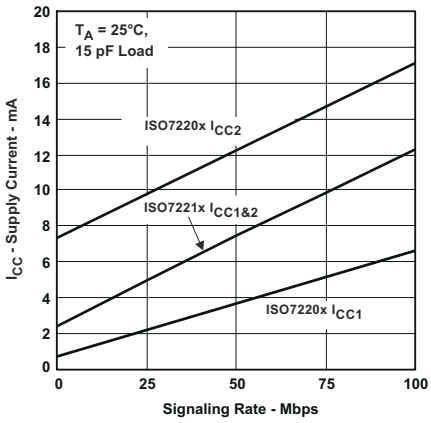


Figure 5-2. 3.3-V_{RMS} Supply Current vs Signaling Rate (Mbps)

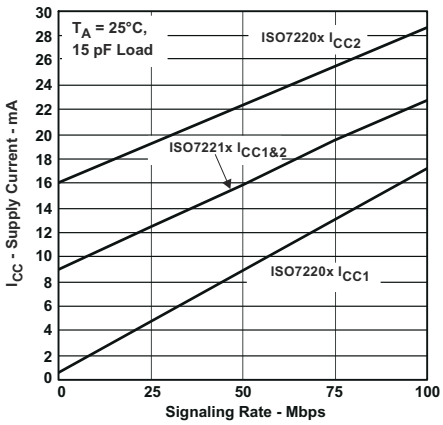


Figure 5-3. 5-V_{RMS} Supply Current vs Signaling Rate (Mbps)

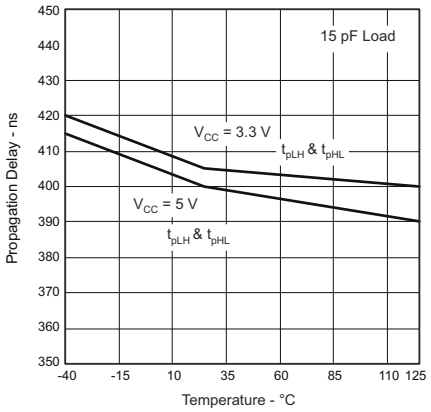


Figure 5-4. Propagation Delay vs Free-Air Temperature, ISO722xA

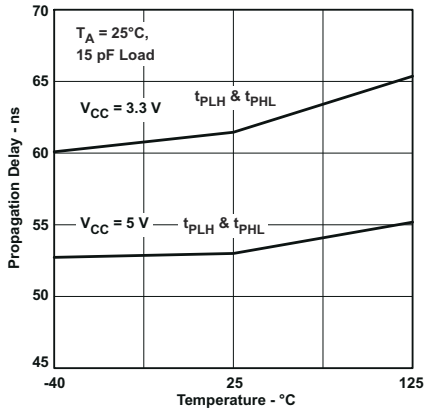


Figure 5-5. Propagation Delay vs Free-Air Temperature, ISO722xB

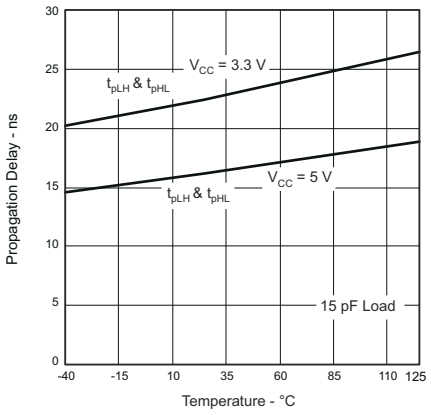


Figure 5-6. Propagation Delay vs Free-Air Temperature, ISO722xC

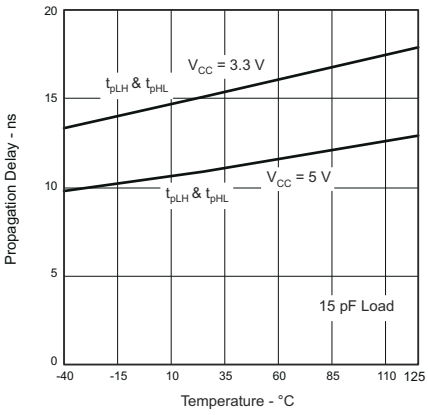


Figure 5-7. Propagation Delay vs Free-Air Temperature, ISO722xM

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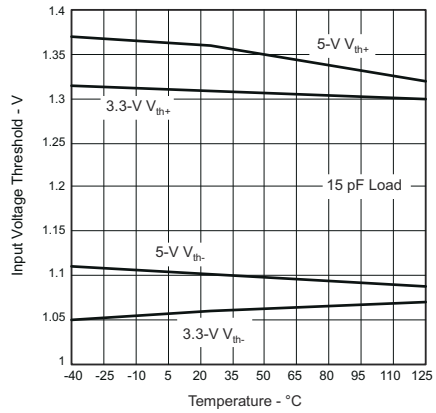


Figure 5-8. ISO722xA, ISO722xB and ISO722xC Input Voltage Low-to-High Switching Threshold vs Free-Air Temperature

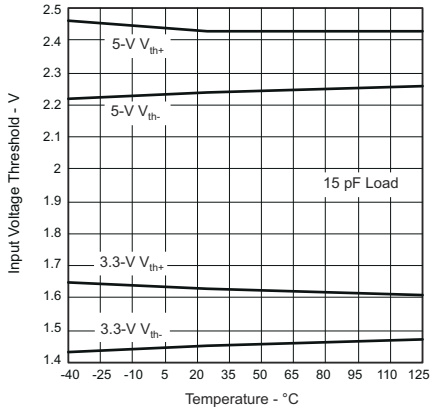


Figure 5-9. ISO722xM Input Voltage High-to-Low vs Free-Air Temperature

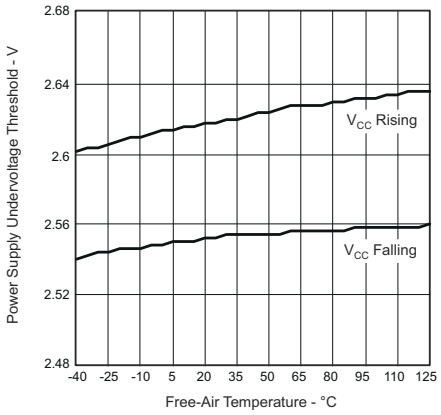


Figure 5-10. V_{CC} Undervoltage Threshold vs Free-Air Temperature

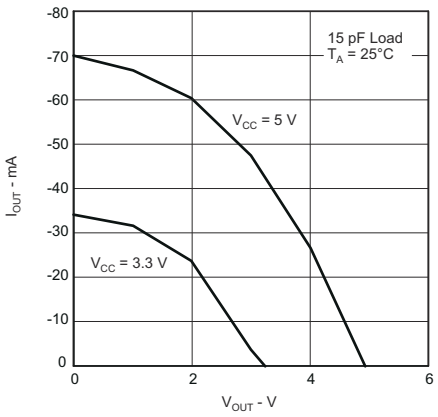


Figure 5-11. High-Level Output Current vs High-Level Output Voltage

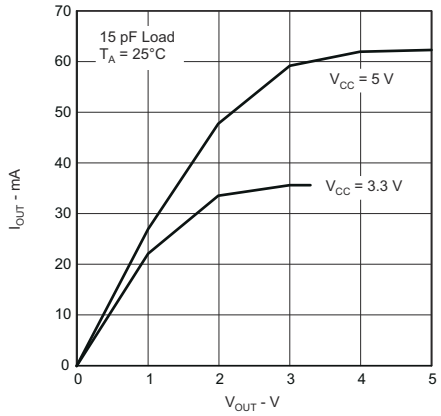


Figure 5-12. Low-Level Output Current vs Low-Level Output Voltage

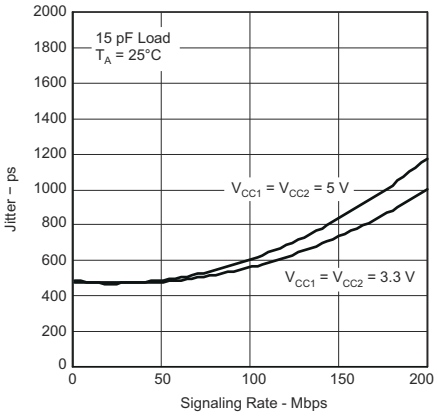
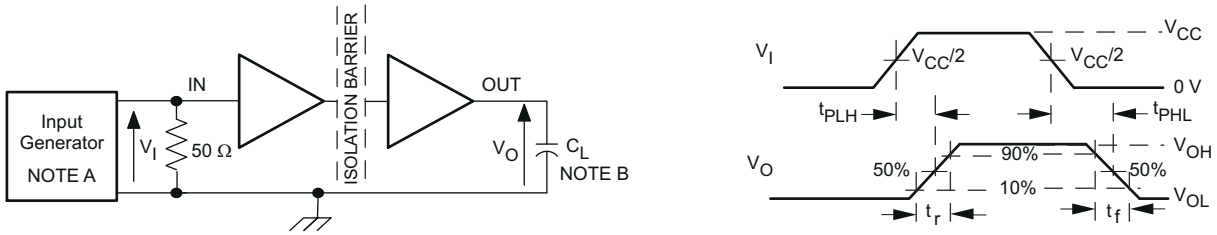


Figure 5-13. ISO722xM Jitter vs Signaling Rate

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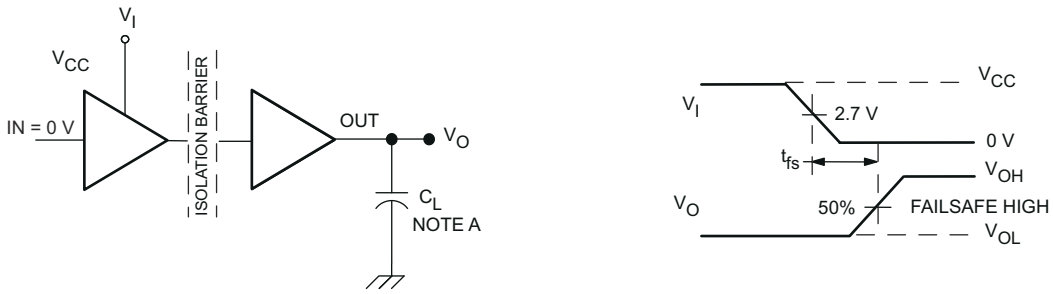
6 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

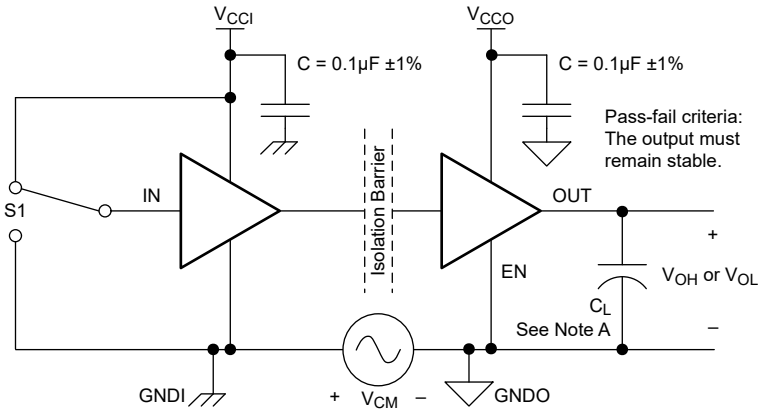
B. C_L = 15 pF and includes instrumentation and fixture capacitance within ± 20%.

Figure 6-1. Switching Characteristic Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ± 20%.

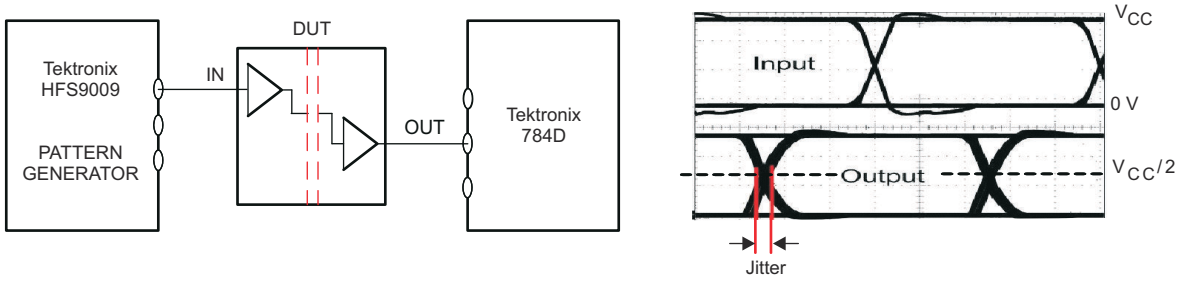
Figure 6-2. Failsafe Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ± 20%.

Figure 6-3. Common-Mode Transient Immunity Test Circuit

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PRBS bit pattern run length is 2^{16} – 1. Transition time is 800 ps.

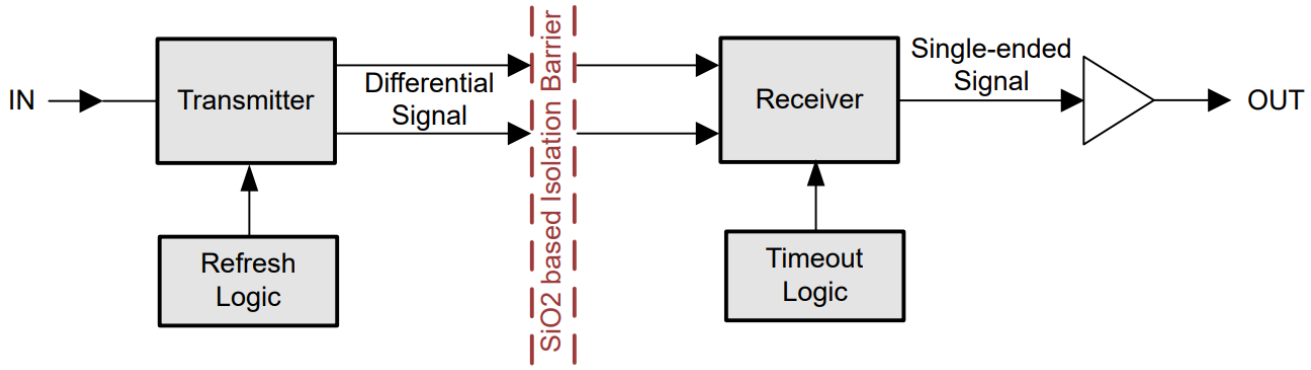
Figure 6-4. Peak-to-Peak Eye-Pattern Jitter Test Circuit and Voltage Waveform

7 Detailed Description

7.1 Overview

The ISO722x family of devices transmit digital data across a silicon dioxide based isolation barrier. The digital input signal (IN) of the device is sampled by a transmitter and at every data edge the transmitter sends a corresponding differential signal across the isolation barrier. When the input signal is static, the refresh logic periodically sends the necessary differential signal from the transmitter. On the other side of the isolation barrier, the receiver converts the differential signal into a single-ended signal which is output on the OUT pin through a buffer. If the receiver does not receive a data or refresh signal, the timeout logic detects the loss of signal or power from the input side and drives the output to the default level.

7.2 Functional Block Diagram



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7.3 Feature Description

The following table provides an overview of the device features.

Table 7-1. Device Features

PART NUMBER	MAXIMUM SIGNALING RATE	INPUT THRESHOLD	CHANNEL DIRECTION
ISO7220A	1 Mbps	≅ 1.5 V (TTL) (CMOS compatible)	Same direction
ISO7220B	5 Mbps	≅ 1.5 V (TTL) (CMOS compatible	
ISO7220C	25 Mbps	≅ 1.5 V (TTL) (CMOS compatible)	
ISO7220M	150 Mbps	V_{CC}/ 2 (CMOS)	
ISO7221A	1 Mbps	≅ 1.5 V (TTL) (CMOS compatible)	Opposite directions
ISO7221B	5 Mbps	≅ 1.5 V (TTL) (CMOS compatible)	
ISO7221C	25 Mbps	≅ 1.5 V (TTL) (CMOS compatible)	
ISO7221M	150 Mbps	V_{CC}/ 2 (CMOS)	

7.4 Device Functional Modes

The ISO7220x and ISO7221x family of devices functional modes are listed in Table 7-2.

Table 7-2. ISO7220x or ISO7221x Function Table

INPUT SIDE V_{CC} (1)	OUTPUT SIDE V_{CC}	INPUT (IN)	OUTPUT (OUT)
PU	PU	H	H
		L	L
		Open	H
PD	PU	X	H
X	PD	X	Undetermined

(1) PU = Powered Up (V_{CC} ≥ 3.0 V), PD = Powered Down (V_{CC} ≤ 2.5 V), X = Irrelevant, H = High Level,
L = Low Level

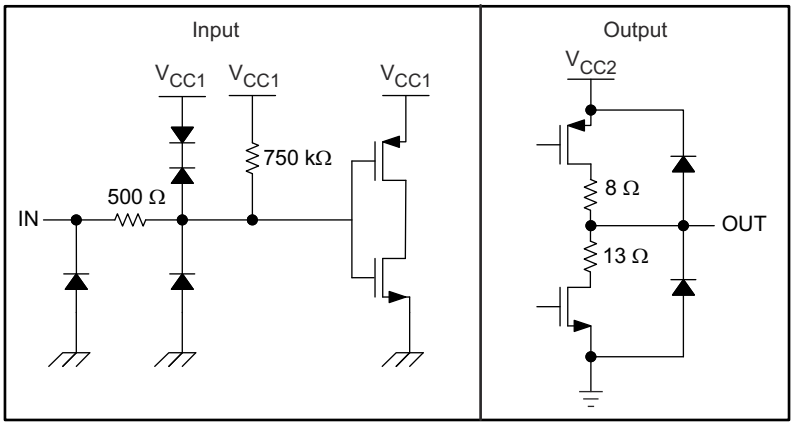


Figure 7-1. Device I/O Schematics

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The ISO7220x and ISO7221x family devices use single-ended TTL or CMOS-logic switching technology. The supply voltage range is from 3 V (2.8 V for C-grade) to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, μC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

8.2 Typical Application

The ISO7221x family of devices can be used with Texas Instruments' mixed signal micro-controller, digital-to-analog converter, transformer driver, and voltage regulator to create an isolated 4- to 20-mA current loop.

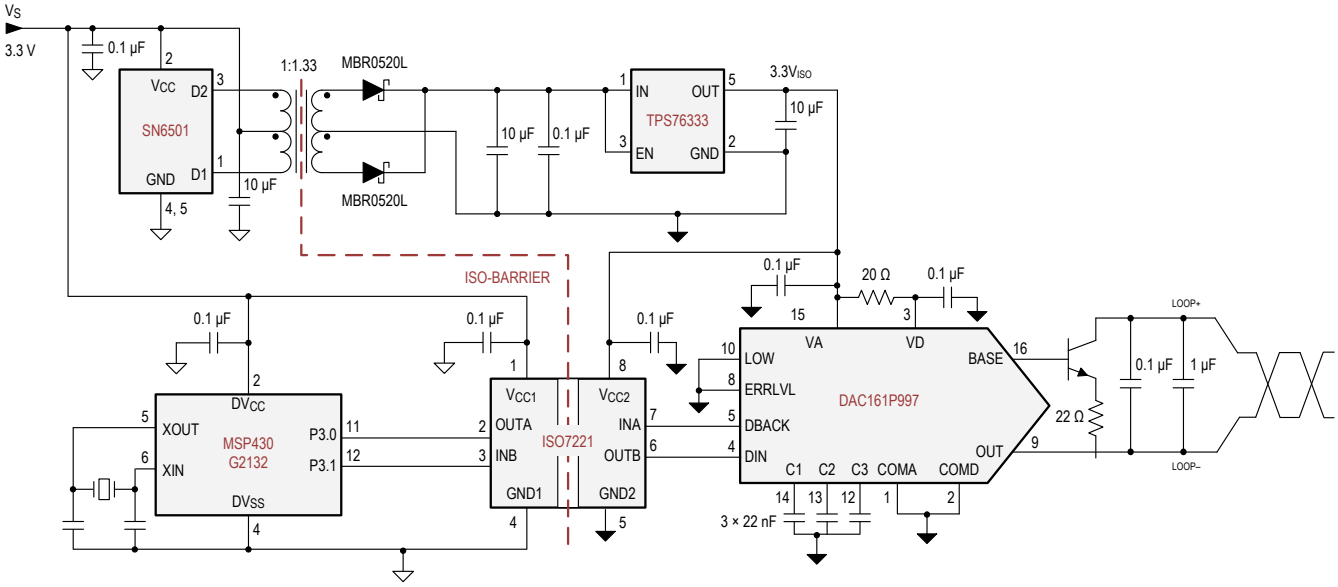


Figure 8-1. Isolated 4- to 20-mA Current Loop

8.2.1 Design Requirements

Unlike optocouplers, which require external components to improve performance, provide bias (or limit current), the ISO7220x and ISO7221x devices require only two external bypass capacitors to operate.

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8.2.2 Detailed Design Procedure

Figure 8-2 and Figure 8-3 show the hookup of a typical ISO7220x and ISO7221x circuit. The only external components are two bypass capacitors.

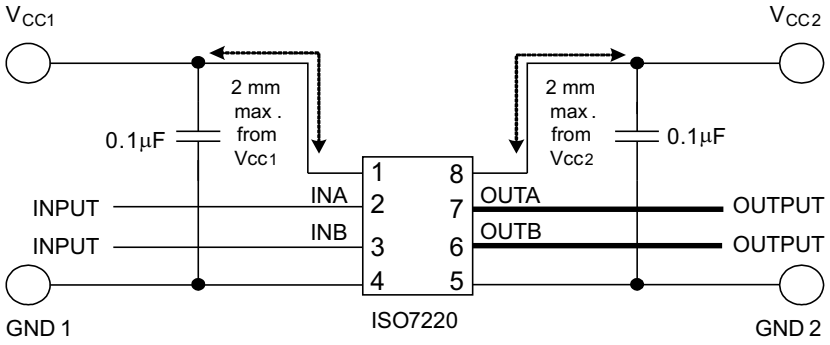


Figure 8-2. Typical ISO7220x Circuit Hook-Up

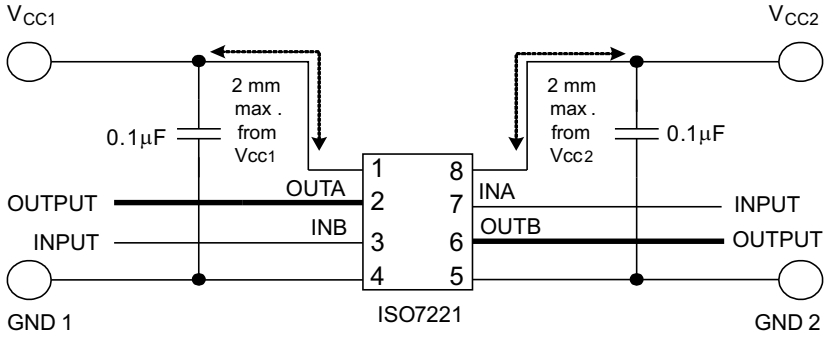


Figure 8-3. Typical ISO7221x Circuit Hook-Up

8.2.3 Insulation Lifetime

At maximum working voltage, the isolation barrier of the ISO72x and ISO72xM family of devices has more than 28 years of life.

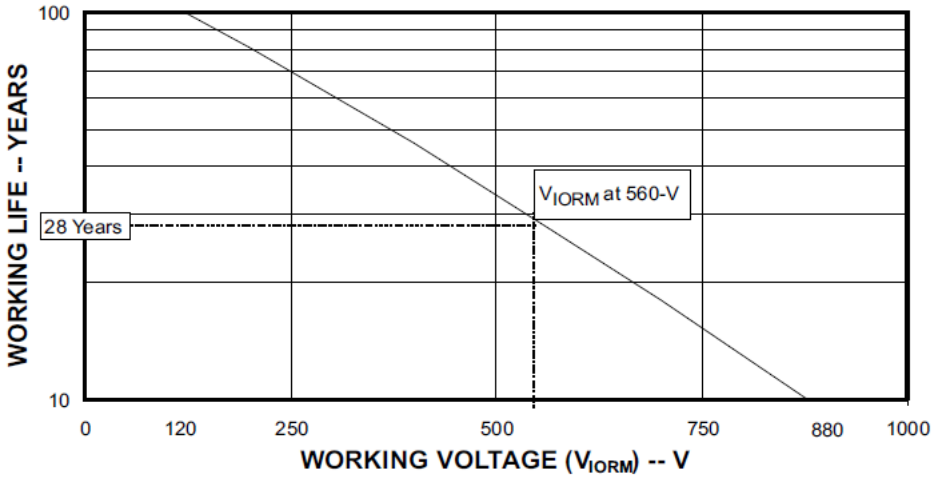


Figure 8-4. Insulation Lifetime Projection

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8.3 Power Supply Recommendations

To help provide reliable operation at all data rates and supply voltages, a 0.1-µF bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors must be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments SN6501 device. For such applications, detailed power supply design and transformer selection recommendations are available in *SN6501 Transformer Driver for Isolated Power Supplies*.

8.4 Layout

8.4.1 Layout Guidelines

A minimum of four layers are required to accomplish a low EMI PCB design (see Figure 8-5). Layer stacking must be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Route the high-speed traces on the top layer to avoid the use of vias (and the introduction of the inductances) and allow for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Place a solid ground plane next to the high-speed signal layer to establish controlled impedance for transmission line interconnects and provide an excellent low-inductance path for the return current flow.
- Place the power plane next to the ground plane to create additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Route the slower speed control signals on the bottom layer to allow for greater flexibility as these signal links typically have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep the planes symmetrical. Adding a second plane system to the stack makes the stack mechanically stable and prevents warping. The power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the *Digital Isolator Design Guide*.

8.4.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

8.4.2 Layout Example

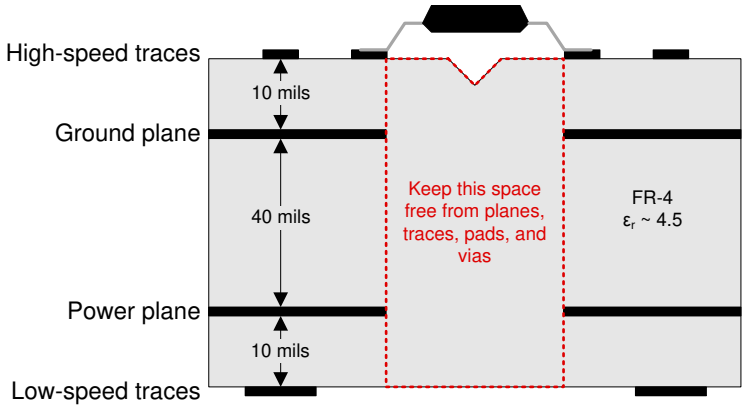


Figure 8-5. Recommended Layer Stack

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9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

For development support, refer to:

- AC-mains LED Lighting with DALI DMX512 & Power Line Communications Reference Design
- Industrial Servo Drive and AC Inverter Drive Reference Design
- Low-Cost Single/Dual-Phase Isolated Electricity Measurement Reference Design
- Noise Tolerant Capacitive Touch HMI Reference Design
- Type 2 PoE PSE, 6kV Lightning Surge Reference Design

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Isolation Glossary,* application note
- Texas Instruments, *Digital Isolator Design Guide Digital*
- Texas Instruments, *How to use isolation to improve ESD, EFT, and Surge immunity in industrial systems,* application note

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

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DeviceNet™ is a trademark of Open DeviceNet Vendors Association.
TI E2E™ is a trademark of Texas Instruments.
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9.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision T (February 2025) to Revision U (October 2025)	Page
• Deleted 'IEC 60601-1 and GB 4943.1' in the *Features* section	1

- Fixed typos and error in the *Insulation Specifications* section....4
- Changed 'Plan to certify' with 'Certified' in all 3 places in the 2nd row in the *Safety-Related Certifications* section.... 4
- Changed 'Certificate planned' with 'Basic certificate: 40047657' in VDE column, 'Master contract number: 220991' in CSA column, and 'File number: E181974' in UL column in the *Safety-Related Certifications* section 4

Changes from Revision S (January 2025) to Revision T (February 2025) **Page**

- Added links to safety-related certifications to the *Features* section....1
- Updated the numbering format for tables, figures, and cross-references throughout the document.... 1

Changes from Revision R (October 2024) to Revision S (January 2025) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document.... 1
- Updated the first page graphic and description to improve accuracy....1
- Updated the links in the *Related Documentation* section....27

Changes from Revision Q (August 2018) to Revision R (October 2024) **Page**

- Updated reference from capacitive isolation to isolation barrier throughout the document....1
- Updated the numbering format for tables, figures, and cross-references throughout the document.... 1
- Updated Thermal Characteristics, Safety Limiting Values, and Thermal Derating Curves to provide more accurate system-level thermal calculations....4
- Updated electrical and switching characteristics to match device performance....12

Changes from Revision P (August 2018) to Revision Q (January 2021) **Page**

- Removed nominal specifications in the RECOMMENDED OPERATING CONDITIONS table....5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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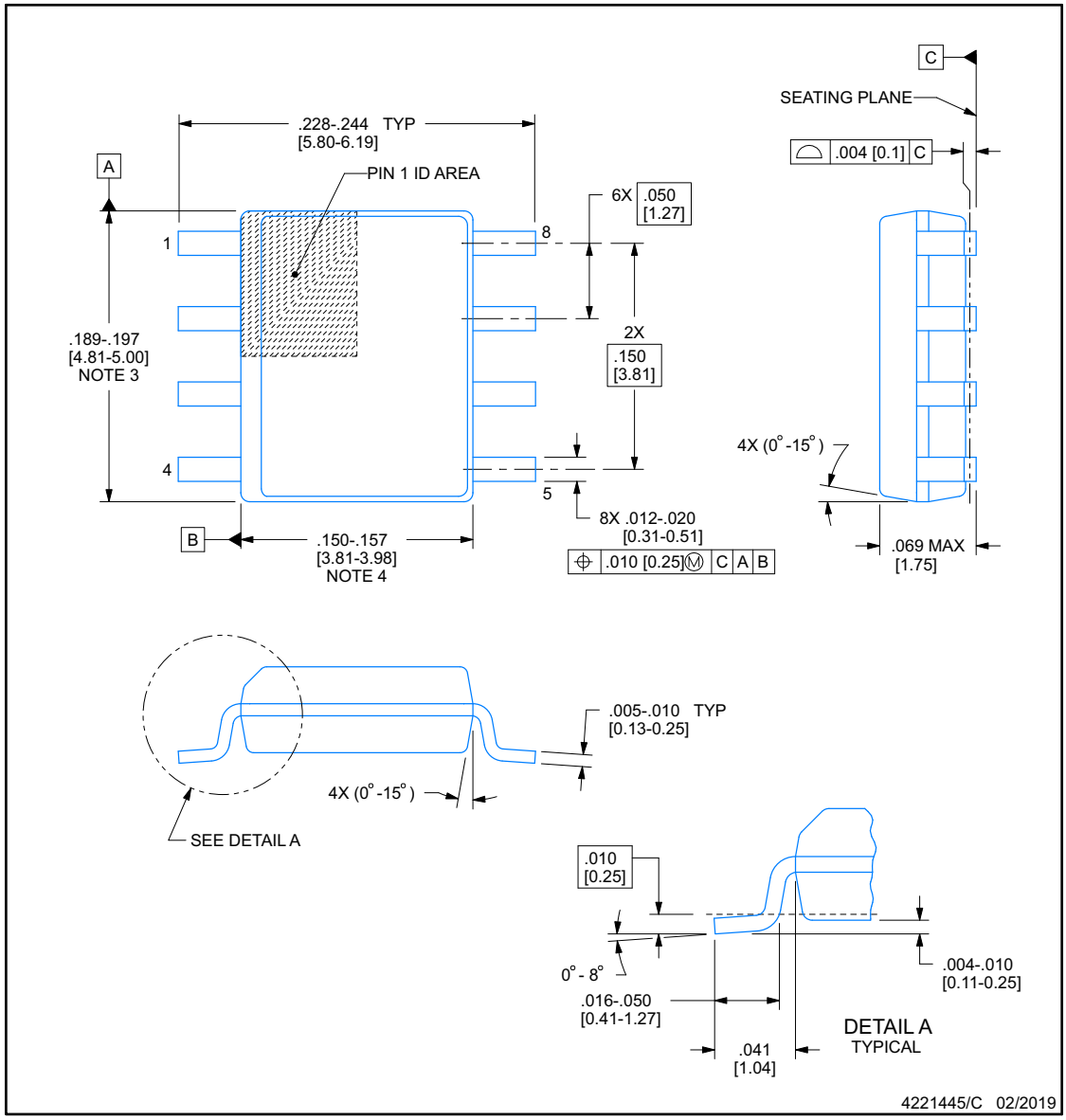


PACKAGE OUTLINE

D0008B

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15], per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

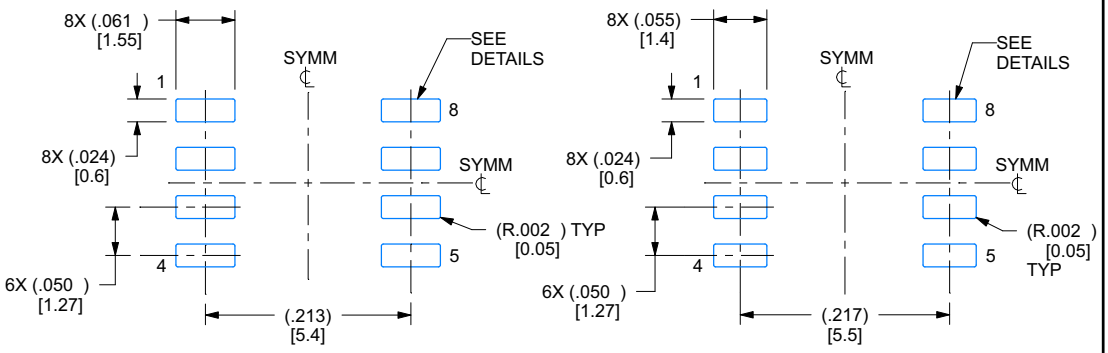
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EXAMPLE BOARD LAYOUT

D0008B

SOIC - 1.75 mm max height

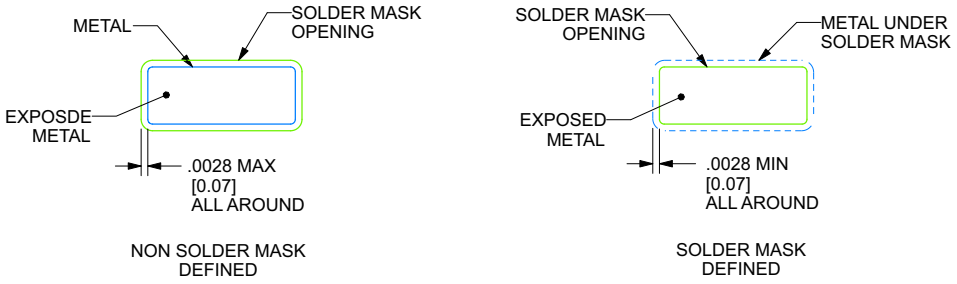
SMALL OUTLINE INTEGRATED CIRCUIT



IPC-7351 NOMINAL
.150 [3.85] CLEARANCE / CREEPAGE

HV / ISOLATION OPTION
.162 [4.1] CLEARANCE / CREEPAGE

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4221445/C 02/2019

NOTES: (continued)

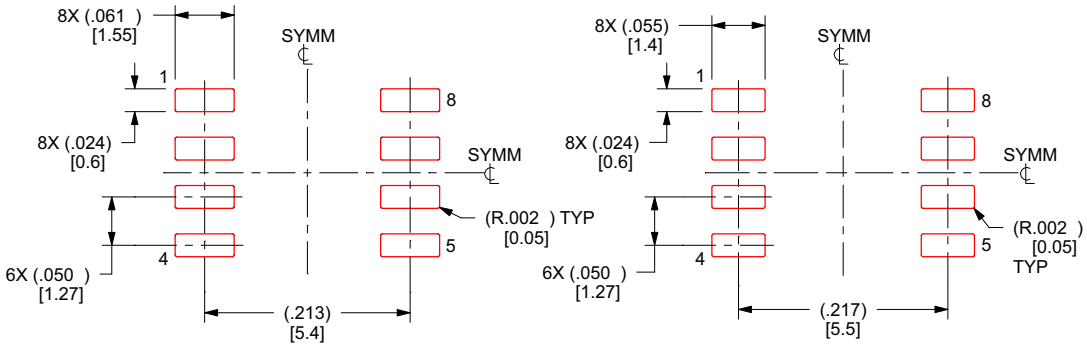
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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EXAMPLE STENCIL DESIGN

D0008B — **SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



IPC-7351 NOMINAL
.150 [3.85] CLEARANCE / CREEPAGE

HV / ISOLATION OPTION
.162 [4.1] CLEARANCE / CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:6X

4221445/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO7220ADR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220A
ISO7220ADR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220A
ISO7220ADRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220A
ISO7220BD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	I7220B
ISO7220BDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220B
ISO7220BDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220B
ISO7220CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220C
ISO7220CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220C
ISO7220MD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	I7220M
ISO7220MDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220M
ISO7220MDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220M
ISO7220MDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220M
ISO7221AD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	I7221A
ISO7221ADR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221A
ISO7221ADR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221A
ISO7221ADRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221A
ISO7221BDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221B
ISO7221BDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221B
ISO7221BDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221B
ISO7221CD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	I7221C
ISO7221CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221C
ISO7221CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221C
ISO7221CDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221C
ISO7221MD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	I7221M
ISO7221MDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221M
ISO7221MDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221M

(1) **Status:** For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF ISO7220A, ISO7221A, ISO7221C :

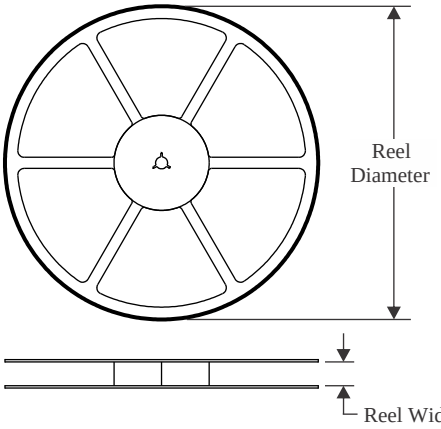
- Automotive : ISO7220A-Q1, ISO7221A-Q1, ISO7221C-Q1

NOTE: Qualified Version Definitions:

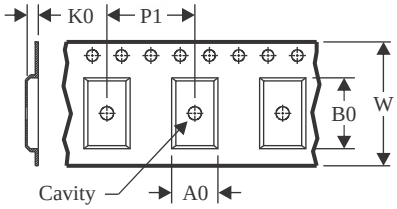
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

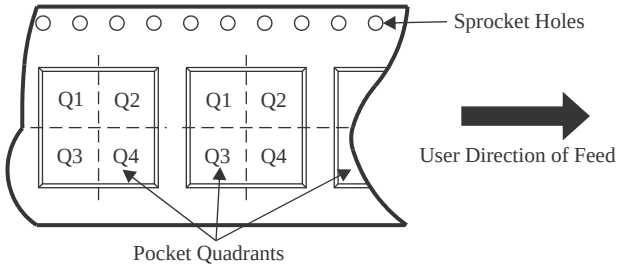


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

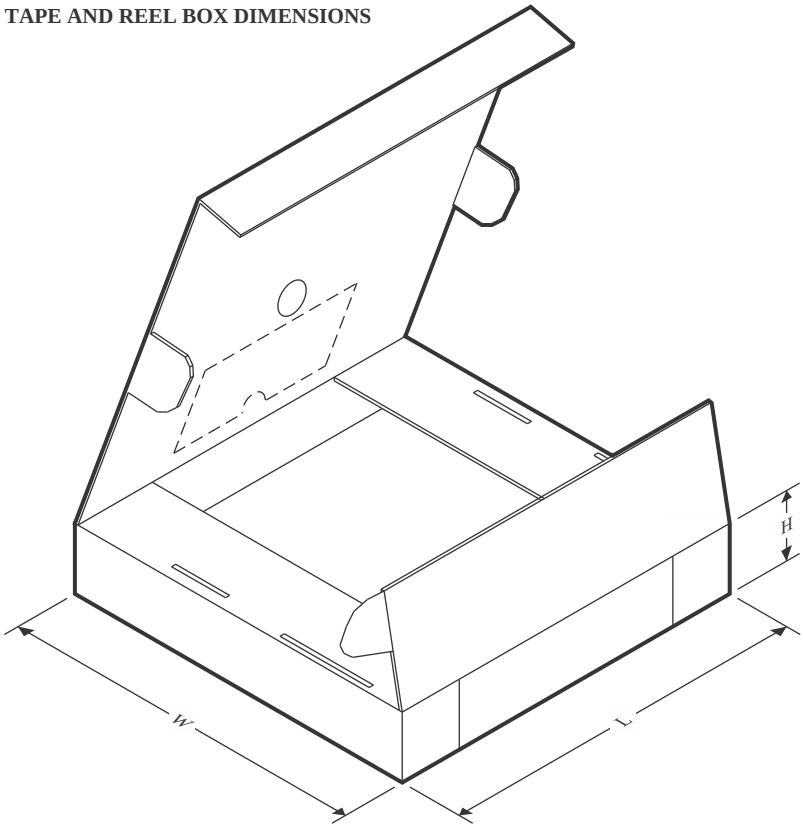
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

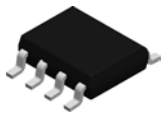
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7220ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7220BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7220CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7220CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7220MDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7221ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7221BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7221CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7221MDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7220ADR	SOIC	D	8	2500	350.0	350.0	43.0
ISO7220BDR	SOIC	D	8	2500	350.0	350.0	43.0
ISO7220CDR	SOIC	D	8	2500	353.0	353.0	32.0
ISO7220CDR	SOIC	D	8	2500	350.0	350.0	43.0
ISO7220MDR	SOIC	D	8	2500	350.0	350.0	43.0
ISO7221ADR	SOIC	D	8	2500	350.0	350.0	43.0
ISO7221BDR	SOIC	D	8	2500	350.0	350.0	43.0
ISO7221CDR	SOIC	D	8	2500	350.0	350.0	43.0
ISO7221MDR	SOIC	D	8	2500	350.0	350.0	43.0

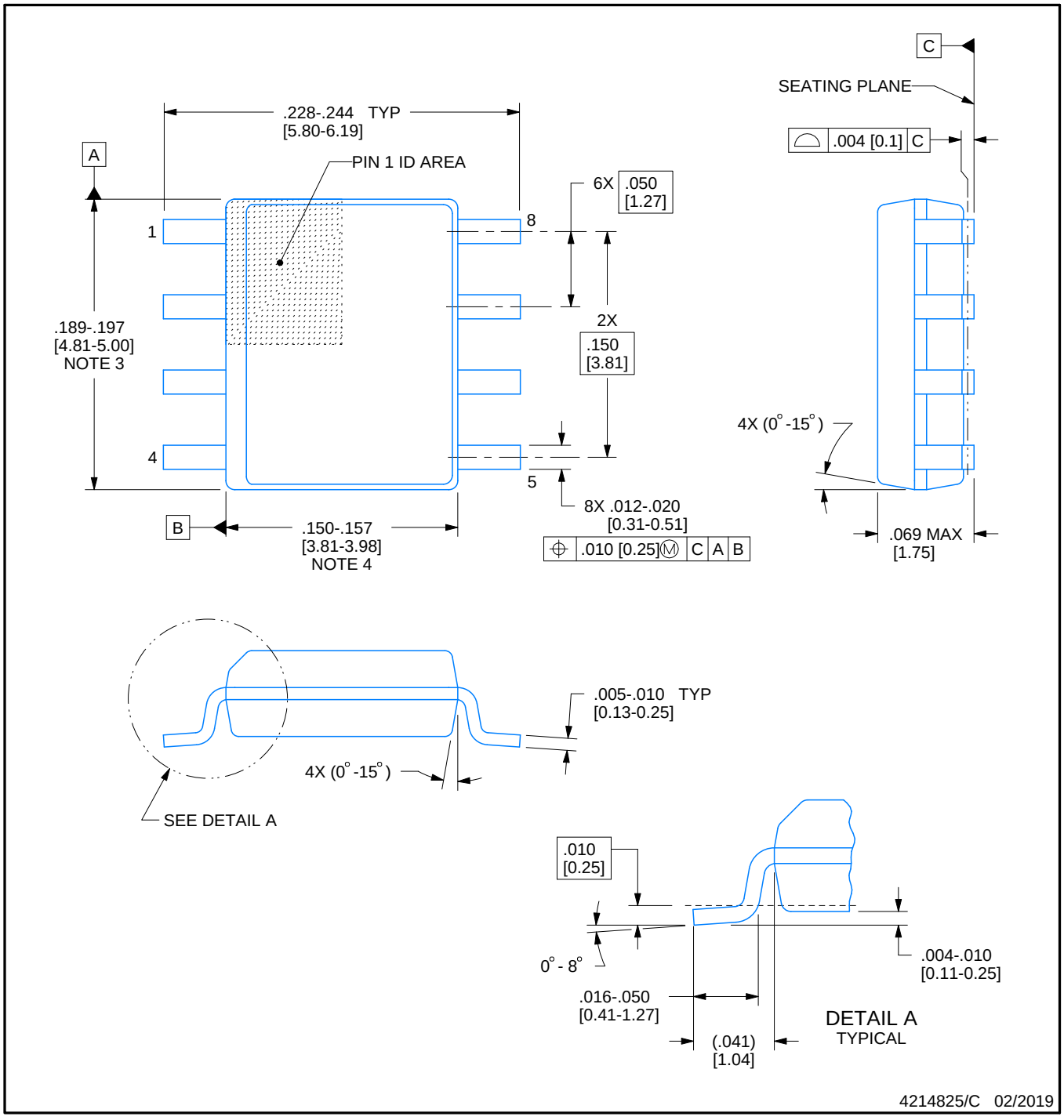


PACKAGE OUTLINE

D0008A

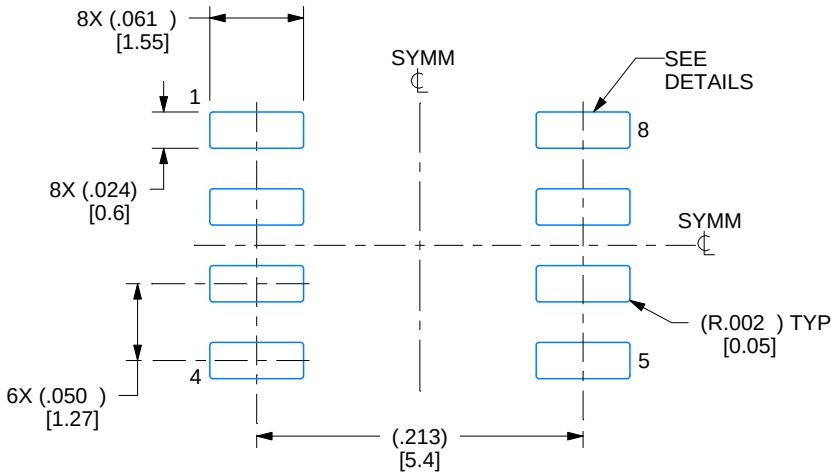
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

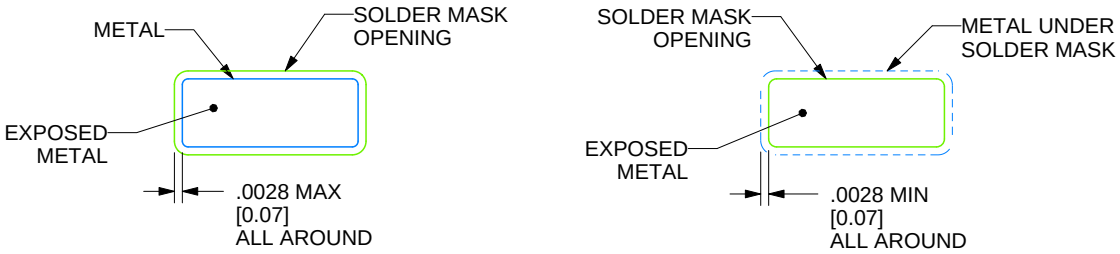


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

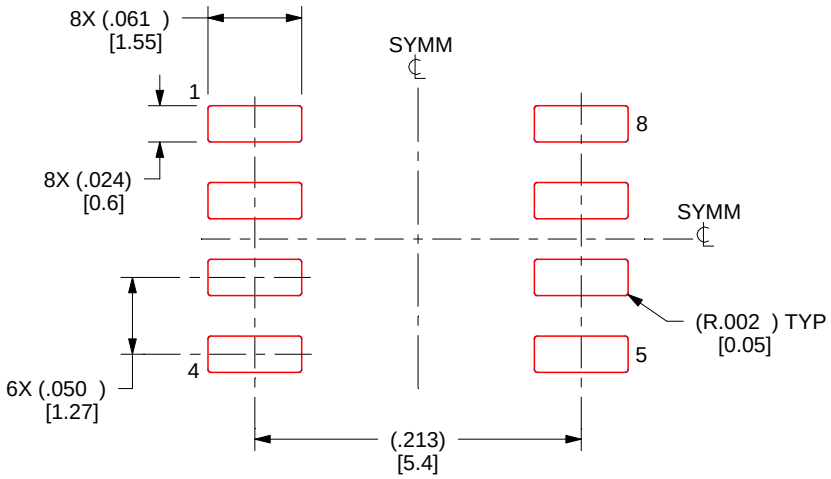
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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