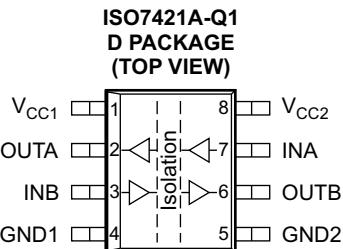


LOW-POWER DUAL DIGITAL ISOLATORS

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
 - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
 - Device HBM ESD Classification Level H3A
 - Device CDM ESD Classification Level C5
- High Signaling Rate: 50 Mbps
- Low Power Consumption
- Low Propagation Delay – 9 ns (Typical)
- Low Skew – 300 ps (Typical)
- 4-kVpeak Maximum Isolation, 2.5 kVrms per UL 1577, IEC/VDE and CSA Approved, IEC 60950-1, IEC 61010-1 End Equipment Standards Approved. All Approvals Pending.
- 50 kV/ μs Transient Immunity (Typical)
- Over 25-Year Isolation Integrity at Rated Voltage
- Operates From 3-V to 5.5-V Supply and Logic Levels



DESCRIPTION

The ISO7421A-Q1 provides galvanic isolation up to 2.5 kVrms for 1 minute per UL. This digital isolator has two isolated channels with bidirectional channel configuration. Each isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO_2) insulation barrier. Used in conjunction with isolated power supplies, these devices prevent noise currents on a data bus or other circuit from entering the local ground and interfering with or damaging sensitive circuitry.

The devices have TTL input thresholds and require two supply voltages from 3 V to 5.5 V, or any combination. All inputs are 5-V tolerant when supplied from a 3-V supply.

ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE ⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	SOIC – D	Reel of 2500	ISO7421AQDRQ1

(1) For the most-current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
GND1	4	–	Ground connection for V_{CC1}
GND2	5	–	Ground connection for V_{CC2}
INA	7	I	Input, channel A
INB	3	I	Input, channel B
OUTA	2	O	Output, channel A
OUTB	6	O	Output, channel B
V_{CC1}	1	–	Power supply, V_{CC1}
V_{CC2}	8	–	Power supply, V_{CC2}

Table 1. FUNCTION TABLE⁽¹⁾

INPUT SIDE VCC	OUTPUT SIDE VCC	INPUT IN	OUTPUT OUT
PU	PU	H	H
		L	L
		Open	H
PD	PU	X	H

(1) PU = Powered up ($V_{CC} \geq 3$ V), PD = Powered down ($V_{CC} \leq 2.4$ V),
X = Irrelevant, H = High level, L = Low level

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

V_{CC}	Supply voltage ⁽²⁾ , V_{CC1} , V_{CC2}	–0.5 V to 6 V	
V_I	Voltage at IN, OUT	–0.5 V to 6 V	
I_O	Output current	±15 mA	
ESD Electrostatic discharge	Human-body model (HBM) AEC-Q100 Classification Level H3A	All pins	4 kV
	Charged-device model (CDM) AEC-Q100 Classification Level C5		1.5 kV
	Machine model (MM)		200 V
$T_{J(Max)}$	Maximum junction temperature	150°C	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V_{CC1} , V_{CC2}	Supply voltage	3	5.5	6	V
I_{OH}	High-level output current	–4			mA
I_{OL}	Low-level output current			4	mA
V_{IH}	High-level input voltage	2	V_{CC}	6	V
V_{IL}	Low-level input voltage	0	0.8	2	V
T_A	Operating temperature	–40	125	150	°C

ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2} = 5 \text{ V} \pm 10\%$, $T_A = -40^\circ\text{C}$ to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -4 \text{ mA}$, see Figure 1	$V_{CC} - 0.8$	4.6		V
		$I_{OH} = -20 \mu\text{A}$, see Figure 1	$V_{CC} - 0.1$	5		
V_{OL}	Low-level output voltage	$I_{OL} = 4 \text{ mA}$, see Figure 1		0.2	0.4	V
		$I_{OL} = 20 \mu\text{A}$, see Figure 1		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis			400		mV
I_{IH}	High-level input current	IN from 0 V or V_{CC}			10	μA
I_{IL}	Low-level input current			-10		μA
C_I	Input capacitance to ground	IN at V_{CC} , $V_I = 0.4 \sin (4E6\pi t)$		1.2		pF
CMTI	Common-mode transient immunity	$V_I = V_{CC}$ or 0 V, see Figure 3	25	50		kV/ μs

SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic I_{CC} measurement)

I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: $V_I = V_{CC}$ or 0 V AC Input: $C_L = 15 \text{ pF}$	2.3	3.6	mA	
I_{CC2}				2.3	3.6		
I_{CC1}		10 Mbps	$C_L = 15 \text{ pF}$	2.9	4.5		
I_{CC2}				2.9	4.5		
I_{CC1}		25 Mbps		4.3	6		
I_{CC2}				4.3	6		
I_{CC1}		50 Mbps		6	9.1		
I_{CC2}				6	9.1		

SWITCHING CHARACTERISTICS

$V_{CC1} = V_{CC2} = 5 \text{ V} \pm 10\%$, $T_A = -40^\circ\text{C}$ to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1		9	14	ns
PWD ⁽¹⁾	Pulse duration distortion $ t_{PHL} - t_{PLH} $			0.3	3.7	ns
$t_{sk(pp)}$	Part-to-part skew time				4.9	ns
$t_{sk(0)}$	Channel-to-channel output skew time				3.6	ns
t_r	Output signal rise time	See Figure 1		1		ns
t_f	Output signal fall time			1		ns
t_{fs}	Fail-safe output delay time from input power loss	See Figure 2		6		μs
t_{ui}	Input pulse duration		7			ns
$1 / t_{ui}$	Signaling rate		0		50	Mbps

(1) Also known as pulse skew

ELECTRICAL CHARACTERISTICS

 $V_{CC1} = 5 \text{ V} \pm 10\%$, $V_{CC2} = 3.3 \text{ V} \pm 10\%$, $T_A = -40^\circ\text{C}$ to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
V_{OH}	High-level output voltage	$I_{OH} = -4 \text{ mA}$, see Figure 1 , 5-V side	$V_{CC} - 0.8$		V		
		$I_{OH} = -20 \mu\text{A}$, see Figure 1	$V_{CC} - 0.1$				
V_{OL}	Low-level output voltage	$I_{OL} = 4 \text{ mA}$, see Figure 1	0.4		0.1	V	
		$I_{OL} = 20 \mu\text{A}$, see Figure 1					
$V_{I(HYS)}$	Input threshold voltage hysteresis		400		mV		
I_{IH}	High-level input current	IN from 0 V or V_{CC}	10		μA		
I_{IL}	Low-level input current		-10		μA		
C_I	Input capacitance to ground	IN at V_{CC} , $V_I = 0.4 \sin(4E6\pi t)$	1.2		pF		
CMTI	Common-mode transient immunity	$V_I = V_{CC}$ or 0 V, see Figure 3	25	40	$\text{kV}/\mu\text{s}$		

SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic I_{CC} measurement)

I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: $V_I = V_{CC}$ or 0 V	2.3	3.6	mA
I_{CC2}			AC Input: $C_L = 15 \text{ pF}$	1.8	2.8	
I_{CC1}		10 Mbps		2.9	4.5	
I_{CC2}				2.2	3.2	
I_{CC1}		25 Mbps		4.3	6	
I_{CC2}				2.8	4.1	
I_{CC1}		50 Mbps		6	9.1	
I_{CC2}				3.8	5.8	

SWITCHING CHARACTERISTICS

 $V_{CC1} = 5 \text{ V} \pm 10\%$, $V_{CC2} = 3.3 \text{ V} \pm 10\%$, $T_A = -40^\circ\text{C}$ to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1	10	17	ns	
PWD ⁽¹⁾	Pulse duration distortion $ t_{PHL} - t_{PLH} $		0.5	5.6	ns	
$t_{sk(pp)}$	Part-to-part skew time			6.3	ns	
$t_{sk(0)}$	Channel-to-channel output skew time			4	ns	
t_r	Output signal rise time	See Figure 1	2		ns	
t_f	Output signal fall time		2		ns	
t_{fs}	Fail-safe output delay time from input power loss	See Figure 2	6		μs	
t_{ui}	Input pulse duration		7		ns	
$1 / t_{ui}$	Signaling rate		0	50	Mbps	

(1) Also known as pulse skew

ELECTRICAL CHARACTERISTICS

$V_{CC1} = 3.3 \text{ V} \pm 10\%$, $V_{CC2} = 5 \text{ V} \pm 10\%$, $T_A = -40^\circ\text{C}$ to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -4 \text{ mA}$, see Figure 1 , 3.3-V side	$V_{CC} - 0.4$			V
		$I_{OH} = -20 \mu\text{A}$, see Figure 1	$V_{CC} - 0.1$			
V_{OL}	Low-level output voltage	$I_{OL} = 4 \text{ mA}$, see Figure 1		0.4		V
		$I_{OL} = 20 \mu\text{A}$, see Figure 1		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis			400		mV
I_{IH}	High-level input current	IN from 0 V or V_{CC}			10	μA
I_{IL}	Low-level input current			-10		μA
C_I	Input capacitance to ground	IN at V_{CC} , $V_I = 0.4 \sin(4E6\pi t)$		1		pF
CMTI	Common-mode transient immunity	$V_I = V_{CC}$ or 0 V, see Figure 3	25	40		kV/ μs

SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic I_{CC} measurement)

I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: $V_I = V_{CC}$ or 0 V	1.8	2.8	mA
I_{CC2}			AC Input: $C_L = 15 \text{ pF}$	2.3	3.6	
I_{CC1}		10 Mbps		2.2	3.2	
I_{CC2}				2.9	4.5	
I_{CC1}		25 Mbps		2.8	4.1	
I_{CC2}				4.3	6	
I_{CC1}		50 Mbps		3.8	5.8	
I_{CC2}				6	9.1	

SWITCHING CHARACTERISTICS

$V_{CC1} = 3.3 \text{ V} \pm 10\%$, $V_{CC2} = 5 \text{ V} \pm 10\%$, $T_A = -40^\circ\text{C}$ to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1		10	17	ns
PWD ⁽¹⁾	Pulse duration distortion $ t_{PHL} - t_{PLH} $			0.5	4	ns
$t_{sk(pp)}$	Part-to-part skew time				8.5	ns
$t_{sk(0)}$	Channel-to-channel output skew time				4	ns
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time			2		ns
t_{fs}	Fail-safe output delay time from input power loss	See Figure 2		6		μs
t_{ui}	Input pulse duration		7			ns
$1 / t_{ui}$	Signaling rate		0	50		Mbps

(1) Also known as pulse skew

ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2} = 3.3 \text{ V} \pm 5\%$, $T_A = -40^\circ\text{C}$ to 125°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH} High-level output voltage	$I_{OH} = -4 \text{ mA}$, see Figure 1	$V_{CC} - 0.4$	3		V
	$I_{OH} = -20 \mu\text{A}$, see Figure 1	$V_{CC} - 0.1$	3.3		
V_{OL} Low-level output voltage	$I_{OL} = 4 \text{ mA}$, see Figure 1		0.2	0.4	V
	$I_{OL} = 20 \mu\text{A}$, see Figure 1		0	0.1	
$V_{I(HYS)}$ Input threshold voltage hysteresis			400		mV
I_{IH} High-level input current	IN from 0 V or V_{CC}			10	μA
I_{IL} Low-level input current			-10		μA
C_I Input capacitance to ground	IN at V_{CC} , $V_I = 0.4 \sin(4E6\pi t)$		1		pF
CMTI Common-mode transient immunity	$V_I = V_{CC}$ or 0 V, see Figure 3 .	25	40		kV/ μs

SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic I_{CC} measurement)

I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: $V_I = V_{CC}$ or 0 V	1.8	2.8	mA
I_{CC2}			AC Input: $C_L = 15 \text{ pF}$	1.8	2.8	
I_{CC1}		10 Mbps		2.2	3.2	
I_{CC2}				2.2	3.2	
I_{CC1}		25 Mbps		2.8	4.1	
I_{CC2}				2.8	4.1	
I_{CC1}		50 Mbps		3.8	5.8	
I_{CC2}				3.8	5.8	

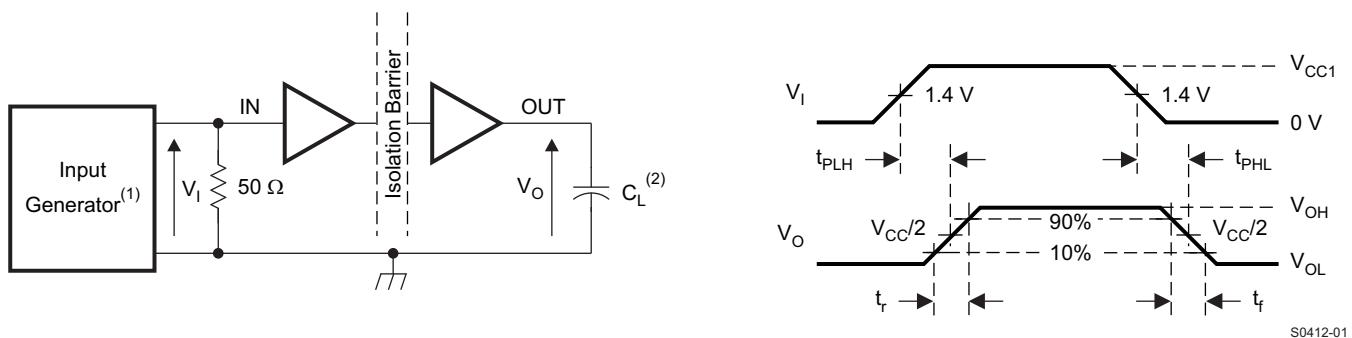
SWITCHING CHARACTERISTICS

$V_{CC1} = V_{CC2} = 3.3 \text{ V} \pm 5\%$, $T_A = -40^\circ\text{C}$ to 125°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL} Propagation delay time	See Figure 1		12	20	ns
PWD ⁽¹⁾ Pulse duration distortion $ t_{PHL} - t_{PLH} $			1	5	ns
$t_{sk(pp)}$ Part-to-part skew time				6.8	ns
$t_{sk(0)}$ Channel-to-channel output skew time				5.5	ns
t_r Output signal rise time	See Figure 1		2		ns
t_f Output signal fall time			2		ns
t_{fs} Fail-safe output delay time from input power loss	See Figure 2		6		μs
t_{ui} Input pulse duration			7		ns
$1 / t_{ui}$ Signaling rate			0	50	Mbps

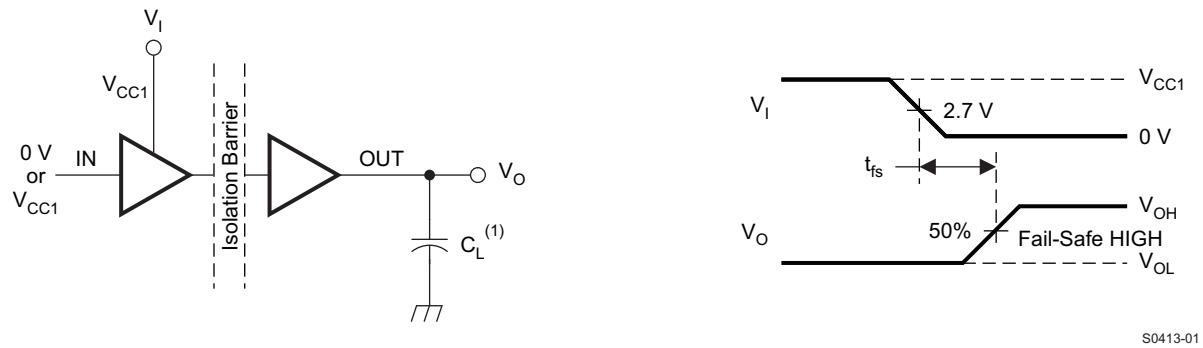
(1) Also known as pulse skew

PARAMETER MEASUREMENT INFORMATION



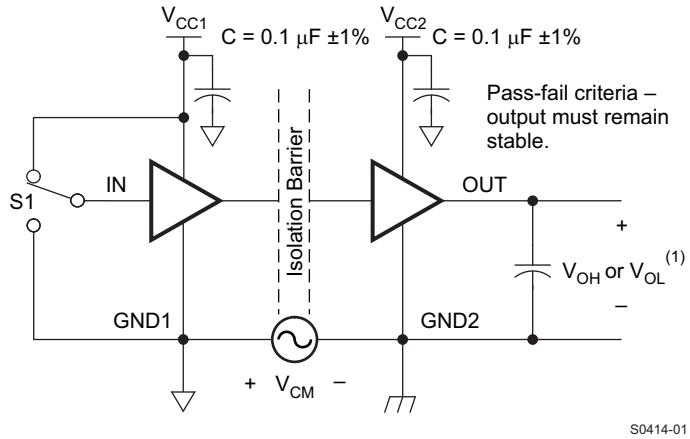
(1) The input pulse is supplied by a generator having the following characteristics: PRR \leq 50 kHz, 50% duty cycle, $t_r \leq 3$ ns, $t_f \leq 3$ ns, $Z_O = 50 \Omega$.
(2) $C_L = 15 \text{ pF}$ and includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 1. Switching Characteristic Test Circuit and Voltage Waveforms



(1) $C_L = 15 \text{ pF}$ and includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 2. Fail-Safe Output Delay-Time Test Circuit and Voltage Waveforms



(1) $C_L = 15 \text{ pF}$ and includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 3. Common-Mode Transient Immunity Test Circuit

DEVICE INFORMATION

PACKAGE CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01) Minimum air gap (clearance)	Shortest terminal-to-terminal distance through air	4.8			mm
L(I02) Minimum external tracking (creepage)	Shortest terminal-to-terminal distance across the package surface	4.3			mm
CTI Tracking resistance (comparative tracking index)	DIN IEC 60112 / VDE 0303 Part 1	>175			V
Minimum internal gap (internal clearance)	Distance through the insulation	0.008			mm
R _{IO} Isolation resistance	Input to output, V _{IO} = 500 V, all pins on each side of the barrier tied together creating a two-terminal device, T _A < 100°C		>10 ¹²		Ω
	Input to output		>10 ¹¹		Ω
C _{IO} Barrier capacitance, input to output	V _I = 0.4 sin (4E6πt)		1		pF

NOTE

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

Creepage and clearance on a printed-circuit board become equal according to the measurement techniques shown in the Isolation Glossary. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

INSULATION CHARACTERISTICS⁽¹⁾

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SPECIFICATION	UNIT
V _{IORM} Maximum working insulation voltage		560	V
V _{PR} Input-to-output test voltage	t = 1 s (100% production), partial discharge 5 pC	1050	V
V _{IOTM} Transient overvoltage	t = 60 s (qualification)	4000	V
	t = 1 s (100% production)		
V _{ISO} Isolation voltage per UL	t = 60 s (qualification)	2500	Vrms
	t = 1 s (100% production)	3000	
R _S Insulation resistance	V _{IO} = 500 V at T _S	>10 ⁹	Ω
Pollution degree		2	

(1) Climatic Classification 40/125/21

Table 2. IEC 60664-1 RATINGS TABLE

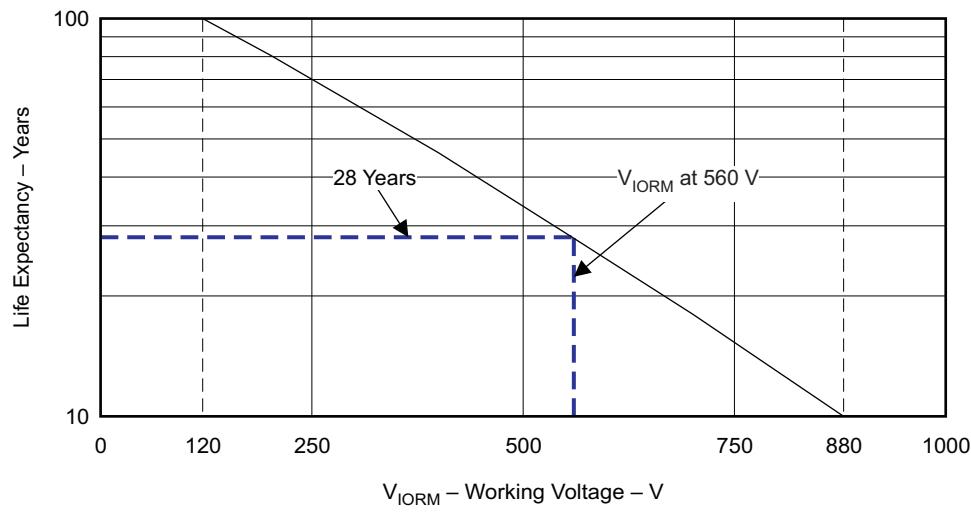
PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	III-a
Installation classification	Rated mains voltage ≤ 150 Vrms	I-IV
	Rated mains voltage ≤ 300 Vrms	I-III
	Rated mains voltage ≤ 400 Vrms	I-II

REGULATORY INFORMATION

VDE	CSA	UL
Certified according to IEC 60747-5-2	Approved under CSA Component Acceptance Notice	Recognized under 1577 Component Recognition Program ⁽¹⁾
File number: pending (40016131)	File number: pending (1698195)	File number: pending (E181974)

(1) Production tested ≥ 3000 Vrms for 1 second in accordance with UL 1577.

LIFE EXPECTANCY versus WORKING VOLTAGE



G001

Figure 4. Life Expectancy versus Working Voltage

IEC SAFETY LIMITING VALUES

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S Safety input, output, or supply current	$\theta_{JA} = 212^\circ\text{C}/\text{W}$, $V_I = 5.5 \text{ V}$, $T_J = 170^\circ\text{C}$, $T_A = 25^\circ\text{C}$			112	mA
	$\theta_{JA} = 212^\circ\text{C}/\text{W}$, $V_I = 3.6 \text{ V}$, $T_J = 170^\circ\text{C}$, $T_A = 25^\circ\text{C}$			171	
T_S Maximum case temperature				150	°C

The safety-limiting constraint is the absolute-maximum junction temperature specified in the *Absolute Maximum Ratings* table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Characteristics* table is that of a device installed in the JESD51-3, Low-Effective-Thermal-Conductivity Test Board for Leaded Surface-Mount Packages and is conservative. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

PACKAGE THERMAL CHARACTERISTICS

(over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA} Junction-to-air thermal resistance	Low-K thermal resistance ⁽¹⁾	212			°C/W
	High-K thermal resistance ⁽¹⁾	122			
θ_{JB} Junction-to-board thermal resistance		37			°C/W
θ_{JC} Junction-to-case thermal resistance		69.1			°C/W
P_D Device power dissipation	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150^\circ\text{C}$, $C_L = 15$ pF, Input a 150-Mbps 50% duty-cycle square wave		390		mW

(1) Tested in accordance with the low-K or high-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages

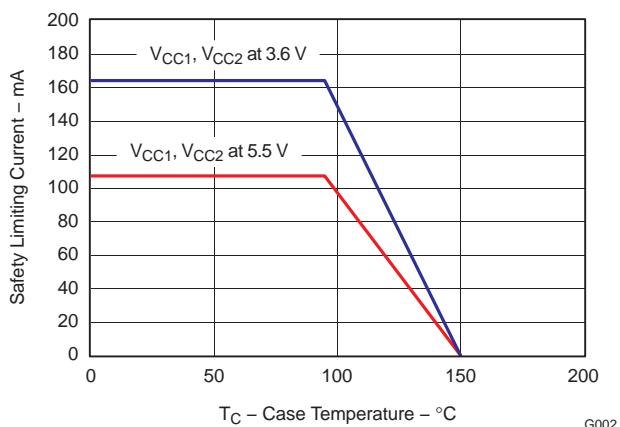


Figure 5. θ_{JC} Thermal Derating Curve per IEC 60747-5-2

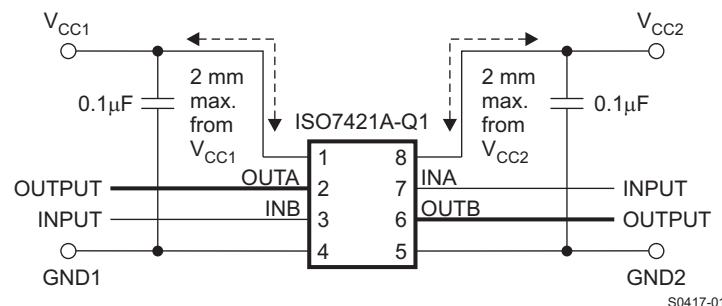


Figure 6. Typical ISO7421A-Q1 Application Circuit

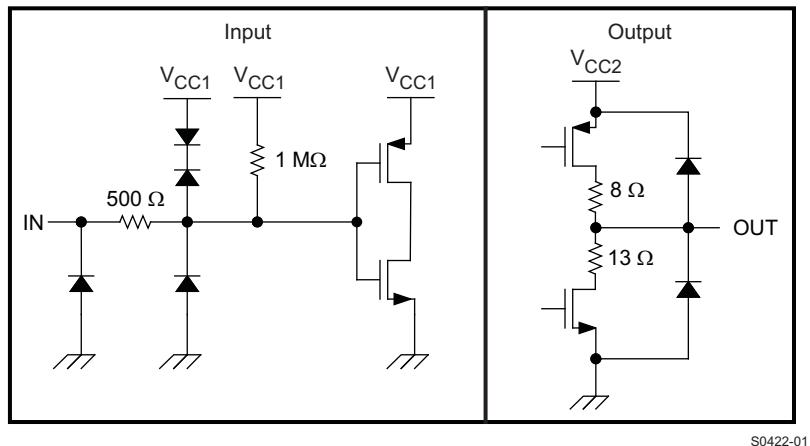
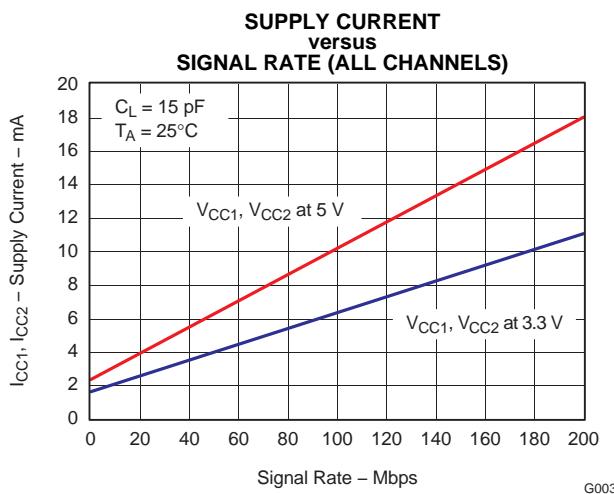
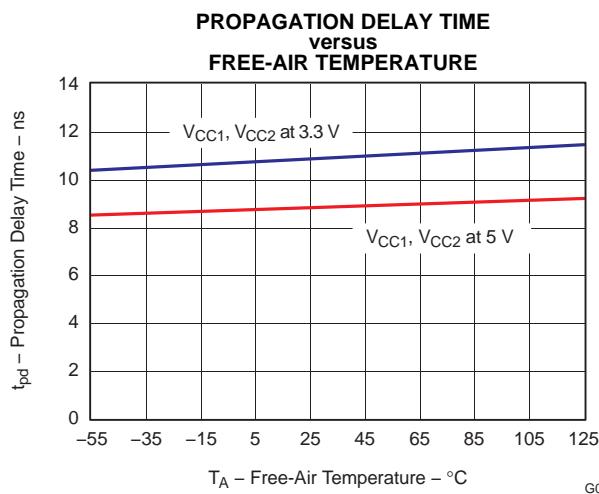
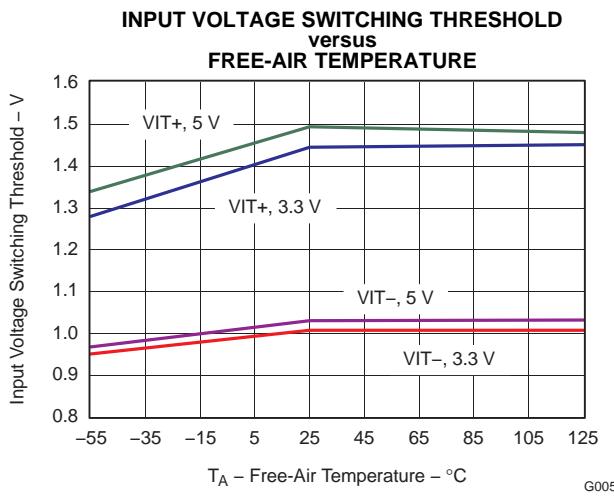
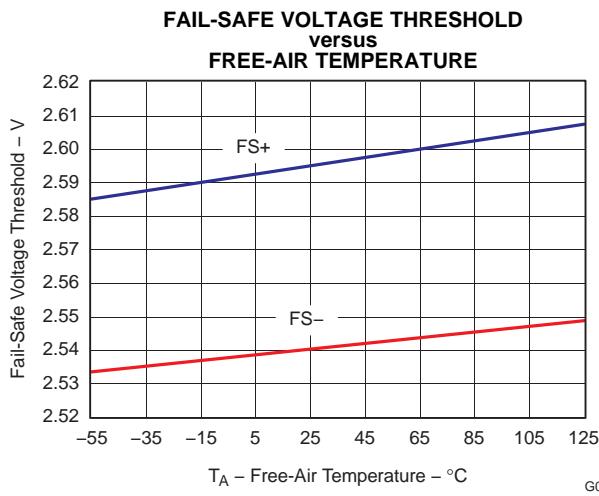
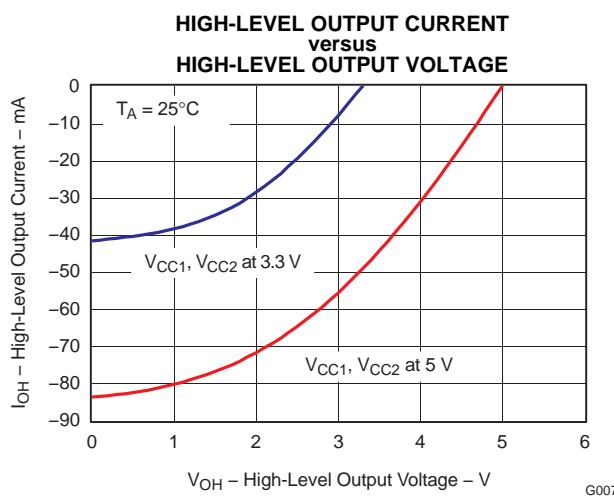
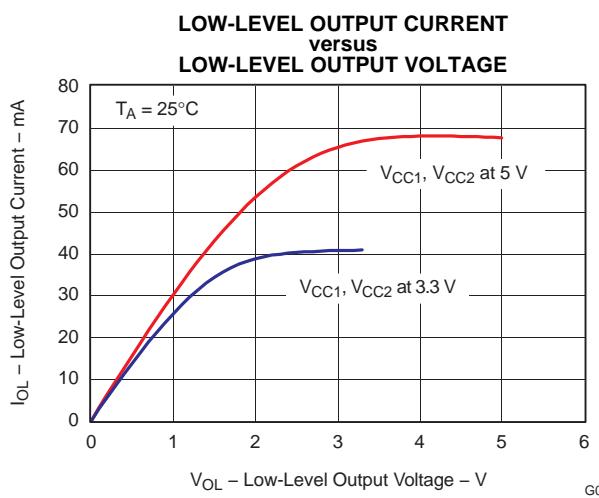


Figure 7. Device I/O Schematics

TYPICAL CHARACTERISTICS


Figure 8.

Figure 9.

Figure 10.

Figure 11.

Figure 12.

Figure 13.

TYPICAL CHARACTERISTICS (continued)

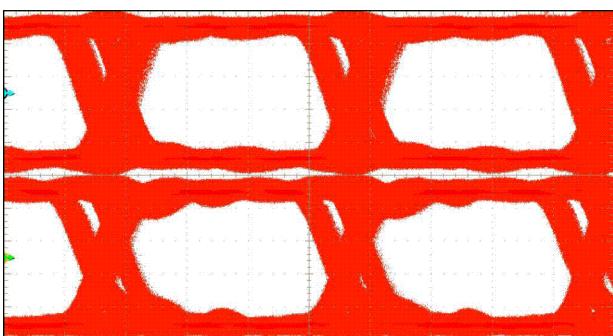


Figure 14. Eye Diagram at 250 MBPS, 5-V V_{CC} , Typical

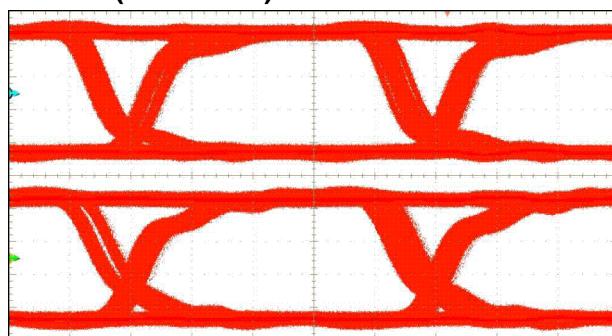


Figure 15. Eye Diagram at 200 MBPS, 5-V V_{CC} , 125°C

REVISION HISTORY

Changes from Revision A (September 2012) to Revision B	Page
• Deleted ISO7420-Q1 part number from header of every page	1
• Deleted ISO7420-Q1 package from pinout drawing	1
• Deleted ISO7420-Q1 part number from Description sectoin	1
• Deleted ISO7420-Q1 from Ordering Information table	1
• Deleted ISO7420-Q1 from Pin Functions table	2
• Deleted ISO7420-Q1 from Supply Current section of 5-V, 5-V Electrical Characteristics table	3
• Deleted ISO7420-Q1 from Supply Current section of 5-V, 3.3-V Electrical Characteristics table	4
•	5
• Deleted ISO7420-Q1 from Supply Current section of 3.3-V, 5-V Electrical Characteristics table	5
• Deleted ISO7420-Q1 from Supply Current section of 3.3-V, 5-V Electrical Characteristics table	6
• Corrected part number in Typical Application Circuit diagram	10

Changes from Original (March, 2012) to Revision A	Page
• Changed High Signaling Rate from 1 to 50 Mbps.	1
• Replaced Supply Current section with marked up table from commercial datasheet SLLSE45, 8.5 max value changed to 9.1.	3
• Changed Signaling rate max value from 1 to 50.	3
• Replaced Supply Current section with marked up table from commercial datasheet SLLSE45, 8.5 max value changed to 9.1 and 5.5 changed to 5.8.	4
• Changed Signaling rate from 1 to 50 Mbps.	4
• Replaced Supply Current section with marked up table from commercial datasheet SLLSE45, 5.5 max value changed to 5.8 and 8.5 changed to 9.1.	5
• Changed Signaling rate from 1 to 50 Mbps.	5
• Replaced Supply Current section with marked up table from commercial datasheet SLLSE45, 5.5 max value changed to 5.8.	6
• Changed Signaling rate from 1 to 50 Mbps.	6

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO7421AQDRQ1	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	7421AQ
ISO7421AQDRQ1.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	7421AQ

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

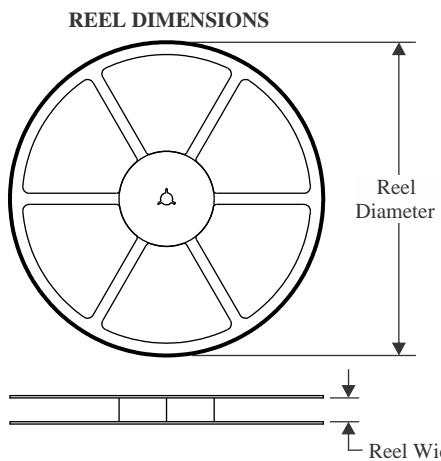
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

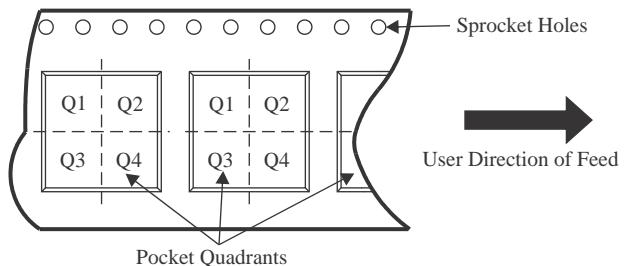
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7421AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

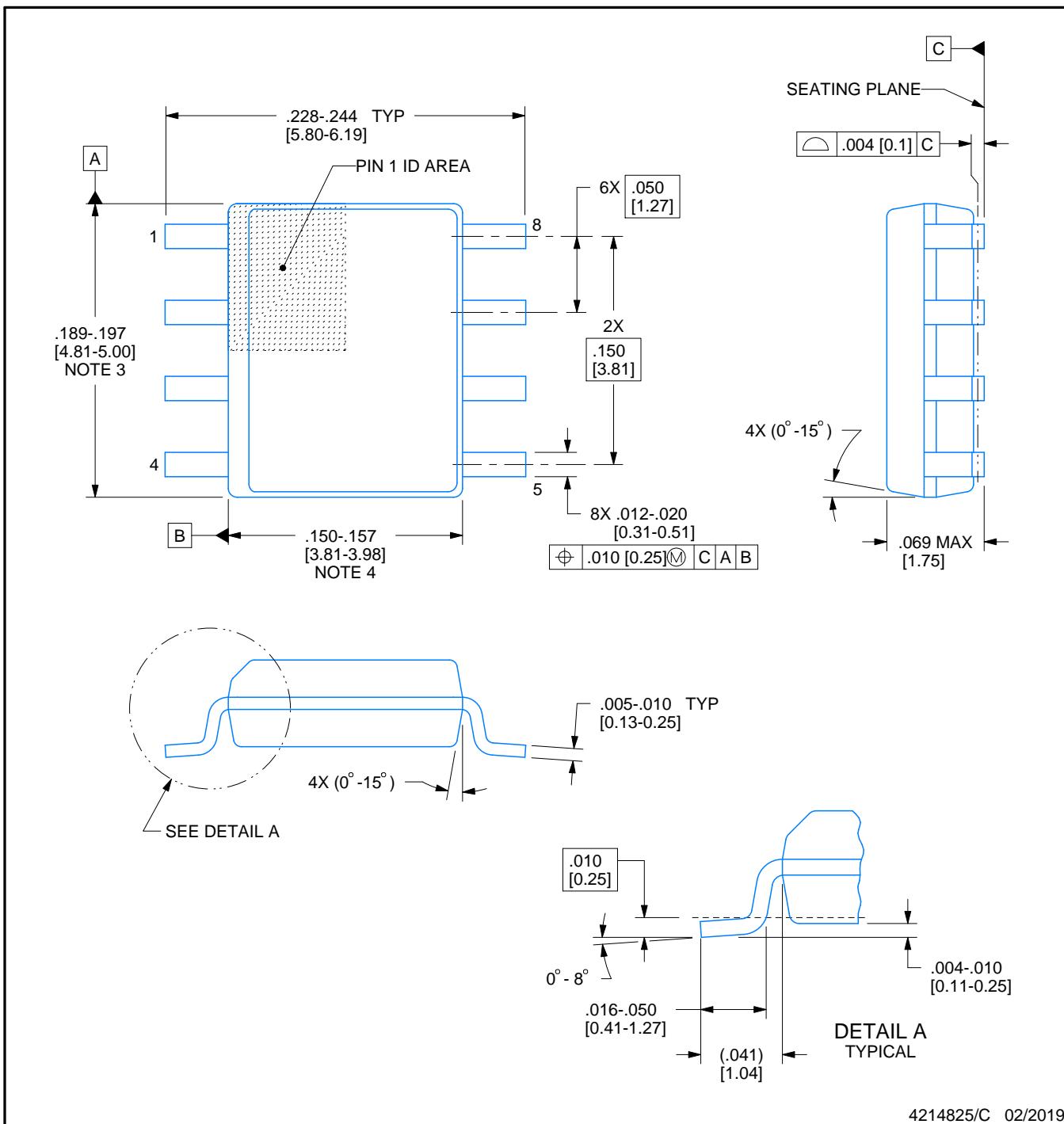
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7421AQDRQ1	SOIC	D	8	2500	350.0	350.0	43.0



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

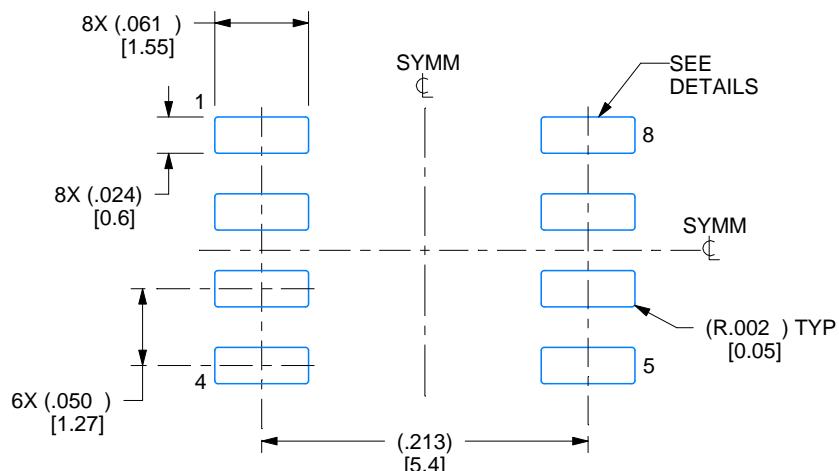
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

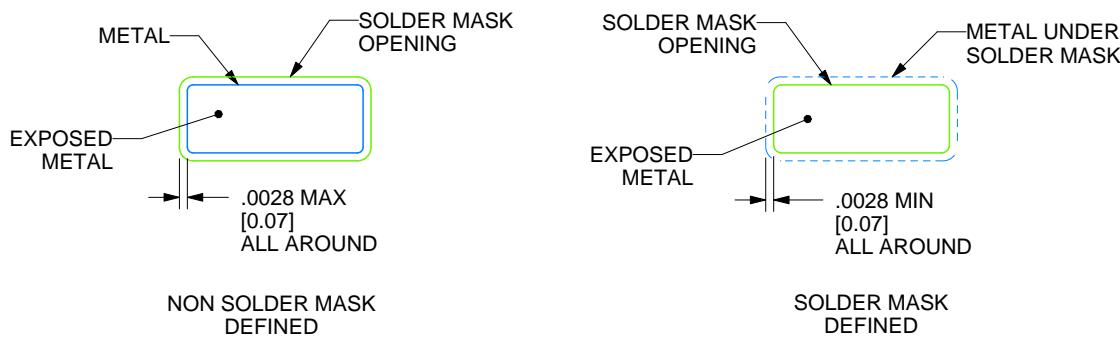
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

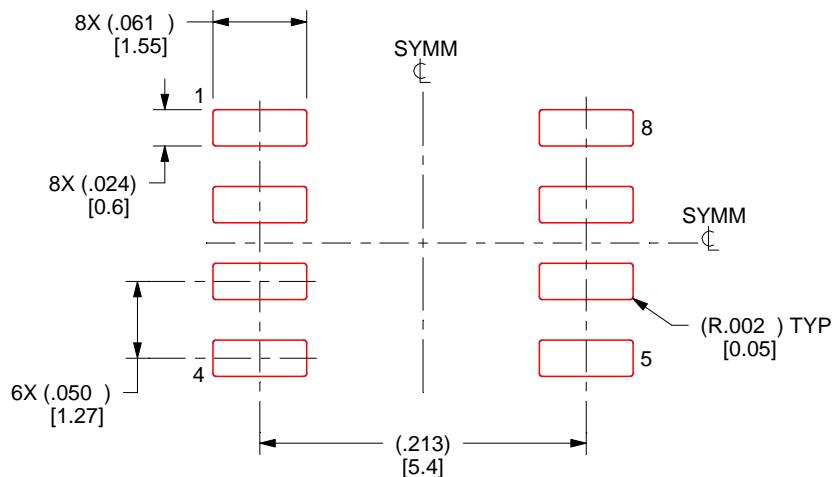
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025