ISOM8610 80V, 150mA Normally Open Opto-emulator Switch With Integrated FETs

1 Features

- Drop-in replacement and pin-to-pin upgrade to industry-standard photorelays
- Single-channel, diode-emulator input
- Single-pole, normally-open, symmetrical 80V output switch
- Primary-side current controlled switch, no additional isolated high voltage supply required for 80V switching
- Ultra-low off-state leakage at V_{OFF} = 70V
  - < 250nA at operating temperature of 25°C
  - < 1µA across operating temperature of –55°C to 125°C
- Fast Response time: 10µs (typical) at I_F = 5mA, V_{CC} = 20V, R_L = 200Ω, C_L = 50pF
- Ultra-low input trigger current of 800µA (at 25°C)
- Robust isolation barrier:
  - Isolation rating: up to 3750V_{RMS}
  - Working voltage: 500V_{RMS}, 707V_{PK}
  - Surge capability: up to 10kV
- Supports Industrial Temperature Range: –55°C to 125°C
- Small SO-4 package
- Safety-related certifications:
  - UL 1577 recognition, 3750V_{RMS} isolation
  - DIN EN IEC 60747-17 (VDE 0884-17) conformity per VDE
  - IEC 62368-1, IEC 61010-1
  - CQC GB 4943.1

2 Applications

- Factory automation and control
- Building automation
- Appliances
- Test and Measurement

3 Description

The ISOM8610 is an 80V single-pole, normally-open switch with an opto-emulator input. The opto-emulator inputs control the back-to-back MOSFETs without any power supply required on the secondary side. The devices are pin-compatible and drop-in replaceable for many traditional optocouplers, allowing enhancement to industry-standard packages with no PCB redesign.

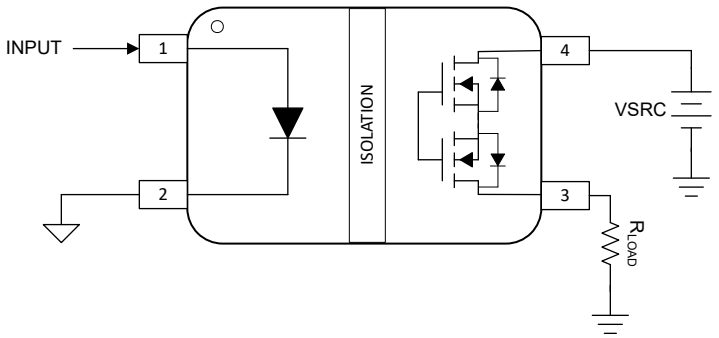
The ISOM8610 opto-emulator switch offers significant reliability and performance advantages compared to optocouplers, like wider temperature ranges and tight process controls resulting in small part-to-part variations. Since there is no aging effect to compensate for, the emulated diode-input stage consumes less power than optocouplers that have LED aging and require higher bias currents over the device lifetime. ISOM8610 switch output can be controlled by just 0.8mA current through anode/cathode pins over the lifetime of the device, enabling system power savings.

The ISOM8610 is offered in a small SO-4 package, supporting a 3.75kV_{RMS} isolation rating. The high performance and reliability of the device enable the devices use in applications like Building automation, Factory automation, Semiconductor test, I/O modules in industrial controllers, factory automation applications, and more spaces.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE (2)	BODY SIZE (NOM)
ISOM8610	DFG (SO, 4)	7.0mm × 3.5mm	4.8mm × 3.5mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Application Example

Table of Contents

4 Pin Configuration and Functions

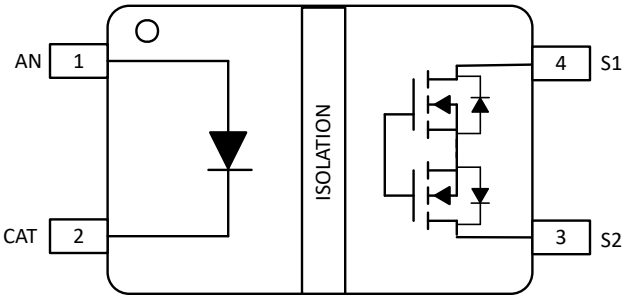


Figure 4-1. ISOM8610 DFG Package, 4-Pin SOIC (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	Description
NAME	NO.		
AN	1	I	Anode connection of diode emulator
CAT	2	I	Cathode connection of diode emulator
S2	3	I/O	Switch input
S1	4	I/O	Switch input

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

See(1) (2)

			MIN	MAX	UNIT
Input	$I_{F(max)}$	LED forward current		50	mA
	V_R	Input reverse voltage at I_R = 10µA		7	V
	P_I	Input power dissipation		100	mW
Output	V_{OFF}	Blocking voltage		80	V
	I_O	Output continuous load current		200	mA
	$\Delta I_O/^oC$	Output continuous load current		-1.1	mA/°C
	I_{OP}	Output pulse current (1µs width)		600	mA
	P_O	Output power dissipation		150	mW
	P_T	Total power dissipation		200	mW
	T_{stg}	Storage temperature	-65	150	°C
	Transient Isolation Voltage	AC Voltage, t=60s		707	V_{RMS}
		DC Voltage, t=60s		1000	V_{DC}

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All specifications are at T_A = 25°C unless otherwise noted

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), ANSI/ESDA/JEDEC JS-002, all pins (2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_A	Ambient temperature	-55		125	°C
T_J	Junction temperature	-55		150	
$I_{F(ON)}$	Input ON-state forward current	0.8		20	mA
I_O	Output continuous load current at I_F=3mA (1)			150	
V_{OFF}	Output Blocking Voltage			70	V
V_{IOWM}	Functional Isolation Working Voltage (AC Voltage, sine wave)			500	V_{RMS}
	Functional Isolation Working Voltage (DC Voltage)			707	V_{DC}

(1) For T_A=25°C, Current available to load must be derated by 1mA/°C for T_A > 25°C

5.4 Thermal Information

THERMAL METRIC(1)		ISOM8610 ISOM8600 DFG 4 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	206.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	96.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	130.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	52.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	127.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)	I_F = 20mA, T_J = 150°C, I_O = 150mA, T_A = 25°C			310	mW
P_{D1}	Maximum power dissipation (side-1)				36	mW
P_{D2}	Maximum power dissipation (side-2)				274	mW

5.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
			4-DFG	
IEC 60664-1				
CLR	External clearance(1)	Side 1 to side 2 distance through air	> 5	mm
CPG	External creepage(1)	Side 1 to side 2 distance across package surface	> 5	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>17	µm
CTI	Comparative tracking index	IEC 60112; UL 746A	>400	V
	Material Group	According to IEC 60664-1	II	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150V_{RMS}	I-IV	
		Rated mains voltage ≤ 300V_{RMS}	I-IV	
		Rated mains voltage ≤ 500V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17) (2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	707	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test. See Insulation Lifetime	500	V_{RMS}
		DC voltage	707	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM}, t = 60s (qualification); V_{TEST} = 1.2 × V_{IOTM}, t = 1s (100% production)	5303	V_{PK}
V_{IMP}	Maximum impulse voltage(3)	Tested in air, 1.2/50µs waveform per IEC 62368-1	7200	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(4)	Test method per IEC 62368-1, 1.2/50µs waveform, V_{TEST} = 1.6 × V_{IMP} or min 10 kV_{PK} (qualification)	6250	V_{PK}
q_{pd}	Apparent charge(5)	Method a: After I/O safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60s; $V_{pd(m)}$ = 1.2 × V_{IORM}, t_m = 10s	≤ 5	pC
		Method a: After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60s; $V_{pd(m)}$ = 1.6 × V_{IORM}, t_m = 10s	≤ 5	
		Method b: At routine test (100% production), V_{ini} = 1.2 × V_{IOTM}, t_{ini} = 1s; $V_{pd(m)}$ = 1.875 × V_{IORM}, t_m = 1s (method b1) or $V_{pd(m)}$ = V_{ini}, t_m = t_{ini} (method b2)	≤ 5	
C_{IO}	Barrier capacitance, input to output(6)	V_{IO} = 0.4 × sin (2 πft), f = 1MHz	1	pF
R_{IO}	Insulation resistance, input to output(6)	V_{IO} = 500V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500V at T_S = 150°C	> 10^9	
	Pollution degree		2	
	Climatic category		55/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	V_{TEST} = V_{ISO}, t = 60s (qualification); V_{TEST} = 1.2 × V_{ISO} , t = 1s (100% production)	3750	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation only* within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier tied together creating a two-pin device.

5.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Plan to certify according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to IEC 61010-1 and IEC 62368-1	Certified according to UL 1577 Component Recognition Program	Certified according to GB4943.1	Certified according to EN 61010-1 and EN 62368-1
Certificate pending	Master contract number: 220991	File number: E181974	Certificate: CQC24001426995	Client ID number: 77311

5.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SOP-4 PACKAGE (DFG)						
I_S	Safety limiting input current	$R_{\theta JA}$=206.3°C/W, V_F=1.5V, I_O=0mA, T_J=150°C, T_A=25°C			400	mA
	Safety limiting output current	$R_{\theta JA}$=206.3°C/W, V_F=1.5V, I_F=20mA, T_J=150°C, T_A=25°C			270	mA
P_S	Safety limiting total power	$R_{\theta JA}$=206.3°C/W, T_J=150°C, T_A=25°C			610	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

5.9 Electrical Characteristics

All specifications are at T_A = 25 ℃ unless otherwise noted

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
INPUT							
V_F	Input forward voltage	I_F = I_{FT}	25°C	0.9	1.1	1.3	V
			–55°C to 125°C	0.85	1.1	1.35	
		I_F = 5mA	25°C	1.1	1.3	1.5	
			–55°C to 125°C	1.1	1.3	1.55	
I_R	Input reverse current	V_R = 5V	–55°C to 125°C			10	µA
C_{IN}	Input capacitance	f = 1MHz, V_F = 0V	25°C		17	28	pF
I_{FT}	Input Trigger forward current; see Figure 6-3	I_o = 100mA (1), R_{ON} = 10Ω (2)	25°C		0.65	0.8	mA
			–55°C to 125°C		0.65	1.2	
$I_{FT,release}$	Release Trigger Current	I_{OFF} = 1µA at 70V	–55°C to 125°C	0.1			mA
$V_{F,\ release}$	Release Trigger Voltage	I_{OFF} = 1µA at 70V	–55°C to 125°C	0.7			V
$I_{F(ON)}$	Input on-state forward current	I_o = 100mA, R_{ON} < 10Ω	25°C	0.8		20	mA
		I_o = 100mA(1), R_{ON} < 15Ω	–55°C to 125°C	1.2		20	
OUTPUT							
V_{OFF}	Output Blocking voltage	I_F = 0mA	–55°C to 125°C			70	V
R_{ON}	Output on-state resistance; see Figure 6-3	I_F = I_{FT}, I_o = 20mA	25°C		6.5	9	Ω
			–55°C to 125°C		6.5	12	
	Output on-state resistance; seeFigure 6-3 (1)	I_F = I_{FT}, I_o = 100mA	25°C		7	10	
			–55°C to 125°C		7	13	
		I_F = I_{FT}, I_o = 100mA, t<1s	25°C		7	10	
	Output on-state resistance; see Figure 6-3	I_F = 3mA, I_o = 20mA	25°C		5.5	7	
			–55°C to 125°C		5.5	12	
	Output on-state resistance; see Figure 6-3 (1)	I_F = 3mA, I_o = 100mA	25°C		6	7.5	
			–55°C to 125°C		6	12	
		I_F = 3mA, I_o = 100mA, t<1s	25°C		5	7	
C_{OFF}	Output off-state capacitance	I_F = 0mA, V_L = 60V, f = 1MHz	–55°C to 125°C		6.5	8	pF
I_{LEAK}	Output off-state leakage; see Figure 6-2	I_F = 0mA, V_{OFF} = 70V	25°C			250	nA
			–55°C to 125°C			1	µA
$R_{ON\ FLAT}$	On-state resistance flatness	I_F = 5mA	25°C		45	75	mΩ
			–55°C to 125°C		45	115	
$R_{ON\ DRIFT}$	On-state resistance drift across temperature	I_F = 3mA, I_o = 40mA	–55°C to 125°C		23	60	m Ω/ºC
BW	–3dB Bandwidth; see Figure 6-4	I_F = 5mA, R_L = 50Ω	25°C	100			MHz
I_L	Insertion Loss (LED On); see Figure 6-4	I_F = 5mA, R_L = 50Ω, f = 1MHz	25°C		-0.45		dB
O_{ISO}	Off-state Isolation; see Figure 6-5	I_F = 0mA , R_L = 50Ω, f = 1MHz	25°C		-45		dB

(1) Current available to load must be derated by 1mA/°C for T_A > 75°C
(2) I_{FT} measured for R_{ON}=15Ω for T_A > 75°C

5.10 Switching Characteristics

All specifications are at T_A = 25 ℃ unless otherwise noted

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
AC							
T_{ON}	Output turn-on time; see Figure 6-1	I_F = 5mA, VCC=20V, R_L = 200Ω, C_L=50pF	–55°C to 125°C			0.2	ms
T_{OFF}	Output turn-off time; see Figure 6-1	I_F = 5mA, VCC=20V, R_L = 200Ω, C_L=50pF	–55°C to 125°C			0.2	ms

5.11 Typical Characteristics

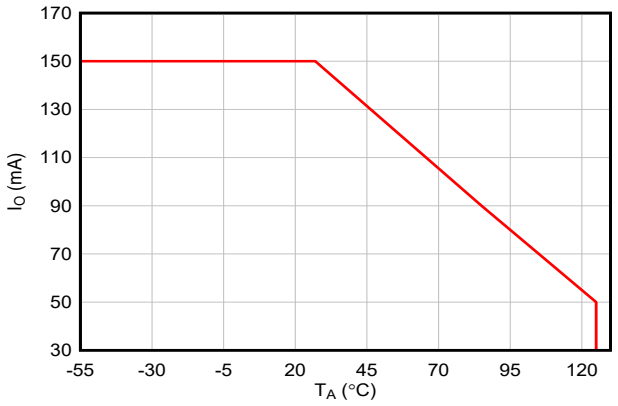


Figure 5-1. Typical Maximum Load Current vs Temperature

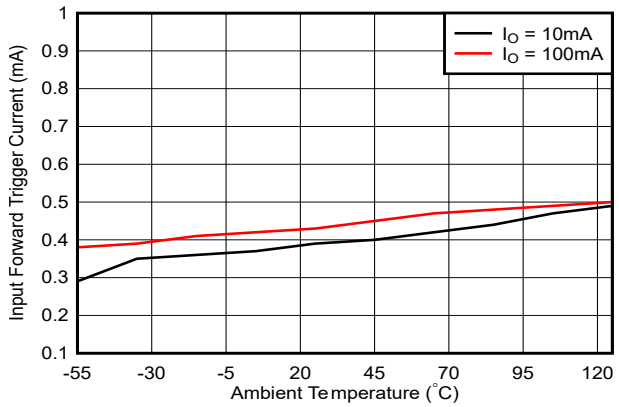


Figure 5-2. Input Forward Trigger Current vs Ambient Temperature

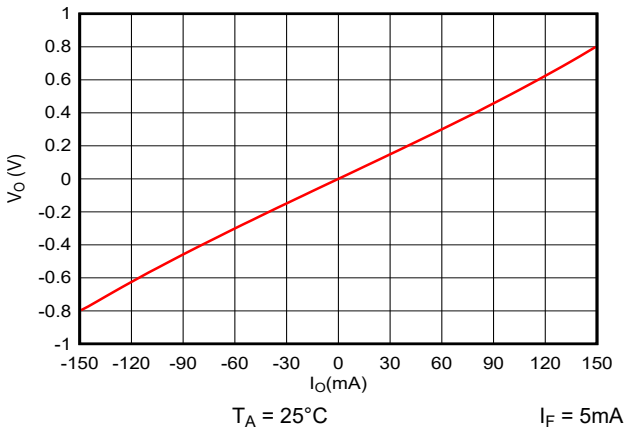


Figure 5-3. Continuous Load Current vs On-State Voltage

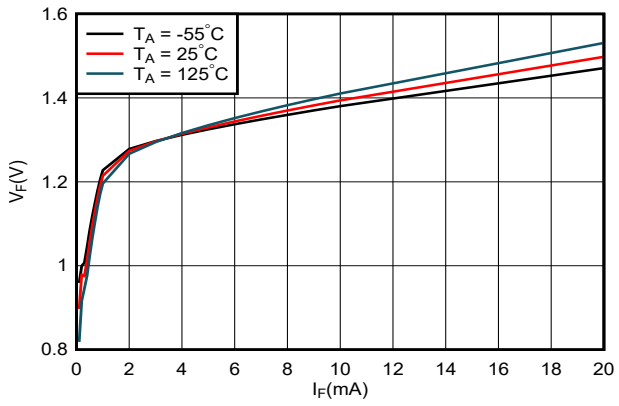


Figure 5-4. Forward Current vs LED Forward Voltage

5.11 Typical Characteristics (continued)

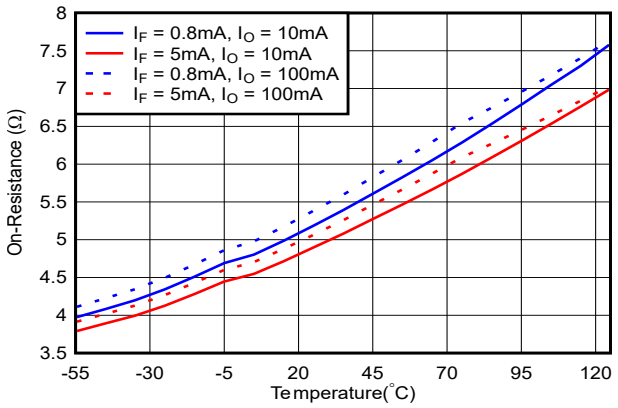


Figure 5-5. On-State Resistance vs Ambient Temperature

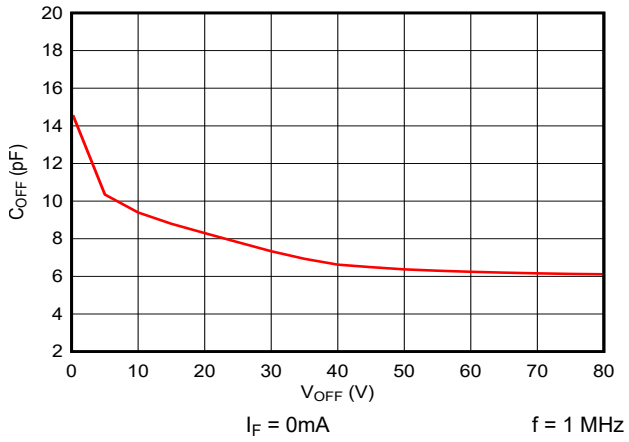


Figure 5-6. Output Capacitance vs Load Voltage

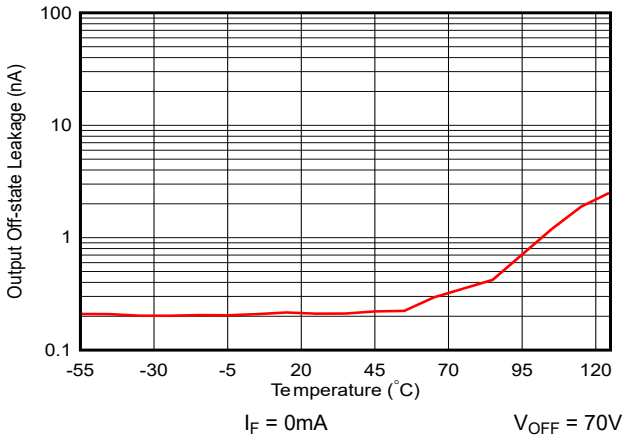


Figure 5-7. Off-State Leakage vs Ambient Temperature

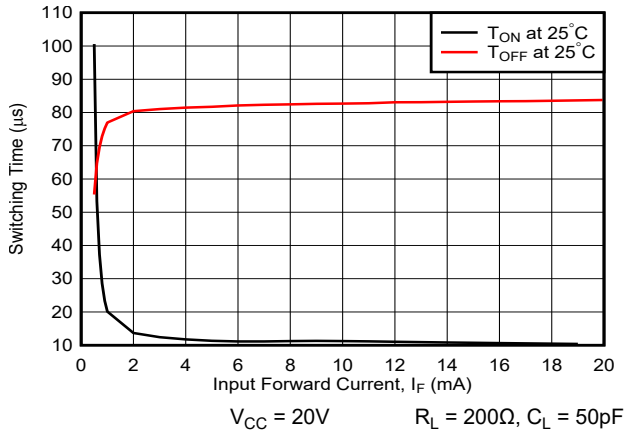


Figure 5-8. Turn-On, Turn-Off Time vs Forward Current

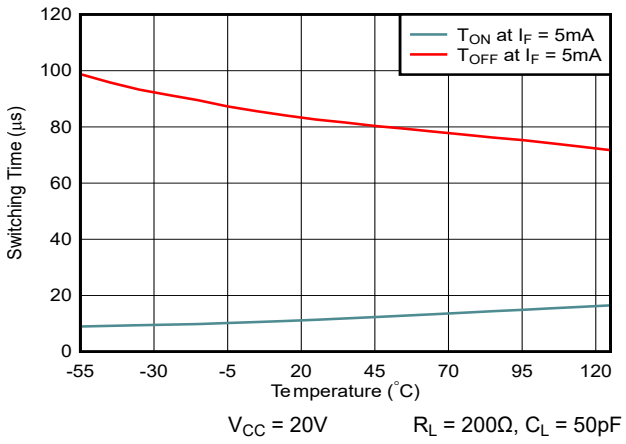


Figure 5-9. Turn-On, Turn-Off Time vs Ambient Temperature

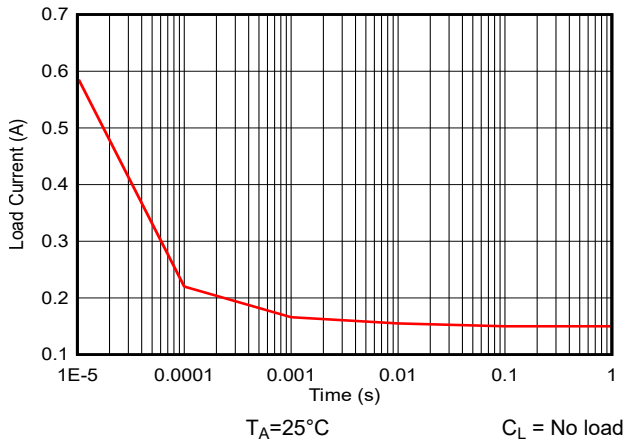


Figure 5-10. Pulse Current Rating Curve at 25°C

6 Parameter Measurement Information

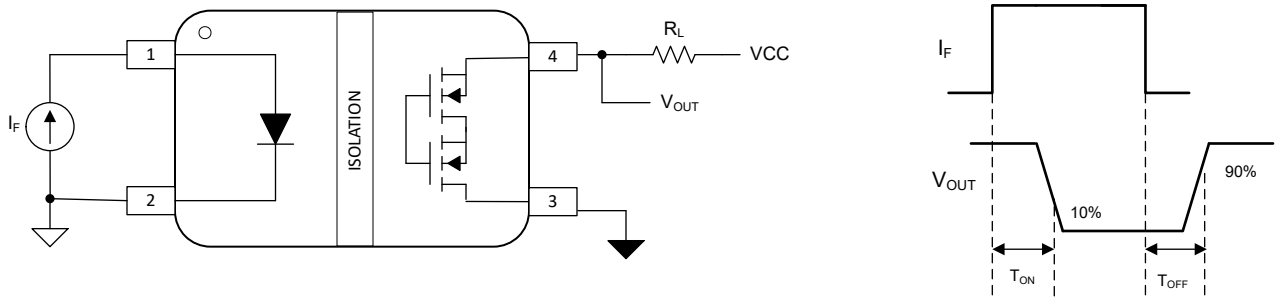


Figure 6-1. ISOM8610 Test Circuit for Turn-On and Turn-Off Time

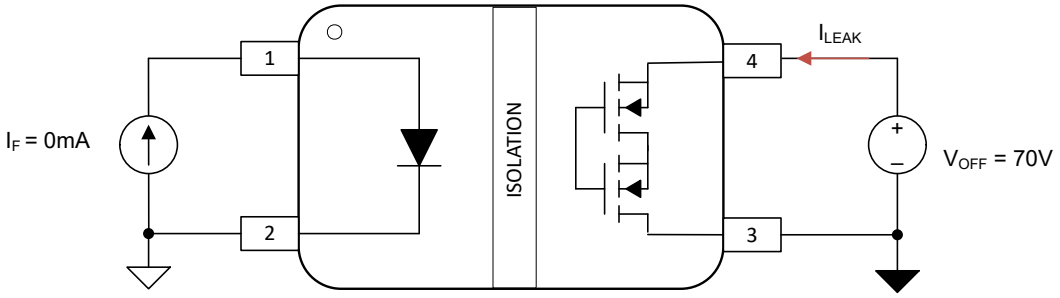


Figure 6-2. ISOM8610 Test Circuit Off-State Leakage

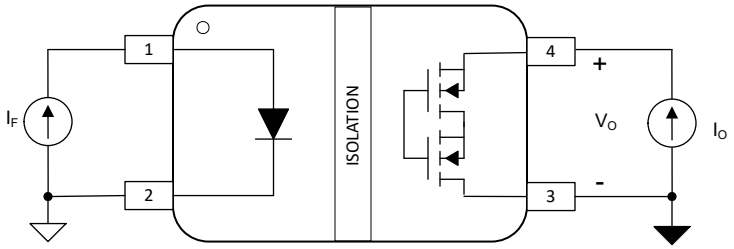


Figure 6-3. ISOM8610 Test Circuit for On-State Resistance

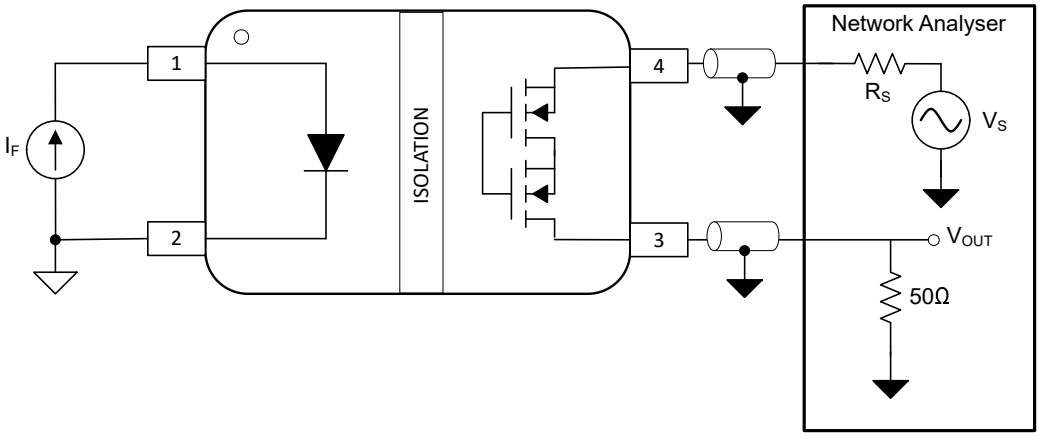


Figure 6-4. ISOM8610 Test Circuit for Insertion Loss

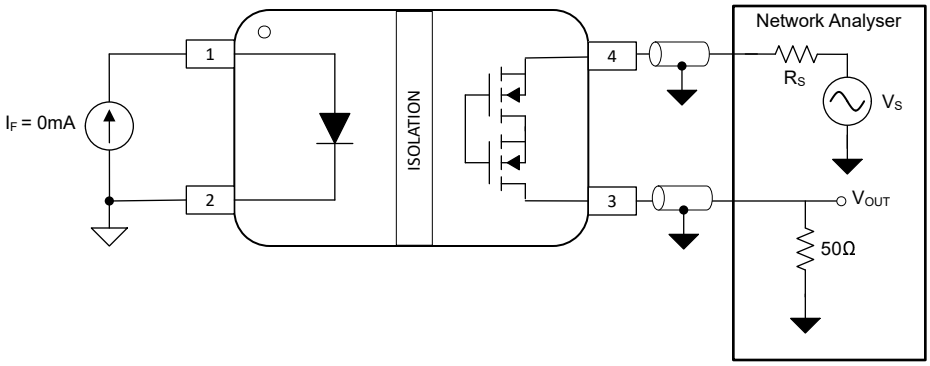


Figure 6-5. ISOM8610 Test Circuit for Off-State Isolation

7 Detailed Description

7.1 Overview

The ISOM8610 are opto-emulator switches that provide up to 3.75kV isolation across barrier and are pin-compatible, drop-in replacements to popular photo-relays. While standard optocouplers use an LED as the input stage, the ISOM8610 uses a current controlled emulated diode as the input stage. The input stage is isolated from the driver stage by TI's proprietary silicon dioxide-based (SiO_2) isolation barrier, which not only provides robust isolation, but also offers best-in-class performance.

The ISOM8610 isolates high voltage signals and offer performance, reliability, and flexibility advantages over traditional optocouplers which age over time. The devices are based on CMOS isolation technology for low-power and high-speed operation, therefore the devices are resistant to the wear-out effects found in optocouplers that degrade performance with increasing temperature, forward current, and device age.

The functional block diagram of the ISOM8610 is shown in *Functional Block Diagram*. The input signal is transmitted across the isolation barrier using an on-off keying (OOK) modulation scheme. The transmitter sends a high-frequency carrier across the barrier to represent switch-ON state and sends no signal to represent the switch-OFF state. The receiver demodulates the signal after advanced signal conditioning and controls the state of the output MOSFETs. These devices also incorporate advanced circuit techniques to maximize CMTI performance and minimize radiated emissions. Figure 7-2 shows conceptual detail of how the OOK scheme works.

7.2 Functional Block Diagram

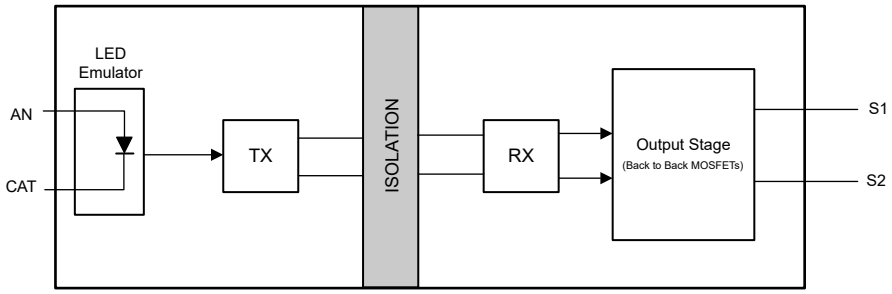


Figure 7-1. Conceptual Block Diagram of an Opto-Emulator

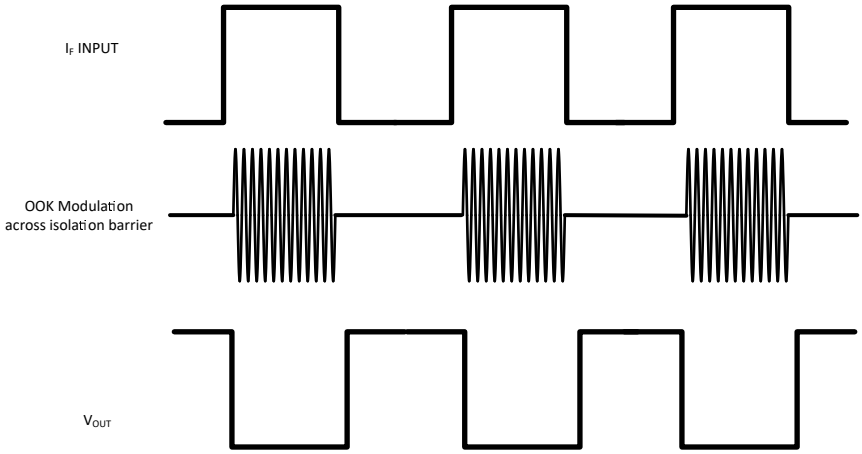


Figure 7-2. On-Off Keying (OOK) Based Modulation Scheme

7.3 Feature Description

The ISOM8610 is a current controlled isolated switch, and is a reliable pin-to-pin replacement of to existing Opto-MOS devices in DFG package. The isolated switch is normally open, which means the switch on secondary side is in OFF state when the primary LED emulator current is lower than the input trigger current level. In the OFF state, the back-to-back MOSFETs on the secondary side block up to 80V of difference between S1 and S2. Once the primary side LED emulator current goes above input trigger current, the switch on the secondary side turns ON. During the ON state, the secondary side back-to-back FETs can conduct currents up to 150mA. The robust SiO_2 dielectric isolation in the ISOM8610 provides best in class isolation performance, faithfully withstanding 3750V_{RMS} isolation ratings between side 1 and side 2, performance limited by package clearance.

7.4 Device Functional Modes

Table 7-1 lists the functional modes for the ISOM86xx devices.

Table 7-1. Function Table

INPUT CURRENT I_F	OUTPUT SWITCH STATE	COMMENTS
$0 < I_F < I_{FT}$	OFF	Switch is in OFF state and presents an off state capacitance (C_{OFF}) across S1 and S2.
$I_{FT} \le I_F$	ON	Switch is in ON state and presents an on resistance (R_{ON}) across S1 and S2

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The ISOM8610 is a single-channel isolated switch with diode-emulator inputs which control an output stage with back-to-back MOSFETs. The devices use robust on-off keying modulation to transmit data across the isolation barrier. Since an isolation barrier separates the two sides of these devices, each side can be sourced independently with voltages and currents within recommended operating conditions. The ISOM8610 is designed to be implemented in a variety of applications like realizing switchable termination in communication lines like CAN and RS485, switching burden resistors in analog input modules and small footprint sink/source capable digital output module in AC Servo motor drives.

The opto-emulators do not conform to any specific interface standard and are intended for isolated switching operations. The ISOM8610 is typically placed between a data controller (that is, an MCU or FPGA), and a sensor or a line transceiver, regardless of the interface type or standard.

8.2 Typical Application

The ISOM8610 can be used in numerous industrial applications. For instance, the device can be used on a CAN node design. The ISOM8610 enables a software configurable termination on the CAN bus, needed in networks where new nodes can be continually added. This design can enable or disable termination across CANH-CANL by driving TERM high or low (with appropriate current limiting series resistor on LED emulator pins) through GPIO of the MCU. The farthest terminals on the CAN Bus must be driving TERM = High to enable 120 ohm resistor across the bus, while all other nodes drive TERM = Low. ISOM8610DFG can easily support ±12V common mode with no distortion of CAN signals on the bus. The ISOM8610 also does not require a bulky secondary side isolated power supply, to perform the switching operation. TERM control is galvanically isolated from the CAN lines for reliable system protection. With this architecture, 60Ω effective termination across the CAN bus can be achieved with flexibility on enabling/disabling a node, with no hardware change. The *Top Design Questions About Isolated CAN Bus Design* application note contains top answers to design questions about Isolated CAN Bus designs. Finally, the ISOM8610 can be used as an 80V isolated switch when used within the *Recommended Operating Conditions*.

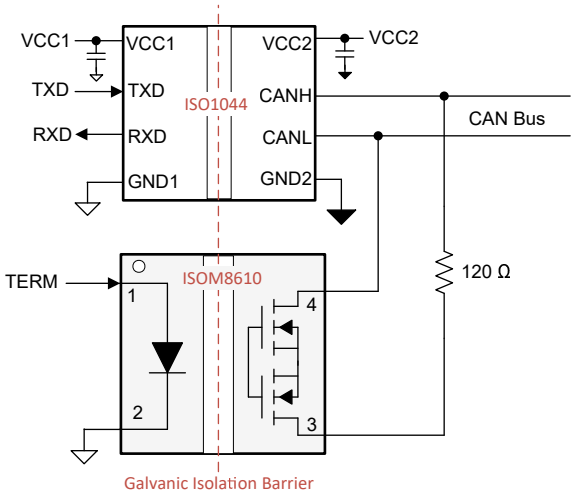


Figure 8-1. Typical Software-Controlled Termination Using the ISOM8610

8.2.1 Design Requirements

To design with the ISOM8610 device, use the parameters listed in Table 8-1.

Table 8-1. Design Parameters

PARAMETER	VALUE	EXAMPLE VALUE
Input forward current, I_F	0.8mA to 20mA	2mA

8.2.2 Detailed Design Procedure

This section presents the design procedure for using the ISOM8610 opto-emulators. External components must be selected to operate the ISOM8610 within the *Recommended Operating Conditions*. The following recommendations on components selection focus on the design of a typical isolated signal circuit with considerations for input current and data rate.

8.2.2.1 Sizing R_{IN}

The input side of the ISOM8610 is current-driven. Placing a series resistor, R_{IN}, in series with the input as shown in Figure 8-1 is recommended to limit the amount of current flowing into the AN pin.

R_{IN} can be sized to minimize current flow and power consumption through the ISOM8610 input-side. R_{IN} must be a value that limits the input forward current to be within the *Recommended Operating Conditions* for the ISOM8610. The equation to calculate R_{IN} for a given input voltage, V_{IN}, and desired input forward current, I_F, is shown in Equation 1 where V_F is the maximum specification for the ISOM8610 input forward voltage:

$$R_{IN} = \frac{V_{IN} - V_{F\,[MAX]}}{I_F} \quad (1)$$

For example, with a 24V input and 2mA desired I_F, R_{IN} can be calculated as:

$$R_{IN} = \frac{24V - 1.5V}{2mA} = 11.25k\Omega \quad (2)$$

8.2.3 Application Curve

The following typical switching curve shows data transmission using the ISOM8610.

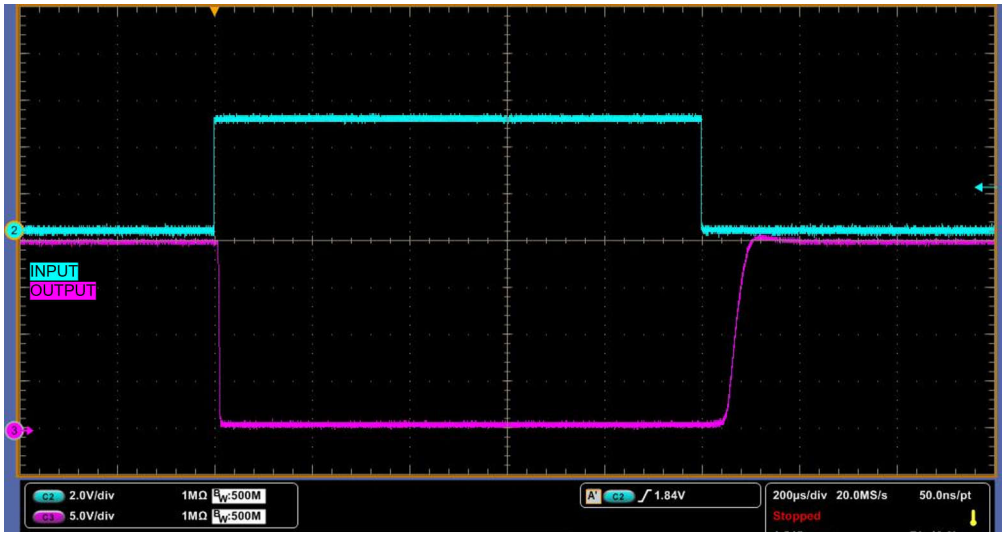


Figure 8-2. Typical Waveform at I_F = 5mA, V_{CC} = 20V, R_L = 200Ω and C_L = 50pF

8.3 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; see Figure 8-3 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 50% for lifetime which translates into minimum required insulation lifetime of 30 years at a working voltage that's 20% higher than the specified value.

Figure 8-4 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over the lifetime of the barrier. Based on the TDDB data, the intrinsic capability of the insulation is $500V_{RMS}$ with a lifetime of 44. Other factors such as package size, pollution degree, and material group can further limit the working voltage of a component.

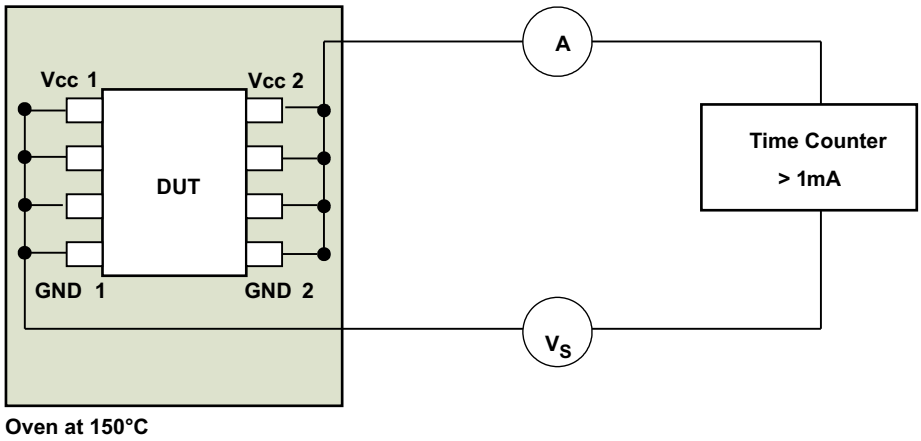


Figure 8-3. Test Setup for Insulation Lifetime Measurement

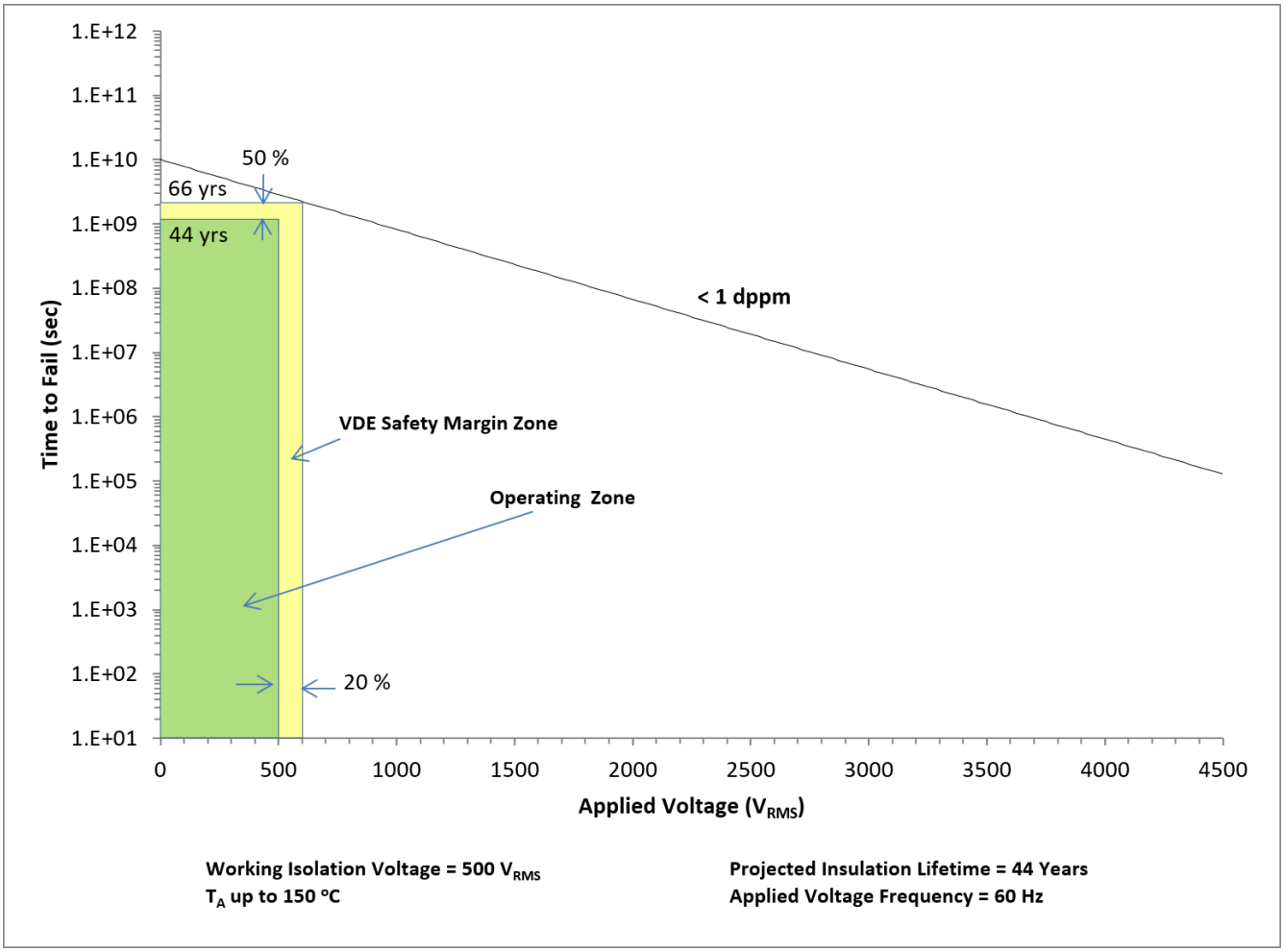


Figure 8-4. Insulation Lifetime Projection Data

8.4 Power Supply Recommendations

The ISOM8610 does not require a dedicated power supply to operate since there is no supply pin. Take care not to violate recommended operating I/O specifications for proper device functionality.

8.5 Layout

8.5.1 Layout Guidelines

- The device connections to ground must be tied to the PCB ground plane using a direct connection or two vias to help minimize inductance.
- The connections of capacitors and other components to the PCB ground plane must use a direct connection or two vias for minimum inductance.

8.5.2 Layout Example

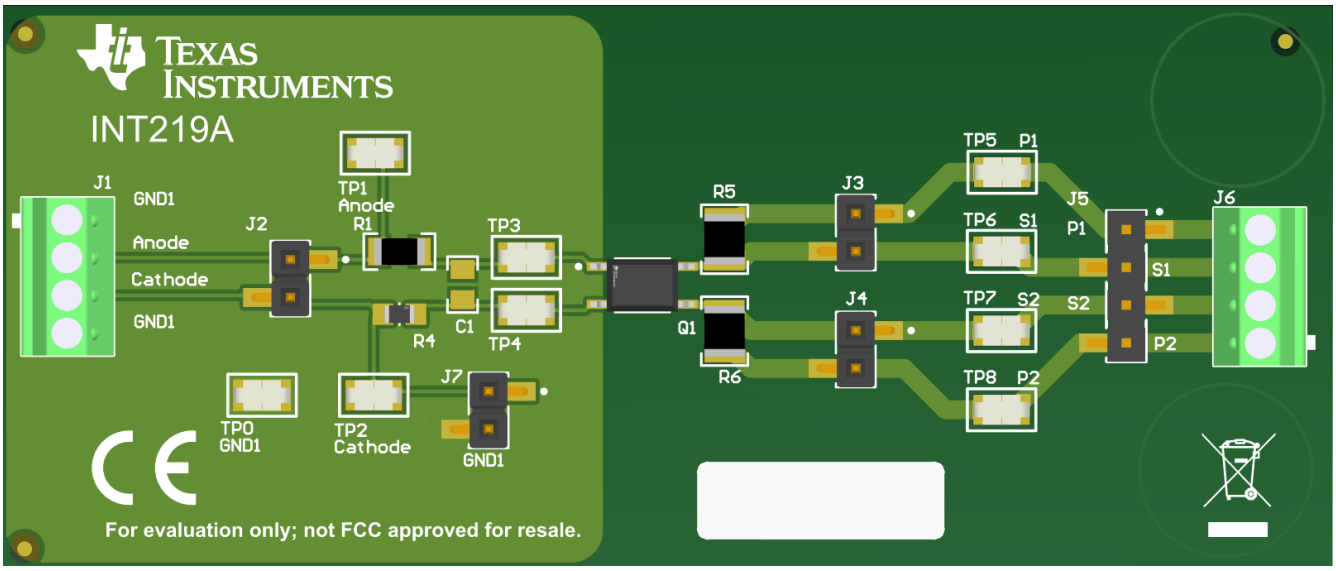


Figure 8-5. Layout Example of ISOM8610 With a 2-Layer Board

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Isolation Glossary*, application note
- Texas Instruments, *Top Design Questions About Isolated CAN Bus Design*, application note
- Texas Instruments, *ISO1044 Isolated CAN FD Transceiver in Small Package*, data sheet

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2024) to Revision B (September 2025)	Page
• Changed to 500 VRMS to match VIOWM	6
• Changed 'Plan to certify' to Certified' and added certificate numbers	7

Changes from Revision * (April 2024) to Revision A (May 2024)	Page
• Updated the number format for tables, figures, and cross-references throughout the document	1
• Added layout guidelines for LED placement	18

11 Mechanical, Packaging, and Orderable Information

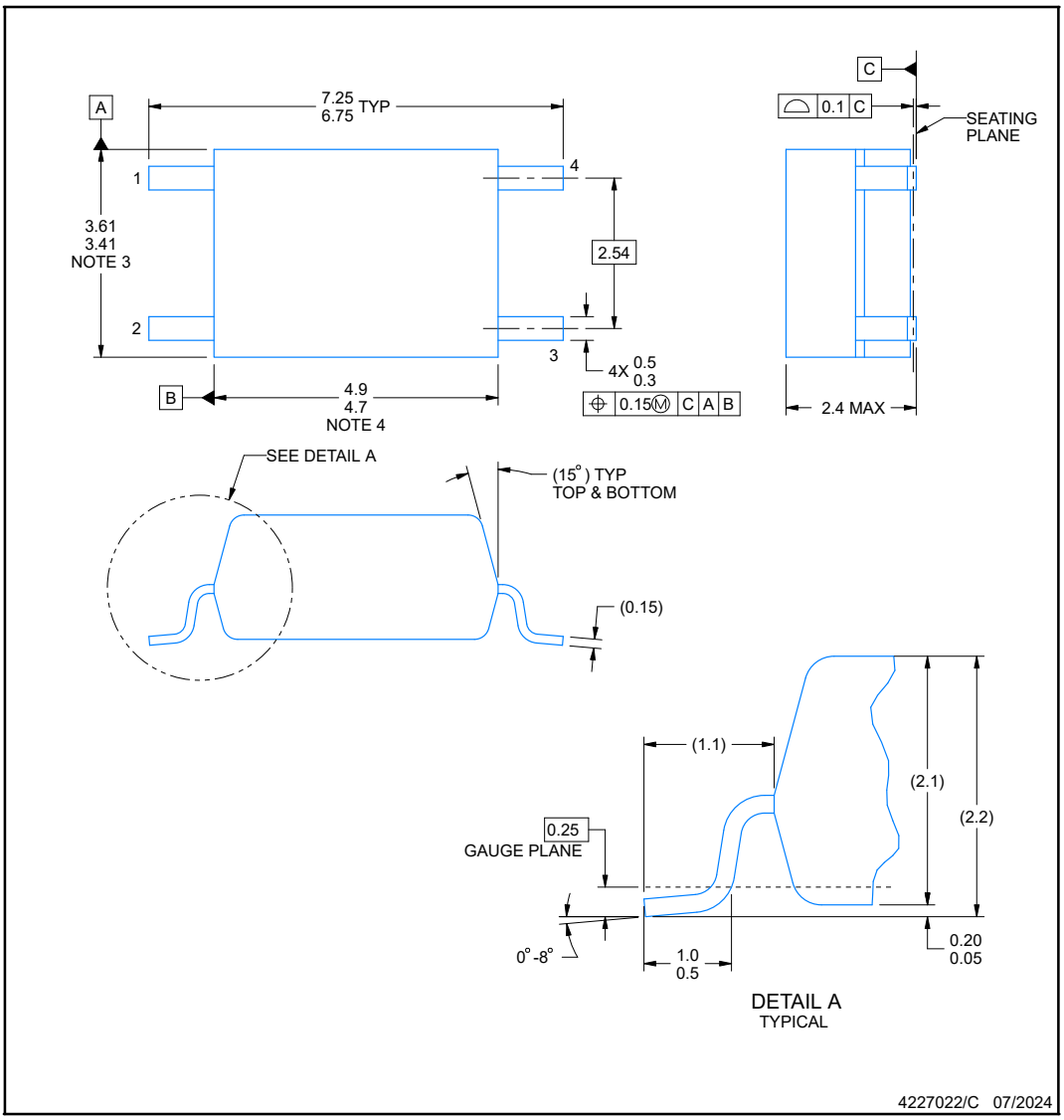
The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

DFG0004A

SOIC - 2.4 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

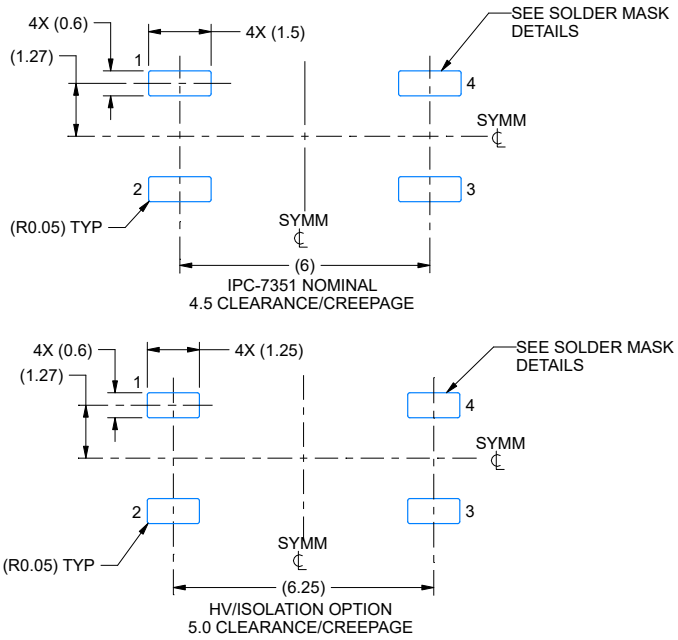
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 mm per side.
4. This dimension does not include interlead flash.

EXAMPLE BOARD LAYOUT

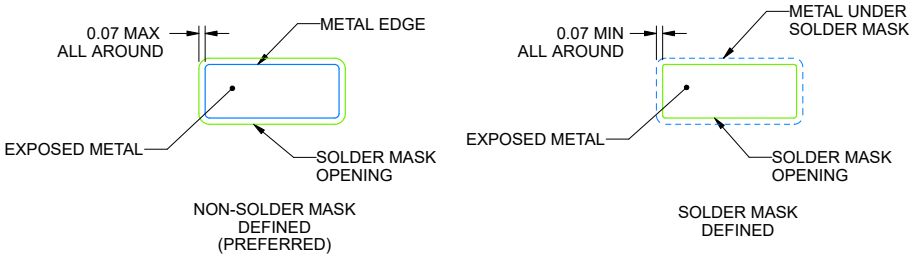
DFG0004A

SOIC - 2.4 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 7X



SOLDER MASK DETAILS

4227022/C 07/2024

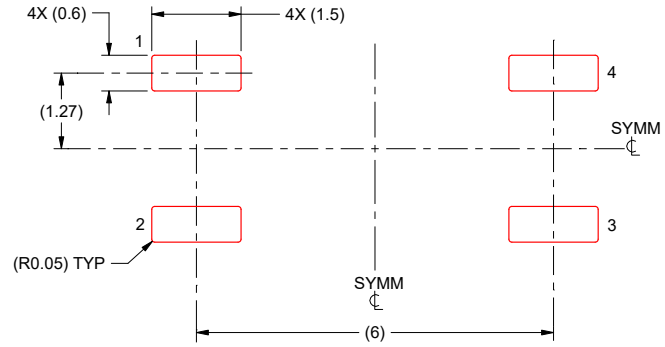
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

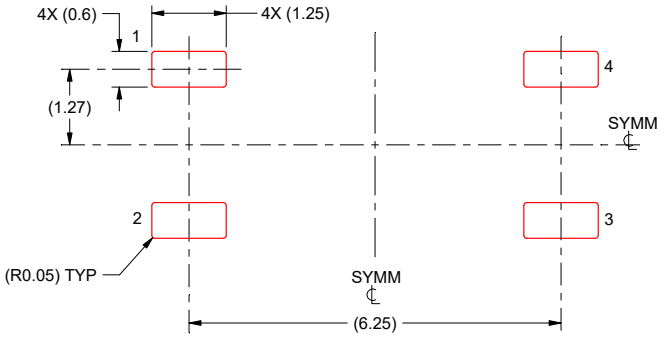
EXAMPLE STENCIL DESIGN

DFG0004A — **SOIC - 2.4 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



IPC-7351 NOMINAL
4.5 CLEARANCE/CREEPAGE



HV/ISOLATION OPTION
5.0 CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4227022/C 07/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISOM8610DFGR	Active	Production	SOIC (DFG) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8610
ISOM8610DFGR.A	Active	Production	SOIC (DFG) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8610

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

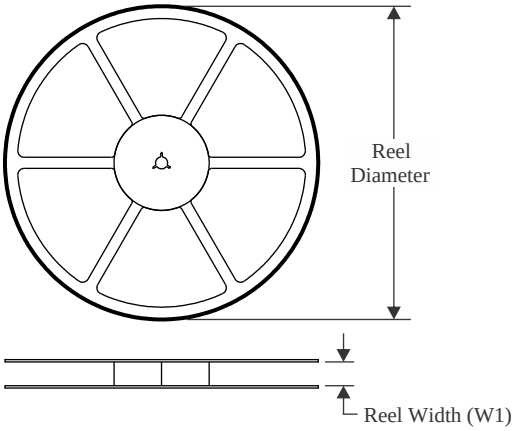
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

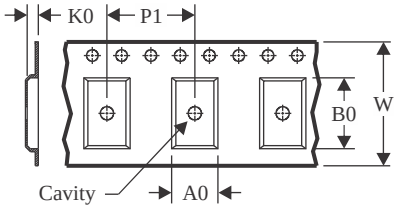
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

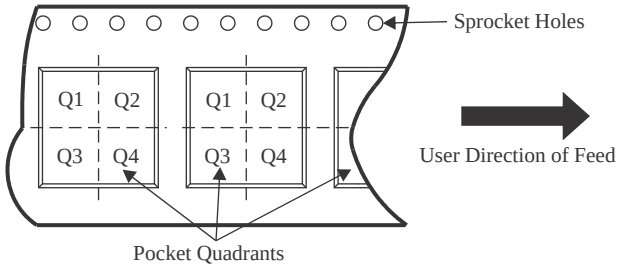


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

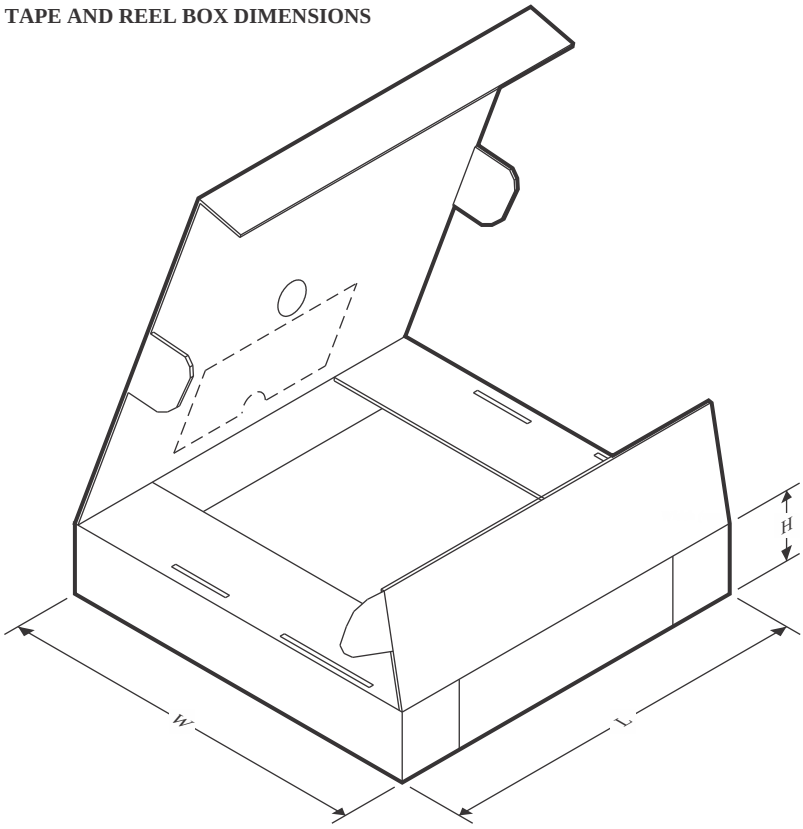
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISOM8610DFGR	SOIC	DFG	4	2000	330.0	12.4	8.0	3.8	2.7	12.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISOM8610DFGR	SOIC	DFG	4	2000	353.0	353.0	32.0

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025