

## LF198QML Monolithic Sample-and-Hold Circuits

Check for Samples: [LF198QML](#)

### FEATURES

- Operates from  $\pm 5\text{V}$  to  $\pm 18\text{V}$  supplies
- Less than  $10\ \mu\text{s}$  acquisition time
- TTL, PMOS, CMOS compatible logic input
- $0.5\ \text{mV}$  typical hold step at  $C_H = 0.01\ \mu\text{F}$
- Low input offset
- $0.002\%$  gain accuracy
- Low output noise in hold mode
- Input characteristics do not change during hold mode
- High supply rejection ratio in sample or hold
- Wide bandwidth

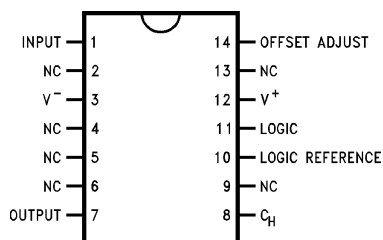
### DESCRIPTION

The LF198 is a monolithic sample-and-hold circuit which utilizes BI-FET technology to obtain ultra-high dc accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, dc gain accuracy is  $0.002\%$  typical and acquisition time is as low as  $6\ \mu\text{s}$  to  $0.01\%$ . A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin, and does not degrade input offset drift. The wide bandwidth allows the LF198 to be included inside the feedback loop of  $1\ \text{MHz}$  op amps without having stability problems. Input impedance of  $10^{10}\ \Omega$  allows high source impedances to be used without degrading accuracy.

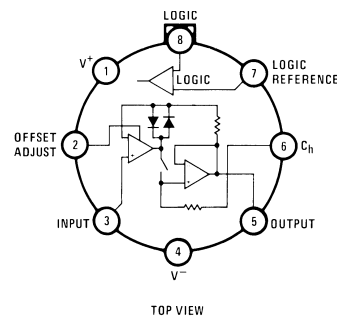
P-channel junction FET's are combined with bipolar devices in the output amplifier to give droop rates as low as  $5\ \text{mV/min}$  with a  $1\ \mu\text{F}$  hold capacitor. The JFET's have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design specifies no feed-through from input to output in the hold mode, even for input signals equal to the supply voltages.

Logic inputs on the LF198 are fully differential with low input current, allowing direct connection to TTL, PMOS, and CMOS. Differential threshold is  $1.4\text{V}$ . The LF198 will operate from  $\pm 5\text{V}$  to  $\pm 18\text{V}$  supplies.

### Connection Diagrams



**Figure 1. Small-Outline Package (CGLA)**  
See Package Number NAC0014A



**Figure 2. Metal Can Package (TO-99)**  
See Package Number LMC0008C



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Typical Connection and Performance Curve

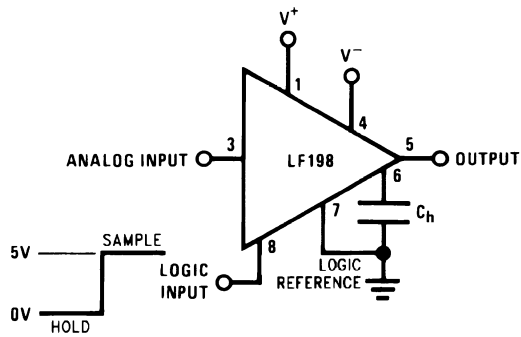


Figure 3.

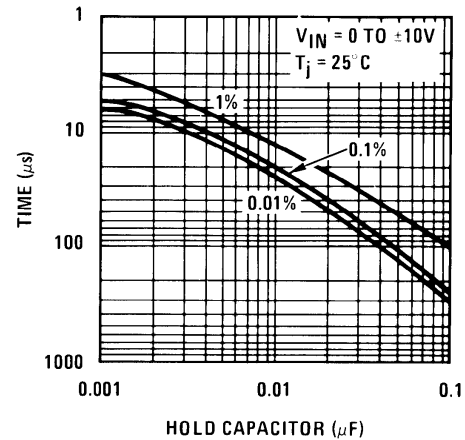
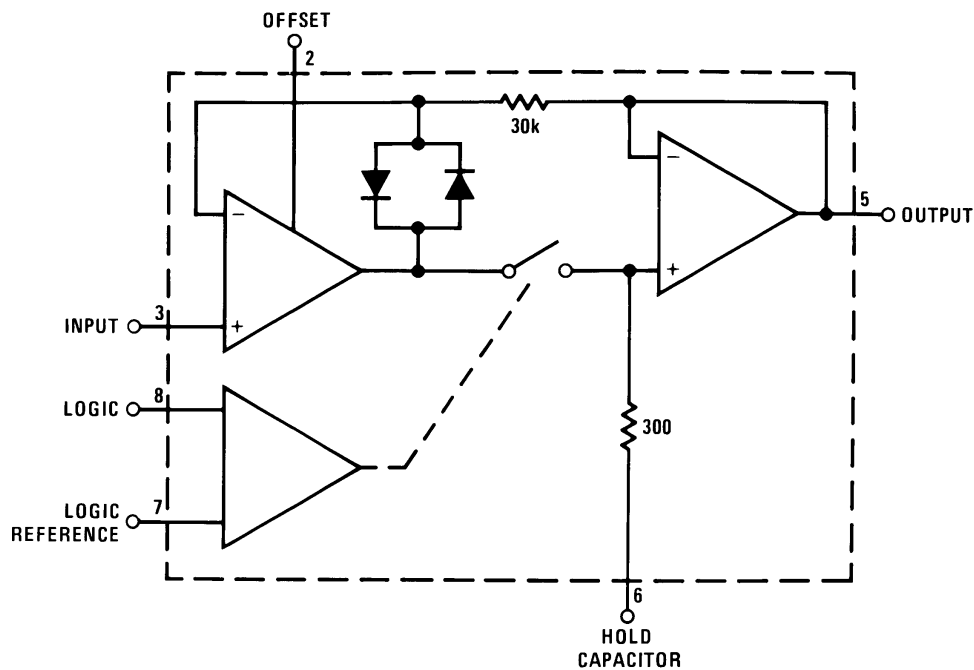


Figure 4. Acquisition Time

## Functional Diagram



## Absolute Maximum Ratings <sup>(1)</sup>

|                                                              |                         |
|--------------------------------------------------------------|-------------------------|
| Supply Voltage                                               | ±18V                    |
| Power Dissipation (Package Limitation) <sup>(2)</sup>        | 500 mW                  |
| Operating Ambient Temperature Range                          | –55°C to +125°C         |
| Maximum Junction Temperature (T <sub>Jmax</sub> )            | +150°C                  |
| Input Voltage                                                | Equal to Supply Voltage |
| Logic To Logic Reference Differential Voltage <sup>(3)</sup> | +7V, –30V               |
| Output Short Circuit Duration                                | Indefinite              |
| Hold Capacitor Short Circuit Duration                        | 10 sec                  |
| Lead Temperature (Soldering, 10 sec.)                        | 260°C                   |
| Thermal Resistance, $\theta_{JA}$                            |                         |
| Metal Can (Still Air at 0.5W)                                | 160°C/W                 |
| Metal Can (500 LF/Min Air at 0.5W)                           | 84°C/W                  |
| Ceramic SOIC (Still Air at 0.5W)                             | 140°C/W                 |
| Ceramic SOIC (500 LF/Min Air Flow at 0.5W)                   | 95°C/W                  |
| $\theta_{JC}$                                                |                         |
| Metal Can                                                    | 48°C/W                  |
| Ceramic SOIC                                                 | 20°C/W                  |
| Package Weight (typical)                                     |                         |
| Metal Can                                                    | TBD                     |
| Ceramic SOIC                                                 | 415mg                   |
| ESD Tolerance <sup>(4)</sup>                                 | 500V                    |

- (1) “Absolute Maximum Ratings” indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For specifications and test conditions, see the Electrical Characteristics. The specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions
- (2) The maximum power dissipation must be derated at elevated temperatures and is dictated by T<sub>JMAX</sub>,  $\theta_{JA}$ , and the ambient temperature, T<sub>A</sub>. The maximum allowable power dissipation at any temperature is  $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ , or the number given in the Absolute Maximum Ratings, whichever is lower. .
- (3) Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.
- (4) Human body model, 100pF discharged through 1.5K $\Omega$

## Quality Conformance Inspection

Mil-Std-883, Method 5005 — Group A

| Subgroup | Description         | Temperature (°C) |
|----------|---------------------|------------------|
| 1        | Static tests at     | +25°C            |
| 2        | Static tests at     | +125°C           |
| 3        | Static tests at     | –55°C            |
| 4        | Dynamic tests at    | +25°C            |
| 5        | Dynamic tests at    | +125°C           |
| 6        | Dynamic tests at    | –55°C            |
| 7        | Functional tests at | +25°C            |
| 8A       | Functional tests at | +125°C           |
| 8B       | Functional tests at | –55°C            |
| 9        | Switching tests at  | +25°C            |
| 10       | Switching tests at  | +125°C           |
| 11       | Switching tests at  | –55°C            |

## Electrical Characteristics

The following specifications apply unless otherwise specified.

$V_{CC} = \pm 15V$ ,  $R_L = 10K\Omega$ ,  $V_{IN} = 0V$ ,  $C_{HOLD} = 0.01 \mu F$ , Logic Reference Pin = 0V, Logic Pin = 4V

| Symbol          | Parameter                           | Conditions                                        | Notes              | Min  | Max | Unit | Sub-groups |
|-----------------|-------------------------------------|---------------------------------------------------|--------------------|------|-----|------|------------|
| $I_{CC+}$       | Positive Supply Current             | $+V_{CC} = 15V, -V_{CC} = -15V$                   |                    |      | 5.5 | mA   | 1, 2       |
|                 |                                     |                                                   |                    |      | 6.5 | mA   | 3          |
|                 |                                     | $+V_{CC} = 18V, -V_{CC} = -18V$ , Mode = "Sample" |                    |      | 5.5 | mA   | 1, 2       |
|                 |                                     |                                                   |                    |      | 6.5 | mA   | 3          |
|                 |                                     | $+V_{CC} = 18V, -V_{CC} = -18V$ , Mode = "Hold"   |                    |      | 5.5 | mA   | 1, 2       |
|                 |                                     |                                                   |                    |      | 6.5 | mA   | 3          |
| $I_{CC-}$       | Negative Supply Current             | $+V_{CC} = 15V, -V_{CC} = -15V$                   |                    | -5.5 |     | mA   | 1, 2       |
|                 |                                     |                                                   |                    | -6.5 |     | mA   | 3          |
|                 |                                     | $+V_{CC} = 18V, -V_{CC} = -18V$ , Mode = "Sample" |                    | -5.5 |     | mA   | 1, 2       |
|                 |                                     |                                                   |                    | -6.5 |     | mA   | 3          |
|                 |                                     | $+V_{CC} = 18V, -V_{CC} = -18V$ , Mode = "Hold"   |                    | -5.5 |     | mA   | 1, 2       |
|                 |                                     |                                                   |                    | -6.5 |     | mA   | 3          |
| $V_{OS}$        | Input Offset Voltage                | $+V_{CC} = 3V, -V_{CC} = -7V$                     |                    | -3.0 | 3.0 | mV   | 1          |
|                 |                                     |                                                   |                    | -5.0 | 5.0 | mV   | 2, 3       |
|                 |                                     | $+V_{CC} = 15V, -V_{CC} = -15V$                   |                    | -3.0 | 3.0 | mV   | 1          |
|                 |                                     |                                                   |                    | -5.0 | 5.0 | mV   | 2, 3       |
|                 |                                     | $+V_{CC} = 3.5V, -V_{CC} = -26.5V$                |                    | -3.0 | 3.0 | mV   | 1          |
|                 |                                     |                                                   |                    | -5.0 | 5.0 | mV   | 2, 3       |
|                 |                                     | $+V_{CC} = 18V, -V_{CC} = -18V$                   |                    | -3.0 | 3.0 | mV   | 1          |
|                 |                                     |                                                   |                    | -5.0 | 5.0 | mV   | 2, 3       |
|                 |                                     | $+V_{CC} = 3.5V, -V_{CC} = -32.5V$                |                    | -3.0 | 3.0 | mV   | 1          |
|                 |                                     |                                                   |                    | -5.0 | 5.0 | mV   | 2, 3       |
|                 |                                     | $+V_{CC} = 26.5V, -V_{CC} = -3.5V$                |                    | -3.0 | 3.0 | mV   | 1          |
|                 |                                     |                                                   |                    | -5.0 | 5.0 | mV   | 2, 3       |
| $I_{IB}$        | Input Bias Current                  | $+V_{CC} = 3V, -V_{CC} = -7V$                     |                    | -25  | 25  | nA   | 1          |
|                 |                                     |                                                   |                    | -75  | 75  | nA   | 2, 3       |
|                 |                                     | $+V_{CC} = 15V, -V_{CC} = -15V$                   |                    | -25  | 25  | nA   | 1          |
|                 |                                     |                                                   |                    | -75  | 75  | nA   | 2, 3       |
|                 |                                     | $+V_{CC} = 3.5V, -V_{CC} = -32.5V$                |                    | -25  | 25  | nA   | 1          |
|                 |                                     |                                                   |                    | -75  | 75  | nA   | 2, 3       |
|                 |                                     | $+V_{CC} = 32.5V, -V_{CC} = -3.5V$                |                    | -25  | 25  | nA   | 1          |
|                 |                                     |                                                   |                    | -75  | 75  | nA   | 2, 3       |
|                 |                                     | $+V_{CC} = 7V, -V_{CC} = -3V$                     |                    | -25  | 25  | nA   | 1          |
|                 |                                     |                                                   |                    | -75  | 75  | nA   | 2, 3       |
| $I_{Leak(Cap)}$ | Leakage Current into Hold Capacitor | $+V_{CC} = 3V, -V_{CC} = -7V$                     | See <sup>(1)</sup> | -100 | 100 | pA   | 1          |
|                 |                                     | $+V_{CC} = 3.5V, -V_{CC} = -32.5V$                |                    | -100 | 100 | pA   | 1          |
|                 |                                     | $+V_{CC} = 32.5V, -V_{CC} = -3.5V$                | See <sup>(1)</sup> | -100 | 100 | pA   | 1          |
|                 |                                     | $+V_{CC} = 7V, -V_{CC} = -3V$                     |                    | -100 | 100 | pA   | 1          |

(1) Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is specified over full input signal range.

## Electrical Characteristics (continued)

The following specifications apply unless otherwise specified.

$V_{CC} = \pm 15V$ ,  $R_L = 10K\Omega$ ,  $V_{IN} = 0V$ ,  $C_{HOLD} = 0.01 \mu F$ , Logic Reference Pin = 0V, Logic Pin = 4V

| Symbol         | Parameter                    | Conditions                                                       | Notes              | Min  | Max       | Unit       | Sub-groups |
|----------------|------------------------------|------------------------------------------------------------------|--------------------|------|-----------|------------|------------|
| $V_{HS}$       | Hold Step                    | $+V_{CC} = 15V$ , $-V_{CC} = -15V$                               | See <sup>(2)</sup> | -2.0 | 2.0       | mV         | 1          |
|                |                              |                                                                  |                    | -5.6 | 5.6       | mV         | 2, 3       |
|                |                              | $+V_{CC} = 3.5V$ , $-V_{CC} = -26.5V$                            | See <sup>(2)</sup> | -2.5 | 2.5       | mV         | 1          |
|                |                              |                                                                  |                    | -5.6 | 5.6       | mV         | 2, 3       |
|                |                              | $+V_{CC} = 26.5V$ , $-V_{CC} = -3.5V$                            | See <sup>(2)</sup> | -2.5 | 2.5       | mV         | 1          |
|                |                              |                                                                  |                    | -5.6 | 5.6       | mV         | 2, 3       |
| $A_E$          | Gain Error                   | $+V_{CC} = 7V$ , $-V_{CC} = -3V$                                 |                    |      | 0.02      | %          | 1          |
|                |                              |                                                                  |                    |      | 0.06      | %          | 2, 3       |
|                |                              | $+V_{CC} = 3.5V$ , $-V_{CC} = -26.5V$                            |                    |      | 0.00<br>5 | %          | 1          |
|                |                              |                                                                  |                    |      | 0.02      | %          | 2, 3       |
|                |                              | $+V_{CC} = 32.5V$ , $-V_{CC} = -3.5V$                            |                    |      | 0.00<br>5 | %          | 1          |
|                |                              |                                                                  |                    |      | 0.06      | %          | 2, 3       |
|                |                              | $+V_{CC} = 26.5V$ , $-V_{CC} = -3.5V$                            |                    |      | 0.00<br>5 | %          | 1          |
|                |                              |                                                                  |                    |      | 0.02      | %          | 2, 3       |
| $Z_I$          | Input Impedance              | $+V_{CC} = 8V$ , $-V_{CC} = -28V$                                |                    | 10.0 |           | G $\Omega$ | 1          |
|                |                              |                                                                  |                    | 0.8  |           | G $\Omega$ | 2, 3       |
|                |                              | $+V_{CC} = 28V$ , $-V_{CC} = -8V$                                |                    | 10.0 |           | G $\Omega$ | 1          |
|                |                              |                                                                  |                    | 0.8  |           | G $\Omega$ | 2, 3       |
| $Z_O$          | Output Impedance             | $+V_{CC} = 18V$ , $-V_{CC} = -18V$                               |                    |      | 2.0       | $\Omega$   | 1          |
|                |                              |                                                                  |                    |      | 4.0       | $\Omega$   | 2, 3       |
| $I_{Charge}$   | Capacitor Charging Current   | $+V_{CC} = 8V$ , $-V_{CC} = -28V$                                |                    | -25  | -4.5      | mA         | 1          |
|                |                              |                                                                  |                    | -25  | -3.0      | mA         | 2, 3       |
|                |                              | $+V_{CC} = 28V$ , $-V_{CC} = -8V$                                |                    | 4.5  | 25        | mA         | 1          |
|                |                              |                                                                  |                    | 3.0  | 25        | mA         | 2, 3       |
| Logic          | Logic Pin Current            | $+V_{CC} = 18V$ , $-V_{CC} = -18V$ , Mode = "Sample", Logic = 7V |                    |      | 10        | $\mu A$    | 1, 2, 3    |
|                |                              | $+V_{CC} = 18V$ , $-V_{CC} = -18V$ , Mode = "Hold", Logic = -30V |                    |      | 1.0       | $\mu A$    | 1          |
|                |                              |                                                                  |                    |      | 0.5       | $\mu A$    | 2, 3       |
| $V_{OS}$       | Input Offset Voltage         | $+V_{CC} = 15V$ , $-V_{CC} = -15V$ , $I_{Drive} = +1mA$          |                    | -3.5 | 3.5       | mV         | 1          |
|                |                              |                                                                  |                    | -6.0 | 6.0       | mV         | 2, 3       |
| Delta $V_{OS}$ | Input Offset Voltage         | $+V_{CC} = 15V$ , $-V_{CC} = -15V$ , $I_{Drive} = +1mA$ to -1mA  |                    | -1.1 | 1.1       | mV         | 1          |
|                |                              |                                                                  |                    | -2.0 | 2.0       | mV         | 2, 3       |
| $I_{OS+}$      | Output Short Circuit Current | $+V_{CC} = 18V$ , $-V_{CC} = -18V$                               |                    | 7.0  | 20        | mA         | 1          |
| $I_{OS-}$      | Output Short Circuit Current | $+V_{CC} = 18V$ , $-V_{CC} = -18V$                               |                    | -25  | -7.0      | mA         | 1          |
| $I_{LogicRef}$ | Logic Reference Pin Current  | $+V_{CC} = 18V$ , $-V_{CC} = -18V$ , Mode = "Sample", Logic = 7V |                    | -1.0 | 1.0       | $\mu A$    | 1          |
|                |                              |                                                                  |                    | -0.5 | 5.0       | $\mu A$    | 2, 3       |
|                |                              | $+V_{CC} = 18V$ , $-V_{CC} = -18V$ , Mode = "Hold", Logic = -30V |                    |      | 10        | $\mu A$    | 1, 2, 3    |

(2) Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1 pF, for instance, will create an additional 0.5 mV step with a 5V logic swing and a 0.01 $\mu F$  hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.

## Electrical Characteristics (continued)

The following specifications apply unless otherwise specified.

$V_{CC} = \pm 15V$ ,  $R_L = 10K\Omega$ ,  $V_{IN} = 0V$ ,  $C_{HOLD} = 0.01 \mu F$ , Logic Reference Pin = 0V, Logic Pin = 4V

| Symbol                | Parameter                    | Conditions                            | Notes              | Min | Max | Unit | Sub-groups |
|-----------------------|------------------------------|---------------------------------------|--------------------|-----|-----|------|------------|
| PSRR                  | Power Supply Rejection Ratio | $+V_{CC} = 10V$ , $-V_{CC} = -15V$    |                    | 80  |     | dB   | 1          |
|                       |                              |                                       |                    | 74  |     | dB   | 2, 3       |
|                       |                              | $+V_{CC} = 15V$ , $-V_{CC} = -10V$    |                    | 80  |     | dB   | 1          |
|                       |                              |                                       |                    | 74  |     | dB   | 2, 3       |
| FTRR                  | Feed Through Rejection Ratio | $+V_{CC} = 3.5V$ , $-V_{CC} = -32.5V$ |                    | 86  |     | dB   | 1          |
|                       |                              |                                       |                    | 74  |     | dB   | 2, 3       |
|                       |                              | $+V_{CC} = 32.5V$ , $-V_{CC} = -3.5V$ |                    | 86  |     | dB   | 1          |
|                       |                              |                                       |                    | 74  |     | dB   | 2, 3       |
| $V_{TH}$              | Differential Logic Level     |                                       | See <sup>(3)</sup> | 0.8 | 2.4 | V    | 1          |
| $V_{OS}$<br>(2nd Stg) | 2nd Stage $V_{OS}$           | $+V_{CC} = 3.5V$ , $-V_{CC} = -32.5V$ |                    | -35 | +35 | mV   | 1          |
|                       |                              |                                       |                    | -50 | +50 | mV   | 2, 3       |
|                       |                              | $+V_{CC} = 3V$ , $-V_{CC} = -7V$      |                    | -35 | +35 | mV   | 1          |
|                       |                              |                                       |                    | -50 | +50 | mV   | 2, 3       |
|                       |                              | $+V_{CC} = 32.5V$ , $-V_{CC} = -3.5V$ |                    | -35 | +35 | mV   | 1          |
|                       |                              |                                       |                    | -50 | +50 | mV   | 2, 3       |
|                       |                              | $+V_{CC} = 7V$ , $-V_{CC} = -3V$      |                    | -35 | +35 | mV   | 1          |
|                       |                              |                                       |                    | -50 | +50 | mV   | 2, 3       |

(3) Parameter tested go no go only for  $V_{th}$  test.

## AC Parameters

The following specifications apply unless otherwise specified.

$V_{CC} = \pm 15V$ ,  $R_L = 10K\Omega$ ,  $V_{IN} = 0V$ ,  $C_{Hold} = 0.01 \mu F$ , Logic Reference Pin = 0V, Logic Pin = 4V

| Symbol   | Parameter        | Conditions                                        | Notes | Min | Max | Unit    | Sub-groups |
|----------|------------------|---------------------------------------------------|-------|-----|-----|---------|------------|
| $T_{AQ}$ | Acquisition Time | Delta $V_{OUT} = 10V$ ,<br>$C_{Hold} = 1000pF$    |       |     | 6.0 | $\mu S$ | 4          |
|          |                  | Delta $V_{OUT} = 10V$ ,<br>$C_{Hold} = 0.01\mu F$ |       |     | 25  | $\mu S$ | 4          |

## DC Parameters: Drift Values

The following conditions apply to all the following parameters, unless otherwise specified.

$V_{CC} = \pm 15V$ ,  $R_L = 10K\Omega$ ,  $V_{IN} = 0V$ ,  $C_{Hold} = 0.01 \mu F$ , Logic Reference Pin = 0V, Logic Pin = 4V

Deltas required for S-Level product ONLY.

| Symbol   | Parameters           | Conditions                         | Notes | Min  | Max | Unit | Sub-groups |
|----------|----------------------|------------------------------------|-------|------|-----|------|------------|
| $V_{OS}$ | Input Offset Voltage | $+V_{CC} = 15V$ , $-V_{CC} = -15V$ |       | -0.5 | 0.5 | mV   | 1          |
| $I_{IB}$ | Input Bias Current   | $+V_{CC} = 15V$ , $-V_{CC} = -15V$ |       | -2.5 | 2.5 | nA   | 1          |

## Typical Performance Characteristics

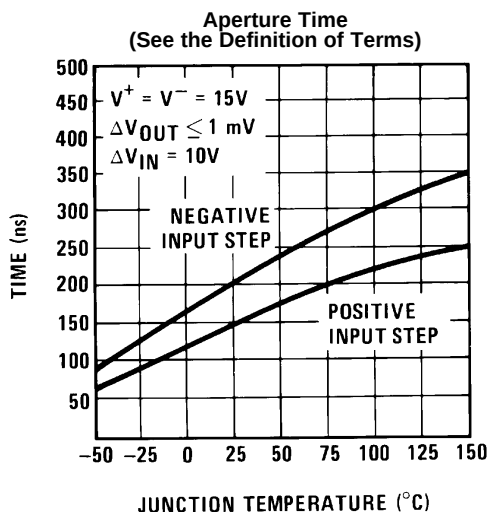


Figure 5.

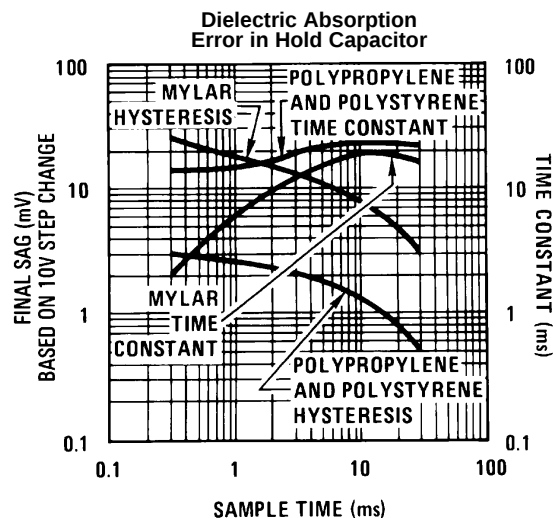


Figure 6.

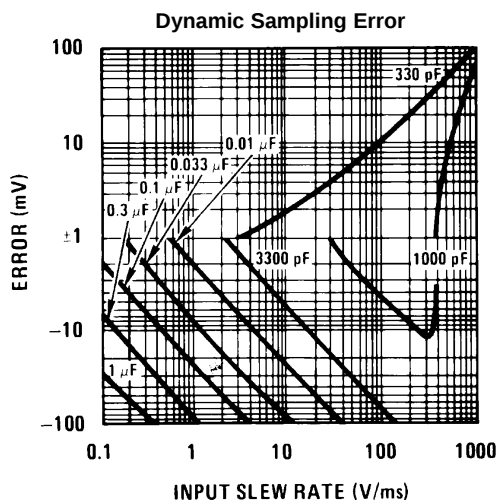


Figure 7.

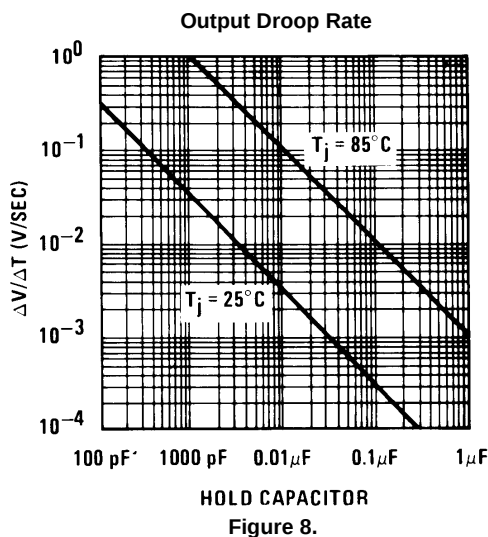


Figure 8.

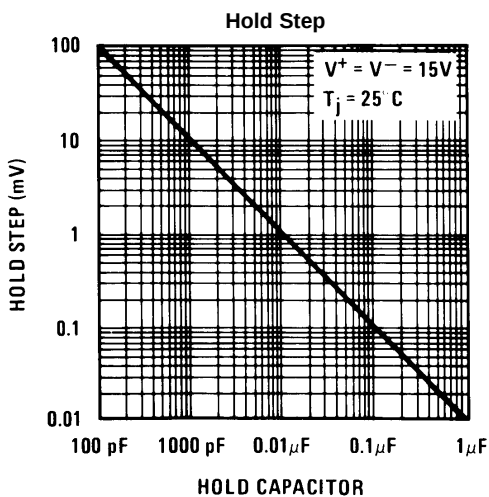


Figure 9.

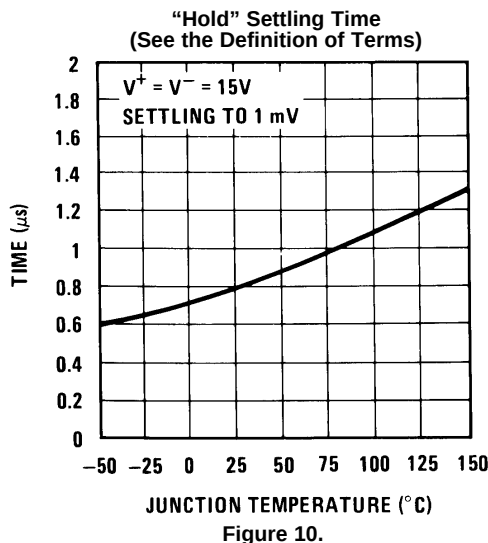
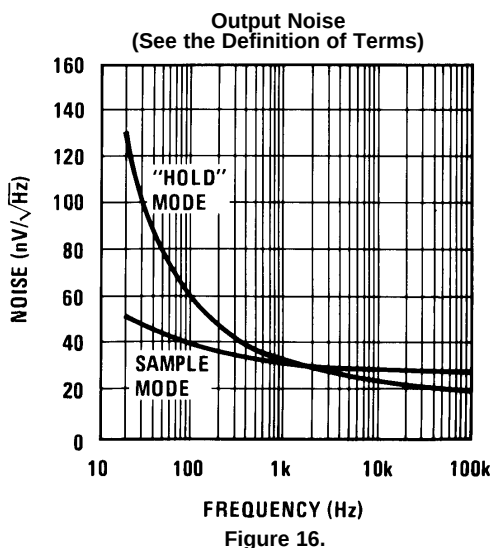
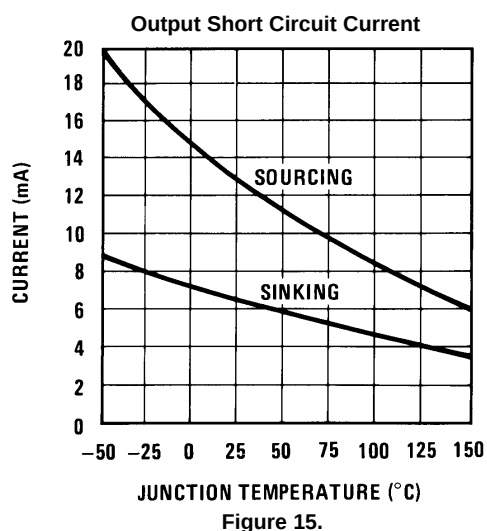
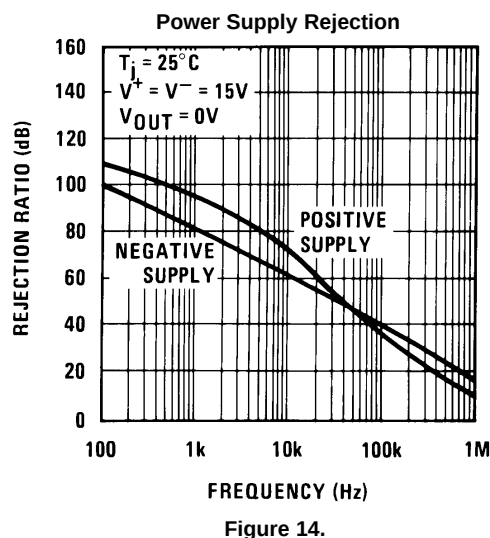
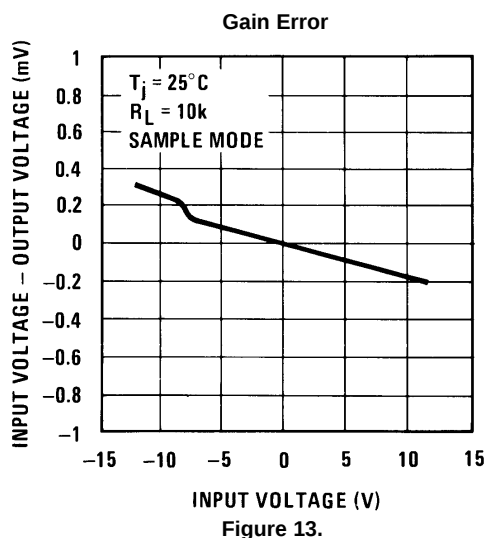
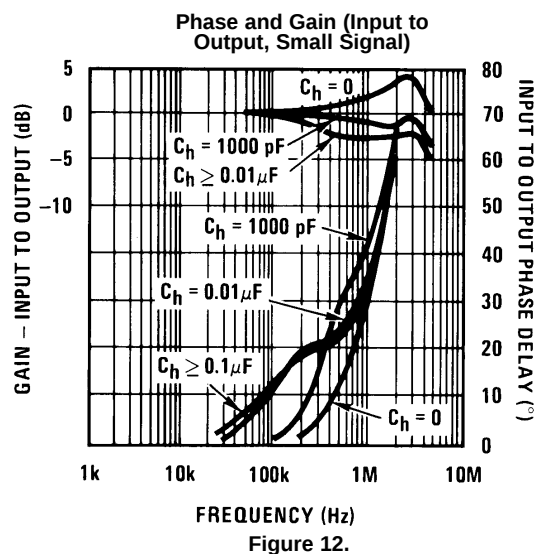
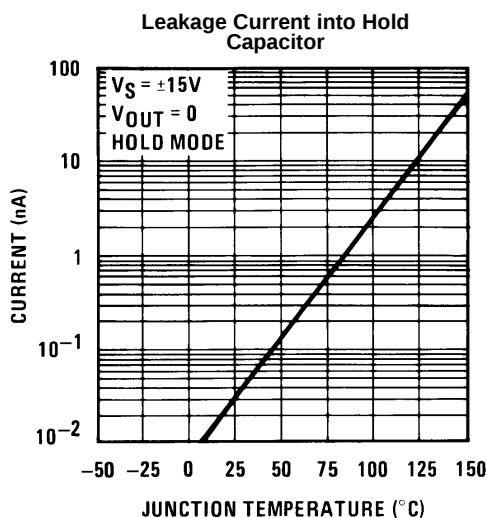
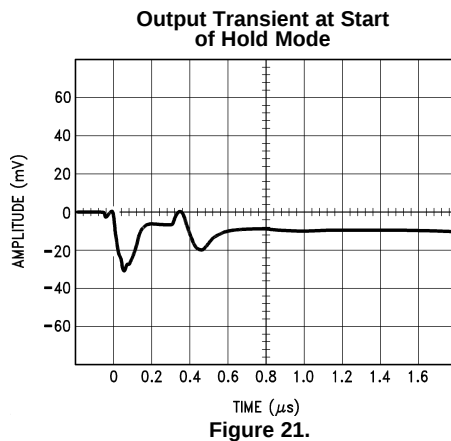
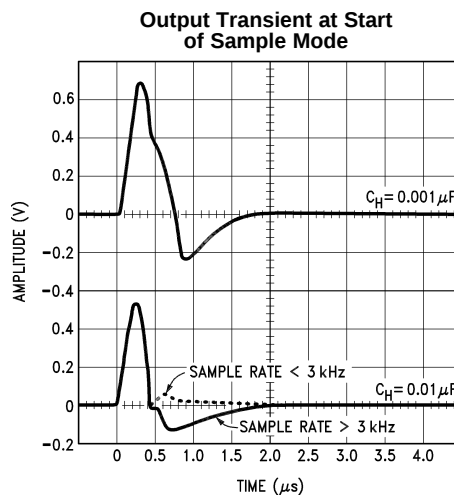
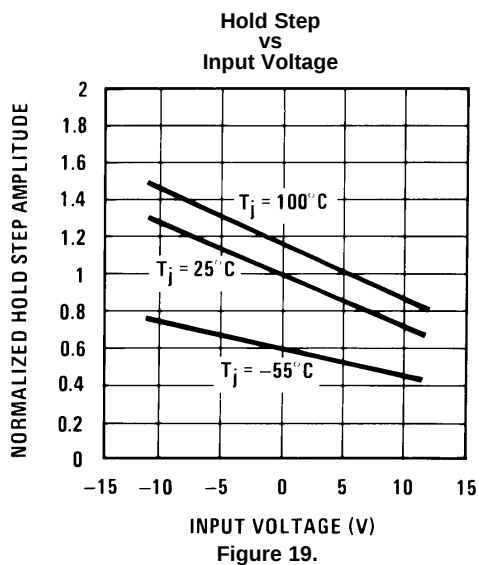
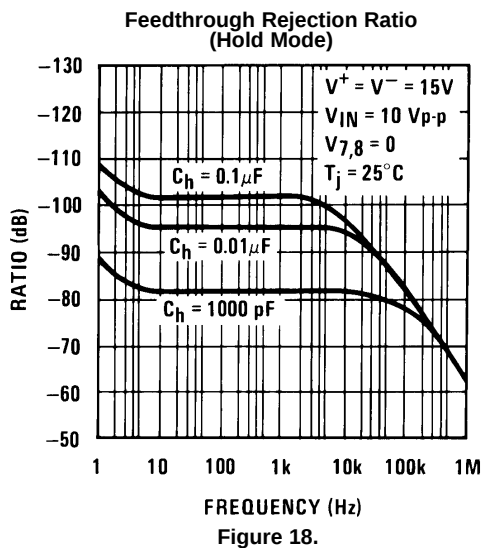
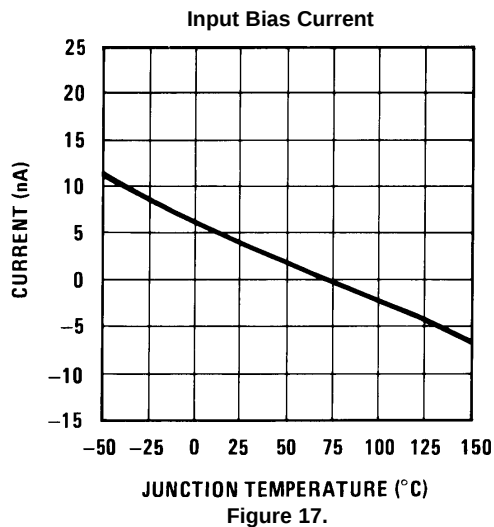


Figure 10.

## Typical Performance Characteristics (continued)



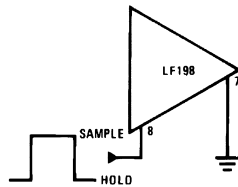
## Typical Performance Characteristics (continued)



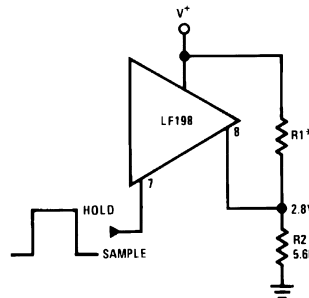
## Logic Input Configurations

### TTL & CMOS

$3V \leq V_{\text{LOGIC}} \text{ (Hi State)} \leq 7V$



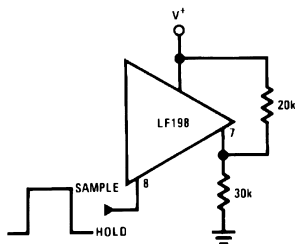
Threshold = 1.4V



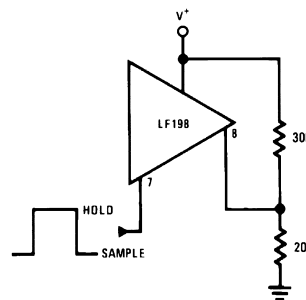
Threshold = 1.4V \* Select for 2.8V at pin 8

### CMOS

$7V \leq V_{\text{LOGIC}} \text{ (Hi State)} \leq 15V$

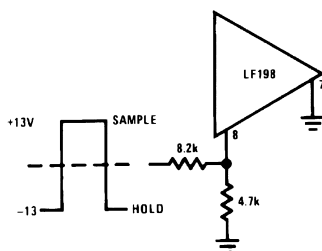


Threshold = 0.6 (V<sup>+</sup>) + 1.4V

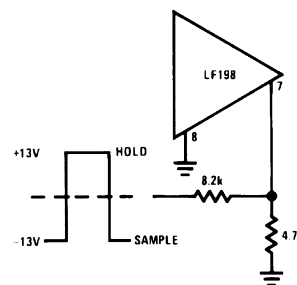


Threshold = 0.6 (V<sup>+</sup>) - 1.4V

### Op Amp Drive



Threshold ≈ +4V



Threshold = -4V

## APPLICATION INFORMATION

### HOLD CAPACITOR

Hold step, acquisition time, and droop rate are the major trade-offs in the selection of a hold capacitor value. Size and cost may also become important for larger values. Use of the curves included with this data sheet should be helpful in selecting a reasonable value of capacitance. Keep in mind that for fast repetition rates or tracking fast signals, the capacitor drive currents may cause a significant temperature rise in the LF198.

A significant source of error in an accurate sample and hold circuit is dielectric absorption in the hold capacitor. A mylar cap, for instance, may “sag back” up to 0.2% after a quick change in voltage. A long sample time is required before the circuit can be put back into the hold mode with this type of capacitor. Dielectrics with very low hysteresis are polystyrene, polypropylene, and Teflon. Other types such as mica and polycarbonate are not nearly as good. The advantage of polypropylene over polystyrene is that it extends the maximum ambient temperature from 85°C to 100°C. Most ceramic capacitors are unusable with > 1% hysteresis. Ceramic “NPO” or “COG” capacitors are now available for 125°C operation and also have low dielectric absorption. For more exact data, see the curve *Dielectric Absorption Error*. The hysteresis numbers on the curve are final values, taken after full relaxation. The hysteresis error can be significantly reduced if the output of the LF198 is digitized quickly after the hold mode is initiated. The hysteresis relaxation time constant in polypropylene, for instance, is 10–50 ms. If A-to-D conversion can be made within 1 ms, hysteresis error will be reduced by a factor of ten.

### DC AND AC ZEROING

DC zeroing is accomplished by connecting the offset adjust pin to the wiper of a 1 kΩ potentiometer which has one end tied to  $V^+$  and the other end tied through a resistor to ground. The resistor should be selected to give  $\approx 0.6$  mA through the 1k potentiometer.

AC zeroing (hold step zeroing) can be obtained by adding an inverter with the adjustment pot tied input to output. A 10 pF capacitor from the wiper to the hold capacitor will give  $\pm 4$  mV hold step adjustment with a 0.01  $\mu$ F hold capacitor and 5V logic supply. For larger logic swings, a smaller capacitor (< 10 pF) may be used.

### LOGIC RISE TIME

For proper operation, logic signals into the LF198 must have a minimum  $dV/dt$  of 1.0 V/ $\mu$ s. Slower signals will cause excessive hold step. If a R/C network is used in front of the logic input for signal delay, calculate the slope of the waveform at the threshold point to ensure that it is at least 1.0 V/ $\mu$ s.

### SAMPLING DYNAMIC SIGNALS

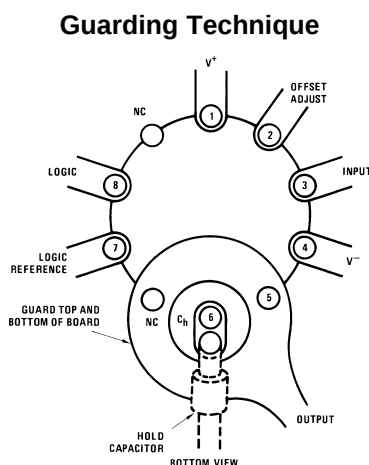
Sample error to moving input signals probably causes more confusion among sample-and-hold users than any other parameter. The primary reason for this is that many users make the assumption that the sample and hold amplifier is truly locked on to the input signal while in the sample mode. In actuality, there are finite phase delays through the circuit creating an input-output differential for fast moving signals. In addition, although the output may have settled, the hold capacitor has an additional lag due to the 300Ω series resistor on the chip. This means that at the moment the “hold” command arrives, the hold capacitor voltage may be somewhat different than the actual analog input. The effect of these delays is opposite to the effect created by delays in the logic which switches the circuit from sample to hold. For example, consider an analog input of 20 Vp-p at 10 kHz. Maximum  $dV/dt$  is 0.6 V/ $\mu$ s. With no analog phase delay and 100 ns logic delay, one could expect up to  $(0.1 \mu s)(0.6 V/\mu s) = 60$  mV error if the “hold” signal arrived near maximum  $dV/dt$  of the input. A positive-going input would give a +60 mV error. Now assume a 1 MHz (3 dB) bandwidth for the overall analog loop. This generates a phase delay of 160 ns. If the hold capacitor sees this exact delay, then error due to analog delay will be  $(0.16 \mu s)(0.6 V/\mu s) = -96$  mV. Total output error is +60 mV (digital) –96 mV (analog) for a total of –36 mV. To add to the confusion, analog delay is proportioned to hold capacitor value while digital delay remains constant. A family of curves (dynamic sampling error) is included to help estimate errors.

A curve labeled *Aperture Time* has been included for sampling conditions where the input is steady during the sampling period, but may experience a sudden change nearly coincident with the “hold” command. This curve is based on a 1 mV error fed into the output.

A second curve, *Hold Settling Time* indicates the time required for the output to settle to 1 mV after the “hold” command.

## DIGITAL FEEDTHROUGH

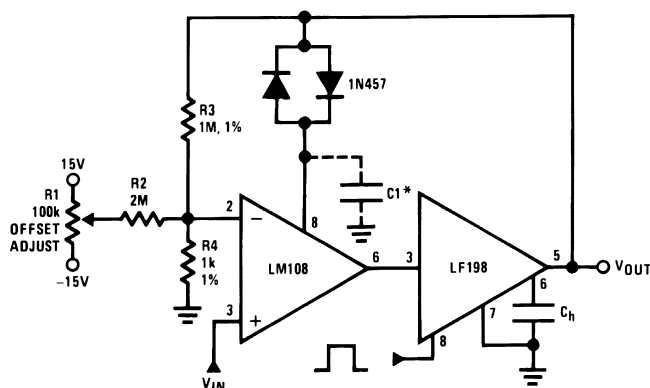
Fast rise time logic signals can cause hold errors by feeding externally into the analog input at the same time the amplifier is put into the hold mode. To minimize this problem, board layout should keep logic lines as far as possible from the analog input and the  $C_h$  pin. Grounded guarding traces may also be used around the input line, especially if it is driven from a high impedance source. Reducing high amplitude logic signals to 2.5V will also help.



**Figure 22. Use 10-pin layout. Guard around  $C_h$  is tied to output.**

## Typical Applications

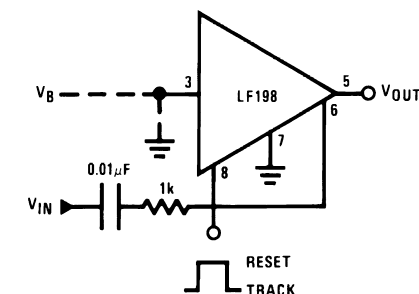
### X1000 Sample & Hold



\*For lower gains, the LM108 must be frequency compensated

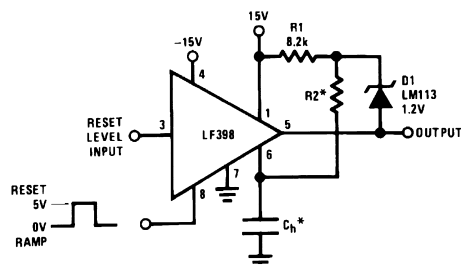
Use  $\approx \frac{100}{A_v}$  pF from comp 2 to ground

### Sample and Difference Circuit (Output Follows Input in Hold Mode)



$$V_{OUT} = V_B + \Delta V_{IN}(\text{HOLD MODE})$$

### Ramp Generator with Variable Reset Level

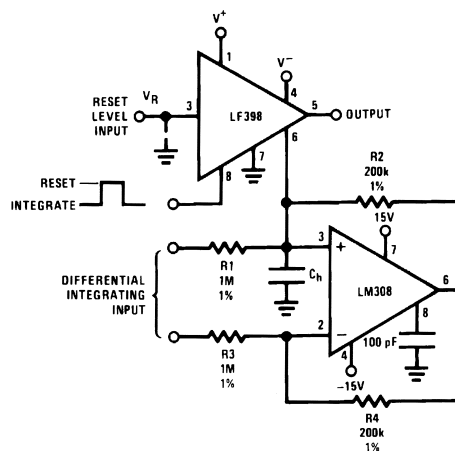


$$\frac{\Delta V}{\Delta T} = \frac{1.2V}{(R2)(C_h)}$$

\*Select for ramp rate

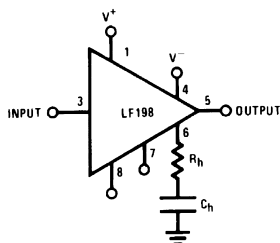
$R2 \geq 10k$

### Integrator with Programmable Reset Level



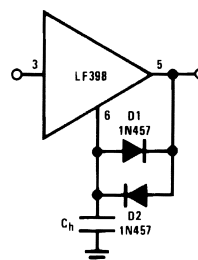
$$V_{OUT}(\text{Hold Mode}) = \left[ \frac{1}{(R1)(C_h)} \int_0^t V_{IN} dt \right] + [V_R]$$

### Output Holds at Average of Sampled Input

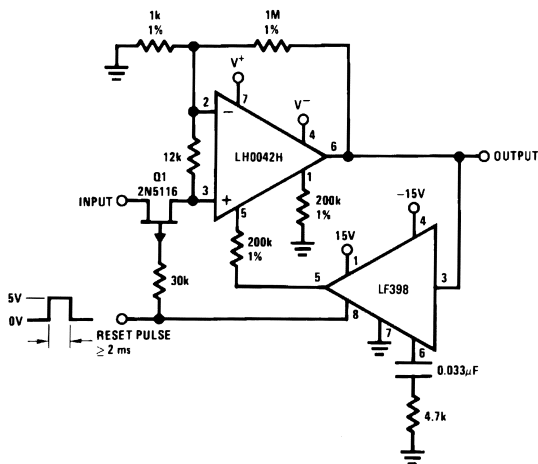


$$\text{Select } (R_h)(C_h) \gg \frac{1}{2\pi f_{IN}(\text{Min})}$$

### Increased Slew Current



### Reset Stabilized Amplifier (Gain of 1000)



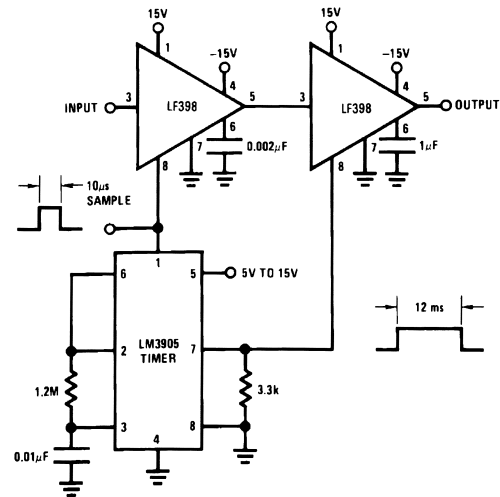
$$V_{OS} \leq 20\mu V \text{ (No trim)}$$

$$Z_{IN} \approx 1 \text{ M}\Omega$$

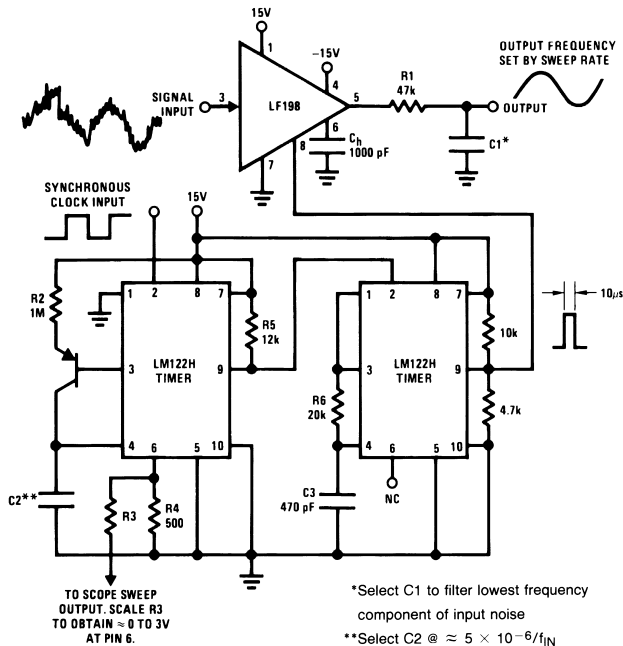
$$\frac{\Delta V_{OS}}{\Delta t} \approx 30\mu V/\text{sec}$$

$$\frac{\Delta V_{OS}}{\Delta T} \approx 0.1\mu V/^{\circ}\text{C}$$

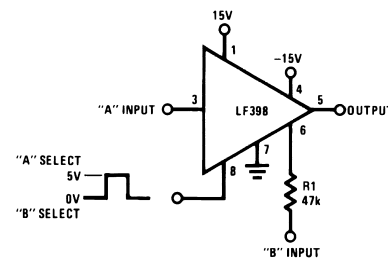
### Fast Acquisition, Low Droop Sample & Hold



### Synchronous Correlator for Recovering Signals Below Noise Level

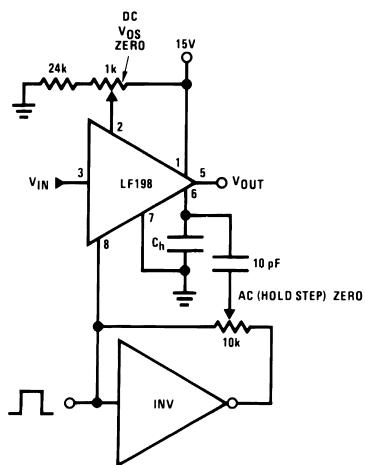


### 2-Channel Switch

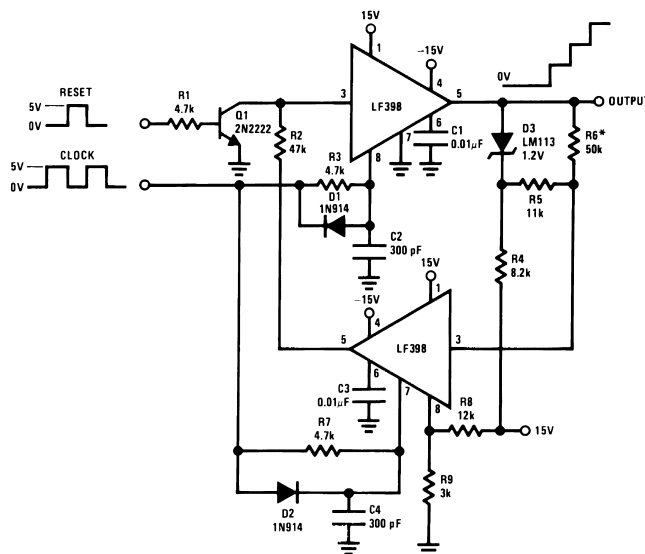


|           | A               | B                 |
|-----------|-----------------|-------------------|
| Gain      | $1 \pm 0.02\%$  | $1 \pm 0.2\%$     |
| $Z_{IN}$  | $10^{10}\Omega$ | 47 k $\Omega$     |
| BW        | $\approx 1$ MHz | $\approx 400$ kHz |
| Crosstalk | -90 dB          | -90 dB            |
| @ 1 kHz   |                 |                   |
| Offset    | $\leq 6$ mV     | $\leq 75$ mV      |

### DC & AC Zeroing

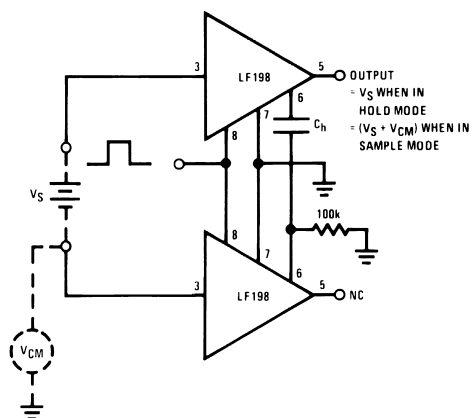


### Staircase Generator

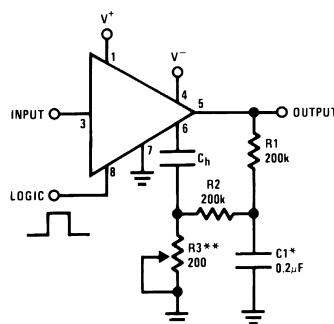


\*Select for step height  
50k  $\rightarrow \approx 1$  V Step

### Differential Hold



### Capacitor Hysteresis Compensation



\*Select for time constant  $C1 = \frac{\tau}{100k}$

\*\*Adjust for amplitude

## Definition of Terms

**Hold Step:** The voltage step at the output of the sample and hold when switching from sample mode to hold mode with a steady (dc) analog input voltage. Logic swing is 5V.

**Acquisition Time:** The time required to acquire a new analog input voltage with an output step of 10V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

**Gain Error:** The ratio of output voltage swing to input voltage swing in the sample mode expressed as a per cent difference.

**Hold Settling Time:** The time required for the output to settle within 1 mV of final value after the “hold” logic command.

**Dynamic Sampling Error:** The error introduced into the held output due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

**Aperture Time:** The delay required between “Hold” command and an input analog transition, so that the transition does not affect the held output.

## REVISION HISTORY SECTION

| Date Released | Revision | Section                       | Originator | Changes                                                                                                                                                                                                                                                    |
|---------------|----------|-------------------------------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 02/25/05      | A        | New release, Corporate format | L. Lytle   | 1 MDS converted to corp. datasheet format. MNLF198–X Rev 3B0 MDS to be archived. Change has been made to Electrical Section, Parameter $I_{OS-}$ . Max limit was 7.0 now is –7.0 confirmed with SG. Added note Parameter tested go no go to $V_{TH}$ test. |
| 03/20/2013    | A        | All Sections                  |            | Changed Layout of National Data Sheet to TI format                                                                                                                                                                                                         |

## PACKAGING INFORMATION

| Orderable part number           | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)                                               |
|---------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|-------------------------------------------------------------------|
| <a href="#">5962-8760801GA</a>  | Active        | Production           | TO-99 (LMC)   8 | 20   JEDEC TRAY (5+1) | No          | Call TI                              | Call TI                           | -55 to 125   | LF198H/883<br>5962-8760801GA Q A<br>CO<br>5962-8760801GA Q ><br>T |
| <a href="#">5962-8760801VZA</a> | Active        | Production           | CFP (NAC)   14  | 88   JEDEC TRAY (5+1) | No          | Call TI                              | Call TI                           | -55 to 125   | LF198WG-<br>QMLV Q<br>5962-87608<br>01VZA ACO<br>01VZA >T         |
| <a href="#">LF198H/883</a>      | Active        | Production           | TO-99 (LMC)   8 | 20   JEDEC TRAY (5+1) | No          | Call TI                              | Call TI                           | -55 to 125   | LF198H/883<br>5962-8760801GA Q A<br>CO<br>5962-8760801GA Q ><br>T |
| <a href="#">LF198WG-QMLV</a>    | Active        | Production           | CFP (NAC)   14  | 88   JEDEC TRAY (5+1) | No          | Call TI                              | Call TI                           | -55 to 125   | LF198WG-<br>QMLV Q<br>5962-87608<br>01VZA ACO<br>01VZA >T         |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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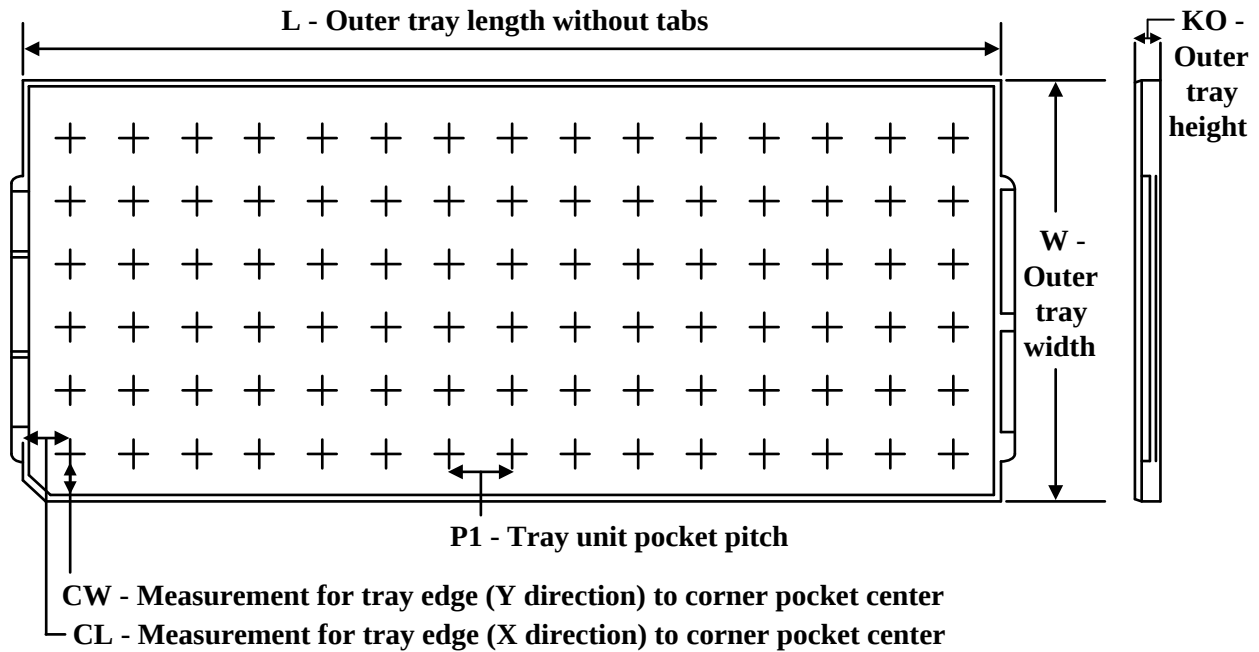
**OTHER QUALIFIED VERSIONS OF LF198QML, LF198QML-SP :**

- Military : [LF198QML](#)
- Space : [LF198QML-SP](#)

NOTE: Qualified Version Definitions:

- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

\*All dimensions are nominal

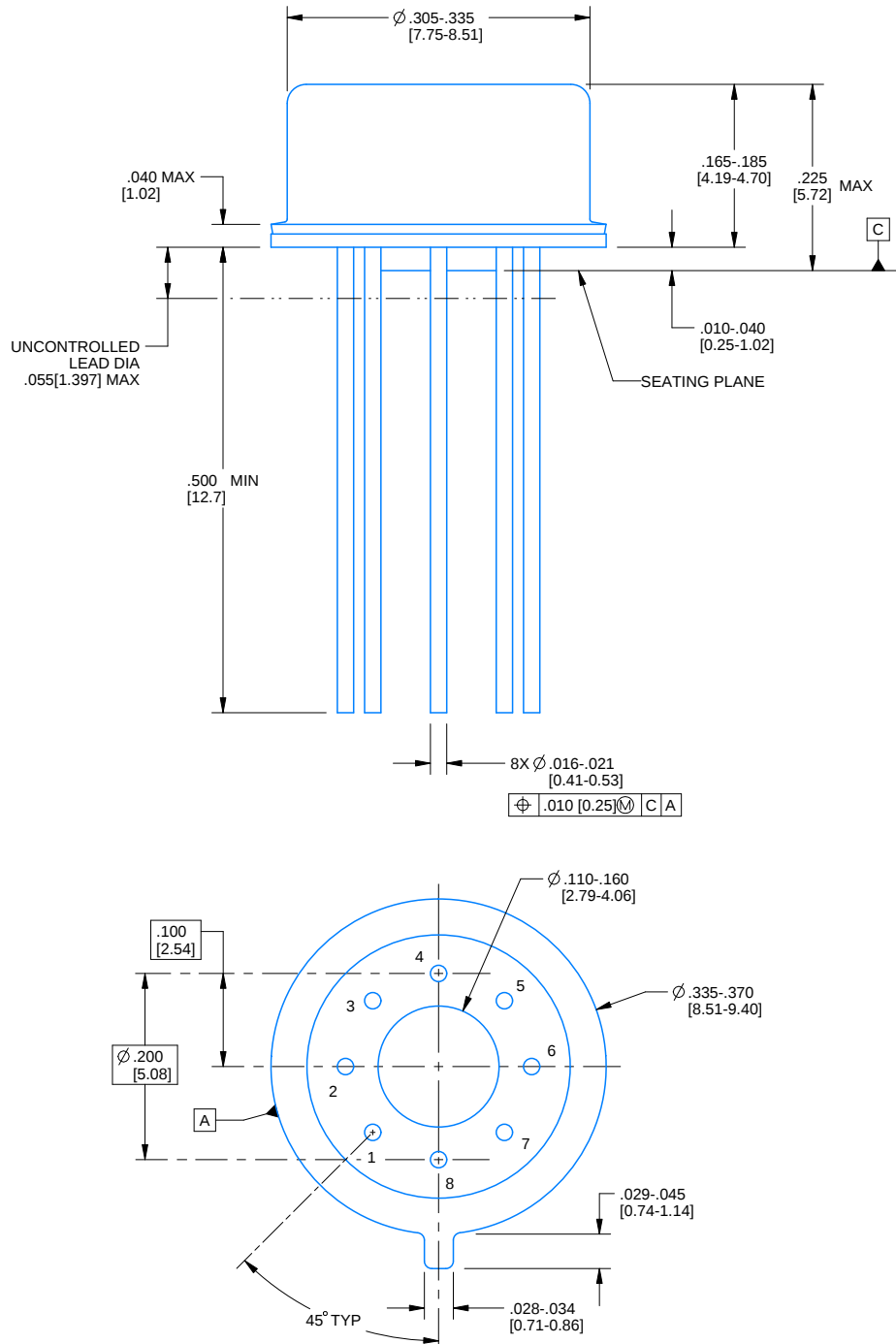
| Device         | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|----------------|--------------|--------------|------|-----|-------------------|----------------------|--------|--------|---------|---------|---------|---------|
| 5962-8760801GA | LMC          | TO-CAN       | 8    | 20  | 2 X 10            | 150                  | 126.49 | 61.98  | 8890    | 11.18   | 12.95   | 18.54   |
| LF198H/883     | LMC          | TO-CAN       | 8    | 20  | 2 X 10            | 150                  | 126.49 | 61.98  | 8890    | 11.18   | 12.95   | 18.54   |

# PACKAGE OUTLINE

LMC0008A

TO-CAN - 5.72 mm max height

TRANSISTOR OUTLINE



4220610/B 09/2024

## NOTES:

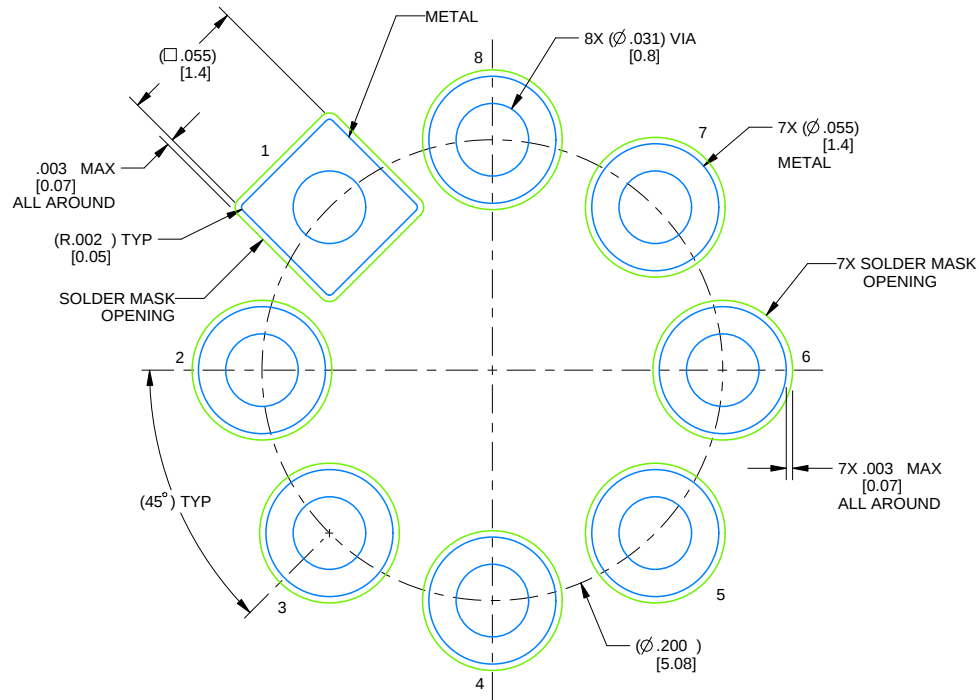
1. All linear dimensions are in inches [millimeters]. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pin numbers shown for reference only. Numbers may not be marked on package.
4. Reference JEDEC registration MO-002/TO-99.

# EXAMPLE BOARD LAYOUT

LMC0008A

TO-CAN - 5.72 mm max height

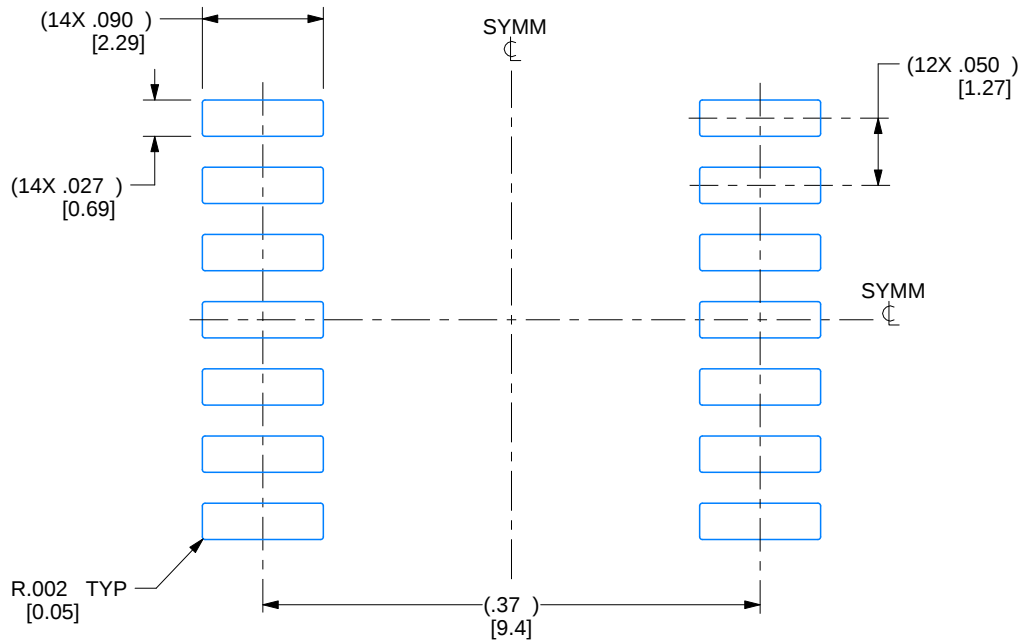
TRANSISTOR OUTLINE



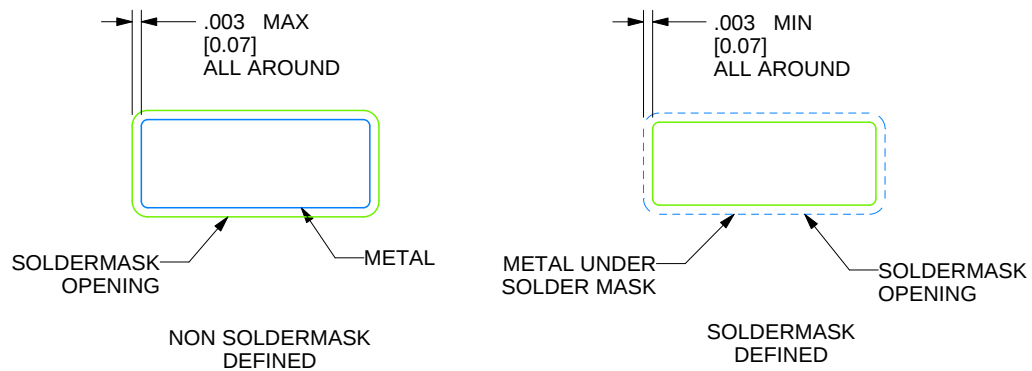
LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 12X

4220610/B 09/2024





RECOMMENDED LAND PATTERN



REVISIONS

| REV | DESCRIPTION                                      | E.C.N.  | DATE       | BY/APP'D                |
|-----|--------------------------------------------------|---------|------------|-------------------------|
| A   | RELEASE TO DOCUMENT CONTROL                      | 2197878 | 12/30/2021 | DAVID CHIN / ANIS FAUZI |
| B   | NO CHANGE TO DRAWING; REVISION FOR YODA RELEASE; | 2198833 | 02/15/2022 | K. SINCERBOX            |
| C   | .3870± .0030 WAS .39000± .00012;                 | 2200916 | 08/08/2022 | D. CHIN / K. SINCERBOX  |

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Last updated 10/2025