LM111QML Voltage Comparator

Check for Samples: LM111QML

FEATURES

- **Available with radiation ensured**
  - **High Dose Rate 50 krad(Si)**
  - **Low Dose and ELDRS Free 100 krad(Si)**
- **Operates from single 5V supply**
- **Input current: 200 nA max. over temperature**
- **Offset current: 20 nA max. over temperature**
- **Differential input voltage range: ±30V**
- **Power consumption: 135 mW at ±15V**
- **Power supply voltage, single 5V to ±15V**
- **Offset voltage null capability**
- **Strobe capability**

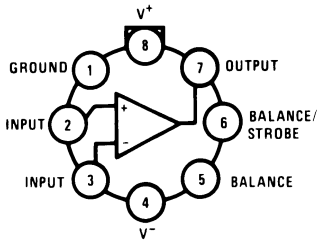
DESCRIPTION

The LM111 is a voltage comparator that has input currents nearly a thousand times lower than devices such as the LM106 or LM710. It is also designed to operate over a wider range of supply voltages: from standard ±15V op amp supplies down to the single 5V supply used for IC logic. The output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, it can drive lamps or relays, switching voltages up to 50V at currents as high as 50 mA.

Both the inputs and the output of the LM111 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the LM106 and LM710 (200 ns response time vs 40 ns) the device is also much less prone to spurious oscillations. The LM111 has the same pin configuration as the LM106 and LM710.

Connection Diagrams

TO-99 Package



Note: Pin 4 connected to case

Figure 1. Top View
Package Number LMC0008C

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CDIP Package

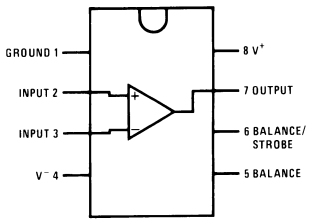


Figure 2. Top View
Package Number NAB008A

CDIP Package

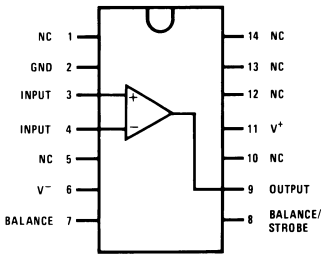


Figure 3. Top View
Package Number J0014A

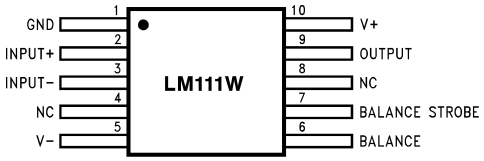


Figure 4. Top View
Package Number NAC0010A, NAD0010A

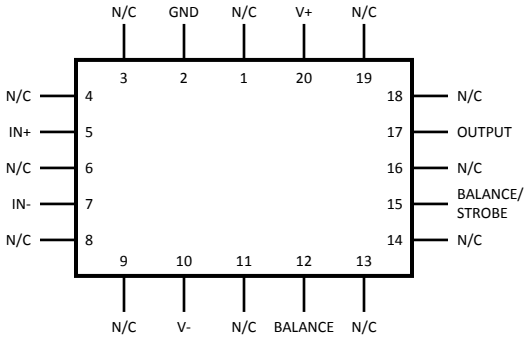
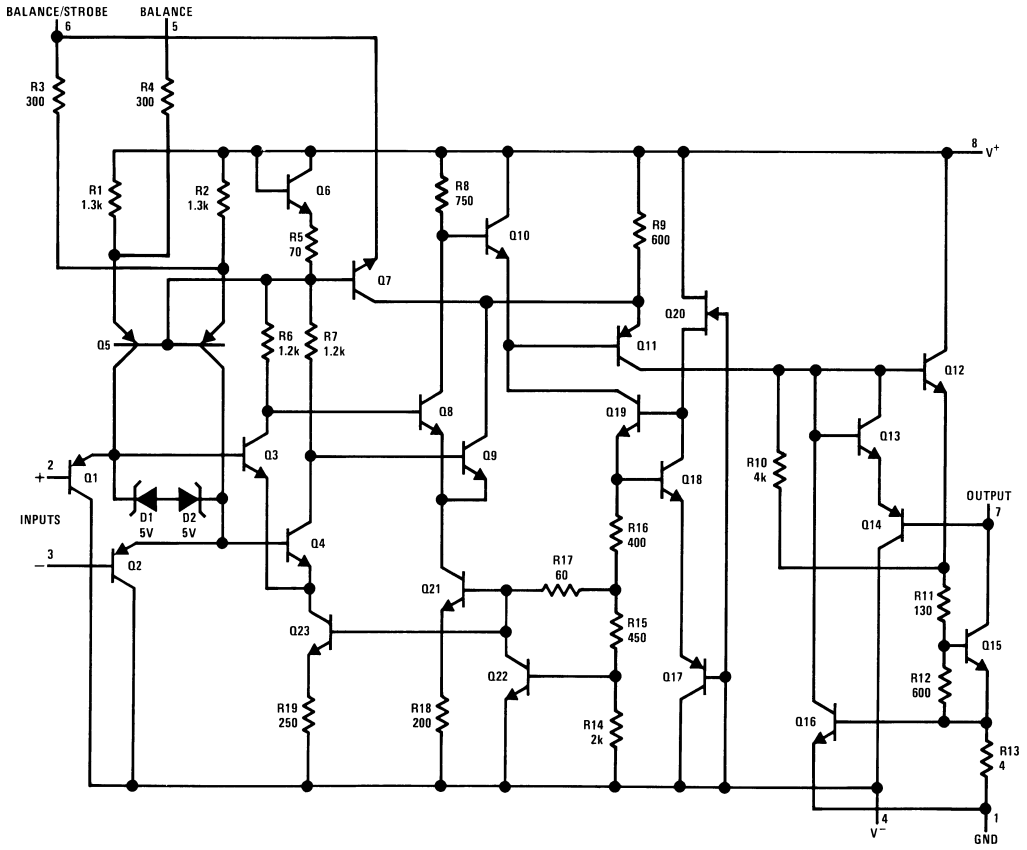


Figure 5. Top View
Package Number NAJ0020A

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Schematic Diagram



Pin connections shown on schematic diagram are for LMC0008C package.

Figure 6.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Positive Supply Voltage	+30.0V
Negative Supply Voltage	-30.0V
Total Supply Voltage	36V
Output to Negative Supply Voltage	50V
GND to Negative Supply Voltage	30V
Differential Input Voltage	±30V
Sink Current	50mA
Input Voltage (2)	±15V
Power Dissipation (3)	
8 LD CDIP	400mW at 25°C
8 LD TO-99	330mW at 25°C
10 LD CLGA	330mW at 25°C
10 LD CLGA	330mW at 25°C
20 LD LCCC	500mW at 25°C
Output Short Circuit Duration	10 seconds
Maximum Strobe Current	10mA
Operating Temperature Range	$-55°C \le T_A \le 125°C$
Thermal Resistance	
θ_{JA}	
8 LD CDIP (Still Air at 0.5W)	134°C/W
8 LD CDIP (500LF/Min Air flow at 0.5W)	76°C/W
8 LD TO-99 (Still Air at 0.5W)	162°C/W
8 LD TO-99 (500LF/Min Air flow at 0.5W)	92°C/W
10 LD CLGA (Still Air at 0.5W)	231°C/W
10 LD CLGA (500LF/Min Air flow at 0.5W)	153°C/W
10 LD CLGA (Still Air at 0.5W)	231°C/W
10 LD CLGA (500LF/Min Air flow at 0.5W)	153°C/W
14 LD CDIP(Still Air at 0.5W)	97°C/W
14 LD CDIP (500LF/Min Air flow at 0.5W)	65°C/W
20 LD LCCC (Still Air at 0.5W)	90°C/W
20 LD LCCC (500LF/Min Air flow at 0.5W)	65°C/W
θ_{JC}	
8 LD CDIP	21°C/W
8 LD TO-99	50°C/W
10 LD CLGA	24°C/W
10 LD CLGA	24°C/W
14 LD CDIP	20°C/W
20 LD LCCC	21°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For specifications and test conditions, see the Electrical Characteristics tables. The specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

(2) This rating applies for ±15V supplies. The positive input voltage limits is 30 V above the negative supply. The negative input voltage limits is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

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Absolute Maximum Ratings (1) (continued)

Storage Temperature Range	$-65°C \le T_A \le 150°C$
Maximum Junction Temperature	175°C
Lead Temperature (Soldering, 60 seconds)	300°C
Voltage at Strobe Pin	$V^+ = -5V$
Package Weight (Typical)	
8 LD TO-99	965mg
8 LD CDIP	1100mg
10 LD CLGA	250mg
10 LD CLGA	225mg
14 LD CDIP	TBD
20 LD LCCC	TBD
ESD Rating (4)	300V

(4) Human body model, 1.5 kΩ in series with 100 pF.

Recommended Operating Conditions

Supply Voltage	$V_{CC} = \pm 15V_{DC}$
Operating Temperature Range	$-55°C \le T_A \le 125°C$

Quality Conformance Inspection

Table 1. Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temperature (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

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LM111/883 Electrical Characteristics DC Parameters(1)

The following conditions apply, unless otherwise specified. V_{56} = 0, R_S = 0 Ω, V_{CC} = ±15V, V_{CM} = 0, V_O = 1.4V WRT −V_{CC}
The pin assignments are based on the 8 pin package configuration. (2)

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
I_{IO}	Input Offset Current	V_{CM} = 13.5V, R_S = 50KΩ		-10	10	nA	1
				-20	20	nA	2, 3
		V_{CM} = 13.5V, V_{85} = V_{86} = 0V, R_S = 50KΩ	(2)	-30	30	nA	1
		V_{CM} = -14.5V, R_S= 50KΩ		-10	10	nA	1
				-20	20	nA	2, 3
		V_{CM} = -14.5V, V_{85} = V_{86} = 0V, R_S= 50KΩ	(2)	-30	30	nA	1
		R_S = 50KΩ		-10	10	nA	1
				-20	20	nA	2, 3
		V_{85} = V_{86} = 0V, R_S = 50KΩ	(2)	-30	30	nA	1
I_{IB}	Input Bias Current	V_{CM} = 13.5V, R_S = 50KΩ			100	nA	1
					150	nA	2, 3
		V_{CM} = -14.5V, R_S = 50KΩ			100	nA	1
					150	nA	2, 3
		R_S = 50KΩ			100	nA	1
					150	nA	2, 3
I_{OL}	Output Leakage Current	V_{CC} = ± 18V, I_5 + I_6 = 5mA, V_O = 35V WRT -V_{CC}	(2)		10	nA	1
			(2)		500	nA	2, 3
I_{GL}	Ground Leakage Current	V_{CC} = ± 18V, I_5 + I_6 = 5mA, V_O = 50V WRT -V_{CC}	(2)		25	nA	1
			(2)		500	nA	2
V_{Sat}	Saturation Voltage	V_I = -5mV, I_7 = 50mA	(2)		1.5	V	1, 2, 3
		V_I = -6mV, I_7 = 8mA	(2)		0.4	V	1, 2, 3
-I_{CC}	Negative Supply Current				5.0	mA	1, 2
					15	mA	3
+I_{CC}	Positive Supply Current				6.0	mA	1, 2
					15	mA	3
I_{L1}	Input Leakage Current	V_{CC} = ± 18V, V_{28} = 1V, V_{38} = 30V, I_5 + I_6 = 5mA V_O = 50V WRT -V_{CC}	(2)		10	nA	1
			(2)		30	nA	2
I_{L2}	Input Leakage Current	V_{CC} = ± 18V, V_{38} = 1V, V_{28} = 30V, I_5 + I_6 = 5mA V_O = 50V WRT -V_{CC}	(2)		10	nA	1
			(2)		30	nA	2
V_OSt	Collector Output Voltage (Strobe)			14		V	1
		I_{St} = 3mA		14		V	1

(1) Calculated parameter.
(2) Pin names based on an 8 pin package configuration. When using higher pin count packages then: Pin 2 & 3 are Inputs, Pin 5 is Balance, Pin 6 is Balance /Strobe, Pin 7 is Output, and Pin 8 is V^+. For example: V_{56} is the Voltage between the Balance and Balance / Strobe pins.

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LM111/883 Electrical Characteristics DC Parameters(1) (continued)

The following conditions apply, unless otherwise specified. V_{56} = 0, R_S = 0 Ω, V_{CC} = ±15V, V_{CM} = 0, V_O = 1.4V WRT −V_{CC}
The pin assignments are based on the 8 pin package configuration. (2)

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	V_{CM} = 13.5V		-3.0	3.0	mV	1
				-4.0	4.0	mV	2, 3
		V_{CM} = 13.5V, V_{85} = V_{86}= 0V	(2)	-3.0	3.0	mV	1
		V_{CM} = -14.5V		-3.0	3.0	mV	1
				-4.0	4.0	mV	2, 3
		V_{CM} = -14.5V, V_{85} = V_{86} = 0V	(2)	-3.0	3.0	mV	1
				-3.0	3.0	mV	1
				-4.0	4.0	mV	2, 3
		V_{85} = V_{86} = 0V	(2)	-3.0	3.0	mV	1
		V_O = 0.4V, +V_{CC} = 4.5V, -V_{CC} = 0V, V_{CM} = 3V		-5.0	5.0	mV	1
				-6.0	6.0	mV	2, 3
		V_O = 4.5V, +V_{CC} = 4.5V, -V_{CC} = 0V, V_{CM} = 3V		-3.0	3.0	mV	1
				-4.0	4.0	mV	2, 3
		V_O = 0.4V, +V_{CC} = 4.5V, -V_{CC} = 0V, V_{CM} = 0.5V		-5.0	5.0	mV	1
				-6.0	6.0	mV	2, 3
		V_O = 4.5V, +V_{CC} = 4.5V, -V_{CC} = 0V, V_{CM} = 0.5V		-3.0	3.0	mV	1
				-4.0	4.0	mV	2, 3
A_{VS}	Large Signal Gain	-12V ≤ V_O ≤ 35V, R_L = 1KΩ	(3)	40		V/mV	4
			(3)	30		V/mV	5, 6

(3) Datalog reading in K=V/mV.

LM111/883 Electrical Characteristics AC Parameters(1)

The following conditions apply, unless otherwise specified. V_{56} = 0, R_S = 0 Ω, V_{CC} = ±15V, V_{CM} = 0, V_O = 1.4V WRT −V_{CC}
The pin assignments are based on the 8 pin package configuration. (2)

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
tR	Response Time				400	nS	7

(1) Calculated parameter.
(2) Pin names based on an 8 pin package configuration. When using higher pin count packages then: Pin 2 & 3 are Inputs, Pin 5 is Balance, Pin 6 is Balance /Strobe, Pin 7 is Output, and Pin 8 is V^+. For example: V_{56} is the Voltage between the Balance and Balance / Strobe pins.

LM111-SMD Electrical Characteristics SMD 5962-8687701 DC Parameters(1)

The following conditions apply, unless otherwise specified. V_{CC} = ±15V, V_{CM} = 0

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	V_I = 0V, R_S = 50Ω		-3.0	+3.0	mV	1
				-4.0	+4.0	mV	2, 3
		+V_{CC} = 29.5V, -V_{CC} = -0.5V, V_I = 0V, V_{CM} = -14.5V, R_S = 50Ω		-3.0	+3.0	mV	1
				-4.0	+4.0	mV	2, 3
		+V_{CC} = 2V, -V_{CC} = -28V, V_I = 0V, V_{CM} = +13V, R_S = 50Ω		-3.0	+3.0	mV	1
				-4.0	+4.0	mV	2, 3
		+V_{CC} = +2.5V, -V_{CC} = -2.5V, V_I = 0V, R_S = 50Ω		-3.0	+3.0	mV	1
				-4.0	+4.0	mV	2, 3

(1) Calculated parameter.

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LM111-SMD Electrical Characteristics SMD 5962-8687701 DC Parameters(1) (continued)

The following conditions apply, unless otherwise specified. V_{CC} = ±15V, V_{CM} = 0

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO} R	Raised Input Offset Voltage	V_I = 0V, R_S = 50Ω	(2)	-3.0	+3.0	mV	1
				-4.5	+4.5	mV	2, 3
		+V_{CC} = 29.5V, -V_{CC} = -0.5V, V_I = 0V, V_{CM} = -14.5V, R_S = 50Ω	(2)	-3	+3	mV	1
				-4.5	+4.5	mV	2, 3
		+V_{CC} = 2V, -V_{CC} = -28V, V_I = 0V, V_{CM} = +13V, R_S = 50Ω	(2)	-3.0	+3.0	mV	1
				-4.5	+4.5	mV	2, 3
I_{IO}	Input Offset Current	V_I = 0V, R_S = 50KΩ		-10	+10	nA	1, 2
				-20	+20	nA	3
		+V_{CC} = 29.5V, -V_{CC} = -0.5V, V_I = 0V, V_{CM} = -14.5V, R_S = 50KΩ		-10	+10	nA	1, 2
				-20	+20	nA	3
		+V_{CC} = 2V, -V_{CC} = -28V, V_I = 0V, V_{CM} = +13V, R_S = 50KΩ		-10	+10	nA	1, 2
				-20	+20	nA	3
I_{IO}R	Raised Input Offset Current	V_I = 0V, R_S = 50KΩ	(2)	-25	+25	nA	1, 2
				-50	+50	nA	3
±I_{IB}	Input Bias Current	V_I = 0V, R_S = 50KΩ		-100	0.1	nA	1, 2
				-150	0.1	nA	3
		+V_{CC} = 29.5V, -V_{CC} = -0.5V, V_I = 0V, V_{CM} = -14.5V, R_S = 50KΩ		-150	0.1	nA	1, 2
				-200	0.1	nA	3
		+V_{CC} = 2V, -V_{CC} = -28V, V_I = 0V, V_{CM} = +13V, R_S = 50KΩ		-150	0.1	nA	1, 2
				-200	0.1	nA	3
V_OSt	Collector Output Voltage (Strobe)	+V_I = Gnd, -V_I = 15V, I_{St} = -3mA, R_S = 50Ω		(3)(4) 14		V	1, 2, 3
CMRR	Common Mode Rejection Ratio	-28V ≤ -V_{CC} ≤ -0.5V, R_S = 50Ω, 2V ≤ +V_{CC} ≤ 29.5V, R_S = 50Ω, -14.5V ≤ V_{CM} ≤ 13V, R_S = 50Ω		80		dB	1, 2, 3
V_{OL}	Low Level Output Voltage	+V_{CC} = 4.5V, -V_{CC} = Gnd, I_O = 8mA, ±V_I = 0.71V, V_{ID} = -6mV			0.4	V	1, 2, 3
		+V_{CC} = 4.5V, -V_{CC} = Gnd, I_O = 8mA, ±V_I = −1.75V, V_{ID} = -6mV			0.4	V	1, 2, 3
		I_O = 50mA, ±V_I = 13V, V_{ID} = -5mV			1.5	V	1, 2, 3
		I_O = 50mA, ±V_I= -14V, V_{ID} = -5mV			1.5	V	1, 2, 3
I_{CEX}	Output Leakage Current	+V_{CC} = 18V, -V_{CC} = -18V, V_O = 32V		-1.0	10	nA	1
				-1.0	500	nA	2
I_L	Input Leakage Current	+V_{CC} = 18V, -V_{CC} = -18V, +V_I = +12V, -V_I = -17V	(5)	-5.0	500	nA	1, 2, 3
		+V_{CC} = 18V, -V_{CC} = -18V, +V_I = -17V, -V_I = +12V	(5)	-5.0	500	nA	1, 2, 3
+I_{CC}	Power Supply Current				6.0	mA	1, 2
					7.0	mA	3

(2) Subscript (R) indicates tests which are performed with input stage current raised by connecting BAL and BAL/STB terminals to +V_{CC}.
(3) I_{ST} = −2mA at −55°C
(4) Group A sample ONLY
(5) V_{ID} is voltage difference between inputs.

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LM111-SMD Electrical Characteristics SMD 5962-8687701 DC Parameters(1) (continued)

The following conditions apply, unless otherwise specified. V_{CC} = ±15V, V_{CM} = 0

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
$-I_{CC}$	Power Supply Current			-5.0		mA	1, 2
				-6.0		mA	3
$\Delta V_{IO} / \Delta T$	Temperature Coefficient Input Offset Voltage	25°C ≤ T ≤ 125°C	(5) (4)	-25	25	µV/°C	2
		-55°C ≤ T ≤ 25°C	(5) (4)	-25	25	µV/°C	3
$\Delta I_{IO} / \Delta T$	Temperature Coefficient Input Offset Current	25°C ≤ T ≤ 125°C	(5) (4)	-100	100	pA/°C	2
		-55°C ≤ T ≤ 25°C	(5) (4)	-200	200	pA/°C	3
I_{OS}	Short Circuit Current	V_O = 5V, t ≤ 10mS, $-V_I$ = 0.1V, $+V_I$ = 0V	(6)		200	mA	1
			(6)		150	mA	2
			(6)		250	mA	3
$+V_{IO}$ adj.	Input Offset Voltage (Adjustment)	V_O = 0V, V_I = 0V, R_S = 50Ω		5.0		mV	1
$-V_{IO}$ adj.	Input Offset Voltage (Adjustment)	V_O = 0V, V_I = 0V, R_S = 50Ω			-5.0	mV	1
$\pm A_{VE}$	Voltage Gain (Emitter)	R_L = 600Ω	(7)	10		V/mV	4
			(7)	8.0		V/mV	5, 6

(6) Actual min. limit used is 5mA due to test setup.
(7) Datalog reading in K=V/mV.

LM111-SMD Electrical Characteristics SMD 5962-8687701 AC Parameters(1)

The following conditions apply, unless otherwise specified. V_{CC} = ±15V, V_{CM} = 0

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
tR_{LHC}	Response Time (Collector Output)	V_{OD}(Overdrive) = -5mV, C_L = 50pF, V_I = -100mV	(2)		300	nS	7, 8B
			(2)		640	nS	8A
tR_{HLC}	Response Time (Collector Output)	V_{OD}(Overdrive) = 5mV, C_L = 50pF, V_I = 100mV	(2)		300	nS	7, 8B
			(2)		500	nS	8A

(1) Calculated parameter.
(2) Group A sample ONLY

LM111 RADIATION Electrical Characteristics SMD 5962L0052401 DC Parameters(1)(2)

The following conditions apply, unless otherwise specified. V_{CC} = ±15V, V_{CM} = 0

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	V_I = 0V, R_S = 50Ω		-3.0	+3.0	mV	1
				-4.0	+4.0	mV	2, 3
		$+V_{CC}$ = 29.5V, $-V_{CC}$ = -0.5V, V_I = 0V, V_{CM} = -14.5V, R_S = 50Ω		-3.0	+3.0	mV	1
				-4.0	+4.0	mV	2, 3
		$+V_{CC}$ = 2V, $-V_{CC}$ = -28V, V_I = 0V, V_{CM} = +13V, R_S = 50Ω		-3.0	+3.0	mV	1
				-4.0	+4.0	mV	2, 3
		$+V_{CC}$ = +2.5V, $-V_{CC}$ = -2.5V, V_I = 0V, R_S = 50Ω		-3.0	+3.0	mV	1
				-4.0	+4.0	mV	2, 3

(1) Calculated parameter.
(2) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are ensured only for the conditions as specified in Mil-Std-883, Method 1019, Condition A.

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LM111 RADIATION Electrical Characteristics SMD 5962L0052401 DC Parameters(1)(2) (continued)

The following conditions apply, unless otherwise specified. V_{CC} = ±15V, V_{CM} = 0

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO} R	Raised Input Offset Voltage	V_I = 0V, R_S = 50Ω	(3)	-3.0	+3.0	mV	1
				-4.5	+4.5	mV	2, 3
		+V_{CC} = 29.5V, -V_{CC} = -0.5V, V_I = 0V, V_{CM} = -14.5V, R_S = 50Ω	(3)	-3.0	+3.0	mV	1
				-4.5	+4.5	mV	2, 3
		+V_{CC} = 2V, -V_{CC} = -28V, V_I = 0V, V_{CM} = +13V, R_S = 50Ω	(3)	-3.0	+3.0	mV	1
				-4.5	+4.5	mV	2, 3
I_{IO}	Input Offset Current	V_I = 0V, R_S = 50KΩ		-10	+10	nA	1, 2
				-20	+20	nA	3
		+V_{CC} = 29.5V, -V_{CC} = -0.5V, V_I = 0V, V_{CM} = -14.5V, R_S = 50KΩ		-10	+10	nA	1, 2
				-20	+20	nA	3
		+V_{CC} = 2V, -V_{CC} = -28V, V_I = 0V, V_{CM} = +13V, R_S = 50KΩ		-10	+10	nA	1, 2
				-20	+20	nA	3
I_{IO}R	Raised Input Offset Current	V_I = 0V, R_S = 50KΩ	(3)	-25	+25	nA	1, 2
				-50	+50	nA	3
±I_{IB}	Input Bias Current	V_I = 0V, R_S = 50KΩ		-100	0.1	nA	1, 2
				-150	0.1	nA	3
		+V_{CC} = 29.5V, -V_{CC} = -0.5V, V_I = 0V, V_{CM} = -14.5V, R_S = 50KΩ		-150	0.1	nA	1, 2
				-200	0.1	nA	3
		+V_{CC} = 2V, -V_{CC} = -28V, V_I = 0V, V_{CM} = +13V, R_S = 50KΩ		-150	0.1	nA	1, 2
				-200	0.1	nA	3
V_OSt	Collector Output Voltage (Strobe)	+V_I = Gnd, -V_I = 15V, I_{St} = -3mA, R_S = 50Ω		(4)(5) 14		V	1, 2, 3
CMRR	Common Mode Rejection Ratio	-28V ≤ -V_{CC} ≤ -0.5V, R_S = 50Ω, 2V ≤ +V_{CC} ≤ 29.5V, R_S = 50Ω, -14.5V ≤ V_{CM} ≤ 13V, R_S = 50Ω		80		dB	1, 2, 3
V_{OL}	Low Level Output Voltage	+V_{CC} = 4.5V, -V_{CC} = Gnd, I_O = 8mA, ±V_I = 0.5V, V_{ID} = -6mV			0.4	V	1, 2, 3
		+V_{CC} = 4.5V, -V_{CC} = Gnd, I_O = 8mA, ±V_I = 3V, V_{ID} = -6mV			0.4	V	1, 2, 3
		I_O = 50mA, ±V_I = 13V, V_{ID} = -5mV			1.5	V	1, 2, 3
		I_O = 50mA, ±V_I = -14V, V_{ID} = -5mV			1.5	V	1, 2, 3
I_{CEX}	Output Leakage Current	+V_{CC} = 18V, -V_{CC} = -18V, V_O = 32V		-1.0	10	nA	1
				-1.0	500	nA	2
I_L	Input Leakage Current	+V_{CC} = 18V, -V_{CC} = -18V, +V_I = +12V, -V_I = -17V	(6)	-5.0	500	nA	1, 2, 3
		+V_{CC} = 18V, -V_{CC} = -18V, +V_I = -17V, -V_I = +12V	(6)	-5.0	500	nA	1, 2, 3
+I_{CC}	Power Supply Current				6.0	mA	1, 2
					7.0	mA	3

(3) Subscript (R) indicates tests which are performed with input stage current raised by connecting BAL and BAL/STB terminals to +V_{CC}.
(4) I_{ST} = −2mA at −55°C
(5) Group A sample ONLY
(6) V_{ID} is voltage difference between inputs.

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LM111 RADIATION Electrical Characteristics SMD 5962L0052401 DC Parameters(1)(2) (continued)

The following conditions apply, unless otherwise specified. V_{CC} = ±15V, V_{CM} = 0

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
$-I_{CC}$	Power Supply Current			-5.0		mA	1, 2
				-6.0		mA	3
ΔV_{IO} / ΔT	Temperature Coefficient Input Offset Voltage	25°C ≤ T ≤ 125°C		-25	25	µV/°C	2
		-55°C ≤ T ≤ 25°C		-25	25	µV/°C	3
ΔI_{IO} / ΔT	Temperature Coefficient Input Offset Current	25°C ≤ T ≤ 125°C		-100	100	pA/°C	2
		-55°C ≤ T ≤ 25°C		-200	200	pA/°C	3
I_{OS}	Short Circuit Current	V_O = 5V, t ≤ 10mS, $-V_I$ = 0.1V, $+V_I$ = 0V	(7)		200	mA	1
			(7)		150	mA	2
			(7)		250	mA	3
$+V_{IO}$ adj.	Input Offset Voltage (Adjustment)	V_O = 0V, V_I = 0V, R_S = 50Ω		5.0		mV	1
$-V_{IO}$ adj.	Input Offset Voltage (Adjustment)	V_O = 0V, V_I = 0V, R_S = 50Ω			-5.0	mV	1
$\pm A_{VE}$	Voltage Gain (Emitter)	R_L = 600Ω	(8)	10		V/mV	4
			(8)	8.0		V/mV	5, 6

(7) Actual min. limit used is 5mA due to test setup.
(8) Datalog reading in K=V/mV.

LM111 RADIATION Electrical Characteristics SMD 5962L0052401 AC Parameters(1)(2)

The following conditions apply, unless otherwise specified. V_{CC} = ±15V, V_{CM} = 0

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
tR_{LHC}	Response Time (Collector Output)	V_{OD}(Overdrive) = -5mV, C_L = 50pF, V_I = -100mV	(3)		300	nS	7, 8B
					640	nS	8A
tR_{HLC}	Response Time (Collector Output)	V_{OD}(Overdrive) = 5mV, C_L = 50pF, V_I = 100mV	(3)		300	nS	7, 8B
					500	nS	8A

(1) Calculated parameter.
(2) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are ensured only for the conditions as specified in Mil-Std-883, Method 1019, Condition A.
(3) Group A sample ONLY

LM111 RADIATION Electrical Characteristics SMD 5962L0052401 DC DELTA Parameters(1)(2)

The following conditions apply, unless otherwise specified. V_{CC} = ±15V, V_{CM} = 0
Delta calculations performed on QMLV devices at group B , subgroup 5.

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	V_I = 0V, R_S = 50Ω		-0.5	0.5	mV	1
		$+V_{CC}$ = 29.5V, $-V_{CC}$ = -0.5V, V_I = 0V, V_{CM} = -14.5V, R_S = 50Ω		-0.5	0.5	mV	1
		$+V_{CC}$ = 2V, $-V_{CC}$ = -28V, V_I = 0V, V_{CM} = +13V, R_S = 50Ω		-0.5	0.5	mV	1

(1) Calculated parameter.
(2) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are ensured only for the conditions as specified in Mil-Std-883, Method 1019, Condition A.

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LM111 RADIATION Electrical Characteristics SMD 5962L0052401 DC DELTA Parameters(1)(2) (continued)

The following conditions apply, unless otherwise specified. V_{CC} = ±15V, V_{CM} = 0
Delta calculations performed on QMLV devices at group B , subgroup 5.

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
$\pm I_{IB}$	Input Bias Current	V_I = 0V, R_S = 50KΩ		-12.5	12.5	nA	1
		$+V_{CC}$ = 29.5V, $-V_{CC}$ = -0.5V, V_I = 0V, V_{CM} = -14.5V, R_S = 50KΩ		-12.5	12.5	nA	1
		$+V_{CC}$ = 2V, $-V_{CC}$ = -28V, V_I = 0V, V_{CM} = +13V, R_S = 50KΩ		-12.5	12.5	nA	1
I_{CEX}	Output Leakage Current	$+V_{CC}$ = 18V, $-V_{CC}$ = -18V, V_O = 32V		-5.0	5.0	nA	1

LM111 RADIATION Electrical Characteristics SMD 5962L0052401 Post Radiation Parameters(1)(2)

The following conditions apply, unless otherwise specified

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
I_{IO}	Input Offset Current	$+V_{CC}$ = 29.5V, $-V_{CC}$ = −0.5V, V_I = 0V, V_{CM} = −14.5V, R_S = 50KΩ		−50	+50	nA	1
		$+V_{CC}$ = 2V, $-V_{CC}$ = −28V, V_I = 0V, V_{CM} = +13V, R_S = 50KΩ		−50	+50	nA	1
$\pm I_{IB}$	Input Bias Current	V_I = 0V, R_S = 50KΩ		−150	0.1	nA	1
		$+V_{CC}$ = 29.5V, $-V_{CC}$ = −0.5V, V_I = 0V, V_{CM} = −14.5V, R_S = 50KΩ		−175	0.1	nA	1
I_{CEX}	Output Leakage Current	$+V_{CC}$ = 18V, $-V_{CC}$ = −18V, V_O = 32V		−25	+25	nA	1

(1) Calculated parameter.
(2) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are ensured only for the conditions as specified in Mil-Std-883, Method 1019, Condition A.

LM111 RADIATION Electrical Characteristics SMD 5962R0052402 DC Parameters(1)(2)

The following conditions apply, unless otherwise specified. V_{CC} = ±15V, V_{CM} = 0

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	V_I = 0V, R_S = 50Ω		-3.0	+3.0	mV	1
				-4.0	+4.0	mV	2, 3
		$+V_{CC}$ = 29.5V, $-V_{CC}$ = -0.5V, V_I = 0V, V_{CM} = -14.5V, R_S = 50Ω		-3.0	+3.0	mV	1
				-4.0	+4.0	mV	2, 3
		$+V_{CC}$ = 2V, $-V_{CC}$ = -28V, V_I = 0V, V_{CM} = +13V, R_S = 50Ω		-3.0	+3.0	mV	1
				-4.0	+4.0	mV	2, 3
		$+V_{CC}$ = +2.5V, $-V_{CC}$ = -2.5V, V_I = 0V, R_S = 50Ω		-3.0	+3.0	mV	1
				-4.0	+4.0	mV	2, 3

(1) Calculated parameter.
(2) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be sensitive in a high dose environment. Low dose rate testing has been performed on a wafer-by-wafer basis, per test method 1019 condition D of MIL-STD-883, with no enhanced low dose rate sensitivity (ELDRS) effect.

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LM111 RADIATION Electrical Characteristics SMD 5962R0052402 DC Parameters[1][2] (continued)

The following conditions apply, unless otherwise specified. V_{CC} = ±15V, V_{CM} = 0

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO} R	Raised Input Offset Voltage	V_I = 0V, R_S = 50Ω	(2)	-3.0	+3.0	mV	1
				-4.5	+4.5	mV	2, 3
		+V_{CC} = 29.5V, -V_{CC} = -0.5V, V_I = 0V, V_{CM} = -14.5V, R_S = 50Ω	(2)	-3.0	+3.0	mV	1
				-4.5	+4.5	mV	2, 3
		+V_{CC} = 2V, -V_{CC} = -28V, V_I = 0V, V_{CM} = +13V, R_S = 50Ω	(2)	-3.0	+3.0	mV	1
				-4.5	+4.5	mV	2, 3
I_{IO}	Input Offset Current	V_I = 0V, R_S = 50KΩ		-10	+10	nA	1, 2
				-20	+20	nA	3
		+V_{CC} = 29.5V, -V_{CC} = -0.5V, V_I = 0V, V_{CM} = -14.5V, R_S = 50KΩ		-10	+10	nA	1, 2
				-20	+20	nA	3
		+V_{CC} = 2V, -V_{CC} = -28V, V_I = 0V, V_{CM} = +13V, R_S = 50KΩ		-10	+10	nA	1, 2
				-20	+20	nA	3
I_{IO}R	Raised Input Offset Current	V_I = 0V, R_S = 50KΩ	(2)	-25	+25	nA	1, 2
				-50	+50	nA	3
±I_{IB}	Input Bias Current	V_I = 0V, R_S = 50KΩ		-100	0.1	nA	1, 2
				-150	0.1	nA	3
		+V_{CC} = 29.5V, -V_{CC} = -0.5V, V_I = 0V, V_{CM} = -14.5V, R_S = 50KΩ		-150	0.1	nA	1, 2
				-200	0.1	nA	3
		+V_{CC} = 2V, -V_{CC} = -28V, V_I = 0V, V_{CM} = +13V, R_S = 50KΩ		-150	0.1	nA	1, 2
				-200	0.1	nA	3
V_OSt	Collector Output Voltage (Strobe)	+V_I = Gnd, -V_I = 15V, I_{St} = -3mA, R_S = 50Ω		(3)(4) 14		V	1, 2, 3
CMRR	Common Mode Rejection Ratio	-28V ≤ -V_{CC} ≤ -0.5V, R_S = 50Ω, 2V ≤ +V_{CC} ≤ 29.5V, R_S = 50Ω, -14.5V ≤ V_{CM} ≤ 13V, R_S = 50Ω		80		dB	1, 2, 3
V_{OL}	Low Level Output Voltage	+V_{CC} = 4.5V, -V_{CC} = Gnd, I_O = 8mA, ±V_I = 0.5V, V_{ID} = -6mV			0.4	V	1, 2, 3
		+V_{CC} = 4.5V, -V_{CC} = Gnd, I_O = 8mA, ±V_I = 3V, V_{ID} = -6mV			0.4	V	1, 2, 3
		I_O = 50mA, ±V_I = 13V, V_{ID} = -5mV			1.5	V	1, 2, 3
		I_O = 50mA, ±V_I = -14V, V_{ID} = -5mV			1.5	V	1, 2, 3
I_{CEX}	Output Leakage Current	+V_{CC} = 18V, -V_{CC} = -18V, V_O = 32V		-1.0	10	nA	1
				-1.0	500	nA	2
I_L	Input Leakage Current	+V_{CC} = 18V, -V_{CC} = -18V, +V_I = +12V, -V_I = -17V	(5)	-5.0	500	nA	1, 2, 3
		+V_{CC} = 18V, -V_{CC} = -18V, +V_I = -17V, -V_I = +12V	(5)	-5.0	500	nA	1, 2, 3
+I_{CC}	Power Supply Current				6.0	mA	1, 2
					7.0	mA	3
-I_{CC}	Power Supply Current			-5.0		mA	1, 2
				-6.0		mA	3

(3) I_{ST} = −2mA at −55°C
(4) Group A sample ONLY
(5) V_{ID} is voltage difference between inputs.

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LM111 RADIATION Electrical Characteristics SMD 5962R0052402 DC Parameters(1)(2) (continued)

The following conditions apply, unless otherwise specified. V_{CC} = ±15V, V_{CM} = 0

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
ΔV_{IO} / ΔT	Temperature Coefficient Input Offset Voltage	25°C ≤ T ≤ 125°C		-25	25	µV/°C	2
		-55°C ≤ T ≤ 25°C		-25	25	µV/°C	3
ΔI_{IO} / ΔT	Temperature Coefficient Input Offset Current	25°C ≤ T ≤ 125°C		-100	100	pA/°C	2
		-55°C ≤ T ≤ 25°C		-200	200	pA/°C	3
I_{OS}	Short Circuit Current	V_O = 5V, t ≤ 10mS, $-V_I$ = 0.1V, $+V_I$ = 0V	(6)		200	mA	1
			(5)		150	mA	2
			(5)		250	mA	3
$+V_{IO}$ adj.	Input Offset Voltage (Adjustment)	V_O = 0V, V_I = 0V, R_S = 50Ω		5.0		mV	1
$-V_{IO}$ adj.	Input Offset Voltage (Adjustment)	V_O = 0V, V_I = 0V, R_S = 50Ω			-5.0	mV	1
$\pm A_{VE}$	Voltage Gain (Emitter)	R_L = 600Ω	(7)	10		V/mV	4
			(7)	8.0		V/mV	5, 6

(6) Actual min. limit used is 5mA due to test setup.
(7) Pin names based on an 8 pin package configuration. When using higher pin count packages then: Pin 2 & 3 are Inputs, Pin 5 is Balance, Pin 6 is Balance /Strobe, Pin 7 is Output, and Pin 8 is V^+. For example: V_{56} is the Voltage between the Balance and Balance / Strobe pins.

LM111 RADIATION Electrical Characteristics SMD 5962R0052402 AC Parameters(1)(2)

The following conditions apply, unless otherwise specified. V_{CC} = ±15V, V_{CM} = 0

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
tR_{LHC}	Response Time (Collector Output)	V_{OD}(Overdrive) = -5mV, C_L = 50pF, V_I = -100mV	(3)		300	nS	7, 8B
					640	nS	8A
tR_{HLC}	Response Time (Collector Output)	V_{OD}(Overdrive) = 5mV, C_L = 50pF, V_I = 100mV	(3)		300	nS	7, 8B
					500	nS	8A

(1) Calculated parameter.
(2) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be sensitive in a high dose environment. Low dose rate testing has been performed on a wafer-by-wafer basis, per test method 1019 condition D of MIL-STD-883, with no enhanced low dose rate sensitivity (ELDRS) effect.
(3) Group A sample ONLY

LM111 RADIATION Electrical Characteristics SMD 5962R0052402 DC DELTA Parameters(1)(2)

The following conditions apply, unless otherwise specified. V_{CC} = ±15V, V_{CM} = 0
Delta calculations performed on QMLV devices at group B , subgroup 5.

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	V_I = 0V, R_S = 50Ω		-0.5	0.5	mV	1
		$+V_{CC}$ = 29.5V, $-V_{CC}$ = -0.5V, V_I = 0V, V_{CM} = -14.5V, R_S = 50Ω		-0.5	0.5	mV	1
		$+V_{CC}$ = 2V, $-V_{CC}$ = -28V, V_I = 0V, V_{CM} = +13V, R_S = 50Ω		-0.5	0.5	mV	1

(1) Calculated parameter.
(2) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be sensitive in a high dose environment. Low dose rate testing has been performed on a wafer-by-wafer basis, per test method 1019 condition D of MIL-STD-883, with no enhanced low dose rate sensitivity (ELDRS) effect.

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LM111 RADIATION Electrical Characteristics SMD 5962R0052402 DC DELTA Parameters(1)(2) (continued)

The following conditions apply, unless otherwise specified. V_{CC} = ±15V, V_{CM} = 0
Delta calculations performed on QMLV devices at group B , subgroup 5.

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
$\pm I_{IB}$	Input Bias Current	V_I = 0V, R_S = 50KΩ		-12.5	12.5	nA	1
		$+V_{CC}$ = 29.5V, $-V_{CC}$ = -0.5V, V_I = 0V, V_{CM} = -14.5V, R_S = 50KΩ		-12.5	12.5	nA	1
		$+V_{CC}$ = 2V, $-V_{CC}$ = -28V, V_I = 0V, V_{CM} = +13V, R_S = 50KΩ		-12.5	12.5	nA	1
I_{CEX}	Output Leakage Current	$+V_{CC}$ = 18V, $-V_{CC}$ = -18V, V_O = 32V		-5.0	5.0	nA	1

LM111 RADIATION Electrical Characteristics SMD 5962R0052402 Post Radiation Parameters(1)(2)

The following conditions apply, unless otherwise specified

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
$I_{IO}R$	Raised Input Offset Current	V_I = 0V, R_S = 50KΩ	(3)	−100	+100	nA	1
$\pm I_{IB}$	Input Bias Current	V_I = 0V, R_S = 50KΩ		−180	0.1	nA	1
		$+V_{CC}$ = 29.5V, $-V_{CC}$ = −0.5V, V_I = 0V, V_{CM} = −14.5V, R_S = 50KΩ		−225	0.1	nA	1
I_{CEX}	Output Leakage Current	$+V_{CC}$ = 18V, $-V_{CC}$ = −18V, V_O = 32V		−1.0	+25	nA	1

(1) Calculated parameter.
(2) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be sensitive in a high dose environment. Low dose rate testing has been performed on a wafer-by-wafer basis, per test method 1019 condition D of MIL-STD-883, with no enhanced low dose rate sensitivity (ELDRS) effect.
(3) Subscript (R) indicates tests which are performed with input stage current raised by connecting BAL and BAL/STB terminals to $+V_{CC}$.

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LM111 Typical Performance Characteristics

Input Bias Current

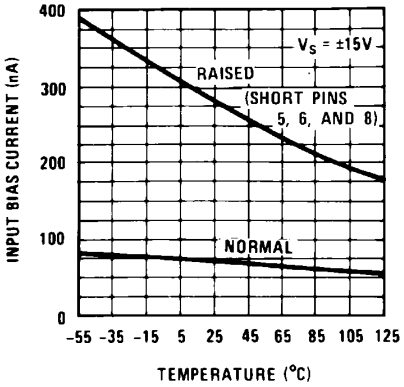


Figure 7.

Input Bias Current

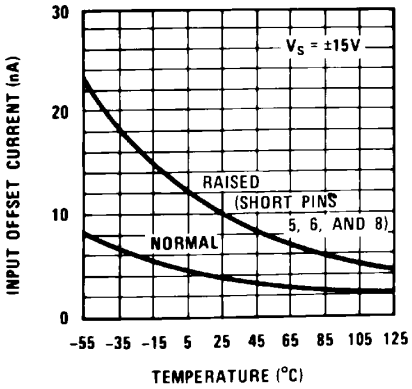


Figure 8.

Input Bias Current

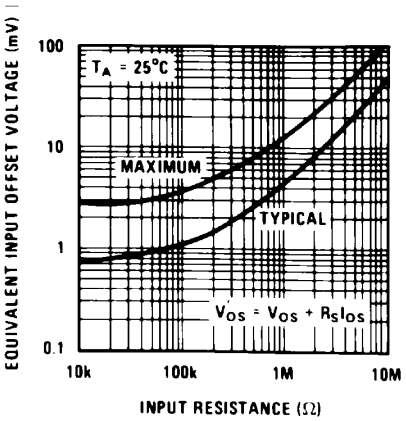


Figure 9.

Input Bias Current

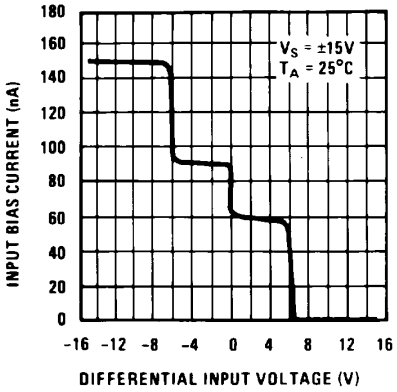


Figure 10.

Input Bias Current

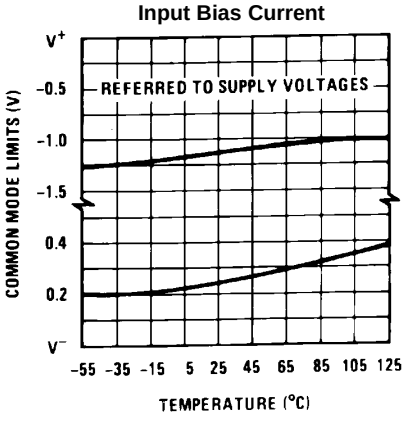


Figure 11.

Input Bias Current

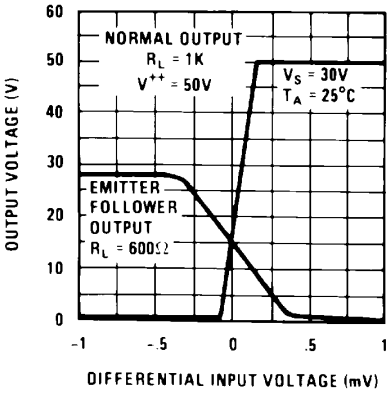


Figure 12.

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LM111 Typical Performance Characteristics (continued)

Input Bias Current
Input Overdrives

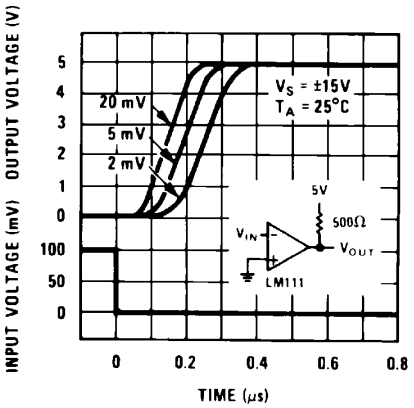


Figure 13.

Input Bias Current
Input Overdrives

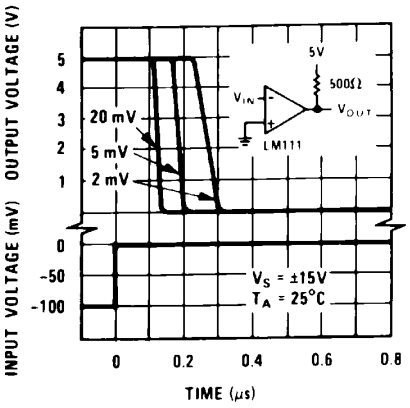


Figure 14.

Input Bias Current

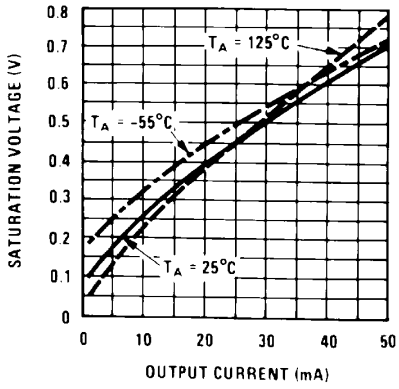


Figure 15.

Response Time for Various Input Overdrives

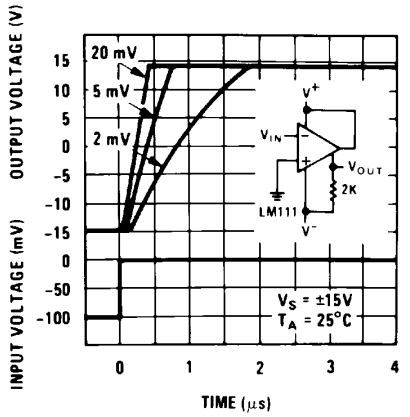


Figure 16.

Response Time for Various Input Overdrives

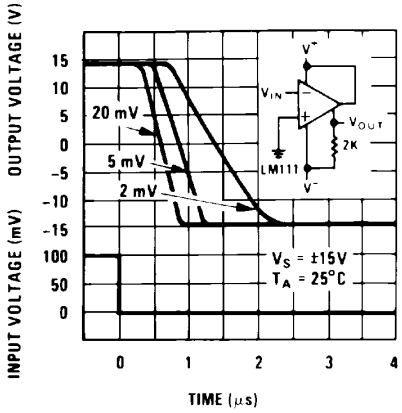


Figure 17.

Output Limiting Characteristics

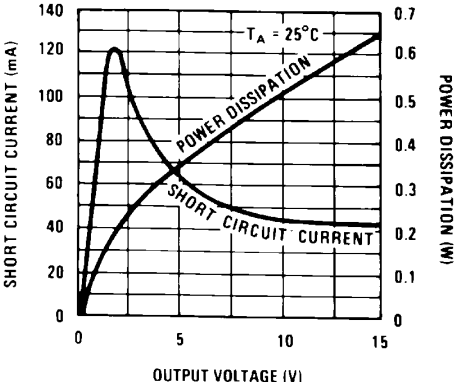


Figure 18.

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LM111 Typical Performance Characteristics (continued)

Supply Current

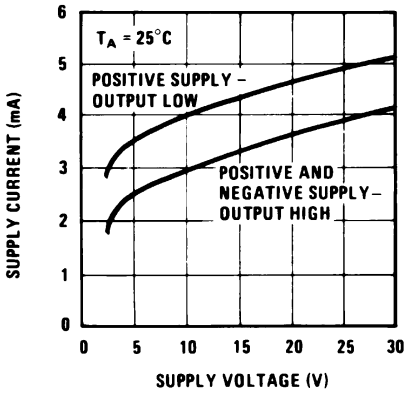


Figure 19.

Supply Current

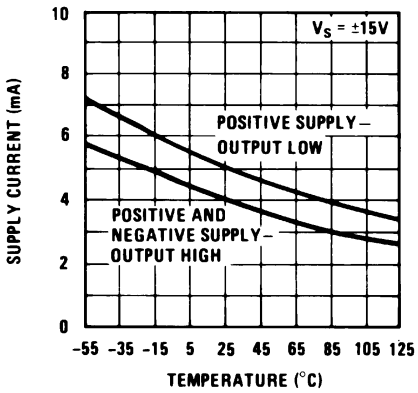


Figure 20.

Leakage Currents

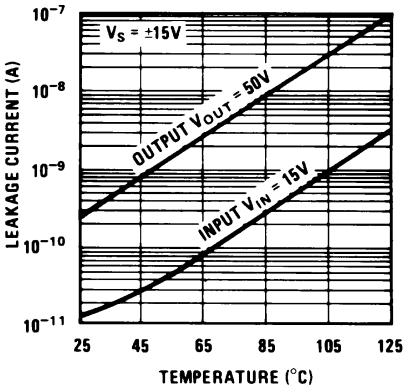


Figure 21.

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APPLICATION HINTS

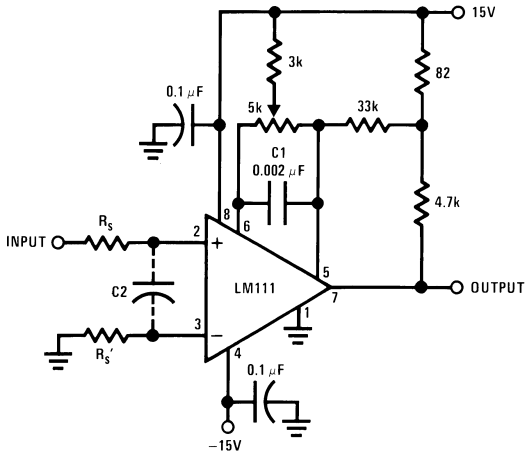
CIRCUIT TECHNIQUES FOR AVOIDING OSCILLATIONS IN COMPARATOR APPLICATIONS

When a high-speed comparator such as the LM111 is used with fast input signals and low source impedances, the output response will normally be fast and stable, assuming that the power supplies have been bypassed (with 0.1 µF disc capacitors), and that the output signal is routed well away from the inputs (pins 2 and 3) and also away from pins 5 and 6.

However, when the input signal is a voltage ramp or a slow sine wave, or if the signal source impedance is high (1 kΩ to 100 kΩ), the comparator may burst into oscillation near the crossing-point. This is due to the high gain and wide bandwidth of comparators like the LM111. To avoid oscillation or instability in such a usage, several precautions are recommended, as shown in Figure 22 below.

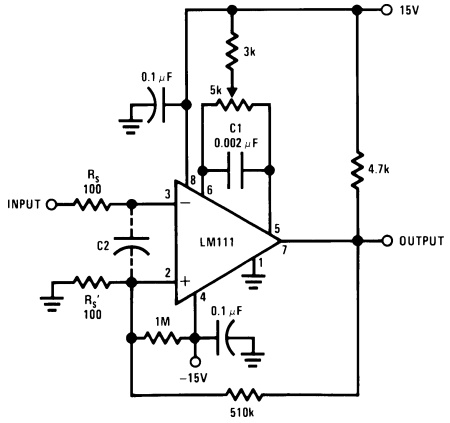
1. The trim pins (pins 5 and 6) act as unwanted auxiliary inputs. If these pins are not connected to a trim-pot, they should be shorted together. If they are connected to a trim-pot, a 0.01 µF capacitor C1 between pins 5 and 6 will minimize the susceptibility to AC coupling. A smaller capacitor is used if pin 5 is used for positive feedback as in Figure 22.
2. Certain sources will produce a cleaner comparator output waveform if a 100 pF to 1000 pF capacitor C2 is connected directly across the input pins.
3. When the signal source is applied through a resistive network, R_S, it is usually advantageous to choose an R_S' of substantially the same value, both for DC and for dynamic (AC) considerations. Carbon, tin-oxide, and metal-film resistors have all been used successfully in comparator input circuitry. Inductive wire wound resistors are not suitable.
4. When comparator circuits use input resistors (e.g. summing resistors), their value and placement are particularly important. In all cases the body of the resistor should be close to the device or socket. In other words there should be very little lead length or printed-circuit foil run between comparator and resistor to radiate or pick up signals. The same applies to capacitors, pots, etc. For example, if R_S=10 kΩ, as little as 5 inches of lead between the resistors and the input pins can result in oscillations that are very hard to damp. Twisting these input leads tightly is the only (second best) alternative to placing resistors close to the comparator.
5. Since feedback to almost any pin of a comparator can result in oscillation, the printed-circuit layout should be engineered thoughtfully. Preferably there should be a ground plane under the LM111 circuitry, for example, one side of a double-layer circuit card. Ground foil (or, positive supply or negative supply foil) should extend between the output and the inputs, to act as a guard. The foil connections for the inputs should be as small and compact as possible, and should be essentially surrounded by ground foil on all sides, to guard against capacitive coupling from any high-level signals (such as the output). If pins 5 and 6 are not used, they should be shorted together. If they are connected to a trim-pot, the trim-pot should be located, at most, a few inches away from the LM111, and the 0.01 µF capacitor should be installed. If this capacitor cannot be used, a shielding printed-circuit foil may be advisable between pins 6 and 7. The power supply bypass capacitors should be located within a couple inches of the LM111. (Some other comparators require the power-supply bypass to be located immediately adjacent to the comparator.)
6. It is a standard procedure to use hysteresis (positive feedback) around a comparator, to prevent oscillation, and to avoid excessive noise on the output because the comparator is a good amplifier for its own noise. In the circuit of Figure 23, the feedback from the output to the positive input will cause about 3 mV of hysteresis. However, if R_S is larger than 100Ω, such as 50 kΩ, it would not be reasonable to simply increase the value of the positive feedback resistor above 510 kΩ. The circuit of Figure 24 could be used, but it is rather awkward. See the notes in paragraph 7 below.
7. When both inputs of the LM111 are connected to active signals, or if a high-impedance signal is driving the positive input of the LM111 so that positive feedback would be disruptive, the circuit of Figure 22 is ideal. The positive feedback is to pin 5 (one of the offset adjustment pins). It is sufficient to cause 1 to 2 mV hysteresis and sharp transitions with input triangle waves from a few Hz to hundreds of kHz. The positive-feedback signal across the 82Ω resistor swings 240 mV below the positive supply. This signal is centered around the nominal voltage at pin 5, so this feedback does not add to the V_{OS} of the comparator. As much as 8 mV of V_{OS} can be trimmed out, using the 5 kΩ pot and 3 kΩ resistor as shown.
8. These application notes apply specifically to the LM111 and are applicable to all high-speed comparators in general, (with the exception that not all comparators have trim pins).

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Pin connections shown are for LM111H in the LMC0008C package

Figure 22. Improved Positive Feedback



Pin connections shown are for LM111H in the LMC0008C package

Figure 23. Conventional Positive Feedback

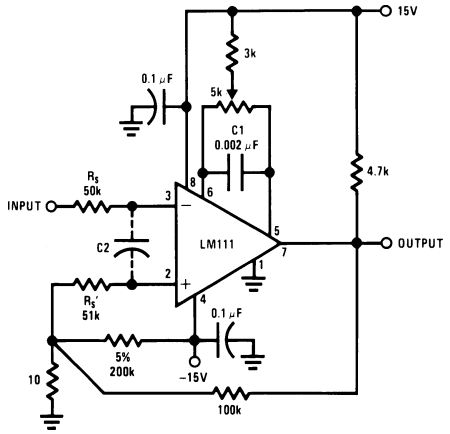


Figure 24. Positive Feedback with High Source Resistance

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TYPICAL APPLICATIONS

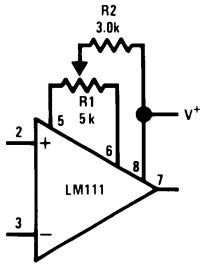
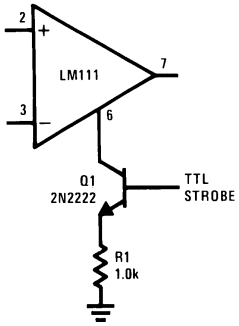
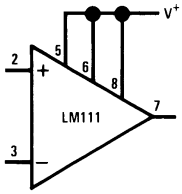


Figure 25. Offset Balancing



Note: Do Not Ground Strobe Pin. Output is turned off when current is pulled from Strobe Pin.

Figure 26. Strobing



Increases typical common mode slew from 7.0V/μs to 18V/μs.

Figure 27. Increasing Input Stage Current

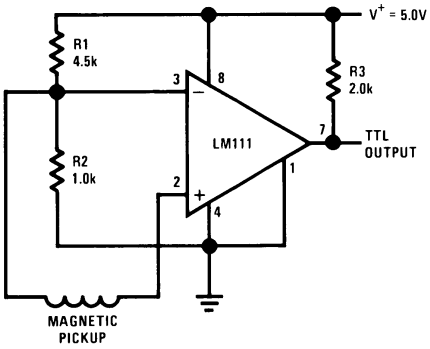


Figure 28. Detector for Magnetic Transducer

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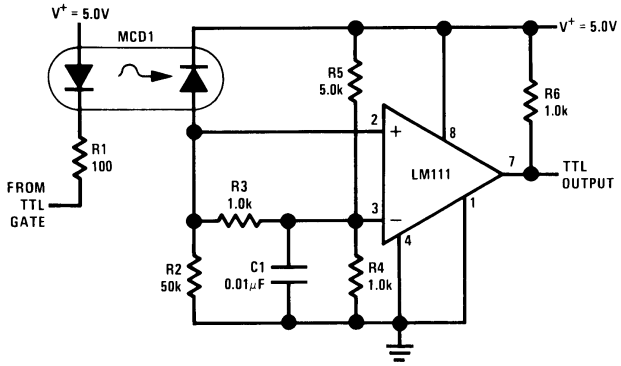
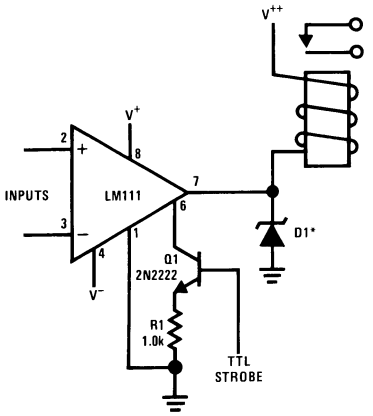
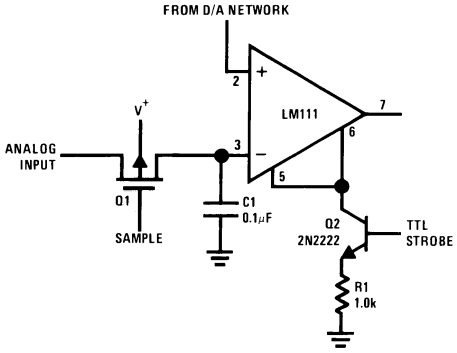


Figure 29. Digital Transmission Isolator



*Absorbs inductive kickback of relay and protects IC from severe voltage transients on V^{++} line.
Note: Do Not Ground Strobe Pin.

Figure 30. Relay Driver with Strobe



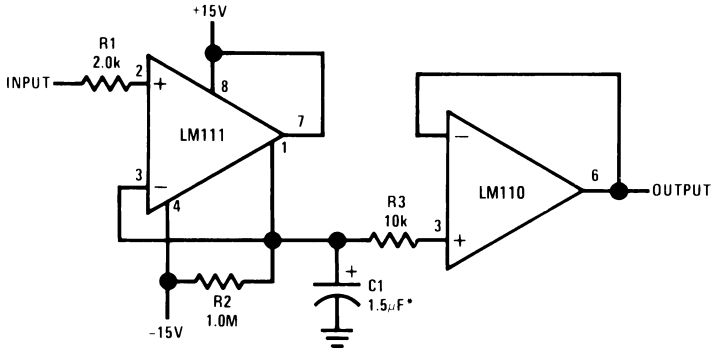
Note: Do Not Ground Strobe Pin.

(1) Typical input current is 50 pA with inputs strobed off.

(2) Pin connections shown on schematic diagram and typical applications are for LMC0008C package.

Figure 31. Strobing off Both Input and Output Stages

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*Solid tantalum

Figure 32. Positive Peak Detector

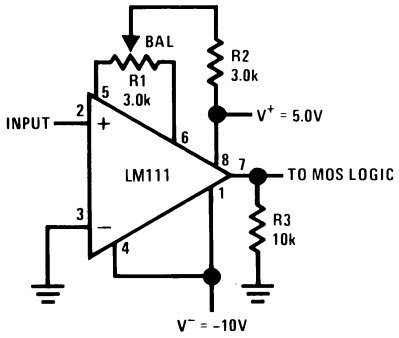


Figure 33. Zero Crossing Detector Driving MOS Logic

TYPICAL APPLICATIONS FOR METAL CYLINDER PACKAGE

(Pin numbers refer to LMC0008C package)

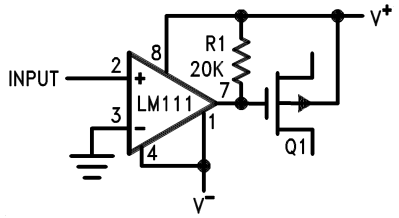
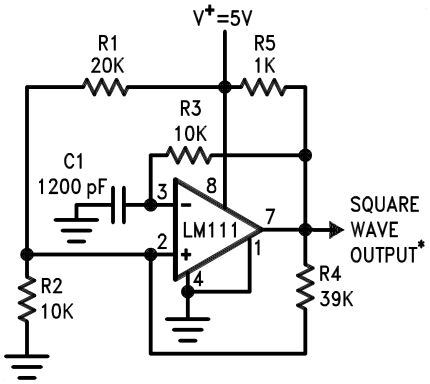


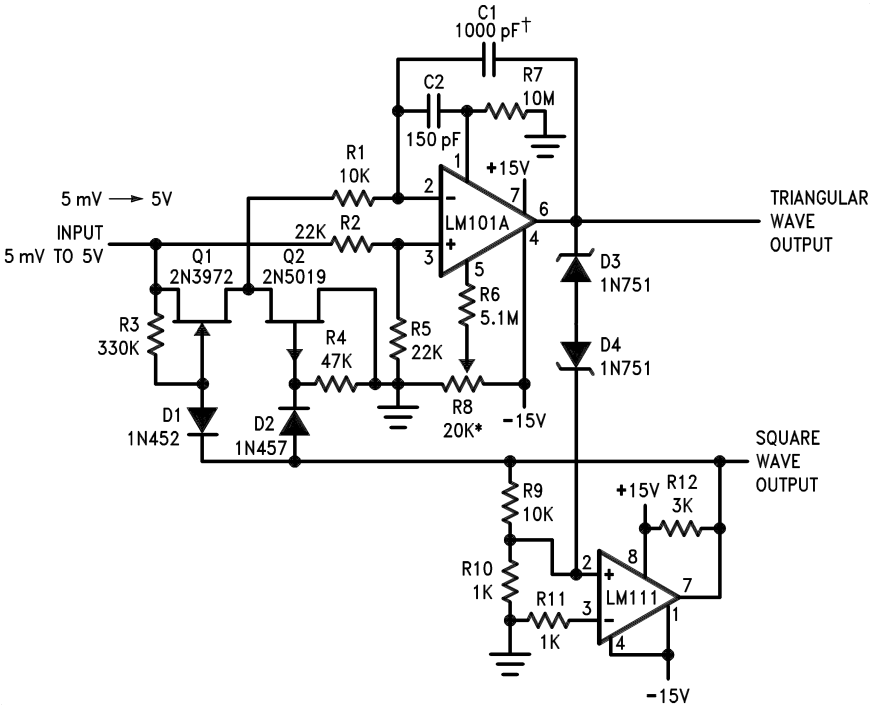
Figure 34. Zero Crossing Detector Driving MOS Switch



*TTL or DTL fanout of two

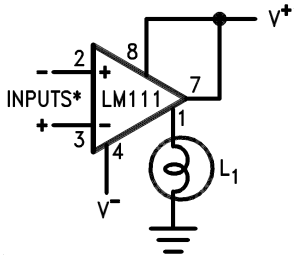
Figure 35. 100 kHz Free Running Multivibrator

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*Adjust for symmetrical square wave time when V_{IN} = 5 mV
†Minimum capacitance 20 pF Maximum frequency 50 kH

Figure 36. 10 Hz to 10 kHz Voltage Controlled Oscillator



*Input polarity is reversed when using pin 1 as output.

Figure 37. Driving Ground-Referred Load

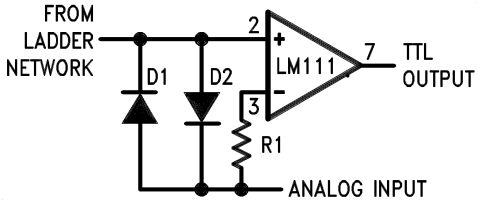
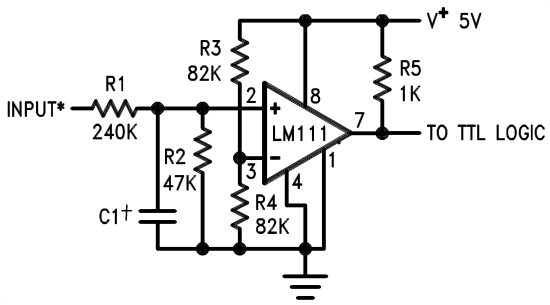


Figure 38. Using Clamp Diodes to Improve Response



*Values shown are for a 0 to 30V logic swing and a 15V threshold.
†May be added to control speed and reduce susceptibility to noise spikes.

Figure 39. TTL Interface with High Level Logic

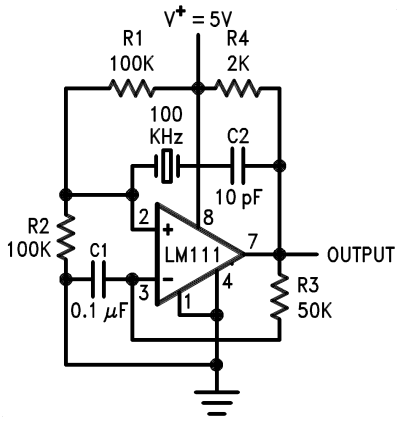


Figure 40. Crystal Oscillator

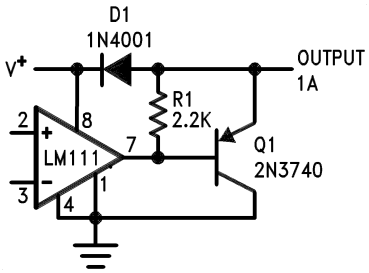
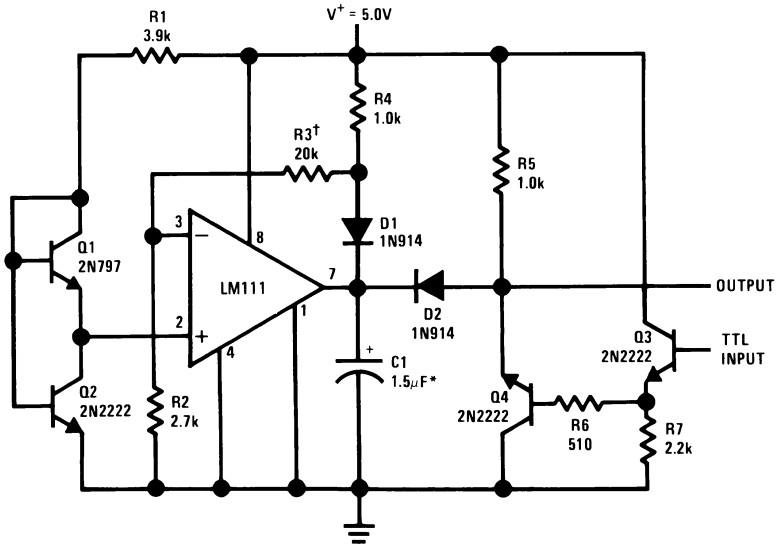


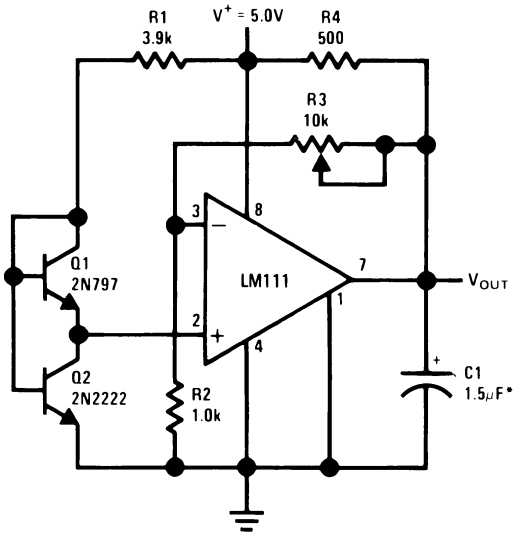
Figure 41. Comparator and Solenoid Driver

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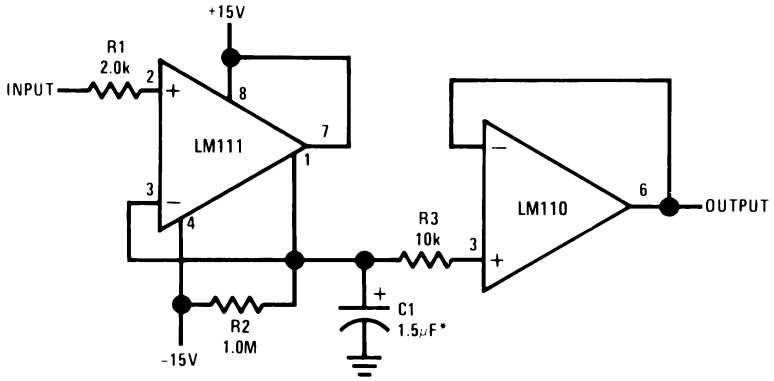
*Solid tantalum
†Adjust to set clamp level

Figure 42. Precision Squarer



*Solid tantalum

Figure 43. Low Voltage Adjustable Reference Supply



*Solid tantalum

Figure 44. Positive Peak Detector

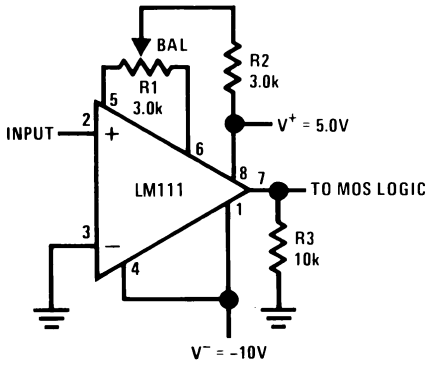
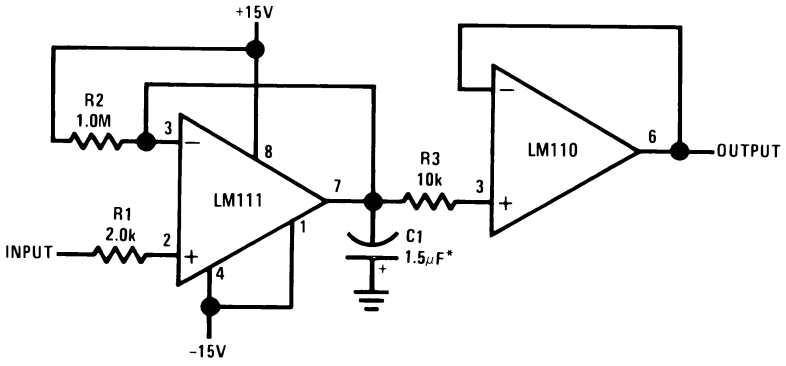


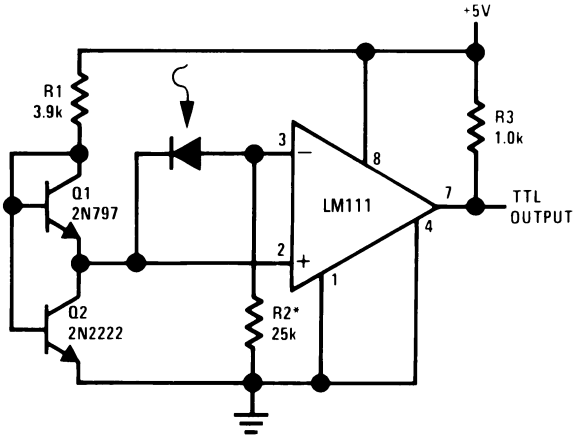
Figure 45. Zero Crossing Detector Driving MOS Logic



*Solid tantalum

Figure 46. Negative Peak Detector

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*R2 sets the comparison level. At comparison, the photodiode has less than 5 mV across it, decreasing leakages by an order of magnitude.

Figure 47. Precision Photodiode Comparator

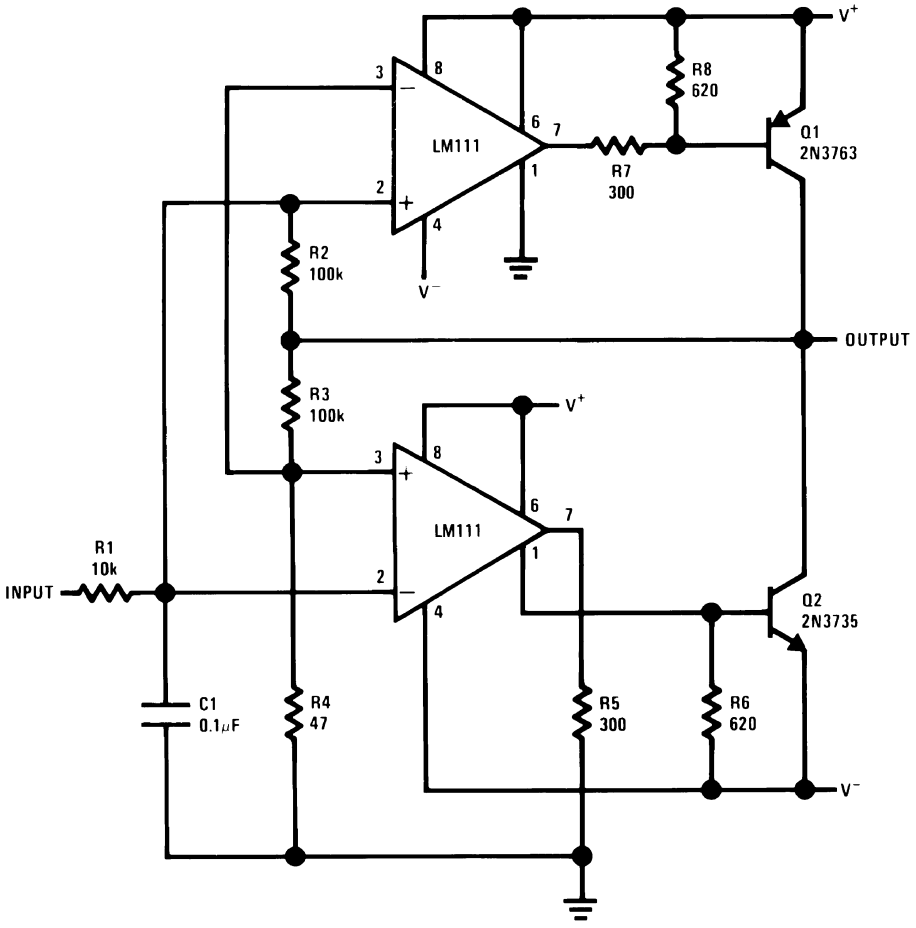


Figure 48. Switching Power Amplifier

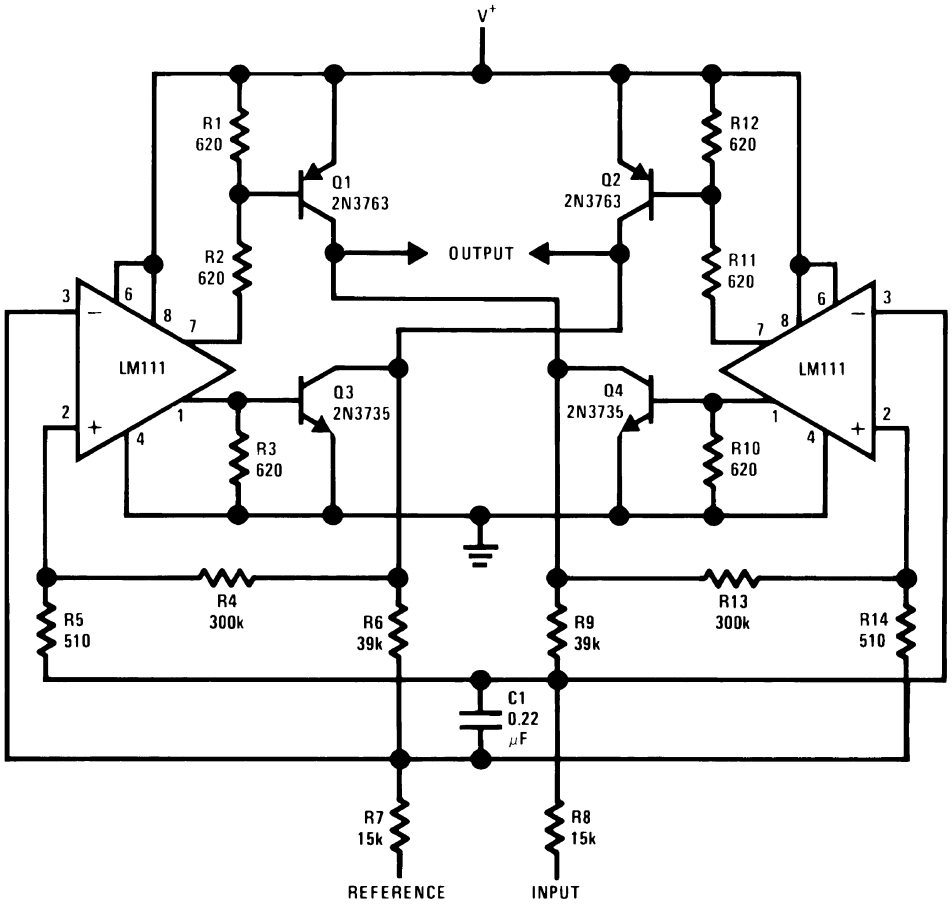


Figure 49. Switching Power Amplifier

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Table 2. Revision History

Released	Revision	Section	Originator	Changes
10/11/05	A	New Release, Corporate format	L. Lytle	3 MDS data sheets converted into one Corp. data sheet format. MNLM111-X Rev 0A0, MDLM111-X Rev. 0B0, and MRLM111-X-RH Rev 0E1. The drift table was eliminated from the 883 section since it did not apply; Note #3 was removed from RH & QML datasheets with SG verification that it no longer applied. Added NSID's for 50k Rad and Post Radiation Table. MDS data sheets will be archived.
12/14/05	B	Ordering Information Table	R. Malone	Removed NSID reference LM111J-8PQMLV, 5962P0052401VPA 30k rd(Si). Reason: NSID on LTB, Inventory exhausted. Added following NSID's: LM111HPQMLV, LM111WPQMLV and LM111WGPQMLV. Reason: Still have Inventory. LM111QML, Revision A will be archived.
06/26/08	C	Features, Ordering Information Table, Electrical section Notes.	Larry McGee	Added Radiation reference, ELDRS NSID's and Note 14 and 15, Low Dose Electrical Table. Deleted 30k rd(Si) NSID's: LM111HPQMLV, LM111WPQMLV and LM111WGPQMLV. Reason: EOL 9/06/05. Revision B will be archived.
03/26/2013	C	All Sections		Changed layout of National Data Sheet to TI format

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962L0052401VGA	Active	Production	TO-99 (LMC) | 8	20 | JEDEC TRAY (5+1)	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	LM111HLQMLV 5962L0052401VGA Q ACO 5962L0052401VGA Q >T
5962L0052401VHA	Active	Production	CFP (NAD) | 10	19 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM111W LQMLV Q 5962L00524 01VHA ACO 01VHA >T
5962L0052401VPA	Active	Production	CDIP (NAB) | 8	40 | TUBE	No	Call TI	Call TI	-55 to 125	LM111J-8LQV 5962L00524 01VPA Q ACO 01VPA Q >T
5962L0052401VZA	Active	Production	CFP (NAC) | 10	54 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM111W GLQMLV Q 5962L00524 01VZA ACO 01VZA >T
5962R0052402VGA	Active	Production	TO-99 (LMC) | 8	20 | JEDEC TRAY (5+1)	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	LM111HRLQV 5962R0052402VGA Q ACO 5962R0052402VGA Q >T
5962R0052402VHA	Active	Production	CFP (NAD) | 10	19 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM111W RLQMLV Q 5962R00524 02VHA ACO 02VHA >T
5962R0052402VPA	Active	Production	CDIP (NAB) | 8	40 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM111J-8RLQV 5962R00524 02VPA Q ACO 02VPA Q >T

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962R0052402VZA	Active	Production	CFP (NAC) | 10	124 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM111W GRLQMLV Q 5962R00524 02VZA ACO 02VZA >T
LM111 MD8	Active	Production	DIESALE (Y) | 0	300 | JEDEC TRAY (5+1)	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	
LM111-MDE	Active	Production	DIESALE (Y) | 0	40 | NOT REQUIRED	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	
LM111H/883	Active	Production	TO-99 (LMC) | 8	20 | JEDEC TRAY (5+1)	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	LM111H/883 Q ACO LM111H/883 Q >T
LM111HLQMLV	Active	Production	TO-99 (LMC) | 8	20 | JEDEC TRAY (5+1)	No	Call TI	Level-1-NA-UNLIM	-55 to 125	LM111HLQMLV 5962L0052401VGA Q ACO 5962L0052401VGA Q >T
LM111HRLQMLV	Active	Production	TO-99 (LMC) | 8	20 | JEDEC TRAY (5+1)	No	Call TI	Level-1-NA-UNLIM	-55 to 125	LM111HRLQV 5962R0052402VGA Q ACO 5962R0052402VGA Q >T
LM111J-8/883	Active	Production	CDIP (NAB) | 8	40 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM111J-8 /883 Q ACO /883 Q >T
LM111J-8LQMLV	Active	Production	CDIP (NAB) | 8	40 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM111J-8LQV 5962L00524 01VPA Q ACO 01VPA Q >T
LM111J-8RLQMLV	Active	Production	CDIP (NAB) | 8	40 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM111J-8RLQV 5962R00524 02VPA Q ACO 02VPA Q >T
LM111J/883	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM111J/883 Q
LM111WG/883	Active	Production	CFP (NAC) | 10	54 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM111WG /883 Q ACO /883 Q >T

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM111WGLQMLV	Active	Production	CFP (NAC) | 10	54 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM111W GLQMLV Q 5962L00524 01VZA ACO 01VZA >T
LM111WGRLQMLV	Active	Production	CFP (NAC) | 10	124 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM111W GRLQMLV Q 5962R00524 02VZA ACO 02VZA >T
LM111WLQMLV	Active	Production	CFP (NAD) | 10	19 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM111W LQMLV Q 5962L00524 01VHA ACO 01VHA >T
LM111WRLQMLV	Active	Production	CFP (NAD) | 10	19 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM111W RLQMLV Q 5962R00524 02VHA ACO 02VHA >T

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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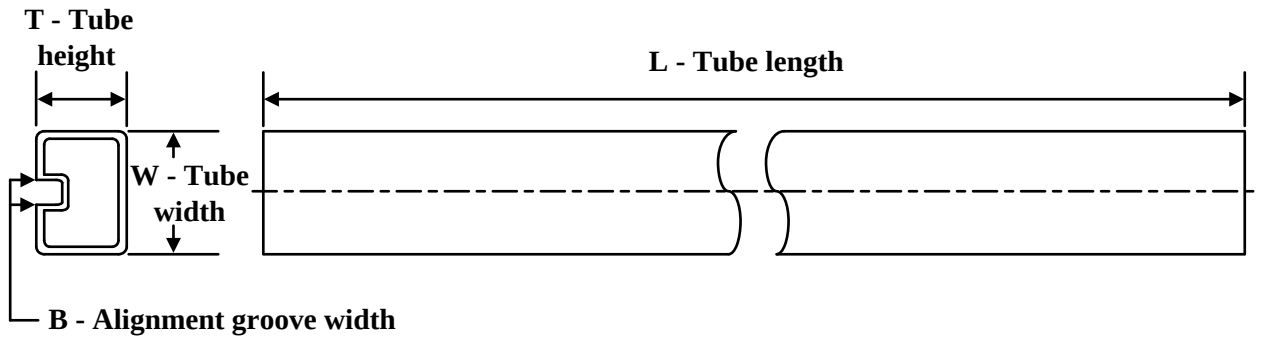
OTHER QUALIFIED VERSIONS OF LM111QML, LM111QML-SP :

- Military : LM111QML
- Space : LM111QML-SP

NOTE: Qualified Version Definitions:

- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

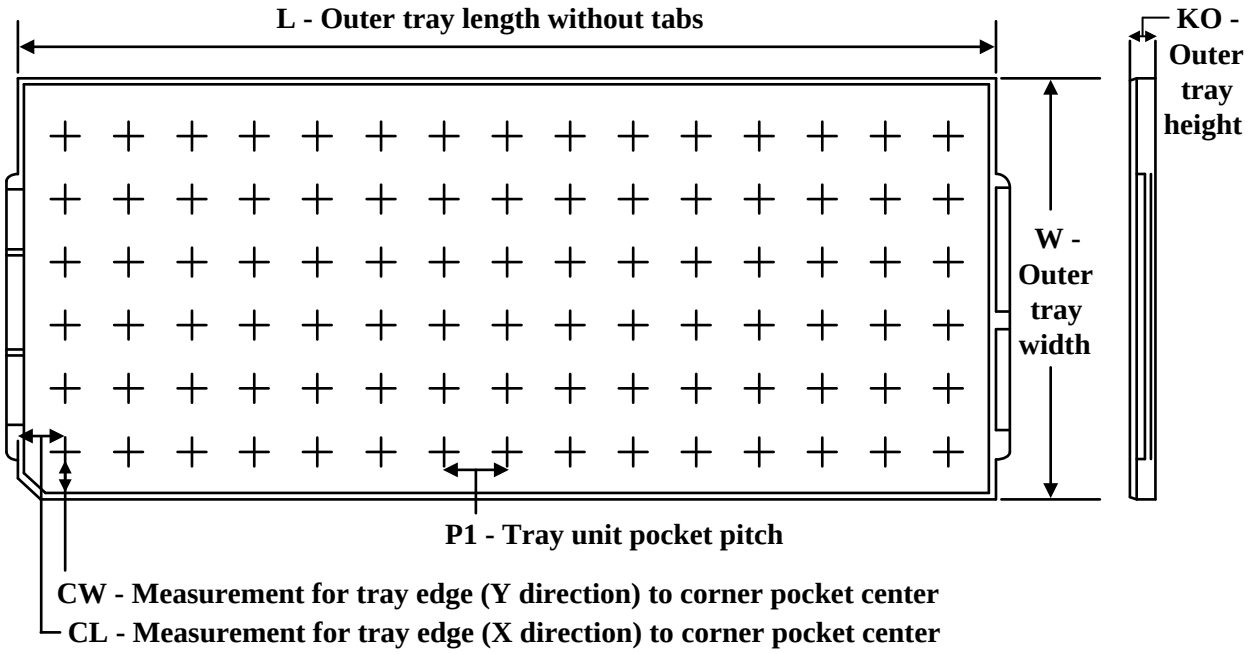
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962L0052401VHA	NAD	CFP	10	19	502	23	9398	9.78
5962L0052401VPA	NAB	CDIP	8	40	506.98	15.24	13440	NA
5962R0052402VHA	NAD	CFP	10	19	502	23	9398	9.78
5962R0052402VPA	NAB	CDIP	8	40	506.98	15.24	13440	NA
LM111J-8/883	NAB	CDIP	8	40	506.98	15.24	13440	NA
LM111J-8LQMLV	NAB	CDIP	8	40	506.98	15.24	13440	NA
LM111J-8RLQMLV	NAB	CDIP	8	40	506.98	15.24	13440	NA
LM111J/883	J	CDIP	14	25	506.98	15.24	13440	NA
LM111WLQMLV	NAD	CFP	10	19	502	23	9398	9.78
LM111WRLQMLV	NAD	CFP	10	19	502	23	9398	9.78

TRAY

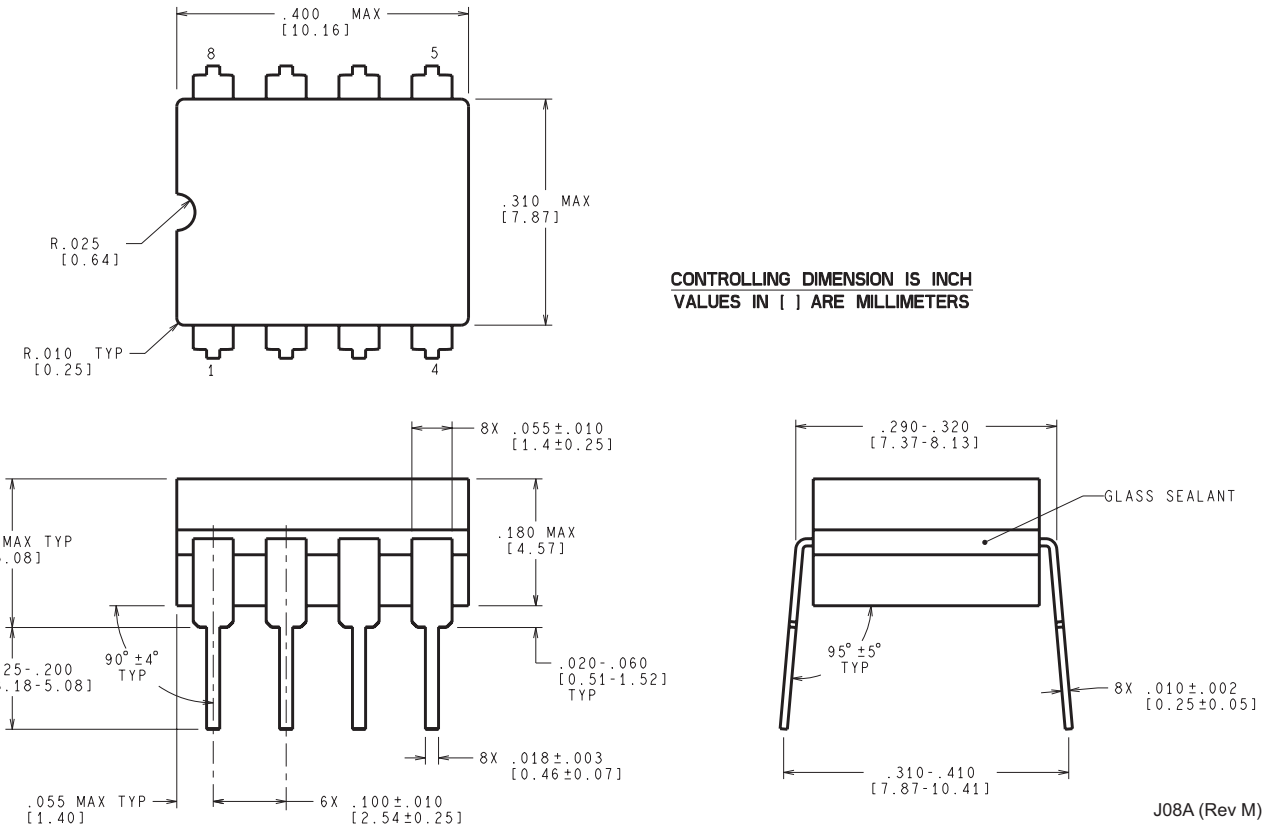


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
5962L0052401VGA	LMC	TO-CAN	8	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54
5962R0052402VGA	LMC	TO-CAN	8	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54
LM111H/883	LMC	TO-CAN	8	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54
LM111HLQMLV	LMC	TO-CAN	8	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54
LM111HRLQMLV	LMC	TO-CAN	8	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54

NAB0008A

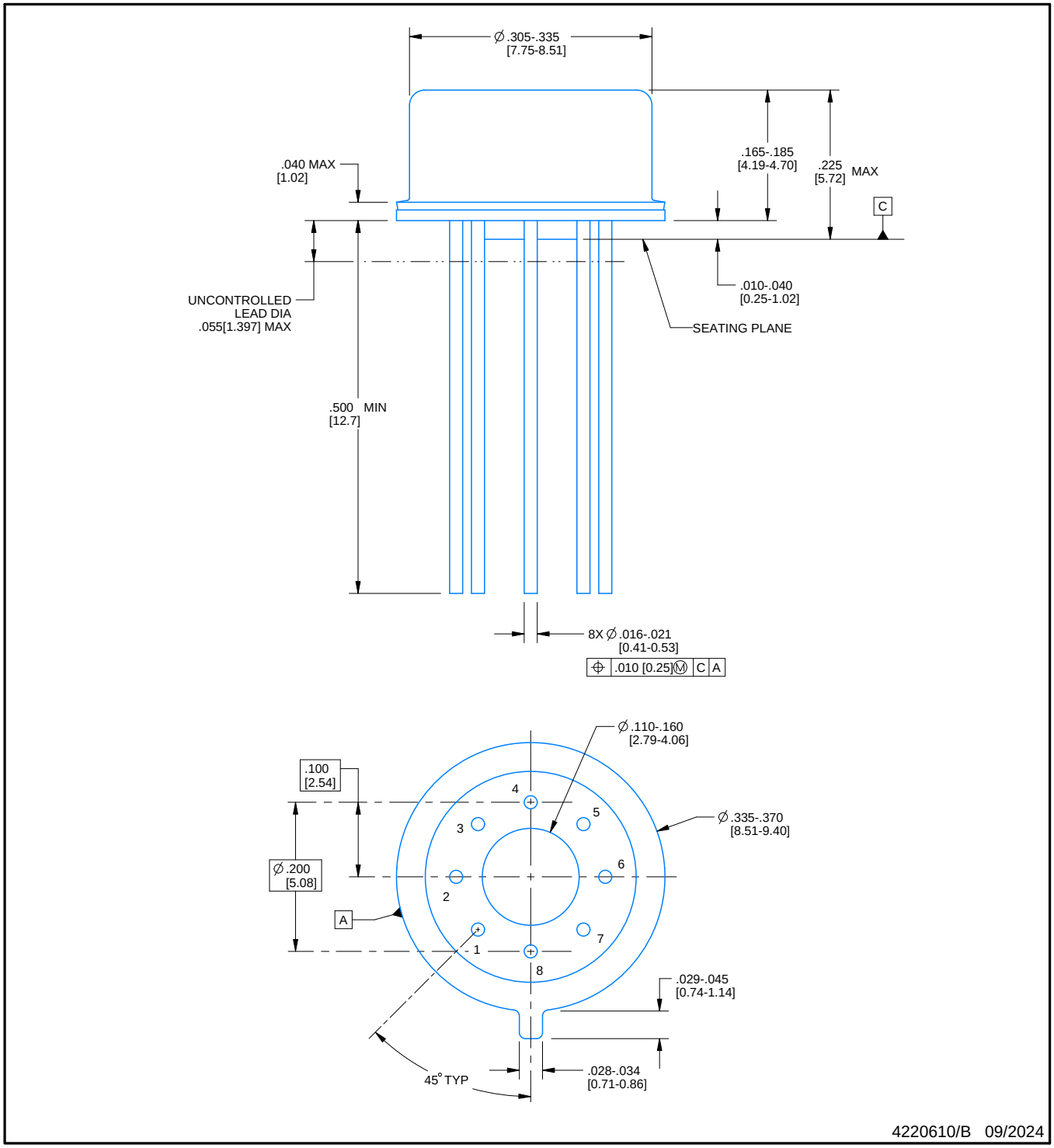

.400 MAX
[10.16]
8
5
.310 MAX
[7.87]
R.025
[0.64]
R.010 TYP
[0.25]
1
4
CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
8X .055±.010
[1.4±0.25]
.200 MAX TYP
[5.08]
.180 MAX
[4.57]
8X .125-.200
[3.18-5.08]
90° ±4°
TYP
.020-.060
[0.51-1.52]
TYP
8X .018±.003
[0.46±0.07]
.055 MAX TYP
[1.40]
6X .100±.010
[2.54±0.25]
.290-.320
[7.37-8.13]
GLASS SEALANT
95° ±5°
TYP
8X .010±.002
[0.25±0.05]
.310-.410
[7.87-10.41]
J08A (Rev M)

PACKAGE OUTLINE

LMC0008A

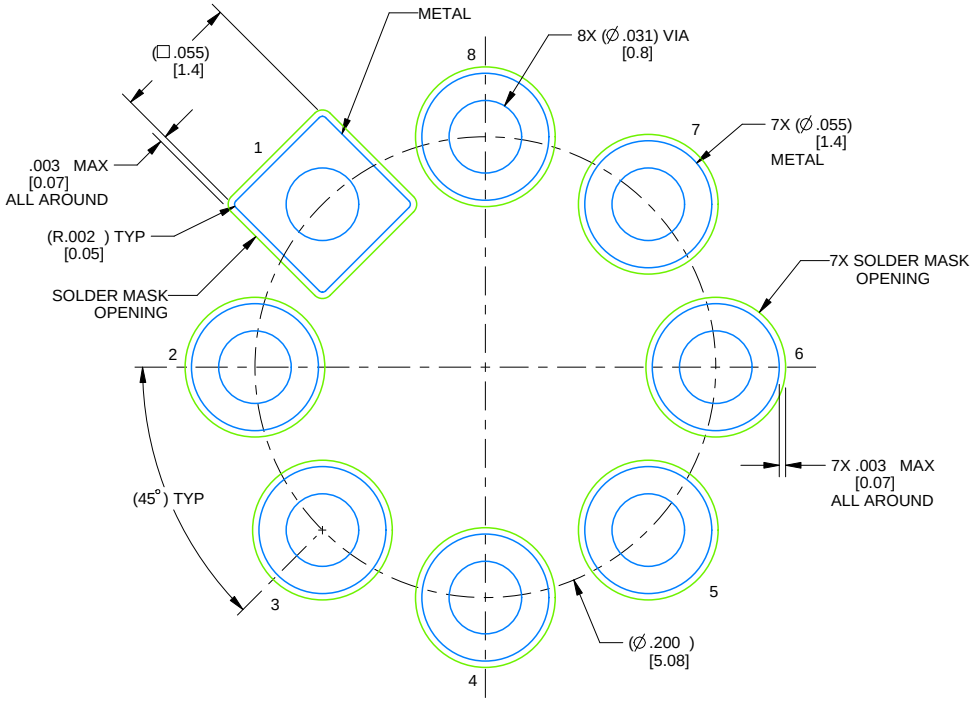
TO-CAN - 5.72 mm max height

TRANSISTOR OUTLINE



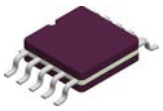
NOTES:

1. All linear dimensions are in inches [millimeters]. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pin numbers shown for reference only. Numbers may not be marked on package.
4. Reference JEDEC registration MO-002/TO-99.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 12X

4220610/B 09/2024

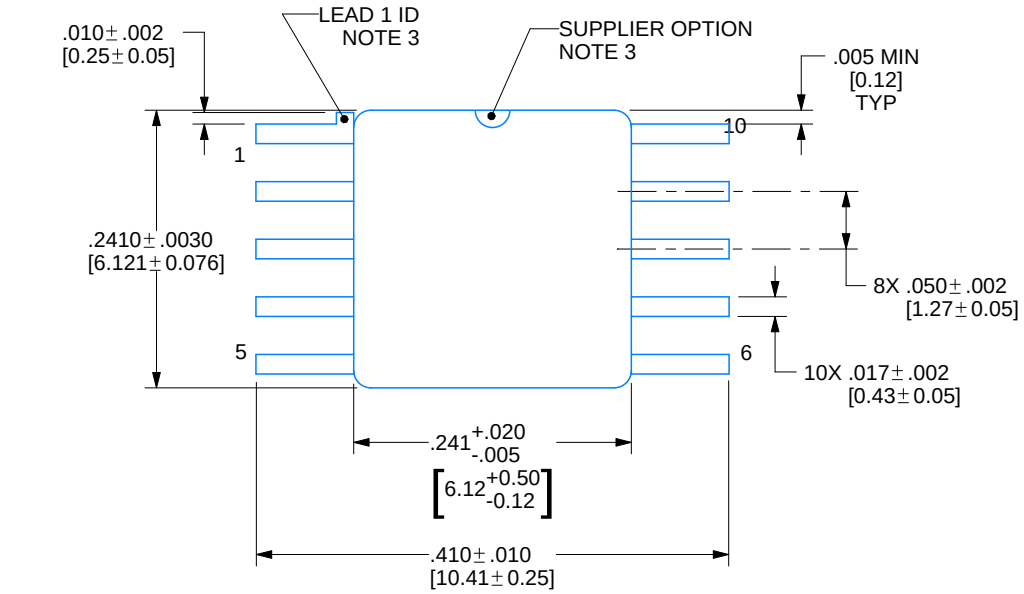


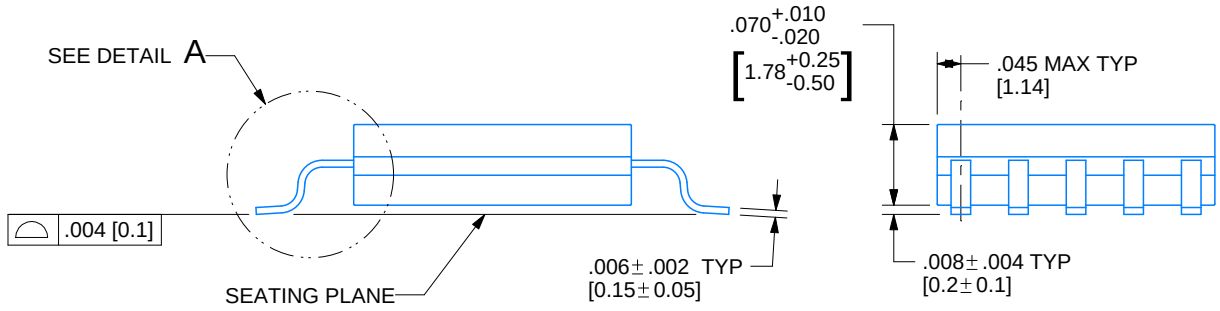
PACKAGE OUTLINE

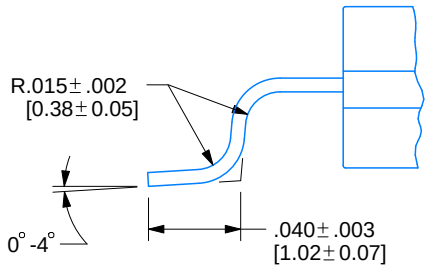
NAC0010A

CFP - 2.33mm max height

CERAMIC FLATPACK







DETAIL A
TYPICAL

4215196/D 08/2022

NOTES:

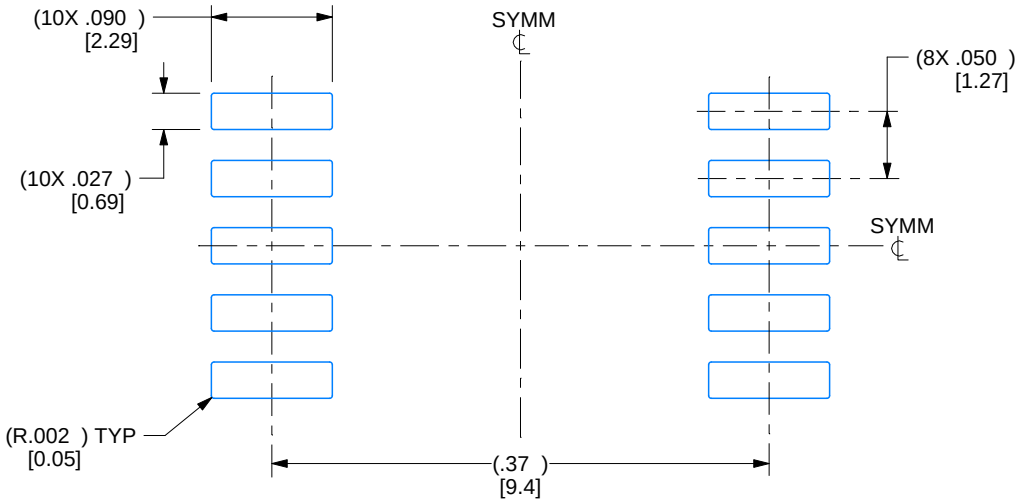
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. For solder thickness and composition, see the "Lead Finish Composition/Thickness" link in the packaging section of the Texas Instruments website
3. Lead 1 identification shall be:
   a) A notch or other mark within this area
   b) A tab on lead 1, either side
4. No JEDEC registration as of December 2021

EXAMPLE BOARD LAYOUT

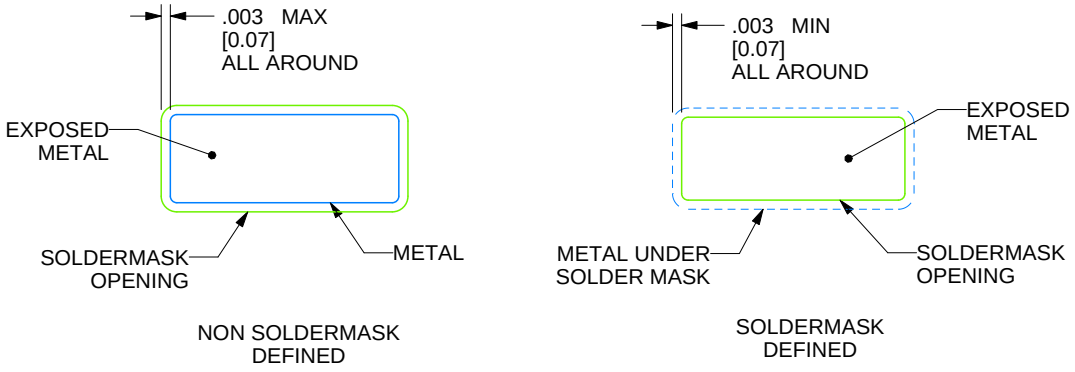
NAC0010A

CFP - 2.33mm max height

CERAMIC FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 7X



4215196/D 08/2022

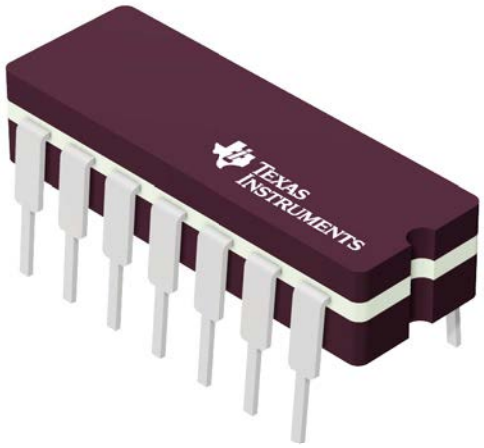
REVISIONS

REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	2197877	12/30/2021	DAVID CHIN / ANIS FAUZI
B	NO CHANGE TO DRAWING; REVISION FOR YODA RELEASE;	2198820	02/14/2022	K. SINCERBOX
C	CHANGE PIN 1 ID LOCATION ON PIN	2198845	02/18/2022	D. CHIN / K. SINCERBOX
D	.2410± .0030 WAS .2700 +.0012/-.0002;	2200915	08/08/2022	D. CHIN / K. SINCERBOX

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

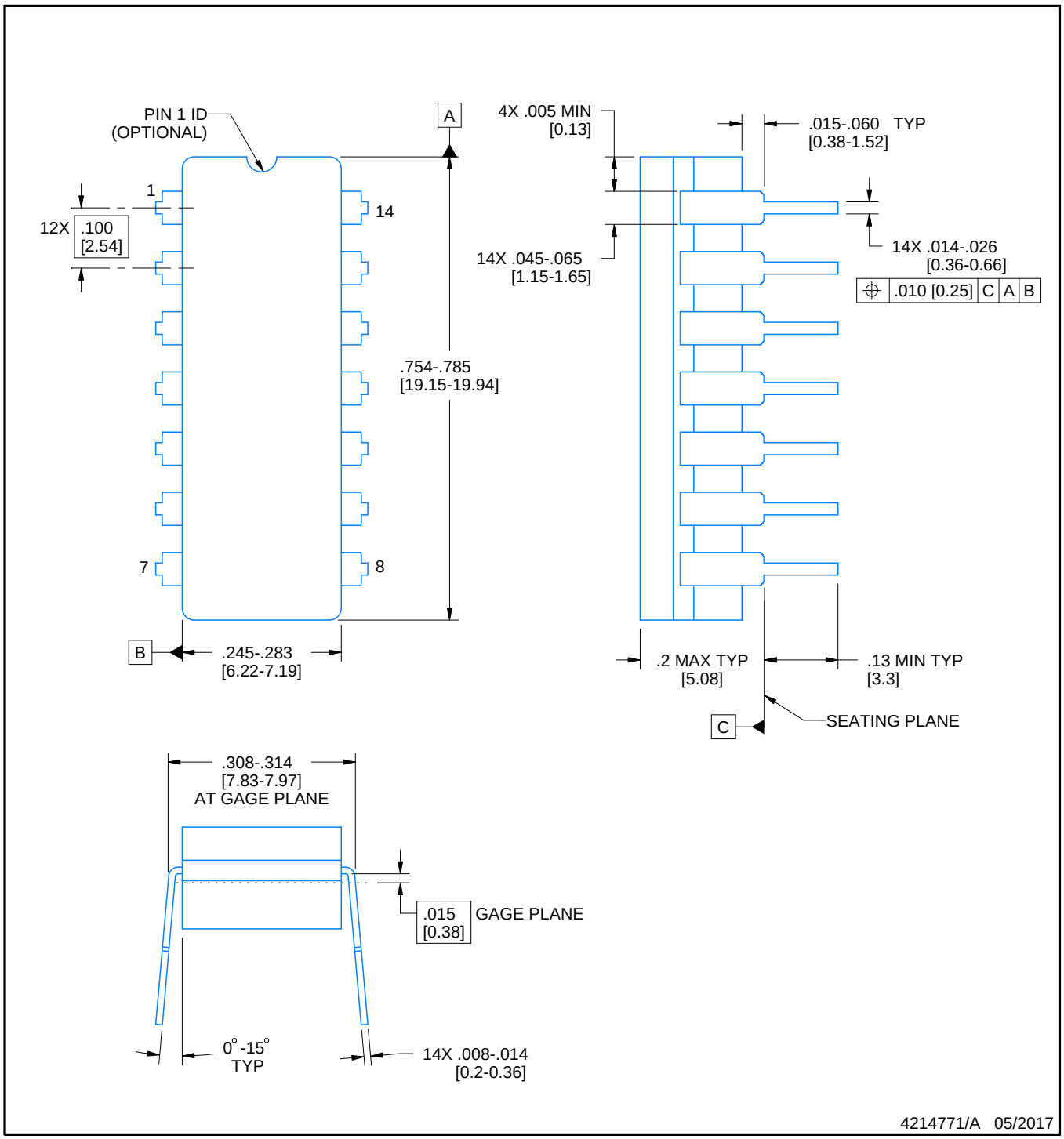


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

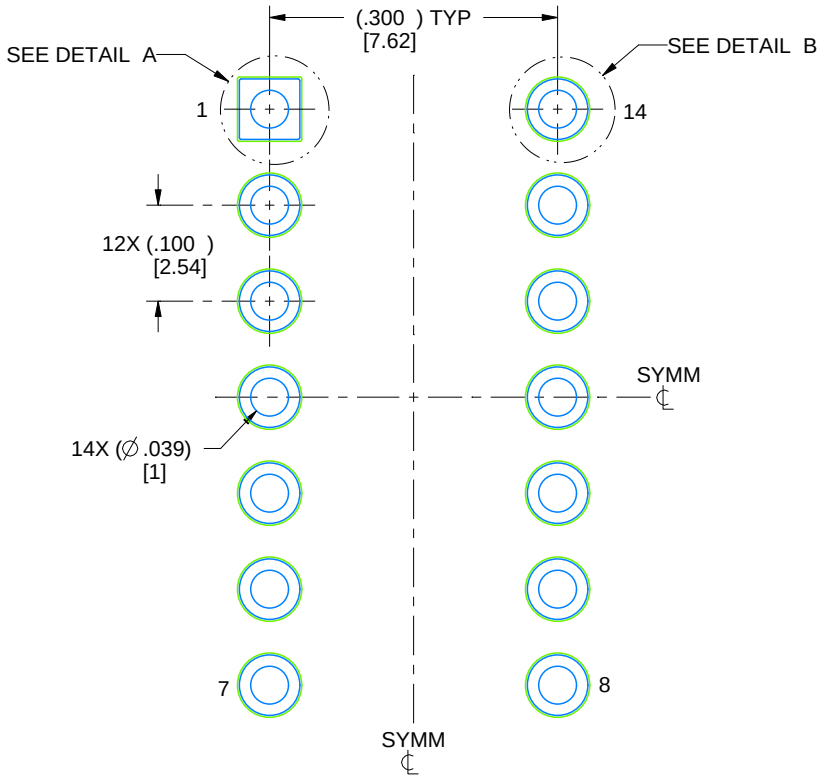
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

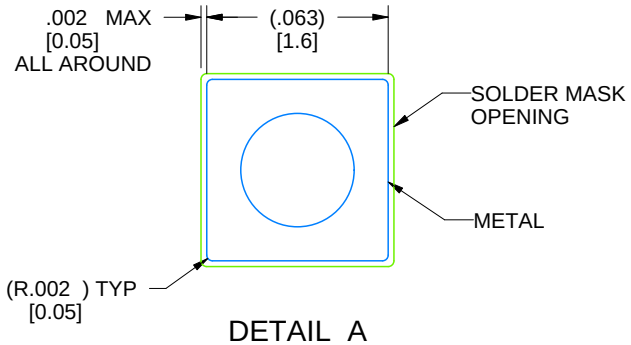
J0014A

CDIP - 5.08 mm max height

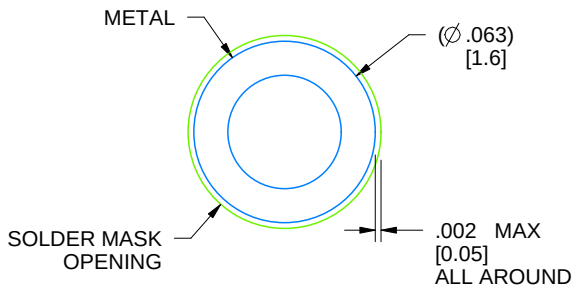
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

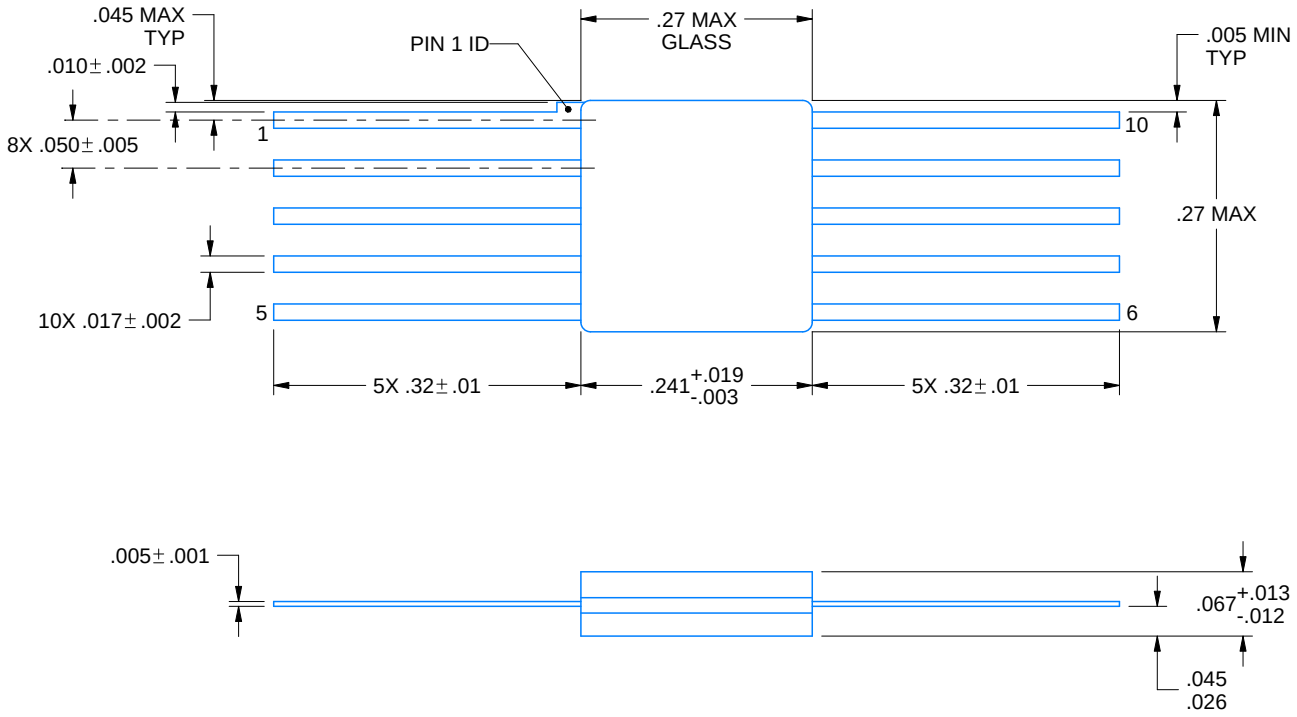
NAD0010A



PACKAGE OUTLINE

CFP - 2.03 mm max height

CERAMIC FLATPACK



4215191/A 06/2021

NOTES:

1. All linear dimensions are in inches. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

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