LM25037/-Q1 Dual-Mode PWM Controller With Alternating Outputs

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Operating Junction Temperature
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- Alternating Outputs for Double-Ended Topologies
- Ultra Wide Input Operating Range from 5.5 V to 75 V
- Current-Mode or Feed-Forward Voltage-Mode Control
- Programmable Maximum Duty Cycle Limit
- 2% Feedback Reference Accuracy
- High Gain-Bandwidth Error Amplifier
- Programmable Line Undervoltage Lockout (UVLO) With Adjustable Hysteresis
- Versatile Dual Mode Overcurrent Protection With Hiccup Delay Timer
- Programmable Soft-Start
- Precision 5-V Reference Output
- Current Sense Leading Edge Blanking
- Resistor Programmed 2-MHz Capable Oscillator
- Oscillator Synchronization Capability With Low-Frequency Lockout Protection
- 16-Pin TSSOP

2 Applications

- Telecom Power Converters
- Industrial Power Converters
- Automotive Power Converters (Q1 Version)

3 Description

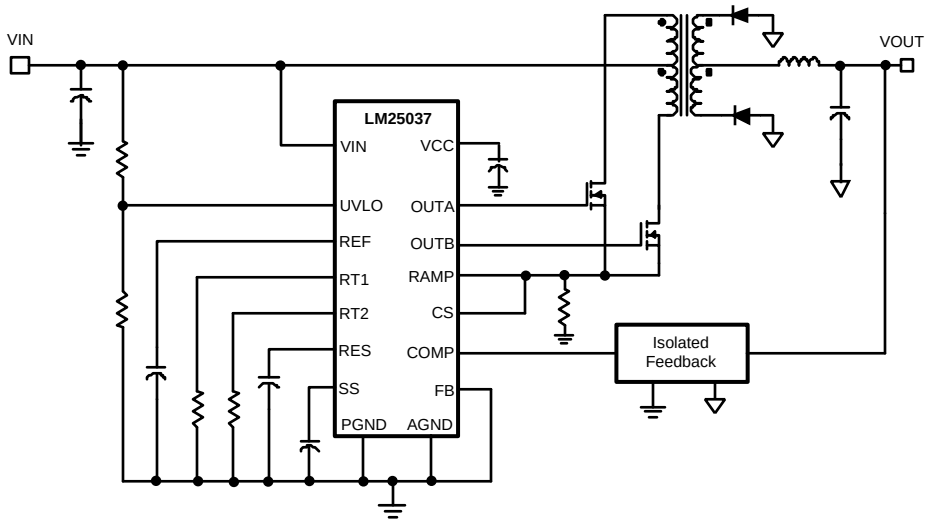
The LM25037 PWM controller contains all the features necessary to implement balanced double-ended power converter topologies, such as push-pull, half-bridge and full-bridge. These double-ended topologies allow for higher efficiencies and greater power densities compared to common single-ended topologies such as the flyback and forward. The LM25037 can be configured for either voltage mode or current mode control with minimum external components. Two alternating gate drive outputs are provided, each capable of 1.2-A peak output current. The LM25037 can be configured to operate directly from the input voltage rail over an ultra-wide range of 5.5 V to 75 V. Additional features include programmable maximum duty cycle limit, line undervoltage lockout, cycle-by-cycle current limit and a hiccup mode fault protection with adjustable timeout delay, soft-start and a 2-MHz capable oscillator with synchronization capability, precision reference and thermal shutdown.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM25037 LM25037-Q1	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Push-Pull Power Converter



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2013) to Revision E	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted Typical Application Circuit Efficiency (previously Figure 1.) graph from *Typical Characteristics*	7

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	24

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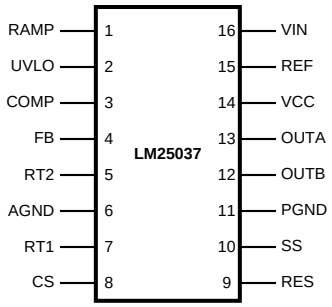
5 Pin Configuration and Functions

PW Package
16-Pin TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION	APPLICATION INFORMATION
NO.	NAME			
1	RAMP	I	Pulse width modulator ramp	Modulation ramp for the PWM comparator. This ramp can be a representative of the primary current (current mode) or proportional to input voltage (feed-forward voltage mode). This pin is reset to ground at the conclusion of every cycle by an internal FET.
2	UVLO	I	Line undervoltage lockout	An external voltage divider from the power source sets the shutdown and standby comparator threshold levels. When UVLO exceeds the 0.45V shutdown threshold, the VCC and REF regulators are enabled. When UVLO exceeds the 1.25V standby threshold, the SS pin is released and the device enters the active mode.
3	COMP	I/O	Input to the pulse width modulator	Output of the error amplifier and input to the PWM comparator.
4	FB	I	Feedback	Connected to inverting input of the error amplifier. An internal 1.25-V reference is connected to the noninverting input of the error amplifier. In isolated applications using an external error amplifier, this pin should be connected to the AGND pin.
5	RT2	I	Oscillator dead-time control	The resistance connected between RT2 and AGND sets the forced dead-time between switching periods of the alternating outputs.
6	AGND	—	Analog ground	Connect directly to Power Ground.
7	RT1	I	Oscillator maximum on-time control	The resistance connected between RT1 and AGND sets the oscillator maximum on-time. The sum of this maximum on-time and the forced dead-time (set by RT2) sets the oscillator period.
8	CS	I	Current sense input	If CS exceeds 250 mV the output pulse will be terminated, entering cycle-by-cycle current limit. An internal switch holds CS low for 65 nS after either output switches high to blank leading edge transients.
9	RES	I/O	Restart timer	If cycle-by-cycle current limit is reached during any cycle, a 18-µA current is sourced to the external RES pin capacitor. If the RES capacitor voltage reaches 2 V, the soft-start capacitor will be fully discharged and then released with a pullup current of 1 uA. After the first output pulse (when SS = 1V), the SS pin charging current will increase to the normal level of 100 µA.
10	SS	I	Soft-start	An external capacitor and an internal 100uA current source set the soft-start ramp. The SS current source is reduced to 1 µA following a restart event (RES pin high).
11	PGND	—	Power ground	Connect directly to Analog Ground
12	OUTB	O	Output driver	Alternating gate drive output of the pulse width modulator. Capable of 1.2-A peak source and sink current.
13	OUTA	O	Output driver	Alternating gate drive output of the pulse width modulator. Capable of 1.2-A peak source and sink current.
14	VCC	I/O	Output of the high voltage start-up regulator. The VCC voltage is regulated to 7.7 V.	If an auxiliary winding raises the voltage on this pin above the regulation set point, the internal start-up regulator will shutdown thus reducing the IC power dissipation. Locally decouple VCC with a 0.47 µF or greater capacitor.

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Pin Functions (continued)

PIN		I/O	DESCRIPTION	APPLICATION INFORMATION
NO.	NAME			
15	REF	O	Output of a 5-V reference	Locally decouple with a 0.1 µF or greater capacitor. Maximum output current is 10 mA (typical).
16	VIN	I	Input voltage source	Input to the VCC Start-up regulator. Operating input range is 5.5 V to 75 V. For power sources outside of this range, the LM25037 can be biased directly at VCC by an external regulator.

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)[(1)(2)]

	MIN	MAX	UNIT
VIN to GND	–0.3	76	V
VCC, RAMP , OUTA, OUTB to GND	–0.3	16	V
CS to GND	–0.3	1	V
UVLO, FB, RT2, RT1, SS, REF to GND	–0.3	7	V
COMP, RES[(3)]			
Junction temperature		150	°C
Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) COMP, RES are output pins. As such, TI does not recommend connecting external power sources to these pins.

6.2 ESD Ratings: LM25037

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings: LM25037-Q1

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[(1)]		±2000	V
	Charged-device model (CDM), per AEC Q100-011	All pins	±750	
		Corner pins (1, 8, 9, 16)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.4 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
VIN voltage	5.5		75	V
External voltage applied to VCC	8		14	V
Operating junction temperature	−40		125	°C

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6.5 Thermal Information

THERMAL METRIC[1]		LM25037/LM25037-Q1 PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	99.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.6 Electrical Characteristics

V_{VIN} = 12V, V_{VCC} = 10V, R_{RT1} = 30.1 kΩ, R_{RT2} = 30.1 kΩ, V_{UVLO} = 3 V, T_J =−40°C to +125° unless otherwise stated.[1][2]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
START-UP REGULATOR (VCC PIN)						
V_{VCC}	VCC voltage	I_{VCC} = 10 mA	7.2	7.7	8.1	V
$I_{VCC(Lim)}$	VCC current limit	V_{VCC} = 7 V	20			mA
$V_{VCC(UV)}$	VCC Undervoltage threshold		4.6	5	5.4	V
	Hysteresis			0.5		V
I_{VIN}	Start-up regulator current	V_{VIN} = 20 V, V_{UVLO} = 0 V		35	58	µA
		V_{VIN} = 75 V, V_{UVLO} = 0 V		45	80	µA
	Supply current into VCC from external source	Outputs and COMP open, V_{VCC} = 10 V, Outputs switching		4		mA
VOLTAGE REFERENCE REGULATOR (REF PIN)						
V_{REF}	REF Voltage	I_{REF} = 0 mA	4.75	5	5.15	V
	REF Voltage Regulation	I_{REF} = 0 to 2.5 mA		7	25	mV
$I_{REF(Lim)}$	REF Current Limit	V_{REF} = 4.5 V	5	10		mA
	VREF Undervoltage threshold		3.7	4	4.3	V
$V_{REF(UV)}$	Hysteresis			0.4		V
UNDERVOLTAGE LOCKOUT AND SHUTDOWN (UVLO PIN)						
V_{UVLO}	Undervoltage threshold		1.20	1.25	1.295	V
I_{UVLO}	Hysteresis current	UVLO pin sinking	17	22	26	µA
	Undervoltage shutdown threshold	UVLO voltage rising	0.35	0.45	0.6	V
	Hysteresis			0.1		V
CURRENT SENSE INPUT (CS PIN)						
V_{CS}	Current limit threshold		0.22	0.255	0.29	V
	CS delay to output	CS from 0 V to 1 V. Time for OUTA and OUTB to fall to 90% of VCC. Output load = 0 pF.		27		ns
	Leading edge blanking time at CS			65		ns
	CS sink impedance (clocked)	Internal FET sink impedance		21	45	Ω

(1) All limits are ensured. All electrical characteristics having room temperature limits are tested during production at T_A = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Typical specifications represent the most likely parametric norm at 25°C operation.

Electrical Characteristics (continued)

V_{VIN} = 12V, V_{VCC} = 10V, R_{RT1} = 30.1 kΩ, R_{RT2} = 30.1 kΩ, V_{UVLO} = 3 V, T_J =−40°C to +125° unless otherwise stated.(1)(2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
CURRENT LIMIT RESTART (RES PIN)							
V_{RES}	RES threshold			1.9	2	2.2	V
	Charge source current	V_{RES} = 1.5 V		14	18	21	µA
	Discharge sink current	V_{RES} = 1 V		5	8	11	µA
SOFT-START (SS PIN)							
I_{SS}	Charging current in normal operation	V_{SS} = 0		70	100	130	µA
	Charging current during a hiccup mode restart	V_{SS} = 0		0.6	1	1.4	µA
	Soft-stop current sink	V_{SS} = 2 V		70	100	130	µA
OSCILLATOR (RT1 AND RT2 PINS)							
DT_1	Dead-time 1	R_{RT2} = 15 kΩ		40	75	105	ns
DT_2	Dead-time 2	R_{RT2} = 50 kΩ			250		ns
F_{SW1}	Frequency 1 (at OUTA, half oscillator frequency)	R_{RT1} = 30.1 kΩ, R_{RT2} = 30.1 kΩ,		178	200	222	kHz
F_{SW2}	Frequency 2 (at OUTA, half oscillator frequency)	R_{RT1} = 11 kΩ, R_{RT2} = 30.1 kΩ,		448	515	578	kHz
	DC level				2		V
	Input sync threshold			2.5	3	3.4	V
PWM CONTROLLER (COMP PIN)							
	Delay to output				65		ns
V_{PWM-OS}	SS to RAMP offset			0.7	1	1.2	V
	Minimum duty cycle	V_{SS} = 0 V	T_J = 25°C			0%	
	COMP open-circuit voltage	V_{FB} = 0 V		4.5	4.75	5	V
	COMP short-circuit current	V_{FB} = 0 V, COMP = 0 V		0.5	1	1.5	mA
VOLTAGE FEED-FORWARD (RAMP PIN)							
	RAMP sink impedance (clocked)				5	20	Ω
ERROR AMPLIFIER							
GBW	Gain bandwidth				4		MHz
	DC gain				75		dB
	Input voltage	V_{FB} = COMP		1.22	1.245	1.27	V
	COMP sink capability	V_{FB} = 1.5 V COMP = 1 V	T_J = 25°C	5	13		mA
	FB bias current				10		nA
MAIN OUTPUT DRIVERS (OUTA and OUTB Pins)							
	Output high voltage	I_{OUT} = 50 mA, (source)		Vcc-0.5	Vcc-0.25		V
	Output low voltage	I_{OUT} = 100 mA (sink)			0.2	0.5	V
	Rise time	C_{LOAD} = 1 nF			17		ns
	Fall time	C_{LOAD} = 1 nF			18		ns
	Peak source current	V_{VCC} = 10 V			1.2		A
	Peak sink current	V_{VCC} = 10 V			1.2		A
THERMAL SHUTDOWN							
T_{SD}	Thermal shutdown threshold				165		°C
	Thermal shutdown hysteresis				25		°C

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6.7 Typical Characteristics

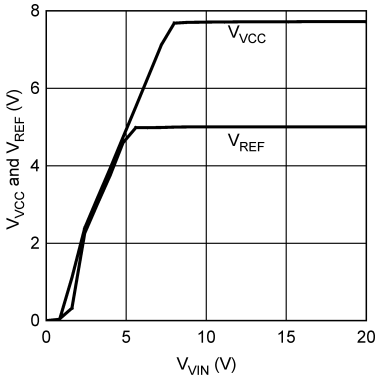

Figure 1. V_{VCC} and V_{REF} vs V_{VIN}

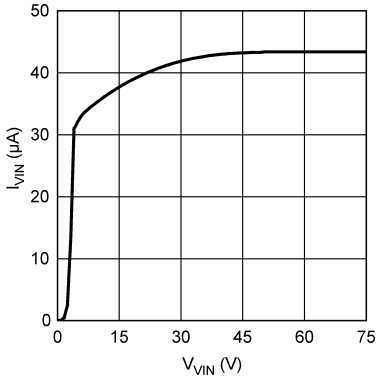

Figure 2. Start-Up Regulator Current (UVLO = 0)

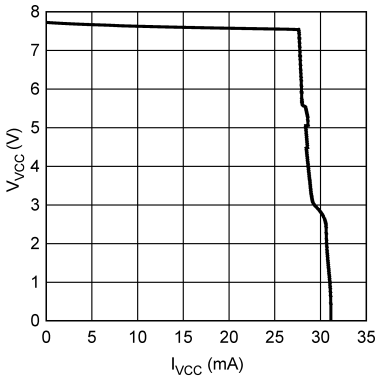

Figure 3. V_{VCC} vs I_{VCC}

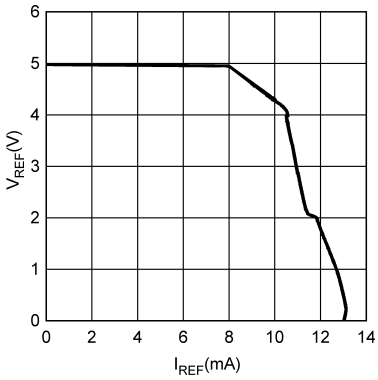

Figure 4. V_{REF} vs I_{REF}

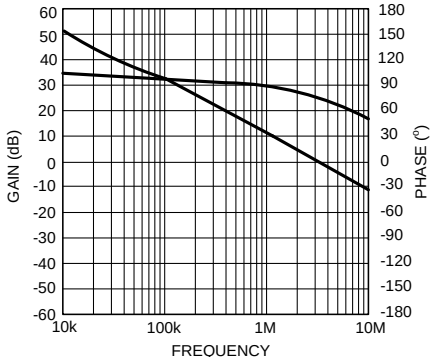

Figure 5. Feedback Amplifier Gain/Phase

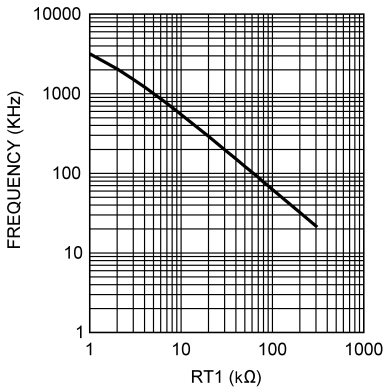

Figure 6. Oscillator Frequency vs RT1

Typical Characteristics (continued)

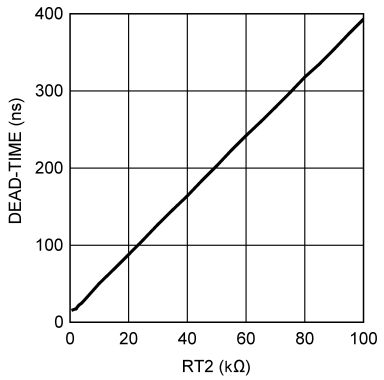

Figure 7. Dead-Time vs RT2

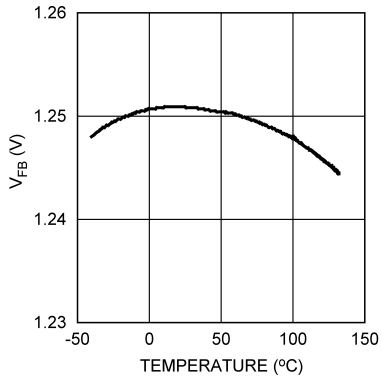

Figure 8. V_{FB} vs Temperature

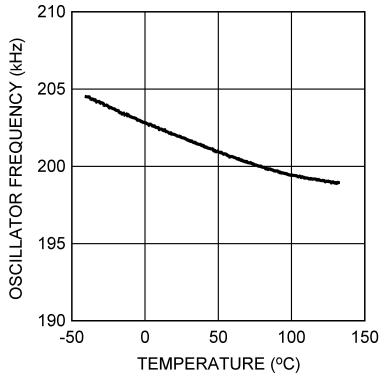

Figure 9. Oscillator Frequency vs Temperature

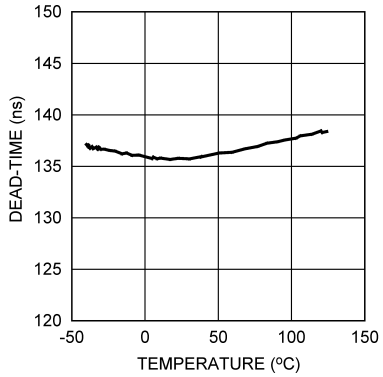

Figure 10. Dead-Time vs Temperature

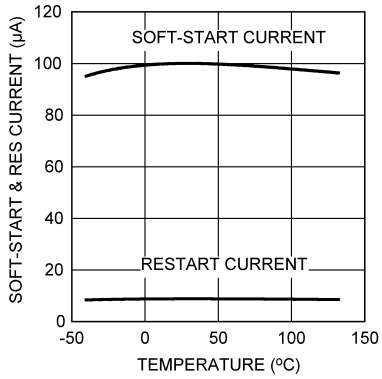

Figure 11. Soft-Start and Restart Current vs Temperature

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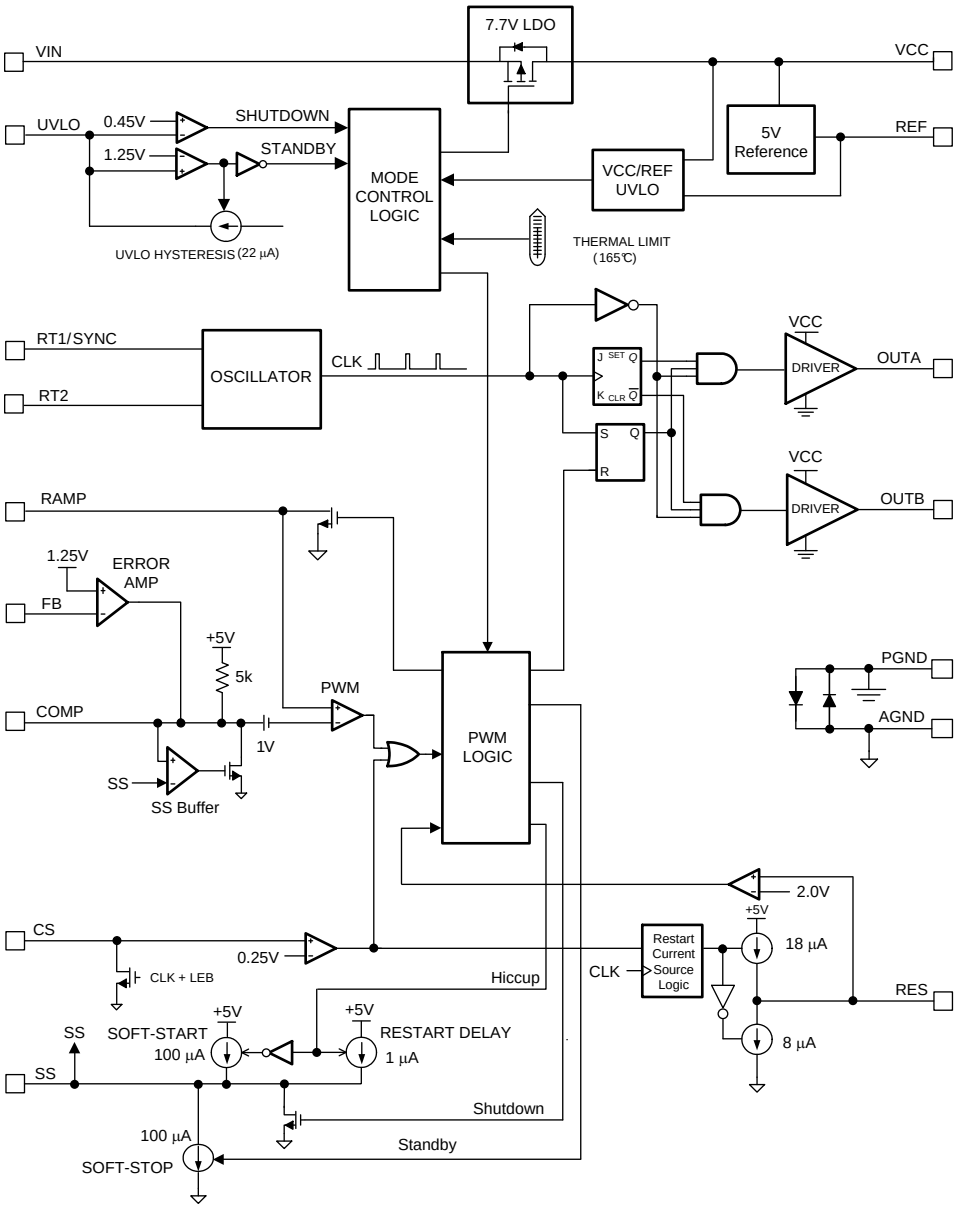
7 Detailed Description

7.1 Overview

The LM25037 PWM controller contains all the features necessary to implement double-ended power converter topologies such as push-pull, half-bridge and full-bridge. The unique architecture allows the modulator to be configured for either voltage-mode or current-mode control. The LM25037 provides two alternating gate driver outputs to drive the primary side power MOSFETs with programmable forced dead-time. The LM25037 can be configured to operate with bias voltages ranging from 5.5 V to 75 V. Additional features include line undervoltage lockout, cycle-by-cycle current limit, voltage feed-forward compensation, and hiccup mode fault protection with adjustable delays, soft-start, and a 2-MHz capable oscillator with synchronization capability, precision reference, and thermal shutdown. These rich set of features simplify the design of double ended topologies. The functional block diagram is show in the *Functional Block Diagram* section.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 High-Voltage Start-Up Regulator

The LM25037 contains an internal high voltage, low drop-out start-up regulator that allows the input pin (VIN) to be connected directly to the supply voltage over a range of 5.5 V to a maximum of 75 V. The regulator output at VCC (7.7 V) is internally current limited with a specified minimum of 20 mA. When the UVLO pin potential is greater than 0.45 V, the VCC regulator is enabled to charge an external capacitor connected to the VCC pin. The VCC regulator provides power to the voltage reference (REF) and the gate drivers (OUTA and OUTB). When the voltage on the VCC pin exceeds its undervoltage (VCC UV) threshold of 5-V nominal, the internal voltage reference (REF) reaches its regulation set point of 5 V and the UVLO voltage is greater than 1.25 V, the controller outputs are enabled. The value selected for the VCC capacitor depends on the total system design, and its start-up characteristics. The recommended range of values for the VCC capacitor is 0.47 µF to 10 µF. The internal power dissipation of the LM25037 can be reduced by powering VCC from an external supply. In typical applications, an auxiliary transformer winding is connected through a diode to the VCC pin. This winding must raise the VCC voltage above 8.2 V to shut off the internal start-up regulator. Powering VCC from an auxiliary winding improves efficiency while reducing the controller's power dissipation. The VCC UV circuit will still function in this mode, requiring that VCC never falls below 5-V nominal during the start-up sequence. The VCC regulator series pass transistor includes a diode between VCC and VIN that should not be forward biased in normal operation. Therefore the auxiliary VCC voltage should never exceed the VIN voltage.

An external DC bias voltage can be used instead of the internal regulator by connecting the external bias voltage to both the VCC and the VIN pins. In this particular case, the external bias must be greater than max VCC UV of 5.4 V and less than the VCC maximum operating voltage rating (14 V).

7.3.2 Line Undervoltage Detector

The LM25037 contains a dual level line Undervoltage Lock Out (UVLO) circuit. When the UVLO pin voltage is less than 0.45 V, the controller is in a low current shutdown mode. When the UVLO pin voltage is greater than 0.45 V but less than 1.25 V, the controller is in standby mode. In standby mode the VCC and REF bias regulators are active while the controller outputs are disabled. When the VCC and REF outputs exceed their respective undervoltage thresholds and the UVLO pin voltage is greater than 1.25 V, the outputs are enabled and normal operation begins. An external set-point voltage divider from VIN to GND can be used to set the minimum operating voltage of the converter. The divider must be designed such that the voltage at the UVLO pin will be greater than 1.25 V when VIN enters the desired operating range. UVLO hysteresis is accomplished with an internal 22-µA current source that is switched on or off into the impedance of the set-point divider. When the UVLO pin voltage exceeds 1.25-V threshold, the current source is activated to quickly raise the voltage at the UVLO pin. When the UVLO pin voltage falls below the 1.25-V threshold, the current source is disabled causing the voltage at the UVLO pin to quickly fall. The hysteresis of the 0.45-V shutdown comparator is internally fixed at 100 mV.

The UVLO pin can also be used to implement various remote enable/disable functions. Turning off the converter by forcing the UVLO pin to standby condition provides a controlled soft-stop. See the *Soft-Start* section for more details.

7.3.3 Reference

The REF pin is the output of a 5-V linear regulator that can be used to bias an opto-coupler transistor and external housekeeping circuits. The regulator output is internally current limited to 10 mA (typical).

7.3.4 Error Amplifier

An internal high gain error amplifier is provided within the LM25037. The amplifier's noninverting reference is tied to a 1.25-V reference. In non-isolated applications the power converter output is connected to the FB pin through the voltage setting resistors and loop compensation is connected between the COMP and FB pins. A typical gain/phase plot is shown in *Typical Characteristics*.

For most isolated applications the error amplifier function is implemented on the secondary side. Because the internal error amplifier is configured as an open-drain output, it can be disabled by connecting FB to ground. The internal 5-K pullup resistor connected between the COMP pin and the 5-V reference can be used as the pullup for an opto-coupler or other isolation device.

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Feature Description (continued)

7.3.5 Cycle-By-Cycle Current Limit

The CS pin is to be driven by a signal representative of the transformer primary current. The current sense signal can be generated by using a sense resistor or a current sense transformer. If the voltage sensed at the CS pin exceeds 0.255 V, the current sense comparator terminates the output driver pulse. If the high current condition persists, the controller operates in a cycle-by-cycle current limit mode with duty cycle determined by the current sense comparator instead of the PWM comparator. Cycle-by-cycle current limiting may eventually trigger the hiccup mode restart cycle; depending on the configuration of the RES pin (see *Overload Protection Timer*). To suppress noise, TI recommends connecting a small R-C filter to the CS pin and placing it near the controller. An internal 21-Ω MOSFET discharges the external current sense filter capacitor at the conclusion of every cycle. The discharge MOSFET remains on for an additional 65 ns after either OUTA or OUTB driver switches high to blank leading edge transients in the current sensing circuit. Discharging the CS pin filter each cycle and blanking leading edge spikes reduces the filtering requirements and improves the current sense response time. The current sense comparator is very fast and may respond to short duration noise pulses. Layout considerations are critical for the current sense filter and sense resistor. The capacitor associated with the CS filter must be placed very close to the device and connected directly to the CS and AGND pins. If a sense resistor located in the source of the main MOSFET switch is used for current sensing, a low inductance type of resistor is required. When designing with a current sense resistor, all the noise sensitive, low power ground connections should be connected together near the AGND pin, and a single connection should be made to the power ground (sense resistor ground point).

7.3.6 Overload Protection Timer

The LM25037 provides a current limit restart timer to disable the outputs and force a delayed restart (hiccup mode) if a current limit condition is repeatedly sensed. The number of cycle-by-cycle current limit events required to trigger the restart is programmed by the external capacitor at the RES pin. During each PWM cycle, the LM25037 either sources to or sinks current from the RES pin capacitor. If no current limit is detected during a cycle, a 8-µA discharge current sink is enabled to pull the RES pin towards ground. If a current limit is detected, the 8 µA sink current is disabled and an 18-µA current source causes the voltage at the RES pin to gradually increase. The LM25037 protects the converter with cycle-by-cycle current limiting while the voltage at RES pin increases. If the RES voltage reaches the 2-V threshold, the following restart sequence occurs (also see Figure 12):

- The RES capacitor and SS capacitors are fully discharged.
- The soft-start current source is reduced from 100 µA to 1 µA.
- The SS capacitor voltage slowly increases. When the SS voltage reaches ≅1 V, the PWM comparator will produce the first narrow output pulse. After the first pulse occurs, the SS source current reverts to the normal 100-µA level. The SS voltage increases at its normal rate, gradually increasing the duty cycle of the output drivers.
- If the overload condition persists after restart, cycle-by-cycle current limiting will begin to increase the voltage on the RES capacitor again, repeating the hiccup mode sequence.
- If the overload condition no longer exists after restart, the RES pin will be held at ground by the 8-µA current sink and normal operation resumes.

The overload timer function is very versatile and can be configured for the following modes of protection:

1. **Cycle-by-cycle only:** The hiccup mode can be completely disabled by connecting a 0-kΩ to 50-kΩ resistor from the RES pin to AGND. In this configuration, the cycle-by-cycle protection will limit the output current indefinitely and no hiccup sequences will occur.
2. **Hiccup only:** The timer can be configured for immediate activation of a hiccup sequence upon detection of an overload by leaving the RES pin open circuit. In this configuration, the first detection of current limit condition by the CS pin comparator will initiate a hiccup cycle with SS capacitor fully discharged and a delayed restart.
3. **Delayed Hiccup:** Connecting a capacitor to the RES pin provides a programmed interval of cycle-by-cycle limiting before initiating a hiccup mode restart, as previously described. The dual advantages of this configuration are that a short term overload will not cause a hiccup mode restart but during extended overload conditions, the average dissipation of the power converter will be very low.
4. **Externally Controlled Hiccup:** The RES pin can also be used as an input. By externally driving the pin to a level greater than the 2-V hiccup threshold, the controller will be forced into the delayed restart sequence.

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Feature Description (continued)

For example, the external trigger for a delayed restart sequence could come from an overtemperature protection circuit or an output overvoltage sensor.

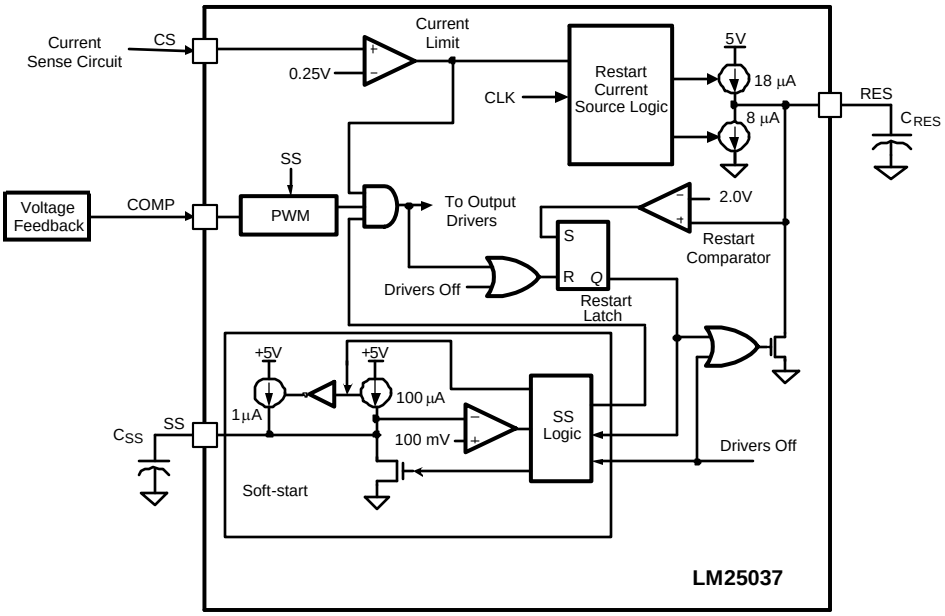

Figure 12. Current Limit Restart Circuit

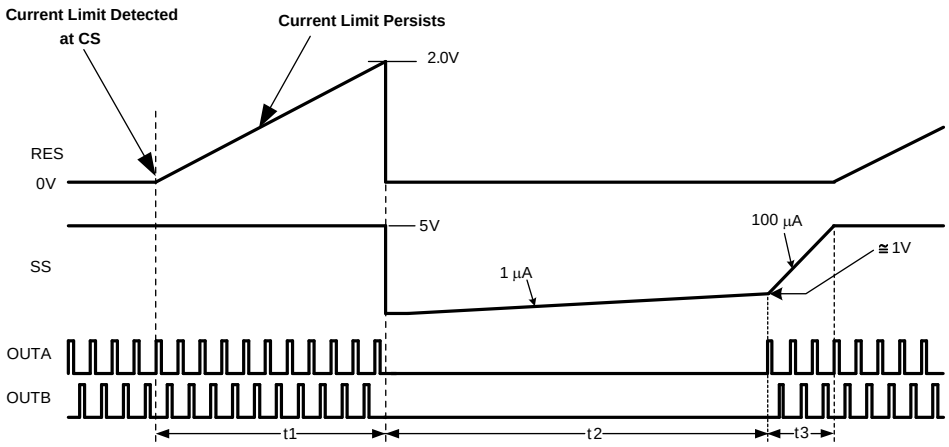

Figure 13. Current Limit Restart Timing

7.3.7 Soft-Start

The soft-start circuit allows the regulator to gradually reach a steady-state operating point, thereby reducing start-up stresses and current surges. When bias is supplied to the LM25037, the SS pin capacitor is discharged by an internal MOSFET. When the UVLO, VCC and REF pins reach their operating thresholds, the SS capacitor is released and charged with a 100-µA current source. The PWM comparator control voltage at the COMP pin is clamped to the SS pin voltage by an internal amplifier. When the PWM comparator input reaches 1 V, output pulses commence with slowly increasing duty cycle. The voltage at the SS pin eventually increases to 5 V, while the voltage at the PWM comparator increases to the value required for regulation as determined by the voltage feedback loop.

One method to disable the regulator is to ground the SS pin. This forces the internal PWM control signal to ground, reducing the output duty cycle quickly to zero. Releasing the SS pin initiates a soft-start sequence and normal operation resumes. A second shutdown method is discussed in *UVLO Divider Selection*.

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Feature Description (continued)

7.3.8 PWM Comparator

The pulse width modulation (PWM) comparator compares the voltage ramp signal at the RAMP pin to the loop error signal. The loop error signal is derived from the internal error amplifier (COMP pin). The resulting control voltage passes through a 1-V level shift before being applied to the PWM comparator. This comparator is optimized for speed to achieve minimum controllable duty cycles. The common mode input voltage range of the PWM comparator is from 0 V to 4.3 V.

7.3.9 RAMP Pin

The voltage at the RAMP pin provides the modulation ramp for the PWM comparator. The PWM comparator compares the modulation ramp signal at the RAMP pin to the loop error signal to control the output duty cycle. The modulation ramp can be implemented either as a ramp proportional to input voltage, known as feed-forward voltage mode control, or as a ramp proportional to the primary current, known as current mode control. The RAMP pin is reset by an internal FET with an $R_{DS(ON)}$ of 5 Ω (typical) at the end of every cycle. The ability to configure the RAMP pin for either voltage mode or current mode allows the controller to be implemented for the optimum control method for the selected power stage topology. Configuring RAMP pin is explained below and the differences between voltage mode control and current mode control in various double-ended topologies is explained in *Application and Implementation*.

7.4 Device Functional Modes

7.4.1 Feed-Forward Voltage Mode

An external resistor (R_{FF}) and capacitor (C_{FF}) connected to VIN, AGND, and the RAMP pins is required to create the PWM ramp signal as shown in Figure 14. It can be seen that the slope of the signal at RAMP will vary in proportion to the input line voltage. This varying slope provides line feed-forward information necessary to improve line transient response with voltage mode control. The RAMP signal is compared to the error signal by the pulse width modulator comparator to control the duty cycle of the outputs. With a constant error signal, the on-time (t_{ON}) varies inversely with the input voltage (VIN) to stabilize the Volt • Second product of the transformer primary. At the end of clock period, an internal FET will be enabled to reset the C_{FF} capacitor. The formulae for R_{FF} and C_{FF} and component selection criteria are explained in the *Application and Implementation* section. The amplitude of the signal driving RAMP pin must not exceed the common mode input voltage range of the PWM comparator (3.3 V) while in normal operation.

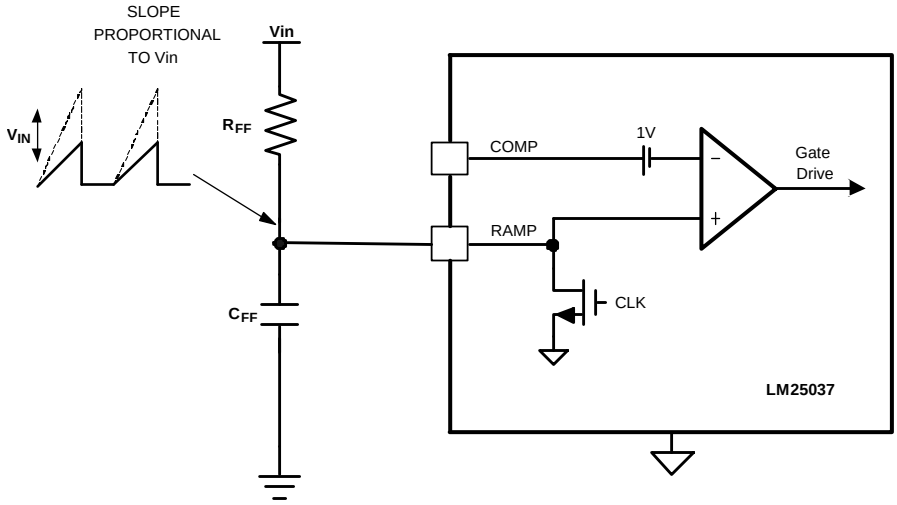

Figure 14. Feed-Forward Voltage Mode Configuration

Device Functional Modes (continued)

7.4.2 Current Mode

The LM25037 can be configured for current mode control by injecting a signal representative of primary current into the RAMP pin. One way to achieve this is shown in Figure 15. Filter components R_{filter} and C_{filter} are used to filter leading edge noise spikes. The signal at the CS pin is thus a ramp on a pedestal. The pedestal corresponds to the continuous conduction current in the transformer at the beginning of an OUTA or OUTB conduction cycle. The R-C circuit (R_{Slope} and C_{Slope}), shown in Figure 15, tied to V_{REF} adds an additional ramp to the current sense signal. This additional ramp signal, known as slope compensation, is required to avoid instabilities at duty cycles above 50% (25% per phase). The compensated RAMP signal consists of two parts, the primary current signal and the slope compensation. The compensated RAMP signal is compared to the error signal by the PWM comparator to control the duty cycle of the outputs. The RAMP capacitor and CS capacitor are reset through internal discharge FETs. The $R_{DS(ON)}$ of RAMP discharge FET is 5 Ω (typical); this ensures fast discharge of the RAMP reset capacitor. Any DC voltage source can be used in place of V_{REF} to generate the slope compensation ramp.

The timing diagram shown in Figure 16 depicts the current mode waveforms and relative timing. When OUTA or OUTB is enabled, the signal at the RAMP pin consists of the CS pin signal (current ramp on a pedestal) plus the slope compensation ramp (dotted lines). When OUTA or OUTB is turned off, the primary current component is absent but the voltage at the RAMP pin continues to rise due to slope compensation component until the end of the clock period, after which it is reset by the RAMP discharge FET. A component selection example is explained in detail in *Application and Implementation*.

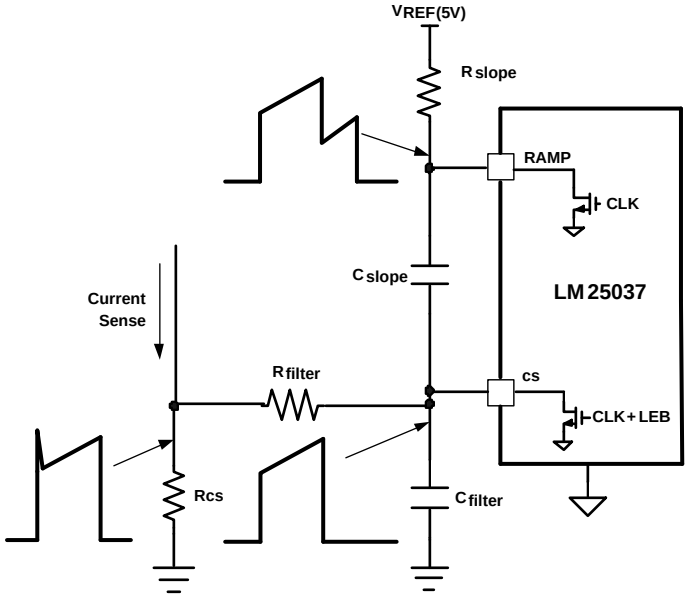

Figure 15. Current Mode Configuration With Slope Compensation

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Device Functional Modes (continued)

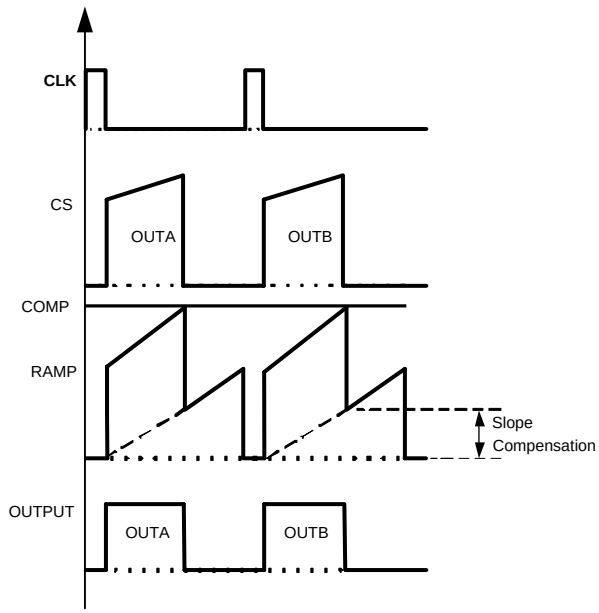

Figure 16. Timing Diagram for Current Mode Configuration

7.4.3 Oscillator

The LM25037 oscillator frequency and the maximum duty cycle are set by two external resistors connected between the RT1 and RT2 pins to AGND. The minimum dead-time between OUTA and OUTB pulses is proportional to the RT2 resistor value and the overall oscillator frequency is inversely proportional to RT1 and RT2 resistor values. Each output switches at half the oscillator frequency. Initially, RT2 should be selected for the desired dead-time or for the desired maximum duty cycle (D_{max}), as given by Equation 1.

$$RT2 = \frac{\text{Dead-Time}}{5.0 \times 10^{-12}} \quad 50\ \text{ns} < DT < 250\ \text{ns}$$

or

$$RT2 = \frac{(1 - D_{max}) / F_{OSC}}{5.0 \times 10^{-12}} \tag{1}$$

TI recommends setting the dead-time range from 50 ns to 250 ns. Beyond 250 ns, RT2 becomes excessively large, and is prone to noise pickup. Fixed internal delays limit the dead-time to greater than 50 ns. After the dead-time has been programmed by RT2, the overall oscillator frequency can be set by selecting resistor RT1 from Equation 2:

$$RT1 = \frac{\frac{1}{F_{OSC}} - (\text{Dead-Time})}{0.162 \times 10^{-9}} \tag{2}$$

For example, if the desired oscillator frequency is 400 kHz (OUTA and OUTB each switching at 200 kHz) and desired dead-time is 100 ns, the maximum duty cycle for each output will be 96% and the values of RT1 and RT2 will be 15 kΩ and 20 kΩ respectively.

Device Functional Modes (continued)

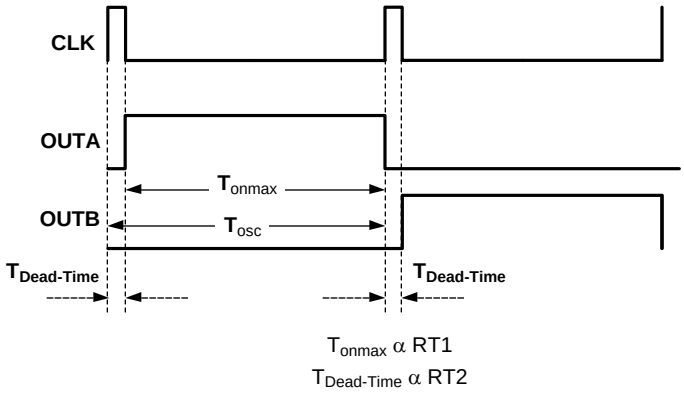

Figure 17. Timing Diagram of OUTA, OUTB and Dead-Time Set By RT2

As shown in Figure 17, the internal clock pulse width is the same as the dead-time set by RT2. This dead-time pulse is used to limit the maximum duty cycle for each of the outputs. Also, the discharge FET connected to the RAMP pin is enabled during the dead-time every clock period. The voltages at both the RT1 and RT2 pins are internally regulated to a nominal 2 V. Both the resistors RT1 and RT2 should be located as close as possible to the IC, and connected directly to the pins. The tolerance of the external resistors and the frequency tolerance indicated in *Electrical Characteristics* must be considered when determining the worst case frequency range.

7.4.4 Sync Capability

The LM25037 can be synchronized to an external clock by applying a narrow AC pulse to the RT1 pin. The external clock must be at least 10% higher than the free-running oscillator frequency set by the RT1 and RT2 resistors. If the external clock frequency is less than the programmed frequency, the LM25037 will ignore the synchronizing pulses. The synchronization pulse width at the RT1 pin must be a minimum of 15-ns wide. The synchronization signal should be coupled into the RT1 pin through a 100-pF capacitor or another value small enough to ensure the sync pulse width at RT1 is less than 60% of the clock period under all conditions. When the synchronizing pulse transitions from low-to-high (rising edge), the voltage at the RT1 pin must be driven to exceed 3 V from its nominal 2-V DC level. During the synchronization clock signal's low time, the voltage at the RT1 pin will be clamped at 2 V by an internal regulator. The RT1 and RT2 resistors are always required, whether the oscillator is free running or externally synchronized.

7.4.5 Gate Driver Outputs (OUTA and OUTB)

The LM25037 provides two alternating gate driver outputs, OUTA and OUTB. The internal gate drivers can each source and sink 1.2-A peak each. The maximum duty cycle is inherently limited to less than 50% and is based on the value of RT2 resistor. As an example, if the COMP pin is in a high state, RT1 = 15 K and RT2 = 20 K then the outputs will operate at maximum duty cycle of 96%.

7.4.6 Thermal Protection

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event the maximum rated junction temperature is exceeded. When activated, typically at 165°C, the controller is forced into a low power standby state with the output drivers (OUTA and OUTB) and the bias regulators (VCC and REF) disabled. This helps to prevent catastrophic failures from accidental device overheating. During thermal shutdown, the soft-start capacitor is fully discharged and the controller follows a normal start-up sequence after the junction temperature falls to the operating level (140°C).

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Topology and Control Algorithm Choice

The LM25037 has all the features required to implement double-ended power converter topologies such as push-pull, half-bridge and full-bridge with minimum external components. One key feature is the flexibility in control algorithm selection; that is, the LM25037 can be used to implement either voltage mode control or current mode control. Designers familiar with these topologies recognize that conventionally, current mode control is used for push-pull and full-bridge topologies while voltage mode control is required for the half-bridge topology. In limited applications, voltage mode control can be used for push-pull and full-bridge topologies as well, with special care to maintain flux balance, such as using a DC-blocking capacitor in the primary (full-bridge). The goal of this section is to illustrate implementation of both current mode control and voltage mode control using the LM25037 and aid the designer in the design process.

8.1.2 Voltage Mode Control Using the LM25037

An external resistor (R_{FF}) and capacitor (C_{FF}) connected to VIN, AGND, and the RAMP pins is required to create a saw-tooth modulation ramp signal shown in Figure 18. The slope of the signal at RAMP will vary in proportion to the input line voltage. The varying slope provides line feed-forward information necessary to improve line transient response with voltage mode control. With a constant error signal, the on-time (t_{ON}) varies inversely with the input voltage (VIN) to stabilize the volt-second product of the transformer primary. Using a line feed-forward ramp for PWM control requires very little change in the voltage regulation loop to compensate for changes in input voltage, as compared to a fixed slope oscillator ramp. Furthermore, voltage mode control is less susceptible to noise and does not require leading edge filtering, and is therefore a good choice for wide input range power converters. Voltage mode control requires a more complicated compensation network, due to the complex-conjugate poles of the L-C output filter.

In push-pull and full-bridge topologies, any asymmetry in the volt-second product applied to primary in one phase may not be cancelled by subsequent phase, possibly resulting in a DC current build-up in the transformer, which pushes the transformer core towards saturation. Special care in the transformer design, such as gapping the core, or adding ballasting resistance in the primary is required to rectify this imbalance when using voltage mode control with these topologies. Current mode control naturally corrects for any volt-second asymmetry in the primary.

The recommended capacitor value range for C_{FF} is from 100 pF to 1500 pF. Referring to Figure 18, it can be seen that value C_{FF} must be small enough such that the capacitor can be discharged within the clock (CLK) pulse width each cycle. The CLK pulse width is same as the dead-time set by RT2. The minimum possible dead-time for LM25037 is 50 ns and the internal discharge FET $R_{DS(ON)}$ is 5 Ω (typical),

The value of R_{FF} required can be calculated using Equation 3.

$$R_{FF} = \frac{-1}{F_{OSC} \times C_{FF} \times \ln\left(1 - \frac{V_{RAMP}}{VIN_{min}}\right)} \tag{3}$$

For example, assuming a V_{Ramp} of 1 volt at VIN_{min} (a good compromise of signal range and noise immunity), oscillator frequency, F_{OSC} of 250 kHz, VIN_{min} of 24 V, and C_{FF} = 270 pF results in a value for R_{FF} of 348 kΩ.

Application Information (continued)

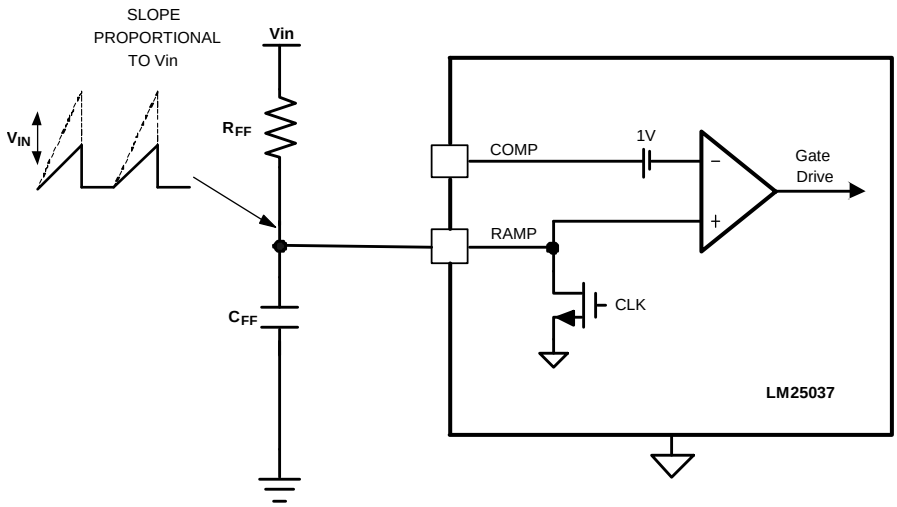

Figure 18. Feed-Forward Voltage Mode Configuration

8.1.3 Current Mode Control Using the LM25037

The LM25037 can be configured in current mode control by applying the primary current signal into the RAMP pin. One way to achieve this is shown in Figure 19, which depicts a simplified push-pull converter. The primary current is sensed using a sense resistor and the current information is then filtered and applied to the RAMP pin through capacitor C_{slope}, for use as the modulation ramp. It can be seen that the signal applied to the RAMP pin consists of the primary current information from the CS pin plus an additional ramp for slope compensation, added by R_{slope} and C_{slope}.

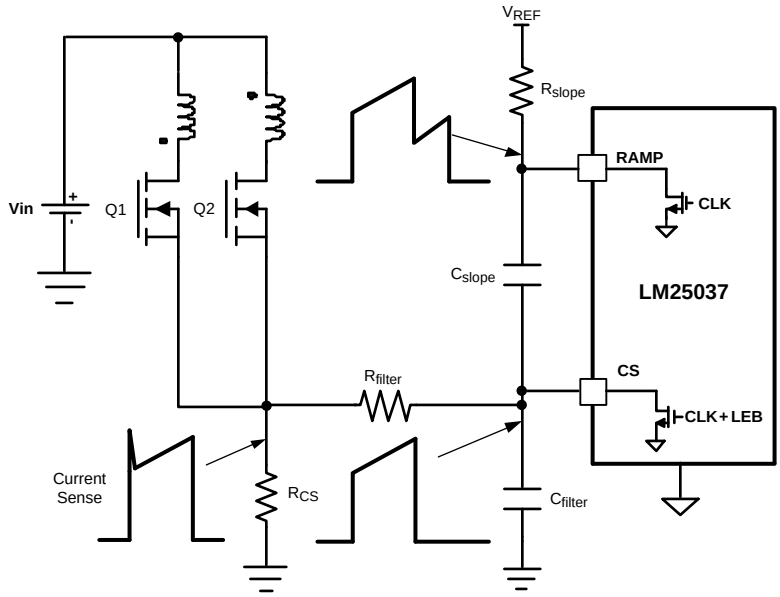

Figure 19. Current Mode Configuration

Current mode control inherently provides line voltage feed-forward, cycle-by-cycle current limiting and ease of loop compensation as it removes the additional pole due to output inductor. Also, in push-pull and full-bridge converters, current mode control inherently balances volt-second product in both the phases by varying the duty cycle as needed to terminate the cycle at the same peak current for each output phase. For duty cycles greater than 50% (25% for each phase), peak current mode controlled circuits are subject to sub-harmonic oscillation.

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Application Information (continued)

Sub-harmonic oscillation is normally characterized by observing alternating wide and narrow duty cycles at the controller output. Adding an artificial ramp (slope compensation) to the current sense signal will eliminate this potential oscillation. Current mode control is also susceptible to noise and layout considerations. TI recommends placing the C_{Filter} and C_{slope} as close to the IC as possible to avoid any noise pickup and trace inductance. When the converter is operating at low duty cycles and light load, the primary current amplitude is small and is susceptible to noise. The artificial ramp, added to avoid sub-harmonic oscillations, provides additional benefits by improving the noise immunity of the converter.

Configuration and component selection for current mode control is recommended as follows: The current sense resistor is selected such that during overcurrent condition, the voltage across the current sense resistor is above the minimum CS threshold of 220 mV. TI recommends setting the impedances of R_{Filter} and C_{Filter} as seen from C_{slope} at relatively low values, so that the slope compensation is primarily dictated by R_{slope} and C_{slope} components. For example, if the filtering time (R_{Filter} and C_{Filter}) for leading edge noise is selected for 50 ns and if the value selected for R_{Filter} = 25 Ω, then

$$C_{Filter} = \frac{50 \times 10^{-9}}{3 \times 25\Omega} \tag{4}$$

Resulting in a value of C_{Filter} = 680 pF (approximated to a standard value). In general, the amount of slope compensation required to avoid sub-harmonic oscillation is equal to at least one-half the down-slope of the output inductor current, transformed to the primary. To mitigate subharmonic oscillation after one switching period, the slope compensation must be equal to one times the down slope of the filter inductor current transformed to primary. This is known as deadbeat control. For circuits where primary current is sensed, the amount of slope compensation for dead-beat control can be calculated using Equation 5.

$$\text{Slope-Comp} = \frac{\text{Turns-Ratio} \times \text{Vout} \times R_{CS}}{F_{OSC} \times L_{filter}}$$

where

- Turns-Ratio is referred with respect to the primary. (5)

For example, for a 5-V output converter with a turns ratio between secondary and primary of 1:2, an oscillator frequency (F_{OSC}) of 250 kHz, a filter inductance of 4 µH (L_{Filter}) and a current sense resistor (R_{CS}) of 32 mΩ, slope compensation of 80 mV will suffice. The slope compensation *volts* that results from Equation 5 is the maximum voltage of the artificial ramp added linearly to the RAMP pin till the end of maximum switching period. For circuits where a current sense tramsformer is used for primary current sensing, the turns-ratio of the current sense transformer must be considered.

C_{slope} should be selected such that it can be fully discharged by the internal RAMP discharge FET. TI recommends capacitor values ranging from 100 pF to 1500 pF. The value must be small enough such that the capacitor can be discharged within the clock (CLK) pulse width each cycle.

R_{slope} can be selected using Equation 6.

$$R_{slope} = \frac{-1}{F_{OSC} \times C_{slope} \times \ln\left(1 - \frac{\text{Slope-Comp}}{V_{REF}}\right)} - R_{filter} \tag{6}$$

For example, with a C_{slope} of 1500 pF, F_{OSC} of 250 kHz, reference voltage of 5 V (V_{REF}), slope compensation of 80 mV and R_{filter} = 25 Ω results in R_{slope} value of 165 kΩ.

8.1.4 VIN and VCC

The voltage applied to the VIN pin, which may be the same as the system voltage applied to the power transformer's primary (V_{PWR}), can vary in the range from 5.5 V to 75 V. The current into the VIN pin depends primarily on the gate charge provided by the output drivers, the switching frequency, and any external loads on the VCC and REF pins. TI recommends using the filter shown in Figure 20 to suppress transients that may occur at the input supply. This is particularly important when VIN is operated close to the maximum operating rating of the LM25037.

Application Information (continued)

When power is applied to VIN and the UVLO pin voltage is greater than 0.45 V, the VCC regulator is enabled and supplies current into an external capacitor connected to the VCC pin. When the voltage on the VCC pin reaches the regulation point of 7.7 V, the voltage reference (REF) is enabled. The reference regulation set point is 5 V. The outputs (OUTA and OUTB) are enabled when the two bias regulators reach their set point and the UVLO pin potential is greater than 1.25 V. In typical applications, an auxiliary transformer winding is connected through a diode to the VCC pin. This winding must raise the VCC voltage above 8.1 V to shut off the internal start-up regulator.

After the outputs are enabled and the external VCC supply voltage has begun supplying power to the IC, the current into the VIN pin drops below 1 mA. VIN should remain at a voltage equal to or greater than the VCC voltage to avoid reverse current through protection diodes.

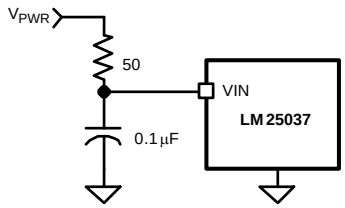

Figure 20. Input Transient Protection

8.1.5 Applications With >75-V Input

For applications where the system input voltage exceeds 75 V or the IC power dissipation is of concern, the LM25037 can be powered from an external start-up regulator as shown in Figure 21. In this configuration, the VIN and the VCC pins should be connected together. The voltage at the VCC and VIN pins must be at least 5.5 V (> Maximum VCC UV voltage) yet not exceed 14 V. An auxiliary winding can be used to reduce the power dissipation in the external regulator once the power converter is active. The NPN base-emitter reverses breakdown voltage, which can be as low as 5 V for some transistors, should be considered when selecting the transistor.

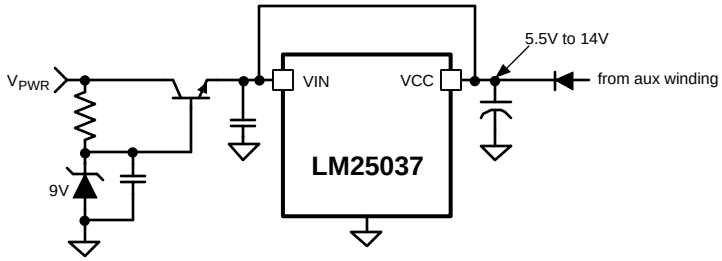

Figure 21. Start-Up Regulator for VPWR >75 V

8.1.6 Current Sense

The CS pin should receive an input signal representative of the transformer's primary current, either from a current sense transformer or from a resistor in series with the source of the OUTA and OUTB MOSFET switches. In both cases, the sensed current creates a voltage ramp across R1, and the R_F/C_F filter suppresses noise and transients as shown in Figure 22 and Figure 23. R1, R_F and C_F should be placed as close to the LM25037 as possible, and the ground connection from the current sense transformer, or R1, should be a dedicated track to the AGND pin. The current sense components must provide greater than 220 mV at the CS pin when an overcurrent condition exists.

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Application Information (continued)

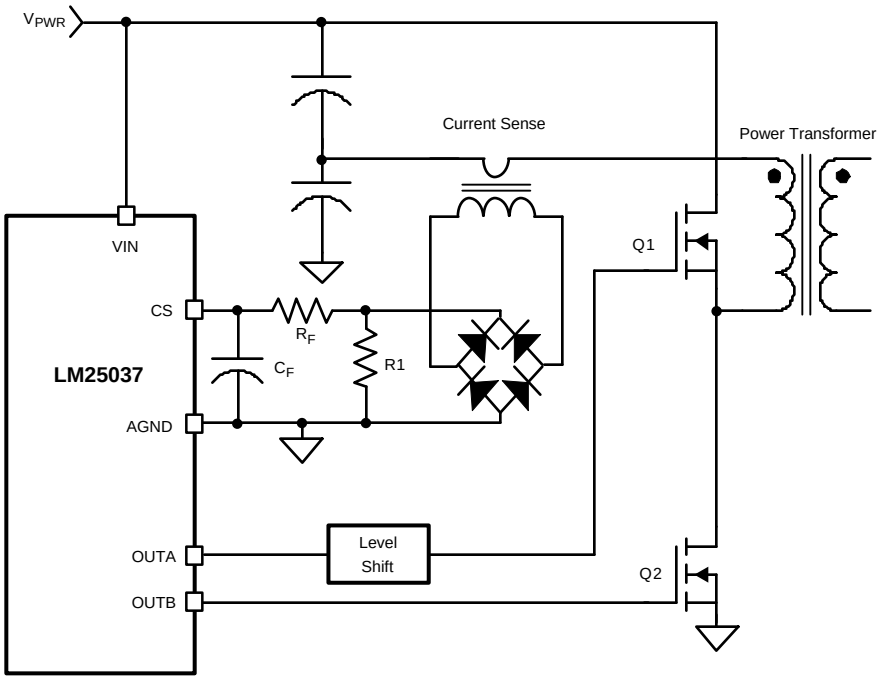

Figure 22. Current Sense Using Transformer

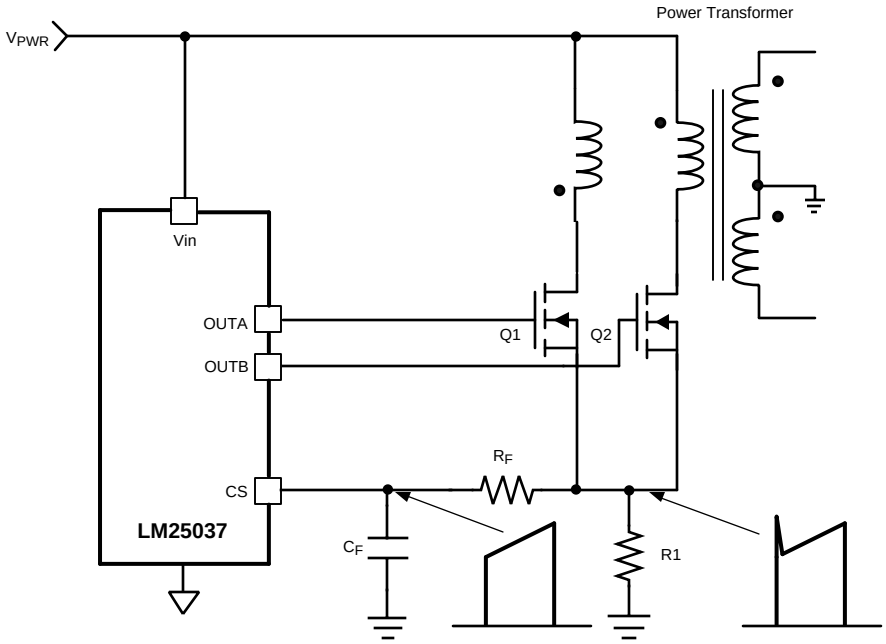

Figure 23. Current Sense Using Current Sense Resistor (R1)

Application Information (continued)

8.1.7 UVLO Divider Selection

A dedicated comparator connected to the UVLO pin detects an input undervoltage condition. When the UVLO pin voltage is less than 0.45 V, the LM25037 controller is in a low current shutdown mode. For a UVLO pin voltage greater than 0.45 V but less than 1.25 V, the controller is in standby mode with VCC and REF regulators active but no switching. Once the UVLO pin voltage is greater than 1.25 V, the controller is fully enabled. When the UVLO pin voltage rises above the 1.25-V threshold, an internal 22-µA current source as shown in Figure 24, is activated thus providing threshold hysteresis. The 22-µA current source is deactivated when the voltage at the UVLO pin falls below 1.25 V. Resistance values for R1 and R2 can be determined using Equation 7.

$$R_1 = \frac{\left(V_{HYS} - \frac{20 \times 10^{-3} \times V_{PWR}}{1.25}\right)}{22\ \mu A}$$

$$R_2 = \frac{1.25 \times R_1}{V_{PWR} - 1.25}$$

where

- V_{PWR} is the desired turnon voltage and V_{HYS} is the desired UVLO hysteresis at V_{PWR}. (7)

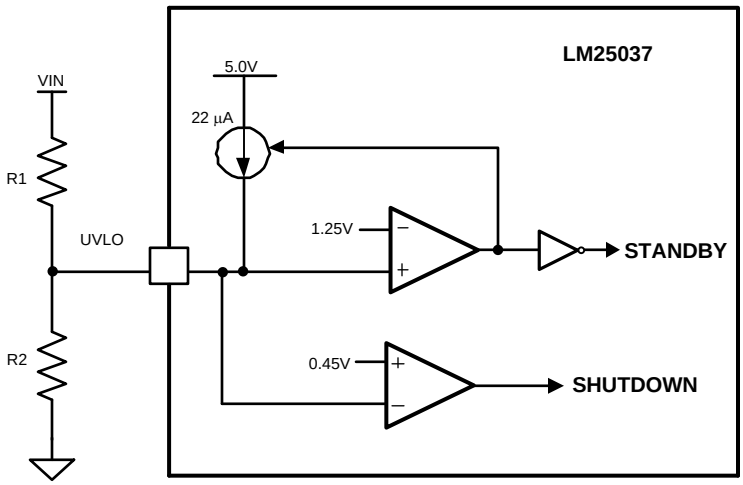

Figure 24. Basic UVLO Configuration

For example, if the LM25037 is to be enabled when V_{PWR} reaches 33 V, and disabled when V_{PWR} decreases to 30 V, R1 should be 113 kΩ, and R2 should be 4.42 kΩ. The voltage at the UVLO pin should not exceed 7 V at any time. Be sure to check both the power and voltage rating (0603 resistors can be rated as low as 50 V) for the selected R1 resistor. To maintain the UVLO threshold accuracy, TI recommends a resistor tolerance of 1% or better.

Remote control of the LM25037 operational modes can be accomplished with open-drain device(s) connected to the UVLO pin as shown in Figure 25.

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Application Information (continued)

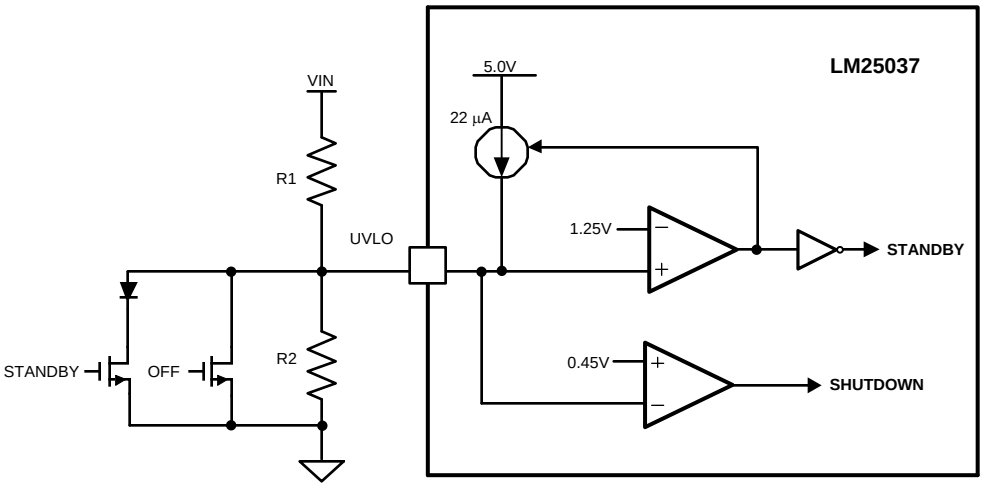

Figure 25. Remote Standby and Disable Control

8.1.8 Hiccup Mode Current Limit Restart (RES)

The basic operation of the hiccup mode current limit is described in the functional description. The delay time to the initiation of a hiccup cycle is programmed by the selection of the RES pin capacitor C_{RES} as illustrated in Figure 26.

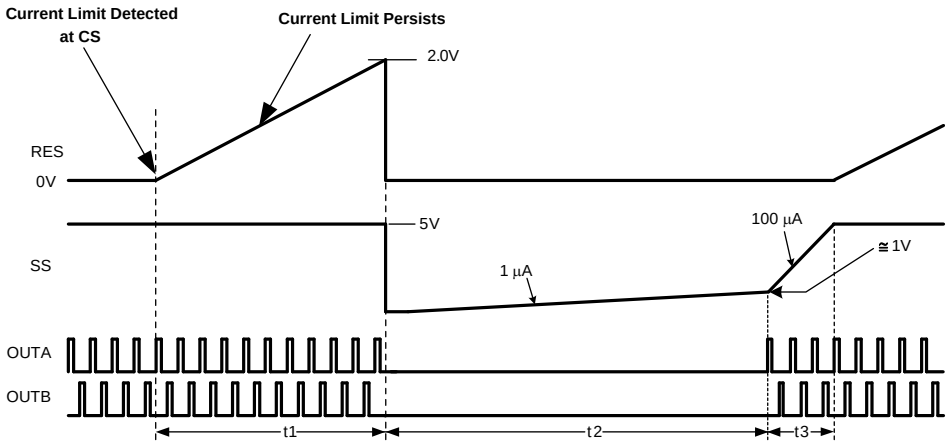

Figure 26. Hiccup Over-Load Restart Timing

In the case of continuous cycle-by-cycle current limit detection at the CS pin, the time required for C_{RES} to reach the 2-V hiccup mode threshold is given by Equation 8:

$$t1 = \frac{C_{RES} \times 2.0V}{18\ \mu A} = 111k \times C_{RES} \tag{8}$$

For example, if C_{RES} = 0.01 µF the time t1 is approximately 2 ms. The cool down time, t2 is set by the soft-start capacitor (C_{SS}) and the internal 1 µA SS current source, and is equal to Equation 9:

$$t2 = \frac{C_{SS} \times 1V}{1\ \mu A} = 1M \times C_{SS} \tag{9}$$

If C_{SS} = 0.01 µF, t2 is ≅10 ms.

The soft-start time t3 is set by the internal 100-µA current source, and is equal to Equation 10:

Application Information (continued)

$$t3 = \frac{C_{SS} \times 4V}{100\ \mu A} = 40k \times C_{SS} \tag{10}$$

If C_{SS} = 0.01 µF, t3 is ≅ 400 µs.

The time t2 provides a periodic cool-down time for the power converter in the event of a sustained overload or short circuit. This off time results in lower average input current and lower power dissipation within the power components. TI recommends that the ratio of t2 / (t1 + t3) be in the range of 5 to 10 to take advantage of this feature.

If the application requires no delay from the first detection of a current limit condition to the onset of the hiccup mode (t1 = 0), the RES pin can be left open (no external capacitor). If it is desired to disable the hiccup mode entirely, the RES pin should be connected to ground (AGND).

8.2 Typical Application

Figure 27 shows an example of an LM25037-controlled 50-W push-pull converter. The converter provides a single regulated 5-V output at 10 A, from an input voltage range of 16 V to 32 V. The converter is configured for current-mode control with external slope compensation. An auxiliary winding on the output filter inductor is used to supply the VCC voltage externally – the VCC level is chosen higher than the internal regulator level, to reduce the power dissipation in the LM25037 IC.

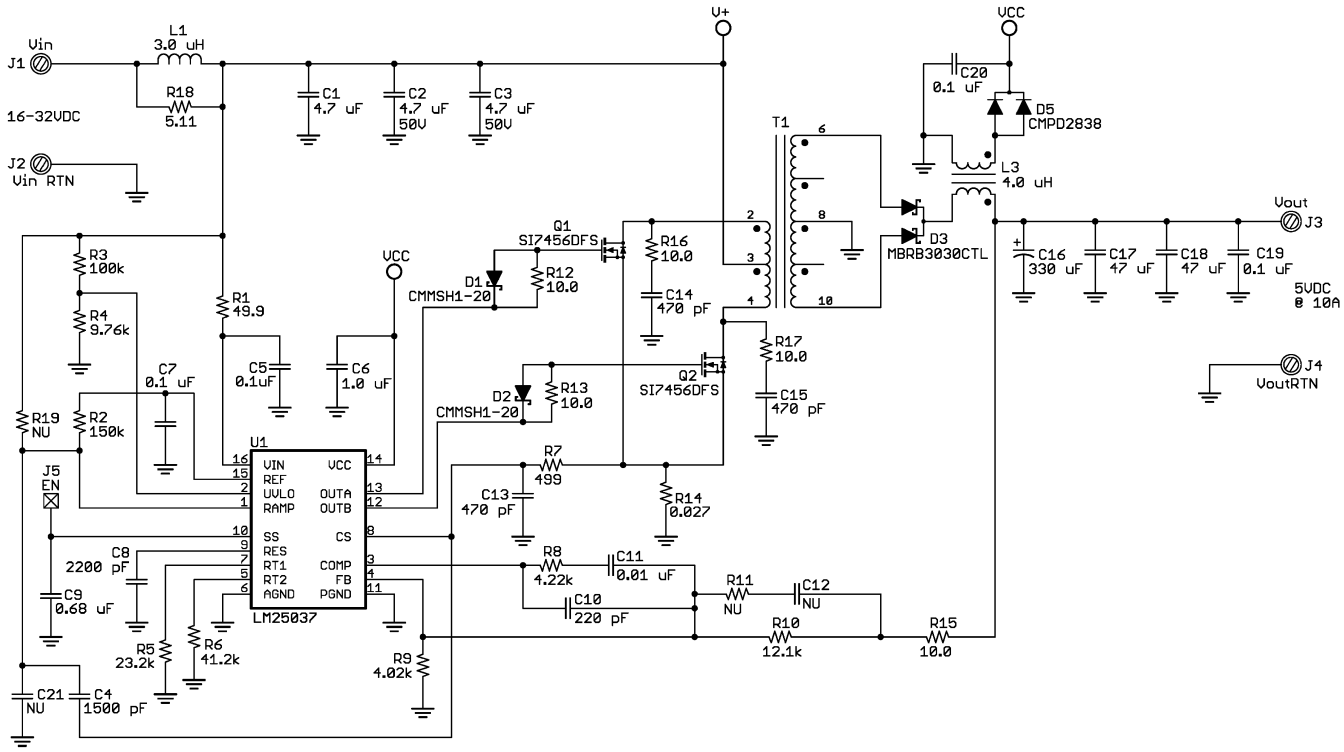

Figure 27. Schematic

8.2.1 Design Requirements

The LM25037 evaluation board is designed to provide the design engineer with a fully functional power converter based on push-pull topology to evaluate the LM25037 controller. Table 1 lists the performance of the evaluation board.

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Typical Application (continued)

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
Input Voltage Range, V_{IN}	16 V to 32 V
UVLO On/Off Levels	14 V On (rising)/11 V Off (falling)
Output Voltage V_{OUT}	5 V
Output Current I_{OUT}	10 A
Oscillator frequency (2x Fsw per phase)	250 kHz
Switching frequency Fsw (per phase)	125 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Oscillator Frequency and Maximum Duty Cycle

The LM25037 oscillator frequency will be twice the switching frequency of each switch in the push-pull power stage, that is, $F_{osc} = 2 \times F_{sw}$.

First of all the dead-time resistor value RT2 is calculated. The recommended range of dead-time is 50 ns to 250 ns. A value of 200 ns is chosen, which will set a maximum duty cycle of approximately 95%. From Equation 11, the required value of resistor on the RT2 pin (R6 in Figure 27) is calculated using Equation 11.

$$R_{RT2} = \frac{Dead_time}{5.0 \times 10^{-12}} = \frac{200 \times 10^{-9}}{5.0 \times 10^{-12}} = 40\ k\Omega \tag{11}$$

The E96 value of 41.2 kΩ is used.

Next, knowing the resistor value on RT2 pin, the required resistor value for the RT1 pin (R5 in Figure 27) can be calculated from Equation 12.

$$R_{RT1} = \frac{\left(\frac{1}{F_{osc}}\right) - Dead_time}{0.162 \times 10^{-9}} = \frac{\left(\frac{1}{250 \times 10^{3}}\right) - 200 \times 10^{-9}}{0.162 \times 10^{-9}} = 23.5\ k\Omega \tag{12}$$

8.2.2.2 Power Stage Design

Referring to the schematic in Figure 27, the push-pull power stage primarily consists of input capacitors C1, C2, and C3, power MOSFETs Q1 and Q2, power transformer T1, output rectifier D3, and output filter L3 and C16, C17, C18. The push-pull transformer has two out-of-phase primary windings, centre-tapped, and two out-of-phase secondary windings, also centre-tapped.

The centre-tap of the primary is connected to the DC input voltage, V_{IN}. The other end of each primary winding connects to Q1 and Q2 respectively. The push-pull controller alternately drives Q1 and Q2 180° out of phase, so that the voltage across each winding is approximately equal to Vin when its respective switch (Q1 or Q2) is turned on.

On the secondary side, the voltage across each secondary winding will be the same as V_{in}, scaled by the transformer turns ratio N_s/N_p. Double-diode D3 alternately rectifies the positive voltage across each secondary winding, to generate a full-wave rectified positive-voltage pulse-train at D3 cathode. This pulse train is then filtered to DC by output filter L3 and C16/C17/C18.

The LM25037 modulates the duty cycle of the pulses to regulate the output voltage to the required level. The duty cycle is adjusted with input line voltage to regulate V_{OUT}:

$$D = \frac{V_{out} \times N_p}{V_{in} \times N_s} \tag{13}$$

Choosing a transformer with turns ratio $N_p/N_s = 2$, maximum duty cycle will occur at minimum operating $V_{IN,}$ which will be approximately 11 V (UVLO turnoff point):

$$D = \frac{V_{out} \times N_p}{V_{in} \times N_s} = \frac{5 \times 2}{11 \times 1} = 91\% \tag{14}$$

Thus there is sufficient margin to the oscillator 95% D_{max} setting (set by choice of RT2 resistor).

Knowing the duty cycle (D), F_{osc} frequency and turns ratio, the output inductor (L_{OUT}) peak-to-peak ripple current in Continuous Conduction Mode (CCM) can be estimated. At minimum V_{IN} of 16 V:

$$\Delta I_{pp} = \frac{\left(V_{in} \times \frac{N_s}{N_p} - V_{out}\right)}{L_{out}} \times \frac{D}{F_{osc}} = \frac{\left(V_{out} - \frac{V_{out}^2}{V_{in}} \times \frac{N_p}{N_s}\right)}{L_{out} \times F_{osc}} = \frac{\left(5 - \frac{5^2}{16} \times \frac{2}{1}\right)}{4\mu \times 250\ k} = 1.88\ A_{pp} \tag{15}$$

And at a maximum V_{IN} of 32 V:

$$\Delta I_{pp} = \frac{\left(V_{out} - \frac{V_{out}^2}{V_{in}} \times \frac{N_p}{N_s}\right)}{L_{out} \times F_{osc}} = \frac{\left(5 - \frac{5^2}{32} \times \frac{2}{1}\right)}{4\mu \times 250\ k} = 3.44\ A_{pp} \tag{16}$$

8.2.2.3 UVLO Setting

To ensure start-up at the required minimum system input voltage of 14 V, with the 3 V of hysteresis to the desired turnoff level, the UVLO divider resistors R3 and R4 are calculated as follows using Equation 17:

$$R3 = \frac{\left(V_{hys} - \frac{20 \times 10^{-3} \times V_{on}}{1.25}\right)}{22\ \mu A} = \frac{\left(3 - \frac{20 \times 10^{-3} \times 14}{1.25}\right)}{22\ \mu A} = 126.2\ k\Omega \tag{17}$$

This is rounded down to a convenient value of 100 kΩ. This reduces the effective hysteresis to approximately 2.5 V.

To set the turnon level to 14 V, calculate the lower UVLO divider resistor:

$$R4 = \frac{1.25 \times R3}{V_{on} - 1.25} = \frac{1.25 \times 100k}{14 - 1.25} = 9.8\ k\Omega \tag{18}$$

The nearest E96 value of 9.76 kΩ is used.

8.2.2.4 VIN, VCC, Start-Up

To reduce the power dissipation in the internal start-up regulator on the VIN pin, a separate external VCC supply is used. This is derived from the auxiliary winding on the output filter inductor L3. The auxiliary to main inductor winding turns ratio is 2:1, so when V_{OUT} is regulated at 5 V, the auxiliary VCC will be approximately 10 V. This is sufficiently greater than the maximum internal VCC regulator level of 8 V to back-bias the internal regulator after start-up.

8.2.2.5 Current Sense Resistor

The CS pin is used to implement cycle-by-cycle current limit, if the peak current exceeds the internal threshold – 255 mV typical, 220 mV minimum. This limit is used to choose the value of the current-sense resistor R14.

Knowing the maximum output inductor peak-peak ripple current in CCM, and the turns ratio the transformer (Ns/Np), the current-limit point can be set as required. Given that the full load output current is 10 A, the current limit target is set at 150%, or 15 A. Thus the required value for R14 may be calculated – it must generate a voltage at the CS pin no higher than the internal cycle-by-cycle limit of minimally 0.22 V at the current limit level at the output.

$$R14 = \frac{0.22\ V}{\left(I_{lim} + \frac{\Delta I}{2}\right) \times \frac{N_s}{N_p}} = \frac{0.22}{\left(15 + \frac{3.44}{2}\right) \times \frac{1}{2}} = 0.026\ \Omega \tag{19}$$

The nearest E96 value of 27 mΩ is chosen for R14. A small filter R7, C13 can be optionally added to filter the leading-edge current spike in the current-sense waveform, if the internal 65-ns leading-edge blanking time is not sufficient. In this case, a 499-Ω resistor and 470-pF capacitor are used, for approximately 235-ns filter time constant.

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8.2.2.6 Current-Mode Control

Push-pull power stages always use peak current-mode control rather than voltage-mode, to keep the transformer balanced, and avoid stair-case saturation. Ideally, the push-pull transformer flux should return to zero at the end of each switching cycle. However, due to small imbalances between each phase of the primary (for example, slightly different Rdson between primary FETs Q1 and Q2), the peak current can be slightly different in each phase. This causes the transformer flux to become slightly biased away from zero after a complete switching. After several switching cycles, this small net imbalance per cycle can accumulate or stair-case to the point that the transformer starts to saturate in one or other direction.

By using current-mode control and connecting the sources of both FETs Q1 and Q2 to the same current sense resistor R14, the LM25037 controller ensures that the same exact peak current flows in each phase of the primary. This means that the transformer has identical peak flux swing in each direction, so it always returns to zero at the end of each switching cycle.

The CS pin ramp is capacitively-coupled to the RAMP pin (input to the internal PWM comparator) using C4, where it is then also summed with the slope compensation ramp (see *Slope Compensation Ramp*).

8.2.2.7 Slope Compensation Ramp

Because current-mode control is being used, slope compensation is required to prevent instability and sub-harmonic oscillation at power stage duty cycles above 50%. For the push-pull topology, this means slope compensation is required when the switch duty cycle is above 25% of the overall switching period. For stability, the slope compensation ramp should be at least half the output inductor current downslope, or more ideally equal to it.

The output inductor downslope, scaled by the transformer turns ratio and current-sense resistor R14, can be expressed as:

$$\frac{dv_{cs}}{dt} = \frac{V_{out}}{L_{out}} \times \frac{N_s}{N_p} \times R14 = \frac{5}{4\mu} \times \frac{1}{2} \times 0.027 = 16.9\ mV / \mu s \tag{20}$$

Resistor R2 and capacitor C4 are used to generate the slope compensation ramp and sum it with the current-sense signal at the CS pin. The RC time constant should be quite large compared to the oscillator period to make the ramp reasonably linear. Assuming that RC >> T_{osc}, the slope of the ramp is approximately:

$$\frac{dv_{ramp}}{dt} = \frac{V_{ref}}{R2 \times C4} \tag{21}$$

Choosing C4 = 1.5 nF, the value of R2 can be calculated using Equation 22 to achieve the required slope.

$$R2 = \frac{V_{ref}}{\frac{dv_{cs}}{dt} \times C4} = \frac{5\ V}{16.9\ mV / \mu s \times 1.5\ nF} = 197\ k\Omega \tag{22}$$

A lower value of 150 kΩ is chosen for R2 to allow for tolerances and to ensure a sufficient slope compensation ramp under all conditions.

8.2.2.8 Soft-start

The soft-start delay to commencement of first PWM switching can be calculated using Equation 23.

$$t_{ss_delay} = \frac{1.0\ V \times C9}{100\ \mu A} = \frac{1.0 \times 0.68\ \mu F}{100\ \mu A} = 6.8\ ms \tag{23}$$

Thereafter, the soft-start ramp time depends on the power stage design and the operating conditions (input voltage and output load).

8.2.2.9 Overload Timer

With a timing capacitor C8 of 2.2 nF on the RES pin, the hiccup-mode timing and duty cycle can be calculated for a sustained overcurrent condition.

Hiccup-mode current-limit persist time t_1:

$$t_1 = \frac{2.0\ V \times C9}{18\ \mu A} = \frac{2.0 \times 2.2\ nF}{18\ \mu A} = 0.244\ ms \tag{24}$$

Hiccup-mode cool-down off-time t2:

$$t_2 = \frac{1.0\ V \times C8}{1\ \mu A} = \frac{1.0 \times 680\ nF}{1\ \mu A} = 680\ ms \tag{25}$$

Thus the hiccup-mode duty cycle is approximately:

$$d_{hiccup} = \frac{t_1}{t_1 + t_2 + t_{ss}} = \frac{0.244}{0.244 + 680 + 6.8} = 0.036\% \tag{26}$$

8.2.2.10 Output Voltage Feedback

In this example, the output of the DC-DC converter is non-isolated from the input, so resistor divider R15, R10, R9 are used to scale V_{OUT} down to the required 1.25-V reference level at the FB pin.

Because current-mode control removes the pole due to the output inductor, the loop compensation components R8, C10, C11 are chosen to implement a simpler Type II compensator. For further details about control loop design and Type II compensator design, see application notes *Seminar 300 Topic 2 - Apdx A - Error Amplifier and Compensation Network Design* (SLUP069) or *Seminar 1400 Topic 5 Designing Stable Control Loops* (SLUP173).

8.2.3 Application Curves

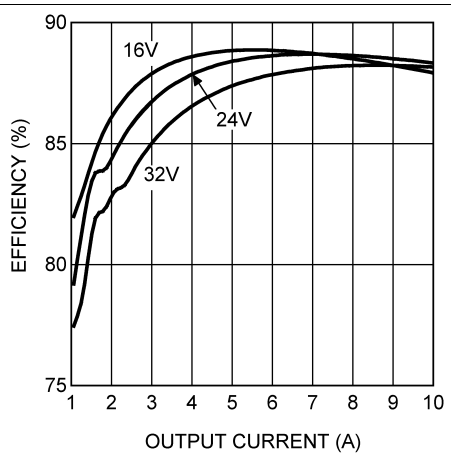
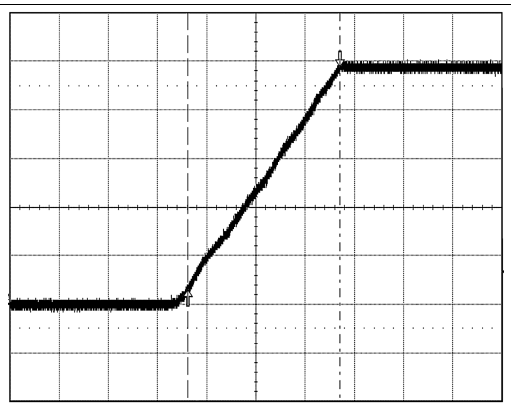


Figure 28. Efficiency vs Output Current and VIN



Conditions:

Input Voltage = 24 VDC | Output Current = 10 A

Trace:

Output Voltage, V/div = 1 V | Horizontal Resolution = 0.5 ms/div

Figure 29. Soft Start

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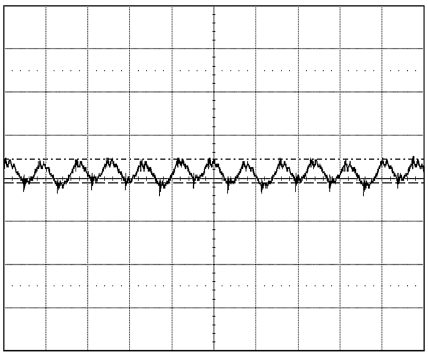
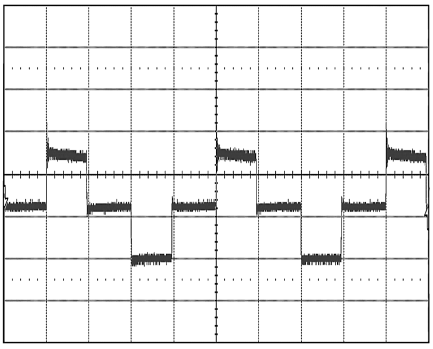


Conditions:
Input Voltage = 24 VDC
Output Current = 10 A
Bandwidth Limit = 20 MHz
Trace:
Output Ripple, V/div = 50 mV
Horizontal Resolution = 5 µs/div

Figure 30. Output Ripple

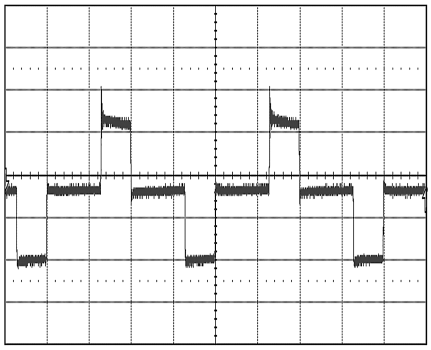
Conditions:
Input Voltage = 24 VDC
Output Current = 5 to 10 A
Bandwidth Limit = 20 MHz
Traces:
Bottom Trace: Output current
A/div = 5 A
Top Trace: Output voltage response
V/div = 100 mV
Horizontal Resolution = 200 µs/div

Figure 31. Transient Response



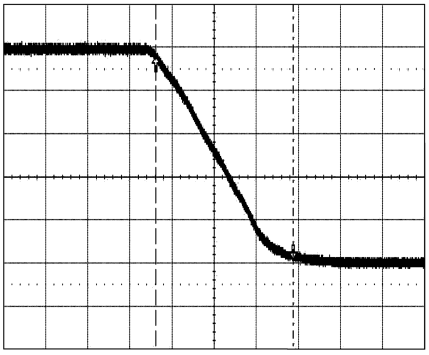
Conditions:
Input Voltage = 24 VDC
Output Current = 5 A
Trace:
Q1 drain-to-source voltage, V/div = 20 V
Horizontal Resolution = 2 µs/div

Figure 32. Drain Waveform of Q1 at 24 V



Conditions:
Input Voltage = 32 VDC
Output Current = 5 A
Trace:
Q1 drain to source voltage, V/div = 20 V
Horizontal Resolution = 2 µs/div

Figure 33. Drain Waveform of Q1 at 32 V



Conditions: Input Voltage = 24 VDC
Trace: Output Voltage, V/div = 1 V
Horizontal Resolution = 0.5 ms/div

Figure 34. Soft Stop

9 Power Supply Recommendations

The VCC pin requires a local decoupling capacitor that is connected to GND. This capacitor ensures stability of the internal regulator from the VIN pin. The decoupling capacitor also provides the current pulses to drive the gates of the external MOSFETs through the driver output (OUTA and OUTB) pins. Place the decoupling capacitor close to the VCC and PGND pins, and track it directly to those pins.

The two ground pins (PGND and AGND) must be connected together with a short direct PCB connection.

10 Layout

10.1 Layout Guidelines

The LM25037 Current Sense and PWM comparators are very fast, and respond to short duration noise pulses. The components at the CS, COMP, SS, UVLO, RT2 and the RT1 pins should be as physically close as possible to the IC, thereby minimizing noise pickup on the PC board trace inductances.

Layout considerations are critical for the current sense filter. If a current sense transformer is used, both leads of the transformer secondary should be routed to the sense filter components and to the IC pins. The ground side of the transformer should be connected through a dedicated PC board trace to the AGND pin, rather than through the ground plane.

If the current sense circuit employs a sense resistor in the drive transistor source, low inductance resistors should be used. In this case, all the noise sensitive, low-current ground trace should be connected in common near the IC, and then a single connection made to the power ground (sense resistor ground point).

While employing current mode control, RAMP pin capacitor and CS pin capacitor must be placed close to the IC. Also, a short direct trace should be employed to connect RAMP capacitor to the CS pin.

The gate drive outputs of the LM25037 should have short, direct paths to the power MOSFETs to minimize inductance in the PC board The two ground pins (AGND, PGND) must be connected together with a short, direct connection, to avoid jitter due to relative ground bounce.

If the internal dissipation of the LM25037 produces high junction temperatures during normal operation, the use of multiple vias under the IC to a ground plane can help conduct heat away from the IC. Judicious positioning of the PC board within the end product, along with use of any available air flow (forced or natural convection) will help reduce the junction temperatures. If using forced air cooling, avoid placing the LM25037 in the airflow shadow of tall components, such as input capacitors.

10.2 Layout Example

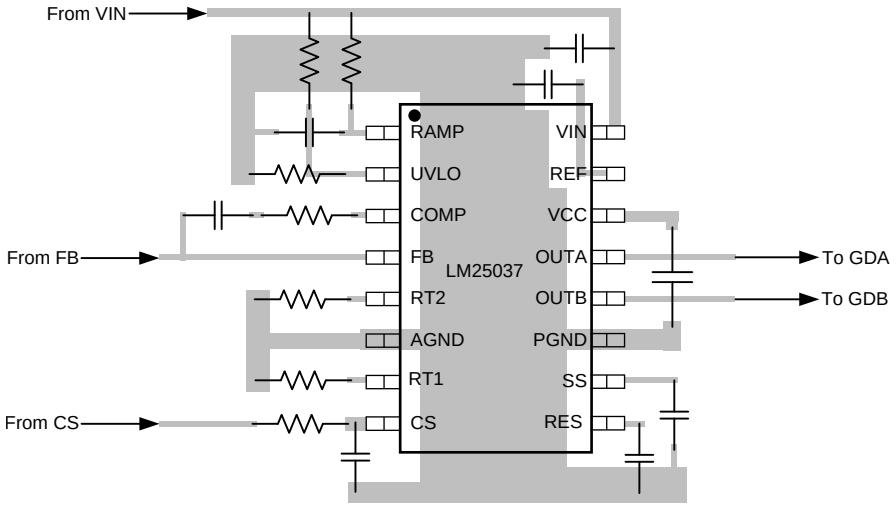


Figure 35. Layout Recommendation

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11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *Seminar 300 Topic 2 - Apdx A - Error Amplifier and Compensation Network Design* (SLUP069)
- *Seminar 1400 Topic 5 Designing Stable Control Loops* (SLUP173)
- User Guide, *AN-1861 LM25037 Evaluation Board* (SNVA352)

11.2 Related Links

The following table lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM25037	Click here	Click here	Click here	Click here	Click here
LM25037-Q1	Click here	Click here	Click here	Click here	Click here

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM25037MTX/NOPB	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L25037 MT
LM25037MTX/NOPB.A	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L25037 MT
LM25037MTX/NOPB.B	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L25037 MT
LM25037QMTX/NOPB	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	M25037 MT
LM25037QMTX/NOPB.A	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	M25037 MT
LM25037QMTX/NOPB.B	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	M25037 MT

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LM25037, LM25037-Q1 :

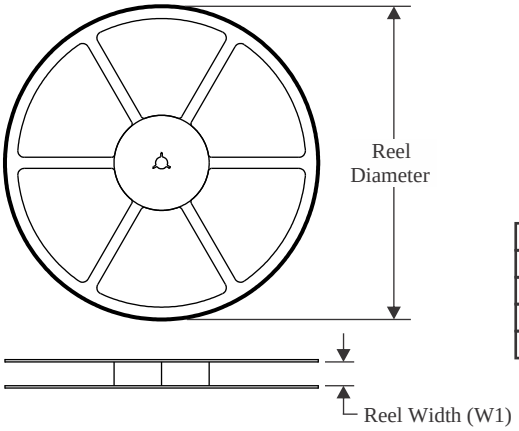
- Catalog : LM25037
- Automotive : LM25037-Q1

NOTE: Qualified Version Definitions:

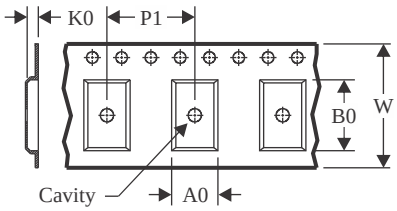
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

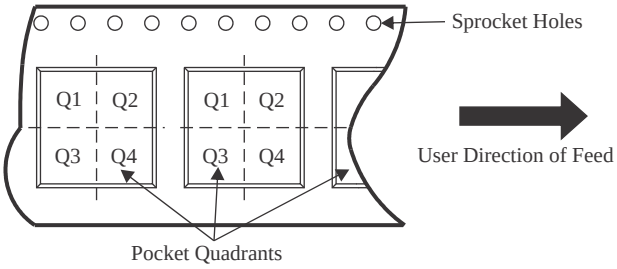


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

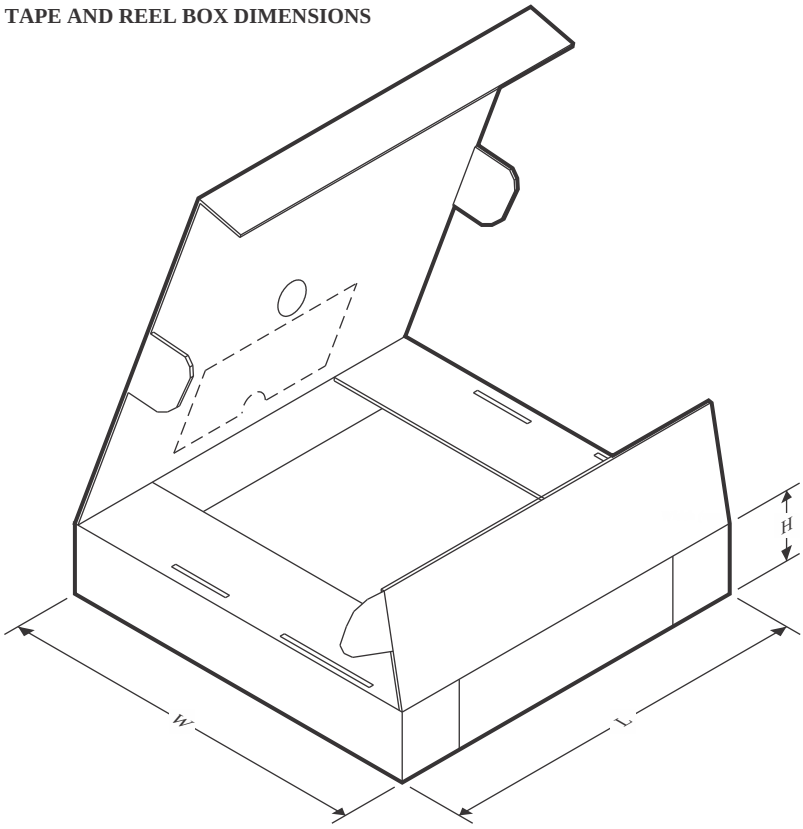
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

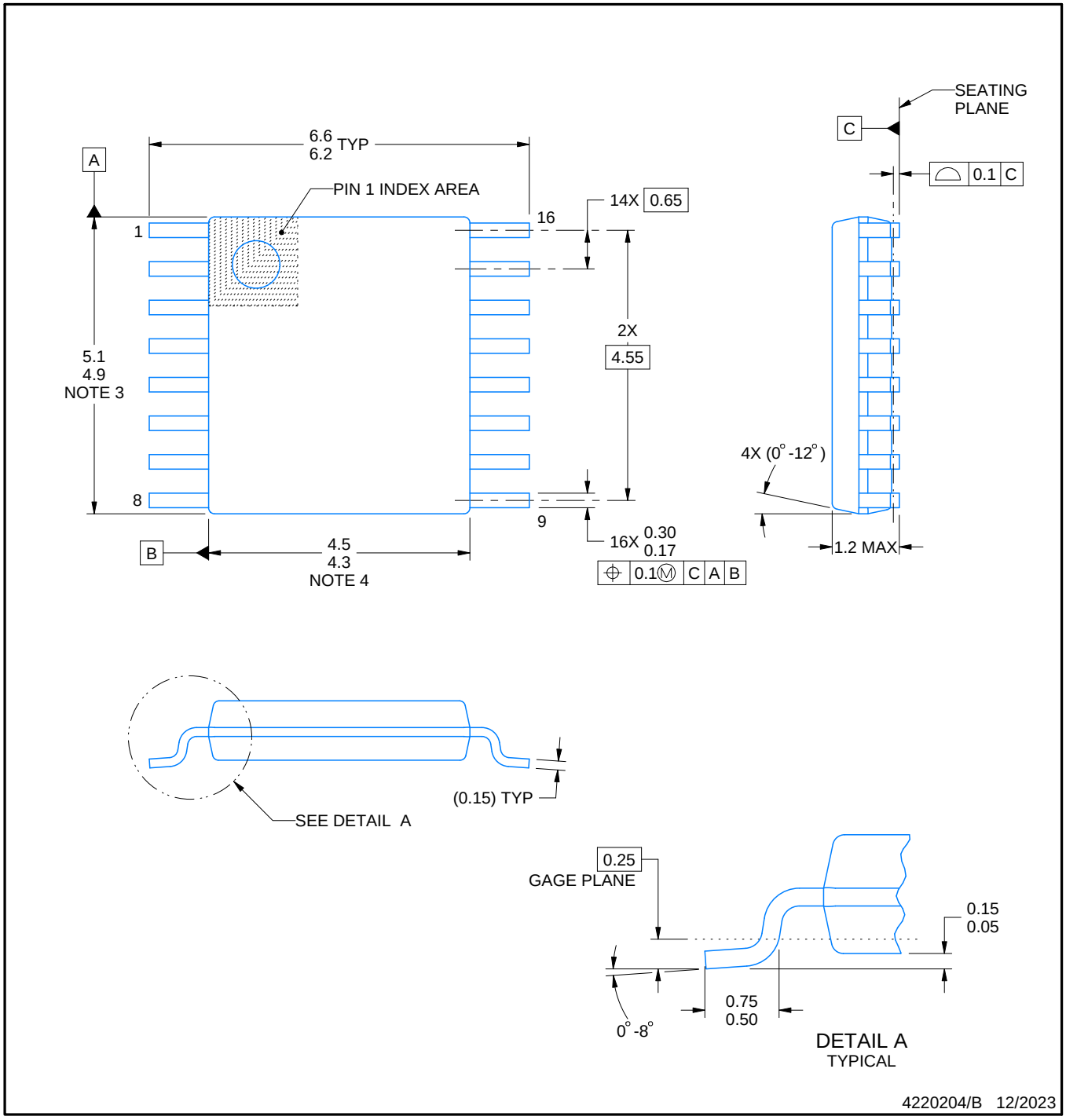
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM25037MTX/NOPB	TSSOP	PW	16	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM25037QMTX/NOPB	TSSOP	PW	16	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



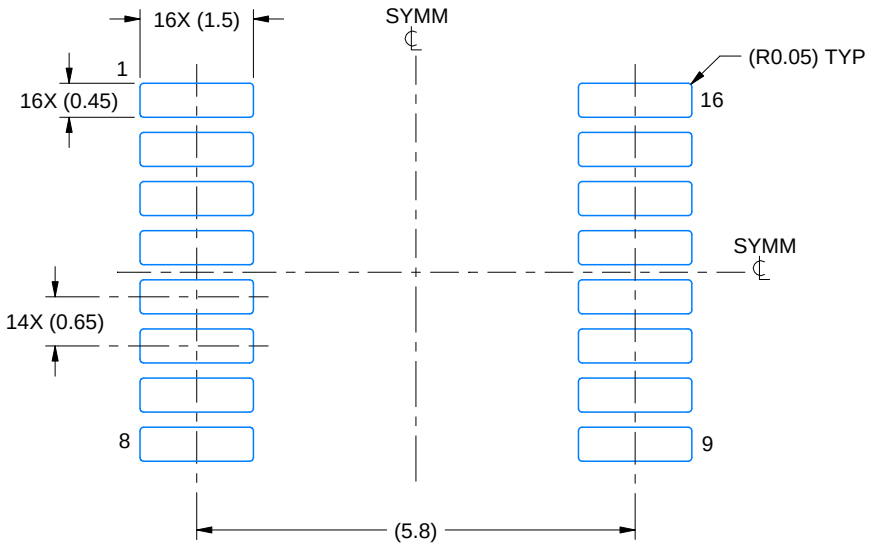
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM25037MTX/NOPB	TSSOP	PW	16	2500	367.0	367.0	35.0
LM25037QMTX/NOPB	TSSOP	PW	16	2500	367.0	367.0	35.0



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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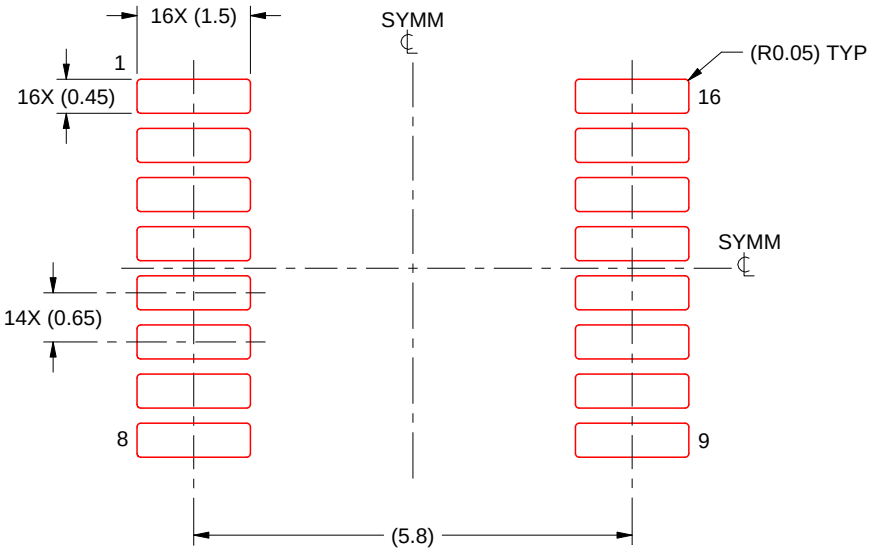
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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