LM2578A/LM3578A Switching Regulator

Check for Samples: LM2578A, LM3578A

FEATURES

- **Inverting and Non-Inverting Feedback Inputs**
- **1.0V Reference at Inputs**
- **Operates from Supply Voltages of 2V to 40V**
- **Output Current up to 750 mA, Saturation Less than 0.9V**
- **Current Limit and Thermal Shut Down**
- **Duty Cycle up to 90%**

APPLICATIONS

- **Switching Regulators in Buck, Boost, Inverting, and Single-Ended Transformer Configurations**
- **Motor Speed Control**
- **Lamp Flasher**

DESCRIPTION

The LM2578A is a switching regulator which can easily be set up for such DC-to-DC voltage conversion circuits as the buck, boost, and inverting configurations. The LM2578A features a unique comparator input stage which not only has separate pins for both the inverting and non-inverting inputs, but also provides an internal 1.0V reference to each input, thereby simplifying circuit design and p.c. board layout. The output can switch up to 750 mA and has output pins for its collector and emitter to promote design flexibility. An external current limit terminal may be referenced to either the ground or the V_{in} terminal, depending upon the application. In addition, the LM2578A has an on board oscillator, which sets the switching frequency with a single external capacitor from <1 Hz to 100 kHz (typical).

The LM2578A is an improved version of the LM2578, offering higher maximum ratings for the total supply voltage and output transistor emitter and collector voltages.

Connection Diagram

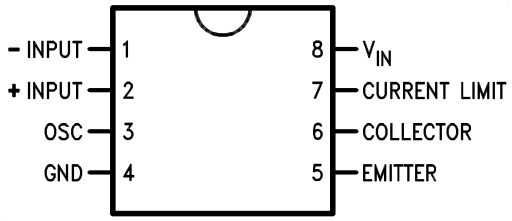
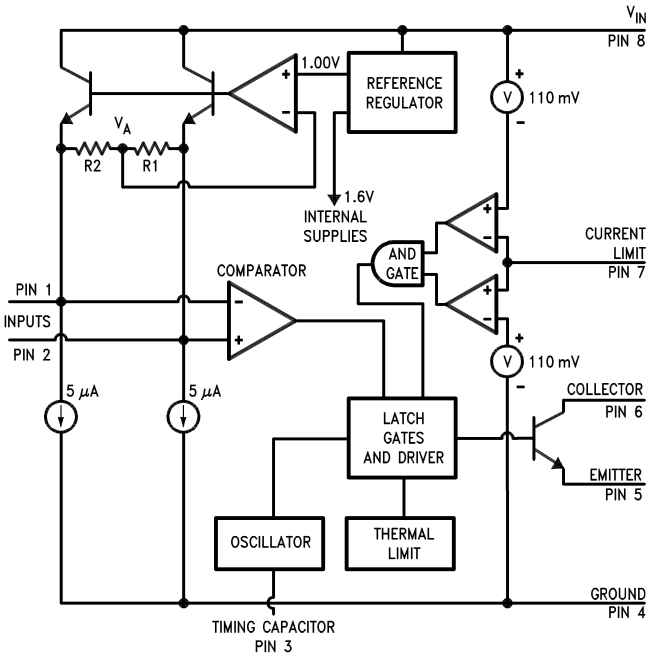


Figure 1. PDIP/SOIC Package
See Package Number D0008A or P0008E

Functional Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

Total Supply Voltage		50V
Collector Output to Ground		−0.3V to +50V
Emitter Output to Ground (3)		−1V to +50V
Power Dissipation (4)		Internally limited
Output Current		750 mA
Storage Temperature		−65°C to +150°C
Lead Temperature	(soldering, 10 seconds)	260°C
Maximum Junction Temperature		150°C
ESD Tolerance (5)		2 kV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) For $T_J \geq 100°C$, the Emitter pin voltage should not be driven more than 0.6V below ground (see Application Information).
(4) At elevated temperatures, devices must be derated based on package thermal resistance. The device in the 8-pin DIP must be derated at 95°C/W, junction to ambient. The device in the SOIC package must be derated at 150°C/W, junction-to-ambient.
(5) Human body model, 1.5 kΩ in series with 100 pF.

Operating Ratings

Ambient Temperature Range	LM2578A	$-40°C \leq T_A \leq +85°C$
	LM3578A	$0°C \leq T_A \leq +70°C$
Junction Temperature Range	LM2578A	$-40°C \leq T_J \leq +125°C$
	LM3578A	$0°C \leq T_J \leq +125°C$

Electrical Characteristics

These specifications apply for 2V ≤ V_{IN} ≤ 40V (2.2V ≤ V_{IN} ≤ 40V for T_J ≤ −25°C), timing capacitor C_T = 3900 pF, and 25% ≤ duty cycle ≤ 75%, unless otherwise specified. Values in standard typeface are for T_J = 25°C; values in **boldface type** apply for operation over the specified operating junction temperature range.

Symbol	Parameter	Conditions	Typical (1)	LM2578A/ LM3578A Limit (2)	Units
OSCILLATOR					
f_{OSC}	Frequency		20		kHz
				24	kHz (max)
				16	kHz (min)
$\Delta f_{OSC}/\Delta T$	Frequency Drift with Temperature		**−0.13**		%/°C
	Amplitude		550		mV_{p-p}
REFERENCE/COMPARATOR (3)					
V_R	Input Reference Voltage	$I_1 = I_2$ = 0 mA and	1.0		V
		$I_1 = I_2$ = 1 mA ±1% (4)		1.050/**1.070**	V (max)
				0.950/**0.930**	V (min)
$\Delta V_R/\Delta V_{IN}$	Input Reference Voltage Line Regulation	$I_1 = I_2$ = 0 mA and	0.003		%/V
		$I_1 = I_2$ = 1 mA ±1% (4)		0.01/**0.02**	%/V (max)
I_{INV}	Inverting Input Current	$I_1 = I_2$ = 0 mA, duty cycle = 25%	0.5		µA
	Level Shift Accuracy	Level Shift Current = 1 mA	1.0		%
				10/**13**	% (max)
$\Delta V_R/\Delta t$	Input Reference Voltage Long Term Stability		100		ppm/1000h
OUTPUT					
V_C (sat)	Collector Saturation Voltage	I_C = 750 mA pulsed, Emitter grounded	0.7		V
				0.90/**1.2**	V (max)
V_E (sat)	Emitter Saturation Voltage	I_O = 80 mA pulsed,	1.4		V
		$V_{IN} = V_C$ = 40V		1.7/**2.0**	V (max)
I_{CES}	Collector Leakage Current	$V_{IN} = V_{CE}$ = 40V, Emitter grounded, Output OFF	0.1		µA
				200/**250**	µA (max)
$BV_{CEO(SUS)}$	Collector-Emitter Sustaining Voltage	I_{SUST} = 0.2A (pulsed), V_{IN} = 0	60		V
				50	V (min)
CURRENT LIMIT					
V_{CL}	Sense Voltage Shutdown Level	Referred to V_{IN} or Ground	110		mV
		See (5)		80	mV (min)
				160	mV (max)
$\Delta V_{CL}/\Delta T$	Sense Voltage Temperature Drift		**0.3**		%/°C
I_{CL}	Sense Bias Current	Referred to V_{IN}	4.0		µA
		Referred to ground	0.4		µA

(1) Typical values are for T_J = 25°C and represent the most likely parametric norm.
(2) All limits specified at room temperature (standard type face) and at temperature extremes (bold type face). Room temperature limits are 100% production tested. Limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate AOQL.
(3) Input terminals are protected from accidental shorts to ground but if external voltages higher than the reference voltage are applied, excessive current will flow and should be limited to less than 5 mA.
(4) I_1 and I_2 are the external sink currents at the inputs (refer to Test Circuit).
(5) Connection of a 10 kΩ resistor from pin 1 to pin 4 will drive the duty cycle to its maximum, typically 90%. Applying the minimum Current Limit Sense Voltage to pin 7 will not reduce the duty cycle to less than 50%. Applying the maximum Current Limit Sense Voltage to pin 7 is certain to reduce the duty cycle below 50%. Increasing this voltage by 15 mV may be required to reduce the duty cycle to 0%, when the Collector output swing is 40V or greater (see Ground-Referred Current Limit Sense Voltage typical curve).

Electrical Characteristics (continued)

These specifications apply for 2V ≤ V_{IN} ≤ 40V (2.2V ≤ V_{IN} ≤ 40V for T_J ≤ −25°C), timing capacitor C_T = 3900 pF, and 25% ≤ duty cycle ≤ 75%, unless otherwise specified. Values in standard typeface are for T_J = 25°C; values in **boldface type** apply for operation over the specified operating junction temperature range.

Symbol	Parameter	Conditions	Typical (1)	LM2578A/ LM3578A Limit (2)	Units
DEVICE POWER CONSUMPTION					
I_S	Supply Current	Output OFF, V_E = 0V	2.0	3.5/**4.0**	mA mA (max)
		Output ON, I_C = 750 mA pulsed, V_E = 0V	14		mA

Typical Performance Characteristics

Oscillator Frequency Change with Temperature

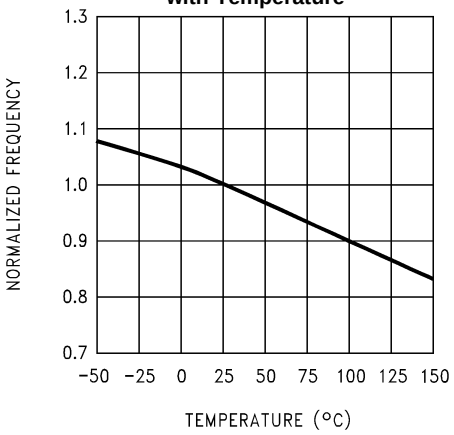


Figure 2.

Oscillator Voltage Swing

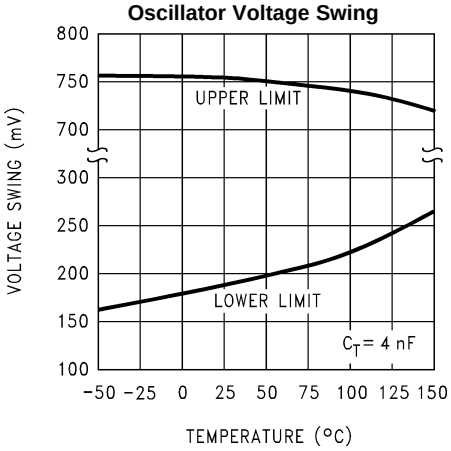


Figure 3.

Input Reference Voltage Drift with Temperature

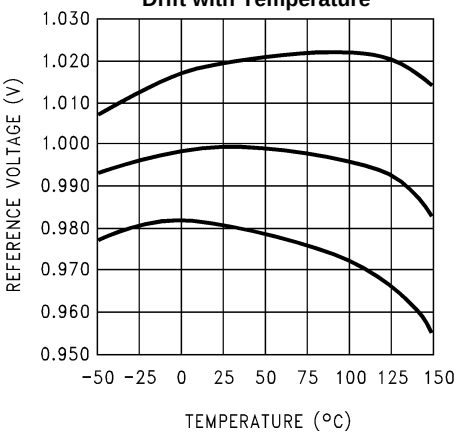


Figure 4.

Collector Saturation Voltage (Sinking Current, Emitter Grounded)

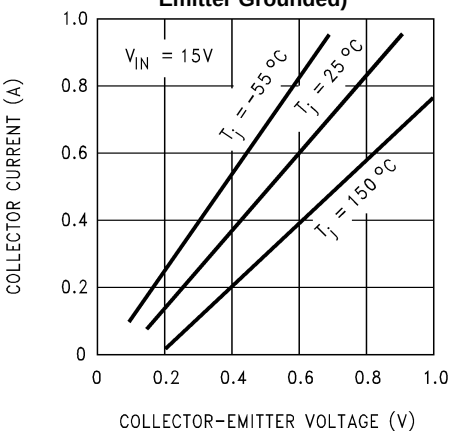


Figure 5.

Emitter Saturation Voltage (Sourcing Current, Collector at V_{in})

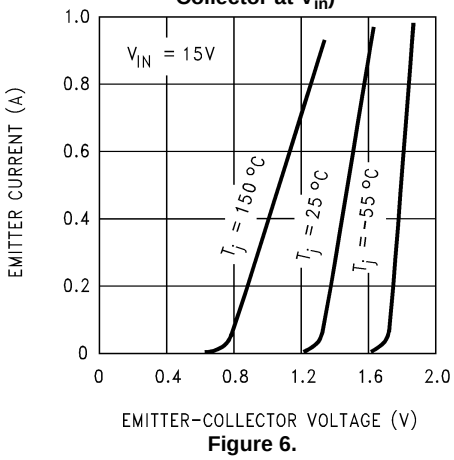


Figure 6.

Ground Referred Current Limit Sense Voltage

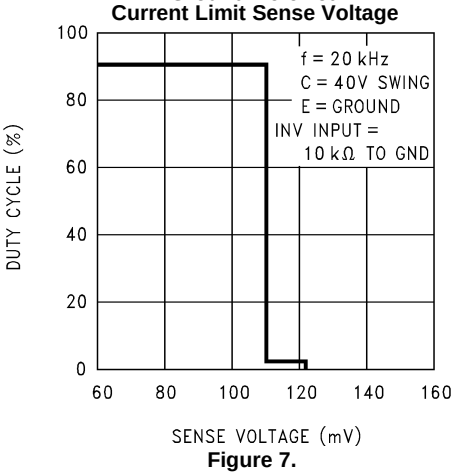


Figure 7.

Typical Performance Characteristics (continued)

Current Limit Sense Voltage Drift with Temperature

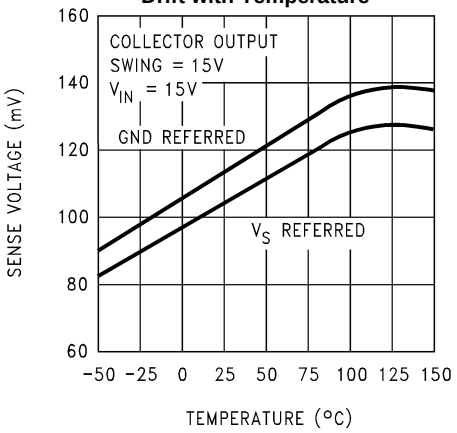


Figure 8.

Current Limit Response Time for Various Over Drives

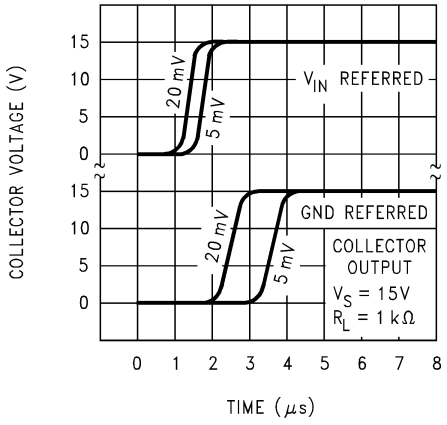


Figure 9.

Current Limit Sense Voltage vs Supply Voltage

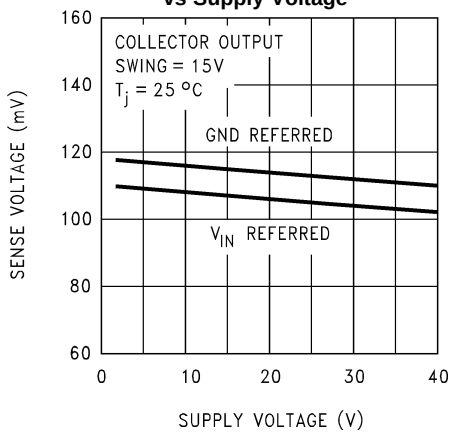


Figure 10.

Supply Current

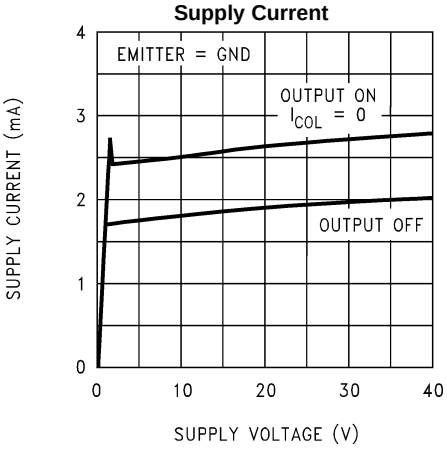


Figure 11.

Supply Current

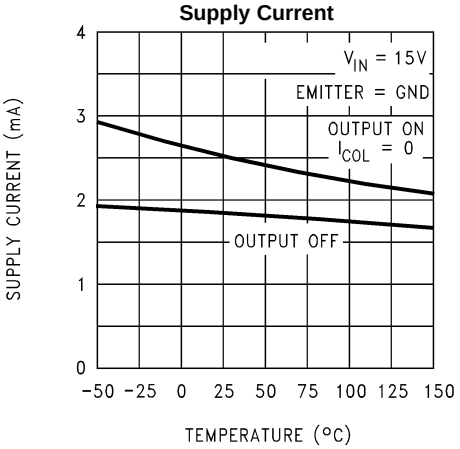


Figure 12.

Collector Current with Emitter Output Below Ground

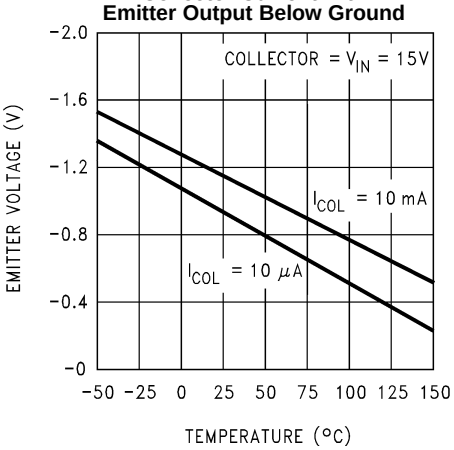


Figure 13.

TEST CIRCUIT*

Parameter tests can be made using the test circuit shown. Select the desired V_{in}, collector voltage and duty cycle with adjustable power supplies. A digital volt meter with an input resistance greater than 100 MΩ should be used to measure the following:

Input Reference Voltage to Ground; S1 in either position.

Level Shift Accuracy (%) = (T_{P3}(V)/1V) × 100%; S1 at $I_1 = I_2 = 1$ mA

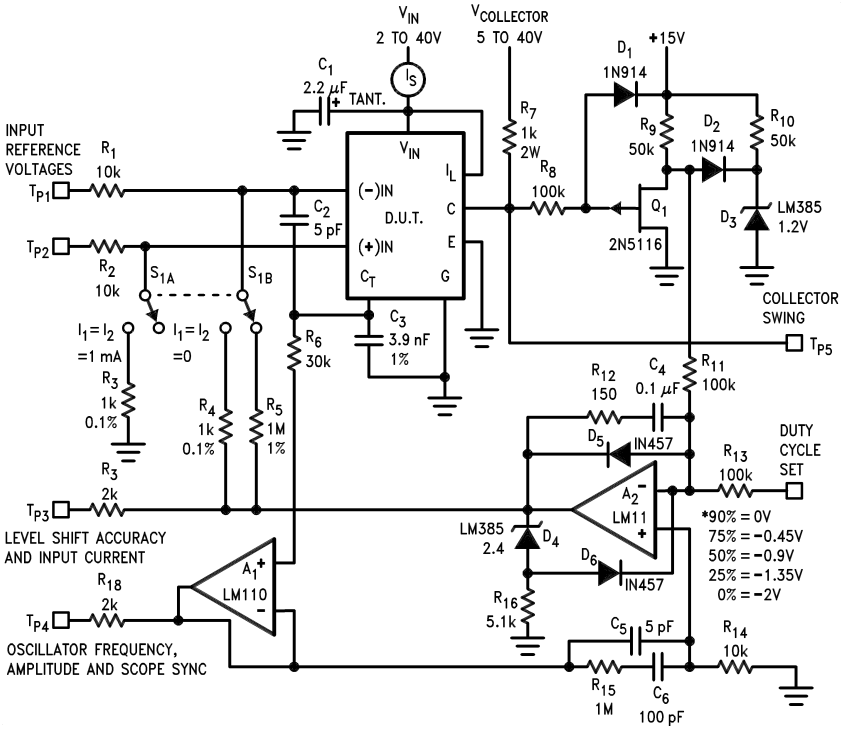
Input Current (mA) = (1V − T_{p3} (V))/1 MΩ: S1 at $I_1 = I_2 = 0$ mA.

Oscillator parameters can be measured at T_{p4} using a frequency counter or an oscilloscope.

The Current Limit Sense Voltage is measured by connecting an adjustable 0-to-1V floating power supply in series with the current limit terminal and referring it to either the ground or the V_{in} terminal. Set the duty cycle to 90% and monitor test point T_{P5} while adjusting the floating power supply voltage until the LM2578A's duty cycle just reaches 0%. This voltage is the Current Limit Sense Voltage.

The Supply Current should be measured with the duty cycle at 0% and S1 in the $I_1 = I_2 = 0$ mA position.

*LM2578A specifications are measured using automated test equipment. This circuit is provided for the customer's convenience when checking parameters. Due to possible variations in testing conditions, the measured values from these testing procedures may not match those of the factory.



Op amp supplies are ±15V
DVM input resistance >100 MΩ
*LM2578 max duty cycle is 90%

Definition of Terms

Input Reference Voltage: The voltage (referred to ground) that must be applied to either the inverting or non-inverting input to cause the regulator switch to change state (ON or OFF).

Input Reference Current: The current that must be drawn from either the inverting or non-inverting input to cause the regulator switch to change state (ON or OFF).

Input Level Shift Accuracy: This specification determines the output voltage tolerance of a regulator whose output control depends on drawing equal currents from the inverting and non-inverting inputs (see the Inverting Regulator of Figure 34, and the RS-232 Line Driver Power Supply of Figure 36).

Level Shift Accuracy is tested by using two equal-value resistors to draw current from the inverting and non-inverting input terminals, then measuring the percentage difference in the voltages across the resistors that produces a controlled duty cycle at the switch output.

Collector Saturation Voltage: With the inverting input terminal grounded thru a 10 kΩ resistor and the output transistor's emitter connected to ground, the Collector SaturationVoltage is the collector-to-emitter voltage for a given collector current.

Emitter Saturation Voltage: With the inverting input terminal grounded thru a 10 kΩ resistor and the output transistor's collector connected to V_{in}, the Emitter Saturation Voltage is the collector-to-emitter voltage for a given emitter current.

Collector Emitter Sustaining Voltage: The collector-emitter breakdown voltage of the output transistor, measured at a specified current.

Current Limit Sense Voltage: The voltage at the Current Limit pin, referred to either the supply or the ground terminal, which (via logic circuitry) will cause the output transistor to turn OFF and resets cycle-by-cycle at the oscillator frequency.

Current Limit Sense Current: The bias current for the Current Limit terminal with the applied voltage equal to the Current Limit Sense Voltage.

Supply Current: The IC power supply current, excluding the current drawn through the output transistor, with the oscillator operating.

Functional Description

The LM2578A is a pulse-width modulator designed for use as a switching regulator controller. It may also be used in other applications which require controlled pulse-width voltage drive.

A control signal, usually representing output voltage, fed into the LM2578A's comparator is compared with an internally-generated reference. The resulting error signal and the oscillator's output are fed to a logic network which determines when the output transistor will be turned ON or OFF. The following is a brief description of the subsections of the LM2578A.

COMPARATOR INPUT STAGE

The LM2578A's comparator input stage is unique in that both the inverting and non-inverting inputs are available to the user, and both contain a 1.0V reference. This is accomplished as follows: A 1.0V reference is fed into a modified voltage follower circuit (see FUNCTIONAL DIAGRAM). When both input pins are open, no current flows through R1 and R2. Thus, both inputs to the comparator will have the potential of the 1.0V reference, V_A. When one input, for example the non-inverting input, is pulled ΔV away from V_A, a current of ΔV/R1 will flow through R1. This same current flows through R2, and the comparator sees a total voltage of 2ΔV between its inputs. The high gain of the system, through feedback, will correct for this imbalance and return both inputs to the 1.0V level.

This unusual comparator input stage increases circuit flexibility, while minimizing the total number of external components required for a voltage regulator system. The inverting switching regulator configuration, for example, can be set up without having to use an external op amp for feedback polarity reversal (see TYPICAL APPLICATIONS).

OSCILLATOR

The LM2578A provides an on-board oscillator which can be adjusted up to 100 kHz. Its frequency is set by a single external capacitor, C_1, as shown in Figure 14, and follows the equation

$f_{OSC} = 8 \times 10^{-5} / C_1$

The oscillator provides a blanking pulse to limit maximum duty cycle to 90%, and a reset pulse to the internal circuitry.

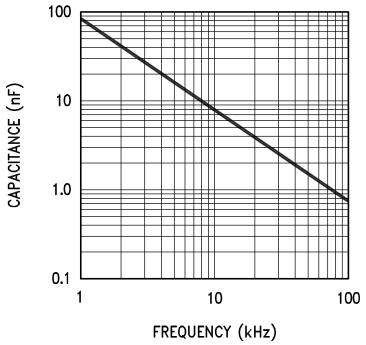


Figure 14. Value of Timing Capacitor vs Oscillator Frequency

OUTPUT TRANSISTOR

The output transistor is capable of delivering up to 750 mA with a saturation voltage of less than 0.9V. (see *Collector Saturation Voltage* and *Emitter Saturation Voltage* curves).

The emitter must not be pulled more than 1V below ground (this limit is 0.6V for $T_J \geq 100°C$). Because of this limit, an external transistor must be used to develop negative output voltages (see the Inverting Regulator Typical Application). Other configurations may need protection against violation of this limit (see the Emitter Output section of the Applications Information).

CURRENT LIMIT

The LM2578A's current limit may be referenced to either the ground or the V_{in} pins, and operates on a cycle-by-cycle basis.

The current limit section consists of two comparators: one with its non-inverting input referenced to a voltage 110 mV below V_{in}, the other with its inverting input referenced 110 mV above ground (see FUNCTIONAL DIAGRAM). The current limit is activated whenever the current limit terminal is pulled 110 mV away from either V_{in} or ground.

Applications Information

CURRENT LIMIT

As mentioned in the functional description, the current limit terminal may be referenced to either the V_{in} or the ground terminal. Resistor R3 converts the current to be sensed into a voltage for current limit detection.

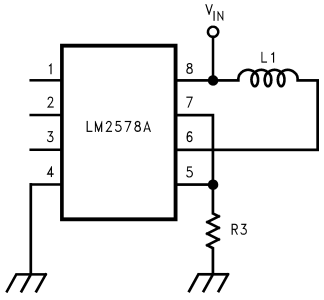


Figure 15. Current Limit, Ground Referred

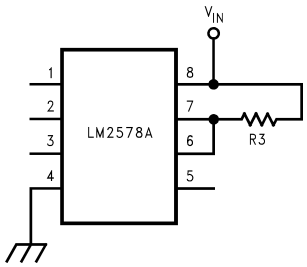


Figure 16. Current Limit, V_{in} Referred

CURRENT LIMIT TRANSIENT SUPPRESSION

When noise spikes and switching transients interfere with proper current limit operation, R1 and C1 act together as a low pass filter to control the current limit circuitry's response time.

Because the sense current of the current limit terminal varies according to where it is referenced, R1 should be less than 2 kΩ when referenced to ground, and less than 100Ω when referenced to V_{in}.

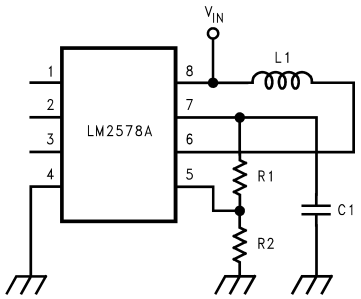


Figure 17. Current Limit Transient Suppressor, Ground Referred

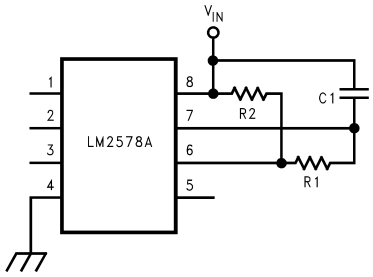


Figure 18. Current Limit Transient Suppressor, V_{in} Referred

C.L. SENSE VOLTAGE MULTIPLICATION

When a larger sense resistor value is desired, the voltage divider network, consisting of R1 and R2, may be used. This effectively multiplies the sense voltage by (1 + R1/R2). Also, R1 can be replaced by a diode to increase current limit sense voltage to about 800 mV (diode V_f + 110 mV).

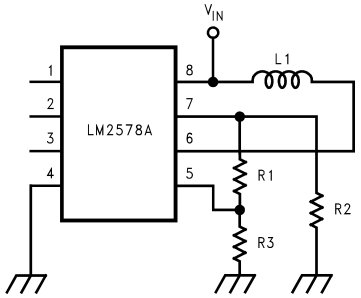


Figure 19. Current Limit Sense Voltage Multiplication, Ground Referred

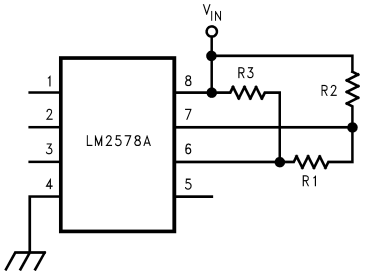


Figure 20. Current Limit Sense Voltage Multiplication, V_{in} Referred

UNDER-VOLTAGE LOCKOUT

Under-voltage lockout is accomplished with few external components. When V_{in} becomes lower than the zener breakdown voltage, the output transistor is turned off. This occurs because diode D1 will then become forward biased, allowing resistor R3 to sink a greater current from the non-inverting input than is sunk by the parallel combination of R1 and R2 at the inverting terminal. R3 should be one-fifth of the value of R1 and R2 in parallel.

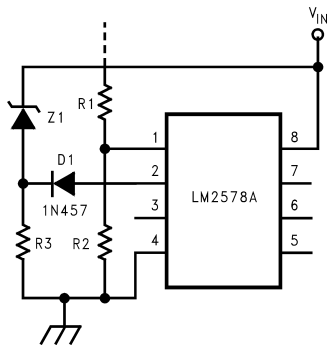


Figure 21. Under-Voltage Lockout

MAXIMUM DUTY CYCLE LIMITING

The maximum duty cycle can be externally limited by adjusting the charge to discharge ratio of the oscillator capacitor with a single external resistor. Typical values are 50 µA for the charge current, 450 µA for the discharge current, and a voltage swing from 200 mV to 750 mV. Therefore, R1 is selected for the desired charging and discharging slopes and C1 is readjusted to set the oscillator frequency.

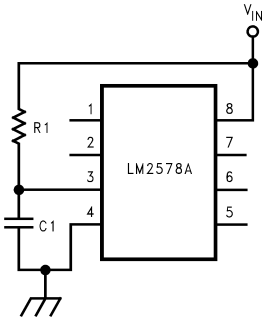


Figure 22. Maximum Duty Cycle Limiting

DUTY CYCLE ADJUSTMENT

When manual or mechanical selection of the output transistor's duty cycle is needed, the cirucit shown below may be used. The output will turn on with the beginning of each oscillator cycle and turn off when the current sunk by R2 and R3 from the non-inverting terminal becomes greater than the current sunk from the inverting terminal.

With the resistor values as shown, R3 can be used to adjust the duty cycle from 0% to 90%.

When the sum of R2 and R3 is twice the value of R1, the duty cycle will be about 50%. C1 may be a large electrolytic capacitor to lower the oscillator frequency below 1 Hz.

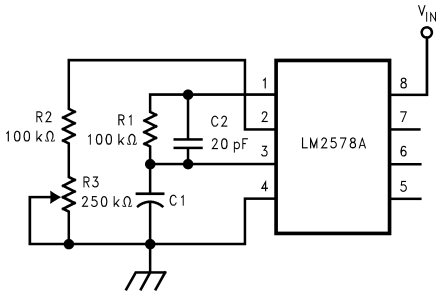


Figure 23. Duty Cycle Adjustment

REMOTE SHUTDOWN

The LM2578A may be remotely shutdown by sinking a greater current from the non-inverting input than from the inverting input. This may be accomplished by selecting resistor R3 to be approximately one-half the value of R1 and R2 in parallel.

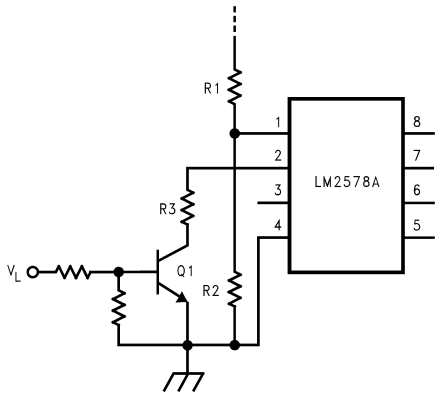


Figure 24. Shutdown Occurs when V_L is High

EMITTER OUTPUT

When the LM2578A output transistor is in the OFF state, if the Emitter output swings below the ground pin voltage, the output transistor will turn ON because its base is clamped near ground. The *Collector Current with Emitter Output Below Ground* curve shows the amount of Collector current drawn in this mode, vs temperature and Emitter voltage. When the Collector-Emitter voltage is high, this current will cause high power dissipation in the output transistor and should be avoided.

This situation can occur in the high-current high-voltage buck application if the Emitter output is used and the catch diode's forward voltage drop is greater than 0.6V. A fast-recovery diode can be added in series with the Emitter output to counter the forward voltage drop of the catch diode (see Figure 15). For better efficiency of a high output current buck regulator, an external PNP transistor should be used as shown in Figure 29.

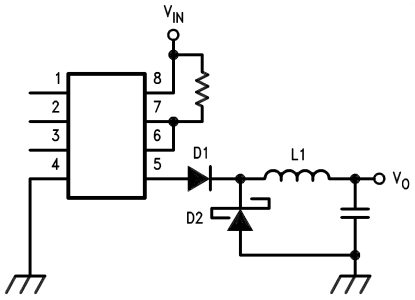


Figure 25. D1 Prevents Output Transistor from Improperly Turning ON due to D2's Forward Voltage

SYNCHRONIZING DEVICES

When several devices are to be operated at once, their oscillators may be synchronized by the application of an external signal. This drive signal should be a pulse waveform with a minimum pulse width of 2 µs. and an amplitude from 1.5V to 2.0V. The signal source must be capable of 1.) driving capacitive loads and 2.) delivering up to 500 µA for each LM2578A.

Capacitors C1 thru CN are to be selected for a 20% slower frequency than the synchronization frequency.

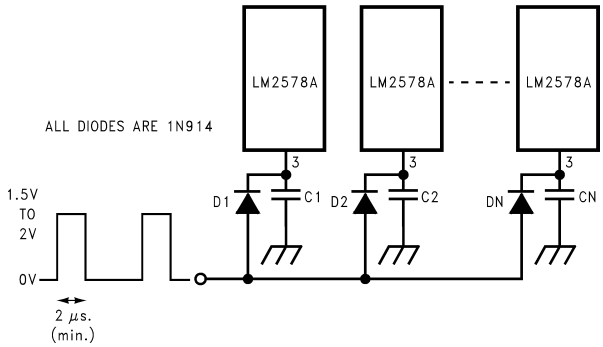


Figure 26. Synchronizing Devices

Typical Applications

The LM2578A may be operated in either the continuous or the discontinuous conduction mode. The following applications (except for the Buck-Boost Regulator) are designed for continuous conduction operation. That is, the inductor current is not allowed to fall to zero. This mode of operation has higher efficiency and lower EMI characteristics than the discontinuous mode.

BUCK REGULATOR

The buck configuration is used to step an input voltage down to a lower level. Transistor Q1 in Figure 27 chops the input DC voltage into a squarewave. This squarewave is then converted back into a DC voltage of lower magnitude by the low pass filter consisting of L1 and C1. The duty cycle, D, of the squarewave relates the output voltage to the input voltage by the following equation:

$V_{out} = D \times V_{in} = V_{in} \times (t_{on})/(t_{on} + t_{off})$.

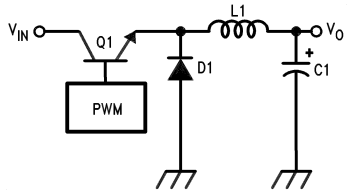


Figure 27. Basic Buck Regulator

Figure 28 is a 15V to 5V buck regulator with an output current, I_o, of 350 mA. The circuit becomes discontinuous at 20% of $I_{o(max)}$, has 10 mV of output voltage ripple, an efficiency of 75%, a load regulation of 30 mV (70 mA to 350 mA) and a line regulation of 10 mV ($12 \le V_{in} \le 18V$).

Component values are selected as follows:

$R1 = (V_o - 1) \times R2$ where R2 = 10 kΩ

$R3 = V/I_{sw(max)}$

R3 = 0.15Ω

where:

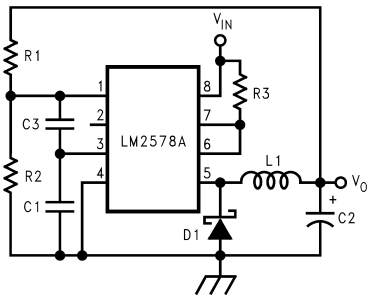
V is the current limit sense voltage, 0.11V

$I_{sw(max)}$ is the maximum allowable current thru the output transistor.

L1 is the inductor and may be found from the inductance calculation chart (Figure 29) as follows:

Given V_{in} = 15V
V_o = 5V
$I_{o(max)}$ = 350 mA
f_{OSC} = 50 kHz
Discontinuous at 20% of $I_{o(max)}$.

Note that since the circuit will become discontinuous at 20% of $I_{o(max)}$, the load current must not be allowed to fall below 70 mA.



V_{in} = 15V
V_o = 5V
V_{ripple} = 10 mV
I_o = 350 mA
f_{osc} = 50 kHz
R1 = 40 kΩ
R2 = 10 kΩ
R3 = 0.15Ω
C1 = 1820 pF
C2 = 220 µF
C3 = 20 pF
L1 = 470 µH
D1 = 1N5818

Figure 28. Buck or Step-Down Regulator

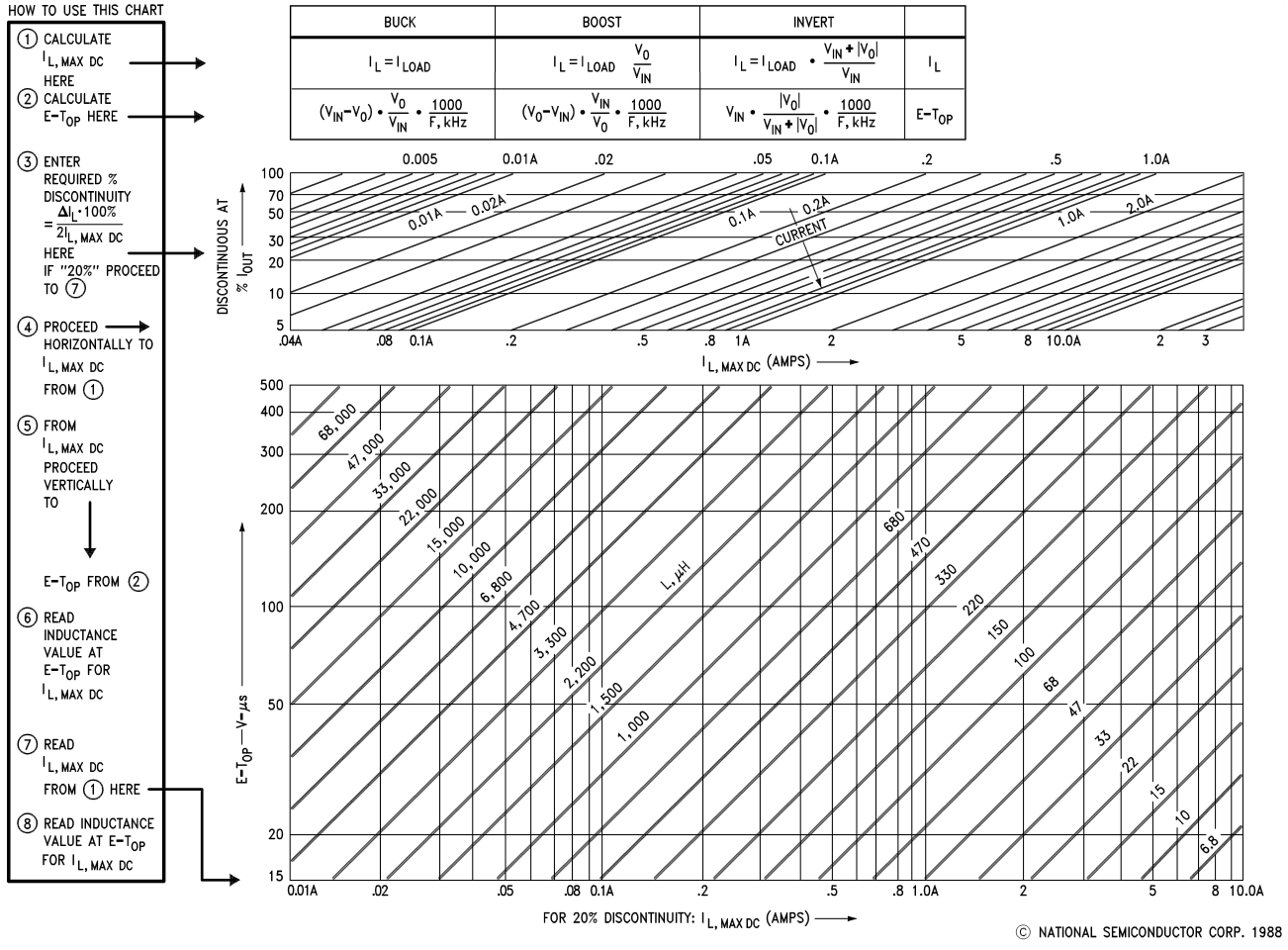


Figure 29. DC/DC Inductance Calculator

Step 1: Calculate the maximum DC current through the inductor, $I_{L(max)}$. The necessary equations are indicated at the top of the chart and show that $I_{L(max)} = I_{o(max)}$ for the buck configuration. Thus, $I_{L(max)}$ = 350 mA.

Step 2: Calculate the inductor Volts-sec product, E-T_{op}, according to the equations given from the chart. For the Buck:

$E\text{-}T_{op} = (V_{in} - V_o)\ (V_o/V_{in})\ (1000/f_{osc})$

$=(15 - 5)\ (5/15)\ (1000/50)$

= 66V-µs.

with the oscillator frequency, f_{osc}, expressed in kHz.

Step 3: Using the graph with axis labeled "Discontinuous At % I_{OUT}" and "$I_{L(max,\ DC)}$" find the point where the desired maximum inductor current, $I_{L(max,\ DC)}$ intercepts the desired discontinuity percentage.

In this example, the point of interest is where the 0.35A line intersects with the 20% line. This is nearly the midpoint of the horizontal axis.

Step 4: This last step is merely the translation of the point found in Step 3 to the graph directly below it. This is accomplished by moving straight down the page to the point which intercepts the desired E-T_{op}. For this example, E-T_{op} is 66V-µs and the desired inductor value is 470 µH. Since this example was for 20% discontinuity, the bottom chart could have been used directly, as noted in step 3 of the chart instructions.

For a full line of standard inductor values, contact Pulse Engineering (San Diego, Calif.) regarding their PE526XX series, or A. I. E. Magnetics (Nashville, Tenn.).

A more precise inductance value may be calculated for the Buck, Boost and Inverting Regulators as follows:

BUCK

$L = V_o\ (V_{in} - V_o)/(\Delta I_L\ V_{in}\ f_{osc})$

BOOST

$L = V_{in}\ (V_o - V_{in})/(\Delta I_L\ f_{osc}\ V_o)$

INVERT

$L = V_{in}\ |V_o|/[\Delta I_L(V_{in} + |V_o|)f_{osc}]$

where ΔI_L is the current ripple through the inductor. ΔI_L is usually chosen based on the minimum load current expected of the circuit. For the buck regulator, since the inductor current I_L equals the load current I_O,

$\Delta I_L = 2 \bullet I_{O(min)}$

ΔI_L = 140 mA for this circuit. ΔI_L can also be interpreted as

$\Delta I_L = 2 \bullet$ (Discontinuity Factor) $\bullet I_L$

where the Discontinuity Factor is the ratio of the minimum load current to the maximum load current. For this example, the Discontinuity Factor is 0.2.

The remainder of the components of Figure 28 are chosen as follows:

C1 is the timing capacitor found in Figure 14.

$C2 \geq V_o\ (V_{in} - V_o)/(8f_{osc}^2 V_{in} V_{ripple} L1)$

where V_{ripple} is the peak-to-peak output voltage ripple.

C3 is necessary for continuous operation and is generally in the 10 pF to 30 pF range.

D1 should be a Schottky type diode, such as the 1N5818 or 1N5819.

BUCK WITH BOOSTED OUTPUT CURRENT

For applications requiring a large output current, an external transistor may be used as shown in Figure 30. This circuit steps a 15V supply down to 5V with 1.5A of output current. The output ripple is 50 mV, with an efficiency of 80%, a load regulation of 40 mV (150 mA to 1.5A), and a line regulation of 20 mV ($12V \leq V_{in} \leq 18V$).

Component values are selected as outlined for the buck regulator with a discontinuity factor of 10%, with the addition of R4 and R5:

$R4 = 10V_{BE1}B_f/I_p$

$R5 = (V_{in} - V - V_{BE1} - V_{sat})\ B_f/(I_{L(max,\ DC)} + I_{R4})$

where:

V_{BE1} is the V_{BE} of transistor Q1.

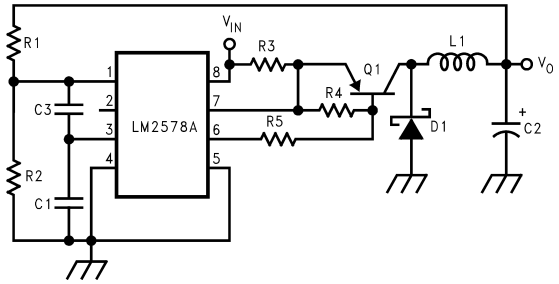
V_{sat} is the saturation voltage of the LM2578A output transistor.

V is the current limit sense voltage.

B_f is the forced current gain of transistor Q1 (B_f = 30 for Figure 30).

$I_{R4} = V_{BE1}/R4$

$I_p = I_{L(max,\ DC)} + 0.5\Delta I_L$



V_{in} = 15V	R4 = 200Ω
V_o = 5V	R5 = 330Ω
V_{ripple} = 50 mV	C1 = 1820 pF
I_o = 1.5A	C2 = 330 µF
f_{osc} = 50 kHz	C3 = 20 pF
R1 = 40 kΩ	L1 = 220 µH
R2 = 10 kΩ	D1 = 1N5819
R3 = 0.05Ω	Q1 = D45

Figure 30. Buck Converter with Boosted Output Current

BOOST REGULATOR

The boost regulator converts a low input voltage into a higher output voltage. The basic configuration is shown in Figure 31. Energy is stored in the inductor while the transistor is on and then transferred with the input voltage to the output capacitor for filtering when the transistor is off. Thus,

$V_o = V_{in} + V_{in}(t_{on}/t_{off})$.

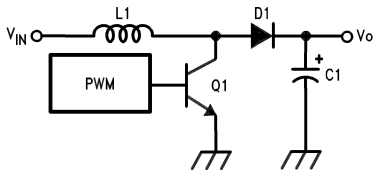
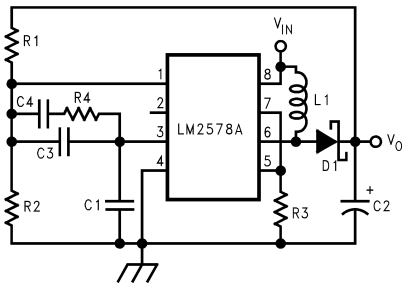


Figure 31. Basic Boost Regulator

The circuit of Figure 32 converts a 5V supply into a 15V supply with 150 mA of output current, a load regulation of 14 mV (30 mA to 140 mA), and a line regulation of 35 mV (4.5V ≤ V_{in} ≤ 8.5V).



V_{in} = 5V

V_o = 15V

V_{ripple} = 10 mV

I_o = 140 mA

f_{osc} = 50 kHz

R1 = 140 kΩ

R2 = 10 kΩ

R3 = 0.15Ω

R4 = 200 kΩ

C1 = 1820 pF

C2 = 470 µF

C3 = 20 pF

C4 = 0.0022 µF

L1 = 330 µH

D1 = 1N5818

Figure 32. Boost or Step-Up Regulator

R1 = (V_o − 1) R2 where R2 = 10 kΩ.

R3 = V/($I_{L(max,\ DC)}$ + 0.5 ΔI_L)

where:

$\Delta I_L = 2(I_{LOAD(min)})(V_o/V_{in})$

ΔI_L is 200 mA in this example.

R4, C3 and C4 are necessary for continuous operation and are typically 220 kΩ, 20 pF, and 0.0022 µF respectively.

C1 is the timing capacitor found in Figure 14.

$C2 \geq I_o\ (V_o - V_{in})/(f_{osc}\ V_o\ V_{ripple})$.

D1 is a Schottky type diode such as a 1N5818 or 1N5819.

L1 is found as described in the buck converter section, using the inductance chart for Figure 29 for the boost configuration and 20% discontinuity.

INVERTING REGULATOR

Figure 33 shows the basic configuration for an inverting regulator. The input voltage is of a positive polarity, but the output is negative. The output may be less than, equal to, or greater in magnitude than the input. The relationship between the magnitude of the input voltage and the output voltage is $V_o = V_{in} \times (t_{on}/t_{off})$.

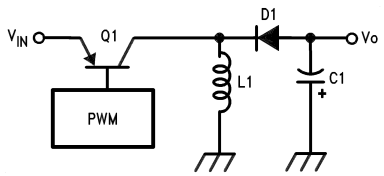


Figure 33. Basic Inverting Regulator

Figure 34 shows an LM2578A configured as a 5V to −15V polarity inverter with an output current of 300 mA, a load regulation of 44 mV (60 mA to 300 mA) and a line regulation of 50 mV (4.5V ≤ V_{in} ≤ 8.5V).

$R1 = (|V_o| + 1)\ R2$ where R2 = 10 kΩ.

$R3 = V/(I_{L(max,\ DC)} + 0.5\ \Delta I_L)$.

$R4 = 10V_{BE1}B_f/(I_{L\ (max,\ DC)} + 0.5\ \Delta I_L)$

where:

V, V_{BE1}, V_{sat}, and B_f are defined in the Buck Converter with Boosted Output Current section.

$\Delta I_L = 2(I_{LOAD(min)})(V_{in} + |V_o|)/V_{IN}$

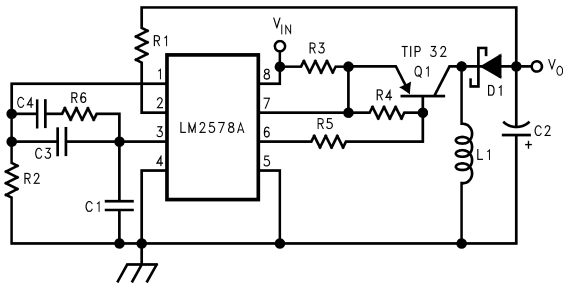
R5 is defined in the Buck Converter with Boosted Output Current section.

R6 serves the same purpose as R4 in the Boost Regulator circuit and is typically 220 kΩ.

C1, C3 and C4 are defined in the Boost Regulator section.

$C2 \geq I_o\ |V_o|/[f_{osc}(|V_o| + V_{in})\ V_{ripple}]$

L1 is found as outlined in the section on buck converters, using the inductance chart of Figure 29 for the invert configuration and 20% discontinuity.



V_{in} = 5V	R4 = 190Ω
V_o = −15V	R5 = 82Ω
V_{ripple} = 5 mV	R6 = 220 kΩ
I_o = 300 mA	C1 = 1820 pF
I_{min} = 60 mA	C2 = 1000 µF
f_{osc} = 50 kHz	C3 = 20 pF
R1 = 160 kΩ	C4 = 0.0022 µF
R2 = 10 kΩ	L1 = 150 µH
R3 = 0.01Ω	D1 = 1N5818

Figure 34. Inverting Regulator

BUCK-BOOST REGULATOR

The Buck-Boost Regulator, shown in Figure 35, may step a voltage up or down, depending upon whether or not the desired output voltage is greater or less than the input voltage. In this case, the output voltage is 12V with an input voltage from 9V to 15V. The circuit exhibits an efficiency of 75%, with a load regulation of 60 mV (10 mA to 100 mA) and a line regulation of 52 mV.

$R1 = (V_o - 1)\ R2$ where R2 = 10 kΩ

R3 = V/0. 75A

R4, C1, C3 and C4 are defined in the Boost Regulator section.

D1 and D2 are Schottky type diodes such as the 1N5818 or 1N5819.

$$C2 \geq \frac{(I_o/V_{ripple})\ (V_o + 2V_d)}{[f_{osc}\ (V_{in} + V_o + 2V_d - V_{sat} - V_{sat1})]}$$

where:

V_d is the forward voltage drop of the diodes.

V_{sat} is the saturation voltage of the LM2578A output transistor.

V_{sat1} is the saturation voltage of transistor Q1.

$$L1 \geq (V_{in} - V_{sat} - V_{sat1})\ (t_{on}/I_p) \quad (1)$$

where:

$$t_{on} = \frac{(1/f_{osc})\ (V_o + 2V_d)}{(V_o + V_{in} + 2V_d - V_{sat} - V_{sat1})}$$

$$I_p = \frac{2I_o\ (V_{in} + V_o + 2V_d - V_{sat} - V_{sat1})}{(V_{in} - V_{sat} - V_{sat1})}$$

RS-232 LINE DRIVER POWER SUPPLY

The power supply, shown in Figure 36, operates from an input voltage as low as 4.2V (5V nominal), and delivers an output of ±12V at ±40 mA with better than 70% efficiency. The circuit provides a load regulation of ±150 mV (from 10% to 100% of full load) and a line regulation of ±10 mV. Other notable features include a cycle-by-cycle current limit and an output voltage ripple of less than 40 mVp-p.

A unique feature of this circuit is its use of feedback from both outputs. This dual feedback configuration results in a sharing of the output voltage regulation by each output so that neither side becomes unbalanced as in single feedback systems. In addition, since both sides are regulated, it is not necessary to use a linear regulator for output regulation.

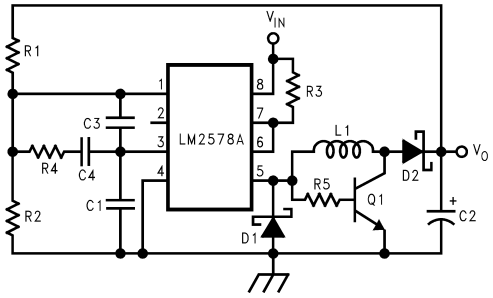
The feedback resistors, R2 and R3, may be selected as follows by assuming a value of 10 kΩ for R1;

$R2 = (V_o - 1V)/45.8\ \mu A = 240\ k\Omega$

$R3 = (|V_o| + 1V)/54.2\ \mu A = 240\ k\Omega$

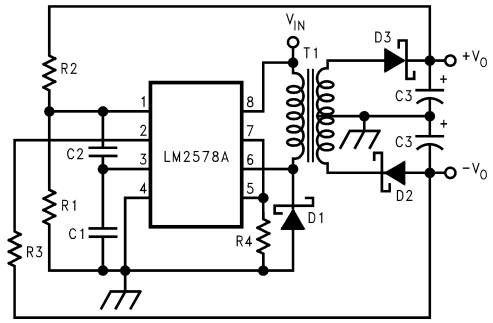
Actually, the currents used to program the values for the feedback resistors may vary from 40 µA to 60 µA, as long as their sum is equal to the 100 µA necessary to establish the 1V threshold across R1. Ideally, these currents should be equal (50 µA each) for optimal control. However, as was done here, they may be mismatched in order to use standard resistor values. This results in a slight mismatch of regulation between the two outputs.

The current limit resistor, R4, is selected by dividing the current limit threshold voltage by the maximum peak current level in the output switch. For our purposes R4 = 110 mV/750 mA = 0.15Ω. A value of 0.1Ω was used.



$9V \le V_{in} \le 15V$
V_o = 12V
I_o = 100 mA
V_{ripple} = 50 mV
f_{osc} = 50 kHz
R1 = 110k
R2 = 10k
R3 = 0.15
R4 = 220k
R5 = 270
C1 = 1820 pF
C2 = 220 µF
C3 = 20 pF
C4 = 0.0022 µF
L1 = 220 µH
D1, D2 = 1N5819
Q1 = D44

Figure 35. Buck-Boost Regulator



V_{in} = 5V
V_o ±12V
I_o = ±40 mA
f_{osc} = 80 kHz
R1 = 10 kΩ
R2 = 240 kΩ
R3 = 240 kΩ
R4 = 0.15Ω
C1 = 820 pF
C2 = 10 pF
C3 = 220 µF
D1, D2, D3 = 1N5819
T1 = PE-64287

Figure 36. RS-232 Line Driver Power Supply

Capacitor C1 sets the oscillator frequency and is selected from Figure 14.

Capacitor C2 serves as a compensation capacitor for synchronous operation and a value of 10 to 50 pF should be sufficient for most applications.

A minimum value for an ideal output capacitor C3, could be calculated as $C = I_o \times t/\Delta V$ where I_o is the load current, t is the transistor on time (typically $0.4/f_{osc}$), and ΔV is the peak-to-peak output voltage ripple. A larger output capacitor than this theoretical value should be used since electrolytics have poor high frequency performance. Experience has shown that a value from 5 to 10 times the calculated value should be used.

For good efficiency, the diodes must have a low forward voltage drop and be fast switching. 1N5819 Schottky diodes work well.

Transformer selection should be picked for an output transistor “on” time of $0.4/f_{osc}$, and a primary inductance high enough to prevent the output transistor switch from ramping higher than the transistor's rating of 750 mA. Pulse Engineering (San Diego, Calif.) and Renco Electronics, Inc. (Deer Park, N.Y.) can provide further assistance in selecting the proper transformer for a specific application need. The transformer used in Figure 36 was a Pulse Engineering PE-64287.

REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	22

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2578AM/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2578 AM	Samples
LM2578AMX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2578 AM	Samples
LM2578AN/NOPB	ACTIVE	PDIP	P	8	40	RoHS & Green	NIPDAU	Level-1-NA-UNLIM	-40 to 125	LM2578AN	Samples
LM3578AM/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 125	3578 AM	Samples
LM3578AMX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 125	3578 AM	Samples
LM3578AN/NOPB	ACTIVE	PDIP	P	8	40	RoHS & Green	NIPDAU	Level-1-NA-UNLIM	0 to 125	LM3578AN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

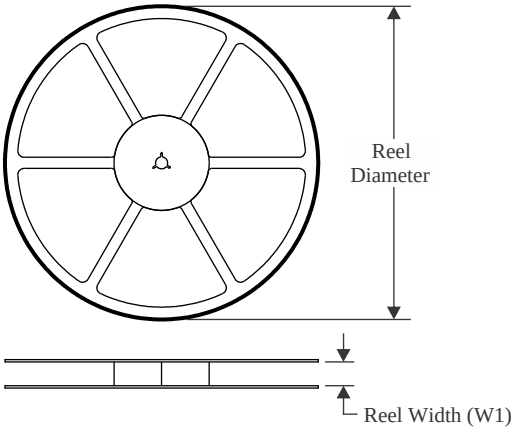
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

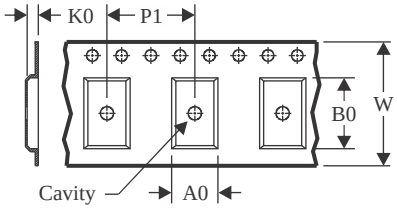
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

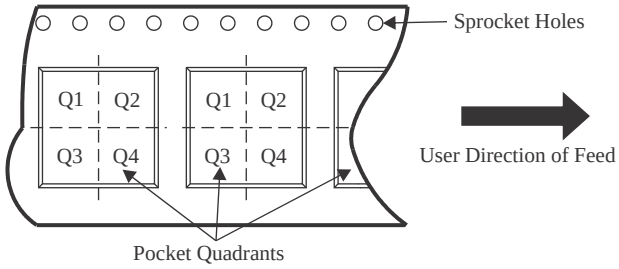


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

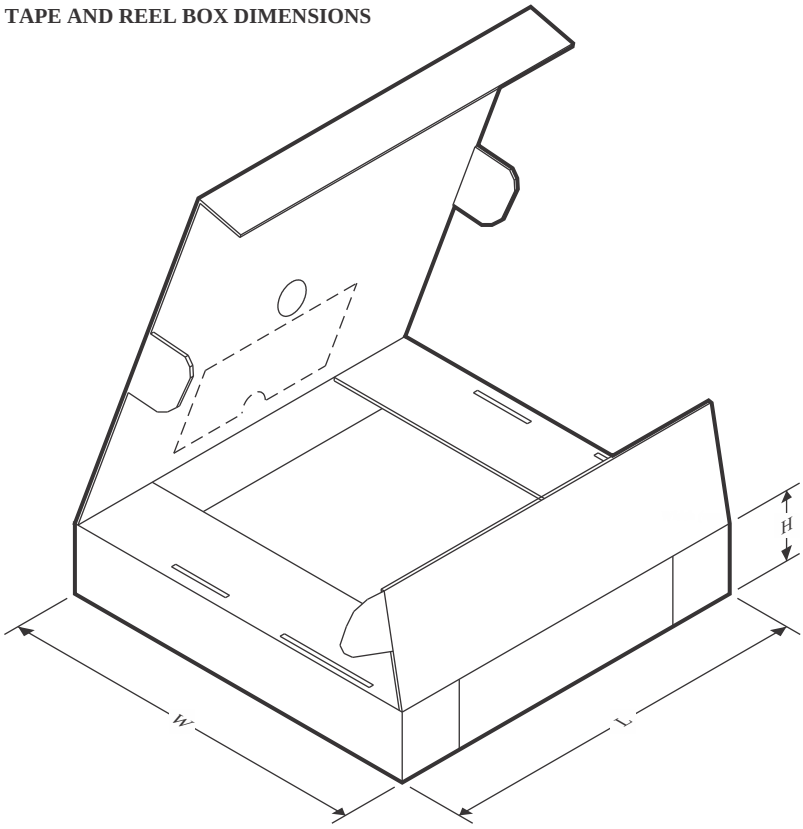
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2578AMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM3578AMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM3578AMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

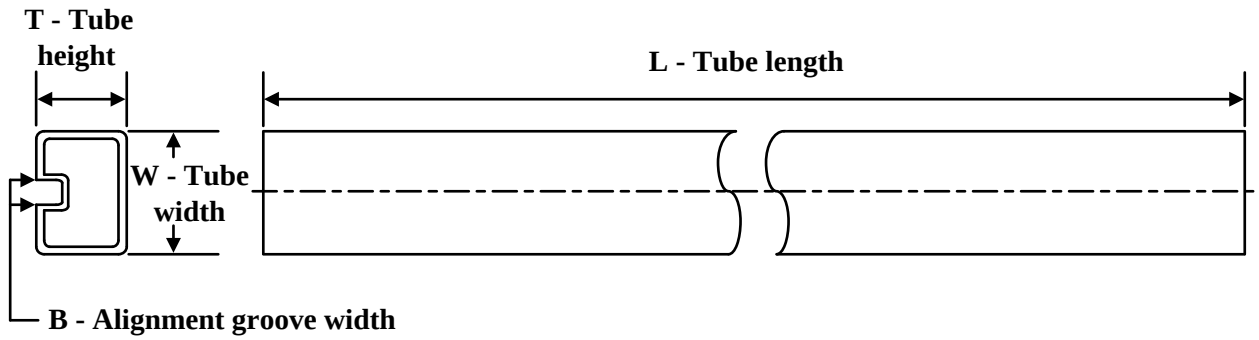
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

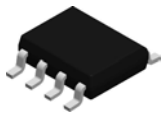
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2578AMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM3578AMX	SOIC	D	8	2500	367.0	367.0	35.0
LM3578AMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM2578AM	D	SOIC	8	95	495	8	4064	3.05
LM2578AM	D	SOIC	8	95	495	8	4064	3.05
LM2578AM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM2578AN/NOPB	P	PDIP	8	40	502	14	11938	4.32
LM3578AM	D	SOIC	8	95	495	8	4064	3.05
LM3578AM	D	SOIC	8	95	495	8	4064	3.05
LM3578AM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM3578AN/NOPB	P	PDIP	8	40	502	14	11938	4.32

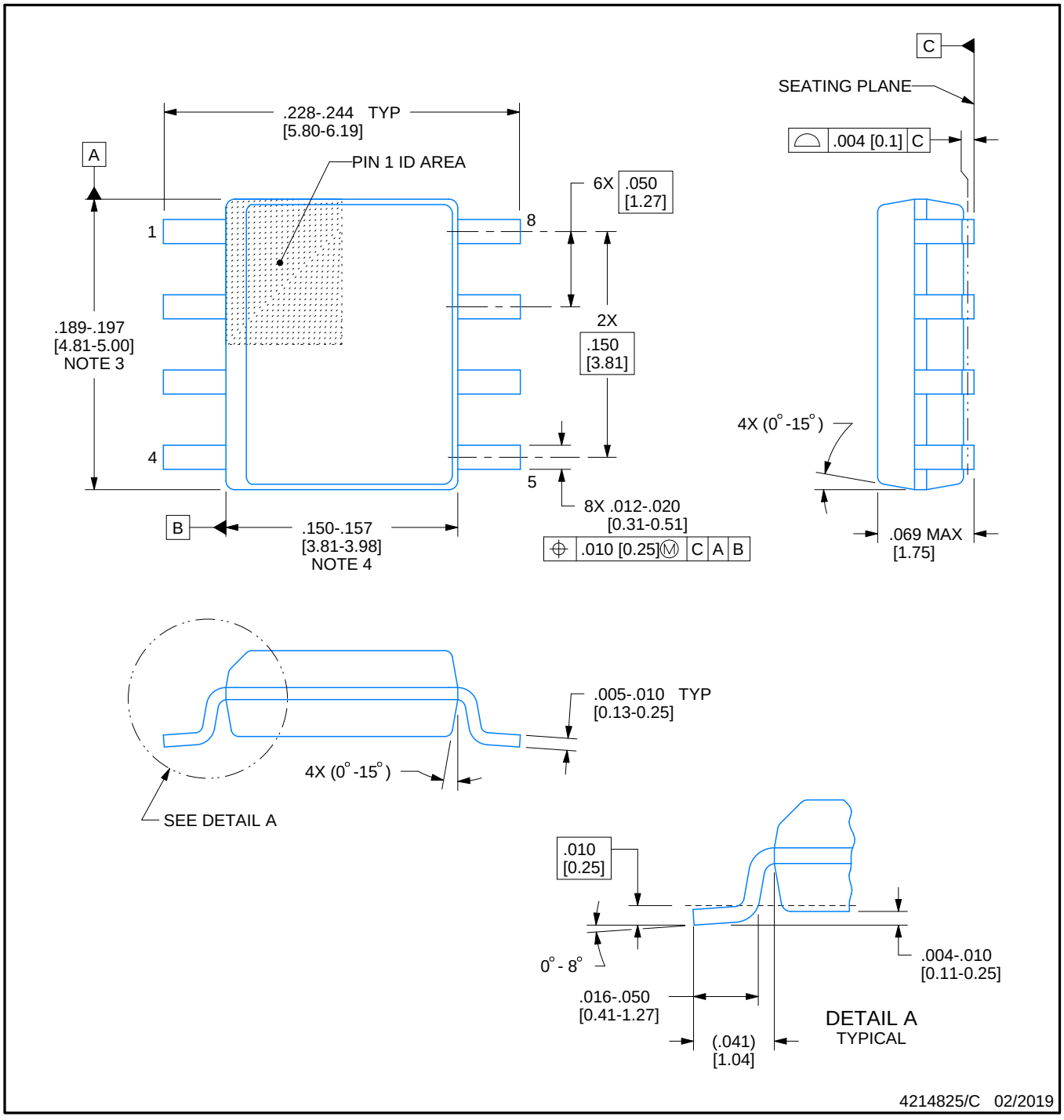


PACKAGE OUTLINE

D0008A

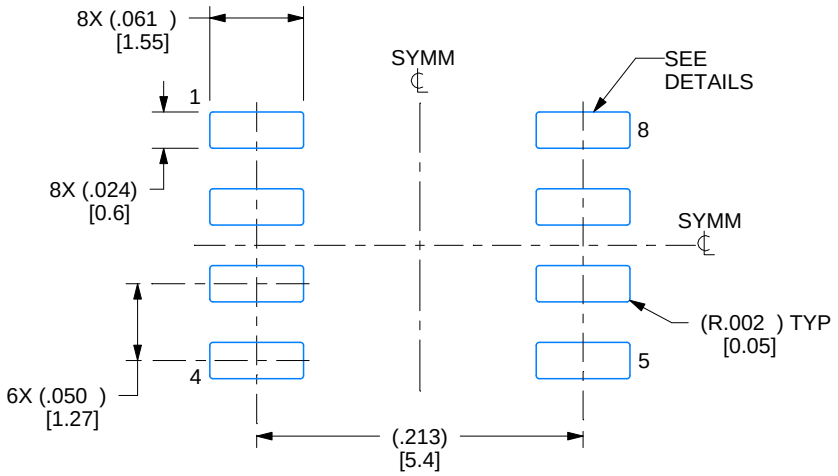
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

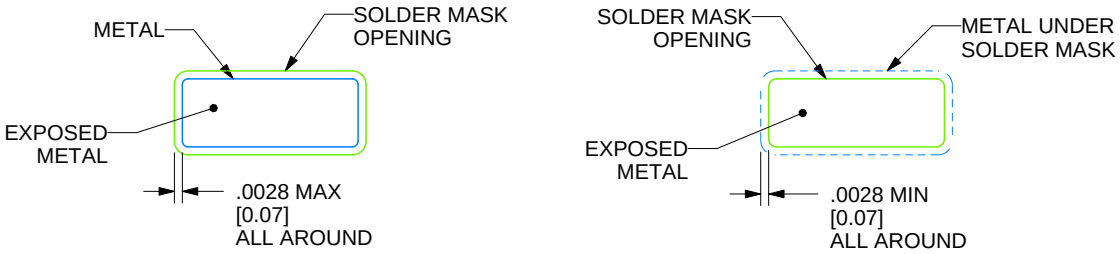


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

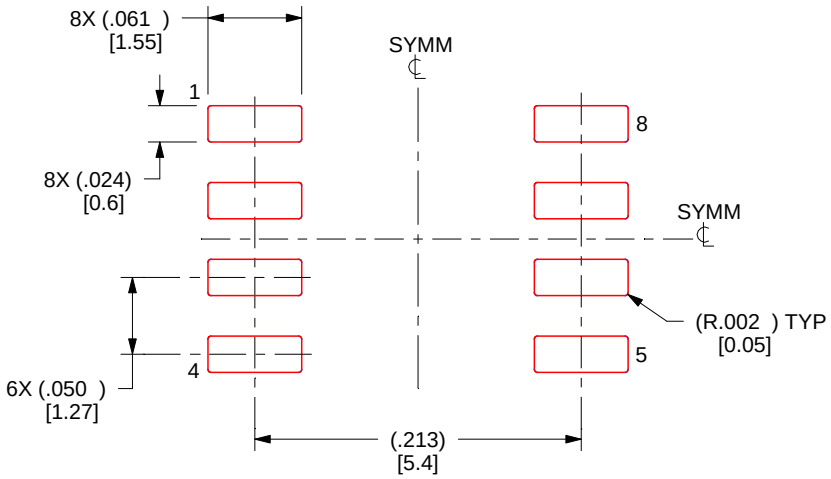
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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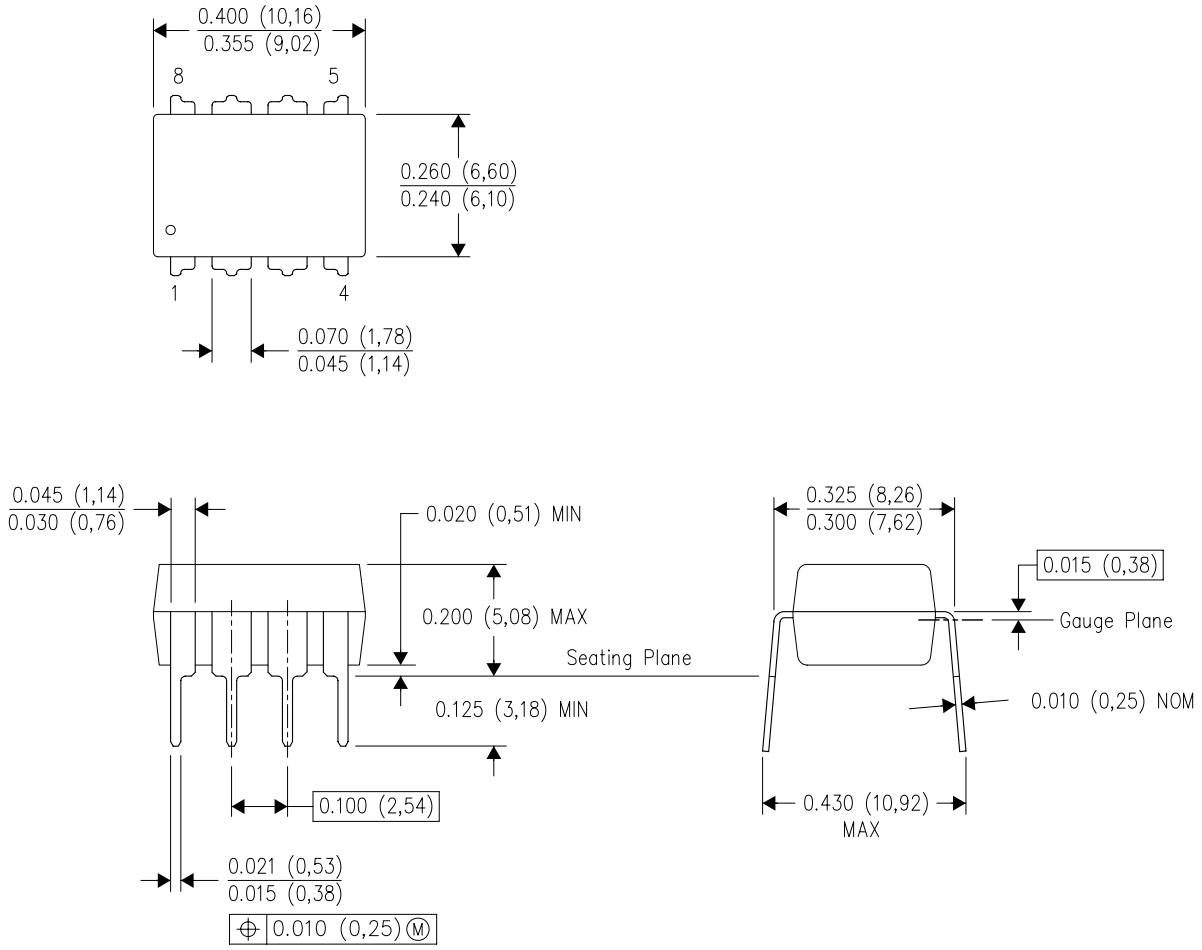
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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