TEXAS INSTRUMENTS

LM124-N, LM224-N
LM2902-N, LM324-N

SNOSC16D – MARCH 2000 – REVISED JANUARY 2015

LMx24-N, LM2902-N Low-Power, Quad-Operational Amplifiers

1 Features

- Internally Frequency Compensated for Unity Gain
- Large DC Voltage Gain 100 dB
- Wide Bandwidth (Unity Gain) 1 MHz (Temperature Compensated)
- Wide Power Supply Range:
  - Single Supply 3 V to 32 V
  - or Dual Supplies ±1.5 V to ±16 V
- Very Low Supply Current Drain (700 µA) —Essentially Independent of Supply Voltage
- Low Input Biasing Current 45 nA (Temperature Compensated)
- Low Input Offset Voltage 2 mV and Offset Current: 5 nA
- Input Common-Mode Voltage Range Includes Ground
- Differential Input Voltage Range Equal to the Power Supply Voltage
- Large Output Voltage Swing 0 V to V^+ − 1.5 V
- **Advantages:**
  - Eliminates Need for Dual Supplies
  - Four Internally Compensated Op Amps in a Single Package
  - Allows Direct Sensing Near GND and V_{OUT} also Goes to GND
  - Compatible With All Forms of Logic
  - Power Drain Suitable for Battery Operation
  - In the Linear Mode the Input Common-Mode, Voltage Range Includes Ground and the Output Voltage
  - Can Swing to Ground, Even Though Operated from Only a Single Power Supply Voltage
  - Unity Gain Cross Frequency is Temperature Compensated
  - Input Bias Current is Also Temperature Compensated

2 Applications

- Transducer Amplifiers
- DC Gain Blocks
- Conventional Op Amp Circuits

3 Description

The LM124-N series consists of four independent, high-gain, internally frequency compensated operational amplifiers designed to operate from a single power supply over a wide range of voltages. Operation from split-power supplies is also possible and the low-power supply current drain is independent of the magnitude of the power supply voltage.

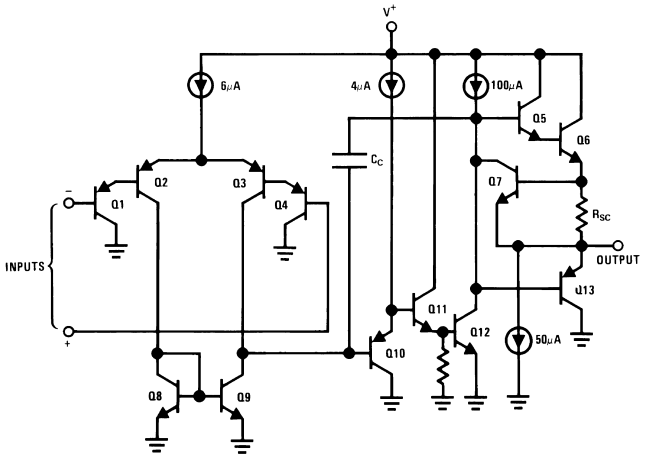
Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124-N series can directly operate off of the standard 5-V power supply voltage which is used in digital systems and easily provides the required interface electronics without requiring the additional ±15 V power supplies.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM124-N	CDIP (14)	19.56 mm × 6.67 mm
LM224-N		
LM324-N	CDIP (14)	19.56 mm × 6.67 mm
	PDIP (14)	19.177 mm × 6.35 mm
	SOIC (14)	8.65 mm × 3.91 mm
	TSSOP (14)	5.00 mm × 4.40 mm
LM2902-N	PDIP (14)	19.177 mm × 6.35 mm
	SOIC (14)	8.65 mm × 3.91 mm
	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Schematic Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 5
6.5 Electrical Characteristics: LM124A/224A/324A ... 5
6.6 Electrical Characteristics: LM124-N/224-N/324-N/2902-N ... 6
6.7 Typical Characteristics ... 8
7 Detailed Description ... 11
7.1 Overview ... 11
7.2 Functional Block Diagram ... 11
7.3 Feature Description ... 11
7.4 Device Functional Modes ... 11
8 Application and Implementation ... 13
8.1 Application Information ... 13
8.2 Typical Applications ... 13
9 Power Supply Recommendations ... 23
10 Layout ... 23
10.1 Layout Guidelines ... 23
10.2 Layout Example ... 23
11 Device and Documentation Support ... 24
11.1 Related Links ... 24
11.2 Trademarks ... 24
11.3 Electrostatic Discharge Caution ... 24
11.4 Glossary ... 24
12 Mechanical, Packaging, and Orderable Information ... 24

4 Revision History

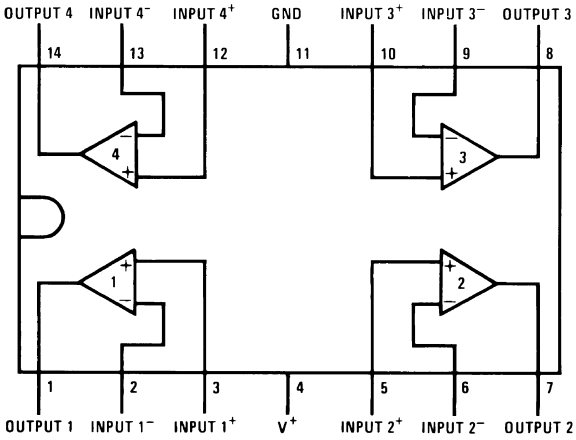
Changes from Revision C (November 2012) to Revision D **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

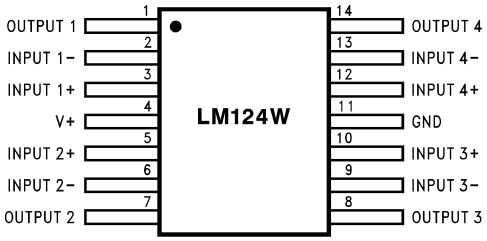
Copyright © 2000–2015, Texas Instruments Incorporated

5 Pin Configuration and Functions

J Package
14-Pin CDIP
Top View



D Package
14-Pin SOIC
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
OUTPUT1	1	O	Output, Channel 1
INPUT1-	2	I	Inverting Input, Channel 1
INPUT1+	3	I	Noninverting Input, Channel 1
V+	4	P	Positive Supply Voltage
INPUT2+	5	I	Nonnverting Input, Channel 2
INPUT2-	6	I	Inverting Input, Channel 2
OUTPUT2	7	O	Output, Channel 2
OUTPUT3	8	O	Output, Channel 3
INPUT3-	9	I	Inverting Input, Channel 3
INPUT3+	10	I	Noninverting Input, Channel 3
GND	11	P	Ground or Negative Supply Voltage
INPUT4+	12	I	Noninverting Input, Channel 4
INPUT4-	13	I	Inverting Input, Channel 4
OUTPUT4	14	O	Output, Channel 4

Copyright © 2000–2015, Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings

See (1)(2).

			LM124-N/LM224-N/LM324-N LM124A/LM224A/LM324A		LM2902-N		
			MIN	MAX	MIN	MAX	UNIT
Supply Voltage, V^+				32		26	V
Differential Input Voltage				32		26	V
Input Voltage			−0.3	32	−0.3	26	V
Input Current (V_{IN} < −0.3 V)(3)				50		50	mA
Power Dissipation(4)	PDIP			1130		1130	mW
	CDIP			1260		1260	mW
	SOIC Package			800		800	mW
Output Short-Circuit to GND (One Amplifier)(5)		V^+ ≤ 15 V and T_A = 25°C	Continuous		Continuous		
Lead Temperature (Soldering, 10 seconds)				260		260	°C
Soldering Information	Dual-In-Line Package	Soldering (10 seconds)		260		260	°C
	Small Outline Package	Vapor Phase (60 seconds)		215		215	°C
		Infrared (15 seconds)		220		220	°C
Storage temperature, T_{stg}			–65	150	–65	150	°C

(1) Refer to RETS124AX for LM124A military specifications and refer to RETS124X for LM124-N military specifications.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3 V (at 25°C).
(4) For operating at high temperatures, the LM324-N/LM324A/LM2902-N must be derated based on a 125°C maximum junction temperature and a thermal resistance of 88°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM224-N/LM224A and LM124-N/LM124A can be derated based on a 150°C maximum junction temperature. The dissipation is the total of all four amplifiers—use external resistors, where possible, to allow the amplifier to saturate of to reduce the power which is dissipated in the integrated circuit.
(5) Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of 15 V, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±250	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply Voltage (V^+ - V^-): LM124-N/LM124A/LM224-N/LM224A/LM324-N/LM324A	3	32	V
Supply Voltage (V^+ - V^-): LM2902-N	3	26	V
Operating Input Voltage on Input pins	0	V+	V
Operating junction temperature, T_J: LM124-N/LM124A	-55	125	°C
Operating junction temperature, T_J: L2902-N	-40	85	°C
Operating junction temperature, T_J: LM224-N/LM224A	-25	85	°C
Operating junction temperature, T_J: LM324-N/LM324A	0	70	°C

Copyright © 2000–2015, Texas Instruments Incorporated

6.4 Thermal Information

THERMAL METRIC[1]		LM124-N / LM224-N	LM324-N / LM2902-N	UNIT
		J/CDIP	D/SOIC	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	88	88	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics: LM124A/224A/324A

V^+ = 5.0 V, [1], unless otherwise stated

PARAMETER		TEST CONDITIONS	LM124A			LM224A			LM324A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage		T_A = 25°C[2]		1	2		1	3		2	3	mV
Input Bias Current[3]		$I_{IN(+)}$ or $I_{IN(-)}$, V_{CM} = 0 V, T_A = 25°C		20	50		40	80		45	100	nA
Input Offset Current		$I_{IN(+)}$ or $I_{IN(-)}$, V_{CM} = 0 V, T_A = 25°C		2	10		2	15		5	30	nA
Input Common-Mode Voltage Range[4]		V^+ = 30 V, (LM2902-N, V^+ = 26 V), T_A = 25°C	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	V
Supply Current		Over Full Temperature Range, R_L = ∞ On All Op Amps V^+ = 30 V (LM2902-N V^+ = 26 V)		1.5	3		1.5	3		1.5	3	mA
		V^+ = 5 V		0.7	1.2		0.7	1.2		0.7	1.2	
Large Signal Voltage Gain		V^+ = 15 V, R_L≥ 2 kΩ, (V_O = 1 V to 11 V), T_A = 25°C	50	100		50	100		25	100		V/mV
Common-Mode Rejection Ratio		DC, V_{CM} = 0 V to V^+ − 1.5 V, T_A = 25°C	70	85		70	85		65	85		dB
Power Supply Rejection Ratio		V^+ = 5 V to 30 V, (LM2902-N, V^+ = 5V to 26 V), T_A = 25°C	65	100		65	100		65	100		dB
Amplifier-to-Amplifier Coupling[5]		f = 1 kHz to 20 kHz, T_A = 25°C, (Input Referred)		−120			−120			−120		dB
Output Current	Source	V_{IN}^+ = 1 V, V_{IN}^- = 0 V, V^+ = 15 V, V_O = 2 V, T_A = 25°C	20	40		20	40		20	40		mA
	Sink	V_{IN}^- = 1 V, V_{IN}^+ = 0 V, V^+ = 15 V, V_O = 2 V, T_A = 25°C	10	20		10	20		10	20		µA
		V_{IN}^- = 1 V, V_{IN}^+ = 0 V, V^+ = 15 V, V_O = 200 mV, T_A = 25°C	12	50		12	50		12	50		
Short Circuit to Ground		V^+ = 15 V, T_A = 25°C[6]		40	60		40	60		40	60	mA
Input Offset Voltage		See[2]			4			4			5	mV
V_{OS} Drift		R_S = 0 Ω		7	20		7	20		7	30	µV/°C
Input Offset Current		$I_{IN(+)}$ − $I_{IN(-)}$, V_{CM} = 0 V			30			30			75	nA

(1) These specifications are limited to −55°C ≤ T_A ≤ +125°C for the LM124-N/LM124A. With the LM224-N/LM224A, all temperature specifications are limited to −25°C ≤ T_A ≤ +85°C, the LM324-N/LM324A temperature specifications are limited to 0°C ≤ T_A ≤ +70°C, and the LM2902-N specifications are limited to −40°C ≤ T_A ≤ +85°C.
(2) V_O ≅ 1.4V, R_S = 0 Ω with V^+ from 5 V to 30 V; and over the full input common-mode range (0 V to V^+ − 1.5 V) for LM2902-N, V^+ from 5 V to 26 V.
(3) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
(4) The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3 V (at 25°C). The upper end of the common-mode voltage range is V^+ − 1.5 V (at 25°C), but either or both inputs can go to 32 V without damage (26 V for LM2902-N), independent of the magnitude of V^+.
(5) Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.
(6) Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of 15 V, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Copyright © 2000–2015, Texas Instruments Incorporated

Electrical Characteristics: LM124A/224A/324A (continued)

V^+ = 5.0 V, (1), unless otherwise stated

PARAMETER		TEST CONDITIONS		LM124A			LM224A			LM324A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{OS} Drift		R_S = 0 Ω			10	200		10	200		10	300	pA/°C
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$			40	100		40	100		40	200	nA
Input Common-Mode Voltage Range(4)		V^+ = 30 V, (LM2902-N, V^+ = 26 V)		0		V^+−2	0		V^+−2	0		V^+−2	V
Large Signal Voltage Gain		V^+ = 15 V (V_OSwing = 1 V to 11 V), R_L ≥ 2 kΩ		25			25			15			V/mV
Output Voltage Swing	V_{OH}	V^+ = 30 V (LM2902-N, V^+ = 26 V)	R_L = 2 kΩ	26			26			26			V
			R_L = 10 kΩ	27	28		27	28		27	28		
	V_{OL}	V^+ = 5 V, R_L = 10 kΩ			5	20		5	20		5	20	mV
Output Current	Source	V_O = 2 V	V_{IN}^+ = +1V, V_{IN}^- = 0V, V^+ = 15V	10	20		10	20		10	20		mA
	Sink		V_{IN}^- = +1V, V_{IN}^+ = 0V, V^+ = 15V	10	15		5	8		5	8		

6.6 Electrical Characteristics: LM124-N/224-N/324-N/2902-N

V^+ = +5.0V, (1), unless otherwise stated

PARAMETER	TEST CONDITIONS	LM124-N / LM224-N			LM324-N			LM2902-N			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	T_A = 25°C(2)		2	5		2	7		2	7	mV
Input Bias Current(3)	$I_{IN(+)}$ or $I_{IN(-)}$, V_{CM} = 0 V, T_A = 25°C		45	150		45	250		45	250	nA
Input Offset Current	$I_{IN(+)}$ or $I_{IN(-)}$, V_{CM} = 0 V, T_A = 25°C		3	30		5	50		5	50	nA
Input Common-Mode Voltage Range(4)	V^+ = 30 V, (LM2902-N, V^+ = 26V), T_A = 25°C	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	V
Supply Current	Over Full Temperature Range R_L = ∞ On All Op Amps, V^+ = 30 V (LM2902-N V^+ = 26 V)		1.5	3		1.5	3		1.5	3	mA
	V^+ = 5 V		0.7	1.2		0.7	1.2		0.7	1.2	
Large Signal Voltage Gain	V^+ = 15V, R_L≥ 2 kΩ, (V_O = 1 V to 11 V), T_A = 25°C	50	100		25	100		25	100		V/mV
Common-Mode Rejection Ratio	DC, V_{CM} = 0 V to V^+ − 1.5 V, T_A = 25°C	70	85		65	85		50	70		dB
Power Supply Rejection Ratio	V^+ = 5 V to 30 V (LM2902-N, V^+ = 5 V to 26 V), T_A = 25°C	65	100		65	100		50	100		dB
Amplifier-to-Amplifier Coupling(5)	f = 1 kHz to 20 kHz, T_A = 25°C (Input Referred)		−120			−120			−120		dB

(1) These specifications are limited to −55°C ≤ T_A ≤ +125°C for the LM124-N/LM124A. With the LM224-N/LM224A, all temperature specifications are limited to −25°C ≤ T_A ≤ +85°C, the LM324-N/LM324A temperature specifications are limited to 0°C ≤ T_A ≤ +70°C, and the LM2902-N specifications are limited to −40°C ≤ T_A ≤ +85°C.
(2) V_O ≅ 1.4V, R_S = 0 Ω with V^+ from 5 V to 30 V; and over the full input common-mode range (0 V to V^+ − 1.5 V) for LM2902-N, V^+ from 5 V to 26 V.
(3) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
(4) The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3 V (at 25°C). The upper end of the common-mode voltage range is V^+ − 1.5 V (at 25°C), but either or both inputs can go to 32 V without damage (26 V for LM2902-N), independent of the magnitude of V^+.
(5) Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

Copyright © 2000–2015, Texas Instruments Incorporated

Electrical Characteristics: LM124-N/224-N/324-N/2902-N (continued)

V^+ = +5.0V, (1), unless otherwise stated

PARAMETER		TEST CONDITIONS		LM124-N / LM224-N			LM324-N			LM2902-N			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Output Current	Source	V_{IN}^+ = 1 V, V_{IN}^- = 0 V, V^+ = 15 V, V_O = 2 V, T_A = 25°C		20	40		20	40		20	40		mA
	Sink	V_{IN}^- = 1 V, V_{IN}^+ = 0 V, V^+ = 15 V, V_O = 2 V, T_A = 25°C		10	20		10	20		10	20		mA
		V_{IN}^- = 1 V, V_{IN}^+ = 0 V, V^+ = 15 V, V_O = 200 mV, T_A = 25°C		12	50		12	50		12	50		µA
Short Circuit to Ground		V^+ = 15 V, T_A = 25°C (6)			40	60		40	60		40	60	mA
Input Offset Voltage		See (2)				7			9			10	mV
V_{OS} Drift		R_S = 0 Ω			7			7			7		µV/°C
Input Offset Current		$I_{IN(+)} - I_{IN(-)}$, V_{CM} = 0 V				100			150		45	200	nA
I_{OS} Drift		R_S = 0 Ω			10			10			10		pA/°C
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$			40	300		40	500		40	500	nA
Input Common-Mode Voltage Range (4)		V^+ = 30 V, (LM2902-N, V^+ = 26 V)		0		V^+−2	0		V^+−2	0		V^+−2	V
Large Signal Voltage Gain		V^+ = 15 V (V_OSwing = 1V to 11V), R_L ≥ 2 kΩ		25			15			15			V/mV
Output Voltage Swing	V_{OH}	V^+ = 30 V (LM2902-N, V^+ = 26 V)	R_L = 2 kΩ	26			26			22			V
			R_L = 10 kΩ	27	28		27	28		23	24		
	V_{OL}	V^+ = 5 V, R_L = 10 kΩ			5	20		5	20		5	100	mV
Output Current	Source	V_O = 2 V	V_{IN}^+ = 1 V, V_{IN}^- = 0 V, V^+ = 15 V	10	20		10	20		10	20		mA
	Sink		V_{IN}^- = 1 V, V_{IN}^+ = 0 V, V^+ = 15 V	5	8		5	8		5	8		mA

(6) Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of 15 V, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Copyright © 2000–2015, Texas Instruments Incorporated

6.7 Typical Characteristics

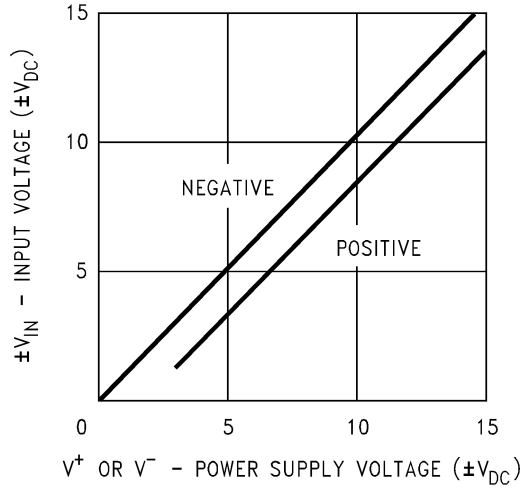


Figure 1. Input Voltage Range

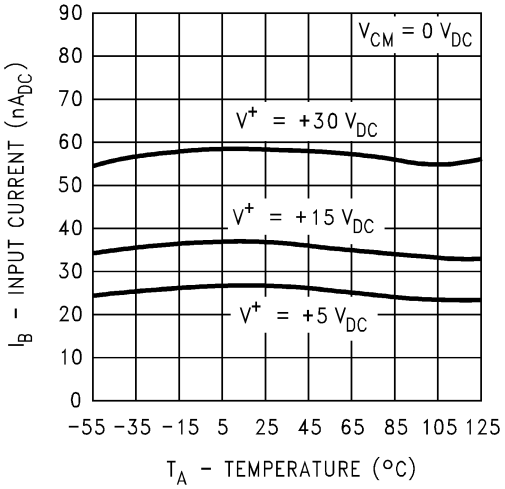


Figure 2. Input Current

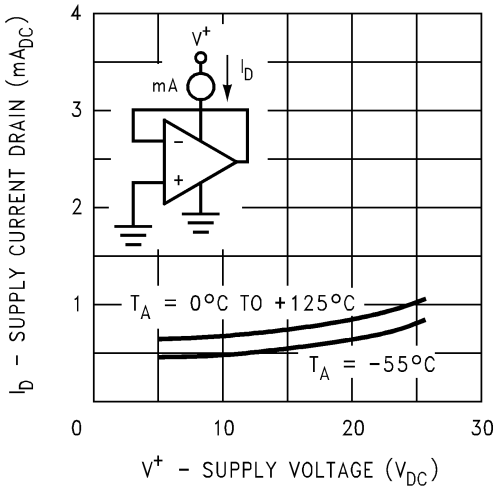


Figure 3. Supply Current

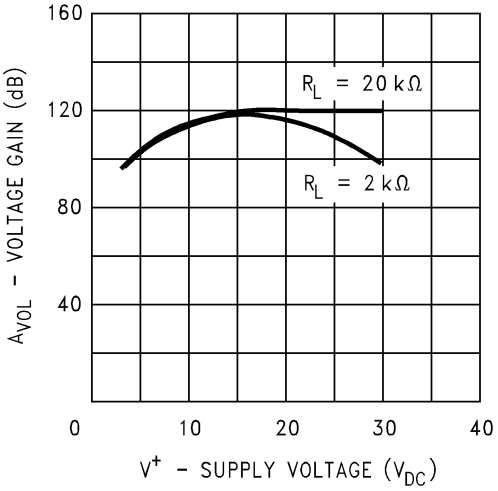


Figure 4. Voltage Gain

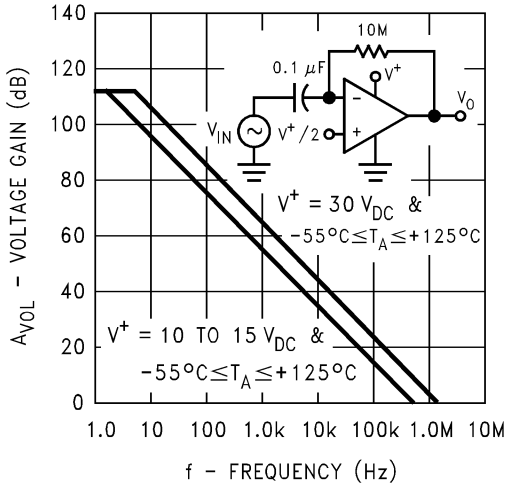


Figure 5. Open-Loop Frequency Response

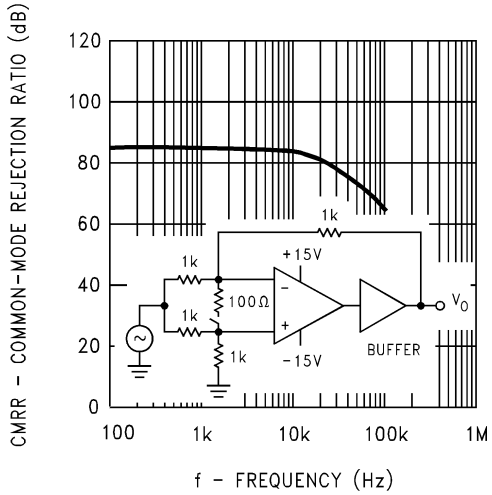


Figure 6. Common Mode Rejection Ratio

Copyright © 2000–2015, Texas Instruments Incorporated

Typical Characteristics (continued)

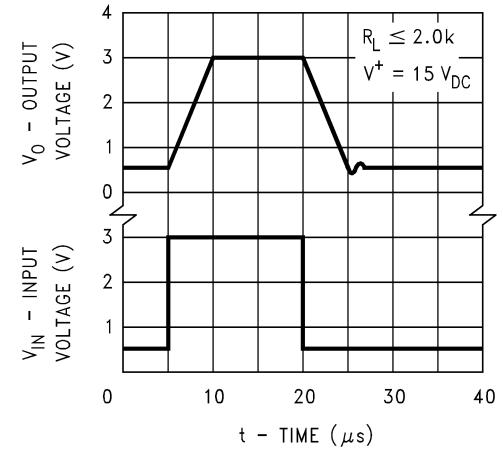


Figure 7. Voltage Follower Pulse Response

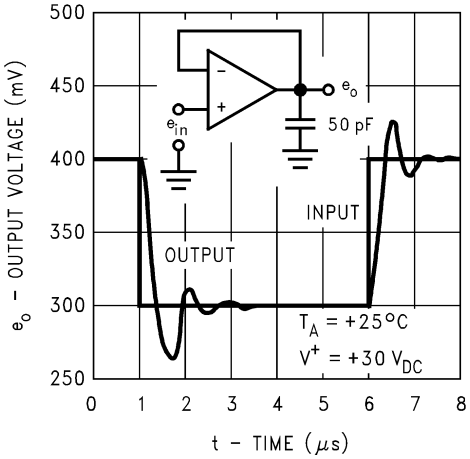


Figure 8. Voltage Follower Pulse Response (Small Signal)

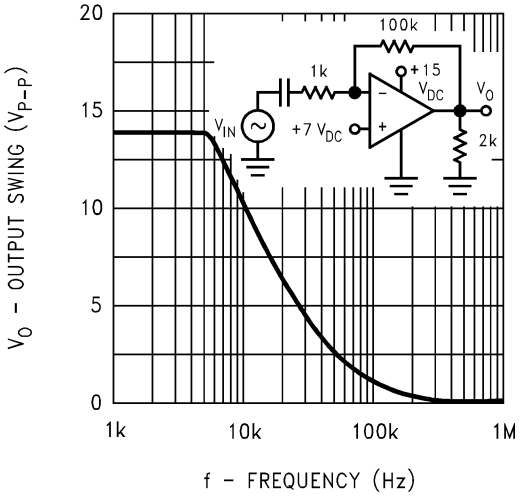


Figure 9. Large Signal Frequency Response

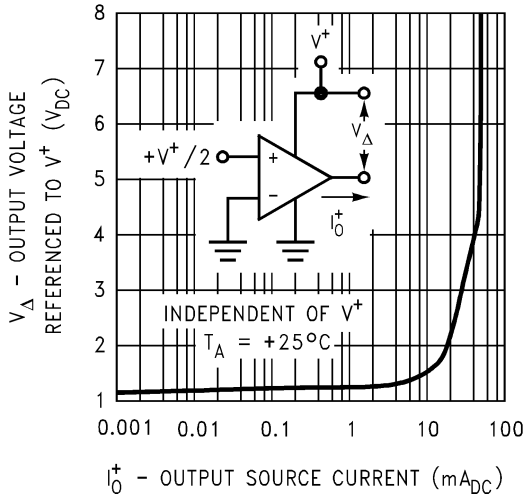


Figure 10. Output Characteristics Current Sourcing

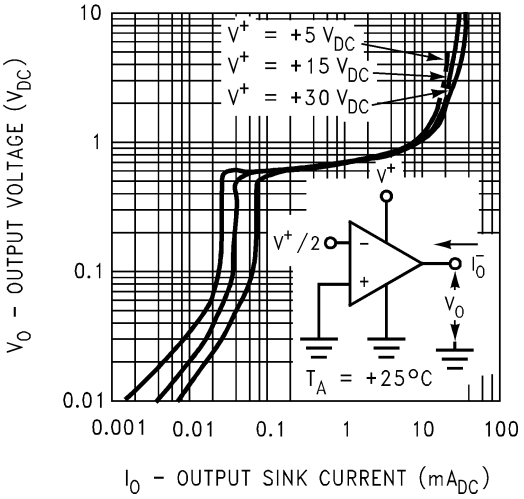


Figure 11. Output Characteristics Current Sinking

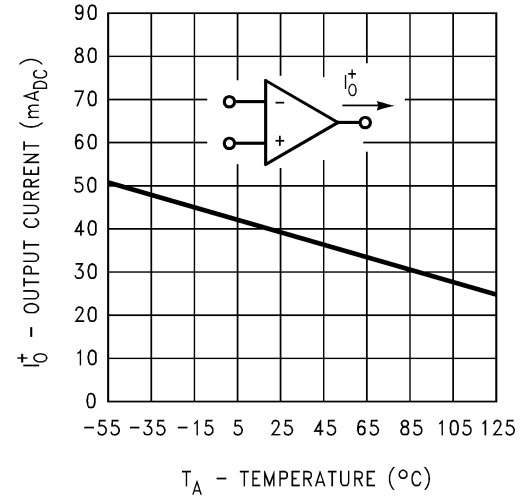


Figure 12. Current Limiting

Typical Characteristics (continued)

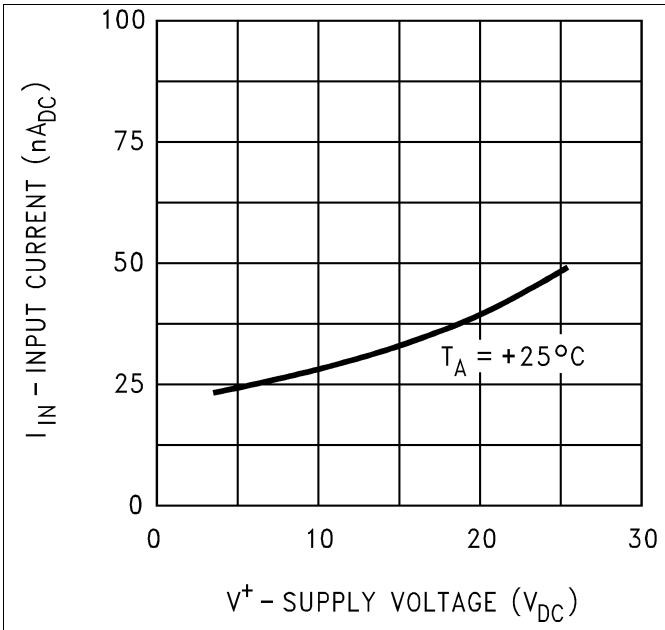


Figure 13. Input Current (LM2902-N Only)

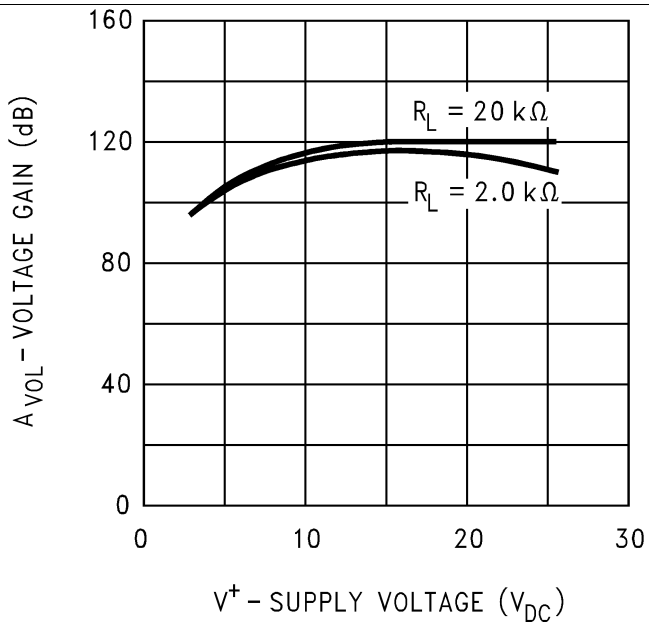


Figure 14. Voltage Gain (LM2902-N Only)

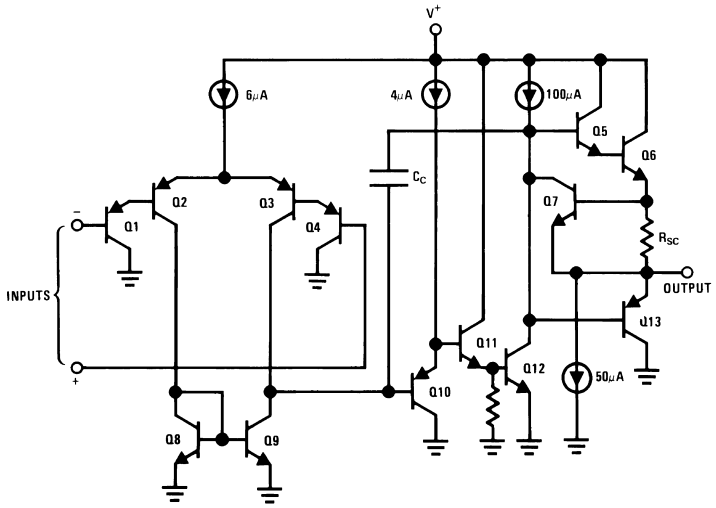
Copyright © 2000–2015, Texas Instruments Incorporated

7 Detailed Description

7.1 Overview

The LM124-N series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC}.

7.2 Functional Block Diagram



7.3 Feature Description

The LM124 provides a compelling balance of performance versus current consumption. The 700 µA of supply current draw over the wide operating conditions with a 1-MHz gain-bandwidth and temperature compensated bias currents makes the LM124 an effective solution for large variety of applications. The input offset voltage of 2 mV and offset current of 5 nA, along with the 45n-A bias current across a wide supply voltage means a single design can be used in a large number of different implementations.

7.4 Device Functional Modes

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion.

Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

Copyright © 2000–2015, Texas Instruments Incorporated

Device Functional Modes (continued)

The bias network of the LM124-N establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 3 V_{DC} to 30 V_{DC}.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see *Typical Characteristics*) than a standard IC op amp.

Copyright © 2000–2015, Texas Instruments Incorporated

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

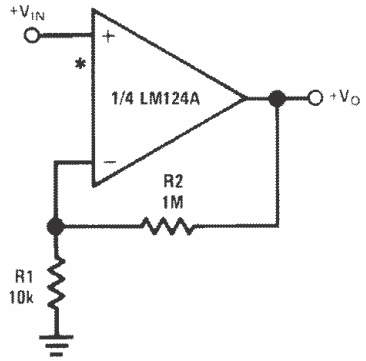
8.1 Application Information

The LM124 series of amplifiers is specified for operation from 3 V to 32 V (±1.5 V to ±16 V). Many of the specifications apply from –40°C to 125°C. Parameters that can exhibit significant variance with regards to operating voltage or temperature are presented in *Typical Characteristics*.

8.2 Typical Applications

Figure 15 emphasizes operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

8.2.1 Non-Inverting DC Gain (0 V Input = 0 V Output)



*R not needed due to temperature independent I_{IN}

Figure 15. Non-Inverting Amplifier with G=100

8.2.1.1 Design Requirements

For this example application, the required signal gain is a non-inverting 100x±5% with a supply voltage of 5 V.

8.2.1.2 Detailed Design Procedure

Using the equation for a non-inverting gain configuration, Av = 1+R2/R1. Setting the R1 to 10 kΩ, R2 is 99 times larger than R1, which is 990 kΩ. A 1MΩ is more readily available, and provides a gain of 101, which is within the desired specification.

The gain-frequency characteristic of the amplifier and its feedback network must be such that oscillation does not occur. To meet this condition, the phase shift through amplifier and feedback network must never exceed 180° for any frequency where the gain of the amplifier and its feedback network is greater than unity. In practical applications, the phase shift should not approach 180° since this is the situation of conditional stability. Obviously the most critical case occurs when the attenuation of the feedback network is zero.

Copyright © 2000–2015, Texas Instruments Incorporated

Typical Applications (continued)

8.2.1.3 Application Curve

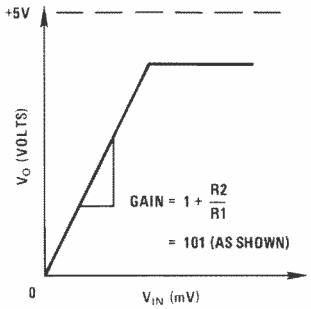
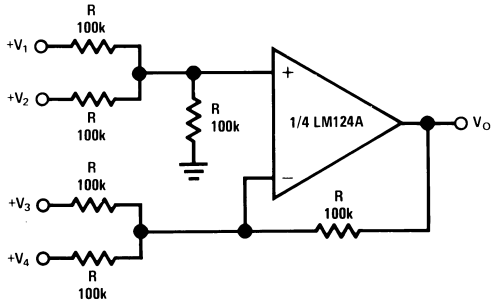


Figure 16. Non-Inverting Amplified Response Curve

Copyright © 2000–2015, Texas Instruments Incorporated

Typical Applications (continued)

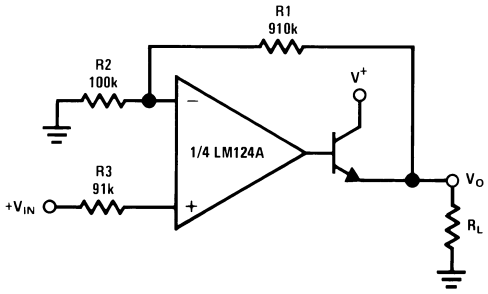
8.2.2 Other Application Circuits at $V^+ = 5.0\ V_{DC}$



Where: $V_0 = V_1 + V_2 - V_3 - V_4$

$(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O > 0\ V_{DC}$

Figure 17. DC Summing Amplifier ($V_{IN'S} \geq 0\ V_{DC}$ And $V_O \geq V_{DC}$)



Where: $V_0 = 0\ V_{DC}$ for $V_{IN} = 0\ V_{DC}$

$A_V = 10$

Figure 18. Power Amplifier

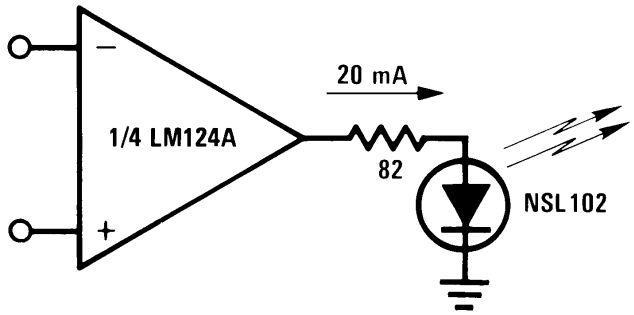
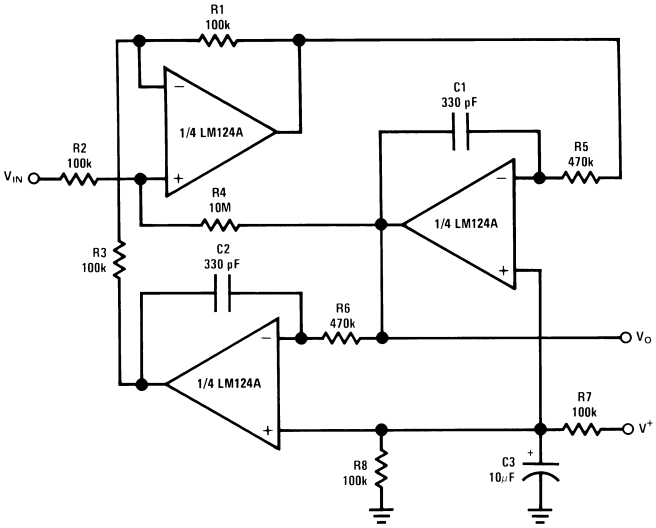


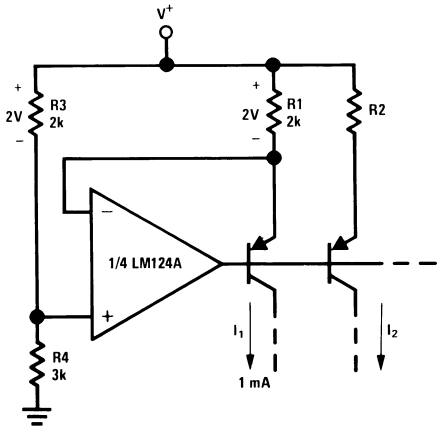
Figure 19. LED Driver



$f_0 = 1$ kHz Q = 50 $A_V = 100$ (40 dB)

Figure 20. "BI-QUAD" RC Active Bandpass Filter

Typical Applications (continued)



$$I_2 = \left(\frac{R1}{R2}\right) I_1$$

Figure 21. Fixed Current Sources

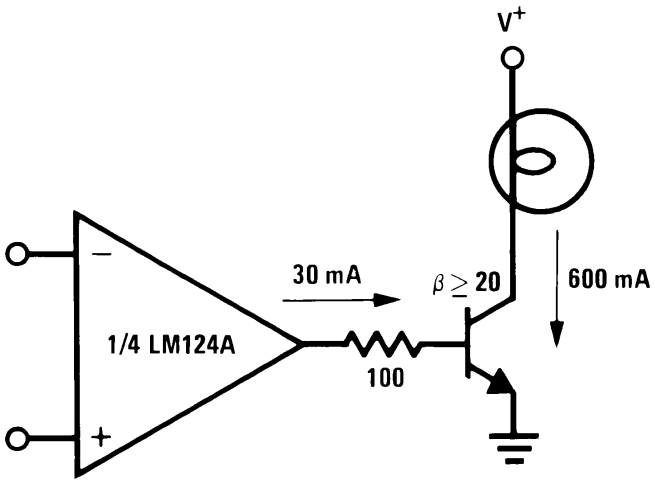
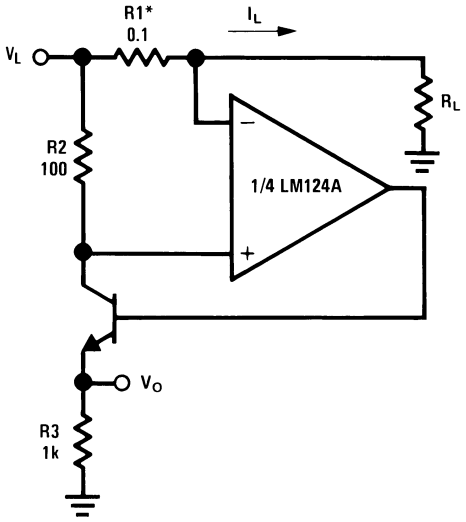


Figure 22. Lamp Driver



*(Increase R1 for I_L small)

Figure 23. Current Monitor

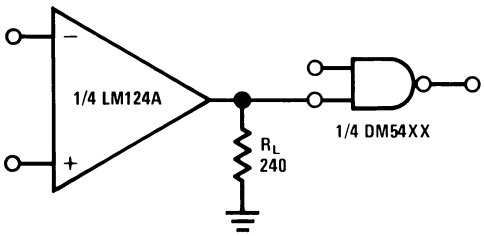


Figure 24. Driving TTL

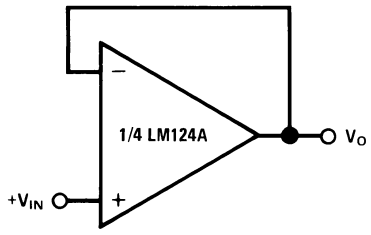


Figure 25. Voltage Follower

Copyright © 2000–2015, Texas Instruments Incorporated

Typical Applications (continued)

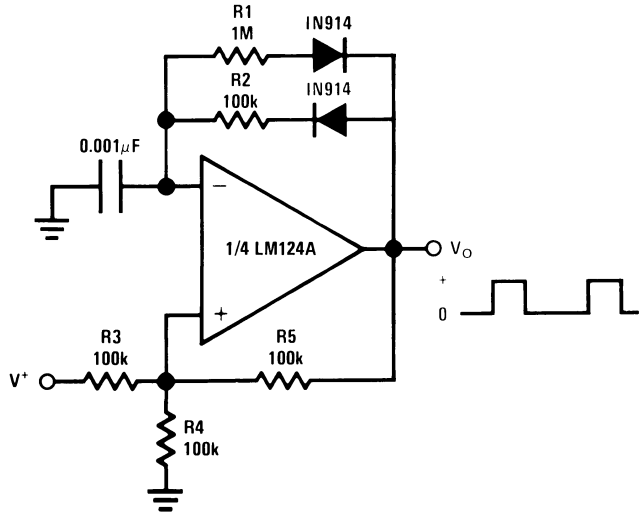


Figure 26. Pulse Generator

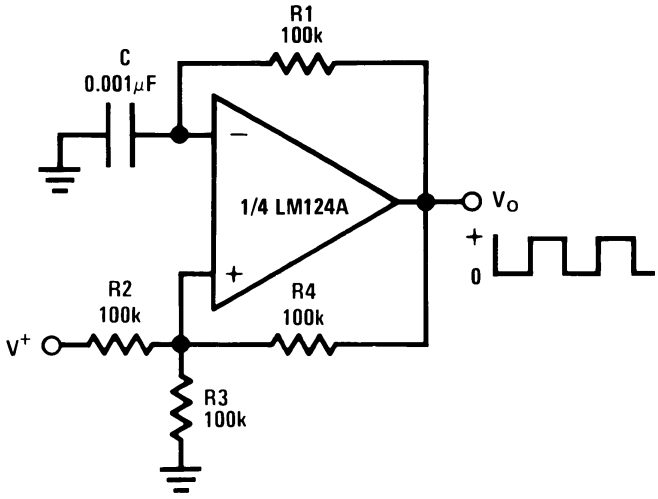


Figure 27. Squarewave Oscillator

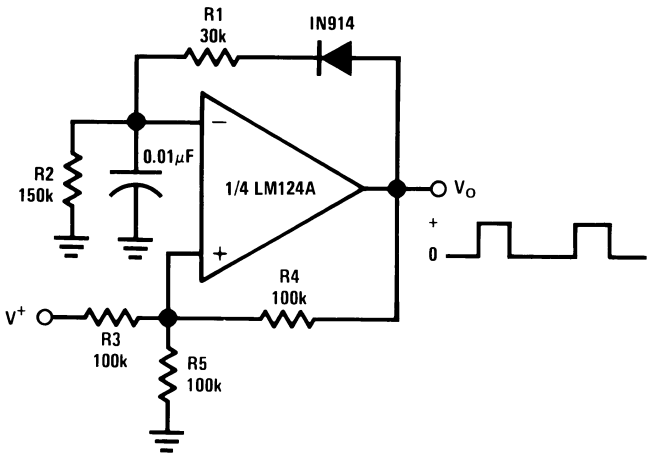
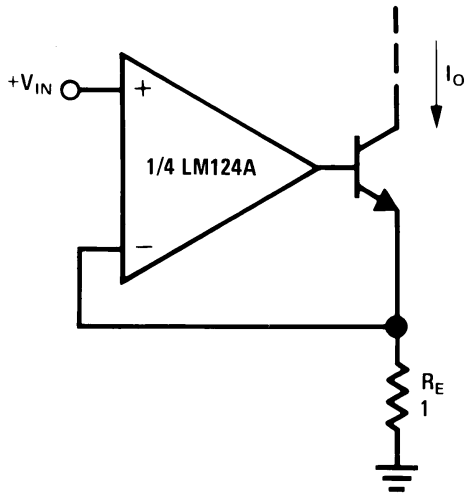


Figure 28. Pulse Generator



I_O = 1 amp/volt V_{IN} (Increase R_E for I_o small)

Figure 29. High Compliance Current Sink

Typical Applications (continued)

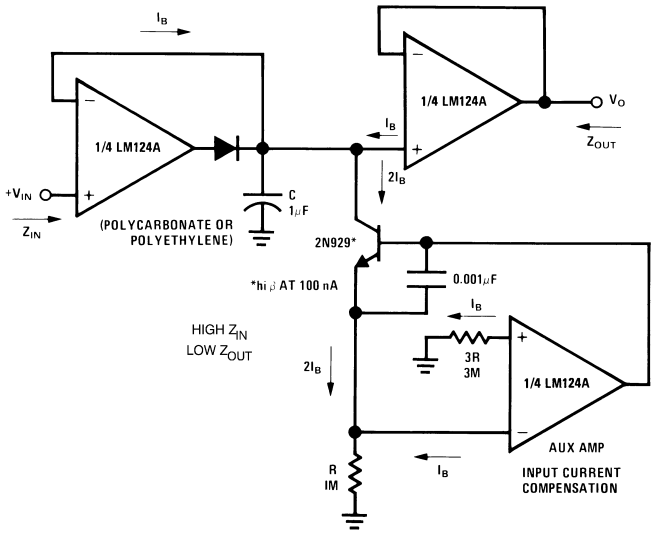


Figure 30. Low Drift Peak Detector

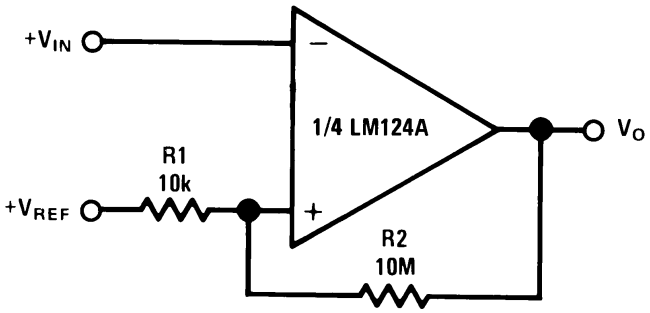
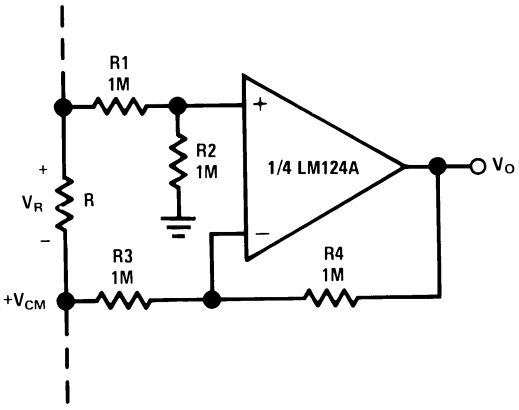
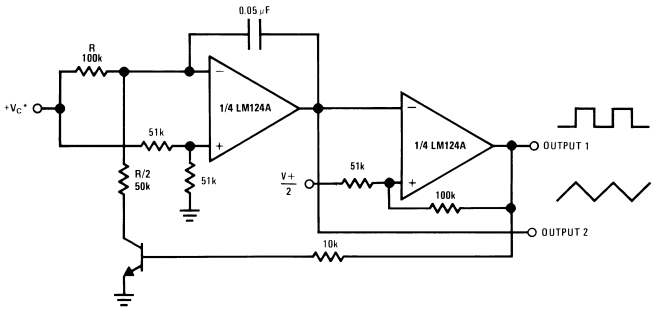


Figure 31. Comparator With Hysteresis



$V_O = V_R$

Figure 32. Ground Referencing a Differential Input Signal

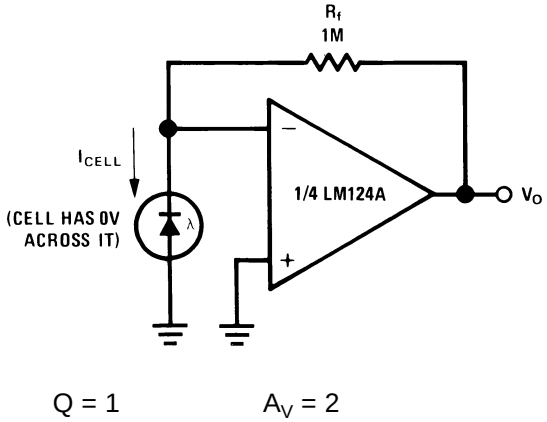


*Wide control voltage range:
0 V_{DC} ≤ V_C ≤ 2 (V^+ −1.5 V_{DC})

Figure 33. Voltage Controlled Oscillator Circuit

Copyright © 2000–2015, Texas Instruments Incorporated

Typical Applications (continued)



Q = 1 A_V = 2

Figure 34. Photo Voltaic-Cell Amplifier

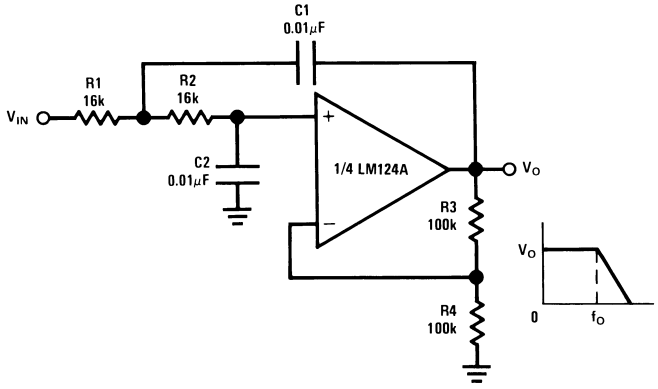
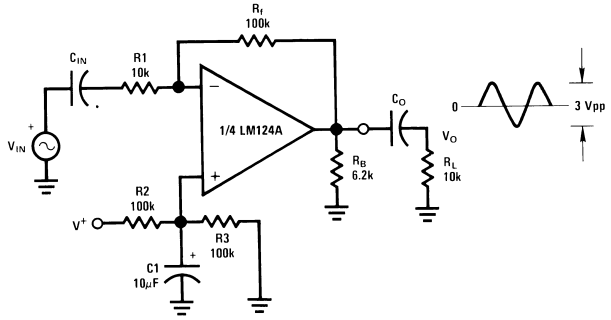
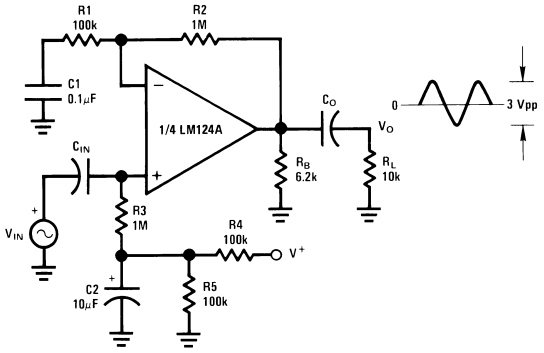


Figure 35. DC Coupled Low-Pass RC Active Filter



$$A_V = \frac{R_f}{R1} \text{ (As shown, } A_V = 10)$$

Figure 36. AC Coupled Inverting Amplifier

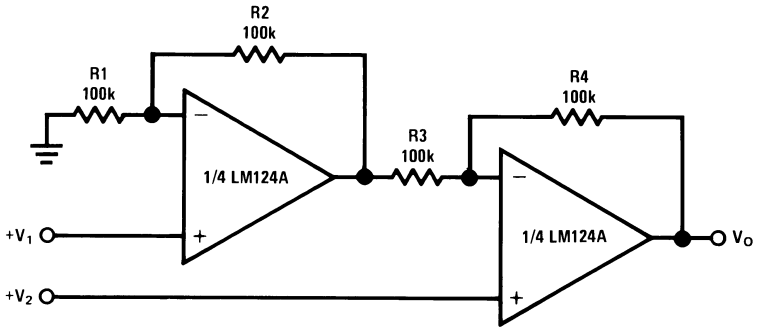


$$A_V = 1 + \frac{R2}{R1}$$

A_V = 11 (As shown)

Figure 37. AC Coupled Non-Inverting Amplifier

Typical Applications (continued)

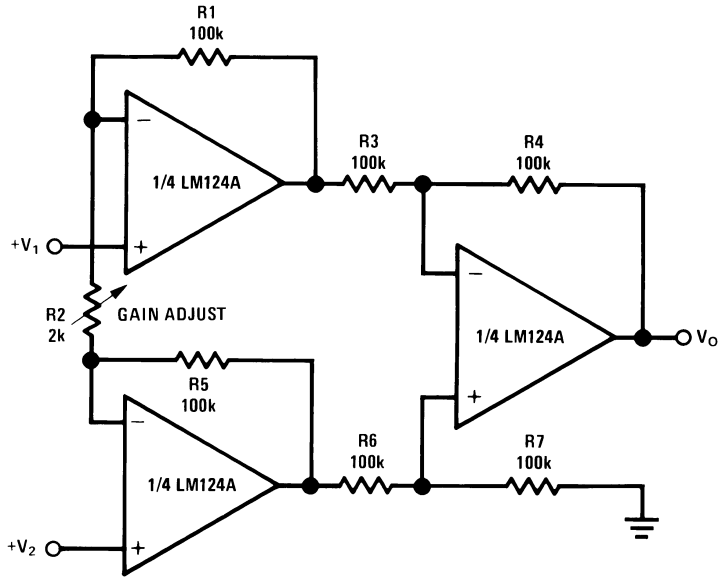


For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

$V_O = 1 + \frac{R4}{R3}(V_2 - V_1)$

As shown: $V_O = 2(V_2 - V_1)$

Figure 38. High Input Z, DC Differential Amplifier



If R1 = R5 & R3 = R4 = R6 = R7 (CMRR depends on match)

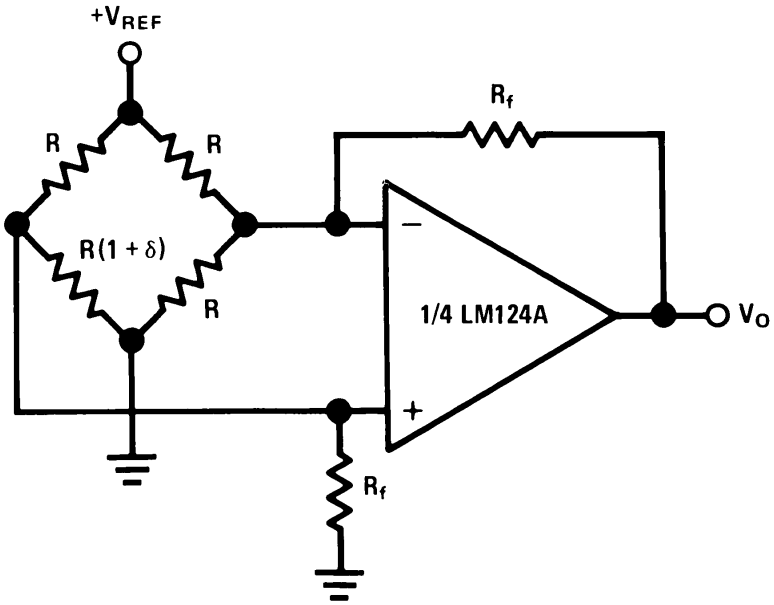
$V_O = 1 + \frac{2R1}{R2}(V_2 - V_1)$

As shown $V_O = 101\,(V_2 - V_1)$

Figure 39. High Input Z Adjustable-Gain DC Instrumentation Amplifier

Copyright © 2000–2015, Texas Instruments Incorporated

Typical Applications (continued)



For $\delta << 1$ and $R_f >> R$

$$V_O \cong V_{REF}\left(\frac{\delta}{2}\right)\frac{R_f}{R}$$

Figure 40. Bridge Current Amplifier

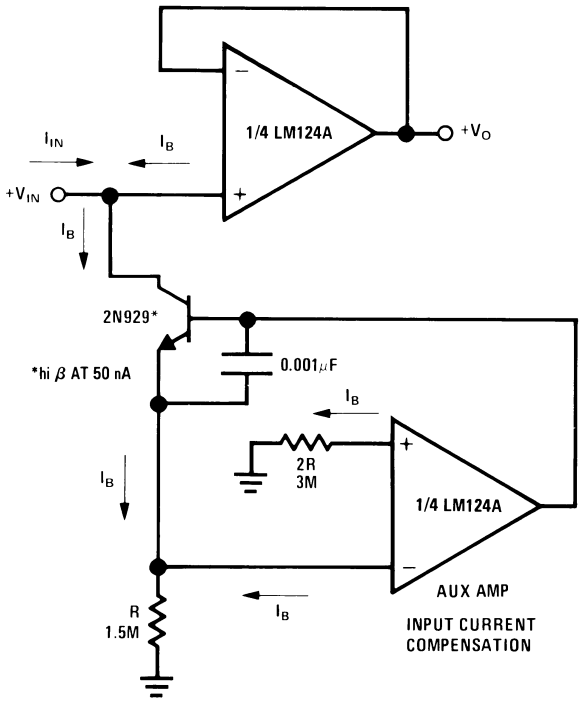
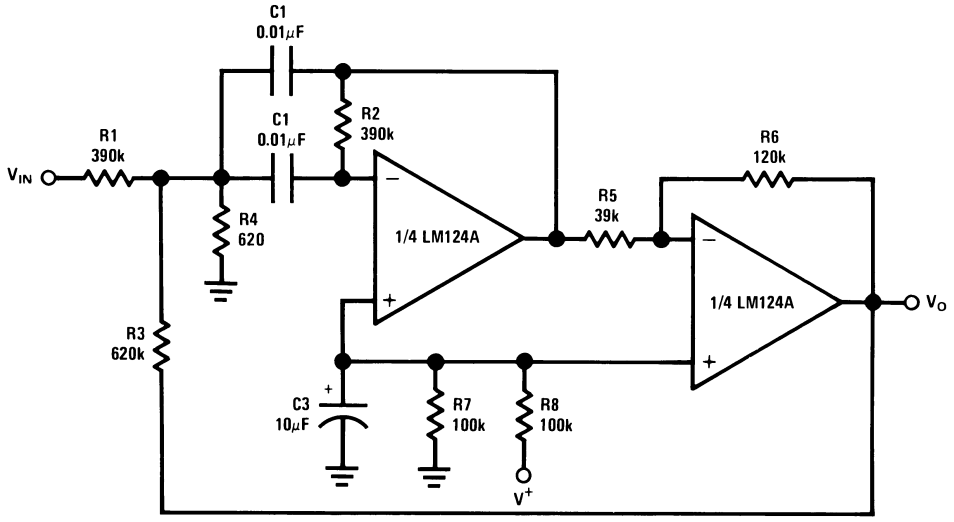


Figure 41. Using Symmetrical Amplifiers to Reduce Input Current (General Concept)

Typical Applications (continued)



f_O = 1 kHz Q = 25

Figure 42. Bandpass Active Filter

Copyright © 2000–2015, Texas Instruments Incorporated

9 Power Supply Recommendations

The pinouts of the package have been designed to simplify PC board layouts. Inverting inputs are adjacent to outputs for all of the amplifiers and the outputs have also been placed at the corners of the package (pins 1, 7, 8, and 14).

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

10 Layout

10.1 Layout Guidelines

The V + pin should be bypassed to ground with a low-ESR capacitor. The optimum placement is closest to the V + and ground pins.

Take care to minimize the loop area formed by the bypass capacitor connection between V + and ground.

The ground pin should be connected to the PCB ground plane at the pin of the device.

The feedback components should be placed as close to the device as possible minimizing strays.

10.2 Layout Example

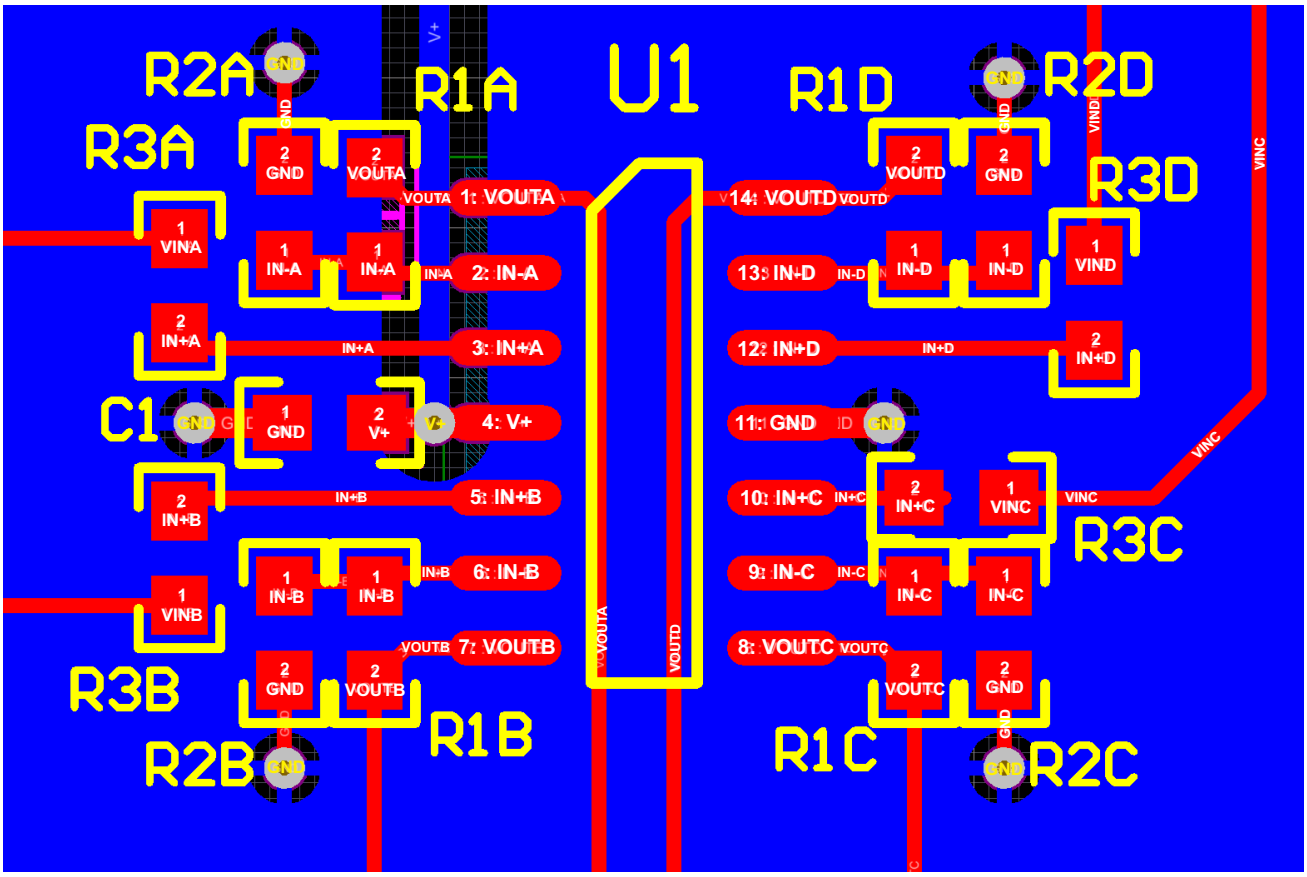


Figure 43. Layout Example

11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM124-N	Click here	Click here	Click here	Click here	Click here
LM224-N	Click here	Click here	Click here	Click here	Click here
LM2902-N	Click here	Click here	Click here	Click here	Click here
LM324-N	Click here	Click here	Click here	Click here	Click here

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2000–2015, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM124AJ/PB	Active	Production	CDIP (J) | 14	25 | TUBE	No	Call TI	Call TI	-55 to 125	LM124AJ
LM124J/PB	Active	Production	CDIP (J) | 14	25 | TUBE	No	Call TI	Call TI	-55 to 125	LM124J
LM224J	Active	Production	CDIP (J) | 14	25 | TUBE	No	Call TI	Call TI	-25 to 85	LM224J
LM2902M/NOPB	Active	Production	SOIC (D) | 14	55 | TUBE	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	LM2902M
LM2902M/NOPB.B	Active	Production	SOIC (D) | 14	55 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM2902M
LM2902MT/NOPB	Active	Production	TSSOP (PW) | 14	94 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM290 2MT
LM2902MT/NOPB.B	Active	Production	TSSOP (PW) | 14	94 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM290 2MT
LM2902MTX/NOPB	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM290 2MT
LM2902MTX/NOPB.B	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM290 2MT
LM2902MX/NOPB	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	LM2902M
LM2902MX/NOPB.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM2902M
LM2902N/NOPB	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	Call TI | Nipdau	Level-1-NA-UNLIM	-40 to 85	LM2902N
LM2902N/NOPB.B	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LM2902N
LM324AM/NOPB	Active	Production	SOIC (D) | 14	55 | TUBE	Yes	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	LM324AM
LM324AM/NOPB.B	Active	Production	SOIC (D) | 14	55 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324AM
LM324AMX/NOPB	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	LM324AM
LM324AMX/NOPB.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324AM
LM324AN/NOPB	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	0 to 70	LM324AN
LM324AN/NOPB.B	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	0 to 70	LM324AN
LM324M/NOPB	Active	Production	SOIC (D) | 14	55 | TUBE	Yes	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	LM324M
LM324M/NOPB.B	Active	Production	SOIC (D) | 14	55 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324M
LM324MT/NOPB	Active	Production	TSSOP (PW) | 14	94 | TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM324 MT
LM324MT/NOPB.B	Active	Production	TSSOP (PW) | 14	94 | TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM324 MT
LM324MTX/NOPB	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM324 MT

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM324MTX/NOPB.B	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM324 MT
LM324MX/NOPB	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	LM324M
LM324MX/NOPB.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324M
LM324N/NOPB	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	Call TI | Nipdau	Level-1-NA-UNLIM	0 to 70	LM324N
LM324N/NOPB.B	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	0 to 70	LM324N

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LM124-N, LM2902-N :

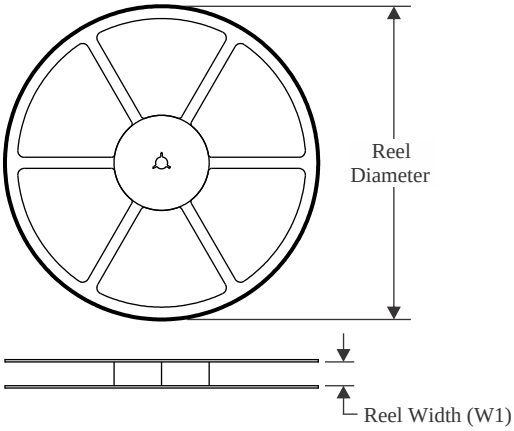
- Automotive : LM2902-Q1
- Enhanced Product : LM2902-EP
- Space : LM124-SP

NOTE: Qualified Version Definitions:

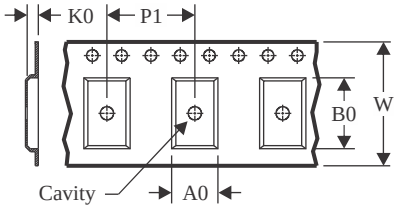
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

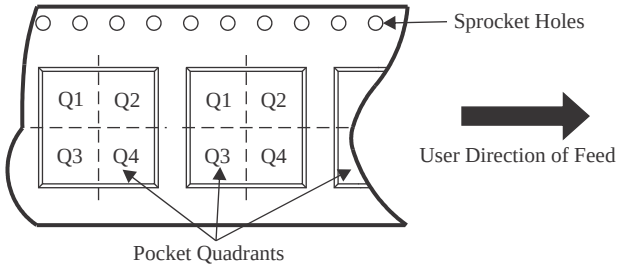


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

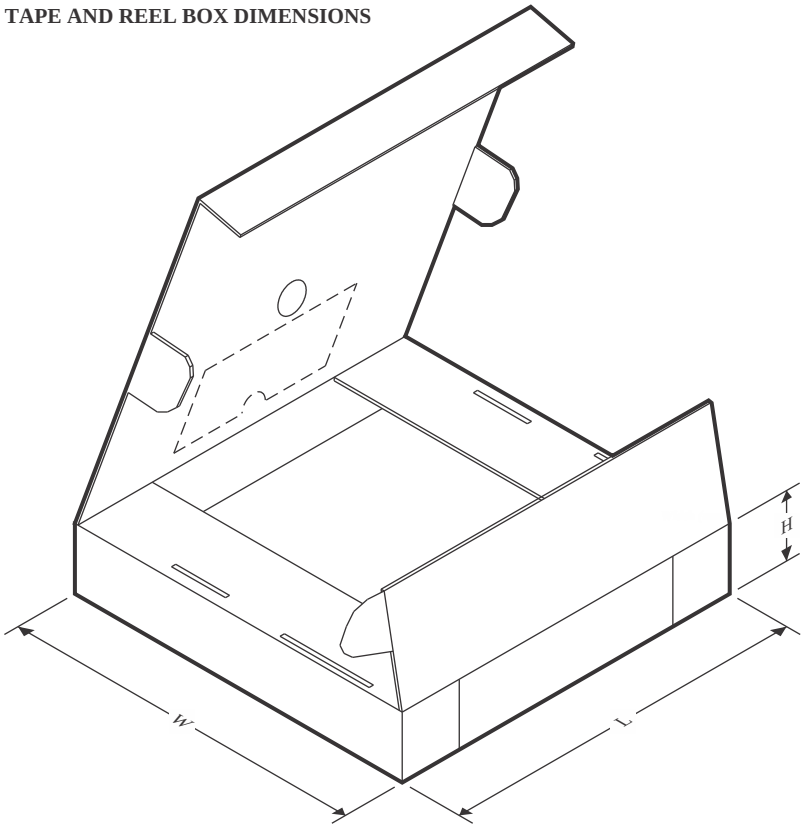
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2902MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2902MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LM324AMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LM324MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM324MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

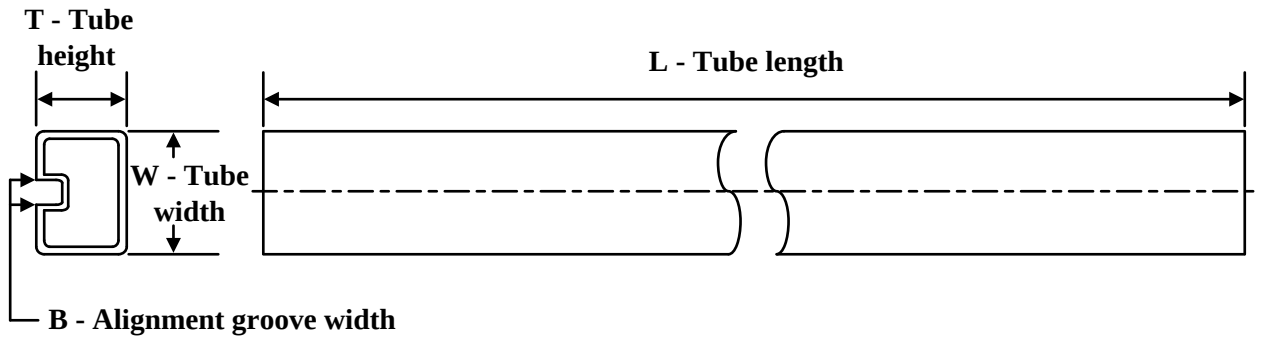
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

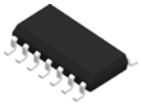
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2902MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0
LM2902MX/NOPB	SOIC	D	14	2500	356.0	356.0	35.0
LM324AMX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
LM324MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0
LM324MX/NOPB	SOIC	D	14	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM124AJ/PB	J	CDIP	14	25	502	14	11938	4.32
LM124J/PB	J	CDIP	14	25	502	14	11938	4.32
LM224J	J	CDIP	14	25	502	14	11938	4.32
LM2902M/NOPB	D	SOIC	14	55	495	8	4064	3.05
LM2902M/NOPB.B	D	SOIC	14	55	495	8	4064	3.05
LM2902MT/NOPB	PW	TSSOP	14	94	495	8	2514.6	4.06
LM2902MT/NOPB.B	PW	TSSOP	14	94	495	8	2514.6	4.06
LM2902N/NOPB	N	PDIP	14	25	502	14	11938	4.32
LM2902N/NOPB.B	N	PDIP	14	25	502	14	11938	4.32
LM324AM/NOPB	D	SOIC	14	55	495	8	4064	3.05
LM324AM/NOPB.B	D	SOIC	14	55	495	8	4064	3.05
LM324AN/NOPB	N	PDIP	14	25	502	14	11938	4.32
LM324AN/NOPB.B	N	PDIP	14	25	502	14	11938	4.32
LM324M/NOPB	D	SOIC	14	55	495	8	4064	3.05
LM324M/NOPB.B	D	SOIC	14	55	495	8	4064	3.05
LM324MT/NOPB	PW	TSSOP	14	94	495	8	2514.6	4.06
LM324MT/NOPB.B	PW	TSSOP	14	94	495	8	2514.6	4.06
LM324N/NOPB	N	PDIP	14	25	502	14	11938	4.32
LM324N/NOPB.B	N	PDIP	14	25	502	14	11938	4.32

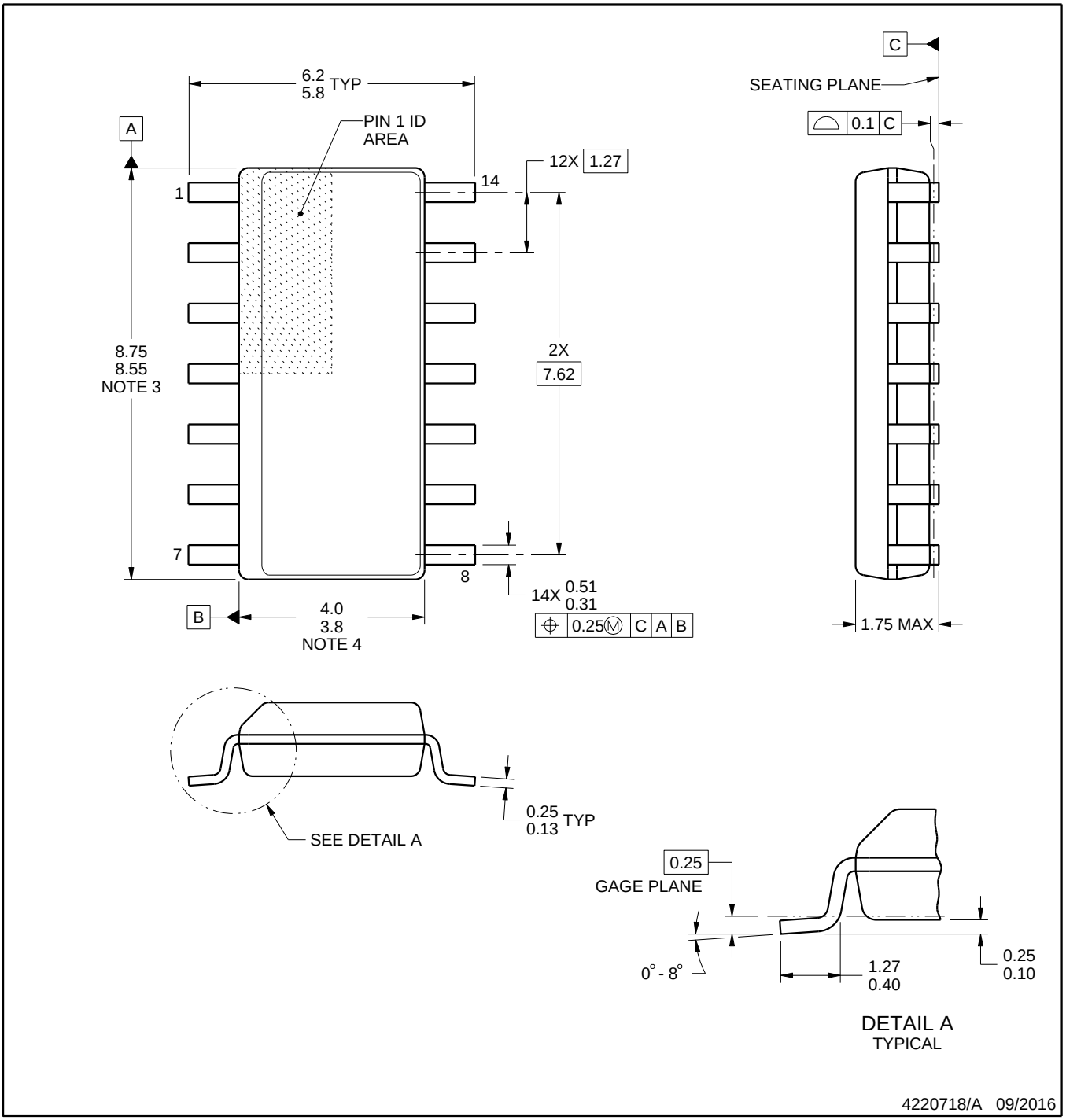


PACKAGE OUTLINE

D0014A

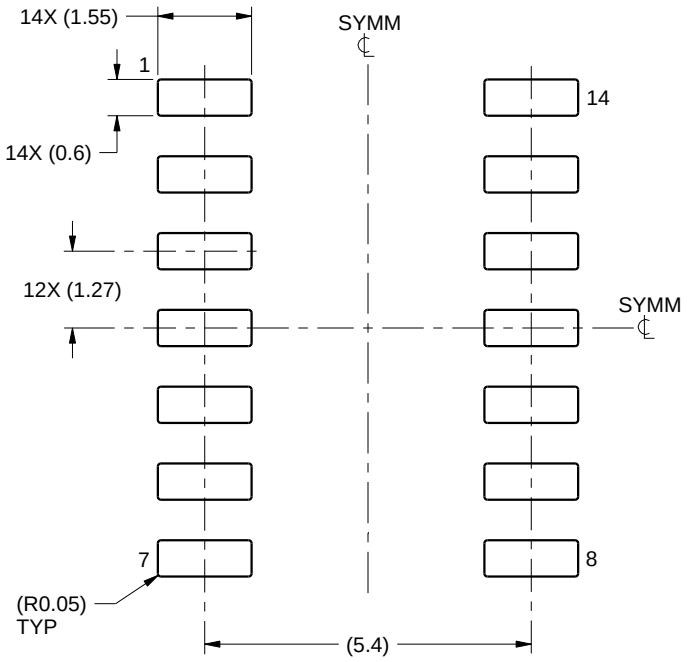
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

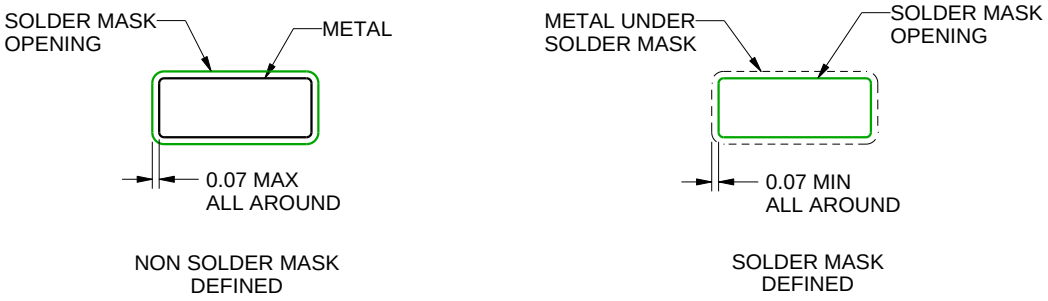


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

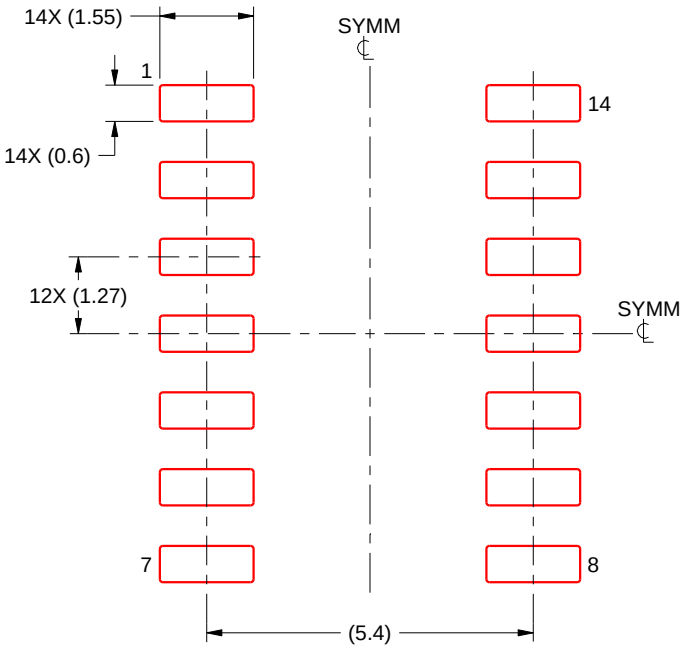
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

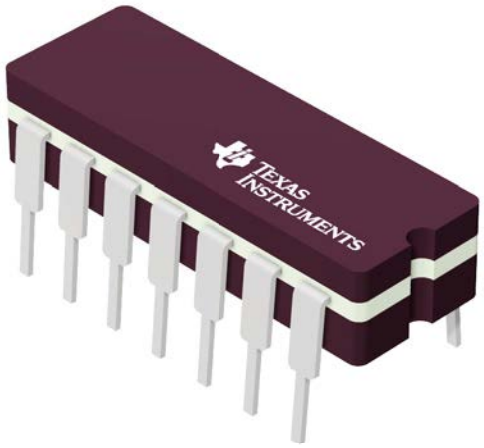
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

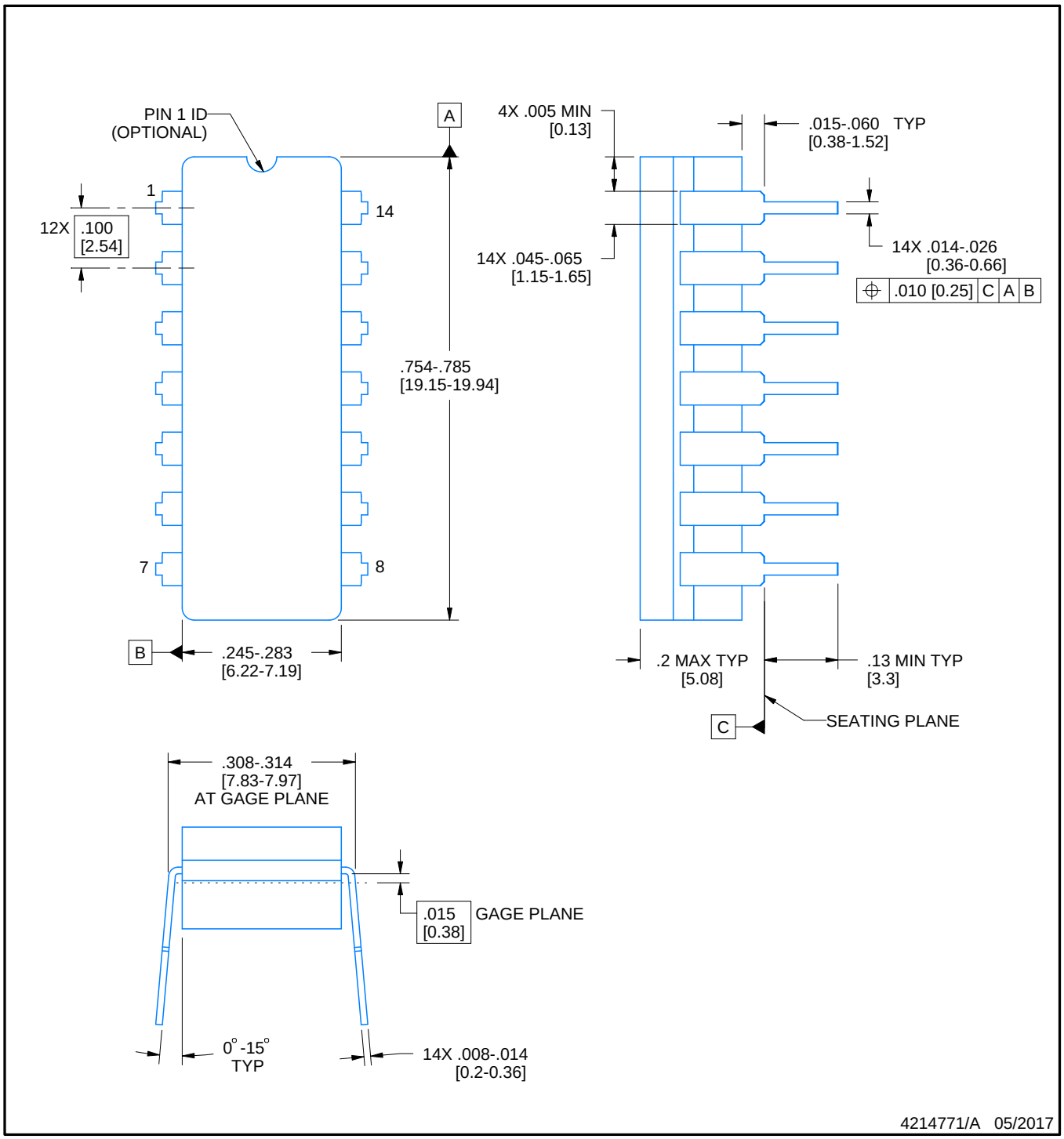
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

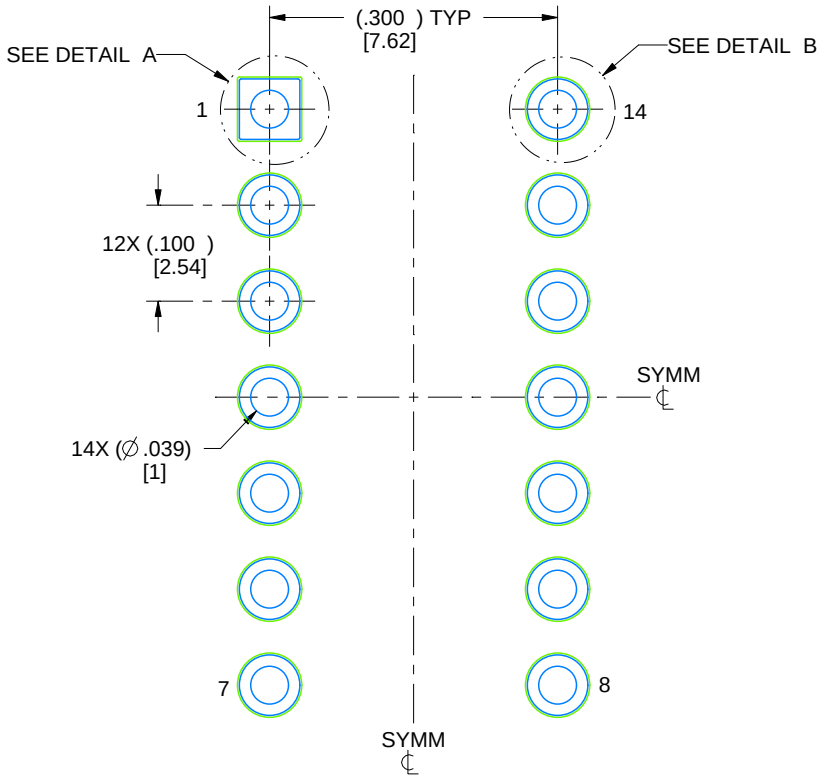
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

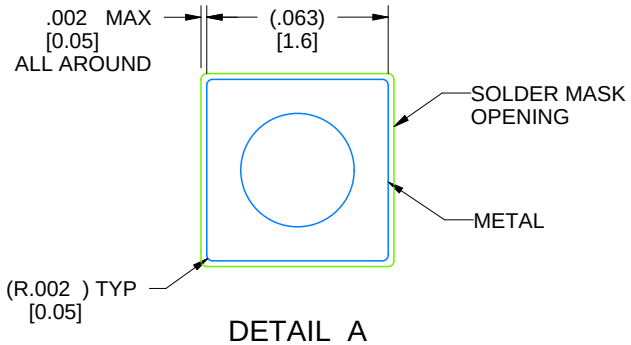
J0014A

CDIP - 5.08 mm max height

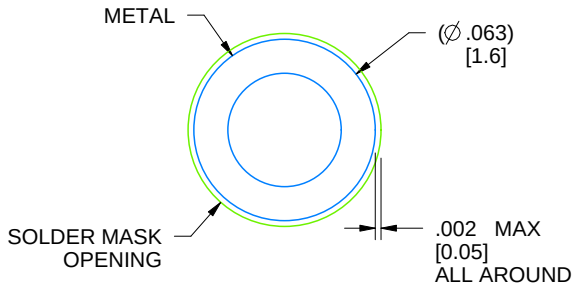
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



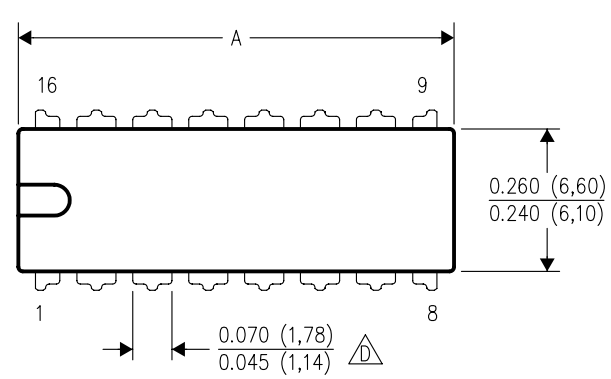
DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

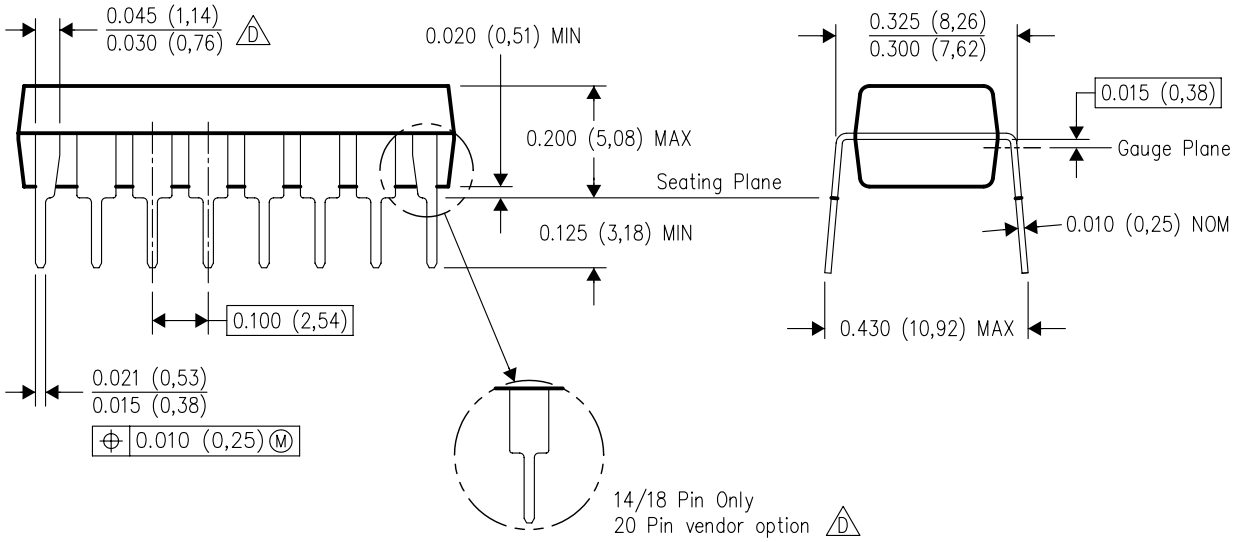
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

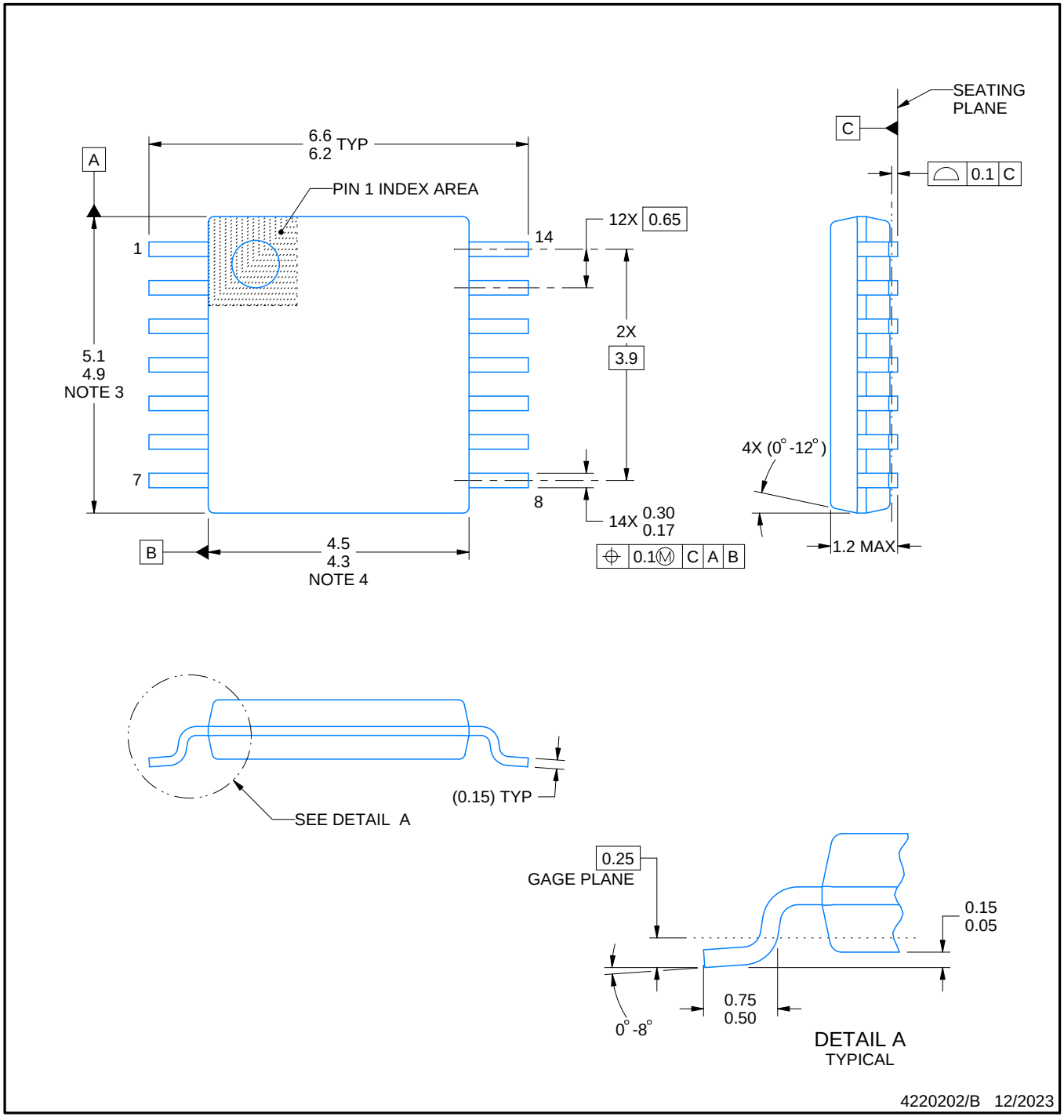
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0014A

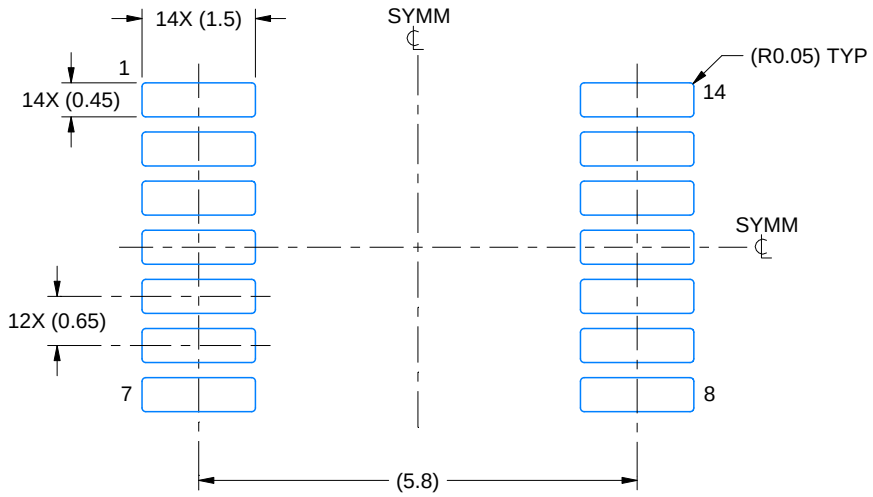
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

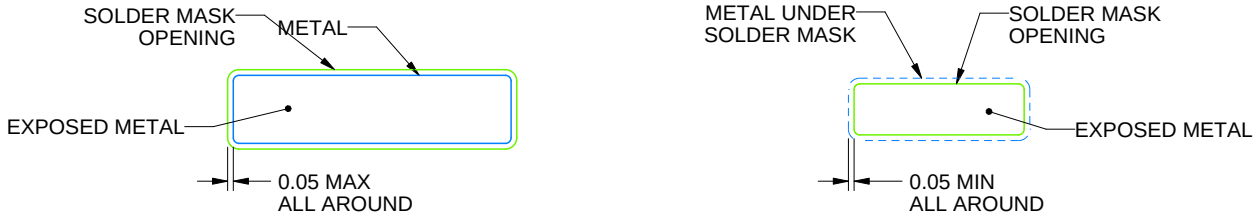


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

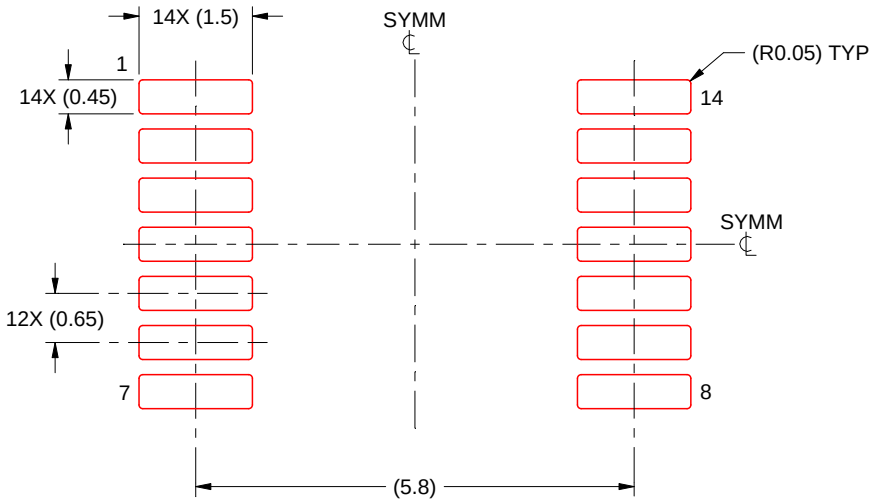


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025