

LM2902-Q1, LM2902B-Q1, and LM2902BA-Q1 Industry-Standard Quad Operational Amplifiers for Automotive Applications

1 Features

- AEC Q-100 qualified for automotive applications
 - Temperature grade 1: –40°C to +125°C
 - Device HBM ESD classification 2
 - Device CDM ESD classification C5
- Wide supply range of:
 - 3V to 36V (LM2902B-Q1 and LM2902BA-Q1)
 - 3V to 32V (LM2902KV and LM2902KAV)
 - 3V to 26V (all other products)
- Input offset voltage maximum at 25°C of:
 - 2mV (LM2902BA-Q1 and LM2902KAV)
 - 3mV (LM2902B-Q1)
 - 7mV (all other products)
- Internal RF and EMI filter (LM2902B-Q1 and LM2902BA-Q1)
- Supply-current of 175µA per channel, typical
- Unity-gain bandwidth of 1.2MHz
- Common-mode input voltage range includes V–
- Differential input voltage range equal to maximum-rated supply voltage

2 Applications

- Automotive lighting
- Body electronics
- Automotive head unit
- Telematics control unit
- Emergency call (eCall)
- Passive safety: brake system
- Electric vehicle / hybrid electric:
 - Inverter and motor control
 - On-board (OBC) and wireless charger
 - Battery management system (BMS)

3 Description

The LM2902-Q1, LM2902B-Q1, and LM2902BA-Q1 are industry-standard operational amplifiers that have been qualified for automotive use in accordance to the AEC-Q100 specifications. The LM2902B-Q1 and LM2902BA-Q1 are the next-generation versions of the LM2902-Q1, which include four high-voltage (36V) operational amplifiers (op amps). The LM2902B-Q1 and LM2902BA-Q1 provide outstanding value for cost-sensitive applications, with features including low offset (3mV and 2mV maximum, respectively), common-mode input range to ground, and high differential input voltage capability.

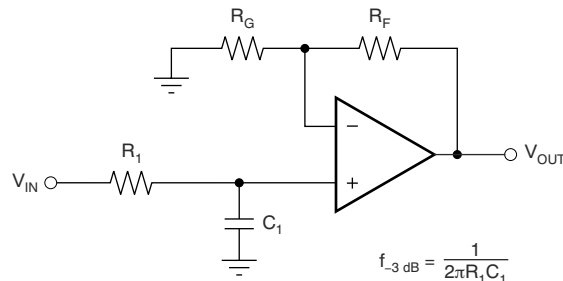
The LM2902B-Q1 and LM2902BA-Q1 simplify circuit design with enhanced features such as unity-gain stability, lower offset voltage of 0.3mV (typical), and lower quiescent current of 240µA (typical). High ESD (1kV, HBM) and integrated EMI and RF filters enable the LM2902B-Q1 and LM2902BA-Q1 devices to be used in the most rugged, environmentally challenging applications for the automotive marketplace.

Device Information

PART NUMBER ⁽¹⁾	CHANNEL COUNT	PACKAGE	PACKAGE SIZE ⁽²⁾
LM2902B-Q1	Quad	D (SOIC, 14)	8.65mm × 6mm
		PW (TSSOP, 14)	5mm × 6.4mm
		RTE (WQFN, 16)	3mm × 3mm
LM2902BA-Q1	Quad	D (SOIC, 14)	8.65mm × 6mm
		PW (TSSOP, 14)	5mm × 6.4mm
LM2902-Q1	Quad	D (SOIC, 14)	8.65mm × 6mm
		PW (TSSOP, 14)	5mm × 6.4mm

(1) For more information, see [Section 11](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right) \left(\frac{1}{1 + sR_1C_1}\right)$$

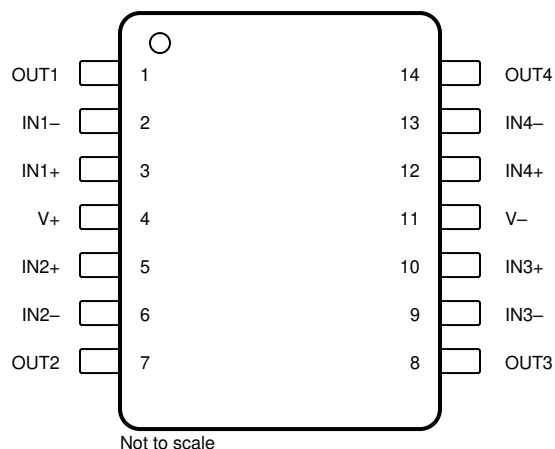
Single-Pole, Low-Pass Filter



Table of Contents

1 Features	1	7.2 Functional Block Diagram.....	18
2 Applications	1	7.3 Feature Description.....	18
3 Description	1	7.4 Device Functional Modes.....	19
4 Pin Configurations and Functions	3	8 Application and Implementation	20
5 Specifications	5	8.1 Application Information.....	20
5.1 Absolute Maximum Ratings.....	5	8.2 Typical Application.....	20
5.2 ESD Ratings.....	5	8.3 Power Supply Recommendations.....	21
5.3 Recommended Operating Conditions.....	5	8.4 Layout.....	21
5.4 Thermal Information.....	6	9 Device and Documentation Support	23
5.5 Electrical Characteristics - LM2902B-Q1 and LM2902BA-Q1.....	7	9.1 Documentation Support.....	23
5.6 Electrical Characteristics: LM2902-Q1, LM2902KV-Q1, LM2902KAV-Q1.....	9	9.2 Receiving Notification of Documentation Updates.....	23
5.7 Operating Conditions: LM2902-Q1, LM2902KV- Q1, LM2902KAV-Q1.....	10	9.3 Support Resources.....	23
5.8 Typical Characteristics.....	11	9.4 Trademarks.....	23
6 Parameter Measurement Information	17	9.5 Electrostatic Discharge Caution.....	23
7 Detailed Description	18	9.6 Glossary.....	23
7.1 Overview.....	18	10 Revision History	23
		11 Mechanical, Packaging, and Orderable Information	24

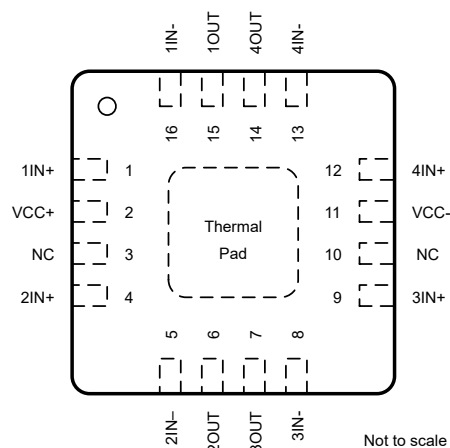
4 Pin Configurations and Functions



**Figure 4-1. D and PW Package
14-Pin SOIC and TSSOP
(Top View)**

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
IN1–	2	Input	Inverting input, channel 1
IN1+	3	Input	Noninverting input, channel 1
IN2–	6	Input	Inverting input, channel 2
IN2+	5	Input	Noninverting input, channel 2
IN3–	9	Input	Inverting input, channel 3
IN3+	10	Input	Noninverting input, channel 3
IN4–	13	Input	Inverting input, channel 4
IN4+	12	Input	Noninverting input, channel 4
NC	—	—	No internal connection
OUT1	1	Output	Output, channel 1
OUT2	7	Output	Output, channel 2
OUT3	8	Output	Output, channel 3
OUT4	14	Output	Output, channel 4
V–	11	—	Negative (lowest) supply or ground (for single-supply operation)
V+	4	—	Positive (highest) supply



**Figure 4-2. RTE Package,
16-Pin WQFN
(Top View)**

Table 4-2. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1IN–	16	Input	Negative input
1IN+	1	Input	Positive input
1OUT	15	Output	Output
2IN–	5	Input	Negative input
2IN+	4	Input	Positive input
2OUT	6	Output	Output
3IN–	8	Input	Negative input
3IN+	9	Input	Positive input
3OUT	7	Output	Output
4IN–	13	Input	Negative input
4IN+	12	Input	Positive input
4OUT	14	Output	Output
NC	3, 10	—	Do not connect
VCC–	11	—	Negative (lowest) supply or ground (for single-supply operation)
VCC+	2	—	Positive (highest) supply

5 Specifications

5.1 Absolute Maximum Ratings

For $T_A = 25^\circ\text{C}$ (unless otherwise noted)⁽¹⁾

	LM2902B-Q1, LM2902BA-Q1	LM2902-Q1	LM2902KV-Q1	UNIT
Supply voltage, V_{CC} ⁽²⁾	40	26	32	V
Differential input voltage, V_{ID} ⁽³⁾	± 40	± 26	± 32	V
Input voltage, V_I	-0.3 to 40	-0.3 to 26	-0.3 to 32	V
Duration of output short circuit (one amplifier) to ground at (or below) $T_A = 25^\circ\text{C}$, $V_{CC} \leq 15\text{V}$ ⁽⁴⁾	Unlimited	Unlimited	Unlimited	
Operating virtual junction temperature, T_J	150	142	142	$^\circ\text{C}$
Storage temperature range, T_{stg}	-65 to 150	-65 to 150	-65 to 150	$^\circ\text{C}$

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values are with respect to network ground terminal GND.
- (3) Differential voltages are at $IN+$ with respect to $IN-$.
- (4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

5.2 ESD Ratings

			VALUE	UNIT
LM2902B-Q1 and LM2902BA-Q1				
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±1000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	
LM2902KV-Q1 and LM2902KAV-Q1				
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±1000	V
		Charged-device model (CDM), per AEC Q100-011	±2000	
LM2902-Q1				
V _(ESD)	Electrostatic discharge	Charged-device model (CDM), per AEC Q100-011	±1500	V

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_S	Supply voltage, $V_S = (V+) - (V-)$	LM2902B-Q1, LM2902BA-Q1	3	36	V
		LM2902KV-Q1, LM2902KAV-Q1	3	30	
		LM2902-Q1	3	26	
V_{CM}	Common-mode voltage		$V-$	$(V+) - 2$	V
T_A	Operating ambient temperature		-40	125	$^\circ\text{C}$

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾	LM2902-Q1, LM2902KV-Q1, LM2902KAV-Q1		LM2902B-Q1, LM2902BA-Q1			UNIT
	D (SOIC)	PW (TSSOP)	D (SOIC)	PW (TSSOP)	RTE (WQFN)	
	14 PINS	14 PINS	14 PINS	14 PINS	16 PINS	
R _{θJA} Junction-to-ambient thermal resistance	101	86	99.3	133.3	64.9	°C/W
R _{θJC} Junction-to-case (top) thermal resistance	—	—	60.4	63.4	68.8	°C/W
R _{θJB} Junction-to-board thermal resistance	—	—	57.5	76.5	40.2	°C/W
Ψ _{JT} Junction-to-top characterization parameter	—	—	19.8	15.6	4.9	°C/W
Ψ _{JB} Junction-to-board characterization parameter	—	—	57.0	75.9	40.0	°C/W
R _{θJC} Junction-to-case (bottom) thermal resistance	—	—	—	—	23.6	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.5 Electrical Characteristics - LM2902B-Q1 and LM2902BA-Q1

For $V_S = (V+) - (V-) = 5V$ to $36V$ ($\pm 2.5V$ to $\pm 18V$), at $T_A = 25^\circ C$, $V_{CM} = V_{OUT} = V_S / 2$, and $R_L = 10k\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V _{OS}	Input offset voltage	LM2902B-Q1		±0.3		±3.0	mV
			T _A = −40°C to +125°C	±4.0			
		LM2902BA-Q1		±0.3		±2	
			T _A = −40°C to +125°C	±2.5			
dV _{OS} /dT	Input offset voltage drift	R _S = 0Ω	T _A = −40°C to +125°C	±7			μV/°C
PSRR	Input offset voltage versus power supply			65	100		dB
	Channel separation	f = 1kHz to 20kHz			120		dB
INPUT VOLTAGE RANGE							
V _{CM}	Common-mode voltage range	V _S = 3V to 36V		V−	(V+) − 1.5		V
		V _S = 5V to 36V, T _A = −40°C to +125°C		V−	(V+) − 2		
CMRR	Common-mode rejection ratio	(V−) ≤ V _{CM} ≤ (V+) − 1.5V, V _S = 3V to 36V		70	80		dB
		(V−) ≤ V _{CM} ≤ (V+) − 2V, V _S = 5V to 36V, T _A = −40°C to +125°C		65	80		
INPUT BIAS CURRENT							
I _B	Input bias current			−10		−35	nA
		T _A = −40°C to +125°C		−50			
dI _{OS} /dT	Input offset current drift	T _A = −40°C to +125°C		10			pA/°C
I _{OS}	Input offset current			±0.5		±4	nA
		T _A = −40°C to +125°C		±5			
dI _{OS} /dT	Input offset current drift	T _A = −40°C to +125°C		10			pA/°C
NOISE							
E _N	Input voltage noise	f = 0.1Hz to 10Hz		3			μV _{PP}
e _N	Input voltage noise density	R _S = 100Ω, V _I = 0V, f = 1kHz (see Noise-Test Circuit)		35			nV/√Hz
INPUT IMPEDANCE							
Z _{ID}	Differential			10 0.1			MΩ pF
Z _{ICM}	Common-mode			4 1.5			GΩ pF
OPEN-LOOP GAIN							
A _{OL}	Open-loop voltage gain	V _S = 15V, V _O = 1V to 11V, R _L ≥ 10kΩ, connected to (V−)		50	100		V/mV
			T _A = −40°C to +125°C	25			
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	R _L = 1MΩ, C _L = 20pF (see Unity-Gain Amplifier)		1.2			MHz
SR	Slew rate	R _L = 1MΩ, C _L = 30pF, V _I = ±10V (see Unity-Gain Amplifier)		0.5			V/μs
Θ _m	Phase margin	G = +1, R _L = 10kΩ, C _L = 20pF		56			°
t _S	Settling time	To 0.1%, V _S = 5V, 2V Step , G = +1, C _L = 100pF		4			μs
	Overload recovery time	V _{IN} × gain > V _S		10			μs
THD+N	Total harmonic distortion + noise	G = +1, f = 1kHz, V _O = 3.53V _{RMS} , V _S = 36V, R _L = 100k, I _{OUT} ≤ 50μA, BW = 80kHz		0.001%			
OUTPUT							
V _O	Voltage output swing from rail	Positive Rail (V+)	I _{OUT} = −50μA	1.35	1.5	V	
			I _{OUT} = −1mA	1.4	1.6		
			I _{OUT} = −5mA	1.5	1.75		
		Negative Rail (V−)	I _{OUT} = 50μA	100	150	mV	
			I _{OUT} = 1mA	0.75	1	V	
			V _S = 5V, R _L ≤ 10kΩ to (V−), T _A = −40°C to +125°C	5	20	mV	
I _O	Output current	Source V _S = 15V, V _O = V−, V _{ID} = 1V	−20 ⁽¹⁾	−30	mA		
			T _A = −40°C to +125°C	−10 ⁽¹⁾			
		Sink V _S = 15V, V _O = V+, V _{ID} = −1V	10 ⁽¹⁾	20			
			T _A = −40°C to +125°C	5 ⁽¹⁾			
		V _{ID} = −1V, V _O = (V−) + 200mV	50	85		μA	
I _{SC}	Short-circuit current	V _S = 20V, (V+) = 10V, (V−) = −10V, V _O = 0V		±40		±60	mA

5.5 Electrical Characteristics - LM2902B-Q1 and LM2902BA-Q1 (continued)

For $V_S = (V_+) - (V_-) = 5V$ to $36V$ ($\pm 2.5V$ to $\pm 18V$), at $T_A = 25^\circ C$, $V_{CM} = V_{OUT} = V_S / 2$, and $R_L = 10k\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{LOAD}	Capacitive load drive			100		pF
R_O	Open-loop output impedance	$f = 1MHz$, $I_O = 0A$		300		Ω
POWER SUPPLY						
I_Q	Quiescent current per amplifier	$V_S = 5V$, $I_O = 0A$, $T_A = -40^\circ C$ to $+125^\circ C$		175	300	μA
		$V_S = 36V$, $I_O = 0A$, $T_A = -40^\circ C$ to $+125^\circ C$		350	750	

(1) Specified by design and characterization only.

5.6 Electrical Characteristics: LM2902-Q1, LM2902KV-Q1, LM2902KAV-Q1

For $V_S = (V_+) - (V_-) = 5V$, at $T_A = 25^\circ C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA ⁽¹⁾	MIN	TYP ⁽²⁾	MAX	UNIT
V _{IO}	Input offset voltage	V _{CC} = 5V to 26V, V _{IC} = V _{ICRmin} , V _O = 1.4V	25°C		3	7	mV
			Full Range			10	
I _{IO}	Input offset current	V _O = 1.4V	25°C		2	50	nA
			Full Range			300	
I _{IB}	Input bias current	V _O = 1.4V	25°C		–20	–250	nA
			Full Range			–500	
V _{ICR}	Common-mode input voltage range	V _{CC} = 5V to 26V	25°C	V–	(V+) – 1.5		V
			Full Range	V–	(V+) – 2		
V _{OH}	High-level output voltage	R _L = 10kΩ	25°C	(V+) – 1.5			V
		V _{CC} = 26V, R _L = 2kΩ	Full Range	22			
		V _{CC} = 26V, R _L ≥ 10kΩ	Full Range	23	24		
V _{OL}	Low-level output voltage	R _L ≤ 10kΩ	Full Range		5	20	mV
A _{VD}	Large-signal differential voltage amplification	V _{CC} = 15V, V _O = 1V to 11V, R _L ≥ 2kΩ	25°C		100		V/mV
			Full Range	15			
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICRmin}	25°C	50	80		dB
k _{SVR}	Supply-voltage rejection ratio (ΔV _{CC} /ΔV _{IO})		25°C	50	100		dB
V _{O1} / V _{O2}	Crosstalk attenuation	f = 1kHz to 20kHz	25°C		120		dB
I _O	Output current	V _{CC} = 15V, V _O = 0, V _{ID} = 1V	25°C	–20	–30	–60	mA
			Full Range	–10			
		V _{CC} = 15V, V _O = 15V, V _{ID} = –1V	25°C	10	20		
			Full Range	5			
		V _{ID} = –1V, V _O = 200mV	25°C		30		μA
I _{OS}	Short-circuit output current	V _{CC} at 5V, GND at –5V, V _O = 0	25°C		±40	±60	mA
I _{CC}	Supply current (four amplifiers)	V _O = 2.5V, no load	Full Range		0.7	1.2	mA
		V _{CC} = 26V, V _O = 0.5V _{CC} , no load	Full Range		1.4	3	
V _{IO}	Input offset voltage	V _{CC} = 5V to 32V, V _{IC} = V _{ICRmin} V _O = 1.4V	25°C		3	7	mV
			Full Range			10	
			25°C		1	2	
			Full Range			4	
ΔV _{IO} /ΔT	Temperature drift	R _S = 0Ω	Full Range		7		μV/°C
I _{IO}	Input offset current	V _O = 1.4V	25°C		2	50	nA
			Full Range			150	
ΔI _{IO} /ΔT	Temperature drift		Full Range		10		pA/°C
I _{IB}	Input bias current	V _O = 1.4V	25°C		–20	–250	nA
			Full Range			–500	
V _{ICR}	Common-mode input voltage range	V _{CC} = 5V to 32V	25°C	0 to V _{CC} – 1.5			V
			Full Range	0 to V _{CC} – 2			
V _{OH}	High-level output voltage	R _L = 10kΩ	25°C	V _{CC} – 1.5			V
		V _{CC} = 32V, R _L = 2kΩ	Full Range	26			
		V _{CC} = 32V, R _L ≥ 10kΩ	Full Range	27			
V _{OL}	Low-level output voltage	R _L ≤ 10kΩ	Full Range		5	20	mV

5.6 Electrical Characteristics: LM2902-Q1, LM2902KV-Q1, LM2902KAV-Q1 (continued)

For $V_S = (V_+) - (V_-) = 5V$, at $T_A = 25^\circ C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A^{(1)}$	MIN	TYP ⁽²⁾	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	$V_{CC} = 15V$, $V_O = 1V$ to $11V$, $R_L \geq 2k\Omega$	$25^\circ C$	25	100		V/mV
			Full Range	15			
	Amplifier-to-amplifier coupling ⁽³⁾	$f = 1kHz$ to $20kHz$, input referred	$25^\circ C$		120		dB
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$	$25^\circ C$	60	80		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC} / \Delta V_{IO}$)		$25^\circ C$	60	100		dB
V_{O1} / V_{O2}	Crosstalk attenuation	$f = 1kHz$ to $20kHz$	$25^\circ C$		120		dB
I_O	Output current	$V_{CC} = 15V$, $V_O = 0$, $V_{ID} = 1V$	$25^\circ C$	-20	-30	-60	mA
			Full Range	-10			
		$V_{CC} = 15V$, $V_O = 15V$, $V_{ID} = -1V$	$25^\circ C$	10	20		mA
			Full Range	5			
		$V_{ID} = -1V$, $V_O = 200mV$	$25^\circ C$	12	40		μA
I_{OS}	Short-circuit output current	V_{CC} at $5V$, GND at $-5V$, $V_O = 0$	$25^\circ C$		± 40	± 60	mA
I_{CC}	Supply current (four amplifiers)	$V_O = 2.5V$, no load	Full Range		0.7	1.2	mA
		$V_{CC} = 32V$, $V_O = 0.5V_{CC}$, no load	Full Range		1.4	3	

- (1) Full range is $-40^\circ C$ to $125^\circ C$.
 (2) All typical values are at $T_A = 25^\circ C$.
 (3) Due to proximity of external components, make sure that coupling is not originating via stray capacitance between these external parts. Typically, this can be detected, as this type of coupling increases at higher frequencies.

5.7 Operating Conditions: LM2902-Q1, LM2902KV-Q1, LM2902KAV-Q1

For $V_S = (V_+) - (V_-) = 15V$, at $T_A = 25^\circ C$

PARAMETER		TEST CONDITIONS	TYP	UNIT
SR	Slew rate at unity gain	$R_L = 1M\Omega$, $C_L = 30pF$, $V_I = \pm 10V$ (see Figure 6-1)	0.5	V/ μs
B_1	Unity-gain bandwidth	$R_L = 1M\Omega$, $C_L = 20pF$ (see Figure 6-1)	1.2	MHz
V_N	Equivalent input noise voltage	$R_S = 100\Omega$, $V_I = 0V$, $f = 1kHz$ (see Figure 6-2)	35	nV/ $\sqrt{Hz}$

5.8 Typical Characteristics

This typical characteristics section is applicable for LM2902B-Q1 and LM2902BA-Q1. Typical characteristics data in this section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{V}$ ($\pm 18\text{V}$), $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).

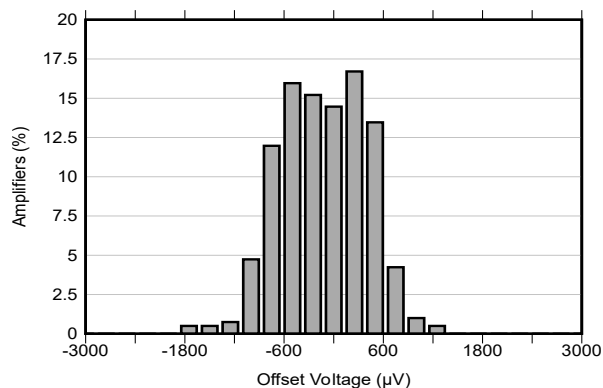


Figure 5-1. Offset Voltage Production Distribution

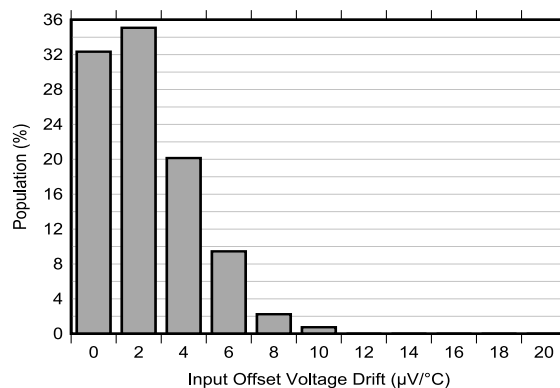


Figure 5-2. Offset Voltage Drift Distribution

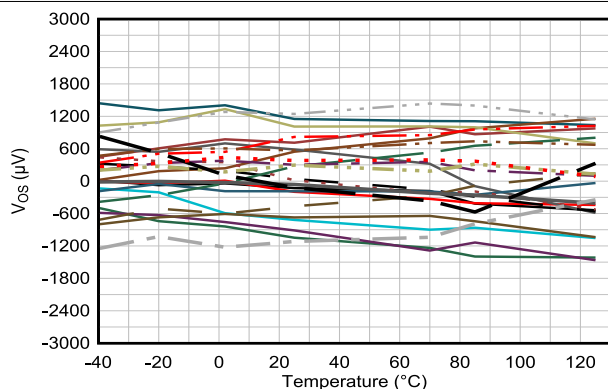


Figure 5-3. Offset Voltage vs Temperature

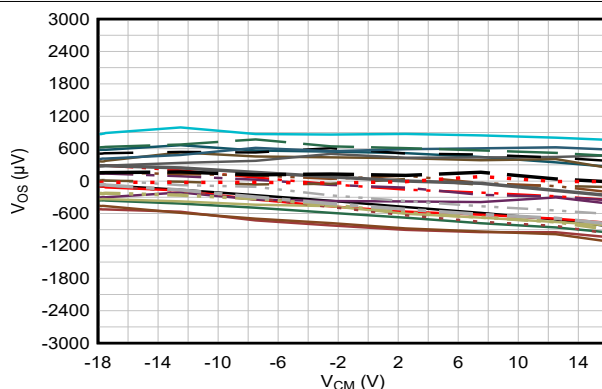


Figure 5-4. Offset Voltage vs Common-Mode Voltage

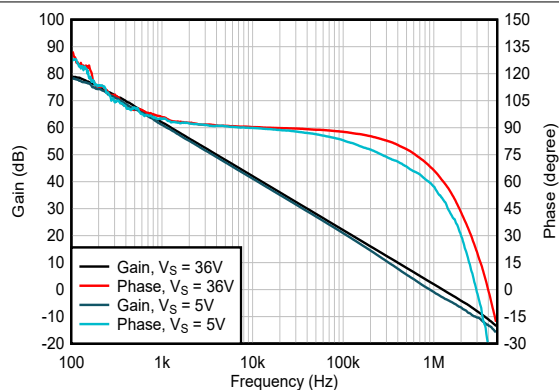


Figure 5-5. Open-Loop Gain and Phase vs Frequency

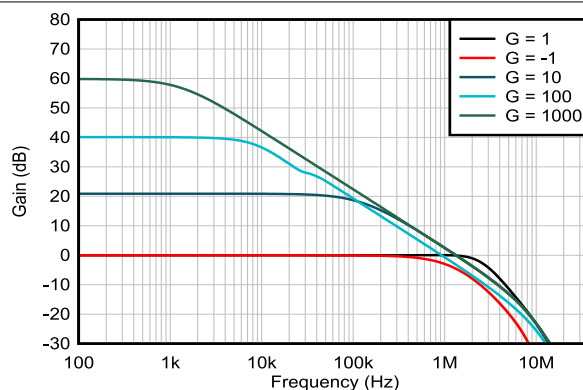


Figure 5-6. Closed-Loop Gain vs Frequency

5.8 Typical Characteristics (continued)

This typical characteristics section is applicable for LM2902B-Q1 and LM2902BA-Q1. Typical characteristics data in this section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{V}$ ($\pm 18\text{V}$), $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).

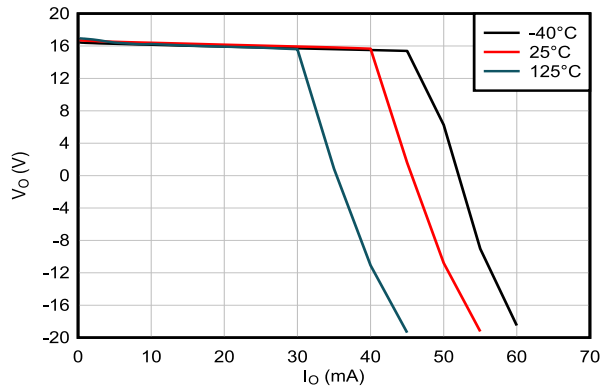


Figure 5-7. Output Voltage Swing vs Output Current (Sourcing)

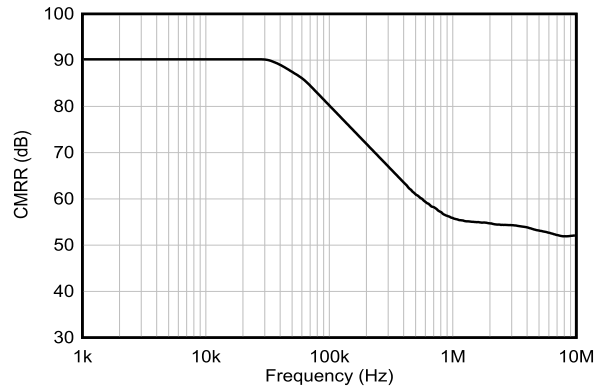


Figure 5-8. CMRR vs Frequency

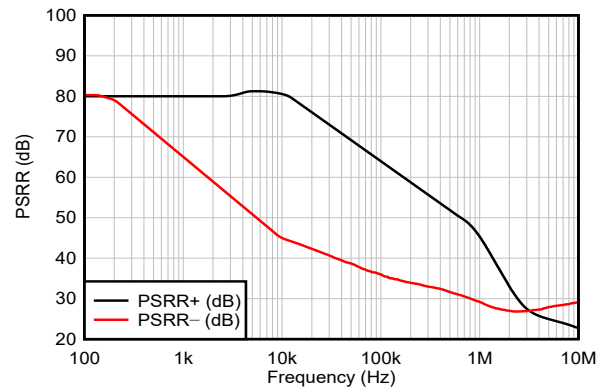


Figure 5-9. PSRR vs Frequency

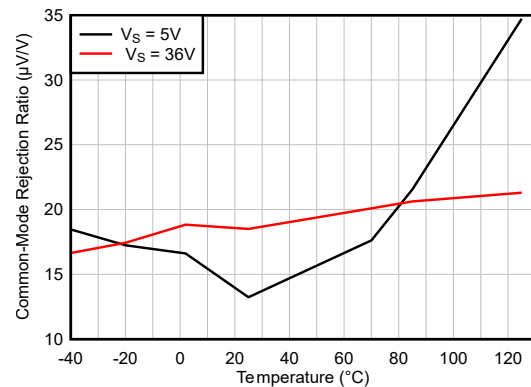


Figure 5-10. Common-Mode Rejection Ratio vs Temperature (dB)

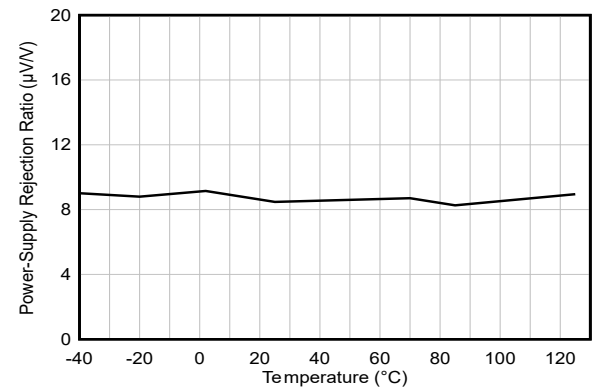


Figure 5-11. Power Supply Rejection Ratio vs Temperature (dB)

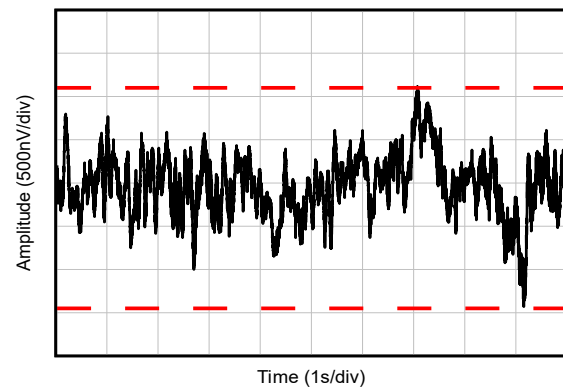


Figure 5-12. 0.1Hz to 10Hz Noise

5.8 Typical Characteristics (continued)

This typical characteristics section is applicable for LM2902B-Q1 and LM2902BA-Q1. Typical characteristics data in this section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{V} (\pm 18\text{V})$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).

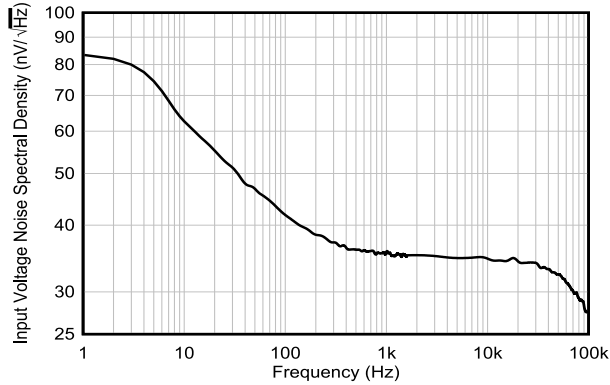
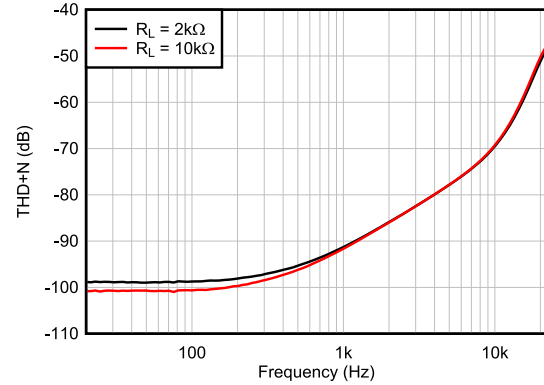
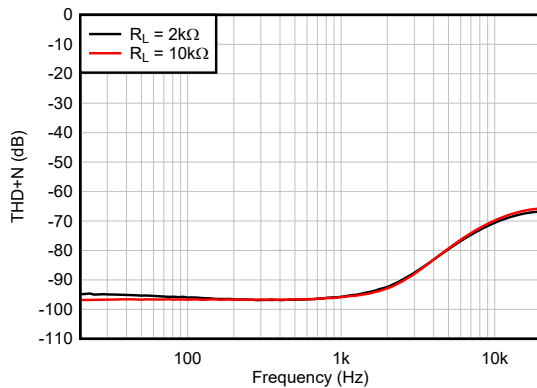


Figure 5-13. Input Voltage Noise Spectral Density vs Frequency



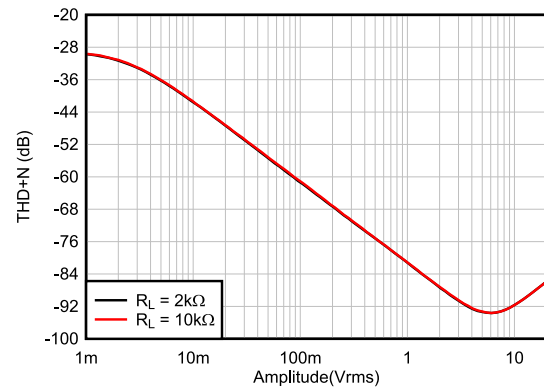
$G = 1$, $f = 1\text{kHz}$, $BW = 80\text{kHz}$,
 $V_{OUT} = 10\text{V}_{PP}$, R_L connected to V_-

Figure 5-14. THD+N Ratio vs Frequency, $G = 1$



$G = -1$, $f = 1\text{kHz}$, $BW = 80\text{kHz}$,
 $V_{OUT} = 10\text{V}_{PP}$, R_L connected to V_-
See [Section 6](#)

Figure 5-15. THD+N Ratio vs Frequency, $G = -1$



$G = 1$, $f = 1\text{kHz}$, $BW = 80\text{kHz}$,
 R_L connected to V_-

Figure 5-16. THD+N vs Output Amplitude, $G = 1$

5.8 Typical Characteristics (continued)

This typical characteristics section is applicable for LM2902B-Q1 and LM2902BA-Q1. Typical characteristics data in this section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{V}$ ($\pm 18\text{V}$), $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).

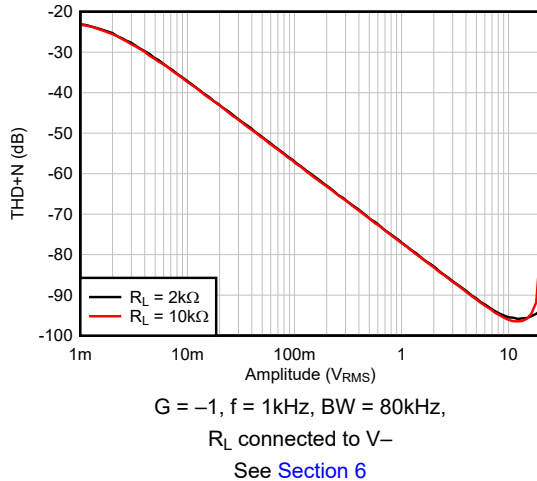


Figure 5-17. THD+N vs Output Amplitude, $G = -1$

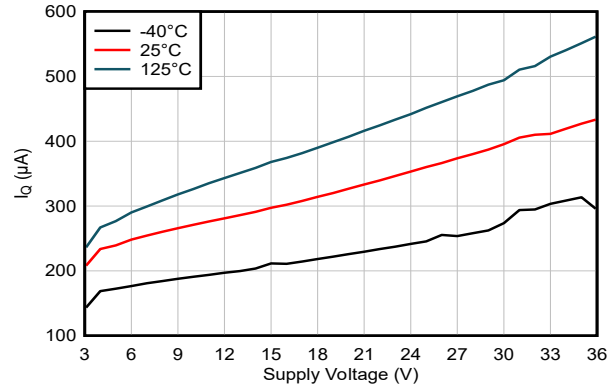


Figure 5-18. Quiescent Current vs Supply Voltage

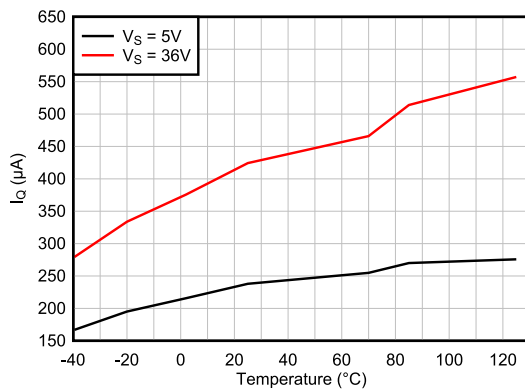


Figure 5-19. Quiescent Current vs Temperature

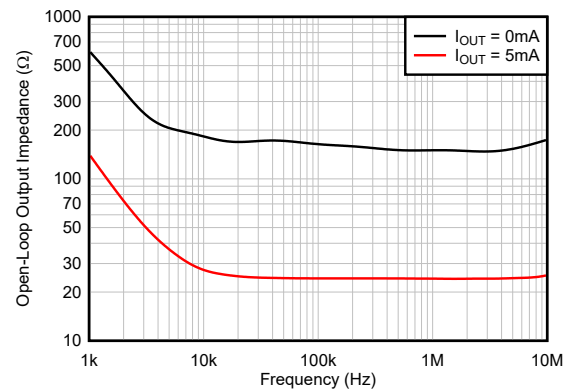


Figure 5-20. Open-Loop Output Impedance vs Frequency

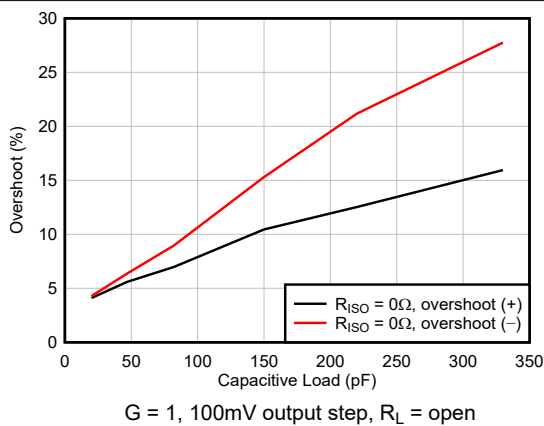


Figure 5-21. Small-Signal Overshoot vs Capacitive Load

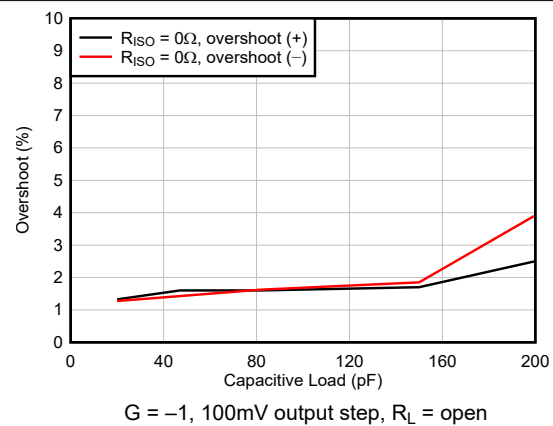


Figure 5-22. Small-Signal Overshoot vs Capacitive Load

5.8 Typical Characteristics (continued)

This typical characteristics section is applicable for LM2902B-Q1 and LM2902BA-Q1. Typical characteristics data in this section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{V}$ ($\pm 18\text{V}$), $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).

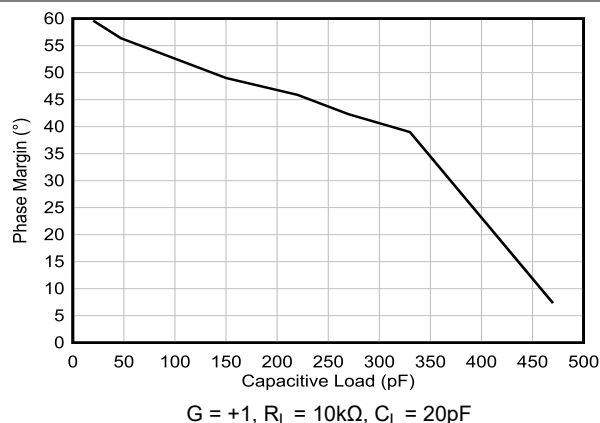


Figure 5-23. Phase Margin vs Capacitive Load

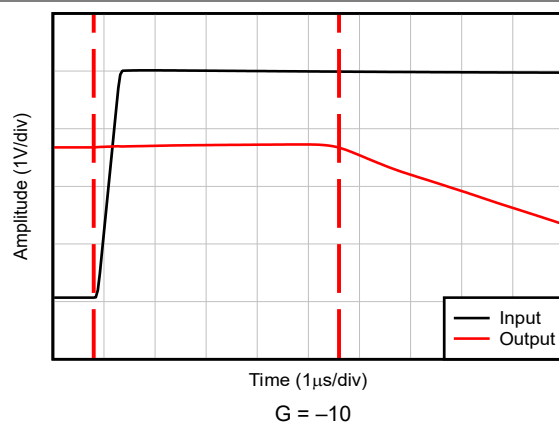


Figure 5-24. Overload Recovery (Positive Rail)

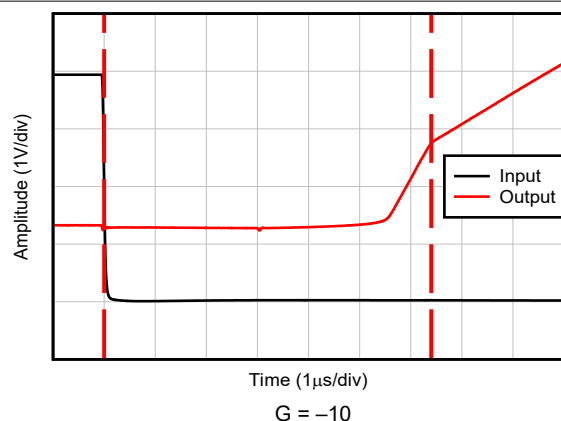


Figure 5-25. Overload Recovery (Negative Rail)

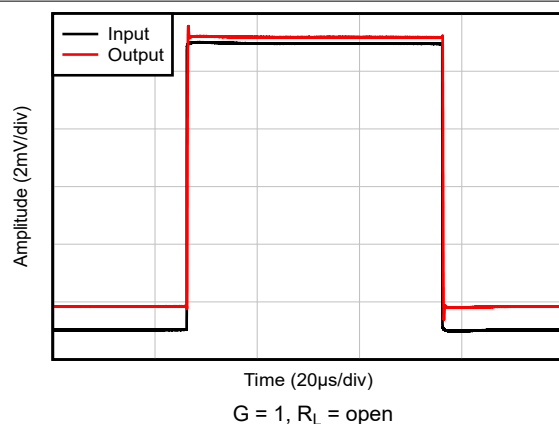


Figure 5-26. Small-Signal Step Response, $G = 1$

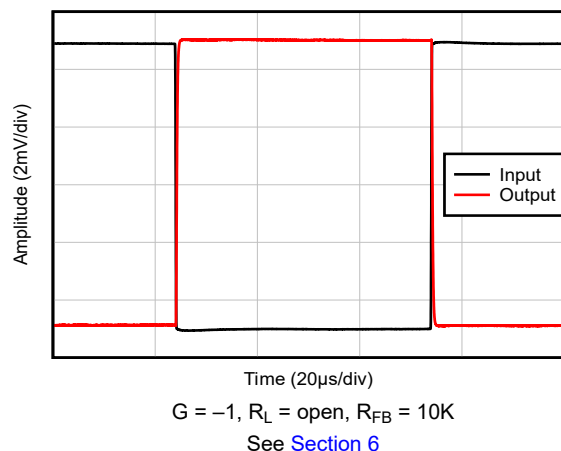


Figure 5-27. Small-Signal Step Response, $G = -1$

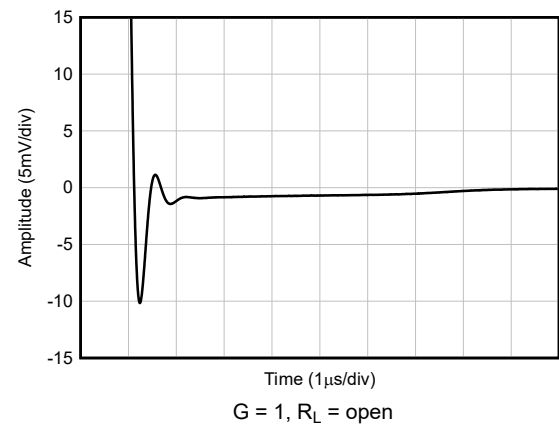


Figure 5-28. Large-Signal Step Response (Falling)

5.8 Typical Characteristics (continued)

This typical characteristics section is applicable for LM2902B-Q1 and LM2902BA-Q1. Typical characteristics data in this section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{V}$ ($\pm 18\text{V}$), $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).

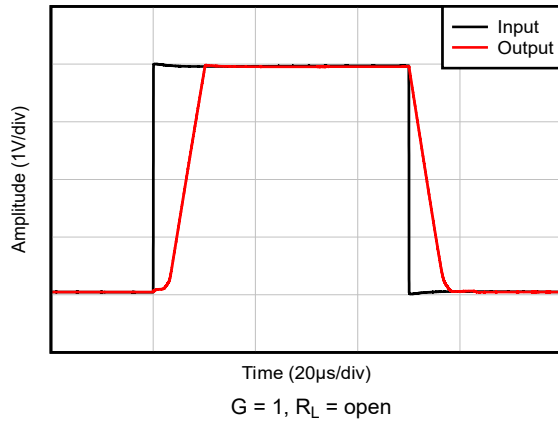


Figure 5-29. Large-Signal Step Response, $G = 1$

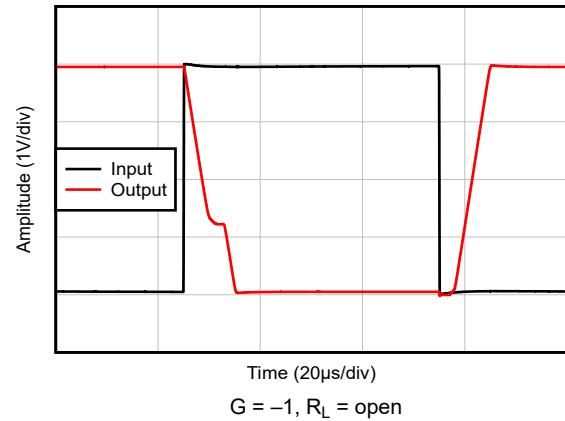


Figure 5-30. Large-Signal Step Response, $G = -1$

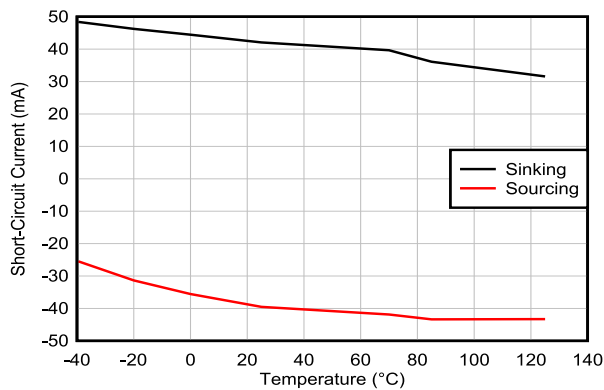


Figure 5-31. Short-Circuit Current vs Temperature

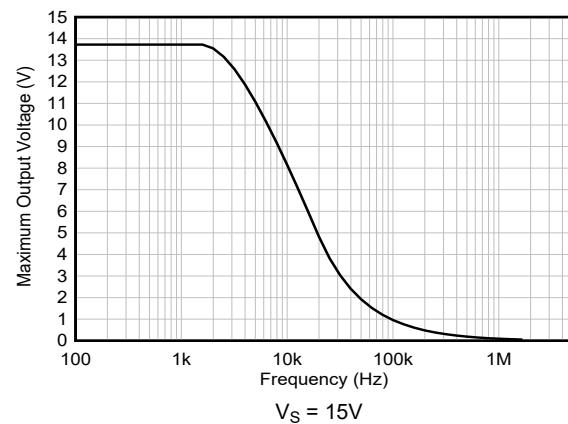


Figure 5-32. Maximum Output Voltage vs Frequency

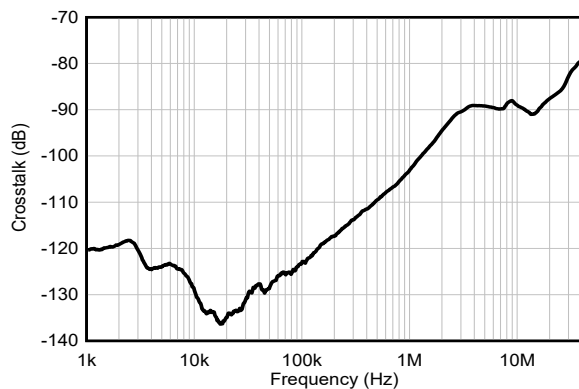


Figure 5-33. Channel Separation vs Frequency

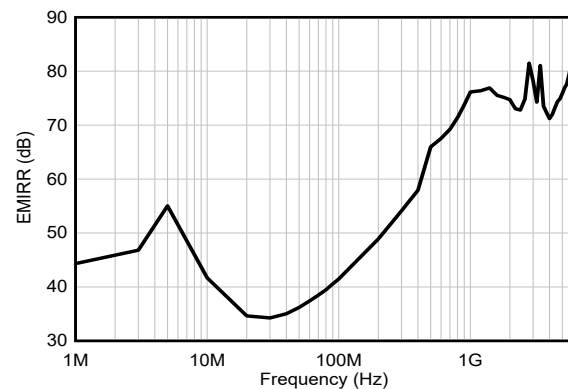


Figure 5-34. EMIRR (Electromagnetic Interference Rejection Ratio) vs Frequency

6 Parameter Measurement Information

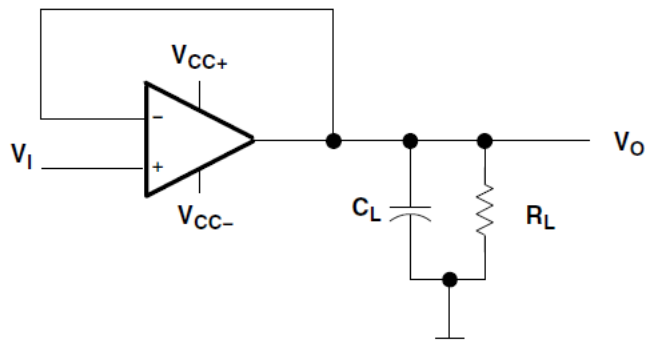


Figure 6-1. Unity-Gain Amplifier

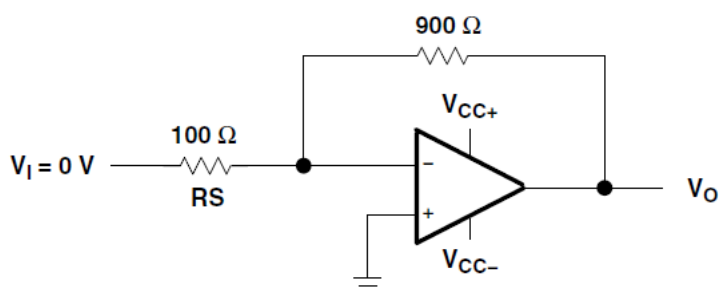


Figure 6-2. Noise-Test Circuit

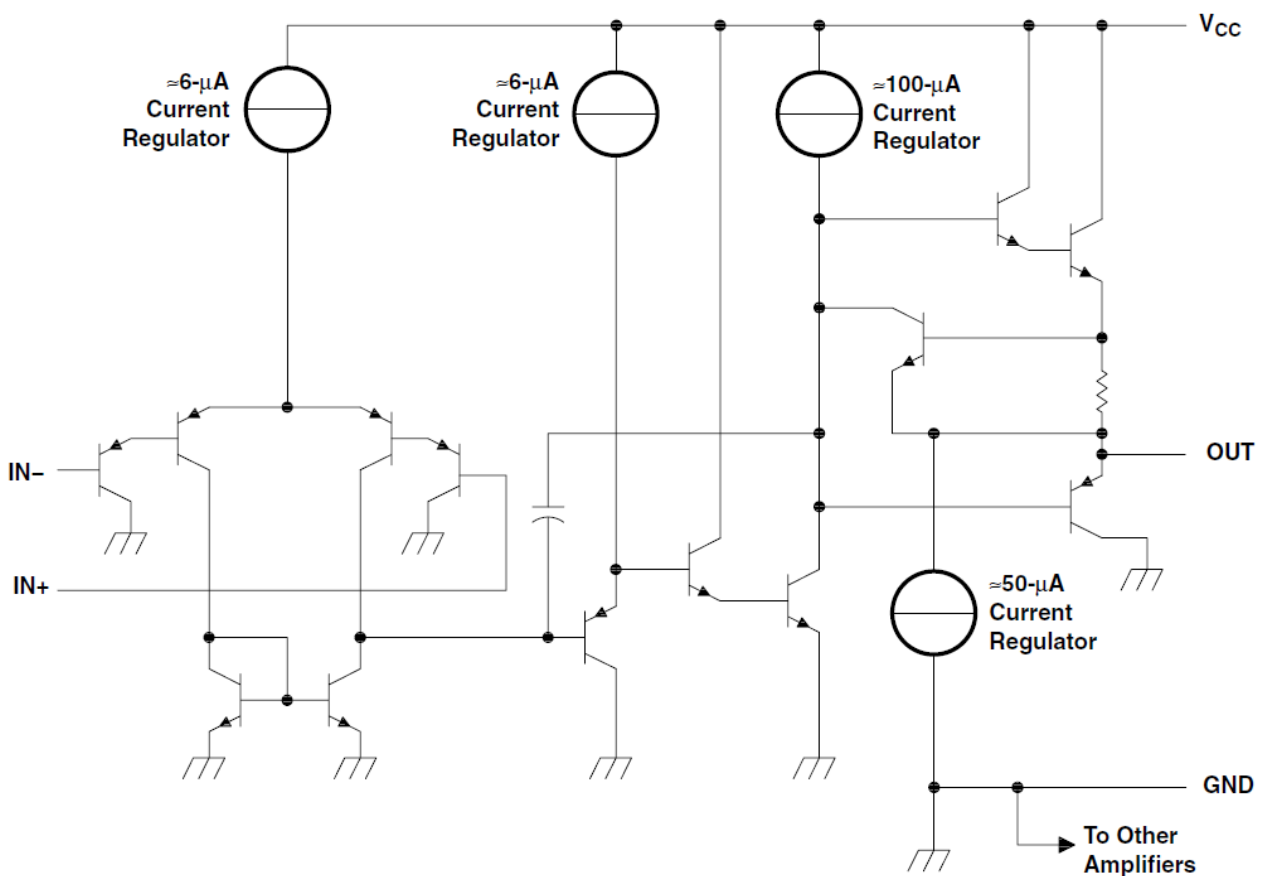
7 Detailed Description

7.1 Overview

The LM2902-Q1, LM2902B-Q1, and LM2902BA-Q1 devices consist of four independent, high-gain frequency-compensated operational amplifiers designed to operate from a single supply over a wide range of voltages. Operation from split supplies also is possible if the difference between the two supplies is within the supply voltage range, and V_S is at least 1.5V more positive than the input common-mode voltage. The low supply-current drain is independent of the magnitude of the supply voltage.

Applications include transducer amplifiers, DC amplification blocks, and all the conventional operational amplifier circuits that now can be implemented more easily in single-supply-voltage systems. For example, these devices can be operated directly from the standard 5V supply used in digital systems and easily can provide the required interface electronics without additional $\pm 5V$ supplies.

7.2 Functional Block Diagram



Schematic (Each Amplifier)

7.3 Feature Description

7.3.1 Input Common-Mode Range

The valid common-mode range is from device ground to $V_S - 1.5V$ ($V_S - 2V$ across temperature). Inputs can exceed V_S up to the maximum V_S without device damage. At least one input must be in the valid input common-mode range for the output to be the correct phase. If both inputs exceed the valid range, then the output phase is undefined. The output phase is undefined if the input is more than 0.3V below V_- . If either input is more than 0.3V below V_- then limit the input current to 1mA.

7.4 Device Functional Modes

The LM2902-Q1, LM2902B-Q1, and LM2902BA-Q1 devices are powered on when the supply is connected. This device can be operated as a single-supply operational amplifier or dual-supply amplifier, depending on the application.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LM2902-Q1, LM2902B-Q1, LM2902BA-Q1 operational amplifiers are useful in a wide range of signal conditioning applications. Inputs can be powered before V_S for flexibility in multiple supply circuits. For full application design guidelines related to this family of devices, please refer to the application report [Application design guidelines for LM324/LM358 devices](#).

8.2 Typical Application

A typical application for an operational amplifier is an inverting amplifier. This amplifier takes a positive voltage on the input and makes the voltage a negative voltage of the same magnitude. In the same manner, the device also makes negative voltages positive.

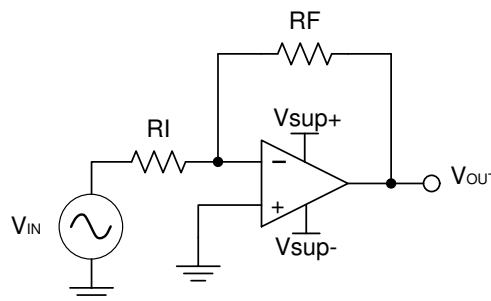


Figure 8-1. Application Schematic

8.2.1 Design Requirements

The supply voltage must be chosen such that the supply is larger than the input voltage range and output range. For instance, this application scales a signal of $\pm 0.5V$ to $\pm 1.8V$. Setting the supply at $\pm 12V$ is sufficient to accommodate this application.

8.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier using [Equation 1](#) and [Equation 2](#):

$$A_V = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

Once the desired gain is determined, choose a value for R_I or R_F . Choosing a value in the kilohm range is desirable because the amplifier circuit uses currents in the milliampere range. This allows the part to not draw too much current. This example uses $10k\Omega$ for R_I which means $36k\Omega$ is used for R_F . This was determined by [Equation 3](#).

$$A_V = -\frac{R_F}{R_I} \quad (3)$$

8.2.3 Application Curve

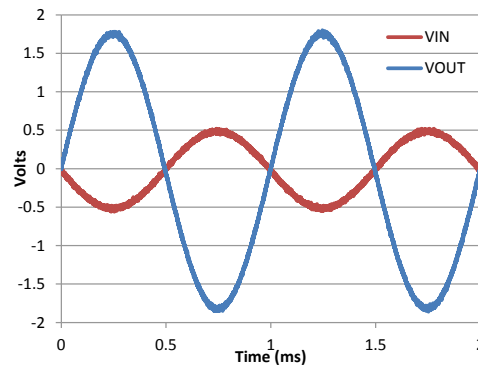


Figure 8-2. Input and Output Voltages of the Inverting Amplifier

8.3 Power Supply Recommendations

CAUTION

Supply voltages larger than specified in the recommended operating region can permanently damage the device (see [Section 5.1](#)).

Place 0.1μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see [Section 8.4](#).

8.4 Layout

8.4.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If keeping traces separate is not possible, crossing the sensitive trace perpendicular as opposed to in parallel with the noisy trace is recommended.
- Place the external components as close to the device as possible. Keeping R_F and R_G close to the inverting input minimizes parasitic capacitance, as shown in [Figure 8-3](#).
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

8.4.2 Layout Example

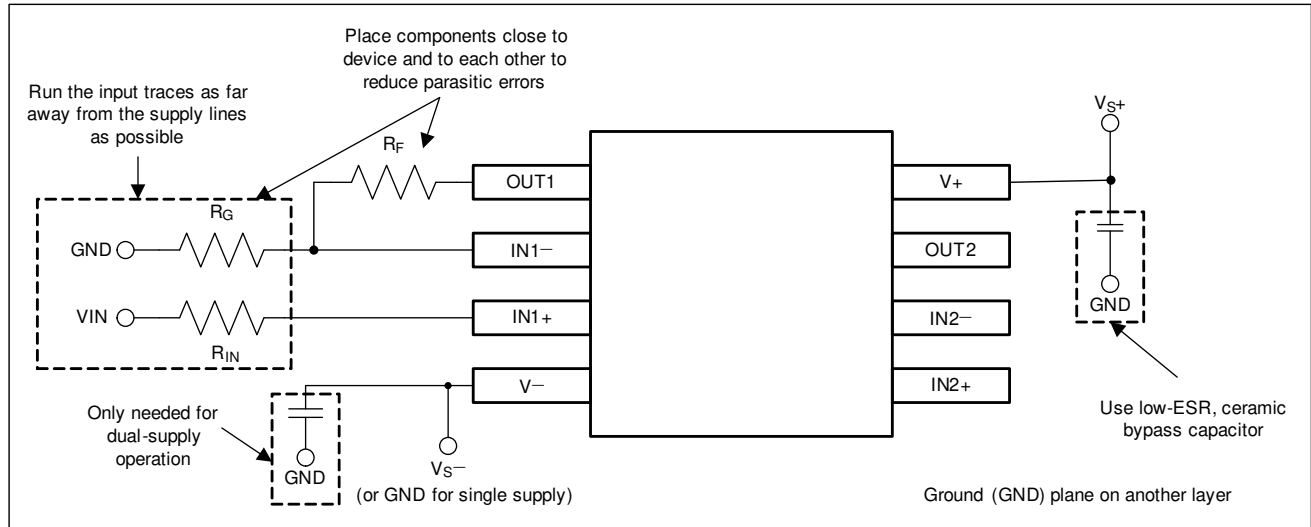


Figure 8-3. Operational Amplifier Board Layout for Noninverting Configuration

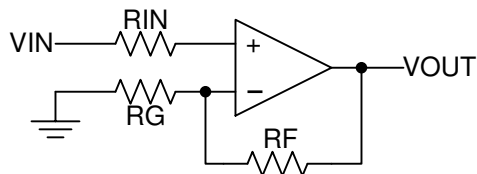


Figure 8-4. Operational Amplifier Schematic for Noninverting Configuration

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Application Design Guidelines for LM324/LM358 Devices application note](#)

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (November 2024) to Revision J (January 2026)	Page
• Added LM2902B-Q1 RTE (WQFN) package as production data throughout the document.....	1
• Updated HBM in <i>Description</i> to match <i>ESD Ratings</i>	1
• Changed human-body model (HBM) from $\pm 2000V$ to $\pm 1000V$ in <i>ESD Ratings</i>	5

Changes from Revision H (October 2023) to Revision I (November 2024)	Page
• Changed the status of the LM2902B-Q1 and LM2902BA-Q1 SOIC-14 package from: <i>preview</i> to: <i>active</i>	1

Changes from Revision G (February 2023) to Revision H (October 2023)	Page
• Changed the format of <i>Package Information</i> table to include package lead size and channel count.....	1
• Changed the status of the LM2902BA-Q1 TSSOP-14 package from: <i>preview</i> to: <i>active</i>	1

Changes from Revision F (May 2022) to Revision G (February 2023)	Page
• Deleted the preview note for the LM2902B-Q1 TSSOP-14 package in the <i>Device Information</i> table.....	1
• Changed the LM2902B-Q1 values in the <i>Thermal Information</i> section.....	6
• Added <i>Typical Characteristics</i> curves for LM2902B-Q1 and LM2902BA-Q1.....	11

Changes from Revision E (April 2008) to Revision F (May 2022)	Page
• Changed the name of the data sheet.....	1
• Revised <i>Features</i> section to include LM2902B-Q1 and LM2902BA-Q1.....	1
• Added <i>Applications</i> section	1
• Added LM2902B-Q1 and LM2902BA-Q1 to the <i>Device Information</i> table.....	1
• Added LM2902B-Q1 and LM2902BA-Q1 to the <i>Description</i> section.....	1
• Updated <i>Pin Configurations and Functions</i> section to include <i>Pin Functions</i> table.....	3
• Added LM2902B-Q1 and LM2902BA-Q1 to the <i>Absolute Maximum Ratings</i> table.....	5
• Added <i>ESD Ratings</i> table with LM2902B-Q1 and LM2902BA-Q1.....	5
• Added LM2902B-Q1 and LM2902B-Q1 to <i>Recommended Operating Conditions</i> section.....	5
• Added LM2902B-Q1 and LM2902BA-Q1 to <i>Thermal Information</i> section.....	6
• Added <i>Overview</i> section to the data sheet.....	18
• Added <i>Feature Description</i> section.....	18
• Added <i>Input Common-Mode Range</i> section to <i>Feature Description</i> section.....	18
• Added <i>Device Functional Modes</i> information for LM2902B-Q1 and LM2902BA-Q1.....	19
• Added <i>Application and Implementation</i> section for LM2902B-Q1 and LM2902BA-Q1.....	20
• Added <i>Application Information</i> section for LM2902B-Q1 and LM2902BA-Q1.....	20
• Added <i>Typical Application</i> section for LM2902B-Q1 and LM2902BA-Q1.....	20
• Added <i>Power Supply Recommendations</i> section to data sheet.....	21
• Added <i>Layout</i> section to data sheet.....	21
• Added <i>Device and Documentation Support</i> section to data sheet.....	23
• Added <i>Mechanical, Packaging, and Orderable Information</i> section to data sheet.....	24

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM2902BAQDRQ1	Active	Production	SOIC (D) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	M2902ABQD
LM2902BAQDRQ1.A	Active	Production	SOIC (D) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	M2902ABQD
LM2902BAQPWRQ1	Active	Production	TSSOP (PW) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2902BAQ
LM2902BAQPWRQ1.A	Active	Production	TSSOP (PW) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2902BAQ
LM2902BQDRQ1	Active	Production	SOIC (D) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2902BQD
LM2902BQDRQ1.A	Active	Production	SOIC (D) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2902BQD
LM2902BQPWRQ1	Active	Production	TSSOP (PW) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902BQ
LM2902BQPWRQ1.A	Active	Production	TSSOP (PW) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902BQ
LM2902BQWRTERQ1	Active	Production	WQFN (RTE) 16	5000 LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2902QW
LM2902KAVQDRQ1	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2902KAQ
LM2902KAVQDRQ1.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2902KAQ
LM2902KAVQPWRG4Q1	Obsolete	Production	TSSOP (PW) 14	-	-	Call TI	Call TI	-40 to 125	2902KAQ
LM2902KAVQPWRQ1	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2902KAQ
LM2902KAVQPWRQ1.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2902KAQ
LM2902KVQDRQ1	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2902KVQ
LM2902KVQDRQ1.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2902KVQ
LM2902KVQPWRG4Q1	Obsolete	Production	TSSOP (PW) 14	-	-	Call TI	Call TI	-40 to 125	2902KVQ
LM2902KVQPWRQ1	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2902KVQ
LM2902KVQPWRQ1.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2902KVQ
LM2902QDRG4Q1	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-40 to 125	2902Q1
LM2902QDRQ1	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2902Q1
LM2902QDRQ1.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2902Q1
LM2902QPWRG4Q1	Obsolete	Production	TSSOP (PW) 14	-	-	Call TI	Call TI	-40 to 125	2902Q1
LM2902QPWRQ1	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2902Q1
LM2902QPWRQ1.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2902Q1

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LM2902-Q1, LM2902B-Q1, LM2902BA-Q1 :

- Catalog : [LM2902](#), [LM2902B](#), [LM2902BA](#)
- Enhanced Product : [LM2902-EP](#)

NOTE: Qualified Version Definitions:

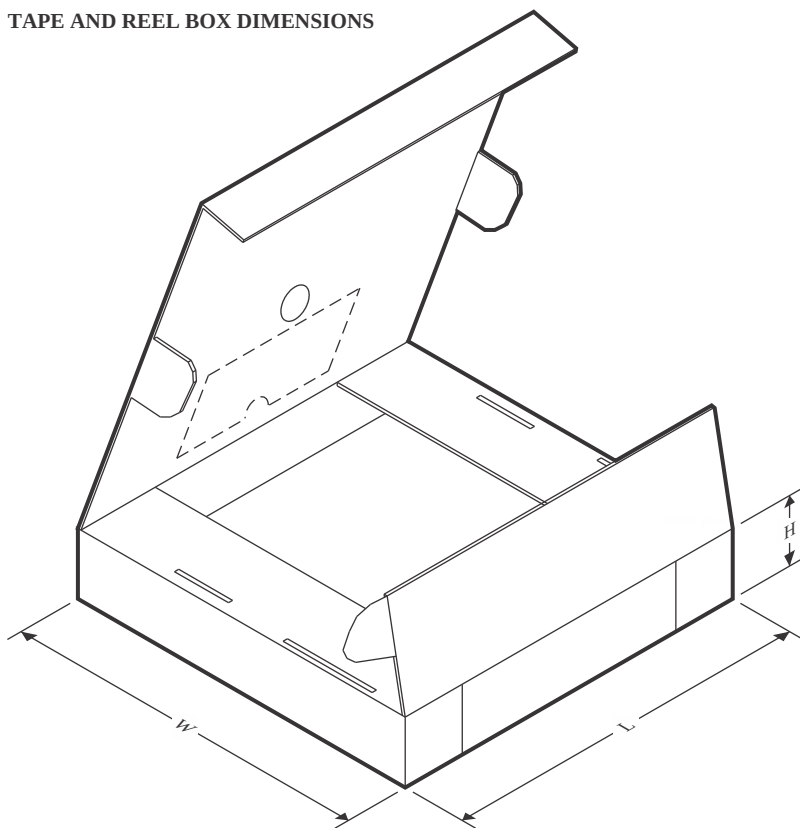
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2902BAQDRQ1	SOIC	D	14	3000	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2902BAQPWRQ1	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2902BQDRQ1	SOIC	D	14	3000	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2902BQPWRQ1	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2902BQWRTERQ1	WQFN	RTE	16	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM2902KAVQDRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2902KAVQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2902KVQDRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2902KVQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2902KVQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2902QDRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2902QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2902QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2902BAQDRQ1	SOIC	D	14	3000	353.0	353.0	32.0
LM2902BAQPWRQ1	TSSOP	PW	14	3000	353.0	353.0	32.0
LM2902BQDRQ1	SOIC	D	14	3000	353.0	353.0	32.0
LM2902BQPWRQ1	TSSOP	PW	14	3000	353.0	353.0	32.0
LM2902BQWRTERQ1	WQFN	RTE	16	5000	367.0	367.0	35.0
LM2902KAVQDRQ1	SOIC	D	14	2500	353.0	353.0	32.0
LM2902KAVQPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0
LM2902KVQDRQ1	SOIC	D	14	2500	353.0	353.0	32.0
LM2902KVQPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0
LM2902KVQPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0
LM2902QDRQ1	SOIC	D	14	2500	353.0	353.0	32.0
LM2902QPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0
LM2902QPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0

GENERIC PACKAGE VIEW

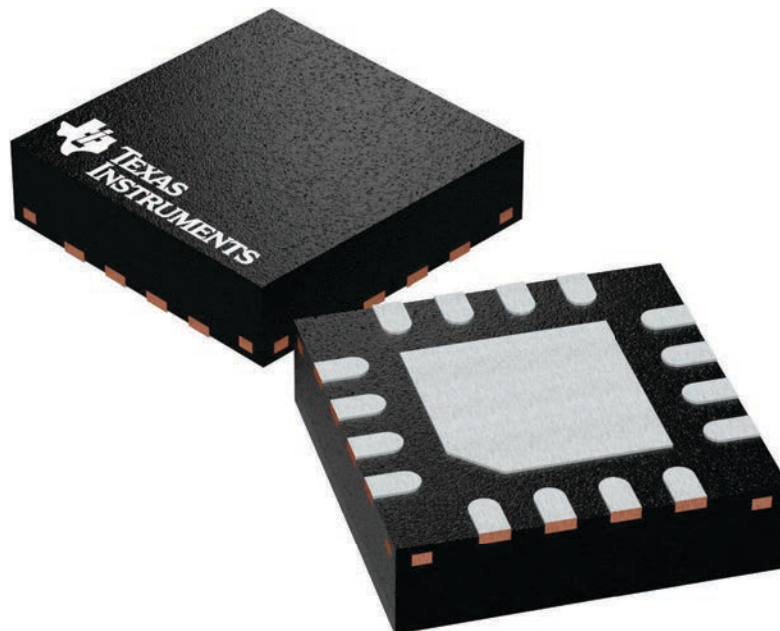
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225944/A

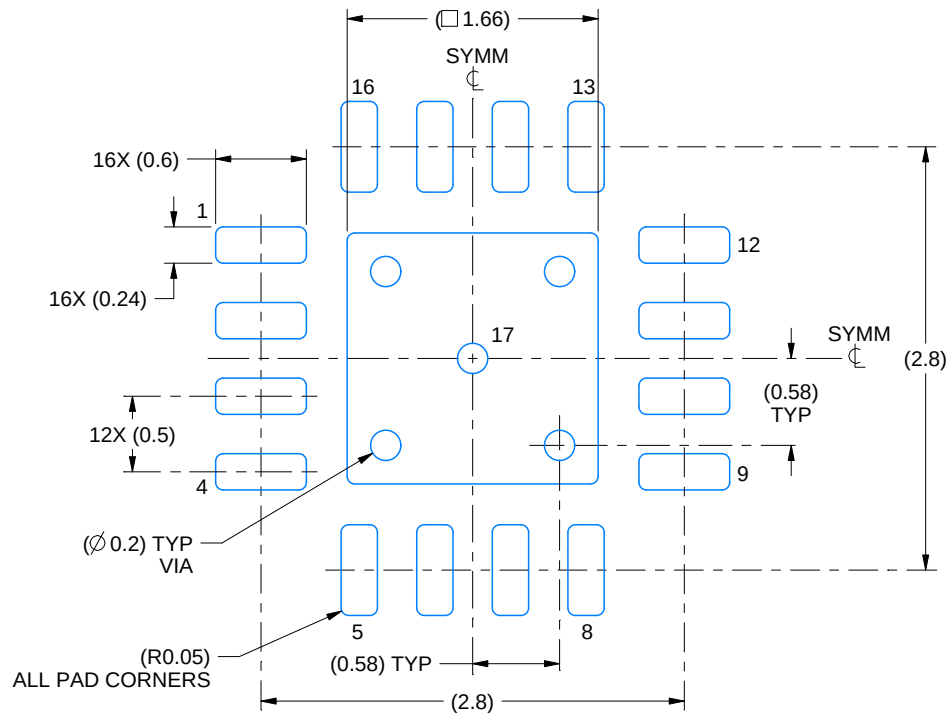


1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

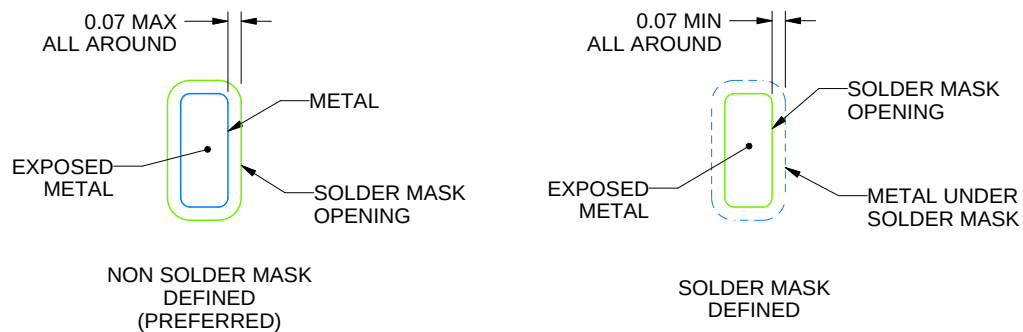
RTE0016K

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4224938/C 03/2022

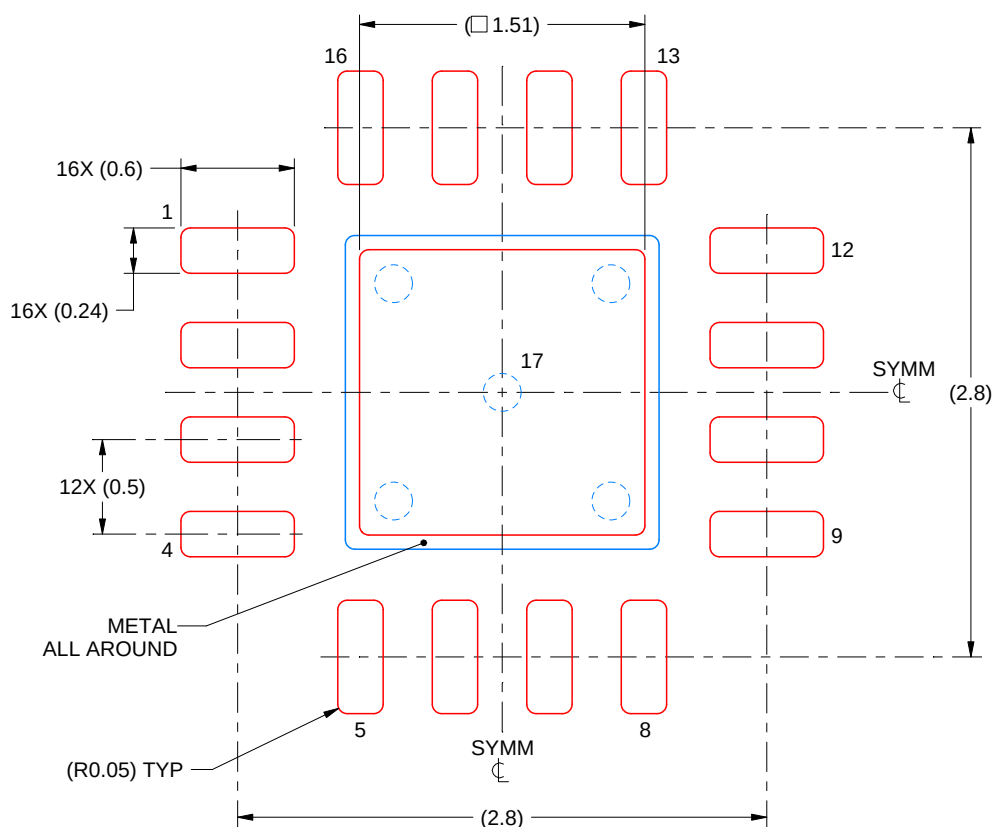
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

RTE0016K

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



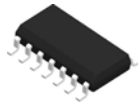
SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

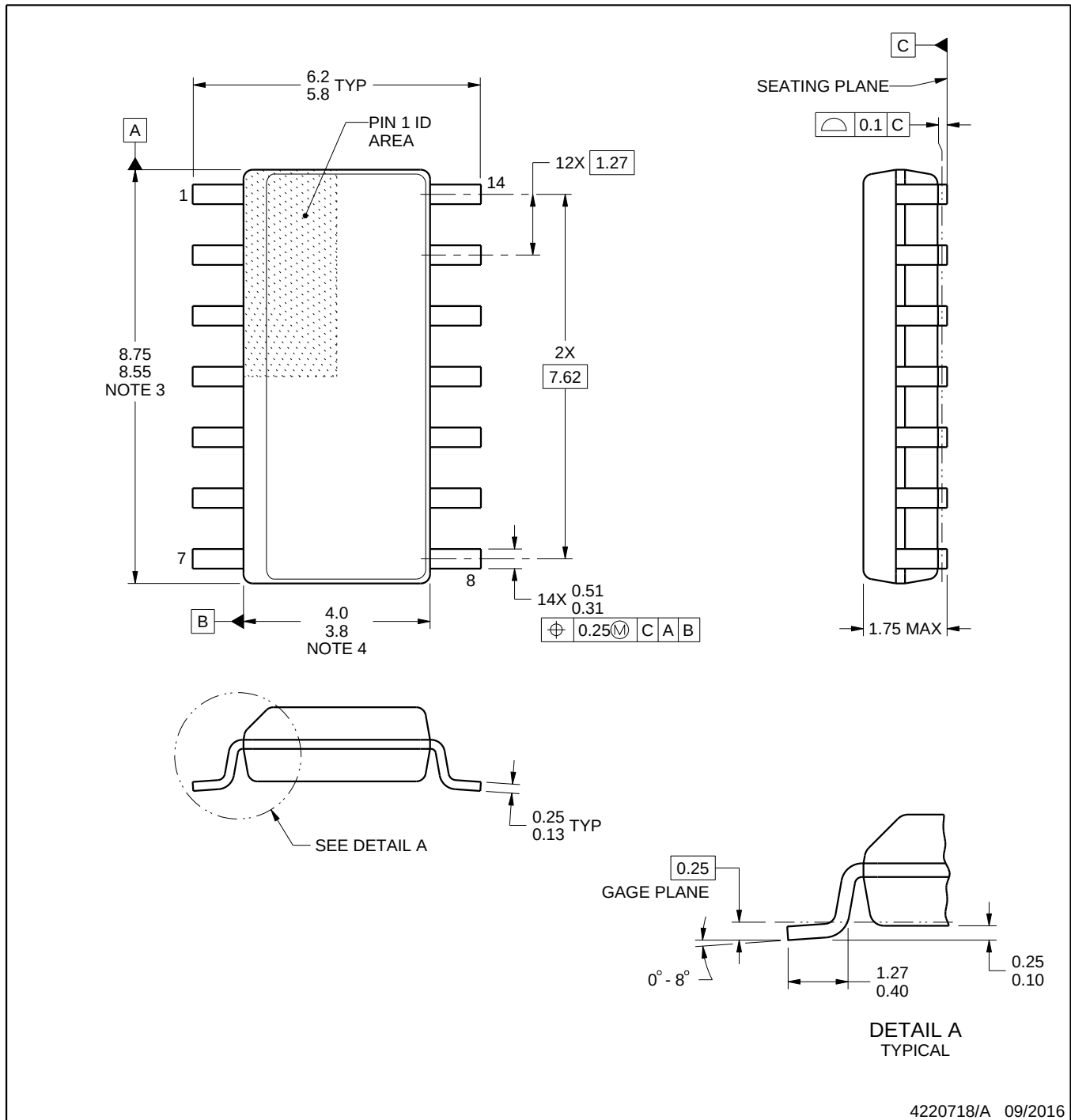
4224938/C 03/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT

**NOTES:**

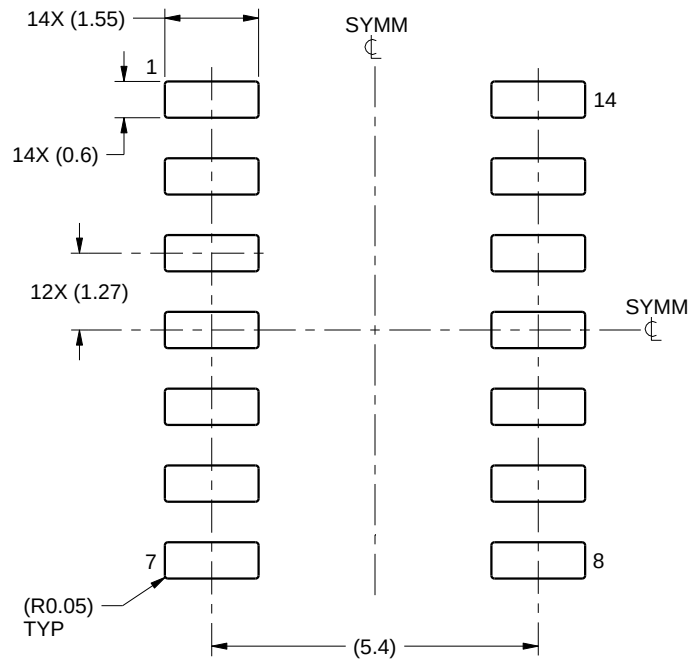
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

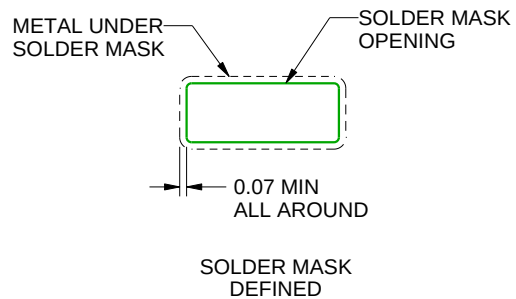
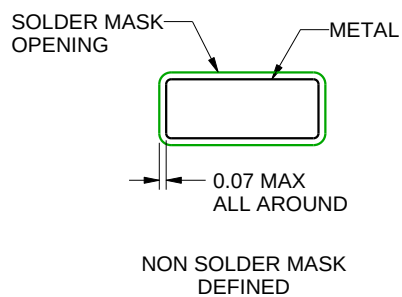
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

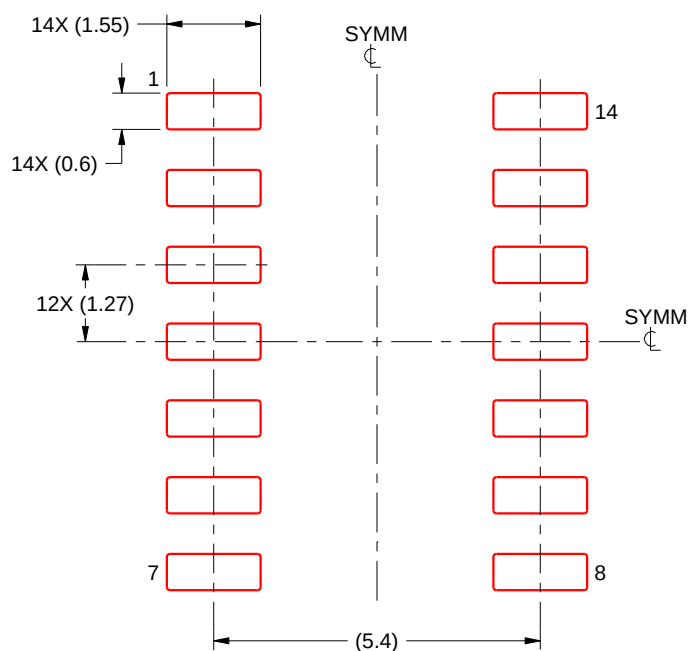
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

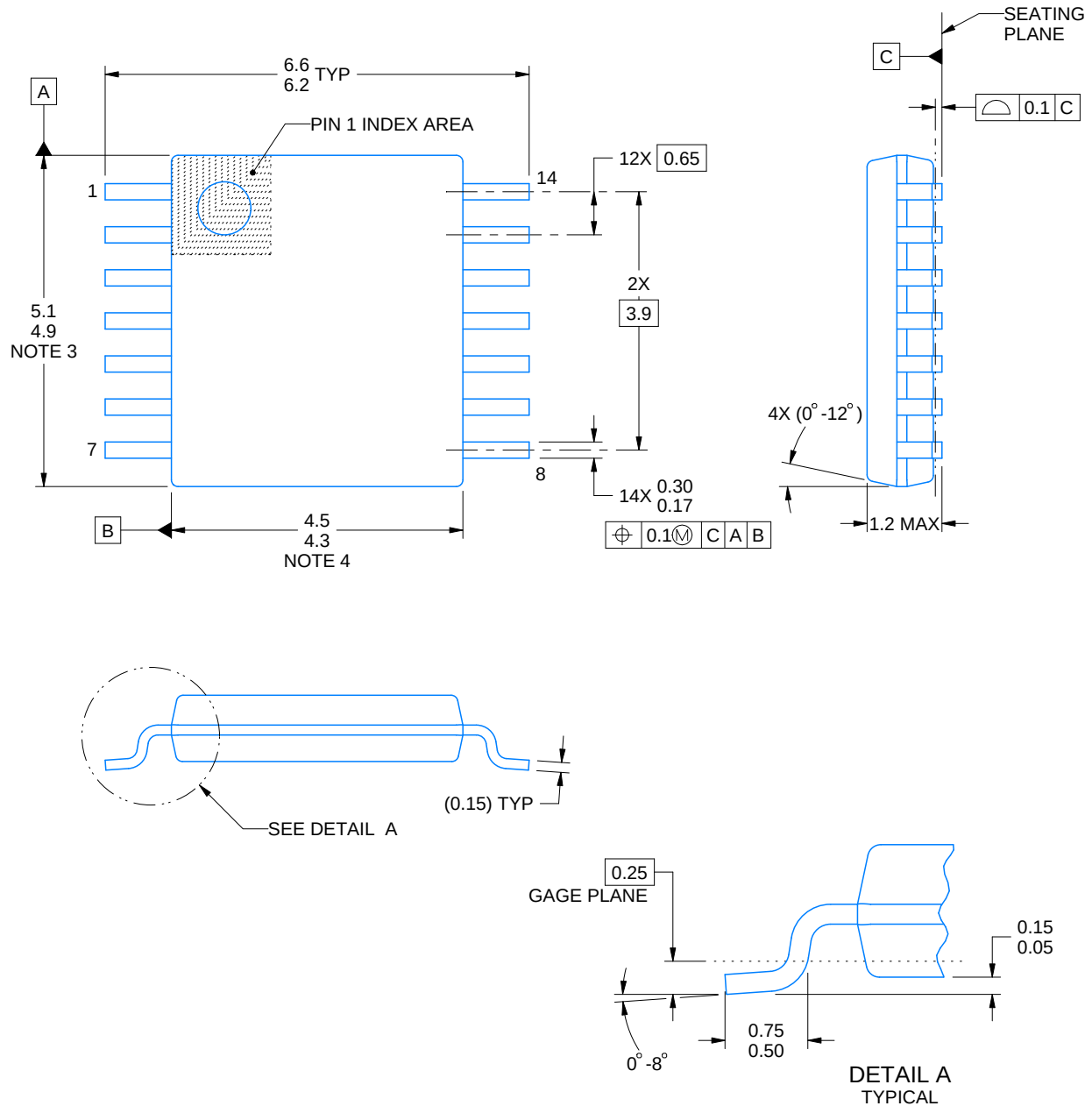
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW0014A

PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

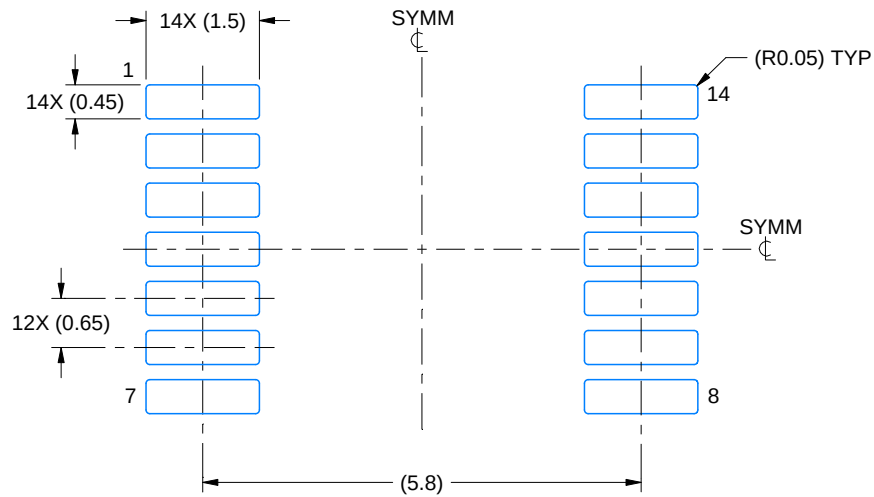
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

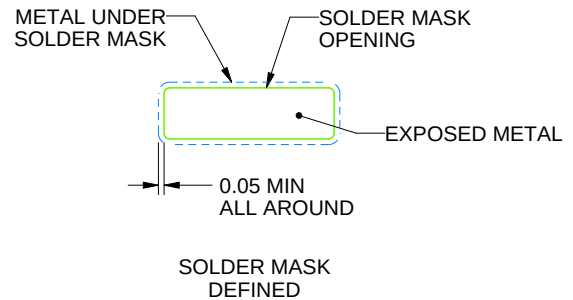
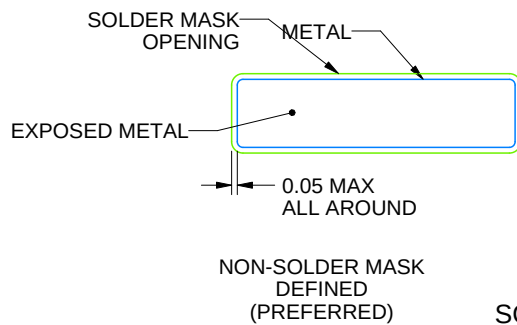
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

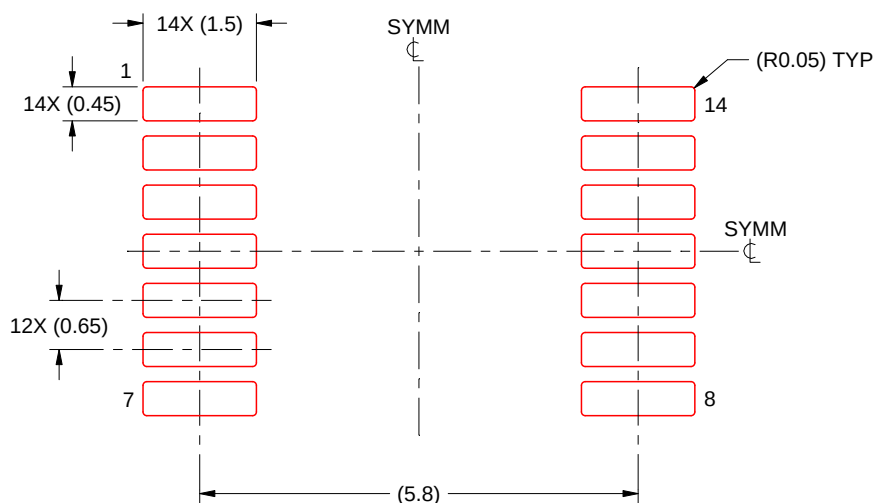
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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