LM3559 Synchronous Boost Flash Driver With Dual 900-mA High-Side Current Sources (1.8-A Total Flash Current)

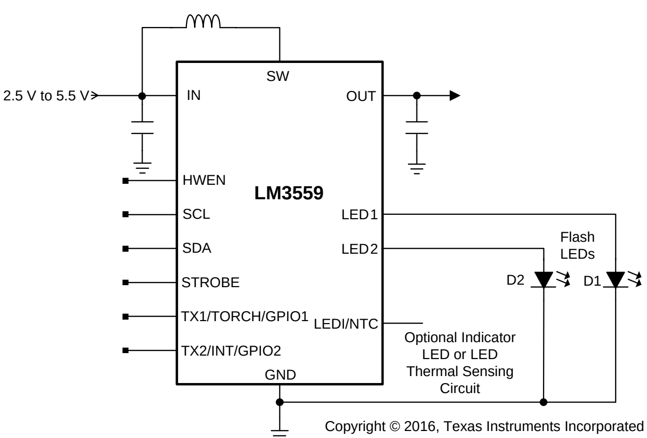
1 Features

- Dual High-Side Current Sources Allow for Grounded Cathode LED Operation
- Accurate and Programmable LED Current from 28.125 mA to 1.8 A
- Optimized Flash Current During Low Battery Conditions
- Independent LED Current Source Programmability
- Four Operating Modes: Torch, Flash, Privacy Indicate, and Message Indicator
- 4-Bit Analog-to-Digital (ADC) for V_{LED} Monitoring
- Battery Voltage Sensing and Current Scale-Back
- LED Sensing and Current Scale-Back
- Hardware Flash and Torch Enable
- Active-Low Hardware Reset
- Dual Synchronization Inputs for RF Power Amplifier Pulse Events
- LED and Output Disconnect During Shutdown
- Open and Short LED Detection
- 400-kHz I^2C-Compatible Interface

2 Applications

- Camera Phone LED Flash
- White LED Biasing

Simplified Schematic



3 Description

The LM3559 is a 2-MHz fixed-frequency synchronous boost converter with two 900-mA constant current drivers for high-current white LEDs. The dual high-side current sources allow for grounded cathode LED operation and can be tied together for providing flash currents of up to 1.8 A. An adaptive regulation method ensures the current for each LED remains in regulation and maximizes efficiency.

The LM3559 is controlled via an I^2C-compatible interface. Features include: an internal 4-bit ADC to monitor the LED voltage, independent LED current control, a hardware flash enable allowing a logic input to trigger the flash pulse, dual TX inputs which force the flash pulse into a low-current torch mode allowing for synchronization to RF power amplifier events or other high-current conditions, an integrated comparator designed to monitor an NTC thermistor and provide an interrupt to the LED current, an input voltage monitor to monitor low battery conditions, and a flash current scale-back feature that actively monitors the battery voltage and optimizes the flash current during low battery-voltage conditions. Additionally, an active high HWEN input provides a hardware shutdown during system software failures.

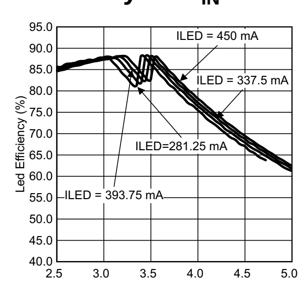
The 2-MHz switching frequency, overvoltage protection, and adjustable current limit allow for the use of tiny, low-profile (1-µH or 2.2-µH) inductors and (10-µF) ceramic capacitors. The device is available in a ultra-small 16-pin DSBGA package (total solution size < 26 mm²) and operates over the –40°C to +85°C temperature range.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM3559	DSBGA (16)	1.96 mm × 1.96 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

LED Efficiency vs V_{IN} Dual LEDs



(Flash Brightness Codes 0x88 - 0xAA)

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2013) to Revision B **Page**

- Added *Device Information* and *Pin Configuration and Functions* sections, *ESD Ratings* and *Thermal Information* tables, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections........ 1
- Added *Thermal Information* table with revised $R_{θJA}$ value (from "50.4°C/W" to "71.3°C/W") and additional thermal values. 4

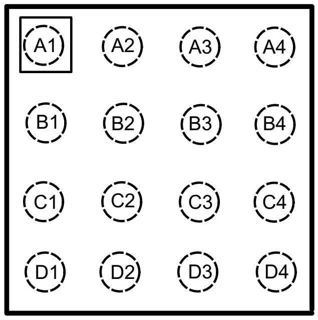
Changes from Original (May 2013) to Revision A **Page**

- Changed layout of National Data Sheet to TI format 42

5 Pin Configuration and Functions

YZR Package
16-Pin DSBGA
Top View

Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
A1	LED1	Power	High-side current source output for flash LED1
A2, B2	OUT	Power	Step-up DC-DC converter output. Connect a 10-µF ceramic capacitor between this pin and GND.
A3, B3	SW	Power	Drain connection for internal NMOS and synchronous PMOS switches
A4, B4	GND	Ground	Ground
B1	LED2	Output	High-side current source output for flash LED2
C1	LEDI/NTC	Input/Output	Configureable as a high-side current source output for indicator LED or comparator input for LED temperature sensing
C2	TX1/TORCH/GPIO1	Input/Output	Configureable as a dual-polarity RF power amplifier synchronization input, a hardware torch mode enable, or as a general purpose logic I/O. This pin has an internal 300-kΩ pulldown to GND.
C3	STROBE	Input	Active high hardware flash enable. Drive STROBE high to turn on the flash current pulse. This pin has an internal 300-kΩ pulldown to GND.
C4	IN	Power	Input voltage connection. Connect IN to the input supply, and bypass to GND with a minimum 10-µF or larger ceramic capacitor.
D1	TX2/INT/GPIO2	Input/Output	Configurable as a dual-polarity power amplifier synchronization input, an interrupt output, or as a general purpose logic I/O. This pin has an internal 300-kΩ pulldown to GND.
D2	SDA	Input/Output	Serial data input output. High impedance in shutdown or in power down.
D3	SCL	Input	Serial clock input. High impedance in shutdown or in power down.
D4	HWEN	Input	Logic high hardware enable. HWEN is a high impedance input and is normally connected with an external pullup resistor to a logic high voltage.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
V_{IN}	–0.3	6	V
V_{SCL}, V_{SDA}, V_{HWEN}, V_{STROBE}, V_{TX1}, V_{TX2}, V_{LED1}, V_{LED2}, $V_{LEDI/NTC}$	–0.3	to the lesser of (V_{IN} + 0.3 V) with 6 V maximum	V
V_{SW}, V_{OUT}	–0.3	6	V
Continuous power dissipation(2)	Internally limited		
Junction temperature, $T_{J\text{-}MAX}$		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typical) and disengages at T_J = 135°C (typical). Thermal shutdown is ensured by design.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Input voltage, V_{IN}	2.5	5.5	V
Junction temperature, T_J	–40	125	°C
Ambient temperature, T_A(1)	–40	85	°C

(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A\text{-}MAX}$) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$), and the junction-to-ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} – (R_{\theta JA} \times P_{D\text{-}MAX})$.

6.4 Thermal Information

THERMAL METRIC(1)		LM3559 YZR (DSBGA) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	71.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	1.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Junction-to-ambient thermal resistance ($R_{\theta JA}$) is taken from a thermal modeling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7. The test board is a 4-layer FR-4 board measuring 102 mm × 76 mm × 1.6 mm with a 2 × 1 array of thermal vias. The ground plane on the board is 50 mm × 50 mm. Thickness of copper layers are 36 µm/18 µm/18 µm/36 µm (1.5 oz/1oz/1oz/1.5 oz). Ambient temperature in simulation is 22°C, still air. Power dissipation is 1 W.

6.5 Electrical Characteristics

Unless otherwise specified, V_{IN} = 3.6 V, V_{HWEN} = V_{IN}, T_A = 25°C.(1) (2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT SOURCE SPECIFICATIONS						
I_{LED}	Current source accuracy	I_{LED1} + I_{LED2}, 3 V ≤ V_{IN} ≤ 4.2 V, V_{OUT} = 4.5 V; 900-mA flash current setting, per current source	–7%	1800	7%	mA
		I_{LED1} + I_{LED2}, 3 V ≤ V_{IN} ≤ 4.2 V, V_{OUT} = 4.5 V; 900-mA flash current setting, per current source –40°C ≤ T_A ≤ 85°C	–4%	1800	4%	mA
		I_{LED1} + I_{LED2}, 3 V ≤ V_{IN} ≤ 4.2 V, V_{OUT} = 4.5 V; 28.125-mA torch current, per current source	–10%	56.2	10%	mA
		I_{LED1} + I_{LED2}, 3 V ≤ V_{IN} ≤ 4.2 V, V_{OUT} = 4.5 V; 28.125-mA torch current, per current source –40°C ≤ T_A ≤ 85°C	–10%	56.2	10%	mA
V_{OUT} – $V_{LED1/2}$	Current source regulation voltage	I_{LED} = 1.8 A (I_{LED1} + I_{LED2}), V_{OUT} = 4.5 V		270		mV
V_{OVP}	Output overvoltage protection trip point(3)	ON threshold		5		V
		ON threshold, –40°C ≤ T_A ≤ 85°C	4.925		5.075	V
		OFF threshold		4.88		V
STEP-UP DC-DC CONVERTER SPECIFICATIONS						
R_{PMOS}	PMOS switch on-resistance	I_{PMOS} = 1A		80		mΩ
R_{NMOS}	NMOS switch on-resistance	I_{NMOS} = 1A		80		mΩ
I_{CL}	Switch current limit(4)	3 V ≤ V_{IN} ≤ 4.2 V; Flash Duration Register bits [6:5] = 00		1.4		A
		3 V ≤ V_{IN} ≤ 4.2 V –40°C ≤ T_A ≤ 85°C; Flash Duration Register bits [6:5] = 00	1.2		1.6	A
		3 V ≤ V_{IN} ≤ 4.2 V; Flash Duration Register bits [6:5] = 01		2.1		A
		3 V ≤ V_{IN} ≤ 4.2 V –40°C ≤ T_A ≤ 85°C; Flash Duration Register bits [6:5] = 01	1.8		2.3	A
		3 V ≤ V_{IN} ≤ 4.2 V; Flash Duration Register bits [6:5] = 10		2.7		A
		3 V ≤ V_{IN} ≤ 4.2 V –40°C ≤ T_A ≤ 85°C; Flash Duration Register bits [6:5] = 10	2.4		3	A
		3 V ≤ V_{IN} ≤ 4.2 V; Flash Duration Register bits [6:5] = 11		3.2		A
		3 V ≤ V_{IN} ≤ 4.2 V –40°C ≤ T_A ≤ 85°C; Flash Duration Register bits [6:5] = 11	2.9		3.5	A
I_{OUT_SC}	Output short-circuit current limit	V_{OUT} < 2.3 V		350		mA
$I_{LEDI/NTC}$	Indicator current	Register 0x12, bits[2:0] = 111, 2.7 V ≤ V_{IN} ≤ 4.2 V $V_{LEDI/NTC}$ = 2 V, –40°C ≤ T_A ≤ 85°C		18		mA
		Register 0x12, bits[2:0] = 111, 2.7 V ≤ V_{IN} ≤ 4.2 V $V_{LEDI/NTC}$ = 2 V	16		20	mA
V_{TRIP}	Comparator trip threshold	Configuration register 1, bit [4] = 1, 3 V ≤ V_{IN} ≤ 4.2 V		1		V
		Configuration register 1, bit [4] = 1, 3 V ≤ V_{IN} ≤ 4.2 V, –40°C ≤ T_A ≤ 85°C	0.97		1.03	V

(1) All voltages are with respect to the potential at the GND pin.
(2) Minimum (MIN) and maximum (MAX) limits are specified by design, test, or statistical analysis. Typical (TYP) numbers represent the most likely norm. Unless otherwise stated, conditions for typical specifications are: V_{IN} = 3.6 V and T_A = 25°C.
(3) The typical curve for overvoltage protection (OVP) is measured in closed loop using *Figure 43* . The OVP value is found by forcing an open circuit in the LED1 and LED2 path and recording the peak value of V_{OUT}. The value given in *Electrical Characteristics* is found in an open loop configuration by ramping the voltage at OUT until the OVP comparator trips. The closed loop data can appear higher due to the stored energy in the inductor being dumped into the output capacitor after the OVP comparator trips. Worst case is an open circuit condition where the output voltage can continue to rise after the OVP comparator trips by approximately I_{IN} × sqrt(L/C_{OUT}).
(4) The typical curve for current limit is measured in closed loop using *Figure 43*, and increasing I_{OUT} until the peak inductor current stops increasing. The value given in *Electrical Characteristics* is measured open loop and is found by forcing current into SW until the current limit comparator threshold is reached. Closed loop data appears higher due to the delay between the comparator trip point and the NFET turning off. This delay allows the closed loop inductor current to ramp higher after the trip point by approximately 20 ns × V_{IN}/L.

Electrical Characteristics (continued)

Unless otherwise specified, V_{IN} = 3.6 V, V_{HWEN} = V_{IN}, T_A = 25°C.(1) (2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{SW}	Switching frequency	2.7 V ≤ V_{IN} ≤ 5.5 V			2		MHz
		2.7 V ≤ V_{IN} ≤ 5.5 V, –40°C ≤ T_A ≤ 85°C		1.8		2.2	MHz
I_Q	Quiescent supply current	Device not switching, V_{OUT} = 3V			650		µA
		Device switching, V_{OUT} = 4.5V			1.55		mA
		Indicate mode, Indicator Register bits [2:0] = 111 $V_{LEDI/NTC}$ = 2 V			590		µA
		Indicate mode, Indicator Register bits [2:0] = 111 $V_{LEDI/NTC}$ = 2 V, –40°C ≤ T_A ≤ 85°C				750	µA
I_{SHDN}	Shutdown supply current	2.7 V ≤ V_{IN} ≤ 5.5 V, –40°C ≤ T_A ≤ 85°C	HWEN = GND			1	µA
I_{STBY}	Standby supply current	2.7 V ≤ V_{IN} ≤ 5.5 V	HWEN = V_{IN}, Enable Register bits [1:0] = 00		1.25		µA
		2.7 V ≤ V_{IN} ≤ 5.5 V, –40°C ≤ T_A ≤ 85°C	HWEN = V_{IN}, Enable Register bits [1:0] = 00			2.4	µA
V_{IN_TH}	VIN monitor threshold	VIN Monitor Register = 0x01			2.9		V
		VIN Monitor Register = 0x01, –40°C ≤ T_A ≤ 85°C		2.85		2.95	V
$V_{IN\_FLASH\_TH}$	VIN flash monitor threshold	VIN Monitor Register = 0x08			2.9		V
		VIN Monitor Register = 0x08, –40°C ≤ T_A ≤ 85°C		2.85		2.95	V
t_{TX}	Flash-to-torch LED current settling time	TX_ Low to High I_{LED1} + I_{LED2} = 1.8A to 112.5mA			20		µs
t_D	Time from when I_{LED} hits target until VLED data is available	ADC Delay Register bit [5] = 1			16		µs
		ADC Delay Register bit [5] = 0 ADC Delay Register bits [4:0] = 0000			250		µs
V_{F_ADC}	ADC threshold	VLED Monitor Register bits [3:0] = 1111			4.6		V
		VLED Monitor Register bits [3:0] = 1111 –40°C ≤ T_A ≤ 85°C		4.4		4.8	V
HWEN, STROBE, TX1/TORCH/GPIO1, TX2/INT/GPIO2 VOLTAGE SPECIFICATIONS							
V_{IL}	Input logic low	2.7 V ≤ V_{IN} ≤ 5.5 V, –40°C ≤ T_A ≤ 85°C		0		0.4	V
V_{IH}	Input logic high	2.7 V ≤ V_{IN} ≤ 5.5 V, –40°C ≤ T_A ≤ 85°C		1.2		V_{IN}	V
R_{PD}	Internal pulldown resistance on TX1, TX2, STROBE				300		kΩ
I²C-COMPATIBLE VOLTAGE SPECIFICATIONS (SCL, SDA)							
V_{IL}	Input logic low	2.7 V ≤ V_{IN} ≤ 5.5 V, –40°C ≤ T_A ≤ 85°C		0		0.4	V
V_{IH}	Input logic high	2.7 V ≤ V_{IN} ≤ 5.5 V		1.3		V_{IN}	V
V_{OL}	Output logic low (SDA)	I_{LOAD} = 3 mA 2.7 V ≤ V_{IN} ≤ 5.5 V, –40°C ≤ T_A ≤ 85°C				0.4	V

6.6 I²C Timing Requirements (SCL, SDA)

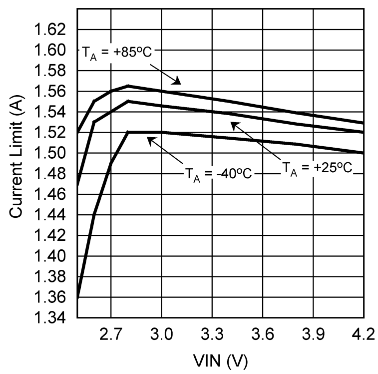
See(1)

		MIN	NOM	MAX	UNIT
$1/t_1$	SCL(clock frequency)		400		kHz
t_2	Data in setup time to SCL high	100			ns
t_3	Data out stable after SCL low	0			ns
t_4	SDA low setup time to SCL low (start)	100			ns
t_5	SDA high hold time after SCL high (stop)	100			ns

(1) Specified by design, not production tested.

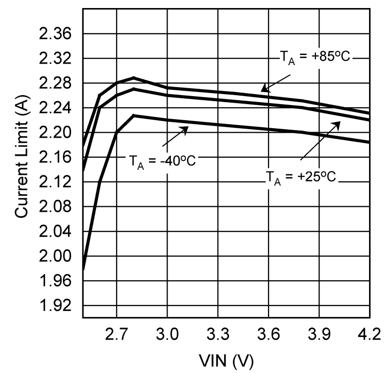
7 Typical Characteristics

Unless otherwise specified: V_{IN} = 3.6 V, C_{OUT} = 10 µF, C_{IN} = 10 µF, L = 1 µH (TOKO FDSD0312-1R0, R_L = 43 mΩ), *Figure 43*.



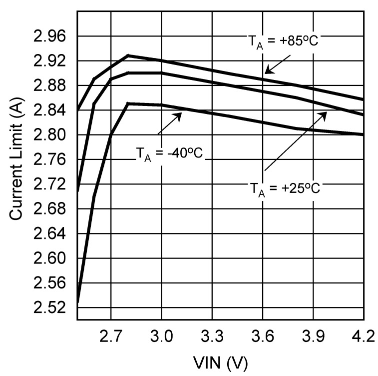
Register Bits [6:5] = 00

Figure 1. Closed Loop Current Limit vs V_{IN} Flash Duration



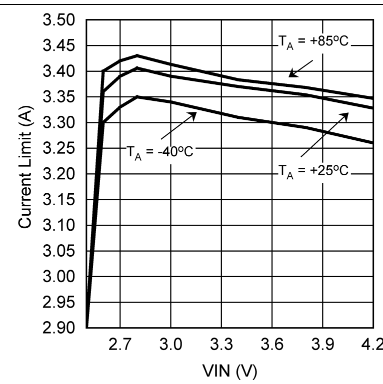
Register Bits [6:5] = 01

Figure 2. Closed Loop Current Limit vs V_{IN} Flash Duration



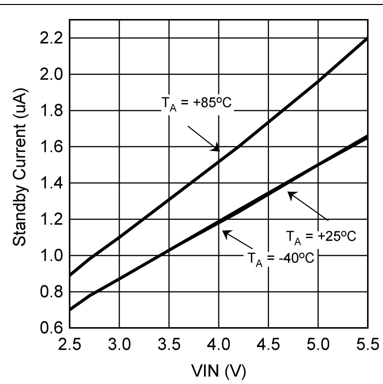
Register Bits [6:5] = 10

Figure 3. Closed Loop Current Limit vs V_{IN} Flash Duration



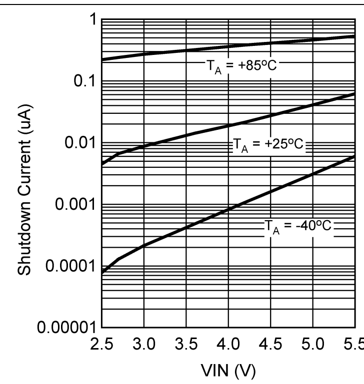
Register Bits [6:5] = 11

Figure 4. Closed Loop Current Limit vs V_{IN} Flash Duration



Enable Register = 0x18

Figure 5. Standby Current vs V_{IN} V_{HWEN} = V_{IN}



V_{HWEN}= 0 V

Figure 6. Shutdown Current vs V_{IN}

Typical Characteristics (continued)

Unless otherwise specified: V_{IN} = 3.6 V, C_{OUT} = 10 µF, C_{IN} = 10 µF, L = 1 µH (TOKO FDSD0312-1R0, R_L = 43 mΩ), *Figure 43*.

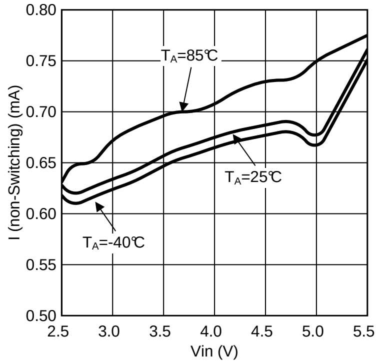


Figure 7. Non-Switching Current vs V_{IN}

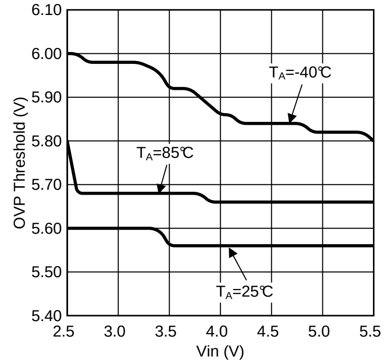


Figure 8. OVP Thresholds vs V_{IN}

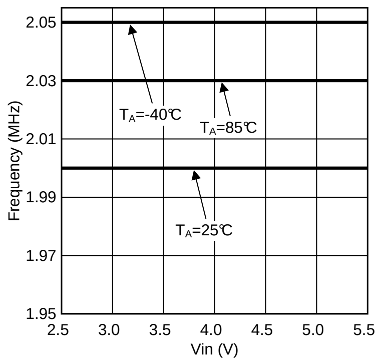
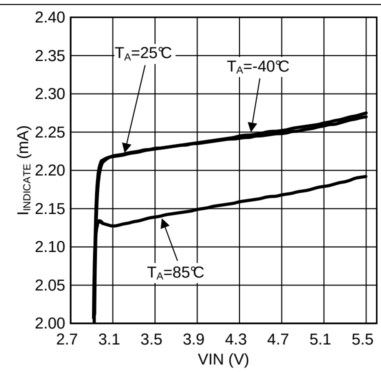
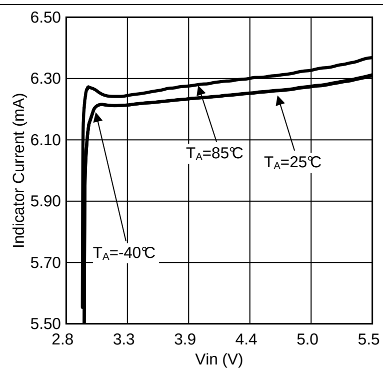


Figure 9. Switching Frequency vs V_{IN}



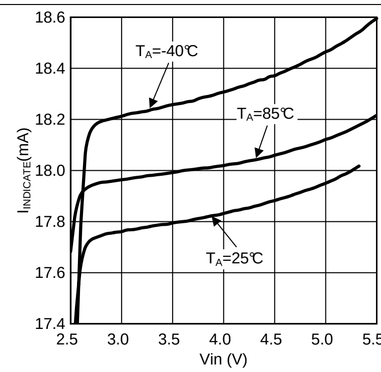
Register Bits [2:0] = 0x00

Figure 10. Indicator Currents vs V_{IN} Indicator



Register Bits [2:0] = 0x02

Figure 11. Indicator Current vs V_{IN} Indicator

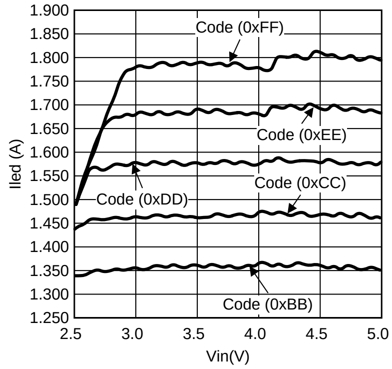


Register Bits [2:0] = 0x07

Figure 12. Indicator Current vs V_{IN} Indicator

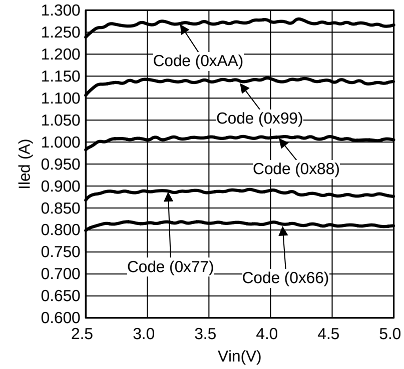
Typical Characteristics (continued)

Unless otherwise specified: V_{IN} = 3.6 V, C_{OUT} = 10 µF, C_{IN} = 10 µF, L = 1 µH (TOKO FDSD0312-1R0, R_L = 43 mΩ), *Figure 43*.



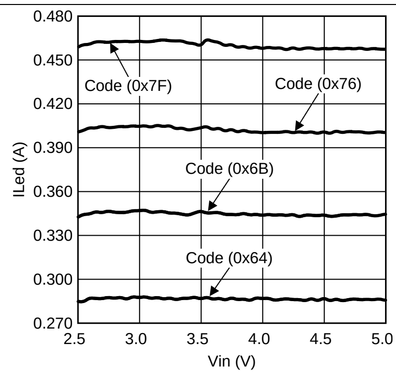
Upper 5 Flash Brightness Codes

Figure 13. I_{LED} (Flash Mode) vs V_{IN} LED1 and LED2 Connected Together



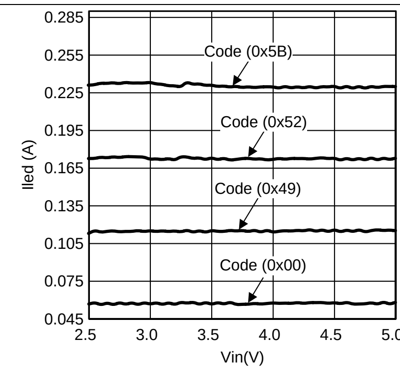
Middle 5 Flash Brightness Codes

Figure 14. I_{LED} (Flash Mode) vs V_{IN} LED1 and LED2 Connected Together



Upper 4 Torch Brightness Codes

Figure 15. I_{LED} (Torch Mode) vs V_{IN} LED1 and LED2 Connected Together



Lower 4 Torch Brightness Codes

Figure 16. I_{LED} (Torch Mode) vs V_{IN} LED1 and LED2 Connected Together

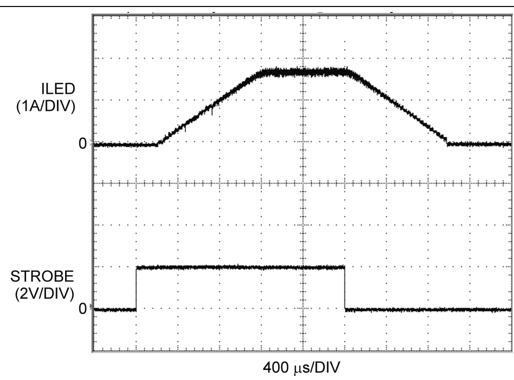


Figure 17. Strobe High-to-Flash LED Current

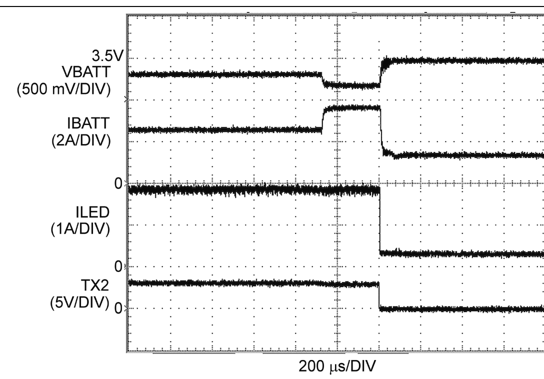


Figure 18. V_{IN} Monitor Operation

Typical Characteristics (continued)

Unless otherwise specified: V_{IN} = 3.6 V, C_{OUT} = 10 µF, C_{IN} = 10 µF, L = 1 µH (TOKO FDSD0312-1R0, R_L = 43 mΩ), *Figure 43*.

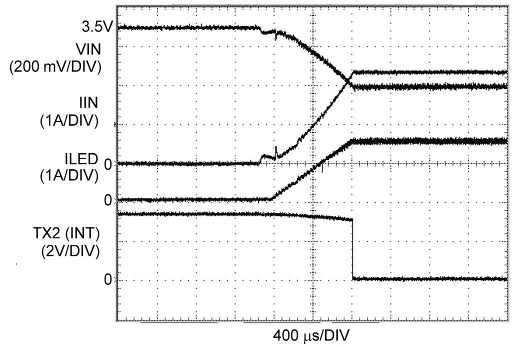


Figure 19. V_{IN} Flash Monitor Operation

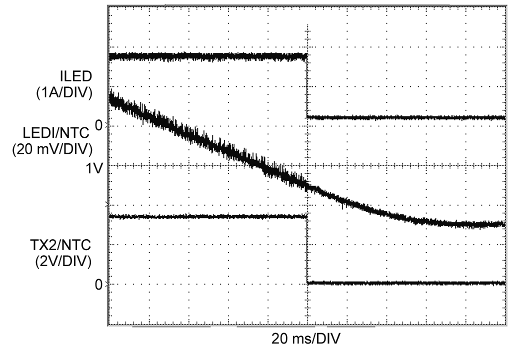


Figure 20. NTC-Mode Operation

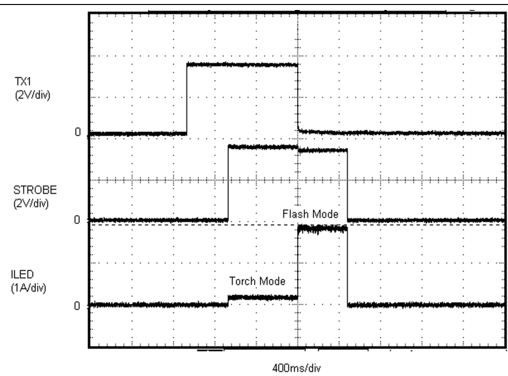


Figure 21. AET-Mode Operation

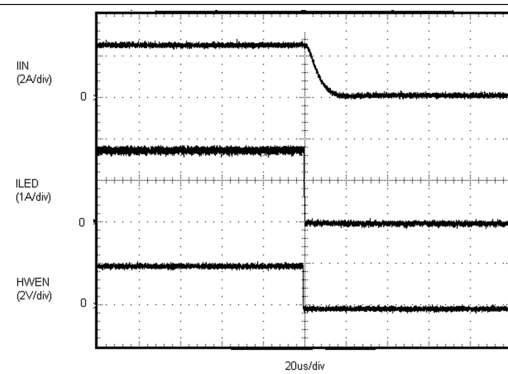


Figure 22. HWEN Operation Device Enabled in Flash Mode

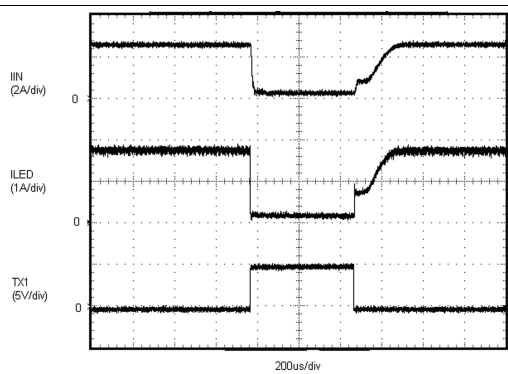
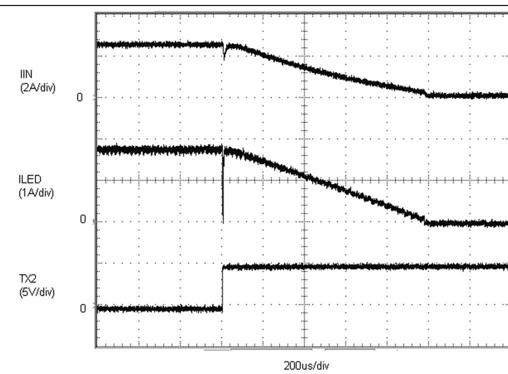


Figure 23. TX1 Interrupt (Force Torch)



TX2 Active High

Figure 24. TX2 Interrupt (Forced Shutdown)

(1) The typical curve for current limit is measured in closed loop using *Figure 43*, and increasing I_{OUT} until the peak inductor current stops increasing. The value given in *Electrical Characteristics* is measured open loop and is found by forcing current into SW until the current limit comparator threshold is reached. Closed loop data appears higher due to the delay between the comparator trip point and the NFET turning off. This delay allows the closed loop inductor current to ramp higher after the trip point by approximately 20 ns × V_{IN}/L.

(2) The typical curve for overvoltage protection (OVP) is measured in closed loop using *Figure 43* . The OVP value is found by forcing an open circuit in the LED1 and LED2 path and recording the peak value of V_{OUT}. The value given in *Electrical Characteristics* is found in an open loop configuration by ramping the voltage at OUT until the OVP comparator trips. The closed loop data can appear higher due to the stored energy in the inductor being dumped into the output capacitor after the OVP comparator trips. Worst case is an open circuit condition where the output voltage can continue to rise after the OVP comparator trips by approximately I_{IN} × sqrt(L/C_{OUT}).

8 Detailed Description

8.1 Overview

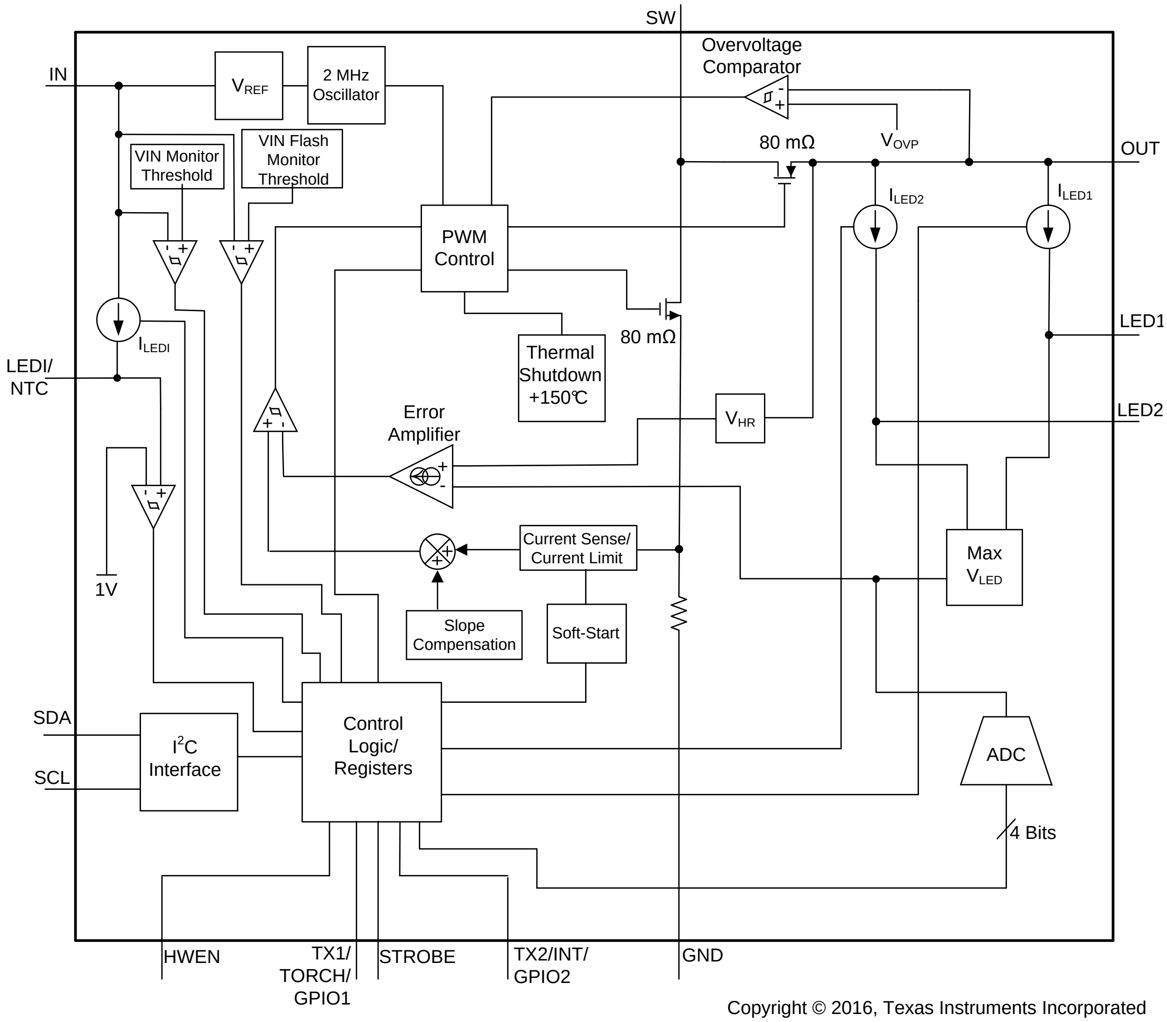
The LM3559 is a high-power white LED flash driver capable of delivering up to 1.8 A of LED current into a single LED, or up to 900 mA into two parallel LEDs. The device incorporates a 2-MHz constant frequency, synchronous boost converter, and two high-side current sources to regulate the LED current over the 2.5-V to 5.5-V input voltage range.

During operation when the output voltage is greater than V_{IN} – 150 mV, the boost converter switches and maintains at least 270 mV across both current sources (LED1 and LED2). This minimum headroom voltage ensures that the current sinks remain in regulation. When the input voltage rises above the LED voltage + current source headroom voltage, the device stops switching and turns the PFET on continuously (pass mode). In pass mode the difference between (V_{IN} - I_{LED} × R_{ON_P}) and the voltage across the LEDs is dropped across the current sources.

Four hardware control pins provide control of the LM3559 device. These include a hardware flash enable (STROBE), dual flash-interrupt inputs (TX1 and TX2) designed to interrupt the flash pulse during high-battery current conditions, and a logic high hardware enable (HWEN) that can be pulled low to rapidly place the device into shutdown. Additional features of the LM3559 include an internal 4-bit ADC for LED voltage monitoring, an internal comparator for LED thermal sensing via an external NTC thermistor, a battery voltage monitor during flash current turnon which monitors VIN and optimizes the flash current during low-battery voltage conditions, an input voltage monitor that can force torch mode or LED shutdown of the flash current during input undervoltage conditions, a low-power Indicator current source with programmable patterns, and a mode for utilizing the flash LEDs as a privacy indicator.

Control of the LM3559 is done via an I^2C-compatible interface. This includes adjustment of the flash and torch current levels, adjustment of the indicator LED currents and indicator pattern, changing the flash timeout duration, changing the switch current limit, and reading back the ADC results. Additionally, there are 8 flag bits that indicate flash current timeout, LED overtemperature, LED failure (by sensing LED short or output OVP condition during flash, torch, or privacy modes), device thermal shutdown, V_{IN} undervoltage condition, tripping of the VIN flash monitor, and the occurrence of a TX interrupt (both TX1 and TX2).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Power Amplifier Synchronization (TX1)

The TX1/TORCH/GPIO1 pin has a triple function. With the Configuration Register 1 Bit [7] = 0 (default) TX1/TORCH/GPIO1 is a power-amplifier-synchronization input. This mode is designed to reduce the flash LED current when TX1 is pulled high (active high polarity) or low (active low polarity). When the LM3559 is engaged in a flash event and the TX1/TORCH pin is pulled high, both LED1 and LED2 are forced into torch mode at the programmed torch current setting. If TX1 is then pulled low before the flash pulse terminates, the LED current returns to the previous flash current level. At the end of the flash timeout, whether the TX1/TORCH pin is high or low, the current sources turn off.

The polarity of the TX1 input can be changed from active high to active low by writing a 0 to bit [5] of Configuration Register 1. With this bit set to 0 the LM3559 is forced into torch mode when TX1/TORCH is pulled low. Figure 25 details the functionality of the TX1 interrupt.

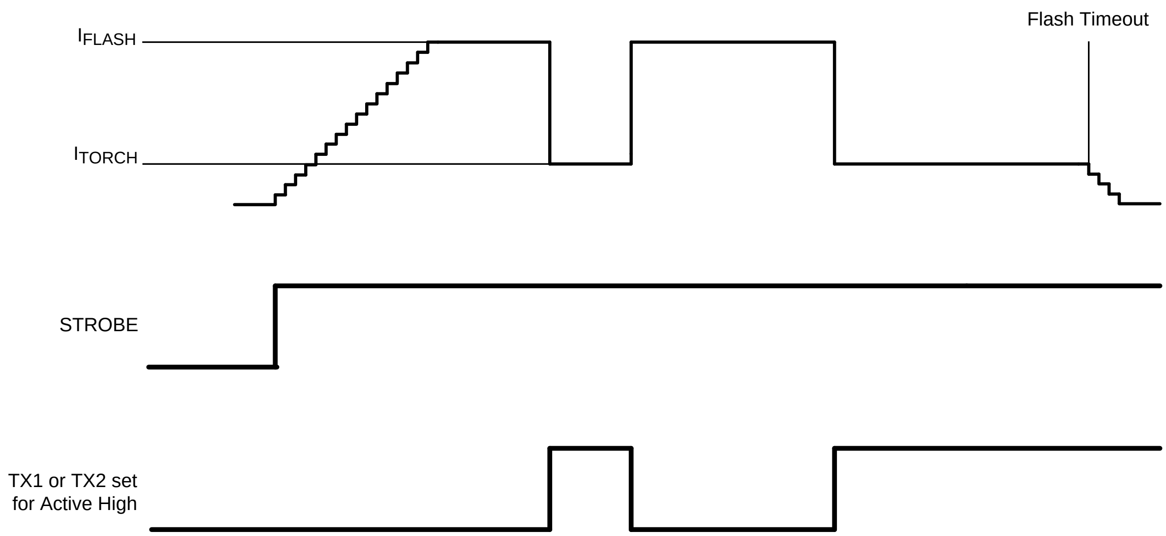


Figure 25. TX1 or TX2 Interrupt Event

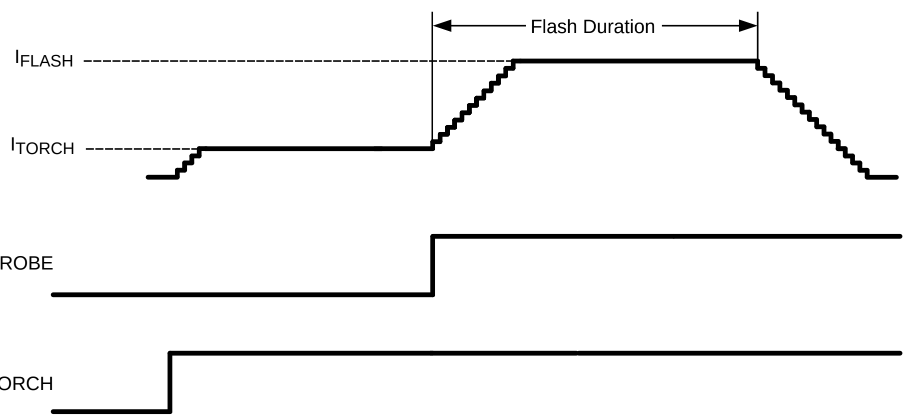


Figure 26. Hardware-Torch Mode

8.3.2 Input Voltage Flash Monitor Fault

The V_{IN} flash monitor flag (bit [6] of the Flags Register reads back a 1 when the input voltage flash monitor is enabled and V_{IN} falls below the programmed V_{IN} flash monitor threshold. This flag must be read back in order to resume normal operation after the LED current has been forced to the lower flash current setting.

Feature Description (continued)

8.3.3 Independent LED Control

Bits [4:3] of the enable register provide for independent turnon and turnoff of the LED1 or LED2 current sources. The LED current is adjusted by writing to the Torch Brightness or Flash Brightness Registers. Both the Torch Brightness and the Flash Brightness Register provide for independent current programming for the LED currents in either LED1 or LED2. (See *Torch Brightness Register* and *Flash Brightness Register* descriptions.)

8.3.4 Hardware Torch

With Configuration Register 1 Bit [7] = 1, TX1/TORCH is configured as a hardware-torch-mode enable. In this mode (TORCH mode), a high at TX1/TORCH turns on the LED current at the programmed torch current setting. The STROBE input and I^2C-enabled flash takes precedence over torch mode. In hardware-torch mode, both LED1 and LED2 current sources turn off after a flash event ,and Configuration Register 1 Bit [7] is reset to 0. In this situation, to re-enter torch mode via hardware torch, the hardware-torch enable bit (Configuration Register 1 Bit [7]) must be reset to 1. Figure 26 details the functionality of the TX1/TORCH/GPIO1 input.

8.3.5 Fault Protections

8.3.5.1 Overvoltage Protection

The output voltage is limited to typically 5 V (5.075 V maximum). In situations such as the current source open, the LM3559 raises the output voltage in order to keep the LED current at its target value. When V_{OUT} reaches 5 V the overvoltage comparator trips and turns off both the internal NFET and PFET switches. When V_{OUT} falls below 4.88 V (typical), the LM3559 begins switching again.

8.3.5.2 Current Limit

The LM3559 features 4 selectable current limits: 1.4 A, 2.1 A, 2.7 A, and 3.2 A. These are programmable through the I^2C-compatible interface via bits [6:5] of the Flash Duration Register. When the current limit is reached, the LM3559 stops switching for the remainder of the switching cycle.

Since the current limit is sensed in the NMOS switch there is no mechanism to limit the current when the device operates in pass mode. In situations where there could potentially be large load currents at OUT and the LM3559 is operating in pass mode, the load current must be limited to 3 A. In boost mode or pass mode, if V_{OUT} falls below approximately 2.3 V the part stops switching, and the PFET operates as a current source, limiting the current to typically 350 mA. This prevents damage to the LM3559 and prevents excessive current draw from the battery during output short-circuit conditions.

8.3.5.3 Flash Timeout

The flash-timeout period sets the amount of time that the flash current is being sourced from current sources LED1 and LED2. Bits [4:0] of the Flash Duration Register set the flash-timeout period. There are 32 different flash-timeout durations in steps of 32 ms giving a flash timeout range of 32 ms to 1024 ms (see Table 5).

8.3.5.4 Indicator LED/Thermistor (LEDI/NTC)

The LEDI/NTC pin serves a dual function, either as a programmable LED message indicator driver, or as a comparator input for negative temperature coefficient (NTC) thermistors.

8.3.5.4.1 Message Indicator Current Source (LEDI/NTC)

LEDI/NTC is configured as a message indicator current source by setting Configuration Register 1 bit [4] = 0. The indicator current source is enabled/disabled via Enable Register bit [6]. Enable Register bit [7] programs the message indictor for blinking mode. When the message indicator is set for blinking mode the pattern programmed into the Indicator Register and Indicator Blinking Register is sent to the message indicator current source.

The Indicator Blinking Register controls the following (see Table 17):

1. Number of blank periods (BLANK#. This has 16 settings. t_{BLANK} = t_{ACTIVE} × BLANK# , where t_{ACTIVE} = t_{PERIOD} × PERIOD#
2. Pulse width (t_{PULSE}) has 16 settings between 0 and 480 ms in steps of 32 ms. The pulse width is the duration which the indicator current is at its programmed set point at the end of the ramp-up time.

Feature Description (continued)

The Indicator Register controls the following (see Table 16):

1. Indicator current level (I_{IND}). There are 8 message indicator current levels from 2.25 mA to 18 mA in steps of 2.25 mA.
2. Number of periods (PERIOD#). This has 8 steps. A period (t_{PERIOD}) is found by ($t_{PERIOD} = t_R + t_F + 2 \times t_{PULSE}$). (See Figure 27 for indicator timing).
3. Ramp times (t_R or t_F) for turnon and turnoff of the indicator current source. Four programmable times of 78 ms, 156 ms, 312 ms, and 624 ms are available. The ramp times apply for both ramp-up and ramp-down and are not independently changeable.

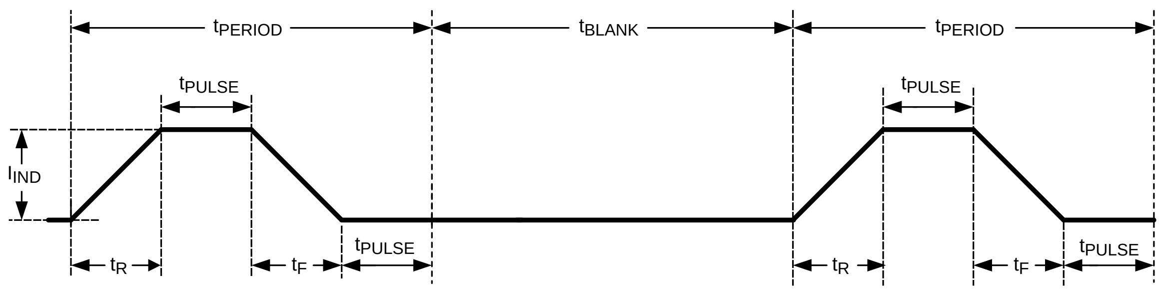


Figure 27. Message Indicator Timing Diagram

8.3.5.4.1.1 *Message Indicator Example 1 (Single Pulse With Dead Time):*

As an example, to set up the message indicator for a 312-ms ramp-up and ramp-down, 192 ms pulse width, and 1 pulse followed by a 5-s delay. The indicator settings will be as follows. $t_R = t_F = 312$ ms, $t_{WIDTH} = 192$ ms ($t_{PERIOD} = 312$ ms × 2 + 192 ms × 2 = 1016 ms). BLANK# setting will be: 5 s / 1016 ms × 1 (PERIOD# = 1). Giving a BLANK# setting of 5. The resulting waveform appears as shown in Figure 28.

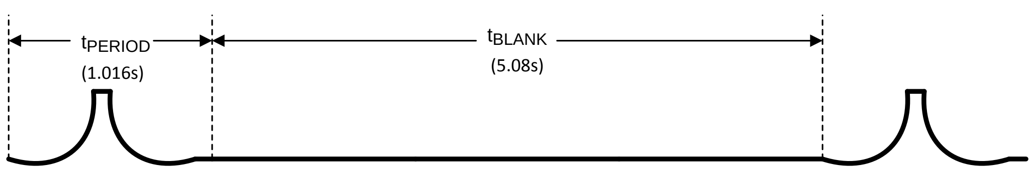


Figure 28. Message Indicator Example 1

8.3.5.4.1.2 *Message Indicator Example 2 (Multiple Pulses With Dead Time):*

Another example has the same t_R, t_F, t_{PULSE}, and t_{BLANK} times as before, but this time the PERIOD# is set to 3. Now the t_{ACTIVE} time is t_{PERIOD} × 3 = 1016 ms × 3 = 3048 ms. This results in a blank time of $t_{BLANK} = t_{ACTIVE}$ × BLANK# = 3.048 s × 5 = 15.24 s (see Figure 29).

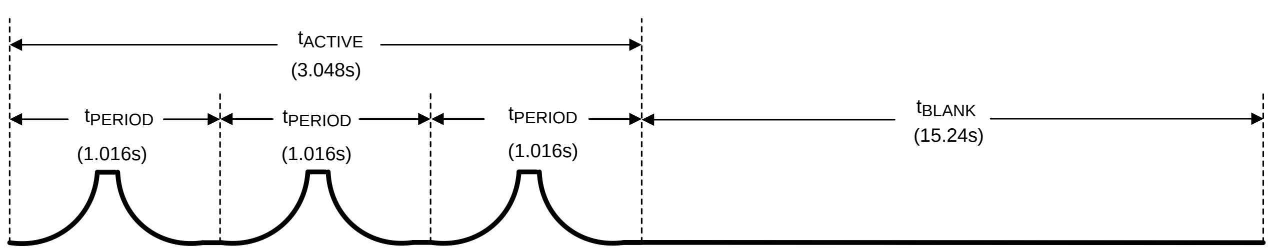


Figure 29. Message Indicator Example 2

Feature Description (continued)

8.3.5.4.1.3 Updating The Message Indicator

The best way to update the message indicator is to disable the message indicator output via the Enable Register bit [7], write the new sequence to the Indicator Register and/or Indicator Blinking Register, and then re-enable the message indicator. Updating the Indicator Registers on the fly can lead to long delays between pattern changes. This is especially true if the PERIOD# or BLANK# setting is changed from a high setting to a lower setting.

8.3.6 Input Voltage (V_{IN}) Monitor

The LM3559 has an internal comparator at IN that monitors the input voltage and can force the LED current into torch mode or into shutdown, if V_{IN} falls below the programmable V_{IN} monitor threshold. Bit 0 in the V_{IN} Monitor Register enables or disables this feature. Bits [2:1] of the VIN Monitor Register program the 4 adjustable thresholds of 2.9 V, 3 V, 3.1 V, and 3.2 V. Bit 3 in Configuration Register 2 selects whether an undervoltage event forces torch mode or forces the LEDs off. See Table 13 for additional information. When the V_{IN} monitor is active and V_{IN} falls below the programmed VIN Monitor threshold, the active current sources (LED1 and/or LED2) either turns off or is forced into the torch current setting. To reset the LED current to its previous level, V_{IN} must go above the V_{IN} monitor threshold and the Flags Register must be read back. See Figure 30 for the V_{IN} monitor timing waveform.

To avoid noise from falsely triggering the V_{IN} monitor, this mode incorporates a 250 µs deglitch timer. With the V_{IN} monitor active, V_{IN} must go below the VIN monitor threshold (V_{IN_TH}) and remain below it for 250 µs before the LEDs are forced into torch mode (or shut down) and the V_{IN} monitor flag is written.

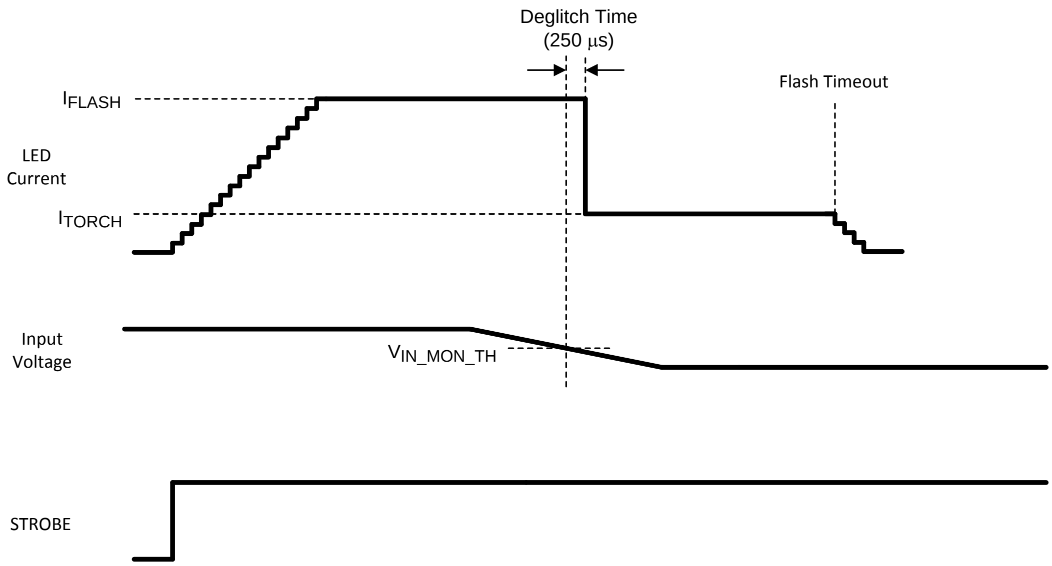


Figure 30. V_{IN} Monitor Waveform

8.3.7 V_{IN} Flash Monitor (Flash Current Rising)

A second comparator at IN is available to monitor the input voltage during the flash current turnon. Bit [3] of the VIN Monitor Register enables/disables this feature. With this bit set to 1 the V_{IN} flash monitor is active. Bits [5:4] of the VIN Monitor Register program the 4 selectable thresholds of (2.9 V, 3 V, 3.1 V, and 3.2 V). The feature operates as follows: during flash current turnon the active current sources (LED1 and/or LED2) transition through each of the lower flash and torch current levels until the target flash current is reached. With the V_{IN} flash monitor active, if the input voltage falls below the V_{IN} flash monitor threshold during the flash current turnon,the flash current is set to the level that the current ramp had risen to at the time of the undervoltage event. The V_{IN} flash monitor only operates during the ramping up of the flash LED current.

The V_{IN} flash monitor ignores the first 2 flash codes during the flash pulse turnon. As a result, if the V_{IN} flash monitor is enabled, and V_{IN} were to fall below the V_{IN} flash threshold as the LED current ramps up through either of the first two levels, then the flash pulse would not be halted until code #3 (168.75-mA per current source).

Feature Description (continued)

To avoid noise from falsely triggering the V_{IN} flash monitor, this mode incorporates an 8-µs deglitch timer as well as an internal analog filter at the input of the V_{IN} flash monitor comparator. With the V_{IN} flash monitor active, V_{IN} must go below the V_{IN} flash monitor threshold (V_{IN_FLASH}) and remain below it for 8 µs before the flash current ramp is halted and the V_{IN} flash monitor flag is written.

8.3.8 Last Flash Register

Once the V_{IN} flash monitor is tripped, the flash code that corresponded to the LED current at which the flash current ramp was halted is written to the Last Flash Register. The Last Flash Register is a read-only register; the lower 4 bits are available to latch the code for LED1 and the upper 4 bits to latch the code for LED2.

For example, suppose that the LM3559 device is set up for a single LED with a target flash current of 1125 mA. The V_{IN} flash monitor is enabled with the V_{IN} flash monitor threshold set to 3. V (VIN Monitor Register bits [5:4] = 0, 1). When the STROBE input is brought high, the LED current begins ramping up through the torch and flash codes at 32 µs per code. As the input current increases, the input voltage at the device IN pin begins to fall due to the source impedance of the battery. By the time the LED current has reached 900 mA (code 0x77 or 450 mA per current source), V_{IN} falls below 3 V. The V_{IN} flash monitor then stops the flash current ramp and the device continues to proceed with the flash pulse, but at 900 mA instead of 1125 mA. Figure 31 details this sequence.

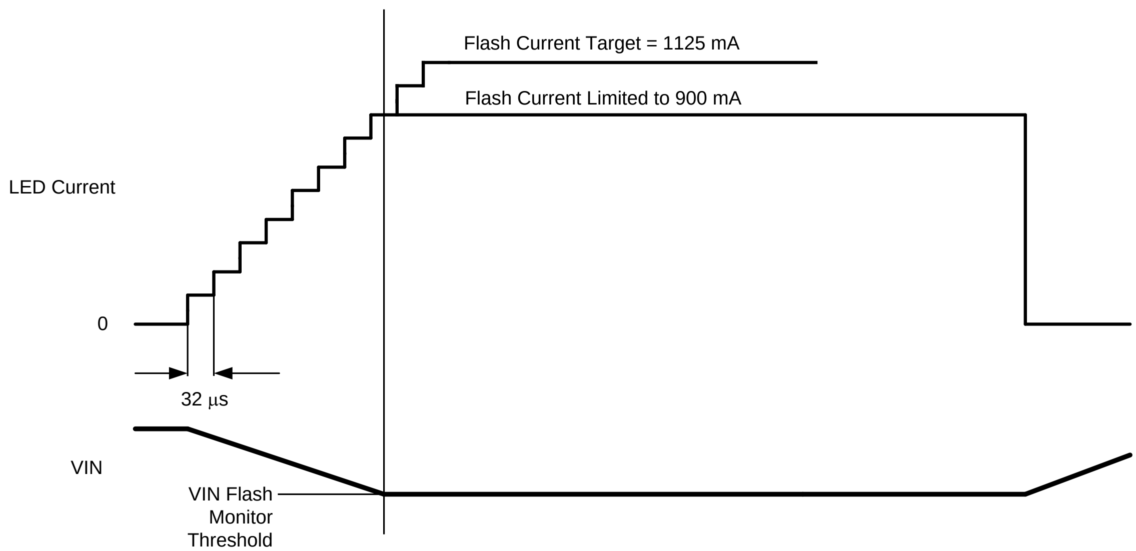


Figure 31. V_{IN} Flash Monitor Example

8.3.9 LED Voltage Monitor

The LM3559 includes a 4-bit ADC which monitors the LED forward voltage (V_{LED}) and stores the digitized value in bits [3:0] of the VLED Monitor Register. The highest voltage of VLED1 or VLED2 is automatically sensed and that becomes the sample point for the ADC. Bit 5, the ADC shutdown bit, enables or disables the ADC with the default state set to enable (bit [5] = 0).

8.3.10 ADC Delay

The ADC Delay Register provides for a programmable delay from 250 µs to 8 ms, in steps of 250 µs. This delay is the delay from when the EOC bit goes low to when the V_{LED} monitor samples the LED voltage. In automatic mode the EOC bit goes low when the Flash LED current hits its target. In manual mode the EOC bit goes low at the end of a readback of the VLED Monitor Register (or when the manual mode bit (bit 4) is re-written with a 1). Figure 32 and Figure 33 detail the timing of the VLED Monitor for both automatic mode and manual mode.

Feature Description (continued)

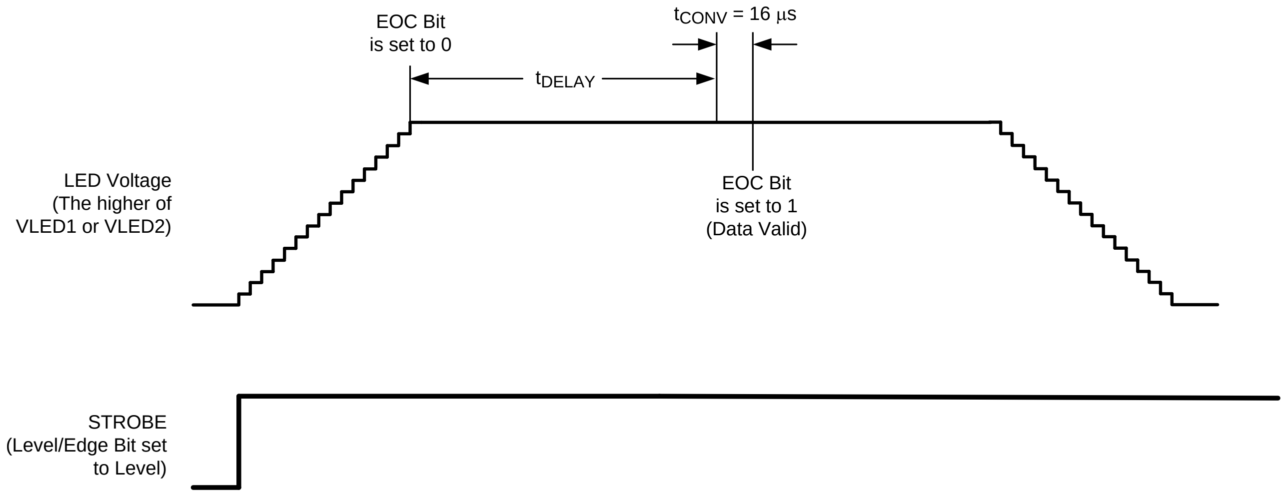


Figure 32. V_{LED} Monitor Automatic Mode

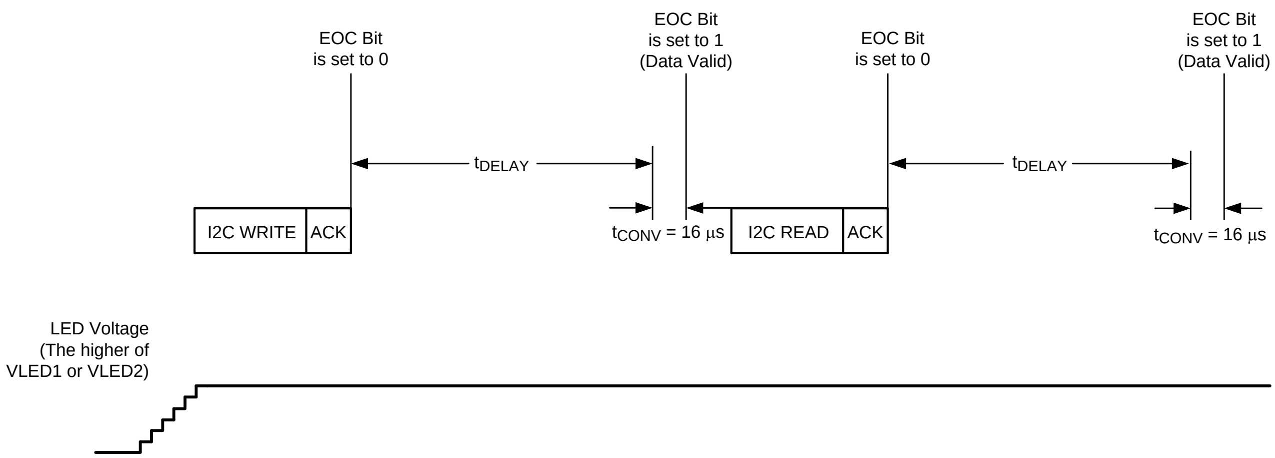


Figure 33. V_{LED} Monitor Manual Mode

8.3.11 Flags Register and Fault Indicators

Eight fault flags are available in the LM3559. These include: a flash timeout, a thermal shutdown, an LED failure flag (LEDF), an LED thermal flag (NTC), a V_{IN} monitor flag, and a V_{IN} flash monitor flag. Additionally, two LED interrupt flag bits (TX1 interrupt and TX2 interrupt) are set when the corresponding interrupt is activated. Reading back a 1 indicates the flagged event has happened. A read of the Flags Register resets these bits.

8.3.11.1 Flash Timeout

The timeout (or TO flag, (bit [0] of the Flags Register), reads back a 1 if the LM3559 is active in flash mode and the timeout period expires before the flash pulse is terminated. The flash pulse can be terminated before the timeout period expires by pulling the STROBE pin low (with Enable Register bit [5] = 0), or by writing a (0,0) to bits [1:0] of the Enable Register. The TO flag is reset to 0 by pulling HWEN low, removing power to the LM3559 device, reading the Flags Register, or when the next flash pulse is triggered.

Feature Description (continued)

8.3.11.2 Thermal Shutdown

When the die temperature of the LM3559 device reaches 150°C, the boost converter shuts down, and the NFET and PFET turn off. Additionally, the active current source (LED1 and/or LED2) turn off. When the thermal shutdown threshold is tripped a 1 is written to bit [1] of the Flags Register (thermal shutdown bit). The device does not start up again until the die temperature falls to below 135°C and the Flags Register is read back, or when the device is shut down and started up again.

8.3.11.3 LED Fault

The LED Fault flag (bit 2 of the Flags Register) reads back a 1 if the part is active in either flash or torch mode and either LED1 or LED2 experience an open or short condition. An LED open condition is signaled if the OVP threshold is crossed at the OUT pin while the device is in either flash or torch mode. An LED short condition is signaled if the voltage at LED1 or LED2 goes below 500 mV while the device is in torch or flash mode. In an LED open condition there is a 2-µs deglitch time from when the output voltage crosses the OVP threshold to when the LED fault flag is triggered. In an LED short condition there is a 250-µs deglitch time before the LED fault flag is set. The LED fault flag can only be reset to 0 by pulling HWEN low, doing a power-on reset of the LM3559, or by removing the fault condition and reading back the Flags Register.

8.3.11.4 TX1 and TX2 Interrupt Flags

The TX1 and TX2 interrupt flags (bits [3] and [4]) indicate an interrupt event has occurred on the respective TX inputs. Bit 3 reads back a 1 if TX1 is in TX mode and there has been a TX1 event since the last read of the Flags Register. Bit 4 read back a 1 if TX2 is in TX mode and there has been a TX2 event since the last read of the Flags Register. A read of the Flags Register automatically resets these bits. A TX event on TX1 or TX2 can be a high-to-low transition or a low-to-high transition depending on the setting of the TX1 and TX2 polarity bits (see Configuration Register 1 Bits [6:5]).

8.3.11.5 LED Thermal Fault (NTC Flag)

The NTC flag (bit [5] of the Flags Register) reads back a 1 if the LM3559 is active in flash or torch mode, the device is in NTC mode, and the voltage at LEDI/NTC has fallen below V_{TRIP} (1 V typical). When this has happened and the LM3559 has been forced into torch mode or LED shutdown (depending on the state of Configuration Register 2 bit [1), the Flags Register must be read, and the voltage at NTC must go above 1 V in order to place the device back in normal operation. (See *NTC Mode* for more details.)

8.3.11.6 Input Voltage Monitor Fault

The V_{IN} monitor flag (bit [7] of the Flags Register) reads back a 1 when the Input Voltage Monitor is enabled and V_{IN} falls below the programmed V_{IN} monitor threshold. This flag must be read back and V_{IN} must go above the V_{IN} monitor threshold in order to resume normal operation.

8.4 Device Functional Modes

8.4.1 Start-Up (Enabling the Device)

Turnon of the LM3559 is done through bits [1:0] of the Enable Register. Bits [1:0] enable the device in torch mode, flash mode, or privacy Indicate mode. Additionally, bit 6 enables the message indicator at the LEDI/NTC pin. On start-up, when V_{OUT} is less than V_{IN}, the internal synchronous PFET turns on as a current source and delivers 350 mA to the output capacitor. During this time both current sources (LED1, and LED2) are off. When the voltage across the output capacitor reaches 2.2 V the active current sources can turn on. At turnon the current sources step through each flash and torch level until their target LED current is reached (32 µs/step). This gives the device a controlled turnon and limits inrush current from the V_{IN} supply.

8.4.2 Pass Mode

At turnon, when the output voltage charges up to (V_{IN} – 150 mV), the device operates in either pass mode or boost mode, depending upon the voltage difference between V_{OUT} and V_{LED}. If the voltage difference between V_{OUT} and V_{LED} is less than 270 mV, the device operates in boost mode. If the difference between V_{OUT} and V_{LED} is greater than 270 mV, the device operates in pass mode. In pass mode the boost converter stops switching, and the synchronous PFET turns fully on, bringing V_{OUT} up to $V_{IN} – I_{IN} \times R_{PMOS}$ (R_{PMOS} = 80 mΩ). In pass mode the inductor current is not limited by the peak current limit. In this situation the output current must be limited to 3 A.

8.4.3 Flash Mode

In flash mode the LED current sources (LED1 and LED2) each provide 16 different current levels from typically 56.25 mA (total) to 1.8 A (total) in steps of 56.25 mA. The flash currents are adjusted via the Flash Brightness Register. Flash mode is activated by writing a 1, 1 to bits [1:0] of the Enable Register or by enabling the hardware flash input (STROBE) via bit [2] of Configuration Register 1 and then pulling the STROBE pin high (high polarity). Once the flash sequence is activated both current sinks (LED1 and LED2) ramp up to their programmed flash current level by stepping through all torch and flash levels (32 µs/step) until the programmed current is reached.

Bit [5] of the Enable Register (STROBE Level/Edge bit) determines how the flash pulse terminates. With the Level/Edge bit = 1 the flash current only terminates when it reaches the end of the flash timeout period. With the level/edge bit = 0, flash mode can be terminated by pulling STROBE low, programming bits [1:0] of the Enable Register with 0,0, or by allowing the flash timeout period to elapse. If the level/edge bit = 0 and STROBE is toggled before the end of the flash timeout period the timeout period resets. Figure 34 and Figure 35 detail the flash pulse termination for the different level/edge bit settings.

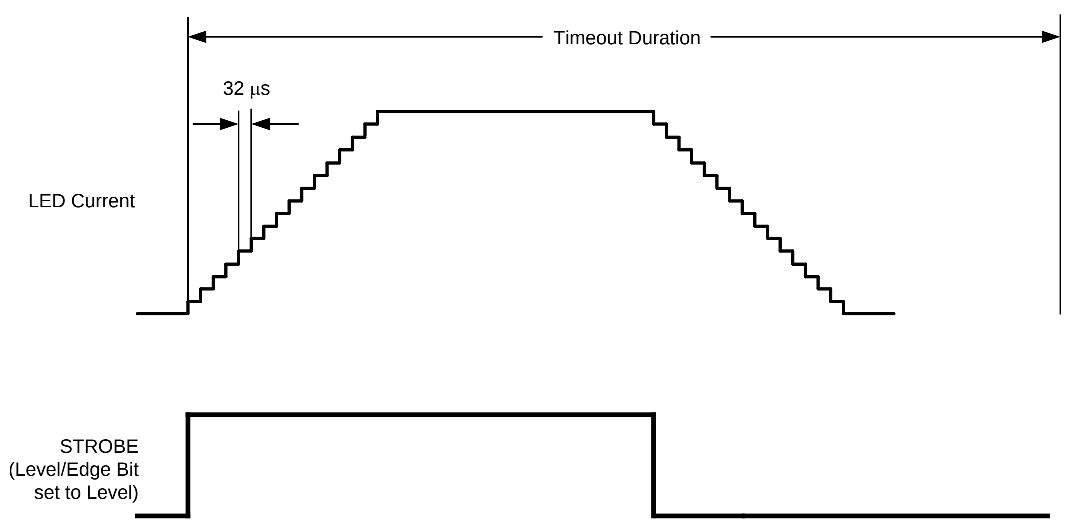


Figure 34. LED Current for Strobe (Level Triggered, Enable Register Bit [5] = 0) Strobe Goes Low Before the End of the Programmed Timeout Duration

Device Functional Modes (continued)

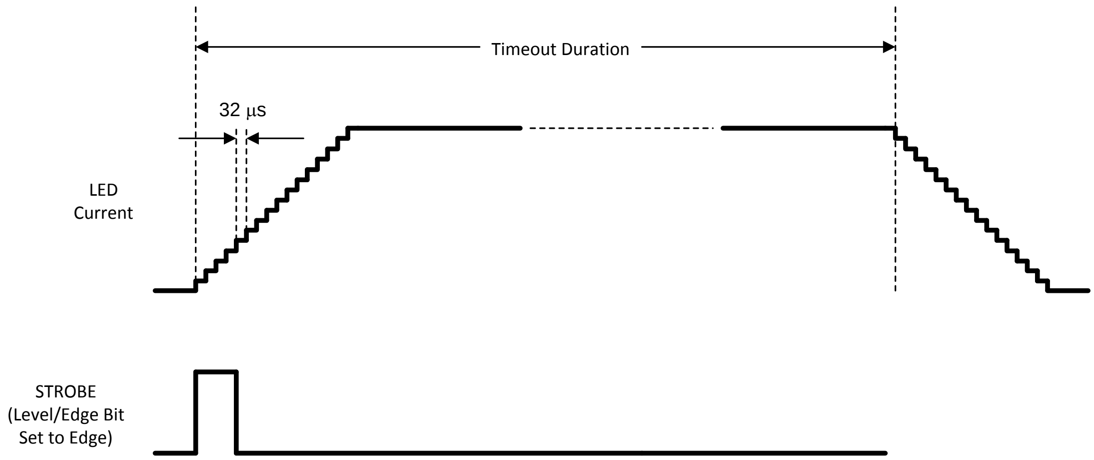


Figure 35. LED Current for Strobe (Edge Triggered, Enable Register Bit [5] = 1)

After the flash pulse terminates; either by a flash timeout, pulling STROBE low or disabling it via the I^2C-compatible interface, LED1 and LED2 turn completely off. This happens even when torch is enabled via the I^2C-compatible interface, and the flash pulse is turned on by toggling STROBE. After a flash event ends, the EN1, EN0 bits (bits [1:0] of the Enable Register) are automatically reset with 0, 0. The exception occurs when the privacy terminate bit is low (bit [3]) in the Privacy Register. In this case, the specific current source that is enabled for privacy mode turns back on after the flash pulse if privacy mode had been enabled before the flash pulse.

8.4.4 Torch Mode

In torch mode the current sources LED1 and LED2 each provide 8 different current levels (Table 3). Torch mode is activated by setting Enable Register bits [1:0] to (1, 0). Once torch mode is enabled, the current sources ramp up to the programmed torch current level by stepping through all of the torch currents at (32 µs/step) until the programmed torch current level is reached.

8.4.5 Privacy-Indicate Mode

The current sources (LED1 and/or LED2) can also be used as a privacy indicator before and after flash mode. Privacy-indicate mode is enabled by setting the Enable Register bit [1:0] to (0,1). Additionally, the Privacy Register contains the bits to select which current source to use as the privacy indicator (either LED1, LED2, or both), whether or not the privacy-indicate mode turns off at the end of the flash pulse, and contains the 8 intensity levels for the privacy indicator.

The intensity of the LEDs in privacy indicate mode is set by PWM'ing the lowest torch current level (28.125 mA). Bits [2:0] of the Privacy Register allow for 8 different duty cycles of 10%, 20%, 30%, 40%, 50%, 60%, 70%, and 80%. See Table 14 for Privacy Register bit settings. Figure 36 details the timing for the privacy-indicate mode on ILED1 or ILED2.

Device Functional Modes (continued)

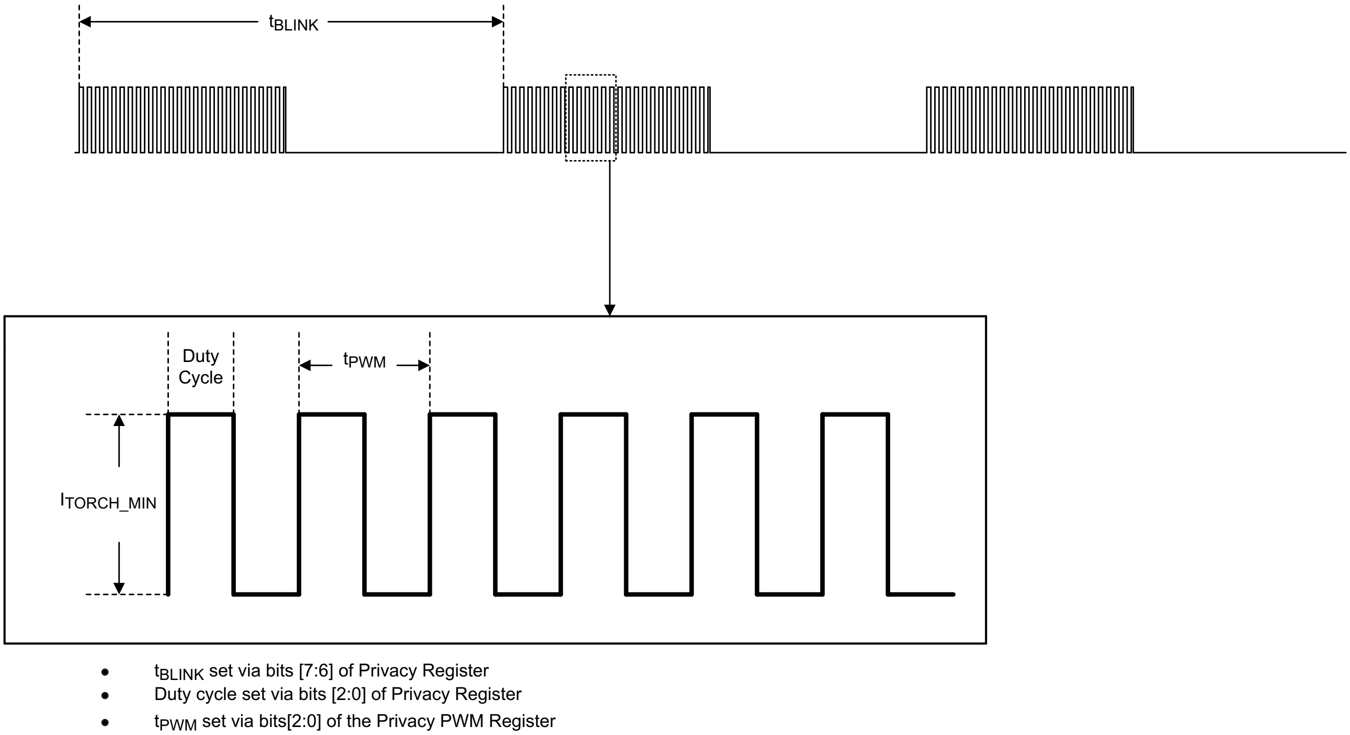


Figure 36. Privacy Indicate Timing

8.4.6 GPIO1 Mode

With bit [0] of the GPIO Register set to 1, the TX1/TORCH/GPIO1 pin is configured as a logic I/O. In this mode the TX1/TORCH/GPIO1 pin is readable and writable as a logic input/output via bits [2:1] of the GPIO Register. See Table 9.

8.4.7 TX2/INT/GPIO2

The TX2/INT/GPIO2 pin has a triple function. In TX2 mode (default) the TX2/INT/GPIO2 pin is an active high flash interrupt. With GPIO Register bit [3] = 1 the TX2/INT/GPIO2 pin is configured as general purpose logic I/O. With GPIO Register bit [6] = 1, and with the TX2/INT/GPIO2 pin configured as a GPIO2 output, the TX2/INT/GPIO2 pin is an interrupt output.

8.4.8 TX2 Mode

In TX2 mode, when Configuration Register 1, bit [6] = 0, the TX2/INT/GPIO2 pin has active low polarity. Under this condition when the LM3559 is engaged in a flash event and TX2 is pulled low, both LED1 and LED2 are forced into torch mode. In TX2 mode with Configuration Register 1, bit [6] = 1 the TX2/INT/GPIO2 input has active high polarity. Under this condition when the LM3559 is engaged in a flash event and the TX2/INT/GPIO2 pin is driven high, both LED1 and LED2 are forced into torch mode. During a flash interrupt event if the TX2/INT/GPIO2 input is disengaged the LED current returns to the previous flash current level. During a flash event, if TX2 is active, the LED current sources still turn off after the flash timeout. Figure 25 details the functionality of the TX2 Interrupt.

Device Functional Modes (continued)

8.4.8.1 TX2 Shutdown

TX2 also has the capability to force shutdown. Bit [0] of Configuration Register 2 set to a 1 changes the TX2 mode from a force torch when active to a force shutdown when active. For example, if TX2/INT/GPIO2 is configured for TX2 mode with active high polarity, and bit [0] of Configuration Register 2 is set to 1 then when TX2 is driven high, the active current sources (LED1 and/or LED2) are forced into shutdown. Once the active current sources are forced into shutdown by activating TX2, the current sources can only be re-enabled if TX2 is deactivated, and the Flags Register is read back.

8.4.9 GPIO2 Mode

With Bit [3] of the GPIO Register set to 1, the TX2/INT/GPIO2 pin is configured as a logic I/O. In this mode the TX2/INT/GPIO2 pin is readable and writeable as a logic input/output via bits [5:4] of the GPIO Register. See Table 9.

8.4.10 Interrupt Output (INT Mode)

The TX2/INT/GPIO2 pin can be reconfigured as an active low interrupt output by setting bit [6] in the GPIO Register to 1 and configuring TX2/INT/GPIO2 as a GPIO2 output. In this mode, TX2/INT/GPIO2 pulls low when any of these conditions exist.

1. The LM3559 is configured for NTC mode (Configuration Register 1 bit [4] = 1) and the voltage at LEDI/NTC has fallen below V_{TRIP} (1 V typical).
2. The LM3559 is configured for V_{IN} monitor mode (VIN Monitor Register bit [0] = 1) and V_{IN} is below the programmed VIN Monitor Threshold.
3. The LM3559 is configured for V_{IN} flash monitor mode (VIN Monitor Register bit [3] = 1) and V_{IN} falls below the programmed V_{IN} flash monitor threshold. Figure 37 shows the functionality of the TX2/INT/GPIO2 input.

Once INT is pulled low due to any of the above conditions having been met, INT only goes back high again if any of the conditions are no longer true and the Flags Register is read.

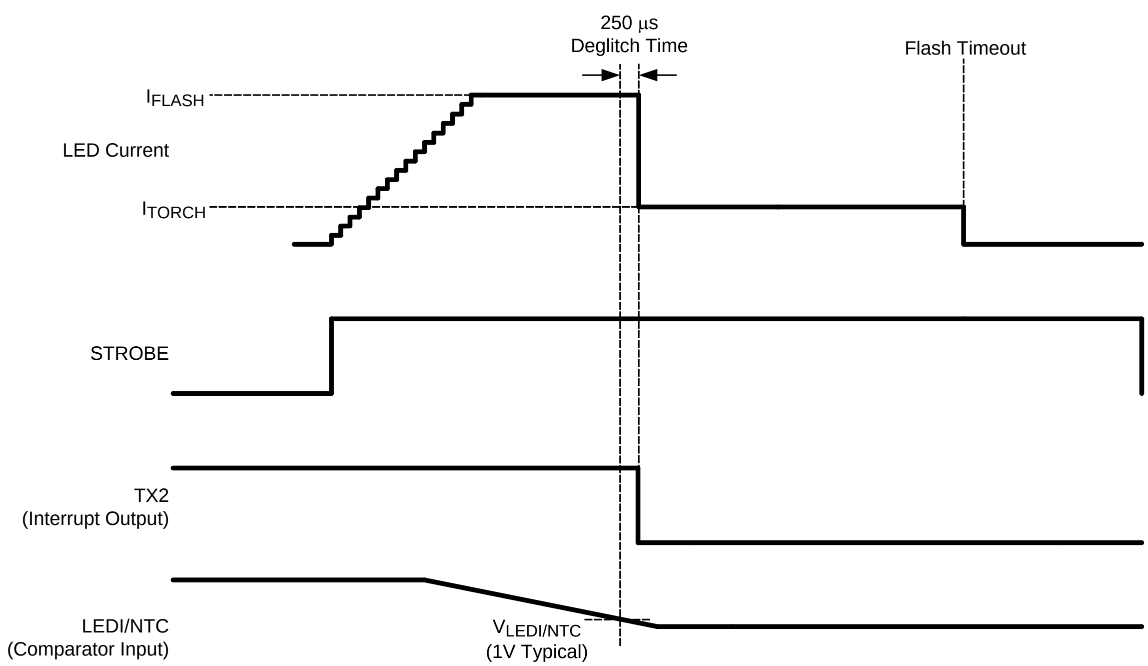


Figure 37. TX2 as an Interrupt Output (During an NTC Event)

Device Functional Modes (continued)

8.4.11 NTC Mode

Writing a 1 to the Configuration Register 1 bit [4] configures the LEDI/NTC pin for NTC mode. In this mode the indicator current source is disabled and LEDI/NTC becomes the positive input to the NTC comparator. NTC mode operates as a LED current interrupt that is triggered when the voltage at LEDI/NTC goes below 1 V.

Two actions can be taken when the NTC comparator is tripped. With Configuration Register 2 bit [1] set to 0 the NTC interrupt forces the LED current from flash mode into torch mode. With Configuration Register 2 bit [1] set to 1 the NTC interrupt forces the LED current into shutdown.

Whether in NTC force torch or NTC shutdown, in order to re-enter flash mode or torch mode after an NTC event, two things must occur. First, the NTC input must be above the 1-V threshold. Secondly, the Flags Register must be read.

To avoid noise from falsely triggering the NTC comparator, this mode incorporates a 250-µs deglitch timer. With NTC mode active, $V_{LEDI/NTC}$ must go below the trip point (V_{TRIP}), and remain below it, for 250 µs before the LEDs are forced into torch mode (or shut down) and the NTC flag is written.

8.4.12 Alternate External Torch (AET Mode)

Configuration Register 2 bit [2] programs the LM3559 for AET mode. With this bit set to 0 (default) TX1/TORCH is a flash current interrupt that forces torch mode only during a flash event. For example, if TX1/TORCH goes high while the LED current is in flash mode, the LEDs are forced into torch mode only for the duration of the timeout counter. At the end of the timeout counter the LEDs turn off.

With the Configuration Register 2 bit [2] set to 1 the LM3559 is configured for AET mode and the operation of TX1/TORCH becomes dependent on its occurrence relative to the STROBE input. In this mode, if TX1/TORCH goes high first, then STROBE goes high next, the LEDs are forced into Torch mode with no timeout. In this mode, if TX1/TORCH goes high after STROBE has gone high, then the TX1/TORCH pin operates as a normal LED current interrupt and the LEDs turn off at the end of the timeout duration (see Figure 38.

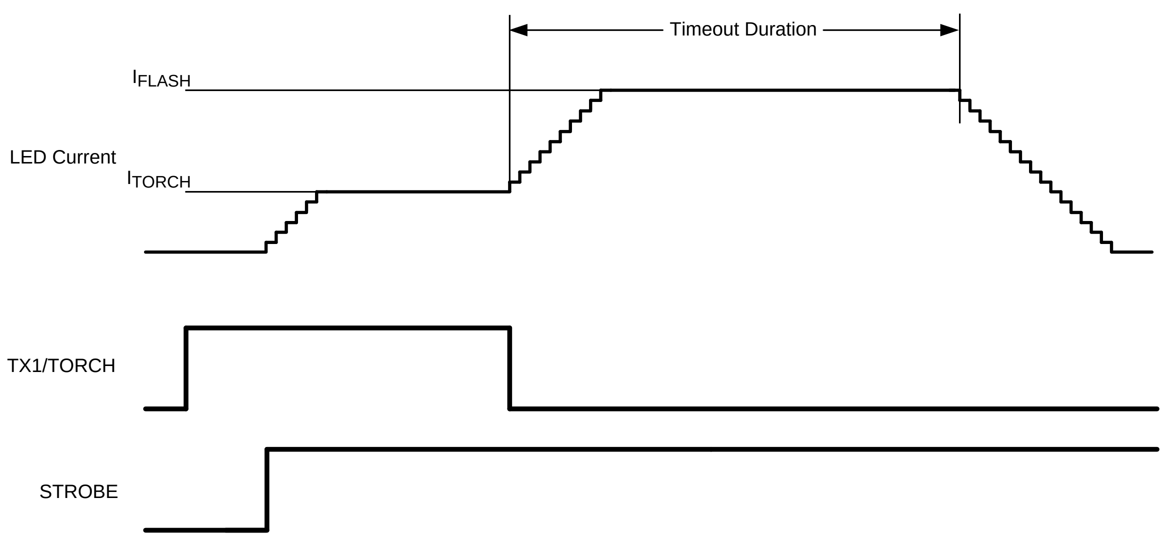


Figure 38. AET Mode Timing

8.4.13 Automatic Conversion Mode

With the ADC enabled, a conversion is performed each time a flash pulse is started. When a flash pulse is started bit [6] of the VLED Monitor Register (end-of-conversion bit) is automatically written with a 0. At the end of the conversion, bit [6] goes high signaling that the V_{LED} data is valid. A read back of the VLED Monitor Register clears the EOC bit. Figure 32 shows the V_{LED} monitor automatic conversion.

Device Functional Modes (continued)

8.4.14 Manual Conversion Mode

The V_{LED} monitor can be set up for manual conversion mode by setting bit [4] of the VLED Monitor Register to 1. When this bit is set high the EOC bit (bit [6]) goes low, and a conversion is performed. When the conversion is complete, the EOC bit goes high again. Subsequent conversions are performed in manual mode by reading back the VLED Monitor Register, which resets the EOC bit and starts another conversion (see Figure 33).

8.5 Programming

8.5.1 I²C-Compatible Interface

8.5.1.1 START and STOP Conditions

The LM3559 is controlled via an I²C-compatible interface. START and STOP conditions classify the beginning and end of the I²C session. A START condition is defined as SDA transitioning from HIGH to LOW while SCL is HIGH. A STOP condition is defined as SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates the START and STOP conditions.

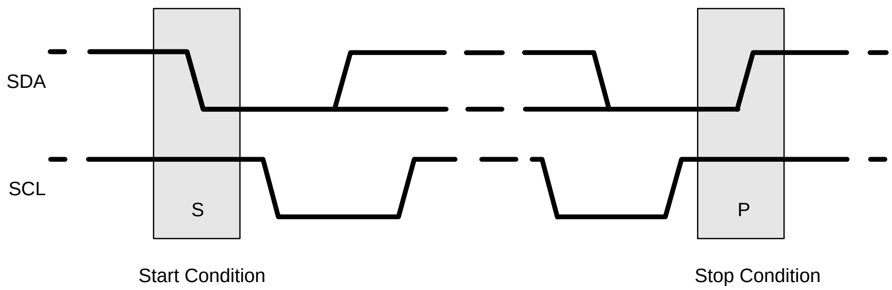


Figure 39. START and STOP Sequences

The I²C bus is considered busy after a START condition and free after a STOP condition. During data transmission the I²C master can generate repeated START conditions. A START and a repeated START condition are equivalent function-wise. The data on SDA must be stable during the HIGH period of the clock signal (SCL). In other words, the state of SDA can only be changed when SCL is LOW. Figure 40 shows the SDA and SCL signal timing for the I²C-Compatible bus. See the *Electrical Characteristics* for timing values.

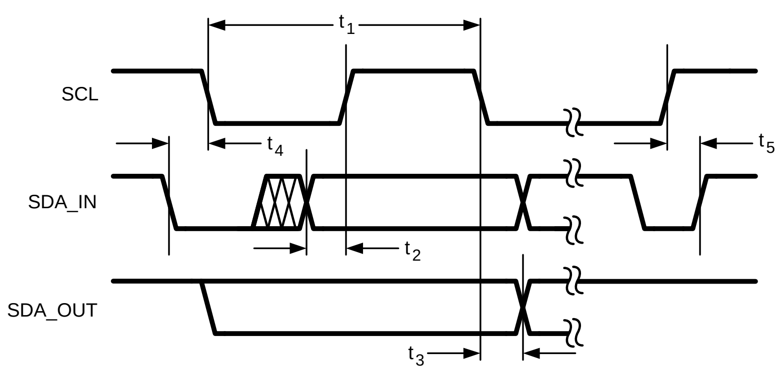


Figure 40. I²C-Compatible Timing

Programming (continued)

8.5.1.2 I²C-Compatible Chip Address

The device address for the LM3559 is 1010011 (0xA7 for read and 0xA6 for write). After the START condition, the I²C master sends the 7-bit address followed by an eighth read or write bit (R/W). R/W = 0 indicates a WRITE and R/W = 1 indicates a READ. The second byte following the device address selects the register address to which the data will be written. The third byte contains the data for the selected register.

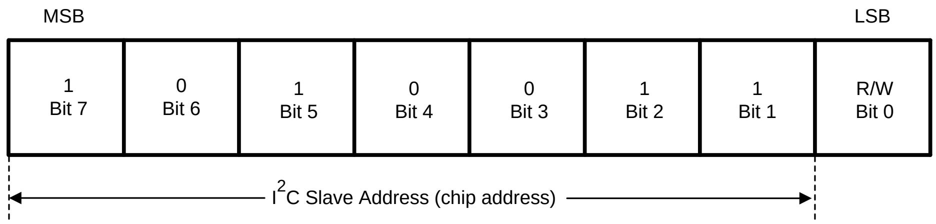


Figure 41. Device Address

8.5.1.3 Transferring Data

Every byte on the SDA line must be eight bits long, with the most significant bit (MSB) transferred first. Each byte of data must be followed by an acknowledge bit (ACK). The acknowledge related clock pulse (9th clock pulse) is generated by the master. The master releases SDA (HIGH) during the 9th clock pulse (write mode). The LM3559 pulls down SDA during the 9th clock pulse, signifying an acknowledge. An acknowledge is generated after each byte has been received.

8.6 Register Maps

Table 1. LM3559 Internal Registers

REGISTER NAME	INTERNAL HEX ADDRESS	POWER-ON/RESET VALUE
Enable	0x10	0x18
Privacy	0x11	0x58
Indicator	0x12	0x00
Indicator Blinking	0x13	0x00
Privacy PWM	0x14	0xF0
GPIO	0x20	0x80
VLED Monitor (ADC)	0x30	0x80
ADC Delay	0x31	0xC0
VIN Monitor	0x80	0xC0
Last Flash	0x81	0x00
Torch Brightness	0xA0	0x52
Flash Brightness	0xB0	0xDD
Flash Duration	0xC0	0x6F
Flags	0xD0	0x00
Configuration 1	0xE0	0x68
Configuration 2	0xF0	0xF0

8.6.1 Enable Register

Bits [1:0] of the Enable Register controls the ON/OFF state of torch mode, flash mode, and privacy-indicate mode. Bits [4:3] turn on/off the main current sources (LED1 and LED2). Bit [5] sets the level or edge control for the STROBE input. Bits 7 and 6 control the indicator current source (see Table 2).

Table 2. Enable Register Descriptions

Bit 7 (EN Blink)	Bit 6 (EN Message Indicator)	Bit 5 (STROBE Level/Edge)	Bit 4 (LED2 Enable)	Bit 3 (LED1 Enable)	Bit 2 (Not Used)	Bit 1 (EN1)	Bit 0 (EN0)
0 = Message indicator blinking function is disabled(1) **(default)** 1 = message indicator blinking function is enabled. The message indicator blinks the pattern programmed in the Indicator Register and Indicator Blinking Register	0 = Message Indicator is disabled **(default)** 1= Message Indicator is enabled.	0 = (Level Sensitive) When STROBE goes high, the flash current will turn on and remain on for the duration the STROBE pin is held high or until the flash timeout occurs, whichever comes first. **(default)** 1 = (Edge Triggered) When STROBE goes high , the flash current will turn on and remain on for the duration of the Flash timeout.	0 = LED2 off 1 = LED2 on **(default)**	0 = LED1 off 1 = LED1 on **(default)**	N/A	**Enable Bits** 00 = Current sources are shut down **(default)** 01 = Privacy-indicate mode 10 = Torch mode 11 = Flash mode (bits reset at timeout)	

(1) Bit 7 enables or disables the message indicator blinking function. With this bit set to 0 and Bit 6 set to 1, the message indicator turns on constantly at the programmed current as set in the Indicator Register, bits [2:0].

8.6.2 Torch Brightness Register

Bits [2:0] of the Torch Brightness Register set the Torch current for LED1. Bits [5:3] set the torch current for LED2. (see Table 3).

Table 3. Torch Brightness Register Descriptions

Bit 7 (N/A)	Bit 6 (N/A)	Bit 5 (TC2A)	Bit 4 (TC2B)	Bit 3 (TC2C)	Bit 2 (TC1A)	Bit 1 (TC1B)	Bit 0 (TC1C)
(Not Used)		**LED2 Torch Current Select Bits** 000 = 28.125 mA (56.25 mA total) 001 = 56.25 mA (112.5 mA total) **010 = 84.375 mA (168.75 mA total) default** 011 = 112.5 mA (225 mA total) 100 = 140.625 mA (281.25 mA total) 101 = 168.75 mA (337.5 mA total) 110 = 196.875 mA (393.75 mA total) 111 = 225 mA (450 mA total)			**LED1 Torch Current Select Bits** 000 = 28.125 mA (56.25 mA total) 001 = 56.25 mA (112.5 mA total) **010 = 84.375 mA (168.75 mA total) default** 011 = 112.5 mA (225 mA total) 100 = 140.625 mA (281.25 mA total) 101 = 168.75 mA (337.5 mA total) 110 = 196.875 mA (393.75 mA total) 111 = 225 mA (450 mA total)		

8.6.3 Flash Brightness Register

Bits [3:0] of the Flash Brightness Register set the Flash current for LED1. Bits [7:4] set the Flash current for LED2. (see Table 4).

Table 4. Flash Brightness Register Descriptions

Bit 7 (FC2A)	Bit 6 (FC2B)	Bit 5 (FC2C)	Bit 4 (FC2D)	Bit 3 (FC1A)	Bit 2 (FC1B)	Bit 1 (FC1C)	Bit 0 (FC1D)
LED2 Flash Current Select Bits 0000 = 56.25 mA (112.5 mA total) 0001 = 112.5 mA (225 mA total) 0010 = 168.75 mA (337.5 mA total) 0011 = 225 mA (450 mA total) 0100 = 281.25 mA (562.5 mA total) 0101 = 337.5 mA (675 mA total) 0110 = 393.75 mA (787.5 mA total) 0111 = 450 mA (900 mA total) 1000 = 506.25 mA (1012.5 mA total) 1001 = 562.5 mA (1125 mA total) 1010 = 618.75 mA (1237.5 mA total) 1011 = 675 mA (1350 mA total) 1100 = 731.25 mA (1562.5 mA total) **1101 = 787.5 mA (1575 mA total) Default** 1110 = 843.75 mA (1687.5 mA total) 1111 = 900 mA (1800 mA total)				**LED1 Flash Current Select Bits** 0000 = 56.25 mA (112.5 mA total) 0001 = 112.5 mA (225 mA total) 0010 = 168.75 mA (337.5 mA total) 0011 = 225 mA (450 mA total) 0100 = 281.25 mA (562.5 mA total) 0101 = 337.5 mA (675 mA total) 0110 = 393.75 mA (787.5 mA total) 0111 = 450 mA (900 mA total) 1000 = 506.25 mA (1012.5 mA total) 1001 = 562.5 mA (1125 mA total) 1010 = 618.75 mA (1237.5 mA total) 1011 = 675 mA (1350 mA total) 1100 = 731.25 mA (1562.5 mA total) **1101 = 787.5 mA (1575 mA total) Default** 1110 = 843.75 mA (1687.5 mA total) 1111 = 900 mA (1800 mA total)			

8.6.4 Flash Duration Register

Bits [4:0] of the Flash Duration Register set the flash timeout duration. Bits [6:5] set the switch current limit (see Table 5).

Table 5. Flash Duration Register Descriptions

Bit 7 (Not used)	Bit 6 (CL1)	Bit 5 (CL0)	Bit 4 (T4)	Bit 3 (T3)	Bit 2 (T2)	Bit 1 (T1)	Bit 0 (T0)
N/A	**Current Limit Select Bits** 00 = 1.4 A peak current limit 01 = 2.1 A peak current limit 10 = 2.7 A peak current limit **11 = 3.2 A peak current limit (default)**		**Flash timeout Select Bits** 00000 = 32 ms timeout 00001 = 64 ms timeout 00010 = 96 ms timeout 00011 = 128 ms timeout 00100 = 160 ms timeout 00101 = 192 ms timeout 00110 = 224 ms timeout 00111 = 256 ms timeout 01000 = 288 ms timeout 01001 = 320 ms timeout 01010 = 352 ms timeout 01011 = 384 ms timeout 01100 = 416 ms timeout 01101 = 448 ms timeout 01110 = 480 ms timeout **01111 = 512 ms timeout (default)** 10000 = 544 ms timeout 10001 = 576 ms timeout 10010 = 608 ms timeout 10011 = 640 ms timeout 10100 = 672 ms timeout 10101 = 704 ms timeout 10110 = 736 ms timeout 10111 = 768 ms timeout 11000 = 800 ms timeout 11001 = 832 ms timeout 11010 = 864 ms timeout 11011 = 896 ms timeout 11100 = 928 ms timeout 11101 = 960 ms timeout 11110 = 992 ms timeout 11111 = 1024 ms timeout				

8.6.5 Flags Register

The Flags Register holds the flag bits indicating flash timeout, thermal shutdown, LED fault (open or short), TX interrupts (TX1 and TX2), LED thermal fault (NTC), V_{IN} monitor trip, and V_{IN} flash monitor trip. All flags are cleared on read back of the Flags Register (see Table 6).

Table 6. Flags Register Descriptions

Bit 7 (V_{IN} Monitor)	Bit 6 (VIN Flash Monitor)	Bit 5 (NTC Fault)	Bit 4 (TX2 Interrupt)	Bit 3 (TX1 Interrupt)	Bit 2 (LED Fault)	Bit 1 (Thermal Shutdown)	Bit 0 (Flash timeout)
0 = V_{IN} is above the VIN Monitor Threshold or V_{IN} monitor threshold is disabled **(default)**	VIN did not fall below the VIN Flash Monitor threshold during the flash pulse turnon or VIN flash monitor is disabled **(default)**	0 = LEDI/NTC pin is above 1V(**default**)	0 = TX2 has not changed state (**default**)	0 = TX1 has not changed state (**default**)	0 = Proper LED Operation (**default**)	0 = Die Temperature below Thermal Shutdown Limit (**default**)	0 = Flash timeout did not expire (**default**)
1 = VI_N monitor is enabled and V_{IN} has fallen below the programmed threshold	1 = V_{IN} flash monitor is enabled and V_{IN} fell below the programmed VIN Flash Monitor threshold during the flash pulse turn-on	1 = NTC mode is enabled and LEDI/NTC has fallen below 1V	1 = TX2 has changed state (TX2 mode only)	1 = TX1 has changed state (TX1 mode only)	1 = LED failed (open or short)	1 = Die temperature has crossed the thermal shutdown threshold	1 = Flash timeout expired

8.6.6 Configuration Register 1

Configuration Register 1 holds the STROBE input enable bit, the STROBE polarity bit, the NTC enable bit, the polarity selection bits for TX1 and TX2, and the hardware-torch enable bit (see Table 7).

Table 7. Configuration Register 1 Descriptions

Bit 7 (Hardware Torch Mode Enable)	Bit 6 (TX2 Polarity)	Bit 5 (TX1 Polarity)	Bit 4 (NTC Mode Enable)	Bit 3 (STROBE Polarity)	Bit 2 (STROBE Input Enable)	Bit 1 (Not Used)	Bit 0 (Not Used)
0 = TX1/TORCH is a TX input **(default)**	0 = TX2 is configured for active low polarity	0 = TX1 is configured for active low polarity	0 = LEDI/NTC pin is configured as an indicator output **(default)**	0 = STROBE input enable is active low. Pulling STROBE low turns on Flash current	0 = STROBE pin disabled **(default)**	N/A	N/A
1 = TX1/TORCH pin is a hardware TORCH enable. This bit is reset to 0 after a flash event.	1 =TX2 pin is configured for active high polarity **(default)**	1 = TX1 is configured for active high polarity **(default)**	1 = LEDI/NTC is configured as a comparator input for an NTC thermistor	1 = STROBE Input is active high. Pulling STROBE high turns on Flash current **(default)**	1 = STROBE Input enabled		

8.6.7 Configuration Register 2

Configuration Register 2 holds the TX2 shutdown select bit, the NTC shutdown select bit, the AET-mode enable bit, and the V_{IN} monitor shutdown bit (see Table 8).

Table 8. Configuration Register 2 Bit Descriptions

Bit 7 (Not used)	Bit 6 (Not used)	Bit 5 (Not used)	Bit 4 (Not used)	Bit 3 (V_{IN} Monitor Shutdown)	Bit 2 (AET mode)	Bit 1 (NTC Shutdown)	Bit 0 (TX2 Shutdown)
N/A	N/A	N/A	N/A	0 = V_{IN} falling below the programmed V_{IN} monitor threshold forces the LED current into the programmed torch current **(default)**	0 = AET Mode Disabled **(default)**	0 = Voltage at LEDI/NTC falling below V_{TRIP} forces the active current source (LED1 and/or LED2) to the programmed torch current **(default)**	0 = TX2 event forces the LED current to the programmed torch current **(default)**
				1 = V_{IN} falling below the programmed V_{IN} monitor threshold forces the LED current into shutdown.	1 = AET Mode Enabled	1 = Voltage at LEDI/NTC falling below V_{TRIP} forces the active current source (either LED1 and/or LED2) into shutdown.	1 = TX2 event forces the LED current into shutdown.

8.6.8 GPIO Register

The GPIO Register contains the control bits which change the state of the TX1/TORCH/GPIO1 pin and the TX2/INT/GPIO2 pins to general purpose I/Os (GPIOs). Additionally, bit 6 of the GPIO Register contains the interrupt configuration bit. Table 9 describes the bit description and functionality of the GPIO register. To configure the TX1 or TX2 pins as GPIO outputs an initial double write is required to register 0x20. For example, to configure TX2 to output a logic high, an initial write of 0xB8 would need to occur twice to force GPIO2 low. Subsequent writes to GPIO2 after the initial setup only requires a single write. To read back the GPIO inputs, a write, then a read, of register 0x20 must occur each time the data is read. For example, if GPIO2 is set up as a GPIO input and the GPIO2 input has then changed state, first a write to 0x20 must occur, then the readback of register 0x20 that follows shows the updated data. When configuring TX2 as an interrupt output, the TX2/GPIO2/INT pin must first be configured as a GPIO output (double write). For example, to configure TX2/GPIO2/INT for INT mode, a write of 0xF8 to register 0x20 must be done twice.

Table 9. GPIO Register

Bit 7 (Not Used)	Bit 6 (TX2/INT/GPIO2 Interrupt Enable)	Bit 5 (TX2/INT/GPIO2 data)	Bit 4 (TX2/INT/GPIO2 data direction)	Bit 3 (TX2/INT/GPIO2 Control)	Bit 2 (TX1/TORCH/GPIO1 data)	Bit 1 (TX1/TORCH/GPIO1 data direction)	Bit 0 (TX1/TORCH/GPIO1 Control)
N/A	0 = TX2/INT/GPIO2 is configured according to bit 3 of this register **(default)**	This bit is the read or write data for the GPIO2 pin in GPIO mode	0 = TX2/INT/GPIO2 is a GPIO Input **(default)**	0 = TX2/INT/GPIO is a TX2 interrupt **(default)**	This bit is the read or write data for the GPIO1 pin in GPIO mode	0 = TX1/TORCH/GPIO1 is a GPIO input **(default)**	0 = TX1/TORCH/GPIO1 pin is configured according to Configuration Register 1 bit[7] **(default)**
	1 = with bits [4:3] = 11, TX2/INT/GPIO2 is an interrupt output. See Interrupt section.		1 = TX2/INT/GPIO2 is a GPIO Output	1 = TX2/INT/GPIO2 is configured as a GPIO		1 TX1/TORCHGPIO1 is an output	1 = TX1/TORCH/GPIO1 pin is configured as a GPIO

8.6.9 Last Flash Register

The Last Flash Register is a read-only register loaded with the flash code corresponding to the flash level that the device was at if any of the following events happens:

1. Voltage at LEDI/NTC falling below V_{TRIP} with the device in NTC mode (Configuration Register 1 bit [4] = 1)
2. Input voltage falling below the programmed V_{IN} monitor threshold with device in V_{IN} monitor mode (VIN Monitor Register bit [0] = 1)
3. Input voltage falling below the programmed V_{IN} flash monitor threshold with the device in V_{IN} flash monitor mode (VIN Monitor Register bit [3] = 1).

The Last Flash Register is updated at the same time that the corresponding flag bit is written to the Flags Register. This results in a delay of 250 µs from when $V_{LEDI/NTC}$ (NTC mode) crosses V_{TRIP}, or V_{IN} (V_{IN} monitor enabled) crosses the V_{IN_TH}. During V_{IN} flash monitor there is a 8-µs deglitch time so the V_{IN} flash monitor flag is written (and the Last Flash Register is updated) 8 µs after V_{IN} falls below V_{IN_FLASH}.

Table 10. Last Flash Register Descriptions

Bit 7 (LF2A)	Bit 6 (LF2B)	Bit 5 (LF2C)	Bit 4 (LF2D)	Bit 3 (LF1A)	Bit 2 (LF1B)	Bit 1 (LF1C)	Bit 0 (LF1D)
These bits are read only and represent the flash current code for LED2 that the LM3559 was at during the interrupt. 0000 = 56.25 mA (112.5 mA total) 0001 = 112.5 mA (225 mA total) 0010 = 168.75 mA (337.5 mA total) 0011 = 225 mA (450 mA total) 0100 = 281.25mA (562.5 mA total) 0101 = 337.5 mA (675 mA total) 0110 = 393.75 mA (787.5 mA total) 0111 = 450 mA (900 mA total) 1000 = 506.25 mA (1012.5 mA total) 1001 = 562.5 mA (1125 mA total) 1010 = 618.75 mA (1237.5 mA total) 1011 = 675 mA (1350 mA total) 1100 = 731.25 mA (1562.5 mA total) 1101 = 787. 5mA (1575 mA total) 1110 = 843.75 mA (1687.5 mA total) 1111 = 900 mA (1800 mA total)				These bits are read only and represent the flash current code for LED1 that the LM3559 was at during the interrupt. 0000 = 56.25 mA (112.5 mA total) 0001 = 112.5 mA (225 mA total) 0010 = 168.75 mA (337.5 mA total) 0011 = 225 mA (450 mA total) 0100 = 281.25mA (562.5 mA total) 0101 = 337.5 mA (675 mA total) 0110 = 393.75 mA (787.5 mA total) 0111 = 450 mA (900 mA total) 1000 = 506.25 mA (1012.5 mA total) 1001 = 562.5 mA (1125 mA total) 1010 = 618.75 mA (1237.5 mA total) 1011 = 675 mA (1350 mA total) 1100 = 731.25 mA (1562.5 mA total) 1101 = 787. 5 mA (1575 mA total) 1110 = 843.75 mA (1687.5 mA total) 1111 = 900 mA (1800 mA total)			

8.6.10 VLED Monitor Register

The VLED Monitor Register controls the internal 4-bit analog to digital converter. Bits [3:0] of this register contain the 4-bit data of the LED voltage. This data is the digitized voltage of the highest of either VLED1 to GND or VLED2 to GND. Bit [4] is the manual mode enable which provides for a manual conversion of the ADC. In manual mode the automatic conversion is still performed. In automatic conversion mode a conversion is performed each time a flash pulse is initiated. Bit [5] is the ADC shutdown bit. Bit [6] signals the end of conversion. This is a read-only bit that goes high when a conversion is complete and data is ready. A read of the VLED Monitor Register clears the EOC bit (see Table 11).

Table 11. VLED Monitor Register Descriptions

<table>
<tr><th>Bit 7
(Not Used)</th><th>Bit 6
(End of Conversion)</th><th>Bit 5
(Shutdown)</th><th>Bit 4
(Manual Mode Enable)</th><th>Bit 3
(ADC3)</th><th>Bit 2
(ADC2)</th><th>Bit 1
(ADC1)</th><th>Bit 0
(ADC0)</th></tr>
<tr><td rowspan="2">N/A</td><td>0 = Conversion in progress (default)</td><td>0 = ADC is enabled (default)</td><td>0 = Manual mode disabled (default)</td><td colspan="4" rowspan="2">0000 = (V_{LED} < 3.2 V) (default)
0001 = (3.2 V ≤ V_{LED} < 3.3 V)
0010 = (3.3 V ≤ V_{LED} < 3.4 V)
0011 = (3.4 V ≤ V_{LED}D < 3.5 V)
0100 = (3.5 V ≤ V_{LED} < 3.6 V)
0101 = (3.6 V ≤ V_{LED} < 3.7 V)
0110 = (3.7 V ≤ V_{LED} < 3.8 V)
0111 = (3.8 V ≤ V_{LED} < 3.9 V)
1000 = (3.9 V ≤ V_{LED} < 4 V)
1001 = (4 V ≤ V_{LED} < 4.1 V)
1010 = (4.1 V ≤ V_{LED} < 4.2 V)
1011 = (4.2 V ≤ V_{LED} < 4.3 V)
1100 = (4.3 V ≤ V_{LED} < 4.4 V)
1101 = (4.4 V ≤ V_{LED} < 4.5 V)
1110 = (4.5 V ≤ V_{LED} < 4.6 V)
1111 = (4.6 V ≤ V_{LED})</td></tr>
<tr><td>1 = Conversion done</td><td>1 = ADC is shutdown, no conversion is performed</td><td>1 = Manual mode is enabled</td></tr>
</table>

8.6.11 ADC Delay Register

The ADC Delay Register programs the delay from when the EOC bit goes low to when a conversion is initiated. This delay applies to both manual mode and automatic mode. Bit 5 is the no-delay bit and can set the delay to effectively 0 (see Table 12, Figure 32, and Figure 33).

Table 12. ADC Delay Register

<table>
<tr><th>Bit 7
(Not Used)</th><th>Bit 6
(Not used)</th><th>Bit 5 (No Delay)</th><th>Bit 4 (D1)</th><th>Bit 3 (D2)</th><th>Bit 2 (D3)</th><th>Bit 1 (D4)</th><th>Bit 0 (D5)</th></tr>
<tr><td colspan="2" rowspan="2">N/A</td><td>0 = Delay is set by bits [4:0] (default)</td><td colspan="5" rowspan="2">Bits [4:0] programs the delay from when the EOC bit goes low to when a conversion is started (250 µs/step).
00000 = 250 µs (default)
:
:
:
:
11111 = 8ms</td></tr>
<tr><td>1 = no delay from when the EOC goes low to when the conversion is started.</td></tr>
</table>

8.6.12 Input Voltage Monitor Register

The VIN Monitor Register contains the enable bit for the V_{IN} monitor, the threshold select for the V_{IN} monitor, the enable bit for the V_{IN} flash monitor, and the threshold select for the V_{IN} flash monitor (see Table 13).

Table 13. VIN Monitor Register

<table>
<tr><th>Bit 7
(Not used)</th><th>Bit 6
(Not used)</th><th>Bit 5
(VIN Flash Monitor Threhold 1)</th><th>Bit 4
(VIN Flash Monitor Threhold 0)</th><th>Bit 3
(VIN Flash Monitor Enable)</th><th>Bit 2
(VIN Monitor Threshold 1)</th><th>Bit 1
(VIN Monitor Threshold 0)</th><th>Bit 0
(VIN Monitor Enable)</th></tr>
<tr><td colspan="2" rowspan="2">N/A</td><td colspan="2" rowspan="2">00= 2.9 V (default)
01 = 3 V
10 = 3.1 V
11 = 3.2 V</td><td>0 = V_{IN} monitor is disabled (default)</td><td colspan="2" rowspan="2">00 = 2.9 V (default)
01= 3 V
10 = 3.1 V
11 = 3.2 V</td><td>0 = V_{IN} monitor disabled (default)</td></tr>
<tr><td>1 = V_{IN} monitor is enabled</td><td>1 = V_{IN} monitorenabled</td></tr>
</table>

8.6.13 Privacy Register

The Privacy Register contains the bits to control which current source is used for the privacy indicator (LED1 or LED2 or both), whether the privacy indicator turns off or remains on after the flash pulse terminates, and the duty cycle settings (between 10% and 80%) for setting the privacy LED current (see Table 14).

Table 14. Privacy Register

Bit 7 (Blink 2)	Bit 6 (Blink 1)	Bit 5 (LED2 Privacy)	Bit 4 (LED1 Privacy)	Bit 3 (Privacy Terminate)	Bit 2 (PD2)	Bit 1 (PD1)	Bit 0 (PD0)
00 = No blinking **01 = 128 ms blink period (default)** 10 = 256 ms blink period 11 = 512 ms blink period		0 = LED2 is off for privacy mode **(default)** 1 = LED2 is on for privacy mode	0 = LED1 is off for privacy mode 1 = LED1 is on for privacy mode **(default)**	0 = Privacy mode turns back on at the end of the flash pulse 1 = Privacy mode turns off at the end of the flash pulse **(default)**	Privacy mode current levels (% of minimum torch current) **000 = 10% (default)** 001 = 20% 010 = 30% 011 = 40% 100 = 50% 101 = 60% 110 = 70% 111 = 80%		

8.6.14 Privacy PWM Period Register

The Privacy PWM Register contains the bits to control the PWM period for the privacy indicate mode (see Table 15).

Table 15. Privacy PWM Period Register

Bits 7-3 (Not Used)	Bit 2 (P3)	Bit 1 (P2)	Bit 0 (P1)
	000 = 5.12 ms 001 = 2.56 ms 010 = 1.28 ms 011 = 640 µs 1XX = 320 µs		

8.6.15 Indicator Register

The Message Indicator Register contain the bits which control the following:

1. Indicator current level
2. Pulse width
3. Ramp times for turnon and turnoff of the indicator current source (see Figure 42 for the message indicator timing diagram).

Table 16. Indicator Register

Bit 7 (R2)	Bit 6 (R1)	Bit 5 (P3)	Bit 4 (P2)	Bit 3 (P1)	Bit 2 (I3)	Bit 1 (I2)	Bit 0 (I1)
(t_{RAMP}) **00 = 78 ms (default)** 01 = 156 ms 10 = 312 ms 11 = 624 ms		(PERIOD#) **000 = 0 (default)** 001 = 1 010 = 2 011 = 3 100 = 4 101 = 5 110 = 6 111 = 7			(I_{IND}) **000 = 2.25 mA (default)** 001 = 4.5 mA 010 = 6.75 mA 011 = 9 mA 100 = 11.25 mA 101 = 13.5 mA 110 = 15.75 mA 111 = 18 mA		

8.6.16 Indicator Blinking Register

The Indicator Blinking Register contain the bits which control the following:

1. Number of periods ($t_{PERIOD} = t_{RAMP} \times 2 + t_{PULSE} \times 2$)
2. Active Time ($t_{ACTIVE} = t_{PERIOD} \times$ PERIOD#)
3. Blank Time ($t_{BLANK} = t_{ACTIVE} \times$ BLANK#)
   – (see Figure 42)

Table 17. Indicator Blinking Register

Bit 7 (M4)	Bit 6 (M3)	Bit 5 (M2)	Bit 4 (M1)	Bit 3 (PW4)	Bit 2 (PW3)	Bit 1 (PW2)	Bit 0 (PW1)
BLANK# **0000 = 0 (default)** 0001 = 1 0010 = 2 0011 = 3 0100 = 4 0101 = 5 0110 = 6 0111 = 7 1000 = 8 1001 = 9 1010 = 10 1011 = 11 1100 = 12 1101 = 13 1110 = 14 1111 = 15				Pulse time (t_{PULSE}) **0000 = 0 (default)** 0001 = 32 ms 0010 = 64 ms 0011 = 92 ms 0100 = 128 ms 0101 = 160 ms 0110 = 196 ms 0111 = 224 ms 1000 = 256 ms 1001 = 288 ms 1010 = 320 ms 1011 = 352 ms 1100 = 384 ms 1101 = 416 ms 1110 = 448 ms 1111 = 480 ms			

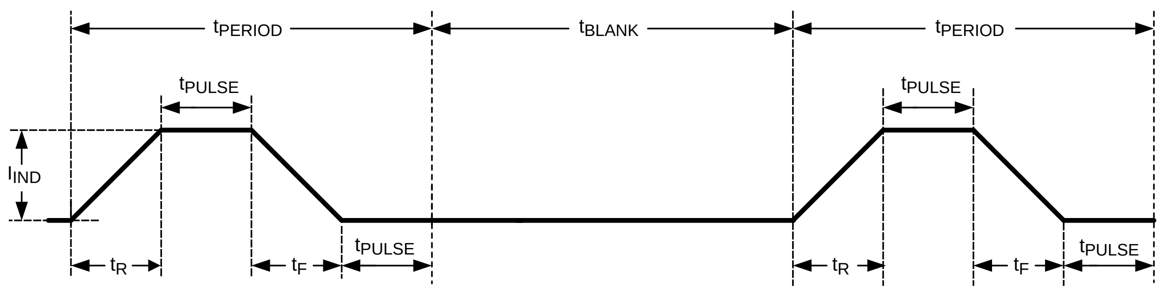


Figure 42. Message Indicator Timing Diagram

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LM3559 is a synchronous boost flash driver with dual 900-mA high-side current sources. The 2-MHz DC-DC boost regulator allows for the use of small external components. The device operates from a typical input voltage from 2.5 V to 5.5 V and an ambient temperature range of –40°C to +85°C.

Table 18. Application Circuit Component List

COMPONENT	MANUFACTURER	VALUE	PART NUMBER	SIZE	RATING
L	Toko	1 µH	FDSD0312-1R0	3 mm × 3 mm × 1.2 mm	3.3 A
C_{IN}/C_{OUT}	Murata	10 µF	GRM188R60J106M	1.6 mm × 0.8 mm × 0.8 mm (0603)	6.3 V
LEDs	Lumiled		PWF-4		V_F = 3.6 V at 1 A

9.2 Typical Applications

9.2.1 LM3559 Typical Application

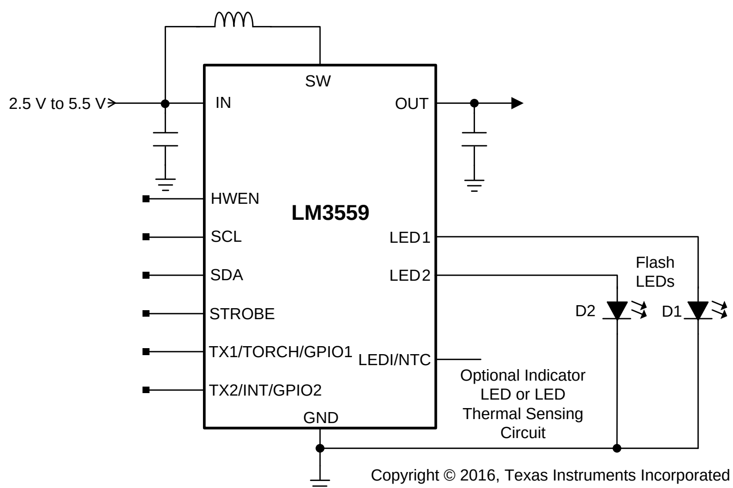


Figure 43. LM3559 Typical Application

Typical Applications (continued)

9.2.1.1 Design Requirements

For typical LED flash driver applications, use the parameters listed in Table 19.

Table 19. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Minimum input voltage	2.5 V
Minimum output voltage	1.8 V
Maximum output voltage	5 V
Maximum output current	1.8 A
Switching frequency	2 MHz

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Output Capacitor Selection

The LM3559 is designed to operate with at least a 10-µF ceramic output capacitor. When the boost converter is running the output capacitor supplies the load current during the boost converters on time. When the NMOS switch turns off the inductor energy is discharged through the internal PMOS switch, supplying power to the load and restoring charge to the output capacitor. This causes a sag in the output voltage during the on time and a rise in the output voltage during the off time. Therefore, choose the output capacitor to limit the output ripple to an acceptable level depending on load current and input/output voltage differentials and also to ensure the converter remains stable.

For proper operation the output capacitor must be at least a 10-µF ceramic. Larger capacitors such as a 22-µF or capacitors in parallel can be used if lower output voltage ripple is desired. To estimate the output voltage ripple considering the ripple due to capacitor discharge (ΔV_Q) and the ripple due to the equivalent series resistance (ESR) of the capacitor (ΔV_{ESR}) use Equation 1 and Equation 2:

For continuous conduction mode, the output voltage ripple due to the capacitor discharge is:

$$\Delta V_Q = \frac{I_{LED} \times (V_{OUT} - V_{IN})}{f_{SW} \times V_{OUT} \times C_{OUT}} \tag{1}$$

The output voltage ripple due to the output capacitors ESR is found by:

$$\Delta V_{ESR} = R_{ESR} \times \left(\frac{I_{LED} \times V_{OUT}}{V_{IN}}\right) + \Delta I_L$$

where

$$\Delta I_L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}} \tag{2}$$

In ceramic capacitors the ESR is very low so a close approximation is to assume that 80% of the output voltage ripple is due to capacitor discharge and 20% from ESR. Table 20 lists different manufacturers for various output capacitors and their case sizes suitable for use with the LM3559.

9.2.1.2.2 Input Capacitor Selection

Choosing the correct size and type of input capacitor helps minimize the voltage ripple caused by the switching of the device boost converter, and reduces noise on the input terminal of the boost converter that can feed through and disrupt internal analog signals. In the *Figure 43* a 10-µF ceramic input capacitor works well. It is important to place the input capacitor as close as possible to the device input (IN) pin. This reduces the series resistance and inductance that can inject noise into the device due to the input switching currents. Table 20 lists various input capacitors that TI recommends for use with the LM3559.

Table 20. Recommended Input/Output Capacitors (X5r Dielectric)

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	VOLTAGE RATING
TDK Corporation	C1608JB0J106M	10 µF	0603 (1.6 mm × 0.8 mm × 0.8 mm)	6.3 V
TDK Corporation	C2012JB1A106M	10 µF	0805 (2 mm × 1.25 mm ×1.25 mm)	10 V
TDK Corporation	C2012JB0J226M	22 µF	0805 (2 mm × 1.25 mm ×1.25 mm)	6.3 V
Murata	GRM188R60J06M	10 µF	0603 (1.6 mm × 0.8 mm × 0.8 mm)	6.3 V
Murata	GRM21BR61A106KE19	10 µF	0805 (2 mm ×1.25 mm × 1.25 mm)	10 V
Murata	GRM21BR60J226ME39L	22 µF	0805 (2 mm ×1.25 mm ×1.25 mm)	6.3 V

9.2.1.2.3 Inductor Selection

The LM3559 is designed to use a 1-µH or 2.2-µH inductor. Table 21 lists various inductors and their manufacturers that can work well with the LM3559. When the device is boosting (V_{OUT} > V_{IN}) the inductor typically is the largest area of efficiency loss in the circuit. Therefore, choosing an inductor with the lowest possible series resistance is important. Additionally, the saturation rating of the inductor must be greater than the maximum operating peak current of the LM3559. This prevents excess efficiency loss that can occur with inductors that operate in saturation and prevents overheating of the inductor and further efficiency loss. For proper inductor operation and circuit performance ensure that the inductor saturation and the peak current limit setting of the LM3559 is greater than I_{PEAK} in *Equation 3*:

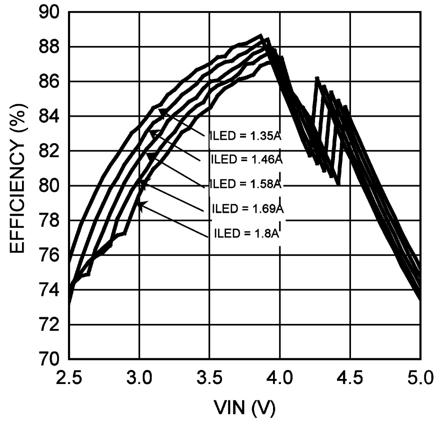
$$I_{PEAK} = \frac{I_{LOAD}}{\eta} \times \frac{V_{OUT}}{V_{IN}} + \Delta I_L \quad \text{where} \quad \Delta I_L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}} \tag{3}$$

where
- f_{SW} = 2 MHz
- Efficiency can be found in *Typical Characteristics*

Table 21. Recommended Inductors

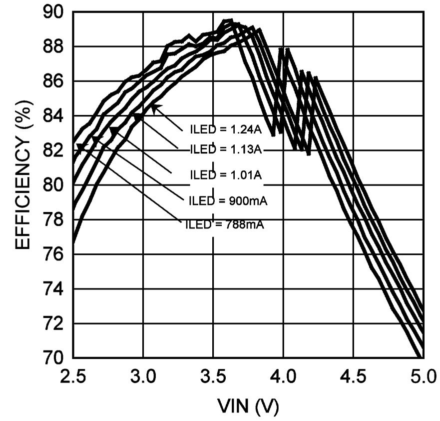
MANUFACTURER	L	PART NUMBER	DIMENSIONS (L×W×H)	I_{SAT}	R_{DC}
TOKO	2.2 µH	FDSD0312-H-2R2M	3 mm × 3.2 mm × 1.2 mm	2.3 A	105 mΩ
TOKO	1 µH	FDSD0312-H-1R0M	3 mm × 3.2 mm × 1.2 mm	3.4 A	43 mΩ
TOKO	1.5 µH	FDSD0312-H-1R5M	3 mm × 3.2 mm × 1.2 mm	2.8 A	71 mΩ
TOKO	2.2 µH	FDSD0312-2R2M	3 mm × 3.2 mm × 1.2 mm	2.3 A	145 mΩ
TOKO	1 µH	FDSD0312-1R0M	3 mm × 3.2 mm × 1.2 mm	3.4 A	70 mΩ
TDK	1 µH	VLS4012ET-1R0N	4 mm × 4 mm × 1.2 mm	2.8 A	50 mΩ
TDK	2.2 µH	VLS252012T-2R2M1R3	2 mm × 2.5 mm × 1.2 mm	1.5 A	130 mΩ

9.2.1.3 Application Curves



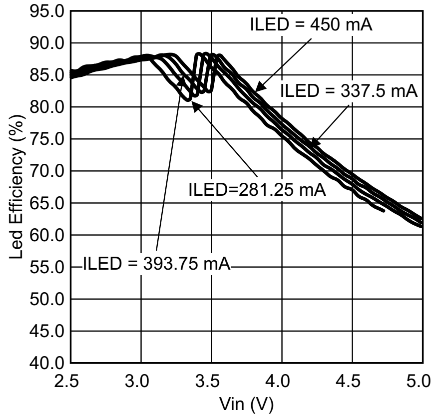
Flash Brightness Codes 0xBB - 0xFF

Figure 44. LED Efficiency vs V_{IN} Dual LEDs



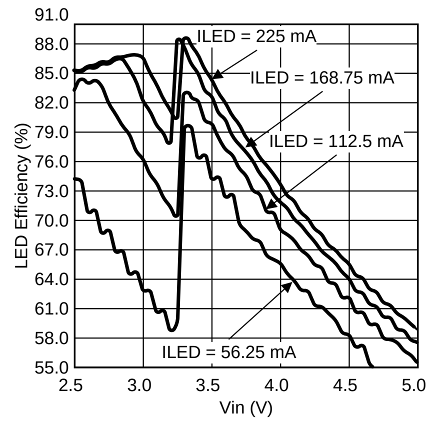
Flash Brightness Codes 0x88 - 0xAA

Figure 45. LED Efficiency vs V_{IN} Dual LEDs



Torch Brightness Codes 0x0F - 0xCF

Figure 46. LED Efficiency vs V_{IN} Dual LEDs



Torch Brightness Codes 0x00 - 0x04

Figure 47. LED Efficiency vs V_{IN} Dual LEDs

9.2.2 LM3559 Typical Application Circuit With Thermistor

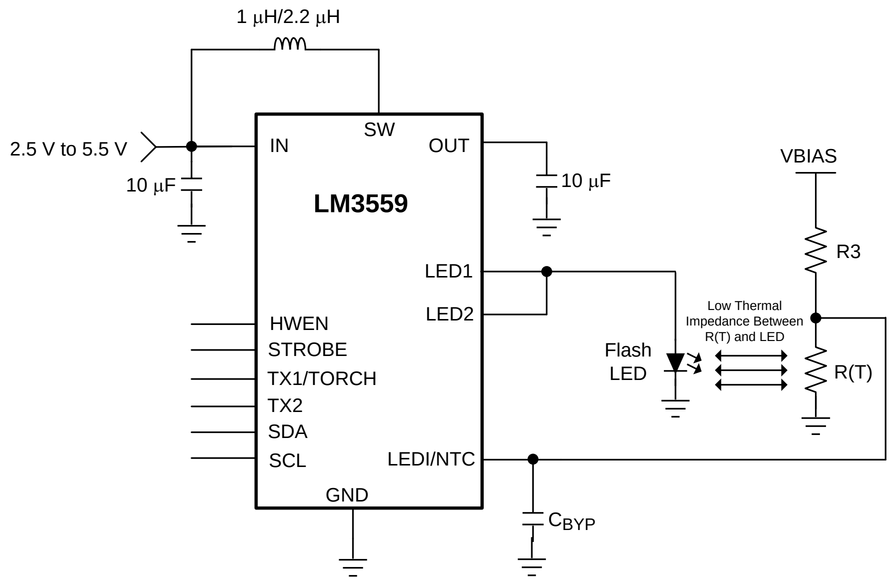


Figure 48. LM3559 Typical Application Circuit With Thermistor

9.2.2.1 Detailed Design Procedure

9.2.2.1.1 NTC Thermistor Selection

Programming bit [4] of Configuration Register 1 with a 1 selects NTC mode and makes the LEDI/NTC pin a comparator input for flash LED thermal sensing. Figure 48 shows the LM3559 using the NTC thermistor circuit. The thermal sensor resistor divider is composed of R3 and R(T), where R(T) is the Negative Temperature Coefficient Thermistor, V_{BIAS} is the bias voltage for the resistive divider, and R3 is used to linearize the NTC's response around the NTC comparators trip point. C_{BYP} is used to filter noise at the NTC input.

In designing the NTC circuit, we must choose values for V_{BIAS}, R(T) and R3. To begin with, NTC thermistors have a non-linear relationship between temperature and resistance:

$$R(T) = R_{25°C} \times e^{\left[\beta\left(\frac{1}{T\,°C + 273} - \frac{1}{298}\right)\right]} \tag{4}$$

where β is given in the thermistor datasheet and R_{25C} is the thermistors value at 25°C. R3 is chosen so that the temperature-to-resistance relationship becomes more linear and can be found by solving for R3 in the R(T) and R3 resistive divider:

$$R3 = \frac{R_{T(TRIP)}\left(V_{BIAS} - V_{TRIP}\right)}{V_{TRIP}}$$

where

- $R_{(T)TRIP}$ is the value of the thermistor at the temperature trip point
- V_{TRIP} = 1 V (typical) (5)

As an example, with V_{BIAS} = 2.5 V and a thermistor whose nominal value at 25°C is 100 kΩ and a β = 4500 K, the trip point is chosen to be 93°C. The value of $R_{(T)}$ at 93°C is:

$$R(T) = 100\,k\Omega \times e^{\left[\beta\left(\frac{1}{93 + 273} - \frac{1}{298}\right)\right]} = 6.047\,k\Omega$$

$$\text{R3 is then: } \frac{6.047\,k\Omega \times (2.5V - 1V)}{1V} = 9.071\,k\Omega \tag{6}$$

Figure 49 shows the linearity of the thermistor resistive divider of the previous example.

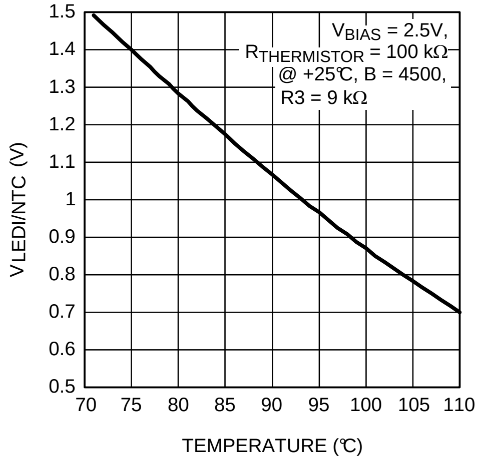


Figure 49. Thermistor Resistive Divider Response vs Temperature

10 Power Supply Recommendations

The LM3556 is designed to operate from an input supply range of 2.5 V to 5.5 V. This input supply must be well regulated and provide the peak current required by the LED configuration and inductor selected.

11 Layout

11.1 Layout Guidelines

The high switching frequency and large switching currents of the LM3559 make the choice of layout important. The following steps should be used as a reference to ensure the device is stable and maintains proper LED current regulation across its intended operating voltage and current range.

1. Place C_{IN} on the top layer (same layer as the LM3559) and as close as possible to the device. The input capacitor conducts the driver currents during the low side MOSFET turnon and turnoff and can detect current spikes over 1 A in amplitude. Connecting the input capacitor through short wide traces to both the IN and GND terminals reduces the inductive voltage spikes that occur during switching and which can corrupt the V_{IN} line.
2. Place C_{OUT} on the top layer (same layer as the LM3559) and as close as possible to the OUT and GND pins. The returns for both C_{IN} and C_{OUT} must come together at one point, and as close as possible to the GND pin. Connecting C_{OUT} through short wide traces will reduce the series inductance on the OUT and GND pins that can corrupt the V_{OUT} and GND line and cause excessive noise in the device and surrounding circuitry.
3. Connect the inductor on the top layer close to the SW pin. There must be a low-impedance connection from the inductor to SW due to the large DC inductor current and, at the same time, the area occupied by the SW node must be small to reduce the capacitive coupling of the high dV/dt present at SW that can couple into nearby traces.
4. Avoid routing logic traces near the SW node to avoid any capacitively coupled voltages from SW onto any high impedance logic lines such as TX1/TORCH/GPIO1, TX2/INT/GPIO2, HWEN, LEDI/NTC (NTC mode), SDA, and SCL. A good approach is to insert an inner layer GND plane underneath the SW node and between any nearby routed traces. This creates a shield from the electric field generated at SW.
5. Terminate the flash LED cathodes directly to the GND pin of the LM3559. If possible, route the LED returns with a dedicated path to keep the high amplitude LED currents out of the GND plane. For flash LEDs that are routed relatively far away from the LM3559, a good approach is to sandwich the forward and return current paths over the top of each other on two layers. This helps to reduce the inductance of the LED current paths.
6. The NTC thermistor is intended to have its return path connected to the LEDs cathode. This allows the thermistor resistive divider voltage (V_{NTC}) to trip the comparators threshold as V_{NTC} is falling. Additionally, the thermistor-to-LED cathode junction must be connected as closely as possible in order to reduce the thermal impedance between the LED and the thermistor. The drawback is that the return of the thermistor may detect the switching currents from the device boost converter. Because of this, it is necessary to have a filter capacitor at the NTC pin which terminates close to the GND of the LM3559 (see C_{BYP} in Figure 48).

11.2 Layout Example

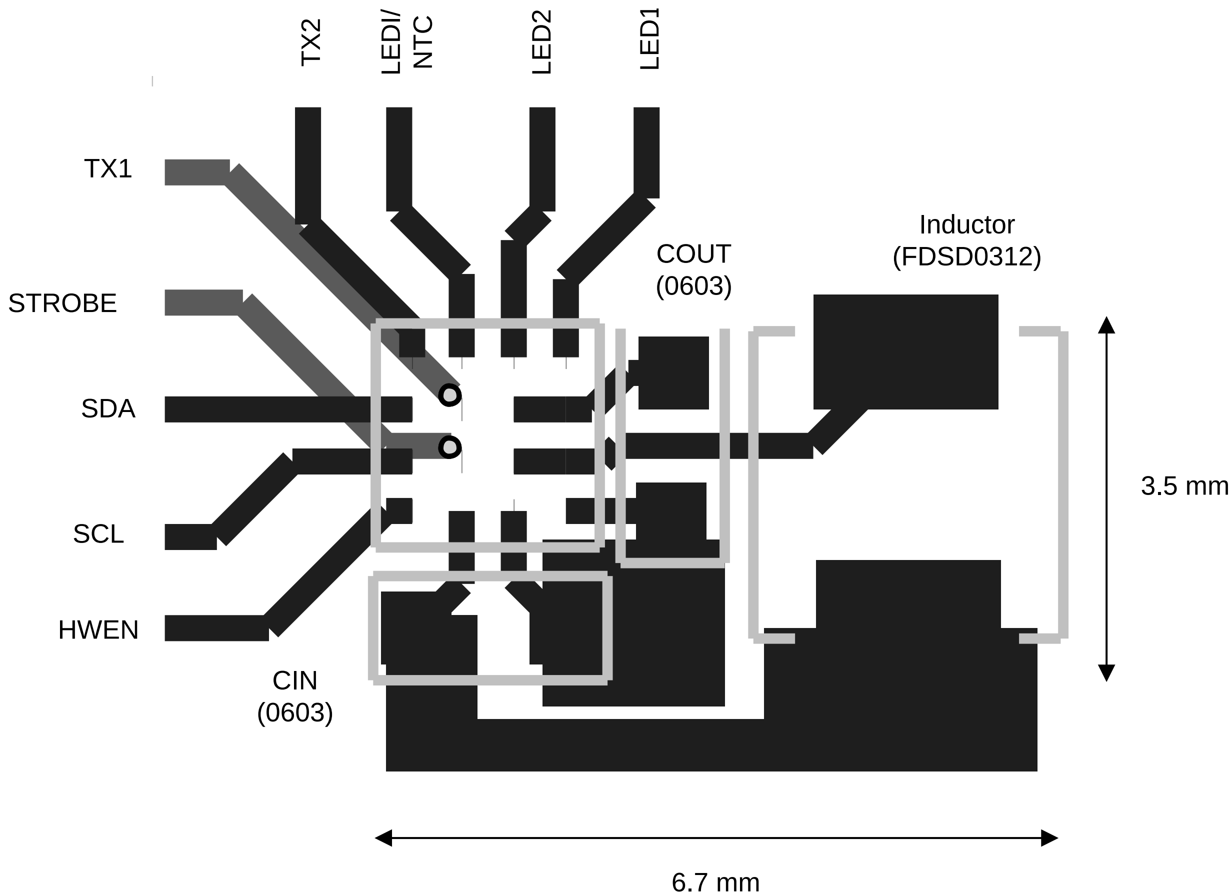


Figure 50. LM3559 Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Documentation Support

12.2.1 Related Documentation

For additional information, see the following:

AN-1112 DSBGA Wafer Level Chip Scale Package (SNVA009)

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates — go to the product folder for your device on ti.com. In the upper right-hand corner, click the *Alert me* button to register and receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM3559TLE/NOPB	Active	Production	DSBGA (YZR) | 16	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	3559
LM3559TLE/NOPB.A	Active	Production	DSBGA (YZR) | 16	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	3559
LM3559TLE/NOPB.B	Active	Production	DSBGA (YZR) | 16	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	3559
LM3559TLX/NOPB	Active	Production	DSBGA (YZR) | 16	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	3559
LM3559TLX/NOPB.A	Active	Production	DSBGA (YZR) | 16	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	3559
LM3559TLX/NOPB.B	Active	Production	DSBGA (YZR) | 16	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	3559

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

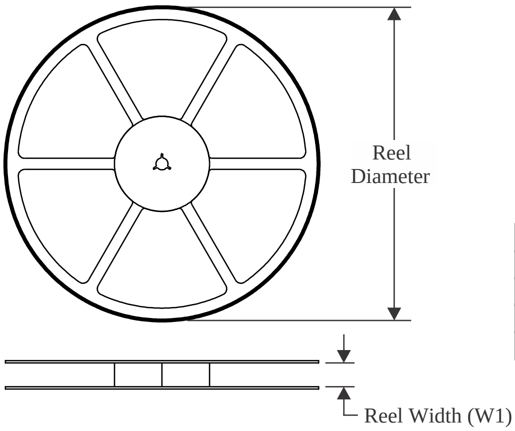
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

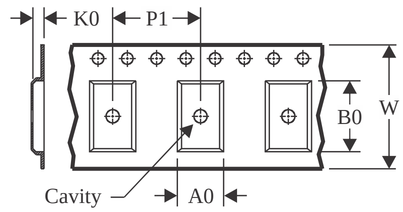
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

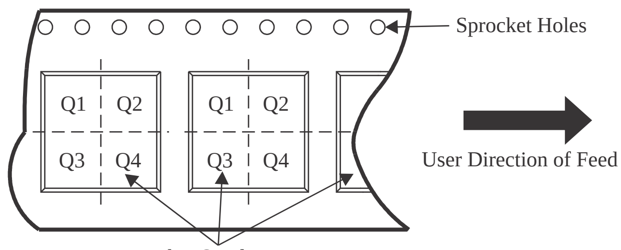


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

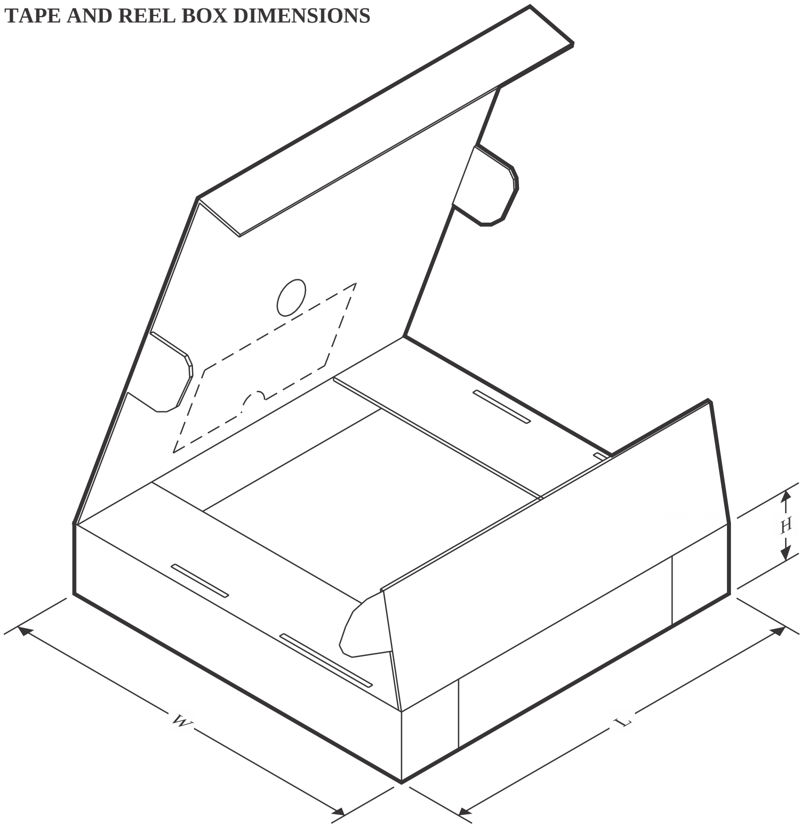
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3559TLE/NOPB	DSBGA	YZR	16	250	178.0	8.4	2.08	2.08	0.76	4.0	8.0	Q1
LM3559TLX/NOPB	DSBGA	YZR	16	3000	178.0	8.4	2.08	2.08	0.76	4.0	8.0	Q1

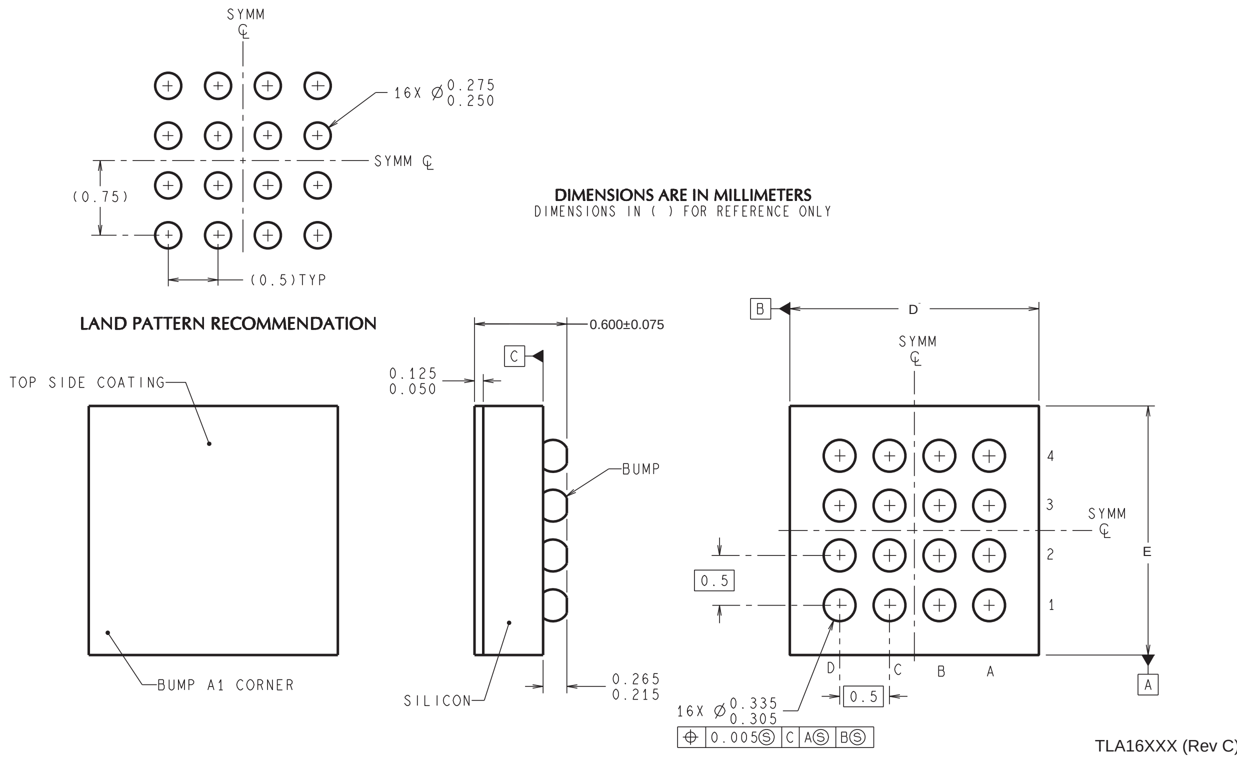
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3559TLE/NOPB	DSBGA	YZR	16	250	208.0	191.0	35.0
LM3559TLX/NOPB	DSBGA	YZR	16	3000	208.0	191.0	35.0

YZR0016



D: Max = 1.99 mm, Min = 1.93 mm

E: Max = 1.99 mm, Min = 1.93 mm

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NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.