LM3630A High-Efficiency Dual-String White LED Driver

1 Features

- Drives up to 2 Strings of 10 Series LEDs
- Wide 2.3-V to 5.5-V Input Voltage Range
- Up to 87% Efficient
- 8-bit I²C-Compatible Programmable Exponential or Linear Brightness Control
- PWM Brightness Control for CABC Operation
- Independent Current Control per String
- True Shutdown Isolation for LEDs
- Internal Soft-Start Limits Inrush Current
- Adaptive Headroom
- Programmable 16-V/24-V/32-V/40-V Overvoltage Protection
- Selectable Boost Frequency of 500 kHz or 1 MHz with Optionally Additional Offset
- Low Profile 12-Pin DSBGA Package
- Solution Size 32 mm²

2 Applications

- Smart-Phone LCD Backlighting
- LCD and Keypad Lighting

3 Description

The LM3630A is a current-mode boost converter which supplies the power and controls the current in up to two strings of 10 LEDs per string. Programming is done over an I²C-compatible interface. The maximum LED current is adjustable from 5 mA to 28.5 mA. At any given maximum LED current the LED brightness is further adjusted with 256 exponential or linear dimming steps. Additionally, pulsed width modulation (PWM) brightness control can be enabled allowing for LED current adjustment by a logic level PWM signal.

The boost switching frequency is programmable at 500 kHz for low switching loss performance or 1 MHz to allow the use of tiny low-profile inductors. A setting for a 10% offset of these frequencies is available. Overvoltage protection is programmable at 16 V, 24 V, 32 V, or 40 V to accommodate a wide variety of LED configurations and Schottky diode/output capacitor combinations.

The device operates over a 2.3-V to 5.5-V operating voltage range and –40°C to +85°C ambient temperature range. The LM3630A is available in an ultra-small 12-bump DSBGA package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (MAX)
LM3630A	DSBGA (12)	1.94 mm × 1.42 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application

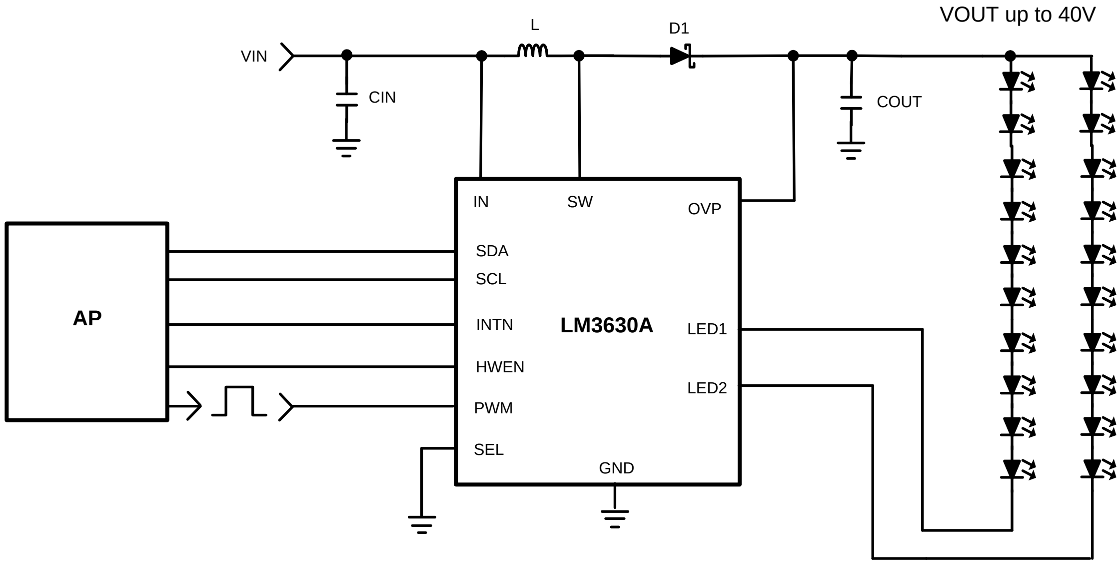


Table of Contents

4 Revision History

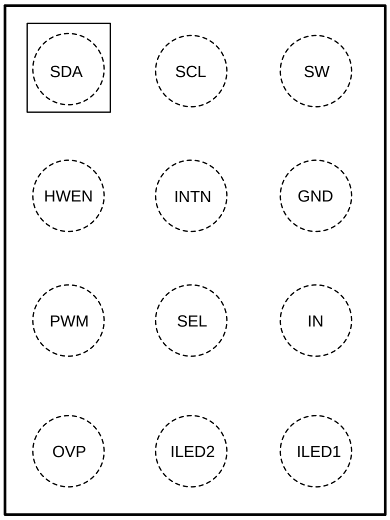
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2014) to Revision B	Page
• Added *Device Information* and *Pin Configuration and Functions* sections, *ESD Rating* table, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections	1

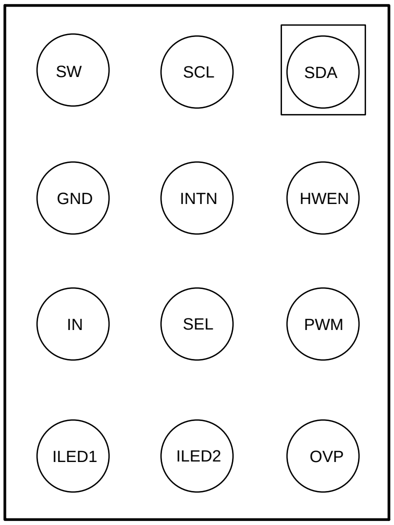
Changes from Original (April 2013) to Revision A	Page
• Changed equation in note 2 of Electrical Char table.	5

5 Pin Configuration and Functions

**YFQ Package
12-Pin DSBGA
Top View**



**YFQ Package
12-Pin DSBGA
Bottom View**



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
A1	SDA	Input/Output	Serial data connection for I^2C-compatible interface
A2	SCL	Input	Serial clock connection for I^2C-compatible interface
A3	SW	PWR	Inductor connection, diode anode connection, and drain connection for internal NFET. Connect the inductor and diode as close as possible to SW to reduce inductance and capacitive coupling to nearby traces.
B1	HWEN	Input	Logic high hardware enable
B2	INTN	Output	Interrupt output for fault status change. Open drain active low signal.
B3	GND	GND	Ground
C1	PWM	Input	External PWM brightness control input
C2	SEL	Input	Selects I^2C-compatible address. Ground selects 7-bit address 36h. V_{IN} selects address 38h.
C3	IN	Input	Input voltage connection. Connect a 2.3-V to 5.5-V supply to IN and bypass to GND with a 2.2-µF or greater ceramic capacitor.
D1	OVP	Input	Output voltage sense connection for overvoltage sensing. Connect OVP to the positive terminal of the output capacitor.
D2	ILED2	Input	Input terminal to internal current sink 2.
D3	ILED1	Input	Input terminal to internal current sink 1.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
IN, HWEN, PWM, SCL, SDA, INTN, SEL to GND		–0.3	6	V
SW, OVP, ILED1, ILED2 to GND		–0.3	45	V
$T_{(J\text{-}MAX)}$	Continuous power dissipation(3)	Internally limited		
	Maximum junction temperature		150	
	Maximum lead temperature (soldering)(4) Vapor phase (60 sec.)		215	°C
	Maximum lead temperature (soldering)(4) Infrared (15 sec.)		220	°C
Storage temperature, T_{stg}		−45	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pin.
(3) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 140°C (typical) and disengages at T_J = 125°C (typical).
(4) For detailed soldering specifications and information, refer to Texas Instruments Application Note 1112: *DSBGA Wafer Level Chip Scale Package* (SNVA009).

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.3		5.5	V
T_A	Operating ambient temperature	−40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		LM3630A YFQ (DBSGA) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	78.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Typical limits are for T_A = 25°C; minimum and maximum limits apply over the full operating ambient temperature range (−40°C ≤ T_A ≤ 85°C); V_{IN} = 3.6 V, unless otherwise specified.(1)

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
ILED1, ILED2	Output current regulation	2.5 V ≤ V_{IN} ≤ 5.5 V, full-scale current = 20 mA		19	20	21	mA
I_{MATCH}	ILED1 to ILED2 current matching (2)	2.5 V ≤ V_{IN} ≤ 5.5 V, I_{LED} = 10 mA, T_A = 25°C	ILED1 on A ILED2 on B	–1%	0.5%	1%	
		2.5 V ≤ V_{IN} ≤ 5.5 V, I_{LED} = 10 mA, 0°C ≤ T_A ≤ 70°C		–2.5%	0.5%	2.5%	
V_{REG_CS}	Regulated current sink headroom voltage	I_{LED} = 5 mA			250		mV
V_{HR}	Current sink minimum headroom voltage	I_{LED} = 95% of nominal, I_{LED} = 20 mA			160	240	
R_{DSON}	NMOS switch on resistance	I_{SW} = 100 mA			0.25		Ω
I_{CL}	NMOS switch current limit	2.5 V ≤ V_{IN} ≤ 5.5 V		480	600	720	mA
				640	800	960	
				800	1000	1200	
				960	1200	1440	
V_{OVP}	Output overvoltage protection	ON threshold, 2.3 V ≤ V_{IN} ≤ 5.5 V	24-V option	23	24	25	V
		ON threshold, 2.3 V ≤ V_{IN} ≤ 5.5 V	40-V option	39	41	44	
		Hysteresis			1		
f_{SW}	Switching frequency	2.5 V ≤ V_{IN} ≤ 5.5 V	560-kHz shift = 1	538	560	582	kHz
			500-kHz shift = 0	481	500	518	
			1.12-MHz shift = 1	1077	1120	1163	
			1-MHz shift = 0	962	1000	1038	
D_{MAX}	Maximum duty cycle				94%		
I_Q	Quiescent current into device, not switching	V_{IN} = 3.6 V	ILED1 = ILED2 = 20 mA, feedback disabled.		350		µA
I_{SHDN}	Shutdown current	2.3 V ≤ V_{IN} ≤ 5.5 V	HWEN = V_{IN}, I^2C shutdown		1	4	µA
			HWEN = GND		1	4	
I_{LED_MIN}	Minimum LED current in ILED1 or ILED2	Full-scale current = 20 mA, BRT = 0x01, Exponential mapping mode			13		
T_{SD}	Thermal shutdown				140		°C
	Hysteresis				15		
t_{WAIT}	Initialization timing	Time period to wait from the assertion of HWEN or after software reset, before an I^2C transaction will be ACK'ed. During this time period an I^2C transaction will be NAK'ed		1			ms

(1) Minimum and maximum limits are specified by design, test, or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm. Unless otherwise specified, conditions for typical specifications are: V_{IN} = 3.6 V and T_A = 25°C.
(2) LED current sink matching between LED1 and LED2 is given by taking the difference between ILED1 and ILED2 and dividing by the sum of ILED1 and ILED2. The formula is $(I_{LED1} - I_{LED2})/(I_{LED1} + I_{LED2})$ at I_{LED} = 10 mA. I_{LED1} is driven by Bank A and I_{LED2} is driven by Bank B.

Electrical Characteristics (continued)

Typical limits are for T_A = 25°C; minimum and maximum limits apply over the full operating ambient temperature range (−40°C ≤ T_A ≤ 85°C); V_{IN} = 3.6 V, unless otherwise specified.(1)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
LOGIC INPUTS (PWM, HWEN, SEL, SCL, SDA)						
V_{IL}	Input logic low	2.3 V ≤ V_{IN} ≤ 5.5 V	0		0.4	V
V_{IH}	Input logic high	2.3 V ≤ V_{IN} ≤ 5.5 V	1.2		V_{IN}	V
V_{OL}	Output logic low (SDA, INTN)	2.3 V ≤ V_{IN} ≤ 5.5 V			400	mV
f_{PWM}	PWM input frequency	2.3 V ≤ V_{IN} ≤ 5.5 V	10		80	kHz
C_{IN}	Input capacitance	SDA		4.5		pF
		SCL		5		pF

6.6 I²C-Compatible Timing Requirements (SCL, SDA)

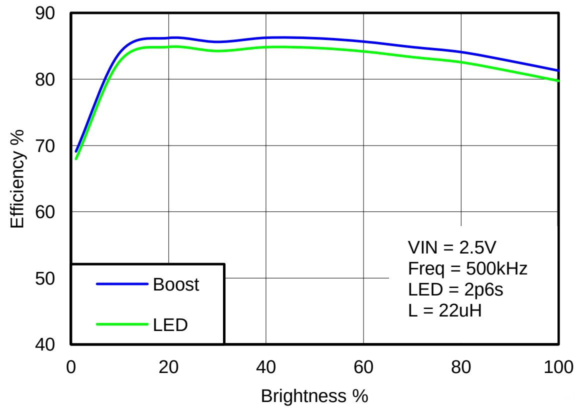
See (1).

		MIN	NOM	MAX	UNIT
t_1	SCL (clock period)	2.5			µs
t_2	Data in setup time to SCL high	100			ns
t_3	Data in setup time to SCL low	0			ns
t_4	SDA low setup time to SCL low (start)	100			ns
t_5	SDA high hold time to SCL high (stop)	100			ns

(1) SCL and SDA must be glitch-free in order for proper brightness to be realized.

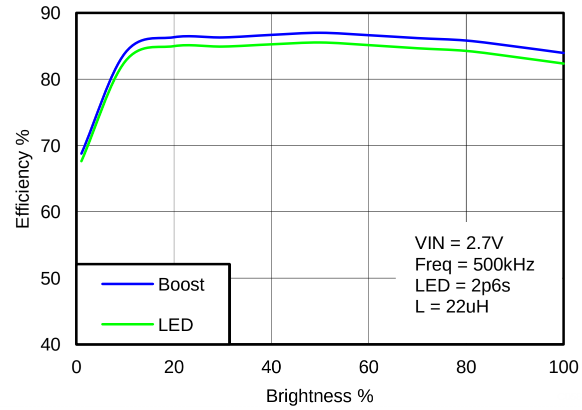
6.7 Typical Characteristics

T_A = 25°C, I_{LED} full-scale = 20 mA, unless specified otherwise.



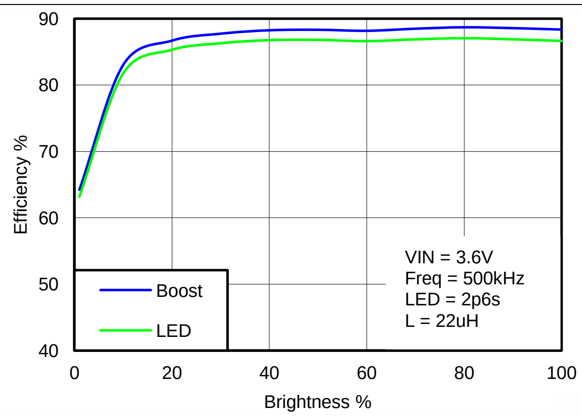
V_{IN} = 2.5 V 2p6s L = 22 µH
Frequency = 500 kHz

Figure 1. Boost and LED Efficiency



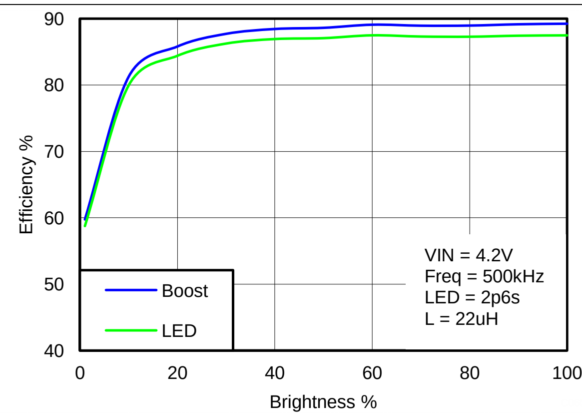
V_{IN} = 2.7 V 2p6s L = 22 µH
Frequency = 500 kHz

Figure 2. Boost and LED Efficiency



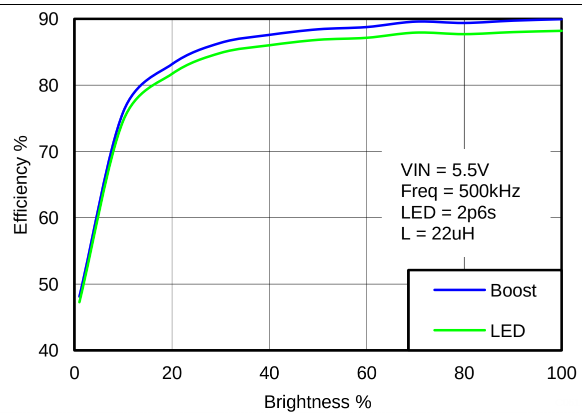
V_{IN} = 3.6 V 2p6s L = 22 µH
Frequency = 500 kHz

Figure 3. Boost and LED Efficiency



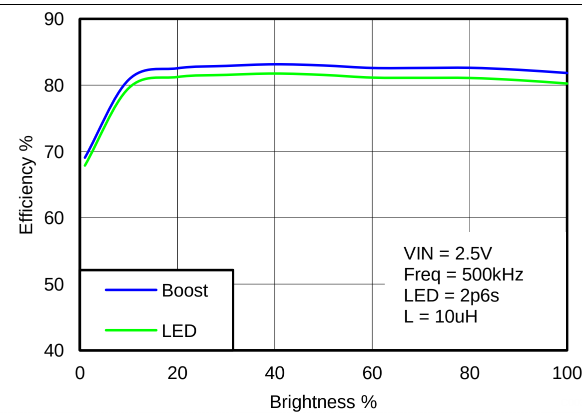
V_{IN} = 4.2 V 2p6s L = 22 µH
Frequency = 500 kHz

Figure 4. Boost And LED Efficiency



V_{IN} = 5.5 V 2p6s L = 22 µH
Frequency = 500 kHz

Figure 5. Boost and LED Efficiency

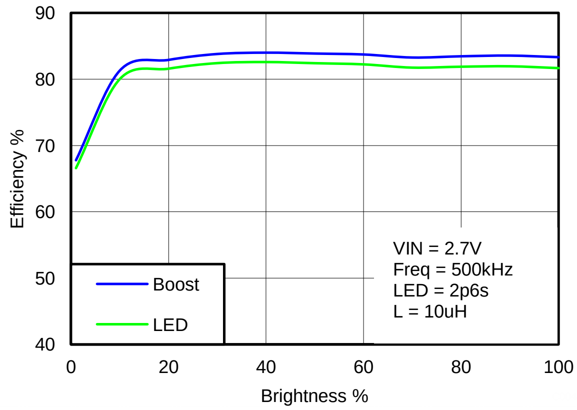


V_{IN} = 2.5 V 2p6s L = 10 µH
Frequency = 500 kHz

Figure 6. Boost and LED Efficiency

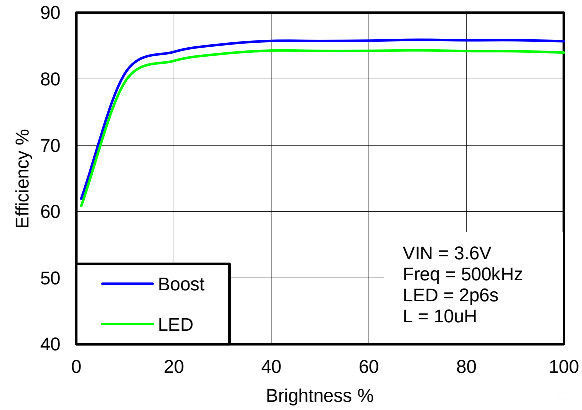
Typical Characteristics (continued)

T_A = 25°C, I_{LED} full-scale = 20 mA, unless specified otherwise.



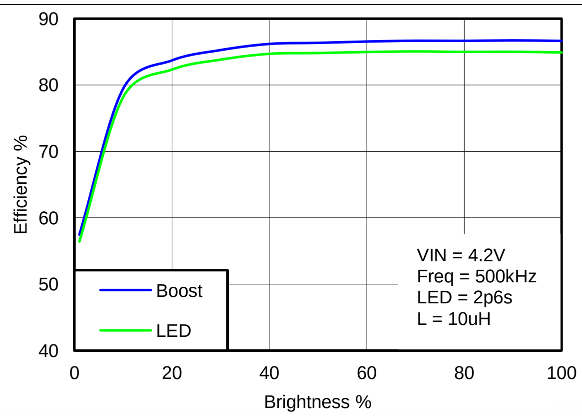
V_{IN} = 2.7 V 2p6s L = 10 µH
Frequency = 500 kHz

Figure 7. Boost and LED Efficiency



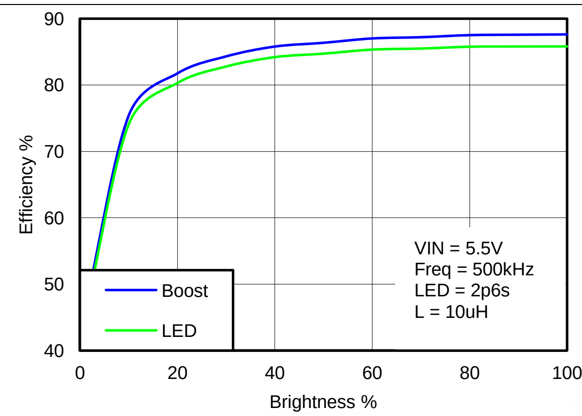
V_{IN} = 3.6 V 2p6s L = 10 µH
Frequency = 500 kHz

Figure 8. Boost and LED Efficiency



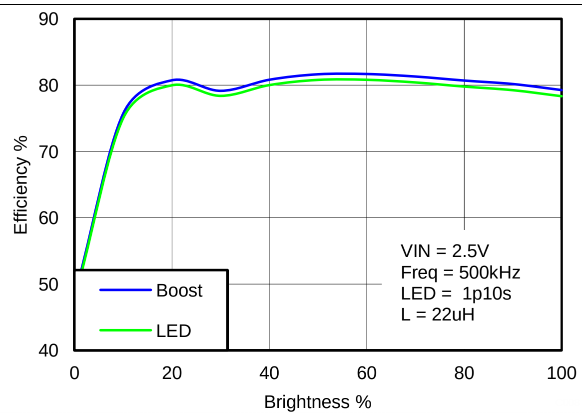
V_{IN} = 4.2 V 2p6s L = 10 µH
Frequency = 500 kHz

Figure 9. Boost and LED Efficiency



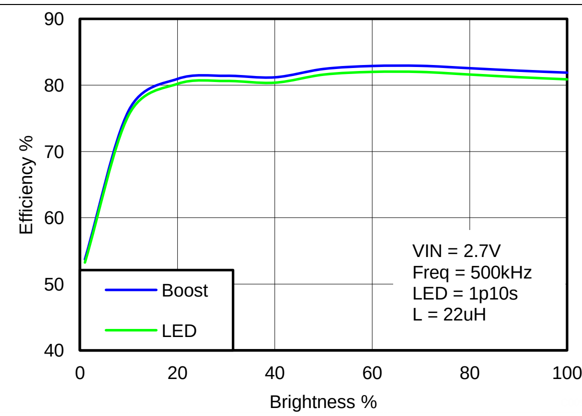
V_{IN} = 5.5 V 2p6s L = 10 µH
Frequency = 500 kHz

Figure 10. Boost and LED Efficiency



V_{IN} = 2.5 V 1p10s L = 22 µH
Frequency = 500 kHz

Figure 11. Boost and LED Efficiency

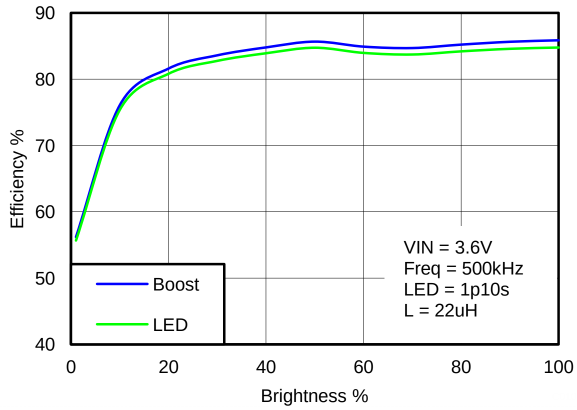


V_{IN} = 2.7 V 1p10s L = 22 µH
Frequency = 500 kHz

Figure 12. Boost and LED Efficiency

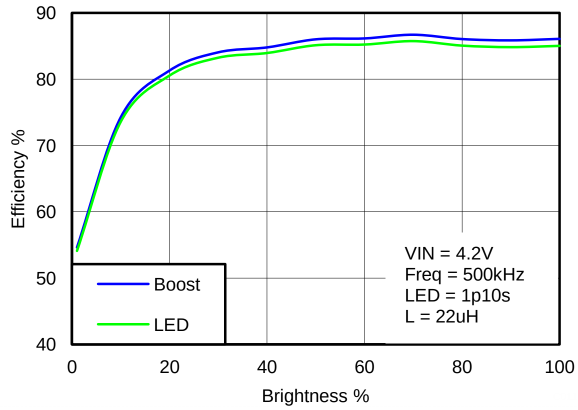
Typical Characteristics (continued)

T_A = 25°C, I_{LED} full-scale = 20 mA, unless specified otherwise.



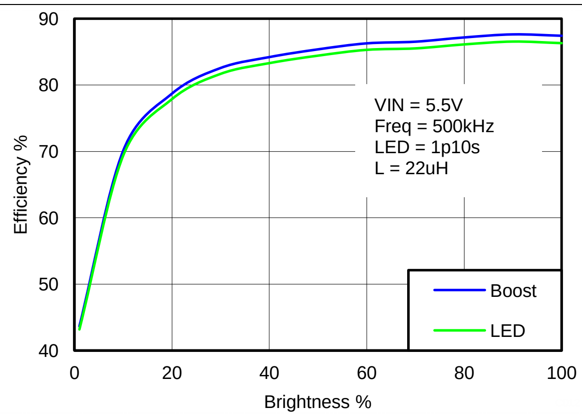
V_{IN} = 3.6 V 1p10s L = 22 µH
Frequency = 500 kHz

Figure 13. Boost and LED Efficiency



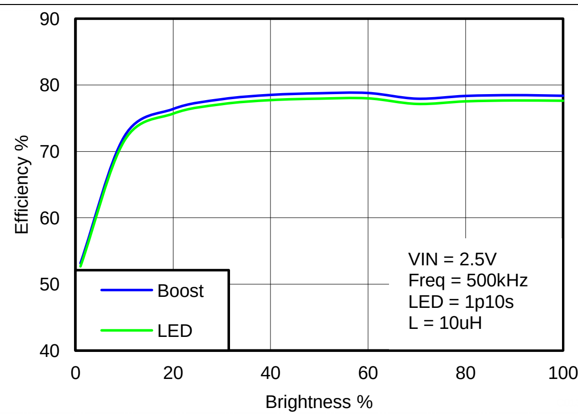
V_{IN} = 4.2 V 1p10s L = 22 µH
Frequency = 500 kHz

Figure 14. Boost and LED Efficiency



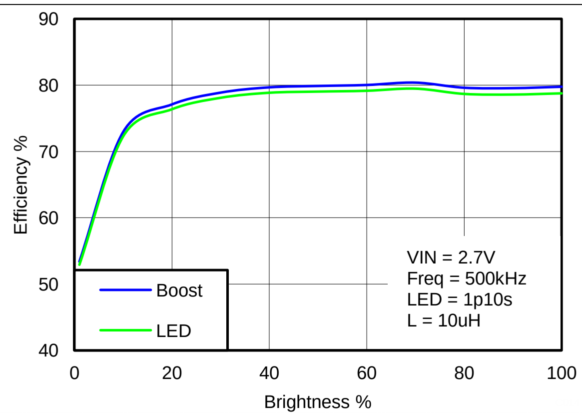
V_{IN} = 5.5 V 1p10s L = 22 µH
Frequency = 500 kHz

Figure 15. Boost and LED Efficiency



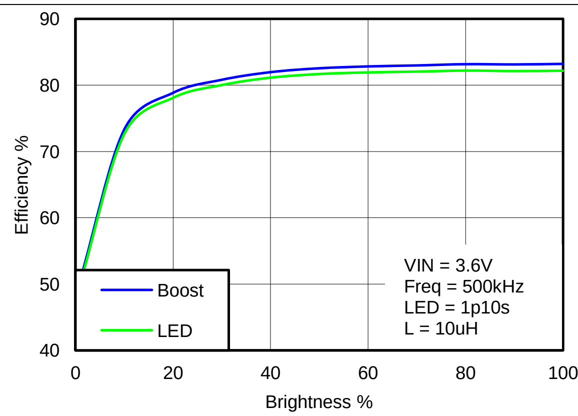
V_{IN} = 2.5 V 1p10s L = 10 µH
Frequency = 500 kHz

Figure 16. Boost and LED Efficiency



V_{IN} = 2.7 V 1p10s L = 10 µH
Frequency = 500 kHz

Figure 17. Boost and LED Efficiency

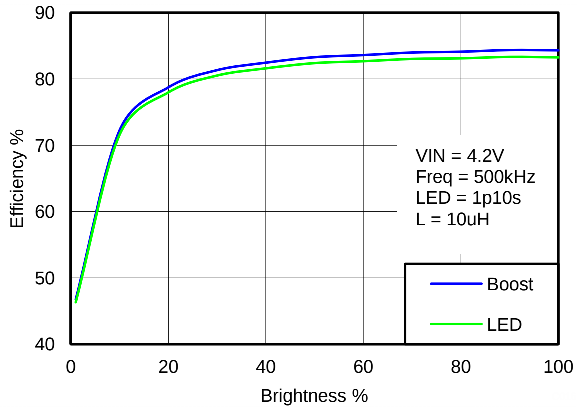


V_{IN} = 3.6 V 1p10s L = 10 µH
Frequency = 500 kHz

Figure 18. Boost and LED Efficiency

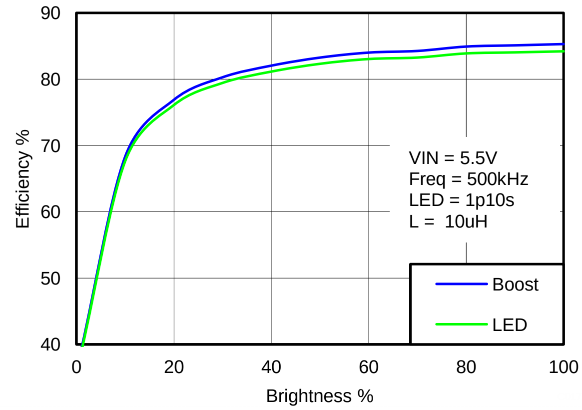
Typical Characteristics (continued)

T_A = 25°C, I_{LED} full-scale = 20 mA, unless specified otherwise.



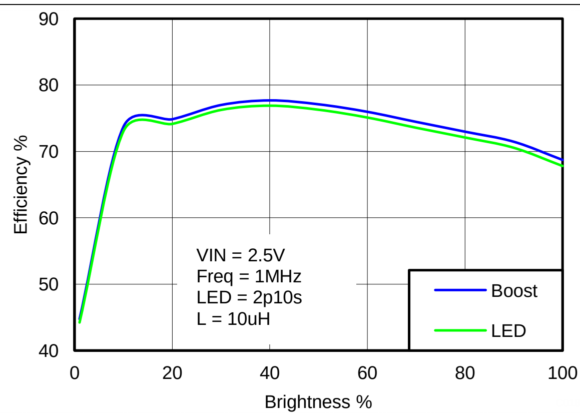
V_{IN} = 4.2 V 1p10s L = 10 µH
Frequency = 500 kHz

Figure 19. Boost and LED Efficiency



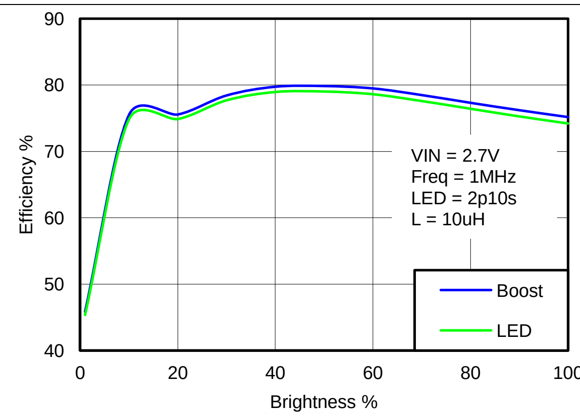
V_{IN} = 5.5 V 1p10s L = 10 µH
Frequency = 500 kHz

Figure 20. Boost and LED Efficiency



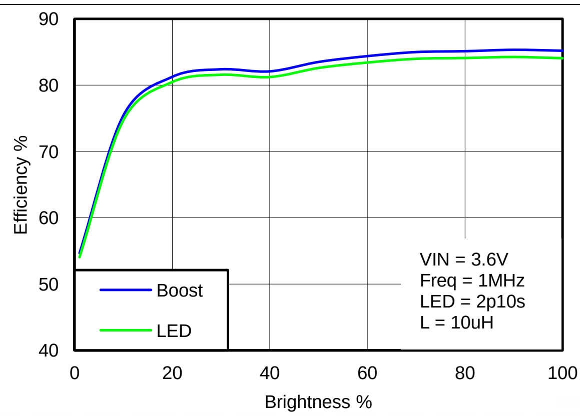
V_{IN} = 2.5 V 2p10s L = 10 µH
Frequency = 1 MHz

Figure 21. Boost and LED Efficiency



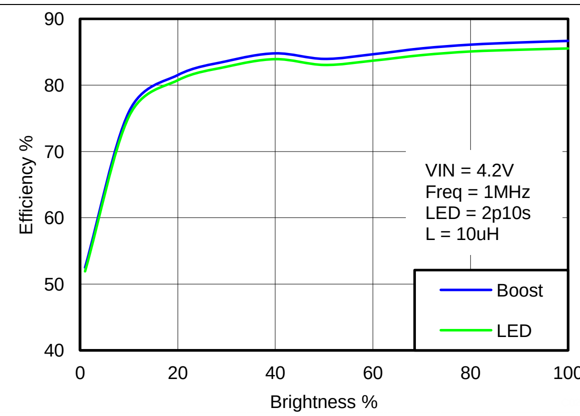
V_{IN} = 2.7 V 2p10s L = 10 µH
Frequency = 1 MHz

Figure 22. Boost and LED Efficiency



V_{IN} = 3.6 V 2p10s L = 10 µH
Frequency = 1 MHz

Figure 23. Boost and LED Efficiency

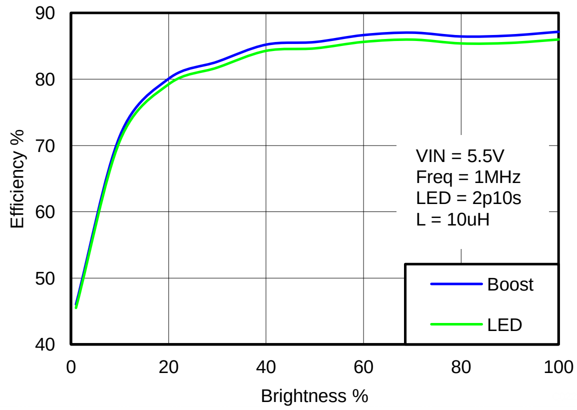


V_{IN} = 4.2 V 2p10s L = 10 µH
Frequency = 1 MHz

Figure 24. Boost and LED Efficiency

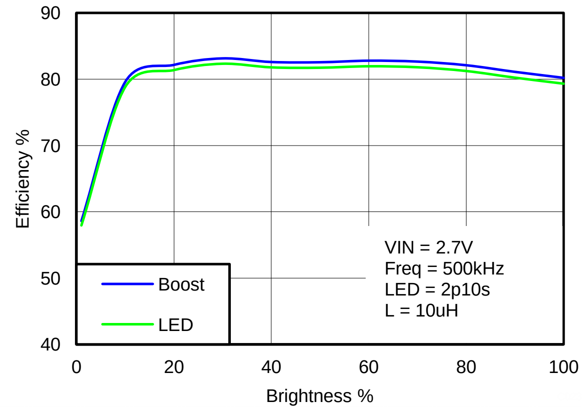
Typical Characteristics (continued)

T_A = 25°C, I_{LED} full-scale = 20 mA, unless specified otherwise.



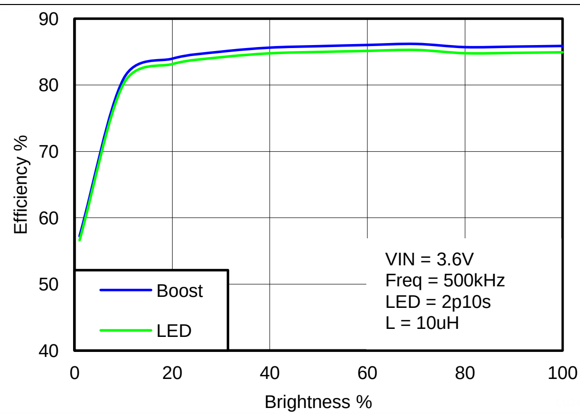
V_{IN} = 5.5 V 2p10s L = 10 µH
Frequency = 1 MHz

Figure 25. Boost and LED Efficiency



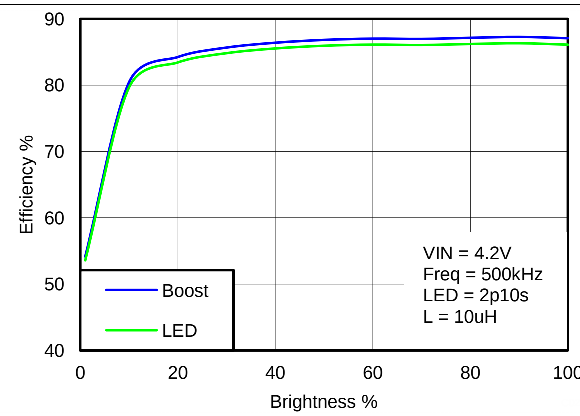
V_{IN} = 2.7 V 2p10s L = 10 µH
Frequency = 500 kHz

Figure 26. Boost and LED Efficiency



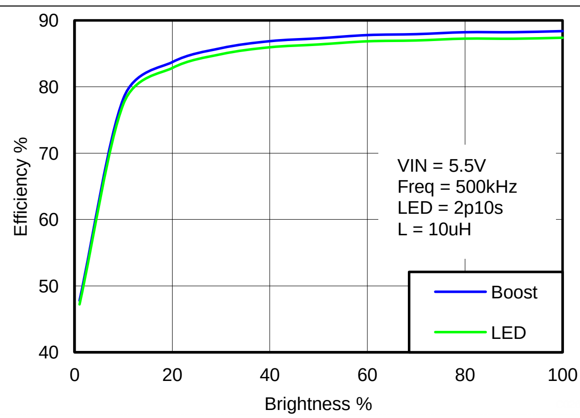
V_{IN} = 3.6 V 2p10s L = 10 µH
Frequency = 500 kHz

Figure 27. Boost and LED Efficiency



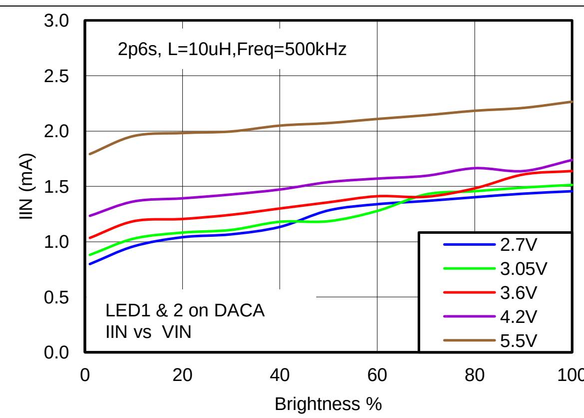
V_{IN} = 4.2 V 2p10s L = 10 µH
Frequency = 500 kHz

Figure 28. Boost and LED Efficiency



V_{IN} = 5.5 V 2p10s L = 10 µH
Frequency = 500 kHz

Figure 29. Boost and LED Efficiency

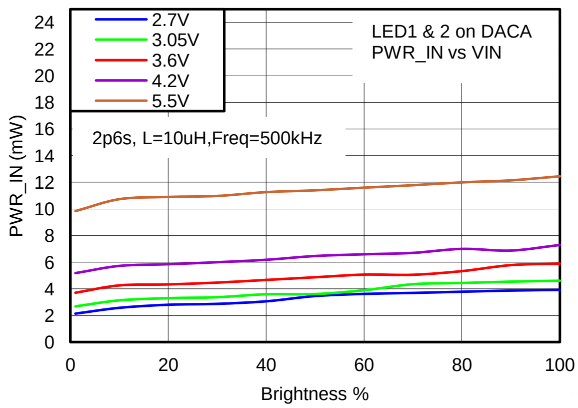


I_{LED} Full Scale = 28.5 mA LED1 and 2 on DACA
Frequency = 500 kHz 2p6s L = 10 µH

Figure 30. I_{IN} Across V_{IN}

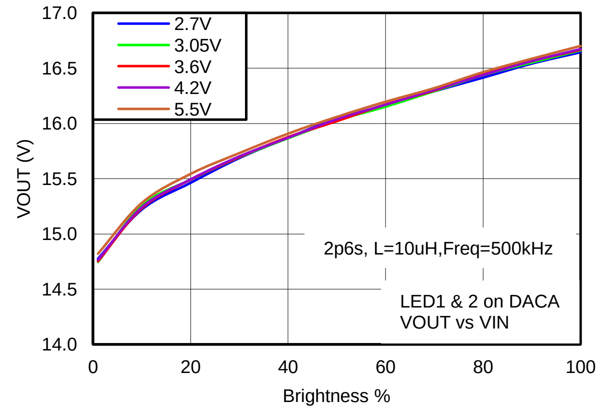
Typical Characteristics (continued)

T_A = 25°C, I_{LED} full-scale = 20 mA, unless specified otherwise.



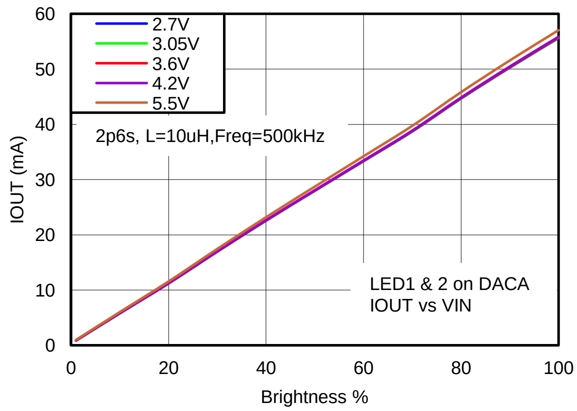
I_{LED} Full Scale = 28.5 mA LED1 and 2 on DACA
Frequency = 500 kHz 2p6s L = 10 µH

Figure 31. P_{WR_IN} Across V_{IN}



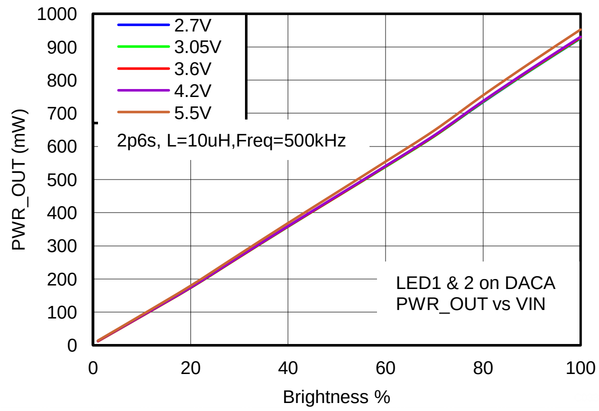
I_{LED} Full Scale = 28.5 mA LED1 and 2 on DACA
Frequency = 500 kHz 2p6s L = 10 µH

Figure 32. V_{OUT} Across V_{IN}



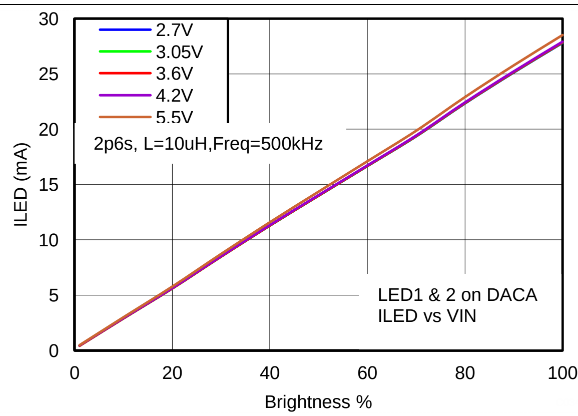
I_{LED} Full Scale = 28.5 mA LED1 and 2 on DACA
Frequency = 500 kHz 2p6s L = 10 µH

Figure 33. I_{OUT} Across V_{IN}



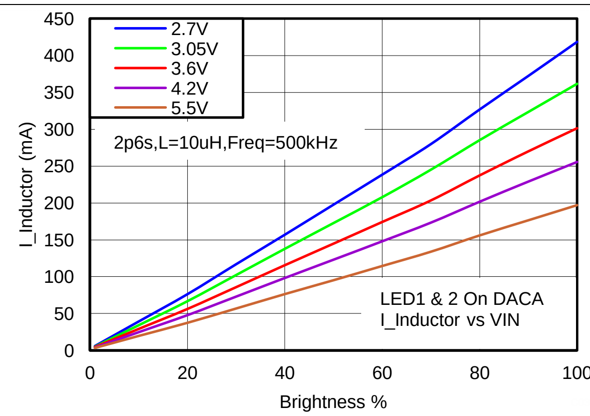
I_{LED} Full Scale = 28.5 mA LED1 and 2 on DACA
Frequency = 500 kHz 2p6s L = 10 µH

Figure 34. P_{WR_OUT} Across V_{IN}



I_{LED} Full Scale = 28.5 mA LED1 and 2 on DACA
Frequency = 500 kHz 2p6s L = 10 µH

Figure 35. I_{LED} Across V_{IN}

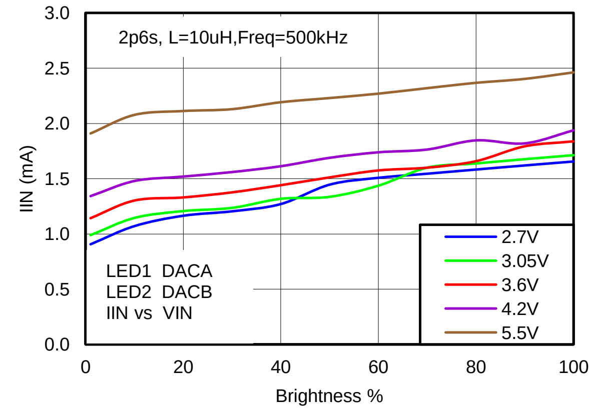


I_{LED} Full Scale = 28.5 mA LED1 and 2 on DACA
Frequency = 500 kHz 2p6s L = 10 µH

Figure 36. $I_{\_INDUCTOR}$ Across V_{IN}

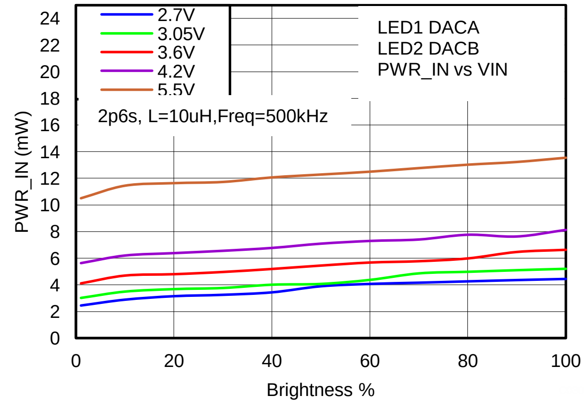
Typical Characteristics (continued)

T_A = 25°C, I_{LED} full-scale = 20 mA, unless specified otherwise.



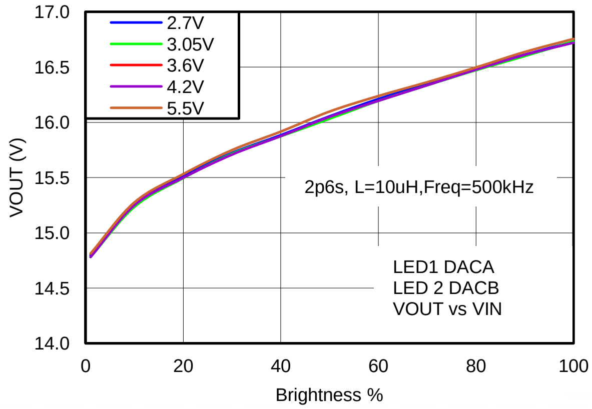
I_{LED} Full Scale = 28.5 mA   LED1 on DACA   2p6s
Frequency = 500 kHz   LED2 on DACB   L = 10 µH

Figure 37. I_{IN} Across V_{IN}



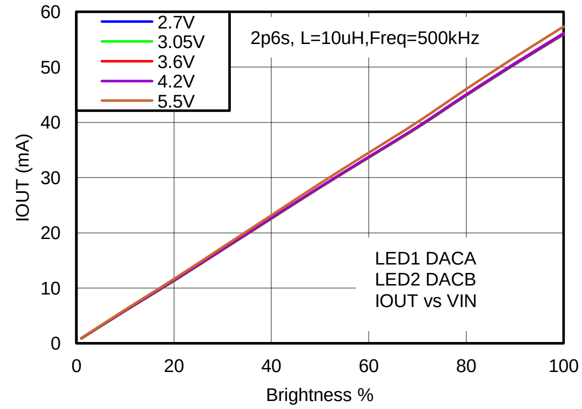
I_{LED} Full Scale = 28.5 mA   LED1 on DACA   2p6s
Frequency = 500 kHz   LED2 on DACB   L = 10 µH

Figure 38. PWR_IN Across V_{IN}



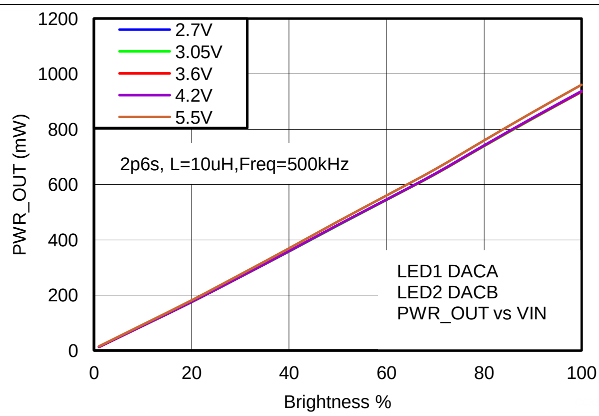
I_{LED} Full Scale = 28.5 mA   LED1 on DACA   2p6s
Frequency = 500 kHz   LED2 on DACB   L = 10 µH

Figure 39. V_{OUT} Across V_{IN}



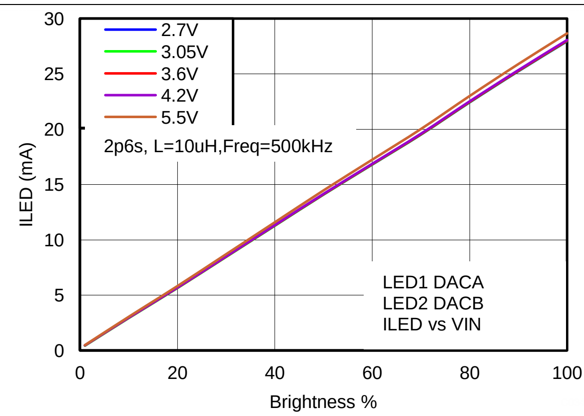
I_{LED} Full Scale = 28.5 mA   LED1 on DACA   2p6s
Frequency = 500 kHz   LED2 on DACB   L = 10 µH

Figure 40. I_{OUT} Across V_{IN}



I_{LED} Full Scale = 28.5 mA   LED1 on DACA   2p6s
Frequency = 500 kHz   LED2 on DACB   L = 10 µH

Figure 41. PWR_OUT Across V_{IN}

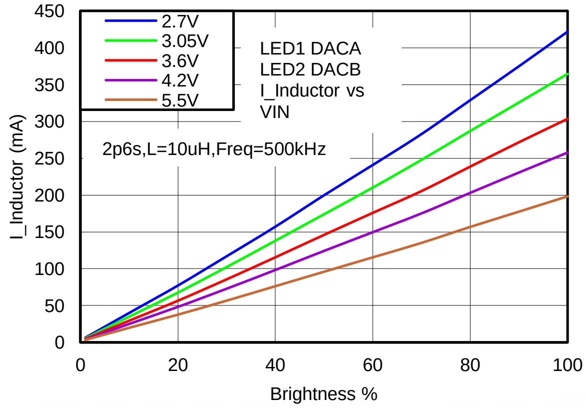


I_{LED} Full Scale = 28.5 mA   LED1 on DACA   2p6s
Frequency = 500 kHz   LED2 on DACB   L = 10 µH

Figure 42. I_{LED} Across V_{IN}

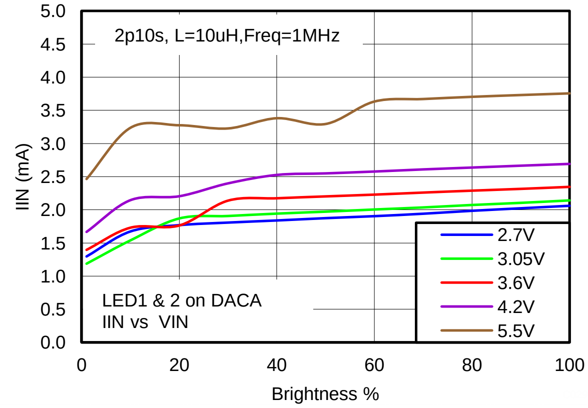
Typical Characteristics (continued)

T_A = 25°C, I_{LED} full-scale = 20 mA, unless specified otherwise.



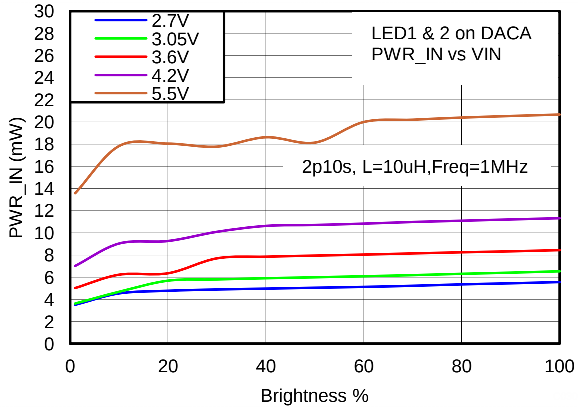
I_{LED} Full Scale = 28.5 mA LED1 on DACA 2p6s
Frequency = 500 kHz LED2 on DACB L = 10 µH

Figure 43. I_INDUCTOR Across V_{IN}



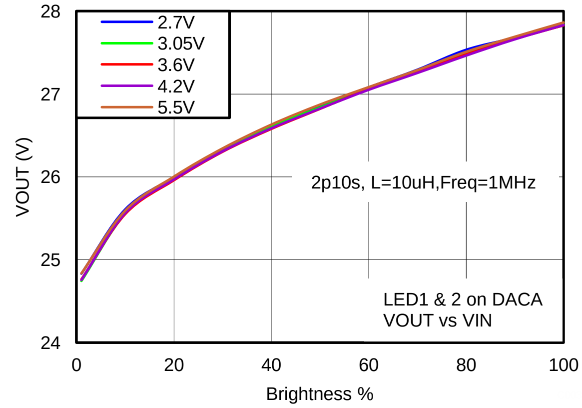
I_{LED} Full Scale = 28.5 mA LED1 and LED2 on DACA
Frequency = 1 MHz 2p10s L = 10 µH

Figure 44. I_{IN} Across V_{IN}



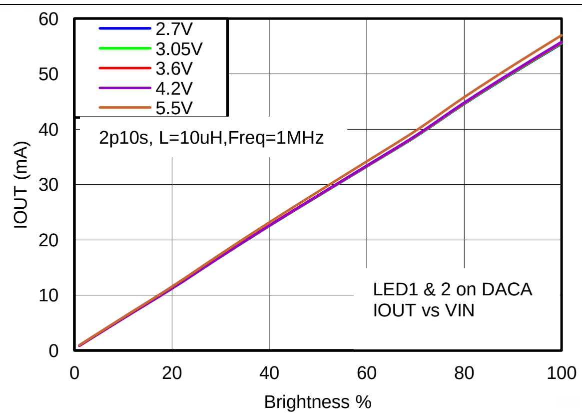
I_{LED} Full Scale = 28.5 mA LED1 and LED2 on DACA
Frequency = 1 MHz 2p10s L = 10 µH

Figure 45. PWR_IN Across V_{IN}



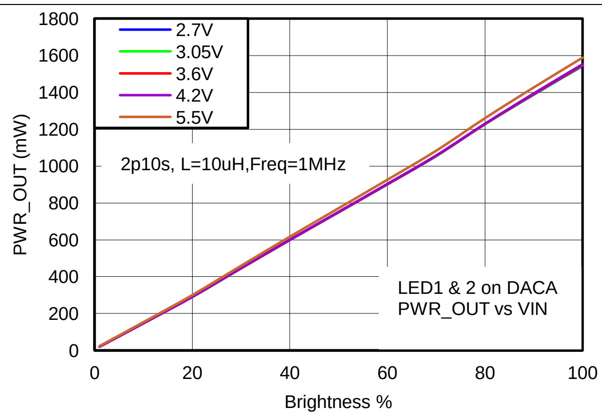
I_{LED} Full Scale = 28.5 mA LED1 and LED2 on DACA
Frequency = 1 MHz 2p10s L = 10 µH

Figure 46. V_{OUT} Across V_{IN}



I_{LED} Full Scale = 28.5 mA LED1 and LED2 on DACA
Frequency = 1 MHz 2p10s L = 10 µH

Figure 47. I_{OUT} Across V_{IN}

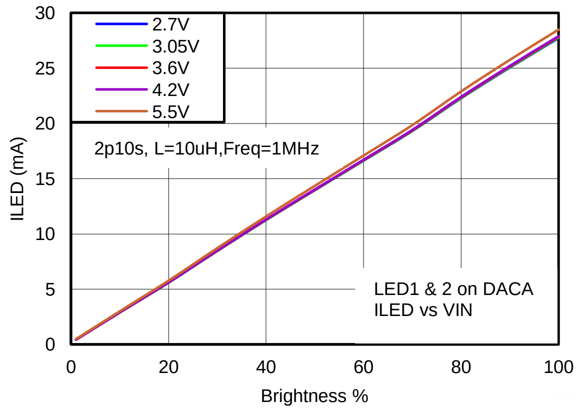


I_{LED} Full Scale = 28.5 mA LED1 and LED2 on DACA
Frequency = 1 MHz 2p10s L = 10 µH

Figure 48. PWR_OUT Across V_{IN}

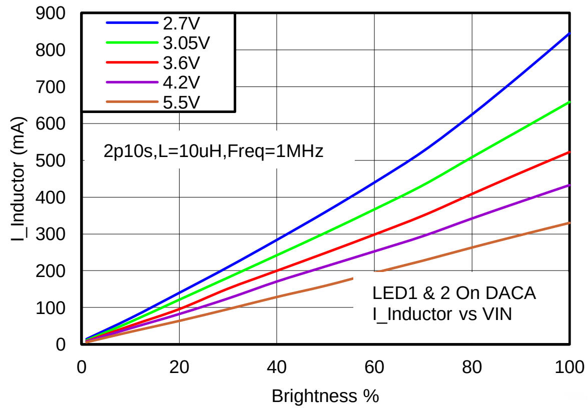
Typical Characteristics (continued)

T_A = 25°C, I_{LED} full-scale = 20 mA, unless specified otherwise.



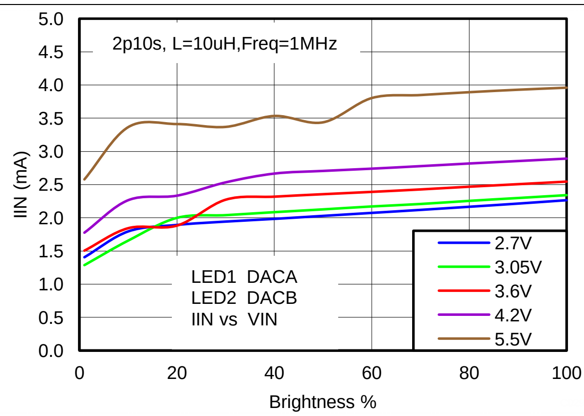
I_{LED} Full Scale = 28.5 mA LED1 and LED2 on DACA
Frequency = 1 MHz 2p10s L = 10 µH

Figure 49. I_{LED} Across V_{IN}



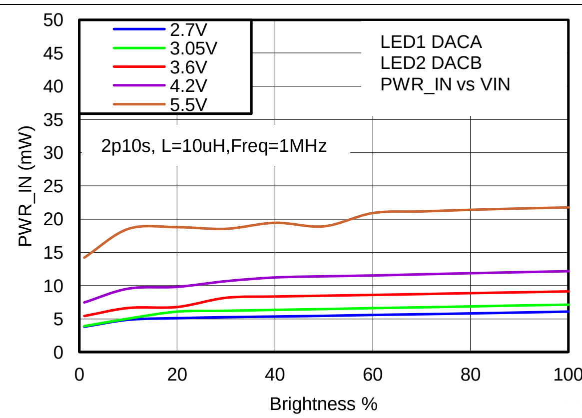
I_{LED} Full Scale = 28.5 mA LED1 and LED2 on DACA
Frequency = 1 MHz 2p10s L = 10 µH

Figure 50. $I_{\_INDUCTOR}$ Across V_{IN}



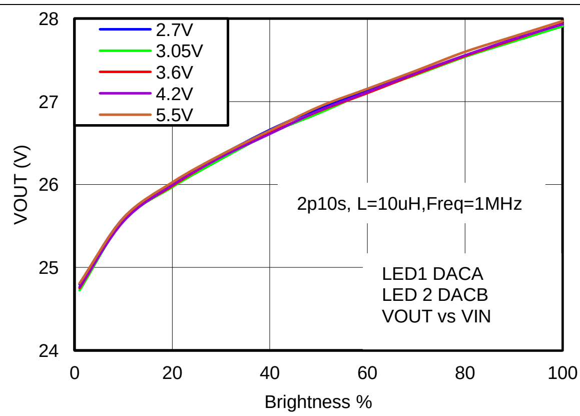
I_{LED} Full Scale = 28.5 mA LED1 on DACA 2p10s
Frequency = 1 MHz LED2 on DACB L = 10 µH

Figure 51. I_{IN} Across V_{IN}



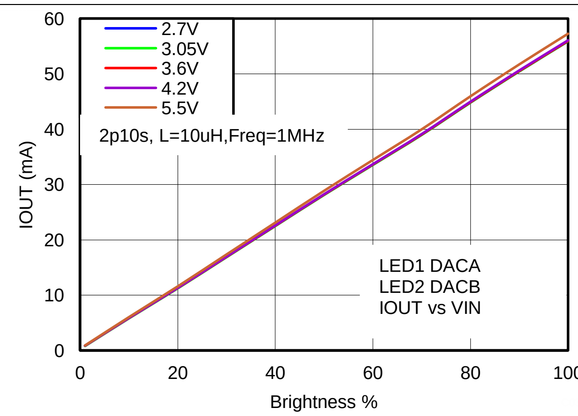
I_{LED} Full Scale = 28.5 mA LED1 on DACA 2p10s
Frequency = 1 MHz LED2 on DACB L = 10 µH

Figure 52. PWR_IN Across V_{IN}



I_{LED} Full Scale = 28.5 mA LED1 on DACA 2p10s
Frequency = 1 MHz LED2 on DACB L = 10 µH

Figure 53. V_{OUT} Across V_{IN}

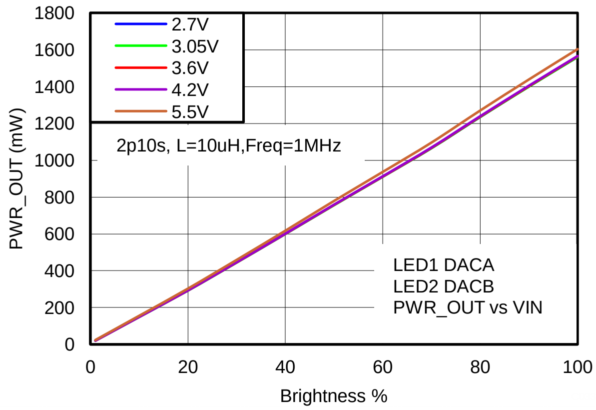


I_{LED} Full Scale = 28.5 mA LED1 on DACA 2p10s
Frequency = 1 MHz LED2 on DACB L = 10 µH

Figure 54. I_{OUT} Across V_{IN}

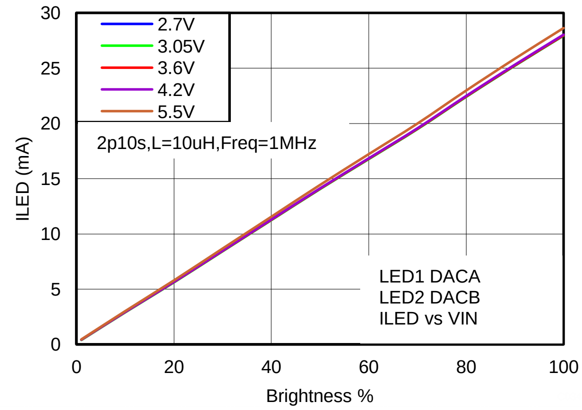
Typical Characteristics (continued)

T_A = 25°C, I_{LED} full-scale = 20 mA, unless specified otherwise.



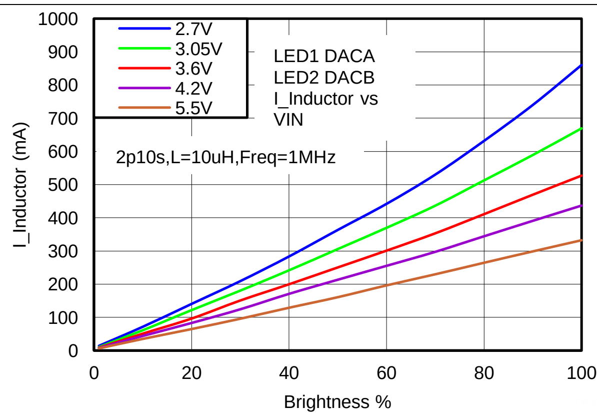
I_{LED} Full Scale = 28.5 mA LED1 on DACA 2p10s
Frequency = 1 MHz LED2 on DACB L = 10 µH

Figure 55. PWR_OUT Across V_{IN}



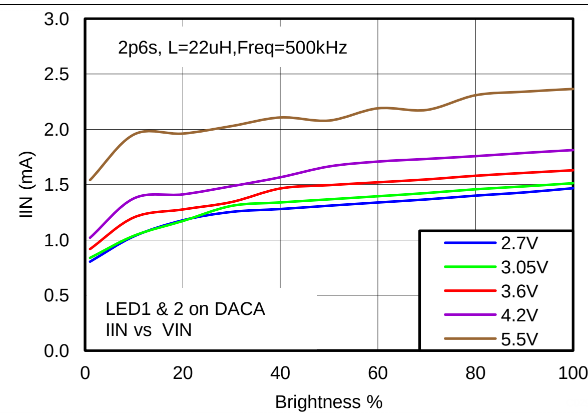
I_{LED} Full Scale = 28.5 mA LED1 on DACA 2p10s
Frequency = 1 MHz LED2 on DACB L = 10 µH

Figure 56. I_{LED} Across V_{IN}



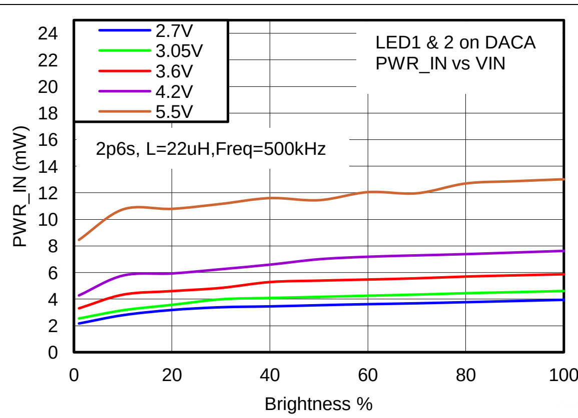
I_{LED} Full Scale = 28.5 mA LED1 on DACA 2p10s
Frequency = 1 MHz LED2 on DACB L = 10 µH

Figure 57. $I_{\_INDUCTOR}$ Across V_{IN}



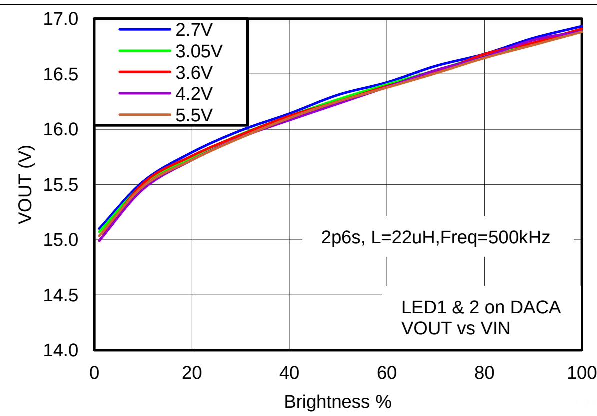
I_{LED} Full Scale = 28.5 mA LED1 and LED2 on DACA
Frequency = 500 kHz 2p6s L = 22 µH

Figure 58. I_{IN} Across V_{IN}



I_{LED} Full Scale = 28.5 mA LED1 and LED2 on DACA
Frequency = 500 kHz 2p6s L = 22 µH

Figure 59. PWR_I_{IN} Across V_{IN}

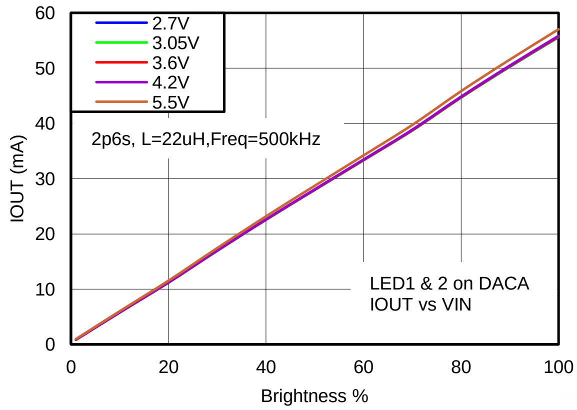


I_{LED} Full Scale = 28.5 mA LED1 and LED2 on DACA
Frequency = 500 kHz 2p6s L = 22 µH

Figure 60. V_{OUT} Across V_{IN}

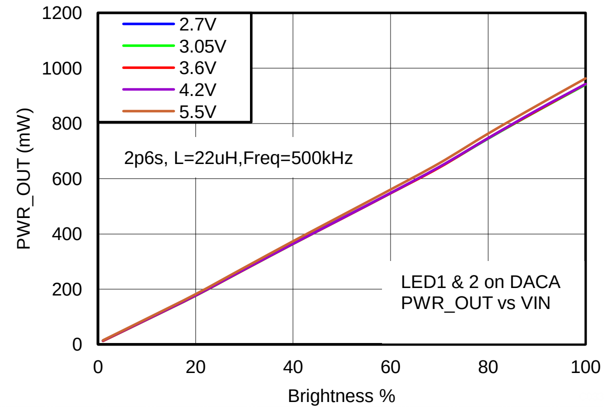
Typical Characteristics (continued)

T_A = 25°C, I_{LED} full-scale = 20 mA, unless specified otherwise.



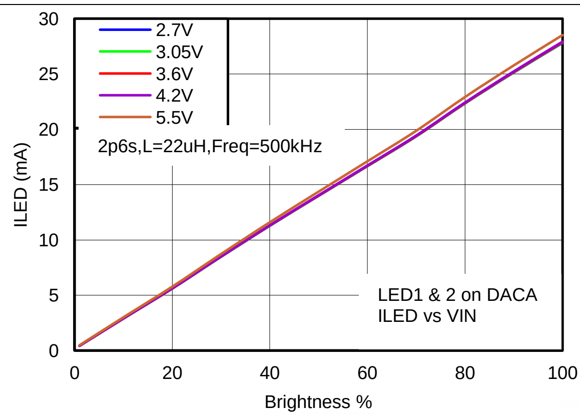
I_{LED} Full Scale = 28.5 mA   LED1 and LED2 on DACA
Frequency = 500 kHz   2p6s   L = 22 µH

Figure 61. I_{OUT} Across V_{IN}



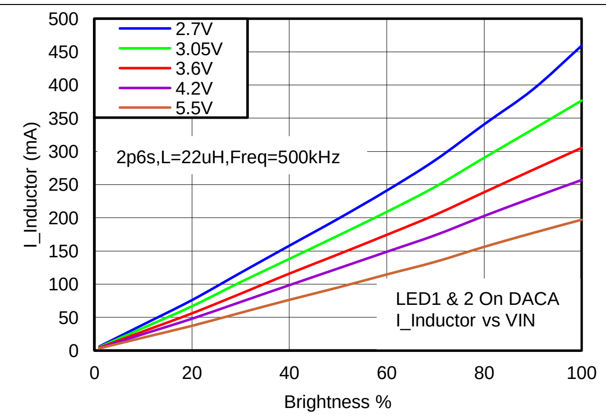
I_{LED} Full Scale = 28.5 mA   LED1 and LED2 on DACA
Frequency = 500 kHz   2p6s   L = 22 µH

Figure 62. PWR_I_{OUT} Across V_{IN}



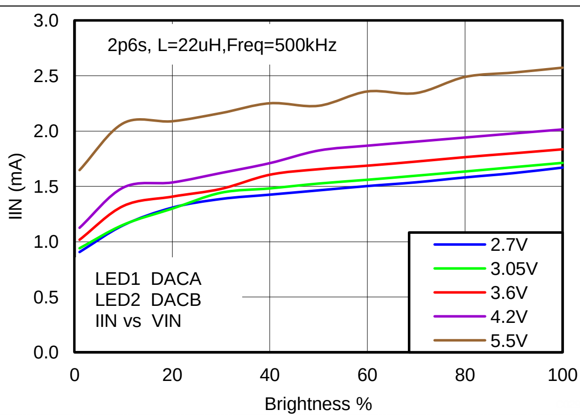
I_{LED} Full Scale = 28.5 mA   LED1 and LED2 on DACA
Frequency = 500 kHz   2p6s   L = 22 µH

Figure 63. I_{LED} Across V_{IN}



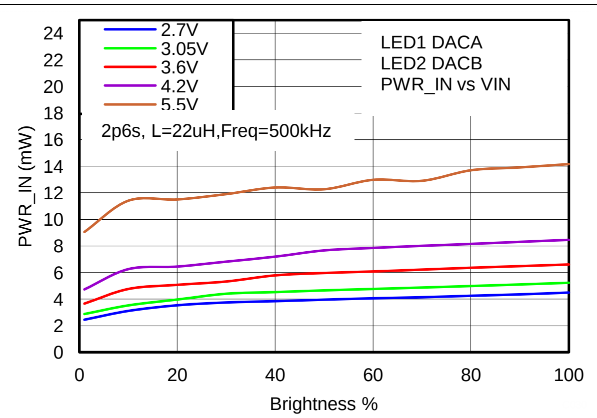
I_{LED} Full Scale = 28.5 mA   LED1 and LED2 on DACA
Frequency = 500 kHz   2p6s   L = 22 µH

Figure 64. $I_{\_INDUCTOR}$ Across V_{IN}



I_{LED} Full Scale = 28.5 mA   LED1 on DACA   2p6s
Frequency = 500 kHz   LED2 on DACB   L = 22 µH

Figure 65. I_{IN} Across V_{IN}

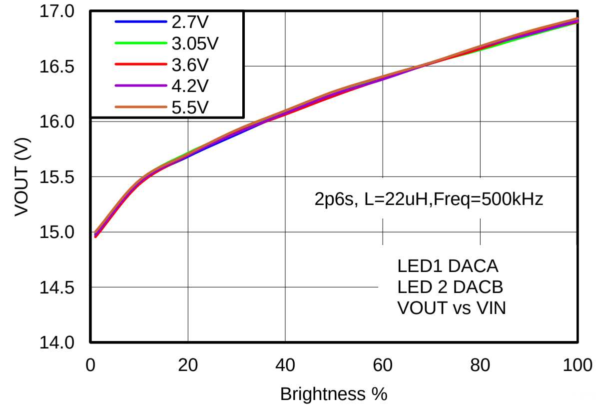


I_{LED} Full Scale = 28.5 mA   LED1 on DACA   2p6s
Frequency = 500 kHz   LED2 on DACB   L = 22 µH

Figure 66. PWR_I_{IN} Across V_{IN}

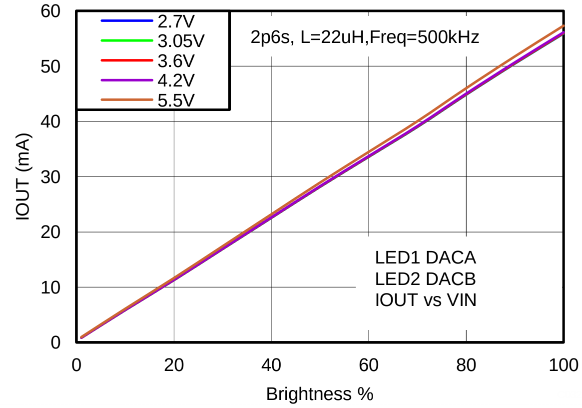
Typical Characteristics (continued)

T_A = 25°C, I_{LED} full-scale = 20 mA, unless specified otherwise.



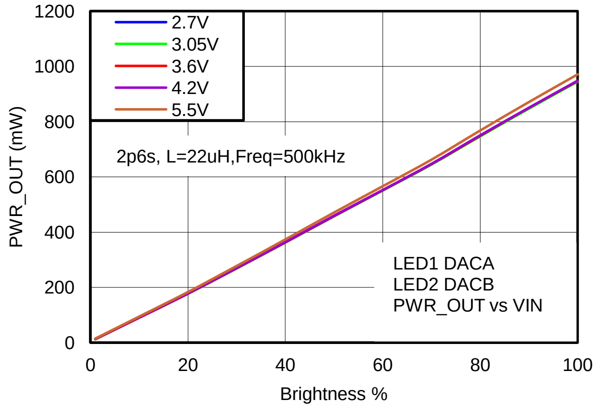
I_{LED} Full Scale = 28.5 mA | LED1 on DACA | 2p6s
Frequency = 500 kHz | LED2 on DACB | L = 22 µH

Figure 67. V_{OUT} Across V_{IN}



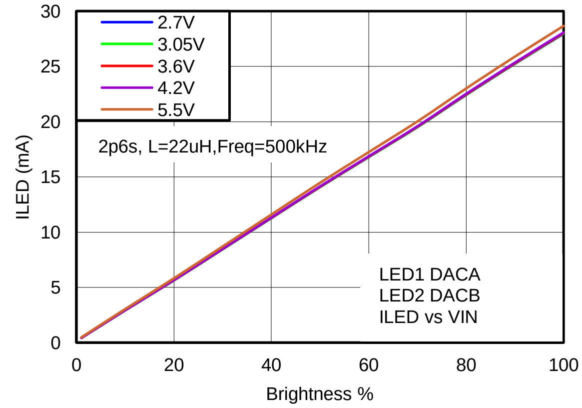
I_{LED} Full Scale = 28.5 mA | LED1 on DACA | 2p6s
Frequency = 500 kHz | LED2 on DACB | L = 22 µH

Figure 68. I_{OUT} Across V_{IN}



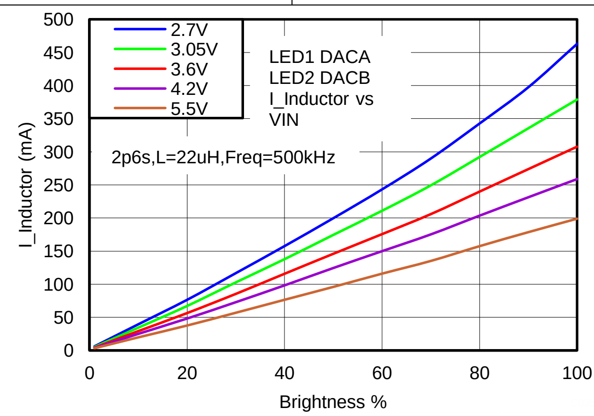
I_{LED} Full Scale = 28.5 mA | LED1 on DACA | 2p6s
Frequency = 500 kHz | LED2 on DACB | L = 22 µH

Figure 69. PWR_OUT Across V_{IN}



I_{LED} Full Scale = 28.5 mA | LED1 on DACA | 2p6s
Frequency = 500 kHz | LED2 on DACB | L = 22 µH

Figure 70. I_{LED} Across V_{IN}



I_{LED} Full Scale = 28.5 mA | LED1 on DACA | 2p6s
Frequency = 500 kHz | LED2 on DACB | L = 22 µH

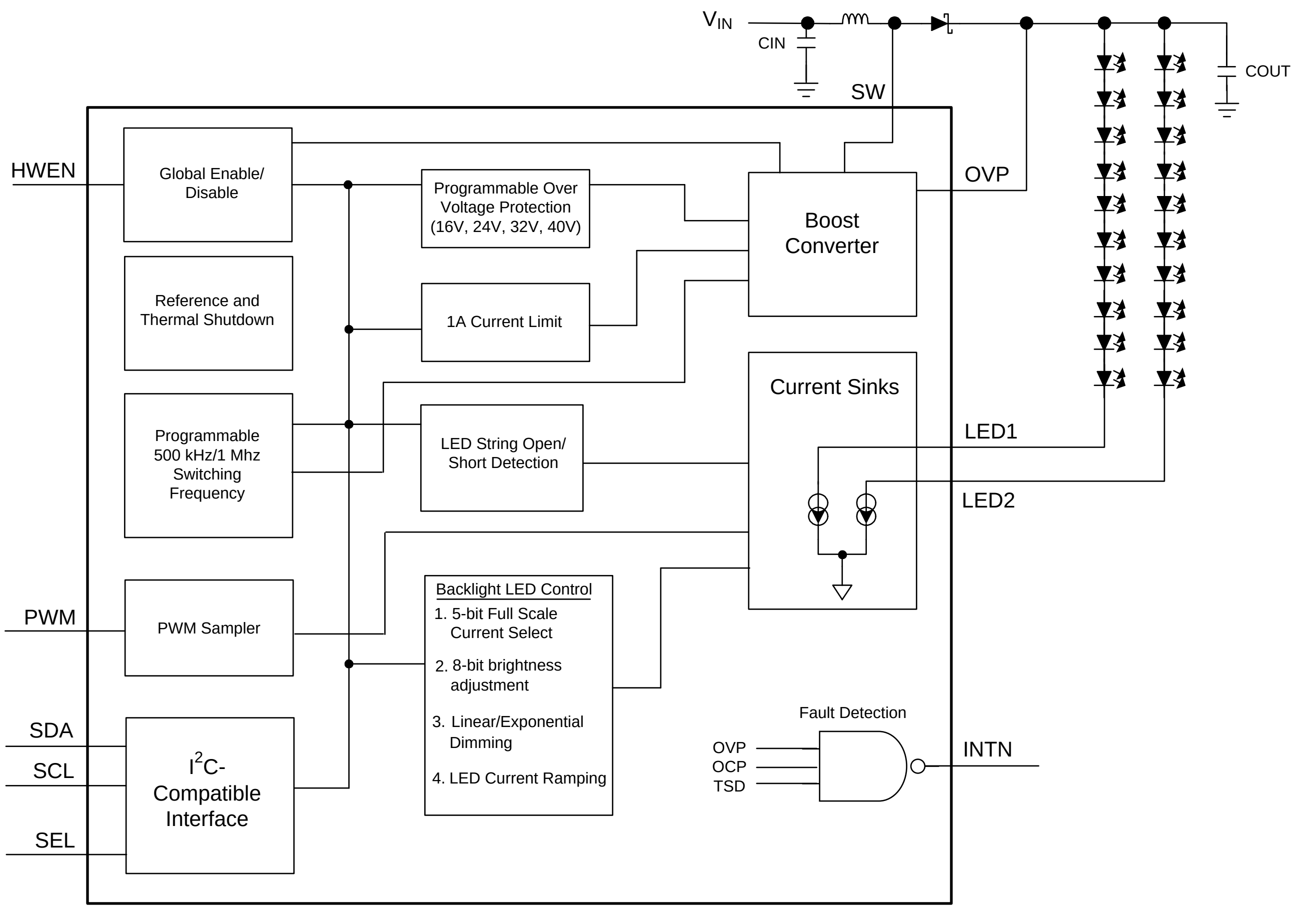
Figure 71. I_$_{INDUCTOR}$ Across V_{IN}

7 Detailed Description

7.1 Overview

The LM3630A provides the power for two high-voltage LED strings (up to 40 V at 28.5 mA each). The two high-voltage LED strings are powered from an integrated asynchronous boost converter. The device is programmable over an I^{2}C-compatible interface. Additional features include a PWM input for content adjustable brightness control, programmable switching frequency, and programmable overvoltage protection (OVP).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operation

7.3.1.1 Control Bank Mapping

Control of the LM3630A device current sinks is not done directly, but through the programming of Control Banks. The current sinks are then assigned to the programmed Control Bank (see Figure 72). Both current sinks can be assigned to Control Bank A or LED1 can use Control Bank A while LED2 uses Control Bank B. Assigning LED1 to Control Bank A and LED2 to Control Bank B allows for better LED current matching. Assigning each current sink to different control banks allows for each current sink to be programmed with a different current or have the PWM input control a specific current sink.

Feature Description (continued)

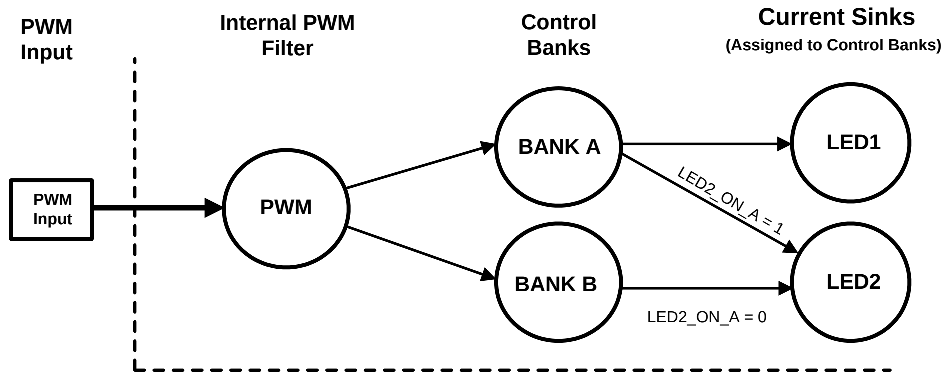


Figure 72. Control Diagram

Table 1. Bank Configuration Examples: Register Values

REGISTERS TO PROGRAM	ILED1 on A, ILED2 ON B WITH PWM DIMMING(1)	ILED1 AND ILED2 ON A WITH PWM DIMMING	ILED1 ON A WITH PWM ILED2 ON B NO PWM
Control	1EH linear or 06h exp	15h linear or 05h exp	1EH linear or 06h exp
Configuration	1Bh	09h	19h
Brightness A	used for A	used for both	used for A
Brightness B	used for B	not used	used for B (A and B do not have to be equal)

(1) LED current matching is specified using this configuration.

7.3.1.2 PWM Input Polaritiy

The PWM Input can be set for active high (default) or active low polarity. With active low polarity the LED current is a function of the negative duty cycle at PWM.

7.3.1.3 HWEN Input

HWEN is the global hardware enable to the LM3630A. HWEN must be pulled high to enable the device. HWEN is a high-impedance input so it cannot be left floating. When HWEN is pulled low the LM3630A is placed in shutdown and all the registers are reset to their default state.

7.3.1.4 SEL Input

SEL is the select pin for the serial bus device address. When this pin is connected to ground, the seven-bit device address is 36H. When this pin is tied to the VIN power rail, the device address is 38H.

7.3.1.5 INTN Output

The INTN pin is an open-drain active-low output signal which indicates detected faults. The signal asserts low when either OCP, OVP, or TSD is detected by the LED driver. The Interrupt Enable register must be set to connect these faults to the INTN pin.

7.3.1.6 Boost Converter

The high-voltage boost converter provides power for the two current sinks (ILED1 and ILED2). The boost circuit operates using a 10-µH to 22-µH inductor and a 1-µF output capacitor. The selectable 500-kHz or 1-MHz switching frequency allows for the use of small external components and provides for high boost converter efficiency. Both LED1 and LED2 feature an adaptive voltage regulation scheme where the feedback point (LED1 or LED2) is regulated to a minimum of 300 mV. When there are different voltage requirements in both high-voltage LED strings, because of different programmed voltages or string mismatch, the LM3630A regulates the feedback point of the highest voltage string to 300 mV and drop the excess voltage of the lower voltage string across the lower strings current sink.

7.3.1.7 Boost Switching Frequency Select

The LM3630A's boost converter can have a 500-kHz or 1-MHz switching frequency. For a 500-kHz switching frequency the inductor value must be between 10 µH and 22 µH. For the 1-MHz switching frequency the inductor can be between 10 µH and 22 µH. Additionally, there is a Frequency Shift bit which offsets the frequency approximately 10%. For the 500 kHz setting, shift = 0. The boost frequency is shifted to 560 kHz when Shift = 1. For the 1-MHz setting, Shift = 0. The boost frequency is shifted to 1120 kHz when shift = 1.

7.3.1.8 Adaptive Headroom

Reference Figure 73 and Figure 74 for the following description.

The adaptive headroom circuit controls the boost output voltage to provide the minimal headroom voltage necessary for the current sinks to provide the specified ILED current. The headroom voltage is fed back to the Error Amplifier to dynamically adjust the Boost output voltage. The error amplifier's reference voltage is adjusted as the brightness level is changed, because the currents sinks require less headroom at lower I_{LED} currents than at higher I_{LED} currents. Note that the VHR Min block dynamically selects the LED string that requires the higher boost voltage to maintain the I_{LED} current; this string has the lower headroom voltage. In Figure 74 this is LED string 2. The headroom voltage on LED string 1 is higher, but this is due to LED string 2 have an overall higher forward voltage than LED string 1. LED strings that have closely matched forward voltages have closely matched headroom voltages and better overall efficiency.

In a single string LED configuration the Feedback enable must be enabled for only that string (LED1 or LED2). The adaptive headroom circuit is control by that single string. In a two string LED configuration the Feedback enable must be enabled for both strings (LED1 and LED2). The VHR Min block then dynamically selects the LED string to control the adaptive headroom circuit.

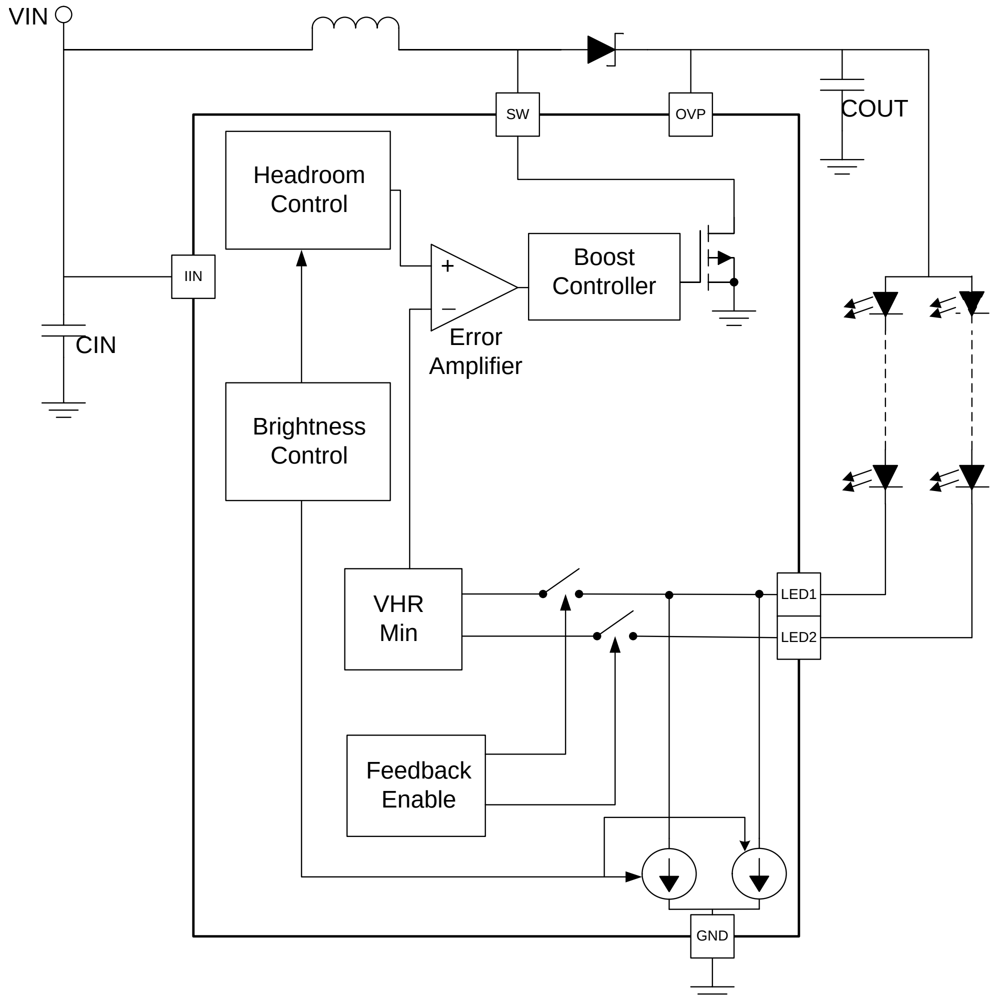


Figure 73. Adaptive Headroom Block Diagram

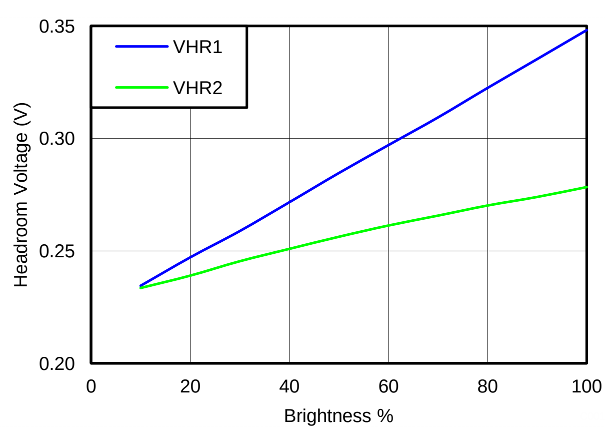


Figure 74. Typical Headroom Voltage Curve

7.3.1.9 Current Sinks

LED1 and LED2 control the current up to a 40-V LED string voltage. Each current sink has 5-bit full-scale current programmability and 8-bit brightness control. Either current sink has its current set through a dedicated brightness register and can additionally be controlled via the PWM input.

7.3.1.10 Current String Biasing

Each current string can be powered from the LM3630A device's boost or from an external source. When powered from an external source the feedback input for either current sink can be disabled in the Configuration Register so it no longer controls the boost output voltage.

7.3.1.11 Full-Scale LED Current

The LM3630A device's full-scale current is programmable with 32 different full-scale levels. The full-scale current is the LED current in the control bank when the brightness code is at max code (0xFF). The 5-bit full-scale current vs code is given by Equation 1:

$$I_{LED\_FULLSCALE} = 5\text{ mA} + \text{Code} \times 0.75\text{ mA} \tag{1}$$

With a maximum full-scale current of 28.5 mA.

7.3.1.12 Brightness Register

Each control bank has its own 8-bit brightness register. The brightness register code and the full-scale current setting determine the LED current depending on the programmed mapping mode.

7.3.1.13 Exponential Mapping

In exponential mapping mode the brightness code to backlight current transfer function is given by Equation 2:

$$I_{LED} = I_{LED\_FULLSCALE} \times 0.85^{\left(44 - \frac{\text{Code} + 1}{5.8181818}\right)} \times D_{PWM}$$

where
- $I_{LED\_FULLSCALE}$ is the full-scale LED current setting
- Code is the backlight code in the brightness register
- DPWM is the PWM input duty cycle (2)

Figure 75 and Figure 76 show the approximate backlight code to LED current response using exponential mapping mode. Figure 75 shows the response with a linear Y axis, and Figure 76 shows the response with a logarithmic Y axis. In exponential mapping mode the current ramp (either up or down) appears to the human eye as a more uniform transition then the linear ramp. This is due to the logarithmic response of the eye.

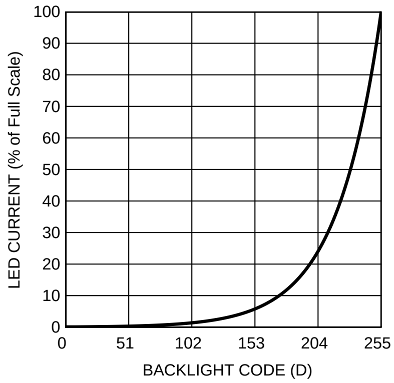


Figure 75. Exponential Mapping Mode (Linear Scale)

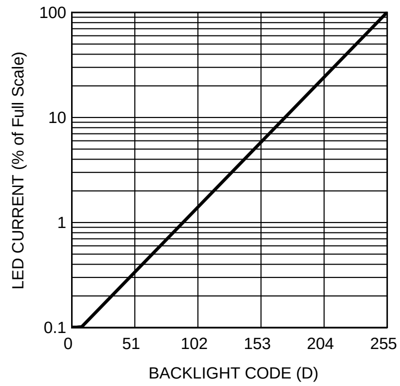


Figure 76. Exponential Mapping Mode (Log Scale)

7.3.1.14 Linear Mapping

In linear mapping mode the brightness code to backlight current has a linear relationship and follows Equation 3:

$$I_{LED} = I_{LED\_FULLSCALE} \times \frac{1}{255} \times Code \times D_{PWM} \tag{3}$$

where

- $I_{LED\_FULLSCALE}$ is the full scale LED current setting
- Code is the backlight code in the brightness register
- DPWM is the PWM input duty cycle

Figure 77 shows the backlight code-to-LED current response using linear-mapping mode. The Configuration Register must be set to enable linear mapping.

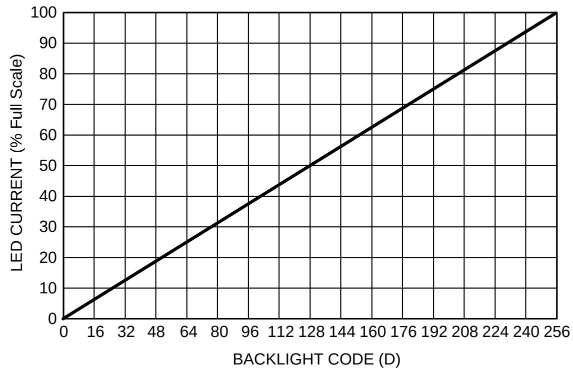


Figure 77. Linear Mapping Mode

7.3.2 Test Features

The LM3630A contains an LED open, an LED short, and overvoltage manufacturing fault detection. This fault detection is designed to be used during the manufacturing process only and not normal operation. These faults do not set the INTN pin.

7.3.2.1 Open LED String (LED1 And LED2)

An open LED string is detected when the voltage at the input to either LED1 or LED2 has fallen below 200 mV, **and** the boost output voltage has hit the OVP threshold. This test assumes that the LED string that is being detected for an open is being powered from the boost output (Feedback Enabled). For an LED string not connected to the boost output, and connected to another voltage source, the boost output would not trigger the OVP flag. In this case an open LED string would not be detected.

7.3.2.2 Shorted LED String

The LM3630A features an LED short fault flag indicating if either of the LED strings have experienced a short. There are two methods that can trigger a short in the LED strings:

1. An LED current sink with feedback enabled, and the difference between OVP input and the LED current sink input voltage goes below 1 V.
2. An LED current sink is configured with feedback disabled (not powered from the boost output) and the difference between V_{IN} and the LED current sink input voltage goes below 1 V.

7.3.2.3 Overvoltage Protection (Manufacturing Fault Detection and Shutdown)

The LM3630A provides an overvoltage Protection (OVP) mechanism specifically for manufacturing test where a display may not be connected to the device. The OVP threshold on the LM3630A has 4 different programmable options (16 V, 24 V, 32 V, and 40 V). The manufacturing protection is enabled in the Fault Status register bit 0. When enabled, this feature causes the boost converter to shutdown anytime the selected OVP threshold is exceeded. The OVP_fault bit in the Fault Status register is set to one. The boost converter does not resume operation until the LM3630A is reset with either a write to the Software Reset bit in the Software Reset register or a cycling of the HWEN pin. The reset clears the fault.

7.3.3 Fault Flags/Protection Features

The Interrupt Status register contains the status of the protection circuits of the LM3630A. The corresponding bits are set to one if an OVP, OCP, or TSD event occurs. These faults do set the INTN pin when the corresponding bit is set in the Interrupt Enable register.

7.3.3.1 Overvoltage Protection (Inductive Boost Operation)

The overvoltage protection threshold (OVP) on the LM3630A has 4 different programmable options (16 V, 24 V, 32 V, and 40 V). OVP protects the device and associated circuitry from high voltages in the event the feedback enabled LED string becomes open. During normal operation, the LM3630A device's inductive boost converter boosts the output up so as to maintain at least 300 mV at the active current sink inputs. When a high-voltage LED string becomes open the feedback mechanism is broken, and the boost converterinadvertently over boosts the output. When the output voltage reaches the OVP threshold the boost converter stops switching, thus allowing the output node to discharge. When the output discharges to V_{OVP} – 1 V the boost converter begins switching again. The OVP sense is at the OVP pin, so this pin must be connected directly to the inductive boost output capacitor's positive terminal.

For current sinks that have feedback disabled the over voltage sense mechanism is not in place to protect from potential over-voltage conditions. In this situation the application must ensure that the voltage at LED1 or LED2 doesn't exceed 40 V.

The default setting for OVP is set at 24 V. For applications that require higher than 24 V at the boost output the OVP threshold has to be programmed to a higher level at power up.

7.3.3.2 Current Limit

The switch current limit for the LM3630A device's inductive boost is set at 1 A. When the current through the NFET switch hits this over current protection threshold (OCP) the device turns the NFET off and the energy of the inductor is discharged into the output capacitor. Switching is then resumed at the next cycle. The current limit protection circuitry can operate continuously each switch cycle. The result is that during high output power conditions the device can continuously run in current limit. Under these conditions the device inductive boost converter stops regulating the headroom voltage across the high voltage current sinks. This results in a drop in the LED current.

7.3.3.3 Thermal Shutdown

The LM3630A contains thermal shutdown protection. In the event the die temperature reaches 140°C, the boost power supply and current sinks shut down until the die temperature drops to typically 125°C.

7.3.4 Initialization Timing

7.3.4.1 Initialization Timing With HWEN Tied to V_{IN}

If the HWEN input is tied to V_{IN}, then the t_{WAIT} time starts when V_{IN} crosses 2.5 V as shown in Figure 78. The initial I^2C transaction can occur after the t_{WAIT} time expires. Any I^2C transaction during the t_{WAIT} period are NAK'ed.

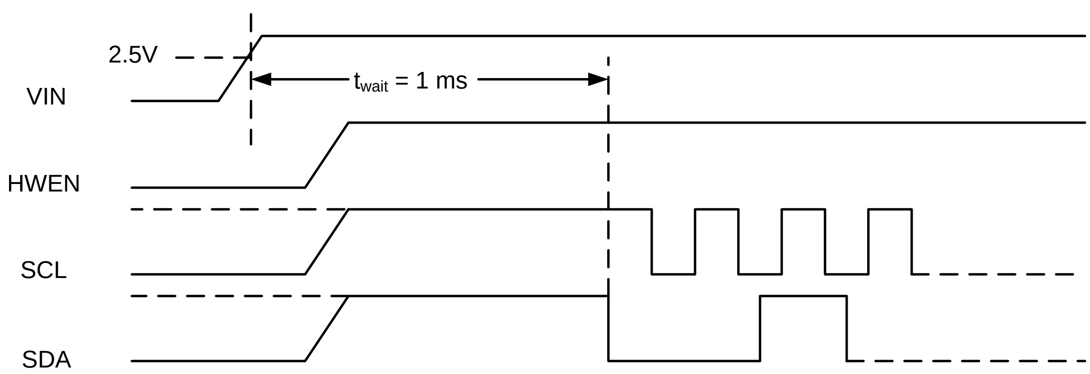


Figure 78. Initialization Timing With HWEN Is Tied to V_{IN}

7.3.4.2 Initialization Timing With HWEN Driven by GPIO

If the HWEN input is driven by a GPIO then the t_{WAIT}time starts when HWEW crosses 1.2 V as shown in Figure 79. The initial I^2C transaction can occur after the t_{WAIT} time expires. Any I^2C transaction during the t_{WAIT} period are NAK'ed.

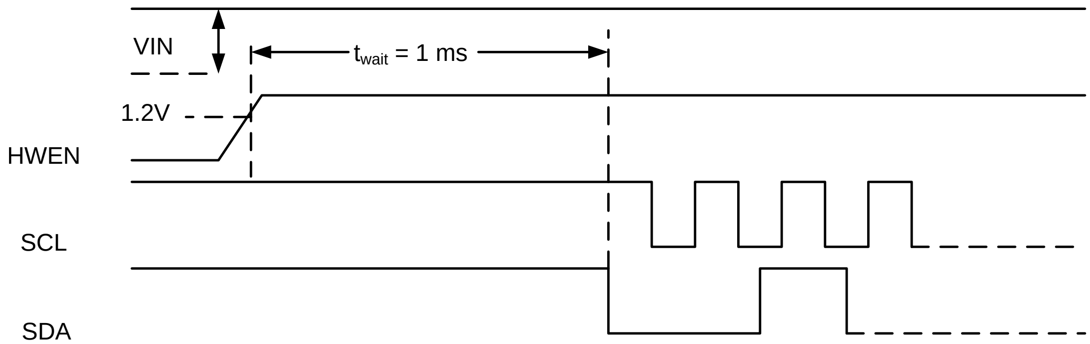


Figure 79. Initialization Timing With HWEN Driven by a GPIO

7.3.4.3 Initialization After Software Reset

The time between the I^2C transaction that issues the software reset, and the subsequent I^2C transaction (that is, to configure the LM3630A) must be at greater or equal to the t_{WAIT} period of 1 ms. Any I^2C transaction during the t_{WAIT} period are NAK'ed.

7.4 Device Functional Modes

7.4.1 LED Current Ramping

7.4.1.1 Start-Up/Shutdown Ramp

The LED current turn on time from 0 to the initial LED current set-point is programmable. Similarly, the LED current shutdown time to 0 is programmable. Both the startup and shutdown times are independently programmable with 8 different levels. The start-up times are independently programmable from the shutdown times, but not independently programmable for each Control bank. For example, programming a start-up or shutdown time, programs the same ramp time for each control bank. The start-up time is used when the device is first enabled to a non-zero brightness value. The shutdown time is used when the brightness value is programmed to zero. If HWEN is used to disable the device, the action is immediate and the Shutdown time is not used. The zero code does take a small amount of time which is approximately 0.5 ms.

Table 2. Start-Up/Shutdown Times

CODE	START-UP TIME	SHUTDOWN TIME
000	4 ms	0
001	261 ms	261 ms
010	522 ms	522 ms
011	1.045 s	1.045 s
100	2.091 s	2.091 s
101	4.182 s	4.182 s
110	8.364 s	8.364 s
111	16.73 s	16.73 s

7.4.1.2 Run-Time Ramp

Current ramping from one brightness level to the next is programmable. There are 8 different ramp up times and 8 different ramp down times. The ramp up time is independently programmable from the ramp down time, but not independently programmable for each Control Bank. For example, programming a ramp up time or a ramp down time programs the same ramp time for each control bank. The run time ramps are used whenever the device is enabled with a non-zero brightness value and a new non-zero brightness value is written.

Table 3. LED Current Run Ramp Times

CODE	RAMP-UP TIME	RAMP-DOWN TIME
000	0	0
001	261 ms	261 ms
010	522 ms	522 ms
011	1.045s	1.045s
100	2.091s	2.091s
101	4.182s	4.182s
110	8.364s	8.364s
111	16.73s	16.73s

7.4.2 PWM Operation

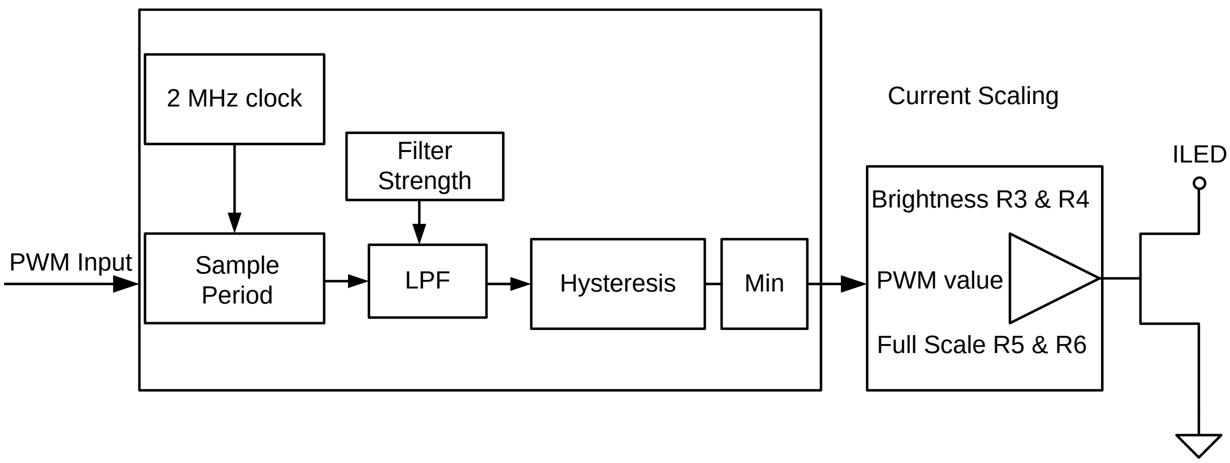


Figure 80. PWM Sampler

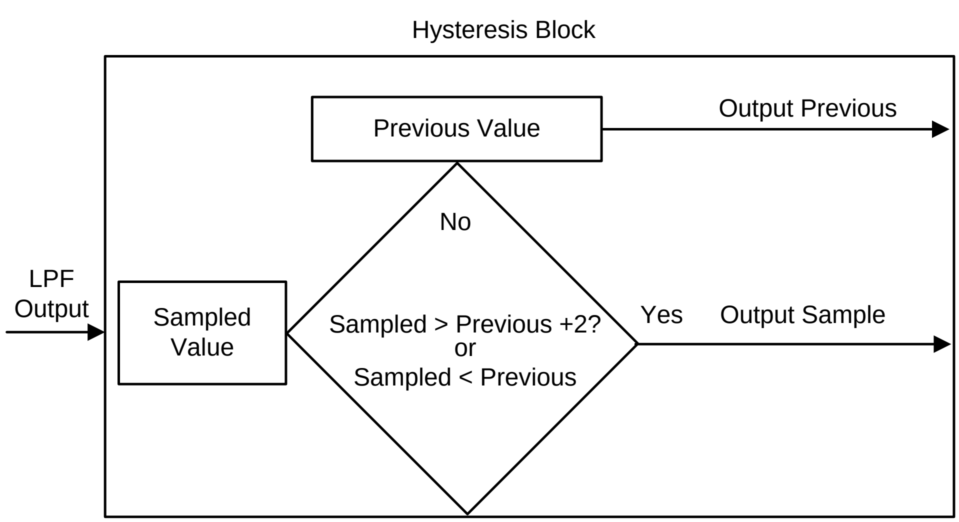


Figure 81. Hysteresis Block (Details)

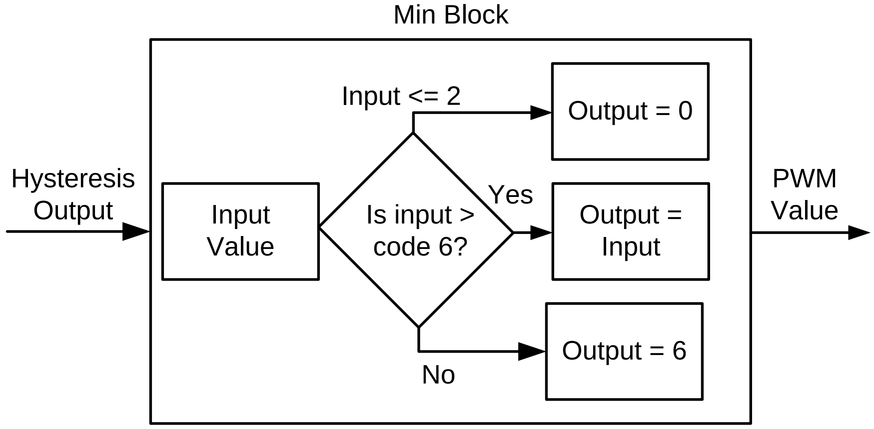


Figure 82. Min Block (Details)

7.4.2.1 PWM Input

The PWM input can be assigned to any control bank. When assigned to a control bank, the programmed current in the control bank also becomes a function of the duty cycle at the PWM input. The PWM input is sampled by a digital circuit which outputs a brightness code that is equivalent to the PWM input duty cycle. The resultant brightness value is a combination of the maximum current setting, the brightness registers, and the equivalent PWM brightness code.

7.4.2.2 PWM Input Frequency

The specified input frequency of the PWM signal is 10 kHz to 80 kHz. The recommended frequency is 30 kHz or greater. The PWM input sampler operates beyond those frequency limits. Performance changes based on the input frequency used. Using frequencies outside the specified range is not recommended. Lower PWM input frequency increases the likelihood that the output of the sampler may change and that a single brightness step may be visible on the screen. This may be visible at low brightness because the step change is large relative to the output level.

7.4.2.3 Recommended Settings

For best performance of the PWM sampler it is recommended to have a PWM input frequency of at least 30 kHz. The Filter Strength (register 50h) must be set to 03h. The Hysteresis 1 bit must be set in register 05h to 1 when setting the maximum current for bank A. For example if max current is 20 mA, register 05h is set to 14h, change that to 94h for 1 bit hysteresis and a smooth min-to-max brightness transition.

7.4.2.4 Adjustments to PWM Sampler

The digital sampler has controls for hysteresis and minimum output brightness which allow the optimization of sampler output. The default hysteresis mode of the PWM sampler requires detecting a two code change in the input to increase brightness. Reducing the hysteresis to change on 1 code allows a smoother brightness transition when the brightness control is swept across the screen in a system. The filter strength bits affect the speed of the output transitions from the PWM sampler. A lower bound to the brightness is enabled by default which limits the minimum output of the PWM sampler to an equivalent code of 6 when the LEDs are turned on. A detected code of 1 is forced to off. A minimum 2% PWM input duty cycle is recommended. Input duty cycles of 1% or less causes delayed off-to-on transitions.

7.4.2.4.1 Filter Strength, Register 50h Bits [1:0]

- Filter Strength controls the amount of sampling cycles that are fed back to the PWM input sampler. A filter strength of 00b allows the output of the PWM sampler to change on every Sample Period. A filter strength of 01b allows the output of the PWM sampler to change every two Sample Periods. A filter strength of 10b allows the output of the PWM sampler to change every four Sample Periods. A filter strength of 11b allows the output of the PWM sampler to change every eight Sample Periods.
- he effect of setting this value to 11b forces the output of the PWM sampler to change less frequently then lower values. The benefit is this reduces the appearance of flicker because the output is slower to change.

The negative is that the output is slower to change.

7.4.2.4.2 Hysteresis 1 Bit, Register 05h, Bit 7

- The default setting for the LM3630A has Bit 7 of register 05h is 0b. This requires the detection of a PWM input change that is at least 3 equivalent codes higher than the present code. If this bit is set to 1b, the hysteresis is turned off and the PWM sampler output is allowed to change by 2 code.
- Setting this bit to 1b turns off the 2 code requirement for the PWM sampler output to change. The benefit is that the output change is smoother. The negative is that there may be some PWM input value where the output could change by one code and it might appear as flicker.

7.4.2.4.3 Lower Bound Disable, Register 05h, Bit 6

- The default setting for the LM3630A has Bit 6 of register 05h is 0b. This turns on the lower bound where the minimum output value of the PWM sampler is an equivalent code of 6. If the PWM sampler detects an equivalent code of 0 or 1, the output is 0, and the LEDs are off. If the PWM sampler detects an equivalent code of 2 through 6, a current equal to code 6 is output. Detection of any higher code outputs that code conforming to the rules of hysteresis above.
- Setting Bit 6 of register 05h to 1b can be used to allow the output to be below an equivalent code 6. The output of the PWM sampler matches the input pulse width conforming to the rules of Hysteresis and equivalent codes 1, 2, 3, 4, and 5 are also allowed. The benefit is the output is allowed to go dimmer than in the default mode. The negative is at the low codes of 1 and 2, the LEDs may not turn on or the LEDs may appear to flicker.
- Disabling the Lower Bound (05h Bit 6 = 1b) allows the minimum duty cycle to be detected at 0.35% PWM input duty cycle. At 30-kHz PWM input frequency, the minimum pulse width required to turn on the LEDs is 0.39% × 33 µS = 129 ns. There is no specified tolerance to this value.

7.4.2.5 Minimum T_{ON} Pulse Width

The minimum T_{ON} pulse width required to produce a non-zero output is dependent upon the LM3630A settings. The default setting of the LM3630A requires a minimum of 0.78% duty cycle for the output to be turned on. Because the lower bound feature is enabled, a value of 0.78% (equivalent brightness code 2) up to 2.35% (equivalent brightness code 6) all produce an output equivalent to brightness code 6. At 30-kHz PWM input frequency, the minimum pulse width required to turn on the LEDs is 0.78% × 33 µS = 260 ns.

Because of the hysteresis on the PWM input, this pulse width may not be sufficient to turn on the LEDs. It is recommended that a minimum pulse width of 2% be used. 2% × 33 µS = 660 ns at 30 kHz input frequency.

Disabling the lower bound as described allows a smaller minimum pulse width.

7.5 Programming

7.5.1 I²C-Compatible Interface

7.5.1.1 Data Validity

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when SCL is LOW.

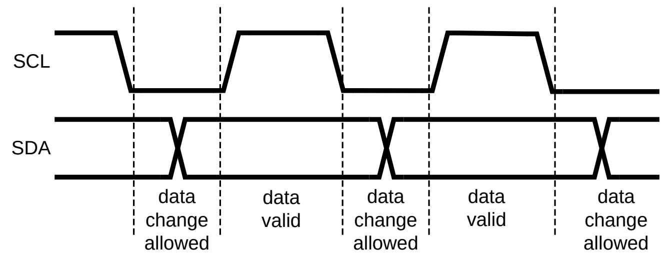


Figure 83. Data Validity Diagram

A pullup resistor between the VIO line of the controller and SDA must be greater than [(V_{IO} – V_{OL}) / 3 mA] to meet the V_{OL} requirement on SDA. Using a larger pullup resistor results in lower switching current with slower edges, while using a smaller pullup results in higher switching currents with faster edges.

7.5.1.2 Start and Stop Conditions

START and STOP conditions classify the beginning and the end of the I²C session. A START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. A STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP conditions. The I²C bus is considered to be busy after a START condition and free after a STOP condition. During data transmission, the I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.

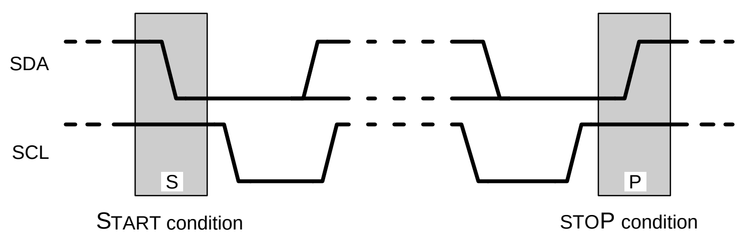


Figure 84. Start and Stop Conditions

7.5.1.3 Transferring Data

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the acknowledge clock pulse. The LM3630A pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The LM3630A generates an acknowledge after each byte is received.

After the START condition, the I²C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LM3630A address is 36h. For the eighth bit, a “0” indicates a WRITE and a “1” indicates a READ. The second byte selects the register to which the data is written. The third byte contains data to write to the selected register.

Programming (continued)

I2C Compatible Address

MSB … LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	1	0	1	1	0	R/W

Figure 85. I²C-Compatible Chip Address (0x36), SEL = 0

I2C Compatible Address

MSB … LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	1	1	0	0	0	R/W

Figure 86. I²C-Compatible Chip Address (0x38), SEL = 1

7.6 Register Maps

7.6.1 LM3630A I²C Register Map

This table summarizes LM3630A I²C-compatible register usage and shows default register bit values after reset, as programmed by the factory. The following sub-sections provide additional details on the use of individual registers. Register bits which are blank in the following tables are considered undefined. Undefined bits should be ignored on reads and written as zero.

SLAVE ADDRESS [0x36h for SEL = 0, 0x38h for SEL = 1]			
BASE REGISTERS			
REGISTER NAME	ADDRESS	TYPE	DEFAULT RESET VALUES
Control	0x00	R/W	0xC0
Configuration	0x01	R/W	0x18
Boost Control	0x02	R/W	0x38
Brightness A	0x03	R/W	0x00
Brightness B	0x04	R/W	0x00
Current A	0x05	R/W	0x1F
Current B	0x06	R/W	0x1F
On/Off Ramp	0x07	R/W	0x00
Run Ramp	0x08	R/W	0x00
Interrupt Status	0x09	R/W	0x00
Interrupt Enable	0x0A	R/W	0x00
Fault Status	0x0B	R/W	0x00
Software Reset	0x0F	R/W	0x00
PWM Out Low	0x12	Read	0x00
PWM Out High	0x13	Read	0x00
Revision	0x1F	Read	0x02
Filter Strength	0x50	R/W	0x00

7.6.2 Register Descriptions

Table 4. Control (Offset = 0x00, Default = 0xC0)

Register Bits							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SLEEP_CMD	SLEEP_ STATUS		LINEAR_A	LINEAR_B	LED_A_EN	LED_B_EN	LED2_ON_A

Name	Bit	Access	Description
SLEEP_CMD	7	R/W	The device is put into sleep mode when set to '1'
SLEEP_STATUS	6	Read	Reflects the sleep mode status. A '1' indicates the part is in sleep mode.
			Used to determine when part has entered or exited sleep mode after writing the SLEEP_CMD bit.
	5	Read	
LINEAR_A	4	R/W	Enables the linear output mode for Bank A when set to '1'.
LINEAR_B	3	R/W	Enables the linear output mode for Bank B when set to '1'.
LED_EN_A	2	R/W	Enables the LED A output
LED_EN_B	1	R/W	Enables the LED B output
LED2_ON_A	0	R/W	Connect the LED2 output to Bank A Control

Table 5. Configuration (Offset = 0x01, Default = 0x18)

Register Bits							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
			FB_EN_B	FB_EN_A	PWM_LOW	PWM_EN-B	PWM_EN_A

Name	Bit	Access	Description
	7	Read	
	6	Read	
	5	Read	
FB_EN_B	4	R/W	Enable Feedback on Bank B
FB_EN_A	3	R/W	Enable Feedback on Bank A
PWM_LOW	2	R/W	Sets the PWM to active low
PWM_EN_B	1	R/W	Enables the PWM for Bank B
PWM_EN_A	0	R/W	Enables the PWM for Bank A

Table 6. Boost Control (Offset = 0x02, Default = 0x38)

Register Bits							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	BOOST_OVP[1]	BOOST_OVP[0]	BOOST_OCP[1]	BOOST_OCP[0]	SLOW_STAR T	SHIFT	FMODE

Name	Bit	Access	Description
	7	Read	
BOOST_OVP	6:5	R/W	Selects the voltage limit for over-voltage protection: 00 = 16 V 01 = 24 V 10 = 32 V 11 = 4 0V
BOOST_OCP	4:3	R/W	Selects the current limit for over-current protection: 00 = 600 mA 01 = 800 mA 10 = 1 A 11 = 1.2 A
SLOW_START	2	R/W	Slows the boost output transition
SHIFT	1	R/W	Enables the alternate oscillator frequencies: For FMODE = 0: SHIFT = 0F = 500 kHz; SHIFT 1F = 560 kHz For FMODE = 1: SHIFT = 0F = 1 MHz; SHIFT 1F = 1120 MHz

Table 6. Boost Control (Offset = 0x02, Default = 0x38) (continued)

Register Bits							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FMODE	0	R/W	Selects the boost frequency: 0 = 500 kHz, 1 = 1MHz				

Table 7. Brightness A (Offset = 0x03, Default = 0x00)(1)

Register Bits							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
A[7]	A[6]	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]
Name	**Bit**	**Access**	**Description**				
A	[7:0]	R/W	Sets the 8-bit brightness value for outputs connected to Bank A. Minimum brightness setting is code 04h.				

(1) These registers are not update if the device is in Sleep Mode (Control: SLEEP_STATUS = 1).

Table 8. Brightness B (Offset = 0x04, Default = 0x00)(1)

Register Bits							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
Name	**Bit**	**Access**	**Description**				
B	[7:0]	R/W	Sets the 8-bit brightness value for outputs connected to Bank B. Minimum brightness setting is code 04h.				

(1) These registers are not update if the device is in Sleep Mode (Control: SLEEP_STATUS = 1).

Table 9. Current A (Offset = 0x05, Default 0x1F)

Register Bits							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Hysteresis	Lower Bound		A[4]	A[3]	A[2]	A[1]	A[0]
Name	**Bit**	**Access**	**Description**				
Hysteresis	7	R/W	Determines the hysteresis of the PWM Sampler. Clearing this bit, the PWM sampler changes its output upon detecting at least 3 equivalent code changes on the PWM input. Setting this bit, the PWM sampler changes its output upon detecting 2 equivalent code changes on the PWM input.				
Lower Bound	6	R/W	Determines the lower bound of the PWM Sampler. Clearing this bit, the PWM sampler outputs code 6 when it detects equivalent codes 2 thru 6; and code 0 when it detects equivalent codes 0 thru 1. Setting this bit, the PWM sampler can output codes below 6, based upon the Hysteresis setting and equivalent code sampled from the input PWM.				
	5	Read					
A	[4:0]	R/W	Sets the 5-bit full-scale current for outputs connected to Bank A.				

Table 10. Current B (Offset = 0x06, Default = 0x1F)

Register Bits							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
			B[4]	B[3]	B[2]	B[1]	B[0]
Name	**Bit**	**Access**	**Description**				
B	[4:0]	R/W	Sets the 5-bit full-scale current for outputs connected to Bank B				

Table 11. On/Off Ramp (Offset = 0x07, Default 0x00)

Register Bits							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
		T_START[2]	T_START[1]	T_START[0]	T_SHUT[2]	T_SHUT[1]	T_SHUT[0]
Name	**Bit**	**Access**	**Description**				
	7	Read					
	6	Read					
T_START	[5:3]	R/W	Ramp time for startup events.				
T_SHUT	[2:0]	R/W	Ramp time for shutdown events.				

Code	Start-Up Time	Shutdown Time
000	4 ms	0*
001	261 ms	261 ms
010	522 ms	522 ms
011	1.045s	1.045 s
100	2.091s	2.091 s
101	4.182s	4.182 s
110	8.364s	8.364 s
111	16.73s	16.73 s

*Code 0 results in approximately 0.5 ms ramp time.

Table 12. Run Ramp (Offset = 0x08, Default = 0x00)

Register Bits							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
		T_UP[2]	T_UP[1]	T_UP[0]	T_DOWN[2]	T_DOWN[1]	T_DOWN[0]
Name	**Bit**	**Access**	**Description**				
	7	Read					
	6	Read					
T_UP	[5:3]	R/W	Time for ramp-up events				
T_DOWN	[2:0]	R/W	Time for ramp-down events				

Code	Ramp-Up Time	Ramp-down Time
000	0*	0*
001	261 ms	261 ms
010	522 ms	522 ms
011	1.045s	1.045 s
100	2.091s	2.091 s
101	4.182s	4.182 s
110	8.364s	8.364 s
111	16.73s	16.73 s

*Code 0 results in approximately 0.5 ms ramp time.

Table 13. Interrupt Status (Offset = 0x09, Default = 0x00)

Register Bits							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
					OCP	OVP	TSD

Name	Bit	Access	Description
	7	Read	
	6	Read	
	5	Read	
	4	Read	
	3	Read	
OCP	2	R/W	An overcurrent condition occurred.
OVP	1	R/W	An overvoltage condition occurred.
TSD	0	R/W	A thermal shutdown event occurred.

The interrupt status register is cleared upon a read of the register. If the condition that caused the interrupt is still present, then the bit is set to one again and another interrupt is signaled on the INTN output pin. The interrupt status register is not cleared if the device is in sleep mode (Control: SLEEP_STATUS = 1). To disconnect the interrupt condition from the INTN pin during sleep mode, disable the fault connection in the Interrupt Enable register. An interrupt condition sets the status bit and causes an event on the INTN pin only if the corresponding bit in the Interrupt Enable register is one and the Global Enable bit is also one.

Table 14. Interrupt Enable (Offset = 0x0A, Default = 0x00)

Register Bits							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
					OCP	OVP	TSD

Name	Bit	Access	Description
GLOBAL	7	R/W	Set to '1' to enable interrupts to drive the INTN pin.
	6	Read	
	5	Read	
	4	Read	
	3	Read	
OCP	2	R/W	Set to '1' to enable the over-current condition interrupt.
OVP	1	R/W	Set to '1' to enable the over-voltage condition interrupt.
TSD	0	R/W	Set to '1' to enable the thermal shutdown interrupt.

Table 15. Fault Status (Offset = 0x0B, Default = 0x00)

Register Bits							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
		OPEN	LED2_SHORT	LED1_SHORT	SHORT_EN	OVP_FAULT	OVP_F_EN

Name	Bit	Access	Description
	7	Read	.
	6	Read	
OPEN	5	R/W	An open circuit was detected on one of the LED strings.
LED2_SHORT	4	R/W	A short was detected on LED string 2.
LED1_SHORT	3	R/W	A short was detected on LED string 1.
SHORT_EN	2	R/W	Set to '1' to enable short test.
OVP_FAULT	1	R/W	An OVP occurred in manufacturing test.
OVP_F_EN	0	R/W	Set to '1' to enable OVP manufacturing test.

Table 16. Software Reset (Offset = 0x0F, Default = 0x00)

Register Bits							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
							SW_RESET

Name	Bit	Access	Description
	7	Read	.
	6	Read	
	5	Read	
	4	Read	
	3	Read	
	2	Read	
	1	Read	
SW_RESET	0	R/W	Set to '1' to reset the device. This is a full reset which clears the registers, executes a power-on reset, and reads the EPROM configuration.

Table 17. PWM_OUT Low (Offset = 0x12, Default 0x00)

Register Bits							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWM_OUT[7]	PWM_OUT[6]	PWM_OUT[5]	PWM_OUT[4]	PWM_OUT[3]	PWM_OUT[2]	PWM_OUT[1]	PWM_OUT[0]

Table 18. PWM_OUT High (Offset = 0x13, Default 0x00)

Register Bits							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
							PWM_OUT[8]

Name	Bit	Access	Description
PWM_OUT	[7:0]	R/W	The value of the PWM detector. Maximum value is 256 or 100h. If PWM_OUT[7:0] is non-zero PWM_OUT[8] is zero.

Table 19. Revision (Offset = 0x1F, Default = 0x02)

Register Bits							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REV[7]	REV[6]	REV[5]	REV[4]	REV[3]	REV[2]	REV[1]	REV[0]

Name	Bit	Access	Description
REV	[7:0]	R/W	Revision value

Table 20. Filter Strength (Offset = 0x50, Default = 0x00)

Register Bits							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
						FLTR_STR[1]	FLTR_STR[0]

Name	Bit	Access	Description
FLTR_STR	[1:0]	R/W	Filter Strength

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM3630A is a dual-channel backlight driver. The device has 5-bit full-scale current programmability (5 mA to 30 mA) and for every full-scale current there is 8 bits of LED current adjustment from 0 to I_{FULL_SCALE}. Both current sinks can be independently controlled via two separate full-scale current registers and two separate 8-bit brightness registers, or can be made to track together via a single brightness register.

8.2 Typical Application

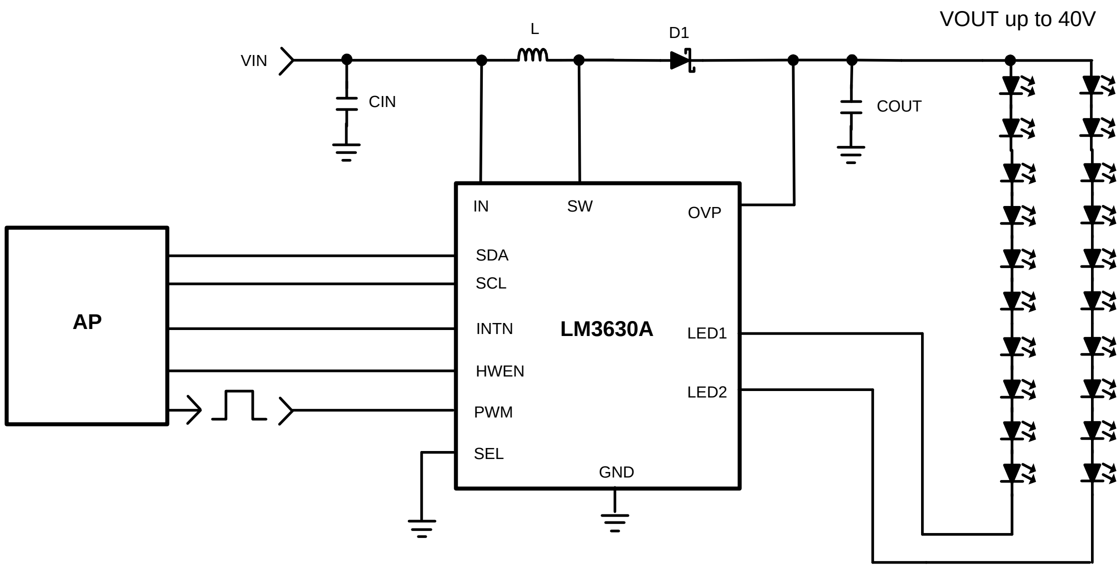


Figure 87. LM3630A Typical Application

8.2.1 Design Requirements

For typical white LED applications, use the parameters listed in Table 21.

Table 21. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Minimum input voltage	2.3 V
Minimum output voltage	V_{IN}
Output current	28.5 mA per channel
Switching frequency	500 kHz or 1 MHz

8.2.2 Detailed Design Procedure

8.2.2.1 Inductor Selection

The LM3630A is designed to work with a 10-µH to 22-µH inductor. When selecting the inductor, ensure that the saturation rating for the inductor is high enough to accommodate the peak inductor current. Equation 4 calculates the peak inductor current based upon LED current, V_{IN}, V_{OUT}, and efficiency.

$$I_{PEAK} = \frac{I_{LED}}{\eta} \times \frac{V_{OUT}}{V_{IN}} + \Delta I_L \tag{4}$$

where:

$$\Delta I_L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}} \tag{5}$$

When choosing L, the inductance value must also be large enough so that the peak inductor current is kept below the LM3630A device's switch current limit. This forces a lower limit on L given by Equation 6.

$$L > \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times f_{SW} \times V_{OUT} \times \left(I_{SW\_MAX} - \frac{I_{LED\_MAX} \times V_{OUT}}{\eta \times V_{IN}} \right)} \tag{6}$$

I_{SW_MAX} is given in *Electrical Characteristics*, efficiency (η) is shown in the*Typical Characteristics*, and f_{SW} is typically 500 kHz or 1 MHz.

Table 22. Inductors

MANUFACTURER	PART NUMBER	VALUE	SIZE	CURRENT RATING	DC RESISTANCE
TDK	VLF4014ST-100M1R0	10 µH	3.8 mm × 3.6 mm × 1.4 mm	1A	0.22 Ω
TDK	VLF302512MT-220M	22 µH	3 mm × 2.5 mm × 1.2 mm	0.43A	0.583 Ω

8.2.2.2 Maximum Power Output

The LM3630A device's maximum output power is governed by two factors: the peak current limit (I_{CL} = 1.2 A maximum), and the maximum output voltage (V_{OVP} = 40 V minimum). When the application causes either of these limits to be reached, it is possible that the proper current regulation and matching between LED current strings may not be met.

In the case of a peak current limited situation, when the peak of the inductor current hits the LM3630A device's current limit the NFET switch turns off for the remainder of the switching period. If this happens, each switching cycle the LM3630A begins to regulate the peak of the inductor current instead of the headroom across the current sinks. This can result in the dropout of the feedback-enabled current sinks and the current dropping below its programmed level.

The peak current in a boost converter is dependent on the value of the inductor, total LED current (I_{OUT}), the output voltage (V_{OUT}) (which is the highest voltage LED string + 0.3 V regulated headroom voltage), the input voltage V_{IN}, and the efficiency (Output Power/Input Power). Additionally, the peak current is different depending on whether the inductor current is continuous during the entire switching period (CCM) or discontinuous (DCM) where it goes to 0 before the switching period ends.

For CCM the peak inductor current is given by:

$$IPEAK = \frac{IOUT \times VOUT}{VIN \times efficiency} + \left[\frac{VIN}{2 \times fsw \times L} \times \left(1 - \frac{VIN \times efficiency}{VOUT} \right) \right] \tag{7}$$

For DCM the peak inductor current is given by:

$$IPEAK = \sqrt{\frac{2 \times IOUT}{fsw \times L \times efficiency} \times (VOUT - VIN \times efficiency)} \tag{8}$$

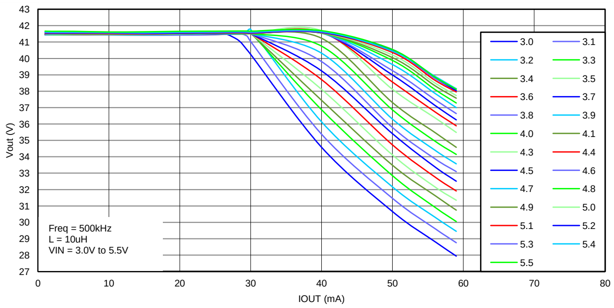
To determine which mode the circuit is operating in (CCM or DCM), a calculation must be done to test whether the inductor current ripple is less than the anticipated input current (I_{IN}). If ΔI_L is < I_{IN}, the device operates in CCM. If ΔI_L is > I_{IN} then the device is operating in DCM.

$$\frac{\text{IOUT x VOUT}}{\text{VIN x efficiency}} > \frac{\text{VIN}}{\text{fsw x L}} \text{ x } \left(1 - \frac{\text{VIN x efficiency}}{\text{VOUT}}\right) \tag{9}$$

Typically at currents high enough to reach the LM3630A device's peak current limit, the device is operating in CCM.

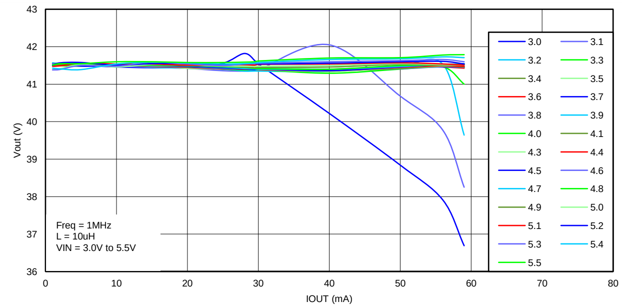
Application Curves show the output current and output voltage derating for a 10-µH and a 22-µH inductor, at switch frequencies of 500 kHz and 1 MHz. A 10-µH inductor is typically a smaller device with lower on resistance, but the peak currents are higher. A 22-µH inductor provides for lower peak currents, but to match the DC resistance of a 10 µH requires a larger-sized device.

8.2.3 Application Curves



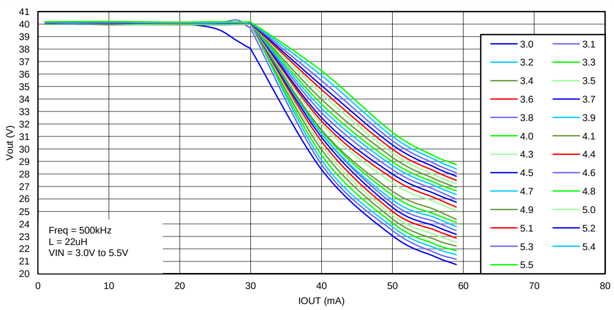
Frequency = 500 kHz   L = 10 µH

Figure 88. Maximum Boost Output Power vs V_{IN}



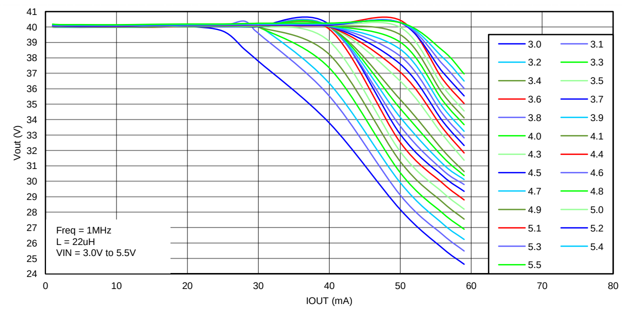
Frequency = 1 MHz   L = 10 µH

Figure 89. Maximum Boost Output Power vs V_{IN}



Frequency = 500 kHz   L = 22 µH

Figure 90. Maximum Boost Output Power vs V_{IN}



Frequency = 1 MHz   L = 22 µH

Figure 91. Maximum Boost Output Power vs V_{IN}

8.3 Initialization Setup

8.3.1 Recommended Initialization Sequence

The recommended initialization sequence for the device registers is as follows:

1. Set Filter Strength register (offset = 50h) to 03h.
2. Set Configuration register (offset = 01h) to enable the PWM and the feedback for Bank A; for example, writing 09h to the Configuration register, enables PWM and feedback for Bank A. Note the Bank B PWM and feedback need to be configured if Bank B is used, otherwise disable the Bank B feedback by clearing bit 4 and disable the Bank B PWM by clearing bit 1.
3. Configure the Boost Control register (offset = 02h) to select the OVP, OCP and FMODE. For example, writing 78h to the Boost Control register sets OVP to 40 V, OCP to 1.2 A and FMODE to 500 kHz.
4. Set the full scale LED current for Bank A and Bank B (if used), by writing to the Current A (offset = 05h), and Current B(offset = 06) registers. For example, writing 14h to the Current A register selects a full scale LED current of 20 mA for Bank A.
5. Set the PWM Sampler Hysteresis to 2 codes by setting Bit 7 of the Current A register. Set the PWM Sampler Lower Bound code to 6 by clearing Bit 6 of the Current A register. Note these settings apply to both Bank A and Bank B. If only Bank B is used, these setting are still necessary when PWM is enabled.
6. Select the current control and enable or disable the LED Bank A and/or B by writing to Control register(offset = 00h). For example, writing 14h to the Control register select linear current control and enables Bank A.
7. Set the LED brightness by writing to Brightness A (offset = 03h) and Brightness B (Offset = 04h) registers. For example, writing FFh to Brightness A sets the LED current to 20 mA, with the Current A register set to 14h, and the PWM input is high.

9 Power Supply Recommendations

The LM3630A operates from a 2.3-V to 5.5-V input voltage. The boost switching frequency is programmable at 500 kHz for low switching loss performance or 1 MHz to allow the use of tiny low-profile inductors. This input supply must be well regulated and provide the peak current required by the LED configuration and inductor selected.

10 Layout

10.1 Layout Guidelines

The LM3630A contains an inductive boost converter which detects a high switched voltage (up to 40 V) at the SW pin, and a step current (up to 900 mA) through the Schottky diode and output capacitor each switching cycle. The high switching voltage can create interference into nearby nodes due to electric field coupling (I = CdV/dt). The large step current through the diode and the output capacitor can cause a large voltage spike at the SW pin and the OVP pin due to parasitic inductance in the step current conducting path (V = Ldi/dt). Board layout guidelines are geared towards minimizing this electric field coupling and conducted noise. Figure 92 highlights these two noise generating components.

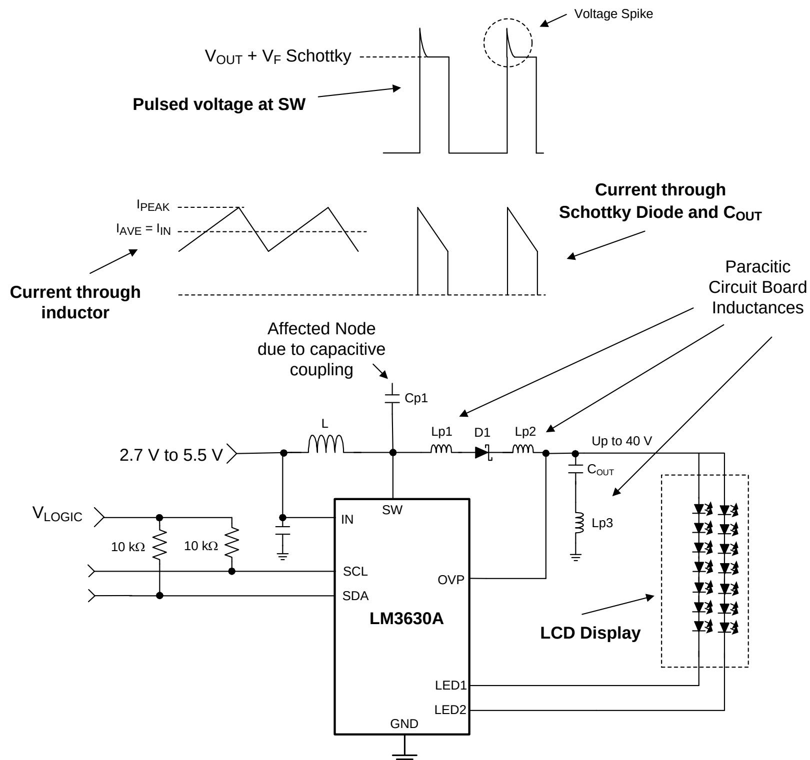


Figure 92. LM3630A Boost Converter Showing Pulsed Voltage At SW (High Dv/Dt) and Current Through Schottky and C_{OUT} (High Di/Dt)

The following lists the main (layout sensitive) areas of the LM3630A in order of decreasing importance:

- Output Capacitor
  - Schottky Cathode to C_{OUT}+
  - C_{OUT}– to GND
- Schottky Diode
  - SW Pin to Schottky Anode
  - Schottky Cathode to C_{OUT}+
- Inductor
  - SW Node PCB capacitance to other traces
- Input Capacitor
  - C_{IN}+ to IN pin
  - C_{IN}– to GND

Layout Guidelines (continued)

10.1.1 Output Capacitor Placement

The output capacitor is in the path of the inductor current discharge path. As a result C_{OUT} detects a high current step from 0 to I_{PEAK} each time the switch turns off and the Schottky diode turns on. Any inductance along this series path from the cathode of the diode through C_{OUT} and back into the LM3630A GND pin will contribute to voltage spikes ($V_{SPIKE} = L_{P\_} \times dI/dt$) at SW and OUT which can potentially overvoltage the SW pin, or feed through to GND. To avoid this, C_{OUT}+ must be connected as close as possible to the Cathode of the Schottky diode and C_{OUT}– must be connected as close as possible to the device GND bump. The best placement for C_{OUT} is on the same layer as the LM3630A so as to avoid any vias that can add excessive series inductance (see Figure 94).

10.1.2 Schottky Diode Placement

The Schottky diode is in the path of the inductor current discharge. As a result the Schottky diode detects a high current step from 0 to I_{PEAK} each time the switch turns off and the diode turns on. Any inductance in series with the diode will cause a voltage spike ($V_{SPIKE} = L_{P\_} \times dI/dt$) at SW and OUT which can potentially overvoltage the SW pin, or feed through to V_{OUT} and through the output capacitor and into GND. Connecting the anode of the diode as close as possible to the SW pin and the cathode of the diode as close as possible to C_{OUT}+ will reduce the inductance ($L_{P\_}$) and minimize these voltage spikes (see Figure 94).

10.1.3 Inductor Placement

The node where the inductor connects to the LM3630A SW bump has 2 issues. First, a large switched voltage (0 to $V_{OUT} + V_{F\_SCHOTTKY}$) appears on this node every switching cycle. This switched voltage can be capacitively coupled into nearby nodes. Second, there is a relatively large current (input current) on the traces connecting the input supply to the inductor and connecting the inductor to the SW bump. Any resistance in this path can cause large voltage drops that will negatively affect efficiency.

To reduce the capacitively coupled signal from SW into nearby traces, the SW bump to inductor connection must be minimized in area. This limits the PCB capacitance from SW to other traces. Additionally, the other traces need to be routed away from SW and not directly beneath. This is especially true for high impedance nodes that are more susceptible to capacitive coupling such as (SCL, SDA, HWEN, PWM, and possibly ASL1 and ALS2). A GND plane placed directly below SW will dramatically reduce the capacitive coupling from SW into nearby traces

To limit the trace resistance of the VBATT to inductor connection and from the inductor to SW connection, use short, wide traces (see Figure 94).

10.1.4 Input Capacitor Selection and Placement

The input bypass capacitor filters the inductor current ripple, and the internal MOSFET driver currents during turnon of the power switch.

The driver current requirement can range from 50 mA at 2.7 V to over 200 mA at 5.5 V with fast durations of approximately 10 ns to 20 ns. This will appear as high di/dt current pulses coming from the input capacitor each time the switch turns on. Close placement of the input capacitor to the IN pin and to the GND pin is critical since any series inductance between IN and C_{IN}+ or C_{IN}– and GND can create voltage spikes that could appear on the V_{IN} supply line and in the GND plane.

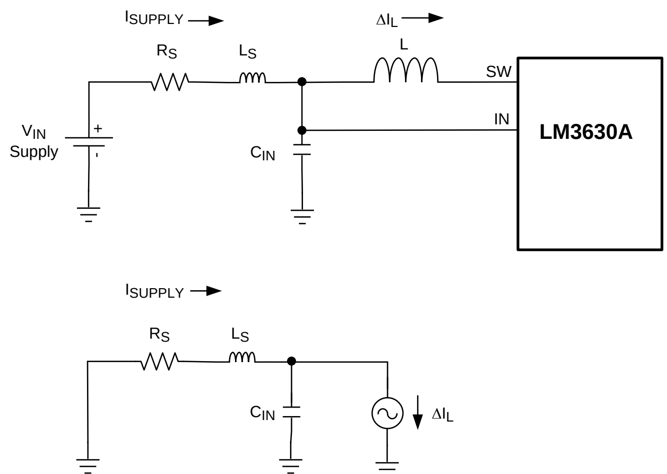
Close placement of the input bypass capacitor at the input side of the inductor is also critical. The source impedance (inductance and resistance) from the input supply, along with the input capacitor of the LM3630A, form a series RLC circuit. If the output resistance from the source (R_S) is low enough the circuit will be underdamped and will have a resonant frequency (typically the case). Depending on the size of L_S the resonant frequency could occur below, close to, or above switching frequency of the device. This can cause the supply current ripple to be:

1. Approximately equal to the inductor current ripple when the resonant frequency occurs well above the LM3630A switching frequency;
2. Greater then the inductor current ripple when the resonant frequency occurs near the switching frequency; and
3. Less then the inductor current ripple when the resonant frequency occurs well below the switching frequency.

Layout Guidelines (continued)

Figure 93 shows the series RLC circuit formed from the output impedance of the supply and the input capacitor. The circuit is re-drawn for the AC case where the V_{IN} supply is replaced with a short to GND and the LM3630A plus inductor is replaced with a current source (ΔI_L). In Figure 93, equation 1 is the criteria for an underdamped response, equation 2 is the resonant frequency, and equation 3 is the approximated supply current ripple as a function of L_S, R_S, and C_{IN}.

As an example, consider a 3.6-V supply with 0.1-Ω of series resistance connected to C_{IN} through 50 nH of connecting traces. This results in an underdamped input filter circuit with a resonant frequency of 712 kHz. Since the switching frequency lies near to the resonant frequency of the input RLC network, the supply current is probably larger then the inductor current ripple. In this case using equation 2 from Figure 93 the supply current ripple can be approximated as 1.68 multiplied by the inductor current ripple. Increasing the series inductance (L_S) to 500 nH causes the resonant frequency to move to around 225 kHz and the supple current ripple to be approximately 0.25 multiplied by the inductor current ripple.



1. $$\frac{1}{L_S \times C_{IN}} > \frac{R_S^2}{4 \times L_S^2}$$

2. $$f_{RESONANT} = \frac{1}{2\pi\sqrt{L_S \times C_{IN}}}$$

3. $$I_{SUPPLYRIPPLE} \approx \Delta I_L \times \frac{\dfrac{1}{2\pi \times 500\ \text{kHz} \times C_{IN}}}{\sqrt{R_S^2 + \left(2\pi \times 500\ \text{kHz} \times L_S - \dfrac{1}{2\pi \times 500\ \text{kHz} \times C_{IN}}\right)^2}}$$

Figure 93. Input RLC Network

10.2 Layout Example

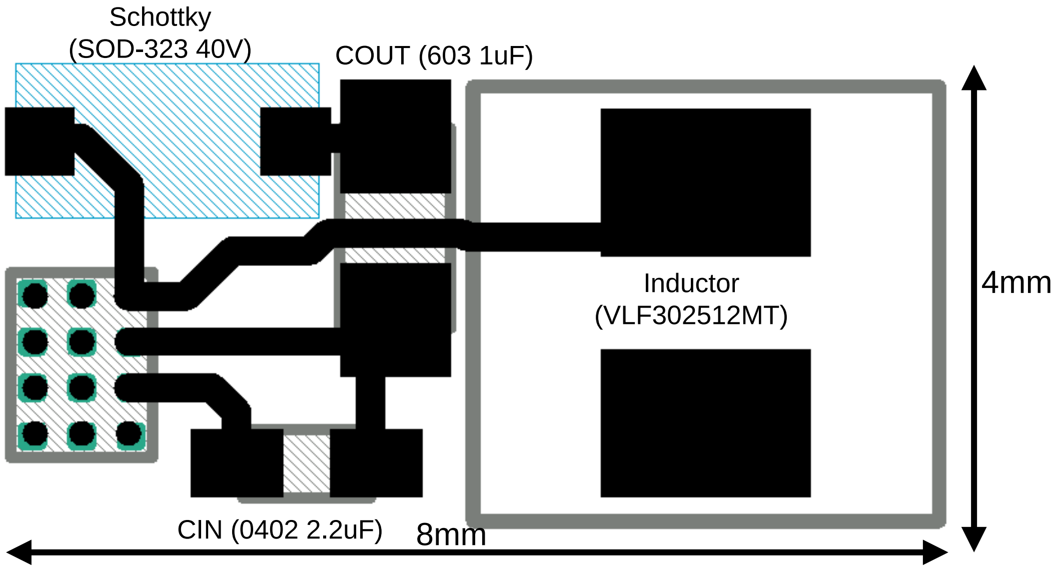


Figure 94. Typical LP3630A PCB Layout (2 × 10 Led Application)

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Documentation Support

11.2.1 Related Documentation

For additional information, see the following:

Texas Instruments Application Note 1112: *DSBGA Wafer Level Chip Scale Package* (SNVA009).

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3630ATME	ACTIVE	DSBGA	YFQ	12	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	D6	Samples
LM3630ATMX	ACTIVE	DSBGA	YFQ	12	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	D6	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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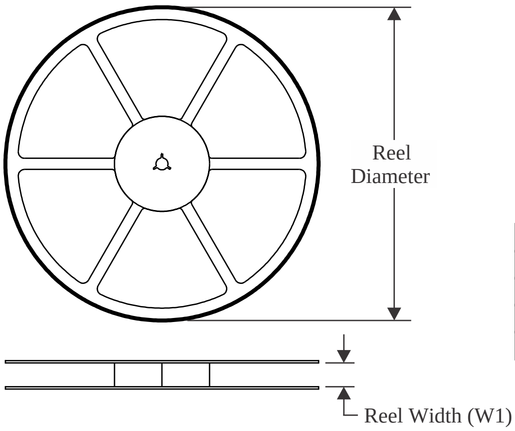
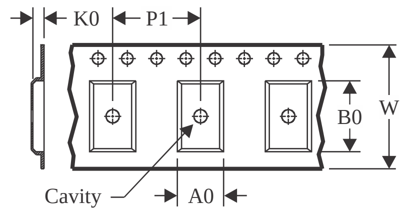
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

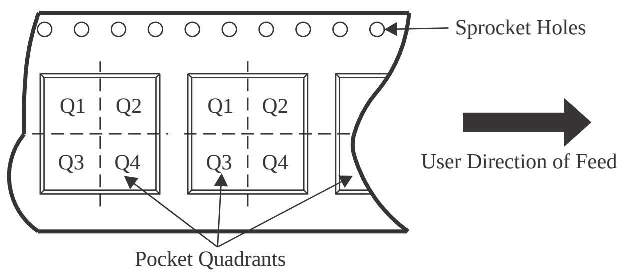


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

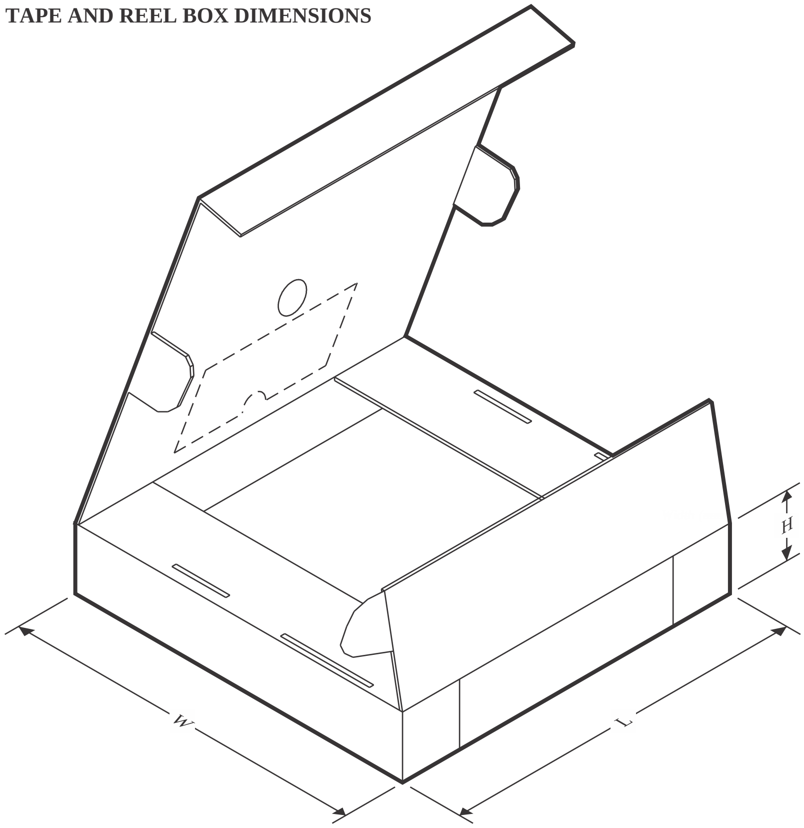
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

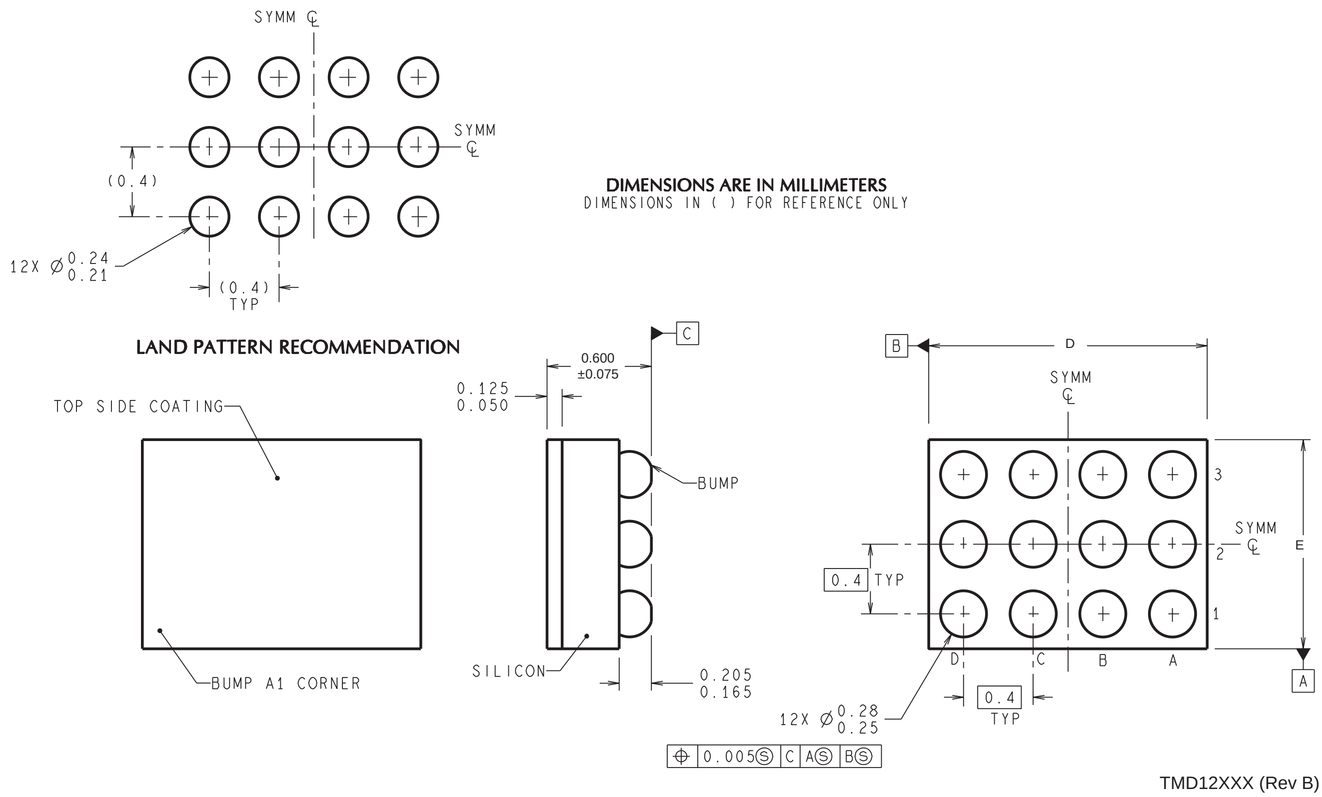
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3630ATME	DSBGA	YFQ	12	250	178.0	8.4	1.52	2.04	0.76	4.0	8.0	Q1
LM3630ATMX	DSBGA	YFQ	12	3000	178.0	8.4	1.52	2.04	0.76	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3630ATME	DSBGA	YFQ	12	250	208.0	191.0	35.0
LM3630ATMX	DSBGA	YFQ	12	3000	208.0	191.0	35.0



D: Max = 1.94 mm, Min = 1.88 mm

E: Max = 1.42 mm, Min = 1.36 mm

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NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.